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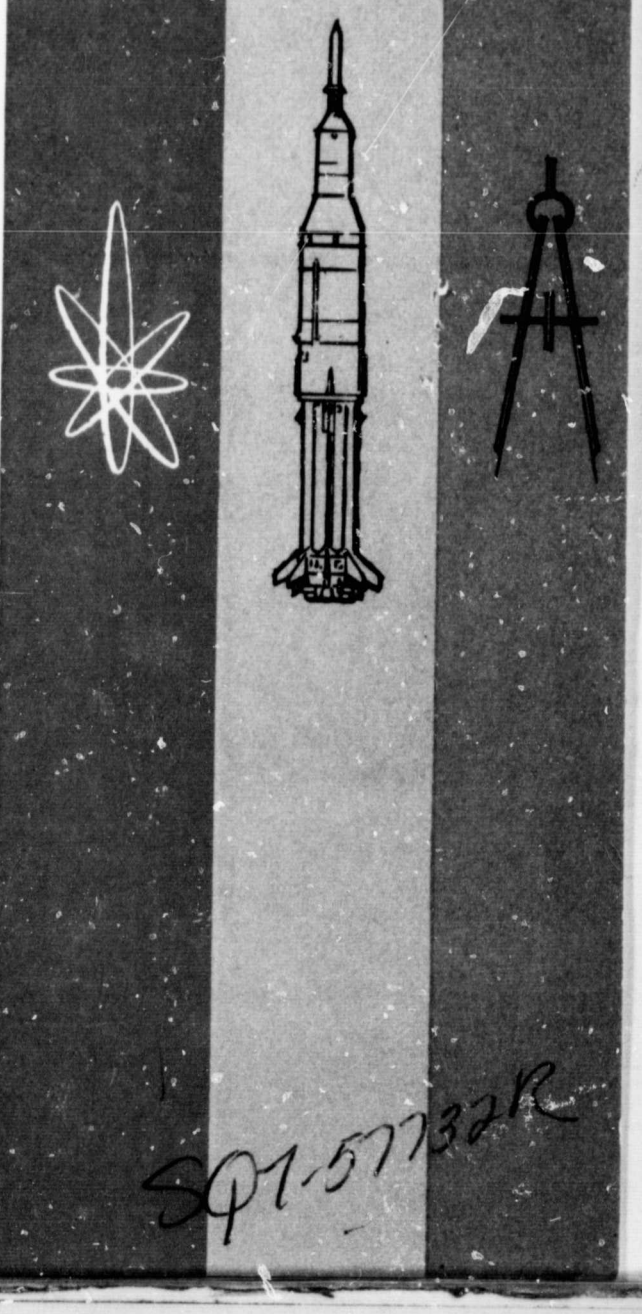
TECHNICAL MEMORANDUM HEE-M17-68

FEBRUARY 16, 1968

A STUDY OF TRUE PRODUCT MODULATORS PHASE III FINAL REPORT

SPACE DIVISION CHRYSLER CORPORATION

HUNTSVILLE OPERATIONS



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TECHNICAL MEMORANDUM HEE-M17-68
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A STUDY OF TRUE PRODUCT MODULATORS

PHASE III

FINAL REPORT

by

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ELECTRICAL AND ELECTRONIC

ENGINEERING DEPARTMENT

Prepared For

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HUNTSVILLE, ALABAMA 35812

Under
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SPACE DIVISION CHRYSLER CORPORATION
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ABSTRACT

This report concludes the third and final phase of a study of true product modulators. Complete results of the study are summarized, but the largest portion of the report involves the description, design, development, and test of a field effect transistor (FET) true product modulator. The modulator concept is based on the variable channel conductance characteristic of the FET.

This modulator dissipates very little power, is small and lightweight, and exhibits commendable performance at room temperature.

An electrical breadboard model of the modulator was constructed and evaluated in Chrysler laboratories. Commendable modulator performance is exhibited at room temperature but degradation is apparent at higher or lower temperatures. Therefore, it is concluded that this modulator is suitable for use in ground based telemetry applications, but resolution of thermal deficiencies is necessary before it can be utilized in an aerospace environment.

This report was prepared under contract NAS8-21198 with the George C. Marshall Space Flight Center, Huntsville, Alabama.

INTRODUCTION

This report, which was prepared under contract NAS8-21198 with the George George C. Marshall Space Flight Center, concludes the third and final phase of a study of true product modulators. During this phase a true product modulator concept based on the variable channel conductance characteristic of the field effect transistor (FET) was investigated. This modulator is small and lightweight, and dissipates very little power. The device functions commendably on the ground and, subject to the resolution of particular thermal conditions, should function adequately in an aerospace environment. An electrical breadboard model of the FET modulator was constructed and evaluated in Chrysler laboratories. This report includes a discussion of functional theory, circuit performance and conclusions.

The complete study of true product modulators was divided into three phases. Various true product modulator techniques were studied and a survey of the industry for available true product modulators was conducted. Phase II involved evaluation in Chrysler laboratories of particular true product modulators. This evaluation appears in Chrysler Memorandum HEE-M104-67. The conclusion was made that the Ohio Semitronics, Inc. Model MC-521 and the F. W. Bell, Inc. Model HM-4050 multipliers are not practical for use in the aerospace environment due to high input power requirements but possibly can be utilized in ground based telemetry applications. This possibility is primarily contingent on elimination of certain undesirable features.

The limited versatility of the Ohio Semitronics, Inc. and F. W. Bell, Inc. modulators led to investigation and development of the FET true product modulator described in the first paragraph above.

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I. FET TRUE PRODUCT MODULATOR CONCEPT

A. GENERAL

A true product modulator is a multiplier which provides at its output terminal the instantaneous product of two input functions. Among modulators or multipliers of this type are servo multipliers, Hall-effect multipliers, and magnetoresistor modulators. Unfortunately these devices exhibit certain undesirable features. The servo multiplier is limited to low frequency applications, whereas high input drive power is a particular disadvantage of the Hall-effect and magnetoresistor units. A modulator which has neither of these disadvantages is a field-effect transistor (FET) modulator. This modulator requires minimum power and is theoretically suitable for use in communication system applications.

B. FUNCTIONAL THEORY

The FET true product modulator concept is based on the variable channel conductance property of the FET. If the transistor is operated in the region where V_{DG}, drain to gate voltage, is less than V_P, pinch-off voltage, the channel conductance can be varied or modulated by V_{GS}, gate to source voltage. This relationship is approximately linear for either a positive or negative V_{DS}, drain to source voltage, if this voltage does not disturb the depletion region set up by gate bias.[1] This requirement means that the magnitude of V_{DS} must be small or approximately 100 millivolts.[2]

Shockley[3] has shown that channel conductance for the case of zero drain to source voltage V_{DS} should obey the relation

$$G_{DS} = \left[G_0\right]\left[1 - \left(\frac{V_{GS}}{V_P}\right)^{1/2}\right] \qquad (1)$$

where

G_{DS} is the channel conductance

G_0 is the value of G_{DS} when V_{GS} is zero

However, in practice the FET approximately behaves according to the following expression.[4]

$$G_{DS} = \left[G_0\right]\left[1 - \frac{V_{GS}}{V_P}\right] \qquad (2)$$

A more exact expression for G_{DS} includes higher order terms but for the present discussion the assumption will be that equation (2) fully describes the transistor channel conductance.

The variable channel conductance property is employed in the simplified model of an FET true product modulator shown in figure I-1. If it is assumed

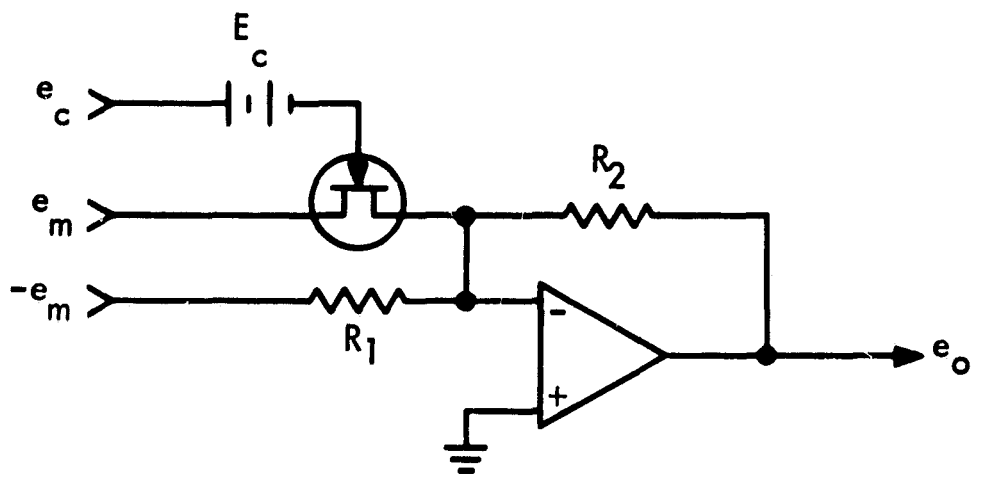

FIGURE I-1. A SIMPLIFIED MODEL OF AN FET TRUE PRODUCT MODULATOR

that the source impedance of each input signal is zero; the operational is ideal; FET drain current is linearly proportional to drain to source voltage; and FET gate to source capacitance is zero, the output voltage expression for this modulator is

$$e_0 = \left[R_2\right]\left[\frac{1}{R_1} - G_{DS}\right]\left[e_m\right] \tag{3}$$

After substituting equation (2) into (3) for G_{DS}

$$e_0 = \left[R_2\right]\left[\frac{1}{R_1} - \left(G_0\right)\left(1 - \frac{V_{GS}}{V_P}\right)\right]\left[e_m\right] \tag{4}$$

From figure I-1 it is apparent that

$$V_{GS} = e_c - E_c \tag{5}$$

Making this substitution

$$e_0 = \left[R_2\right]\left[\frac{1}{R_1} - G_0\left(1 - \frac{e_c - E_c}{V_P}\right)\right]\left[e_m\right] \tag{6}$$

Rearranging

$$e_0 = \left\{\frac{R_2 G_0}{V_P}\right\}\left\{e_m e_c\right\} + \left\{\left[R_2\right]\left[\frac{1}{R_1} - G_0\left(\frac{V_P + E_c}{V_P}\right)\right]\right\}\left\{e_m\right\} \tag{6}$$

This equation is the sum of two terms. One term is the product of input voltages e_m and e_c while the other is a function of e_m alone. Note that this expression will reduce to the desired true product

$$e_0 = \left[\frac{R_2 G_0}{V_P}\right]\left[e_m e_c\right] \tag{7}$$

if

$$\frac{1}{R_1} = \left[G_0\right]\left[\frac{V_P + E_c}{V_P}\right] \tag{8}$$

Unfortunately equation (7) does not correspond to reality. Recall that the derivation of this expression is based on the assumptions of zero source impedances, a linear FET, and an ideal operational amplifier. FET and operational amplifier limitations must be taken into consideration before an optimum modulator can be designed. Excessive amplifier offset voltage and offset current will affect accuracy for all input signal frequencies. The amplifier gain-bandwidth product and phase shift are factors that limit high frequency performance.

One of the more important modulator design considerations is the fact that the FET is not truly linear. A more exact expression for channel conductance is[5]

$$G_{DS} = \left[G_0\right]\left[1 + A_1 V_{GS} + A_2 V_{GS}^2\right] \tag{9}$$

Also the transistor drain current is given by the expression[6]

$$I_D = \left[G_{DS}\right]\left[V_{DS} + B V_{DS}^2\right] \tag{10}$$

Earlier it was assumed that transistor gate to source capacitance is zero. In reality finite capacitance does exist and will affect high frequency performance.

With the knowledge of amplifier and FET limitations in mind but still assuming zero source impedances, a more exact expression for the modulator output voltage of figure I.1 can be written. First, low frequency performance will be considered. For this case the output voltage expression is

$$e_0 = \left[R_2\right]\left[I_R - I_D\right] + \left[\frac{R_1 + R_2}{R_1}\right]\left[E_R\right] \tag{11}$$

where

I_R is the amplifier input current

E_R is the amplifier offset voltage

Now the FET drain to source voltage is given by

$$V_{DS} = e_m + E_R \tag{12}$$

When equations (5) and (9) through (12) are combined the output voltage expression becomes

$$e_0 = I_R R_2 + \left\{\frac{R_1 + R_2}{R_1}\right\}\left\{E_R\right\} + \left\{\frac{R_2}{R_1}\right\}\left\{e_m\right\}$$

$$- \left|R_2 G_0\right| \left|e_m + E_R\right| \left|1 + A_1\left(e_c - E_c\right) + A_2\left(e_c - E_c\right)^2\right|$$

$$- \left|R_2 G_0\right| \left|B\left(e_m + E_R\right)^2\right| \left|1 + A_1\left(e_c - E_c\right) + A_2\left(e_c - E_c\right)^2\right| \tag{13}$$

After rearranging terms

$$e_0 = - \left\{\left[R_2 G_0\right]\left[A_1 - 2A_2 E_c\right]\right\}\left\{e_m e_c\right\}$$

$$+ \left\{\left[R_2\right]\left[\frac{1}{R_1} - G_0\left(1 - A_1 E_c + A_2 E_c^{\,2}\right)\left(1 + 2BE_R\right)\right]\right\}\left\{e_m\right\}$$

$$- \left\{\left[R_2 G_0\right]\left[A_1 - 2A_2 E_c\right]\right\}\left\{E_R + B\left(e_m + E_R\right)^2\right\}\left\{e_c\right\}$$

$$- \left\{R_2 G_0 A_2\right\}\left\{e_m + E_R + B\left(e_m + E_R\right)^2\right\}\left\{e_c^{\,2}\right\}$$

$$+ \left\{\left[\frac{R_1 + R_2}{R_1}\right] - \left[R_2 G_0\right]\left[1 - A_1 E_c + A_2 E_c^{\,2}\right]\left[1 + BE_R\right]\right\}\left\{E_R\right\} + I_R R_2$$

$$- \left\{\left[R_2 G_0 B\right]\left[1 - A_1 E_c + A_2 E_c^{\,2}\right]\right\}\left\{e_m^{\,2}\right\} \tag{13}$$

It is evident that this expression includes the desired product of input signals e_m and e_c in addition to many unwanted terms. Contributions to error caused by most of the undesirable terms is either small or can be reduced to zero if particular resistors are properly chosen.

The first term in equation (13) is the product of e_m and e_c. Note that the coefficient of e_m in the second term will equal zero for a particular value of resistor R_1. For reasonable accuracy error resulting from terms involving amplifier offset voltages and currents can be neglected. If extreme accuracy is desired, however, this error can be reduced to zero if resistors R_1 and R_2 are chosen correctly. For low level input signals (less than 100 millivolts) error resulting from the remaining terms with one exception will be small. This exception is the last term of equation (13) which involves the square of e_m.

Assuming that resistors R_1 and R_2 have been chosen properly and neglecting terms that contribute minimal error, the expression for the modulator output voltage of figure I-1 becomes

$$e_0 = -\left\{\left[R_2G_0\right]\left[A_1 - 2A_2E_c\right]\right\}\left\{e_m e_c\right\} - \left\{\left[R_2G_0B\right]\left[1 - A_1E_c + A_2E_c^2\right]\right\}\left\{e_m^2\right\} \qquad (14)$$

For optimum results the undesirable term must at best be removed, but at least minimized in magnitude. Fortunately it is possible to remove this term completely but at the expense of additional circuitry. This is done in the actual FET true product modulator model of figure I-2.

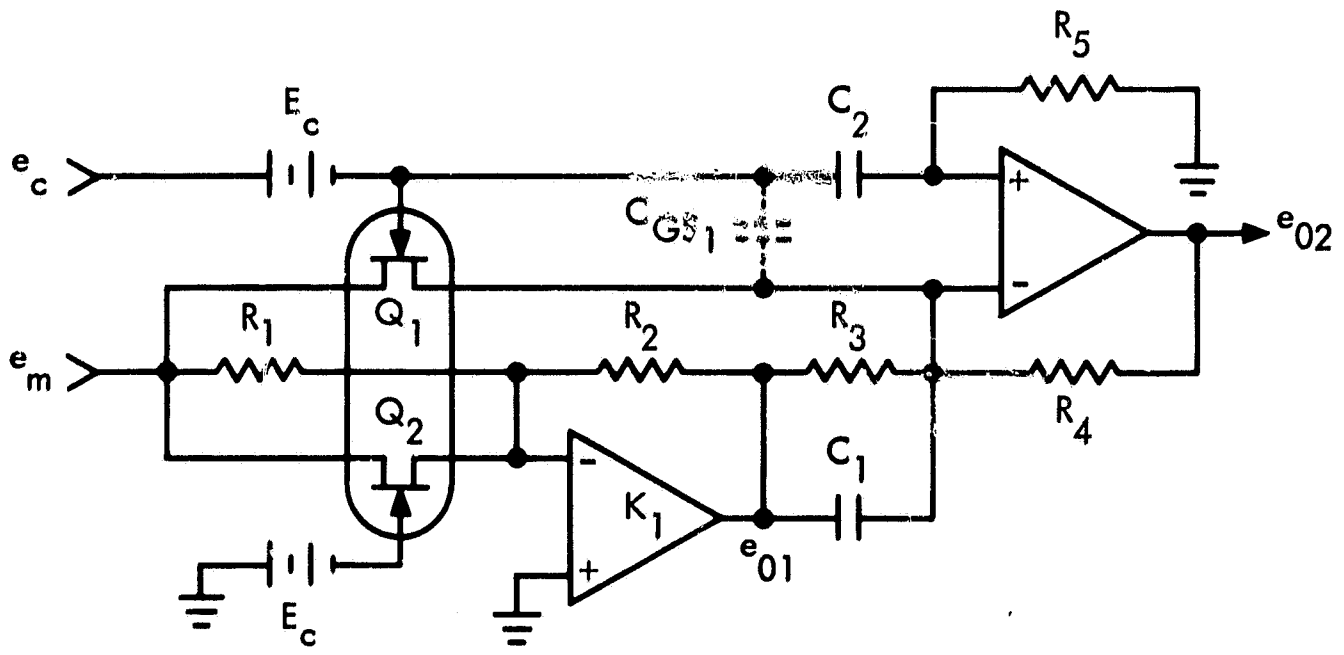

FIGURE I-2. ACTUAL FET TRUE PRODUCT MODULATOR MODEL

Analgous to dc error caused by the operational amplifier in the simplified modulator of figure I-1, dc error resulting from operational amplifiers in the actual modulator is small and can also be reduced to zero very easily. Therefore, in the following discussion this error will be neglected. For simplicity other terms that contribute minimal error will be neglected also. On this basis the following equations are legitimate. Referring to figure I-2 the output expression for amplifier K_1 is

$$e_{01} = -\left\{\left[R_2G_{02}\right]\left[1 - A_3E_c + A_4E_c^{\,2}\right]\right\}\left\{e_m + B_1e_m^{\,2}\right\} - \left\{\frac{R_2}{R_1}\right\}\left\{e_m\right\} \qquad (15)$$

and the output voltage for the complete modulator is

$$e_{02} = -\left\{\left[R_4G_{01}\right]\left[A_1 - 2A_2E_c\right]\right\}\left\{e_me_c\right\}$$
$$-\left\{\left[R_4G_{01}\right]\left[1 - A_1E_c + A_2E_c^{\,2}\right]\right\}\left\{e_m + B_2e_m^{\,2}\right\} - \left\{\frac{R_4}{R_3}\right\}\left\{e_{01}\right\} \qquad (16)$$

After substituting equation (15) into (16) and rearranging terms

$$e_{02} = -\left\{\left[R_4G_{01}\right]\left[A_1 - 2A_2E_c\right]\right\}\left\{e_me_c\right\}$$
$$+\left\{\left[\frac{R_2R_4G_{02}}{R_3}\right]\left[1 - A_3E_c + A_4E_c^{\,2}\right]\right.$$
$$\left. - \left[R_4G_{01}\right]\left[1 - A_1E_c + A_2E_c^{\,2}\right] + \frac{R_2R_4}{R_1R_3}\right\}\left\{e_m\right\}$$
$$+\left\{\left[\frac{R_2R_4G_{02}B_1}{R_3}\right]\left[1 - A_3E_c + A_4E_c^{\,2}\right]\right.$$
$$\left. - \left[R_4G_{01}B_2\right]\left[1 - A_1E_c + A_2E_c^{\,2}\right]\right\}\left\{e_m^{\,2}\right\} \qquad (17)$$

Observe that particular resistor values will eliminate undesirable terms in equation (17). When this is done the desired product for dc or low frequency input signals results. This is expressed by the following equation.

$$e_0 = -\left\{\left[R_2G_{01}\right]\left[A_1 - A_2E_c\right]\right\}\left\{e_me_c\right\} \qquad (18)$$

Returning to equation (17) briefly, it is noteworthy that resistor R_1 is unnecessary if transistors Q_1 and Q_2 have identical characteristics. Very likely, however, it would be too costly to select transistors with the same characteristics, although matched transistors are commercially available that have similar characteristics. Now consider high frequency performance. For this case recall that the amplifier gain-bandwidth product and phase shift, and the FET gate to source capacitance are factors that must be taken into account. Otherwise the output signal will be shifted in phase. Also the modulation input signal, the square of this signal, and the carrier input signal will all appear as attenuated components of the output signal in addition to the desired product of e_m and e_c. At higher modulator and carrier signal frequencies, the magnitude of these undesirable components is significant.

Capacitors C_1 and C_2 are included in the actual true product modulator of figure I-2 to eliminate these component frequencies from the output signal frequency spectrum. How this is accomplished will become evident from the following discussion which is based on the assumption that these same capacitors have not been included in the modulator circuit. For the moment it will also be assumed that the open loop voltage gain of each amplifier is independent of frequency. For these conditions the modulator output voltage expression is:

$$
\begin{aligned}
e_0 = &- \left\{\left[R_4G_{01}\right]\left[A_1 - 2A_2E_c\right]\left[\underline{/\theta_{m1} + \theta_{m2} + \theta_c}\right]\right\}\left\{e_m e_c\right\} \\
&+ \left\{\left[\frac{R_2R_4G_{02}}{R_3}\right]\left[1 - A_3E_c + A_4E_c^{\,2}\right]\left[\underline{/\theta_{m1} + \theta_{m2}}\right]\right. \\
&\left. - \left[R_4G_{01}\right]\left[1 - A_1E_c + A_2E_c^{\,2}\right]\left[\underline{/\theta_{m2}}\right] + \left[\frac{R_2R_4}{R_1R_3}\right]\left[\underline{/\theta_{m1} + \theta_{m2}}\right]\right\}\left\{e_m\right\} \\
&+ \left\{\left[\frac{R_2R_4G_{01}B_1}{R_3}\right]\left[1 - A_3E_c + A_4E_c^{\,2}\right]\left[\underline{/2\theta_{m1} + 2\theta_{m2}}\right]\right. \\
&\left. - \left[R_4G_{01}\right]\left[1 - A_1E_c + A_2E_c^{\,2}\right]\left[\underline{/2\theta_{m2}}\right]\right\}\left\{e_m^{\,2}\right\} \\
&+ \left\{\frac{R_4}{X_{GS1}}\underline{/90^o}\right\}\left\{e_c\right\}
\end{aligned}
\tag{19}
$$

where

θ_{m1} is the phase shift through amplifier K_1 at frequency f_m.

θ_{m2} is the phase shift through amplifier K_2 at frequency f_m.

θ_c is the phase shift through amplifier K_2 at frequency f_c.

X_{GS} is the reactance of the gate to source capacitance of transistor Q_1 at frequency f_c.

Now consider the terms involving e_m and the square of e_m. Note that the coefficient of each term is the difference of a pair of vectors that are not in phase. Therefore, with the exception of a dc input signal, these terms will always be present; even for the special case of transistors with identical characteristics. Although phase angles θ_{m1} and θ_{m2} are quite small if good amplifiers are used, the magnitude of these components is significant, especially at the highest modulating frequency. This results from the fact that the magnitude of each vector comprising the coefficient of e_m and the square of e_m is much larger than the coefficient in the desired true product term. This means that the slightest phase separation between the vectors of each coefficient causes a large difference in magnitude when compared to the coefficient of the true product term. Therefore, some means must be provided to ensure that the phase separation is zero, regardless of the modulation signal frequency. This is accomplished with capacitor C_1.

The phase shift θ_{m1} through amplifier K_1 corresponds to a phase lag. Capacitor C_1 in conjunction with resistors R_3 and R_4 introduces a phase lead equal in magnitude to θ_{m1} so that vectors comprising the coefficient of e_m are in phase. This is also true for vectors comprising the coefficient of the square of e_m. Therefore, proper choice of capacitor C_1 for high frequency operation and resistors R_1 and R_2 for both high and low input signal frequencies will eliminate terms involving e_m and the square of e_m for all modulation frequencies.

Returning to equation (19) observe another undesirable term which involves e_c, the carrier signal. This term does not appear in the low frequency modulator output signal expression (18). Earlier it was stated that small but finite capacitance exists between gate and source of each FET. Capacitance C_{GS}, of transistor Q_1 in figure I-2 is connected to the inverting terminal of amplifier K_2 and provides a path for carrier signal current at higher carrier frequencies. This is unavoidable. However, compensation is provided by capacitor C_2 in the actual true product modulator of figure I-2. This capacitor provides a path for carrier signal current to the non-inverting terminal of amplifier K_2 which offsets the effect of carrier current at the inverting terminal. If the following expression is satisfied, carrier suppression is also complete.

$$\frac{R_5}{R_4} = \left[\frac{G_{GS1}}{C_2}\right]\left[\frac{R_3}{R_3(R_4G_{DS1} + 1) + R_4}\right] \qquad (20)$$

where

G_{DS1} is the channel conductance of transistor Q_1

C_{GS1} is the gate to source capacitance of transistor Q_1

Total carrier rejection does not occur since G_{DS1}, the channel conductance of transistor Q_1, is modulated by the carrier signal. This causes a very slight imbalance in equation (2) when the amplitude of the carrier is maximum.

Returning to equation (19) it is apparent that the product of input signals e_m and e_c does not occur instantaneously but is delayed in time. This corresponds to a total phase shift equal to the sum of θ_{m1}, θ_{m2}, and θ_c. Earlier it was stated that phase angles θ_{m1} and θ_{m2} are quite small, if good amplifiers are used. In many cases this slight phase shift can be neglected.

Phase angle θ_c which corresponds to frequency f_c may be significant at higher carrier frequencies. Nevertheless, the angle is very nearly linearly proportional to frequency if the amplifier loop gain or the difference between open loop and closed loop gain factors at the operating frequency is large.

The amplitude of the modulator output signal versus frequency plot is another consideration in the design of an optimum true product modulator. For optimum results this amplitude must be independent of frequency over the frequency range of each input signal. Recall that one of the assumptions on which equation (19) is based is that the open loop voltage gain of each amplifier is independent of frequency. In reality this gain factor is related to frequency by the gain-bandwidth product. This means the amplifier open loop gain is inversely proportional to frequency. Therefore, closed loop gain is reduced significantly for a high carrier frequency unless loop gain is again much larger than closed loop gain. The use of broadband amplifiers ensures that this condition is satisfied and that the modulator output signal amplitude versus frequency plot is flat.

Assuming amplifier open loop voltage gain and phase shift limitations have been taken into consideration and after the proper choice of resistor and capacitors has been made to eliminate undesirable terms in equation (19), the output voltage expression for the modulator of figure I-2 becomes

$$e_0 = \left\{\left[R_4 G_{01}\right]\left[A_1 - 2A_2 E_c\right]\left[\angle\theta_c\right]\right\}\left\{e_m e_c\right\} \qquad (21)$$

This equation represents the output signal for high frequency performance. In the derivation of equation (21) and preceeding equations it was assumed that the source impedance of e_m and of e_c is zero. In reality the impedance of each is finite but will contribute negligible error if it is much less than the modulator input impedance.

So far nothing has been said about modulator performance in the aerospace environment. The modulator output signal amplitude is dependent on the value of resistor R_4 and FET channel conductance. This conductance is sensitive to temperature variations. However, at a particular gate bias point,[7,8] the zero temperature coefficient point, channel conductance is constant, regardless of temperature. Therefore, according to theory, the modulator output signal amplitude will also be stable if both transistors in figure I-2 are biased at this point.

II. ELECTRICAL BREADBOARD

A. SCHEMATICS

Shown in figure II-1 is the complete electrical schematic for the FET true product modulator model of figure I-2. Pin connections for each operational amplifier used in the modulator breadboard are shown in figure II-2.

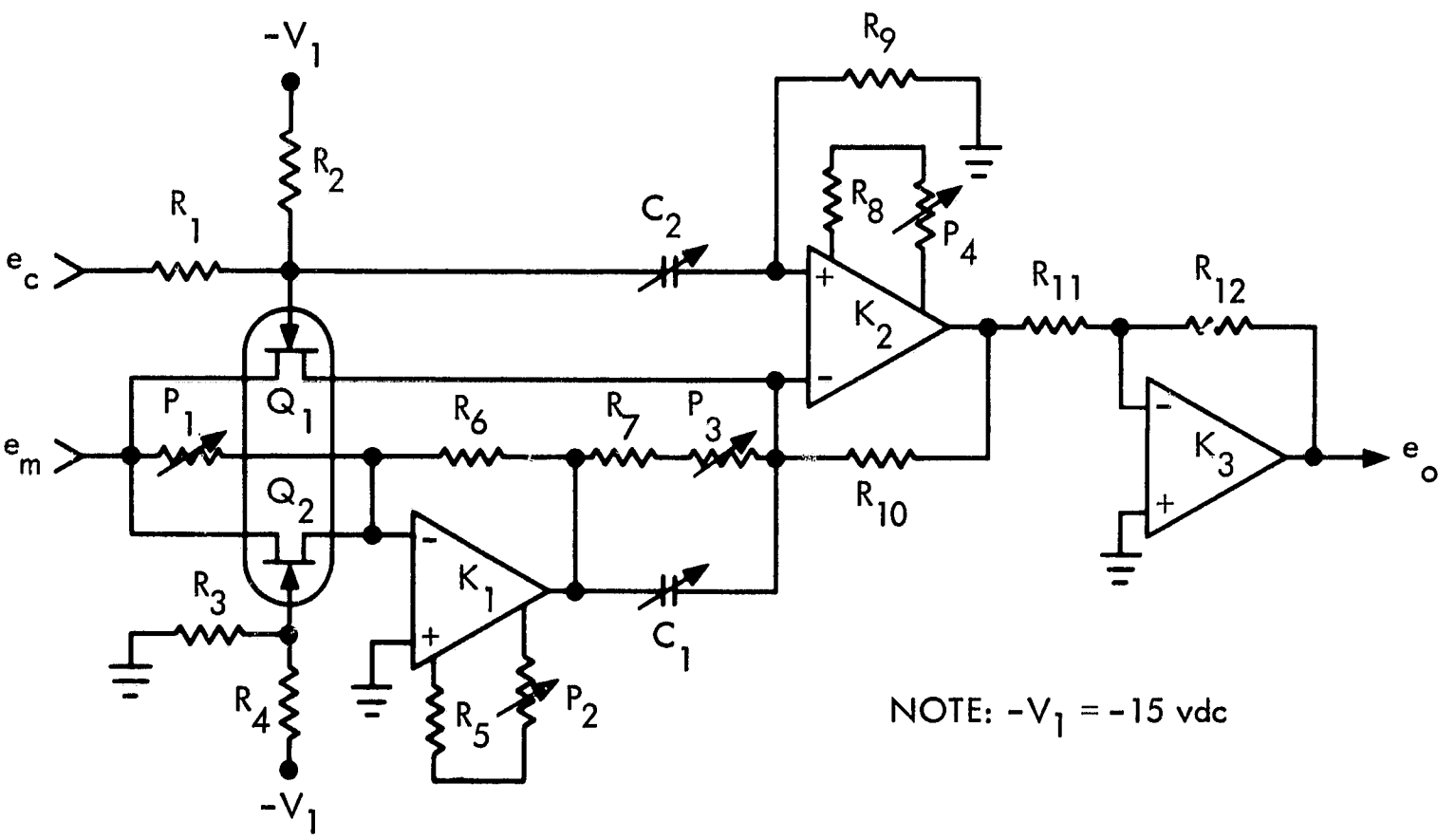

FIGURE II-1. FET TRUE PRODUCT MODULATOR ELECTRICAL SCHEMATIC

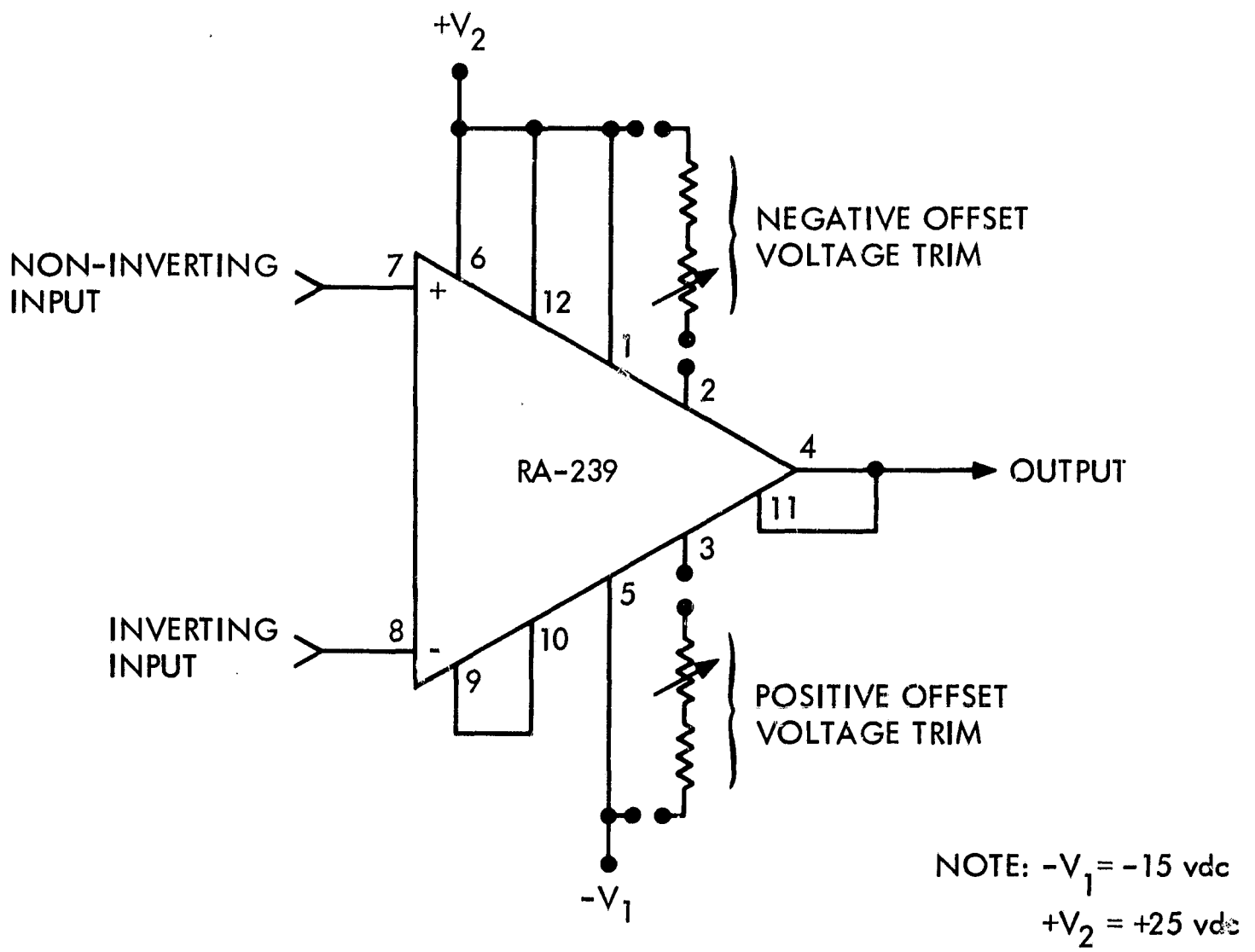

FIGURE II-2. OPERATIONAL AMPLIFIER PIN CONNECTIONS

B. PARTS LIST

The parts list for the FET true product modulator corresponds to the electrical schematic shown in figure II-1.

Operational Amplifiers

$K_1 = K_2 = K_3$ = RA-239

Transistors

$Q_1 = Q_2$ = 2N3955 Dual N-channel

Potentiometers*

P_1 = 100 kilohms
$P_2 = P_4$ = 50 kilohms
P_3 = 100 ohms

Capacitors*

$C_1 \cong$ 15 pf
$C_2 \cong$ 5 pf

Resistors

$R_1 = R_3$ = 1.27 kilohms 1/8 w 1%
$R_2 = R_4 = R_{10} = R_{12}$ = 23.7 kilohms 1/8 w 1%
$R_5 = R_8$ = 12 kilohms 1/8 w 10%
R_6 = 1000 ohms 1/8 w 1%
R_7 = 937 ohms 1/8 w 1%
*$R_9 \cong$ 390 ohms 1/8 w 10%
P_{11} = 1.5 kilohms 1/8 w 1%

*The exact value or setting for these components is determined according to the alignment procedure in section II.D.

C. BREADBOARD DESCRIPTION

The modulator breadboard differs slightly from the modulator concept described in section I.B. Observe that amplifier K_3 appears in the breadboard electrical schematic of figure II-1 but is not included in the modulator model shown in figure I-2. This amplifier was added for amplification only, and may not be required in a prototype or engineering model.

Recall, from the discussion of the modulator concept in section I.B, the statement that source impedances of input signals e_m and e_c must be much less than the modulator input impedance for optimum performance. For the laboratory evaluated breadboard the source impedance for each input signal, which is not necessarily the maximum allowable value, was set equal to ten ohms. Excessive source impedance will cause unacceptable distortion, but time limitations prevented determination of the maximum allowable impedance.

In the breadboard electrical schematic of figure II-1 the setting for each potentiometer and variable capacitor is a function of the particular operational amplifiers and FET pair employed in the modulator circuit. Each setting is determined according to the alignment procedure in section II.D. For an engineering model the potentiometers and variable capacitors may be replaced by fixed resistors and capacitors equivalent in value to potentiometer and variable capacitor settings, respectively.

The operational amplifier type used in the modulator breadboard is the Radiation, Inc. RA-239 broadband amplifier. This amplifier is designed for use over the full military temperature range ($-55^{o}C$ to $+125^{o}C$). Less expensive are the RA-339 and RA-539 amplifiers. If less than optimum performance can be tolerated, a significant cost reduction can be realized. The RA-339 will perform over the full temperature range but offset voltage and current does not quite compare with RA-239 specifications. However, an approximate 50% reduction in amplifier cost results, if the modulator multiplication error caused by the increased offset voltage and current can be tolerated.

A third modulator consideration is the use of the RA-539. The RA-539 is similar to the RA-239 and RA-339 but performance is limited to the temperature range of 0^{o} to $+75^{o}C$. An advantage, however, is the fact that it costs less than either the RA-239 or RA-339. Its cost is approximately one third the cost of the RA-239, which is the most expensive amplifier. Therefore, incorporation of the RA-539 into the modulator for use at room temperature should not alter performance significantly, but perhaps more important the modulator cost is reduced.

D. ALIGNMENT PROCEDURE

The FET true product modulator shown in figure II-1 provides the true product of e_m, the modulation input signal, and e_c, the carrier signal. The maximum amplitude and frequency range of each signal is defined below.

$\overline{e_m}$ = 50 mv rms $\qquad$ f_m = 0 to 3000 Hz

$\overline{e_c}$ = 50 mv rms $\qquad$ f_c = 0 to 125 kHz

For optimum modulator performance, particular components comprising the modulator require adjustment. Adjustments are made with a dc voltmeter, preferably a digital unit for accuracy, an rms voltmeter, a frequency selective voltmeter, and two signal generators.

Components requiring adjustment are potentiometers, variable capacitors, and resistor R_9 in figure II-1. Values of some of these components are interdependent. Therefore, the following sequence must be followed.

Resistor R_9

Resistor R_9 corresponds to resistor R_5 in the modulator model shown in section I.B equation (20) in the same section defines the relation of resistor R_5 to other components comprising the modulator model. From the expression that results when equation (20) is rewritten with component subscripts changed to conform to corresponding components in the modulator breadboard schematic shown in figure II-1, the value of R9 can be calculated. Equation (20) becomes

$$\frac{R_9}{R_{10}} = \frac{C_{GS1}}{C_2} \quad \frac{R_7 + P_3}{(R_7 + P_3)(R_{10}G_{DS1} + 1) + R_{10}} \tag{22}$$

C_{GS1}, not shown in figure II-1, is the gate to source capacitance of transistor Q_1 and G_{DS1} is the channel conductance of the same transistor.

Using the nominal value of C_{GS1} which appears on the transistor specification sheet; the measured value of G_{DS1} corresponding to the transistor gate bias point; and neglecting the resistance of potentiometer P_3 a relationship between resistor R_9 and capacitor C_2 results. Operational amplifier bias current flowing through R_9 causes a dc error voltage offset at the modulator output terminal. Therefore, R_9 should be as small as possible. With this in mind the value of R_9 may be chosen.

The choice of R_9 also determines the value of C_2. However, this is a nominal value. Recall that the resistance of potentiometer P_3 was neglected and that the nominal value of C_{GS1} was used in equation (22) above. In this equation the sum of resistance of potentiometer P_3 and resistor R_7 appears. The exact resistance setting for P_3, which will be determined later in the alignment procedure is small compared to R_7. Therefore, the value of C_2 determined above will not differ significantly from the exact value which will be determined later.

Potentiometer P_3

Potentiometer P_3 is used to remove $2f_m$, the second harmonic of the modulation signal from the output signal frequency spectrum. To adjust P_3 and other components in the subsequent alignment procedure set

e_m = 50 mv rms
e_c = 50 mv rms

and the source resistance of each input signal generator equal to ten ohms.

For alignment of P_3 set

f_m = 3000 Hz
f_c = 125 kHz

Using the frequency selective voltmeter, adjust P_3 until $2f_m$ disappears.

Potentiometer P_1

The function of potentiometer P_1 is the removal of f_m from the output signal frequency spectrum for low modulation frequency operation. Set

f_m = 300 Hz
f_c = 125 kHz

and adjust P_1 until f_m disappears.

Capacitor C_1

Removel of f_m for high modulation frequency operation is accomplished with capacitor C_1. Set

f_m = 3000 Hz
f_c = 125 kHz

and adjust C_1 until f_m disappears.

Potentiometer P_4

Potentiometer P_4 is used to remove f_c for low carrier frequency operation. Set

f_m = 3000 Hz
f_c = 5 kHz

and adjust P_4 until f_c disappears.

Capacitor C_2

Capacitor C_2 removes f_c from the output signal frequency spectrum for high carrier frequency operation. Set

f_m = 3000 Hz
f_c = 125 kHz

and adjust C_2 until f_c disappears.

Potentiometer P_2

The setting of potentiometer P_2 determines the dc voltage level at the modulator output terminal when both input signal amplitudes are zero. Set

e_m = 0 volts rms
e_c = 0 volts rms

and maintain ten ohms source impedance for each signal generator. Adjust P_2 for the desired dc output voltage level.

III. PERFORMANCE DATA

A. GENERAL

Tabulated data in the following sub-sections relates performance of the FET true product modulator breadboard at room temperature unless otherwise indicated. The breadboard schematic is shown in figure II-1. Also the schematic parts list in section II.B applies for all tests unless noted otherwise. A final consideration is the fact that the source resistance of each modulator input signal is ten ohms.

B. OUTPUT SIGNAL FREQUENCY SPECTRUM

Output signal frequency spectrum data represents desirable and undesirable components in the modulator output signal. The voltage magnitude of each frequency component is given. In addition a comparison of undesirable components and desirable sideband frequencies is expressed.

Data is tabulated for two conditions. For the first condition the gate of each FET is biased at the point which corresponds to the optimum output signal spectrum. This data is tabulated for room temperature operation only. Test results for the second condition, which was tabulated for $-20^{o}C$, $+25^{o}C$, and $+85^{o}C$ performance, represents the frequency spectrum when each FET gate terminal is biased at its zero drift point. This point is where FET channel conductance theoretically is not affected by temperature variations.

Equipment utilized to obtain frequency spectrum data is listed below.

1-HP Wide Range Oscillator, Model 200CD
1-HP Audio Oscillator, Model 200J
1-HP Wave Analyzer, Model 302A
1-Sierra Frequency Selective Voltmeter, Model 126A

1. Optimum FET Bias Point

e_m = 50 mv rms @ 3000 Hz
e_c = 50 mv rms @ 120 kHz

V_{SG1} = 0.75 vdc
V_{SG2} = 0.[illegible] vdc

FREQUENCY COMPONENT	SIGNAL LEVEL	REJECT RATIO
	mv rms	db
f_m	1.20	-51.3
$2f_m$	1.50	-49.4
$f_c - 3f_m$	1.11	-52.0
$f_c - 2f_m$	0.37	-61.5
$f_c - f_m$	445.00	0.0
f_c	0.88	-54.0
$f_c + f_m$	445.00	0.0
$f_c + 2f_m$	0.37	-61.5
$f_c + 3f_m$	1.11	-52.0
$2f_c - 2f_m$	0.37	-61.5
$2f_c - f_m$	1.11	-52.0
$2f_c$	0.37	-61.5
$2f_c + f_m$	1.11	-52.0
$2f_c + 2f_m$	0.37	-61.5
$3f_c - f_m$	0.37	-61.5
$3f_c$	-	-
$3f_c + f_m$	0.37	-61.5

2. Zero FET Drift Bias Point

e_m = 50 mv rms @ 500 Hz
e_c = 50 mv rms @ 8000 Hz

V_{SG1} = 2.10 vdc
V_{SG2} = 2.12 vdc

FREQUENCY COMPONENT	TEMPERATURE					
	-20°C		+25°C		+85°C	
	SIGNAL LEVEL	REJECT RATIO	SIGNAL LEVEL	REJECT RATIO	SIGNAL LEVEL	REJECT RATIO
	mv rms	db	mv rms	db	mv rms	db
f_m	75.0	-22.3	0.6	-62.5	73.0	-16.7
$2f_m$	14.0	-37.9	0.3	-68.5	1.3	-51.7
$f_c - 4f_m$	0.5	-66.8	0.2	-72.0	0.1	-74.0
$f_c - 3f_m$	16.0	-36.7	6.1	-42.4	1.8	-48.9
$f_c - 2f_m$	44.0	-28.0	3.3	-47.7	6.9	-37.2
$f_c - f_m$	1100.0	0.0	800.0	0.0	500.0	0.0
f_c	90.0	-21.7	3.7	-46.7	9.5	-34.4
$f_c + f_m$	1100.0	0.0	800.0	0.0	500.0	0.0
$f_c + 2f_m$	44.0	-28.0	3.3	-47.7	6.9	-37.2
$f_c + 3f_m$	16.0	-36.7	6.1	-42.4	1.8	-48.9
$f_c + 4f_m$	0.5	-66.8	0.2	-72.0	0.1	-74.0
$2f_c + 3f_m$	0.5	-66.8	0.8	-60.0	0.2	-68.0
$2f_c - 2f_m$	13.0	-38.5	3.0	-48.5	0.2	-68.0
$2f_c - f_c$	40.0	-28.8	2.8	-49.1	5.6	-39.0
$2f_c$	27.0	-32.2	5.9	-42.6	0.3	-64.4
$2f_c + f_m$	40.0	-28.8	2.8	-49.1	5.6	-39.0
$2f_c + 2f_m$	13.0	-38.5	3.0	-48.5	0.2	-68.0
$2f_c + 3f_m$	0.5	-66.8	0.8	-60.0	0.2	-68.0
$3f_c - 2f_m$	0.5	-66.8	0.5	-64.1	0.1	-74.0
$3f_c - f_m$	8.5	-42.2	2.1	-51.6	0.3	-64.4
$3f_c$	0.8	-62.8	1.1	-57.2	0.1	-74.0
$3f_c + f_m$	8.5	-42.2	2.1	-51.6	0.3	-64.4
$3f_c + 2f_m$	0.5	-66.8	0.5	-64.1	0.1	-74.0

C. FREQUENCY RESPONSE

Modulator frequency response places a maximum limit on the carrier input signal frequency. Data tabulated below is a plot of modulator output signal amplitude versus carrier frequency for a constant dc modulation input signal. The output voltage in the same plot is also shown normalized to the lowest frequency output voltage.

Equipment utilized to obtain this data is listed below.

1-HP Wide Range Oscillator, Model 200CD
1-EDC Precision DC Voltage Standard, Model VS-11N
1-John Fluke True rms Voltmeter, Model 910A

e_c = 50 mv rms e_m = +75 mv dc

CARRIER FREQUENCY	MODULATOR OUTPUT	
kHz	mv rms	db
5	975	0.00
10	975	0.00
20	975	0.00
30	975	0.00
40	973	-0.02
50	971	-0.04
60	968	-0.06
70	965	-0.10
80	962	-0.12
90	956	-0.16
100	949	-0.24
110	944	-0.28
120	938	-0.34
130	933	-0.38
140	926	-0.44
150	921	-0.50

D. PHASE SHIFT

Both modulation and carrier signal phase shift through the modulator was measured with the equipment listed below.

1-HP Wide Range Oscillator, Model 200CD
1-EDC Precision DC Voltage Standard, Model VS-11N
1-AD-YU Precision Phase Meter, Model 405H

The largest modulation signal phase, which corresponds to the maximum modulation signal frequency (3kHz), is less than the phase meter resolution (0.5 degree). It is felt that the required effort to precisely measure this angle is not warranted at this time, therefore, modulation signal phase shift data is not included in this report.

Data tabulated below depicts carrier signal phase shift versus frequency for a dc modulation input signal.

e_c = 50 mv rms $\qquad\qquad$ e_m = +75 mv dc

CARRIER FREQUENCY	CARRIER PHASE SHIFT
kHz	Degrees
30	5.9
60	10.6
90	16.4
120	22.2

E. LINEARITY

Linearity is defined by the following equation.

$$LIN = \left[\frac{\epsilon}{F.S.}\right] \left[100\%\right] \tag{23}$$

where

ϵ is the difference between calculated and measured output voltage.
F.S. is difference between maximum and minimum measured output voltage or full scale range.

This expression was used to determine modulator linearity in terms of the modulation input signal and also in terms of the carrier. Modulation linearity data was obtained by setting the carrier input signal to a constant dc voltage and recording modulator output voltage versus modulation input signal amplitude. This test was performed at zero and 3000 Hz modulation frequencies.

For carrier linearity data, the modulation signal was set to a constant dc voltage and modulator output voltage versus the carrier input signal amplitude was recorded. This test was performed at 5 kHz and 120 kHz carrier frequencies.

Equipment utilized to obtain this data is listed below.

1-HP Wide Range Oscillator, Model 200CD
2-EDC Precision DC Voltage Standard, Model VS-11N
1-John Fluke rms Voltmeter, Model 910A
1-Electro Instruments Digital Voltmeter, Model 620

1. Modulation Linearity

Low Frequency

f_m = 0 Hz e_c = 75 mv dc

MODULATION INPUT	OUTPUT		LINEARITY
	MEAS	CAL	
vdc	vdc	vdc	%
0.0	0.0	0.0	0.00
2.0	40.0	40.5	0.03
4.0	79.0	81.0	0.12
6.0	120.0	121.6	0.10
8.0	159.0	162.1	0.19
10.0	204.0	202.6	-0.09
20.0	408.0	405.3	-0.17
40.0	810.0	810.5	0.03
60.0	1216.0	1215.8	-0.01
80.0	1621.0	1621.0	0.00

High Frequency

f_m = 3000 Hz e_c = 75 mv dc

MODULATION INPUT	OUTPUT		LINEARITY
	MEAS	CAL	
mv rms	mv rms	mv rms	%
2.00	32.2	32.2	0.00
4.00	62.5	63.1	0.08
6.03	93.8	94.6	0.11
8.05	125.5	126.0	0.07
10.06	157.0	156.9	-0.01
20.05	312.0	311.7	-0.04
30.09	468.0	467.3	-0.09
40.15	625.0	623.2	-0.24
50.32	781.0	781.0	0.00

2. Carrier Linearity

Low Frequency

f_c = 5 kHz e_m = 75 mv dc

CARRIER INPUT	OUTPUT		LINEARITY
	MEAS	CAL	
mv rms	mv rms	mv rms	%
0.28	6.0	6.0	0.00
10.00	195.0	195.9	0.09
20.08	391.0	392.8	0.19
30.02	586.0	586.9	0.09
40.06	782.0	783.0	0.10
50.04	978.0	978.0	0.00

High Frequency

f_c = 120 kHz e_c = 75 mv dc

CARRIER INPUT	OUTPUT		LINEARITY
	MEAS	CAL	
mv rms	mv rms	mv rms	%
0.28	8.0	8.0	0.00
10.00	190.0	189.8	-0.02
20.00	378.0	376.9	-0.12
30.04	565.0	564.7	-0.03
40.03	750.0	751.5	0.16
50.00	938.0	938.0	0.00

IV. CONCLUSIONS

Based on results of the study of true product modulators, it is concluded that no modulator or multiplier is available as a standard product that is suitable for use in both ground and aerospace telemetry applications. To be suitable the modulator must not only function adequately in both environments but also be practical. A practical modulator must be reasonably priced and for use in an aerospace environment, it must be small and lightweight and dissipate minimum power.

Modulators are available that very probably will function adequately in ground based telemetry applications. The statement was made in Chrysler Technical Memorandum HEE-MID4-67 that the Ohio Semitronics, Inc. Model MC-521 and the F. W. Bell, Inc. Model HM-4050 multipliers possibly can be used in ground based telemetry applications. However this possibility is contingent on elimination of certain undesirable features which are described in the aforementioned technical memorandum.

The FET true product modulator described in this report is another modulator that should function satisfactorily in most ground based systems and, subject to the resolution of particular thermal problems will possibly function in an aerospace environment. This modulator dissipates very little power; is small and lightweight; and exhibits commendable performance at room temperature.

Test results in section III are indicative of modulator performance. These tests involve the modulator output signal frequency spectrum, frequency response, phase shift, and linearity.

The output signal frequency spectrum test was performed for two conditions. For the first test the gate of each FET in the modulator circuit of figure II-1 was biased at the voltage point which corresponds to the optimum modulator frequency spectrum for room temperature operation. Test results in section III.B.1 are an indication that modulator performance is good indeed.

For the second test the gate of each FET was biased at its zero drift point. This is the point where transistor channel conductance theoretically is not affected by temperature variations. Corresponding to the zero drift bias point it was expected that modulator performance would be degraded somewhat but not affected appreciably by temperature variations.

As expected for room temperature operation, modulator test results in section III.B.2 are less than optimum but still good. In section I.B it was shown how the modulator design eliminates many effects of FET non-linear characteristics, regardless of transistor gate bias. However, FET non-linear characteristics corresponding to the zero drift bias point, are greater than non-linear characteristics corresponding to the bias point for the first test.

Therefore, the magnitude of undesirable frequency components in the output frequency spectrum, that are not eliminated by the modulator design, are more significant.

Although modulator performance for room temperature operation at the zero drift bias point compares favorably with optimum results that were obtained in the first test, performance at -20°C and +85°C is not good. The magnitude of many undesirable frequency componente increased significantly. A change from the room temperature value was expected, but it was also expected that this change would be minor. Anticipated performance was based on the following realities. The instantaneous FET gate voltage of transistor Q_1 in figure II-1 of section II.A corresponds to the zero drift bias point at only two instants in time during a cycle of e_c, the carrier signal. This means that FET channel conductance and correspondingly the magnitude of undesirable frequency components are sensitive to temperature variations at every other instant in time. However, the variation of channel conductance from the zero drift point value is small. Therefore, it was expected that the change in magnitude of undesirable frequency components would also be small at each temperature extreme.

For use in an aerospace environment this poor performance over the operating range of course must be eliminated. The performance might be partly if not completely caused by the fact that each FET might not have been biased precisely at its zero drift point. Assuming that this is the cause of poor performance it is probable that the expense involved would be prohibitive to precisely locate this bias point. If this assumption is true the considerable manufacturing expense would probably rule out the use of the FET true product modulator in an aerospace environment.

Since recorded modulator frequency spectrum data at the temperature extremes is poor, subsequent tests were performed at room temperature only. Modulator frequency response data in section III.C reveals that the output signal versus frequency plot begins to slope gradually at 40 kHz. Based on modulator functional theory in section I.B and published Radiation, Inc. operational amplifier specifications this performance is predictable. For many uses the modulator frequency response is acceptable. However, modulator functional theory reveals that performance can be improved by increasing amplifier loop gain.

Modulator phase shift data is recorded in section III.D. Both modulation and carrier signal phase shift through the modulator was measured. As expected modulation phase shift is much less than the carrier angle. This is explained by the fact that phase shift, like modulator frequency response, is related to amplifier loop gain, which is in turn inversely proportional to frequency. At the upper modulation signal input frequency (3 kHz) amplifier loop gain is sufficient to limit modulation phase shift to a very small angle. The statement was made in section III.D that the modulation signal phase shift is less than the resolution (0.5 degree) of the phase meter used for measurement. It is very probable that precise measurement would reveal that this angle is considerably less than 0.5 degree. This contention is based on modulator theory and published amplifier specifications. Therefore, the conclusion is

that modulation signal phase shift can be neglected for the majority of applications.

Although carrier signal phase shift is significant, measured data reveals that the angle is linearly proportional to frequency. For many applications this is acceptable. In any event this angle can be reduced in magnitude by increasing amplifier loop gain.

Overall modulator loop gain can be increased to realize improved frequency response and phase shift characteristics by removing amplifier K_3 in figure II-1. However, removal of this amplifier is contingent upon the required output signal level. Recall from the modulator breadboard description in section II.C that the sole function of this amplifier is for amplification.

Linearity test data is section III.E.1 and section III.E.2 depicts modulator linearity in terms of each input signal. In each case the test was performed for both low and high frequency input signals. This was done to demonstrate universal modulator linearity. Tabulated results confirm fulfillment of the necessary requirement that linearity be independent of frequency.

The discussion of test results substantiates the statement made earlier in this section that the FET true product modulator should function adequately in most ground based systems. Unfortunately thermal problems deter use of the modulator in an aerospace environment. Additional investigation is a necessity to positively determine the cause and possibly arrive at a practical solution to these problems. However, it is concluded from accumulated knowledge that a practical solution does not appear likely.

Restating in brief, the basic conclusion the study of true product modulators revealed that previously mentioned modulators are available that should function adequately in ground based systems but apparently no true product modulator presently exists that will function in a completely satisfactory manner in an aerospace environment.

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TECHNICAL MEMORANDUM HEE
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A STUDY OF TRUE PRODUCT MODULATORS

PHASE III

FINAL REPORT

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