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ABSTRACT

This paper analyses the performance of an Integrate and Dump circuit when used for PCM data regeneration. This analysis is made using the circuit's transfer function. The influence of the circuit parameters is also analyzed and some conclusions are reached which can be used as design criteria.

BIT ERROR ANALYSIS FOR A PCM EQUIPMENT USING INTEGRATE AND DUMP MODE OF DATA REGENERATION

The analysis of the error probability in a PCM data link is fundamental for evaluating the system's reliability and performance. One of the techniques employed for data regeneration is called Integrate and Dump. Basically, the principles of operation of this mode are: Integration of the incoming data during a fraction of the Bit period; sampling of the Integrator output at a time near the end of integration time; and resetting of the Integrator before the next Bit. Figure 1 shows the block diagram of one such circuit. In Figure 1 is also included a PCM data Simulator, a Noise generator, a Low pass filter and an Adder, these elements are part of the Test set-up used for evaluating the performance of the PCM equipment

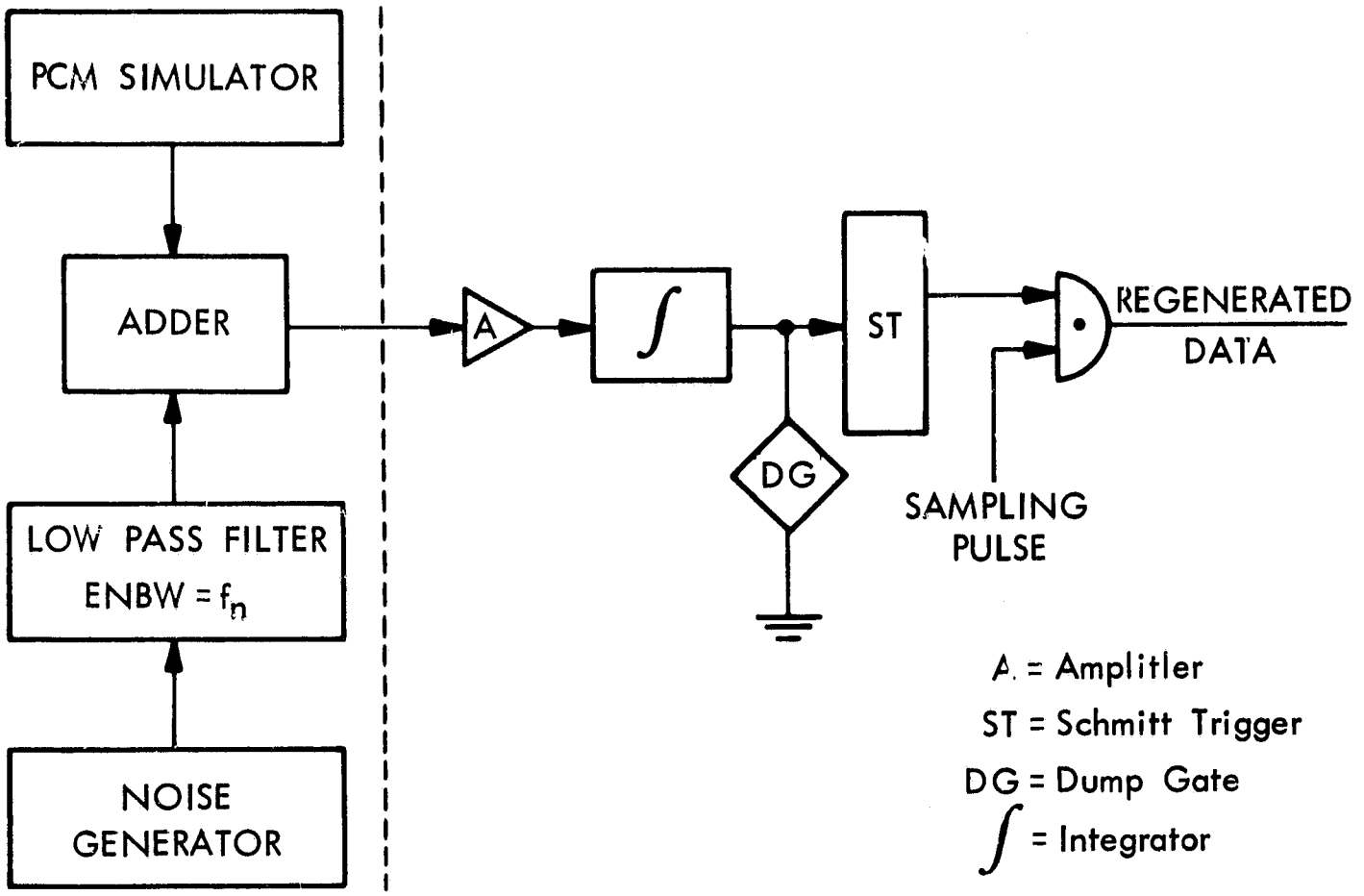

Figure 1-Block Diagram.

The integrator can be an active or a passive integrator, however, most of the time and for simplifying the circuit a passive integrator is used. This passive integrator is an RC network as shown in Figure 2. This is going to be the circuit discussed in this paper.

The Dump gate or Reset gate can have many different configurations and we will not analyze it in detail. During the integration of the incoming data bits the dump gate represents a very high resistance in parallel with the capacitor C shown in Figure 2. During the dumping action, the effective resistance of the Dump gate is very low so that a fast discharge of the capacitor C is accomplished.

The Schmitt trigger is the Decider element, that is, if the level in the output of the Integrator exceeds its threshold the conduction state of the Schmitt trigger informs the sampling gate that a "one" is present in the data. If the threshold is not exceeded the output of the Schmitt trigger will inform the sampling gate that a "zero" is present in the data. In this manner the output of the sampling gate will be the regenerated incoming data.

Since the Schmitt trigger is the decision element, errors made in the data regeneration can be attributed to erroneous crossings of the Schmitt trigger's threshold and this is a function of the Signal-to-Noise ratio at the input of the Schmitt trigger. Normally the threshold of the Schmitt trigger will be zero volts, that is, if the input to the decider is above zero volts a "one" is recognized and if it is below zero volts a "zero" is recognized.

The analysis presented here is based on a zero volts threshold.

The probability distribution of the bit errors will be considered Gaussian and so the error function, erf, of the normal probability curve shall be used.

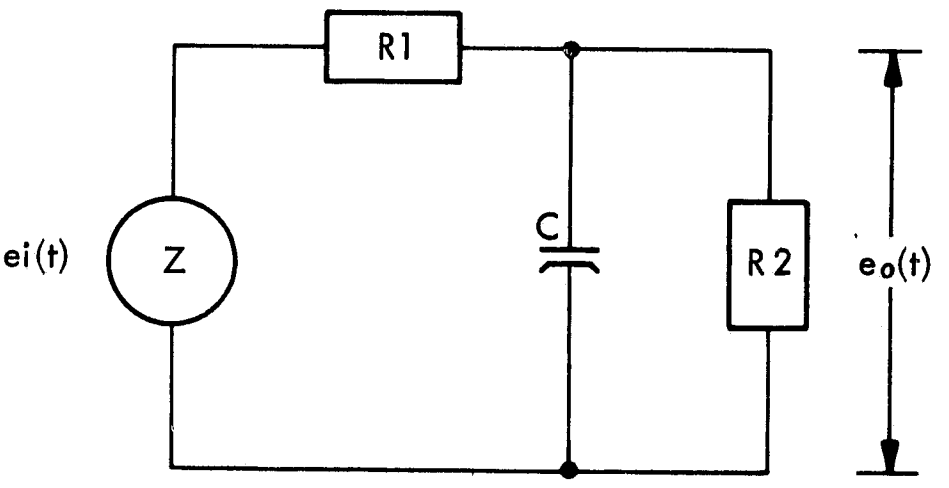

Figure 2-Passive Integrator.

The probability of an erroneous crossing of the decision threshold can be expressed as:

$$P_e = \frac{1}{2} \; 1 - \mathrm{erf} \; S_0/N_0 \sqrt{2} \qquad (1)$$

where S_0 = peake signal voltage at sampling time and N_0 = rms noise voltage at the decider's input.

To evaluate S_0 and N_0 we will use the transfer function of the network indicated in Figure 2. The generator indicated in Figure 2 corresponds to the amplifier in Figure 1. It is considered here that this amplifier does not change the Signal-to-Noise ratio found at the input of the PCM equipment (Very wide bandpass) and that its output impedance as seen from the integrator is very small compared to R_1. (Emitter follower stage in its output).

The load resistor R_2, in Figure 2, is included to make our analysis more general and because its value is important and has influence on the circuit's performance. In some equipment, R_2 will be found to be a physical resistor easily identifiable and in others it can be found as the input impedance of the circuit connected to the integrator's output.

The transfer function of the circuit of Figure 2 is:

$$H(s) = 1/R_1C \left(s + \alpha/R_1C\right) \qquad (2)$$

$$\alpha = 1 + R_1/R_2$$

The transfer function $H(s)$ indicated in (2) will be applied both to determine S subindex 0, peak signal at sampling time, and N subindex 0, rms noise at sampling time. This transfer function does not take into consideration the effect of the Dump gate since the sampling of the integrator output takes place before the dumping time which in some cases occurs during the following bit period. Apart from this, the assumption is made that there is no residual charge in after the dumping action. Practical tests have demonstrated that both of the above considerations have a very small influence on the accuracy of the predicted bit errors for a particular system as long as all the parameters appearing in Equation (9) are properly evaluated. Accuracy has always been within 0.5 db.

To find S_0, peak signal voltage at sampling time, we take $e_i(s) = 1/s$, and the initial charge in C equal to zero. To assume that the input to the integrator is a step function can be done since each bit finds the integrator reset and so to the integrator each bit will "look" like a step. This assumption simplifies the analysis without incurring in errors. With this consideration we find that:

$$S_0 = \frac{1}{a}\left(1 - \exp\left(-aT/R_1C\right)\right) \tag{3}$$

In (3), T is the sampling time. For the purpose of simplification the input step has a peak value of 1 volt. We have considered here only a positive step since after all we are looking for the absolute value of S_0. We can consider that the input PCM data is actually varying between +1 and -1 volt with a random pattern. It is important to notice then that the rms value of the data is also 1 volt rms.

To calculate the rms value of noise at the integrator output we use the following:

$$N_0^2\,(\text{rms}) = \int_0^\infty N(\omega)\,\left|H(j\omega)\right|^2\,d\omega \tag{4}$$

where $N(\omega)$ = noise spectral density at ;the input to our integrator and its units (volts rms^2/radian). In this paper we will only consider white noise so that $N(\omega)$ is constant and can be taken out of the integrand.

To make our analysis more realistic a correction has to be made to (4) since in practically all cases as well as in the test set-up shown in Figure 1 we will be dealing with band limited white noise, therefore the upper limit of integration will be set as ω_n.

This ω_n is the angular cut-off frequency of the Effective Noise Bandwidth (ENBW) of the equipment feeding the data to the PCM DHE. With this consideration we write:

$$N_0^2\,(\text{rms}) = N(\omega)\int_0^{\omega_n}\left|H(j\omega)\right|^2\,d\omega \tag{4a}$$

$$N_0^2\,(\text{rms}) = \frac{H(\omega)}{R_1 C}\ \text{arc tg}\ \left(2\pi f_n\ R_1 C/\alpha\right) \tag{5}$$

$$\omega_n = 2\pi f_n$$

$$\frac{\pi}{2} > \text{arc tg}\ \left(2\pi f_n\ R_1 C/\alpha\right) > 0$$

Now we have most of the elements needed to calculate $N_0(\text{rms})$ except $N(\omega)$. This we can calculate by relating it to the available (noise rms voltage)^2 at the input of the PCM DHE equipment. We can write:

$$\text{SNR} = 1/N(\omega) \cdot 2\pi f_n \tag{6}$$

SNR is the Signal-to-Noise power ratio at the input to the PCM DHE. It is important to remember here that the PCM data has been assumed to have 1 volt rms.

From (5) and (6) we obtain:

$$N_0^2\,(\text{rms}) = \frac{\text{arc tg}\ \left(2\pi f_n\ \tau/\alpha\right)}{2\cdot\pi\cdot\alpha\cdot\tau\cdot f_n\cdot(\text{SNR})} \tag{7}$$

$$R_1 C = \tau$$

If we let arc tg $(2\pi f_n \tau/\alpha) = \pi/2\ \beta$, we obtain:

$$N_0^2\,(\text{rms}) = \beta/4\cdot\alpha\cdot\tau\cdot f_n\cdot(\text{SNR}) \tag{8}$$

From (3) and (8) we now obtain the argument of the error function erf, which will enable us to compute P_e.

$$S_0 N_0 \cdot \sqrt{2} = \left(1 - \exp\left(-\alpha T/\tau\right)\right) \sqrt{2 \cdot \tau \cdot f_n \cdot (SNR)/\alpha\beta} \qquad (9)$$

To see the effect of changing the different parameters of the circuit in Figure 2 upon the probability of errors in the regenerated data a family of curves have been plotted. The first family of curves is shown in Figure 3 and corresponds to P_e vs. SNR at the PCM DHE input as a function of τ, (time constant of the RC network). Table I gives the values plotted in Figure 3.

The values given above have been calculated setting $f_n = \pi$. (Bit rate);

A second family of curves has been plotted for P_e vs. SNR as a function of T, (sampling time as a fraction of the Bit period), with the same ENBW. Table II gives the computed values.

In Table I and II, α has been set equal to 1.0; in Table I, T was equal 1.0 (Bit period); and in Table II, τ was equal to 1.0 (Bit period).

The results obtained in Table I correspond to a change in the value of C in the circuit of Figure 2 while keeping R_1, R_2 constant. The results presented in Table II do not correspond to a change in circuit elements but to a change in timing of the sampling action. Finally, a third family of curves was plotted corresponding to P_e vs. SNR as a function of α. This corresponds to a change in value of R_2 in the circuit of Figure 2. This curves are shown in Figure 5 and the results are included in Table III.

To calculate the figures shown in Table III, the value of f_n was set equal to π. (Bit rate)

CONCLUSIONS:

From the results shown in Figure 3 and Table I, we see that the best performance of an integrate and dump circuit used for data regeneration are obtained when the value of τ is equal to 0.7 (bit period), however another important conclusion is that there is not too much difference in performance if τ has a value between 0.5 and 1.0 (bit period), this means that the design of a PCM DHE equipment can be simplified so that it uses fixed values for R_1 and C over a Bit rate range of 1:2 if the values selected for R_1 and C make τ vary between 0.5 and 1.0 (bit period).

The Bit rate range can even be extended to 1:3 if R_1 and C are selected so that τ varies between 0.5 and 1.5 (bit period), however a slight degradation (less than 1 db) occurs when τ has values between 1.0 and 1.5 (bit period).

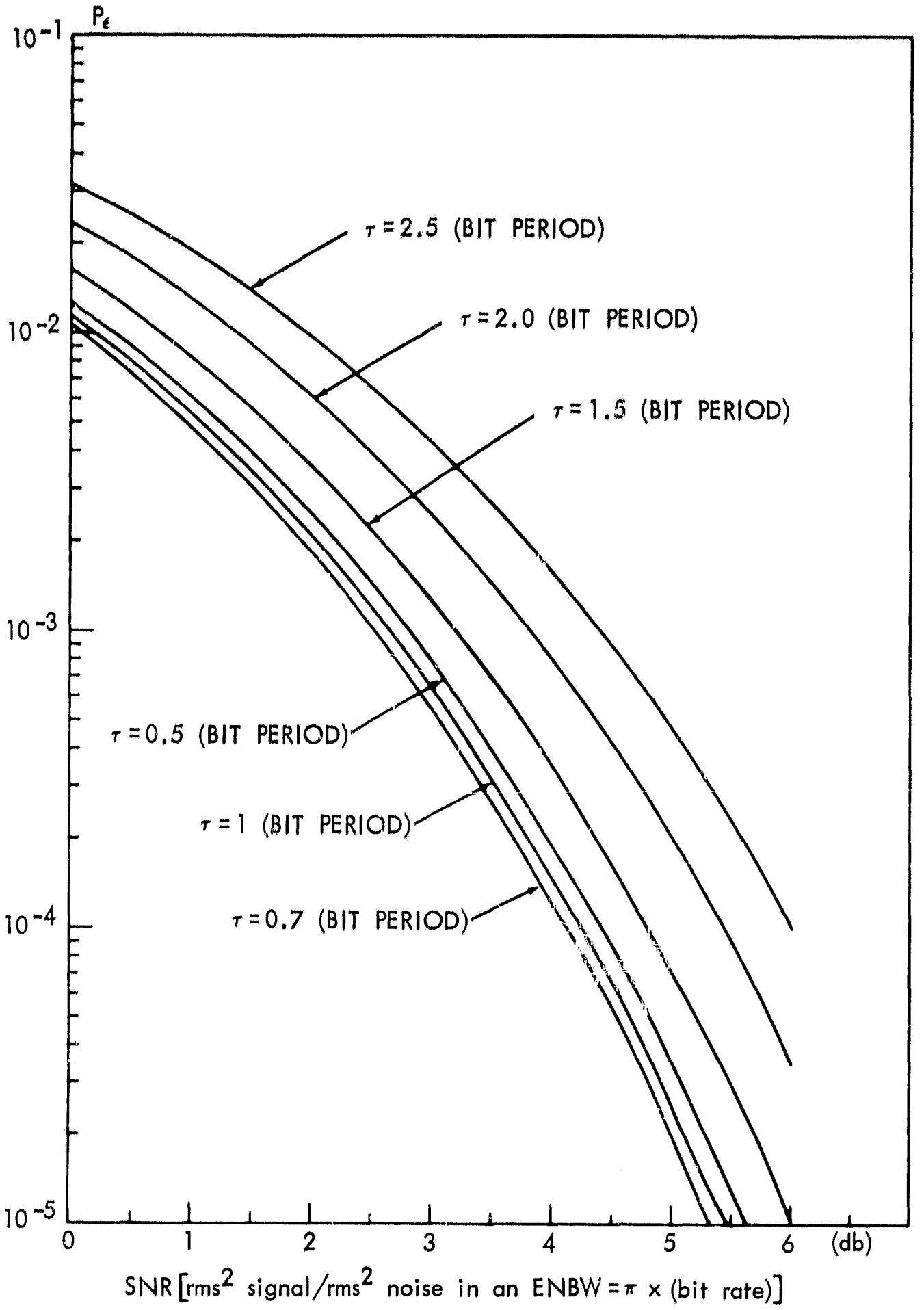

Figure 3-P_e vs. SNR as a Function of τ

From the curves plotted in Figure 4, we see the effect of changing the sampling time. The best performance is obtained if the integration times approaches one bit period. In designing a PCM DHE equipment with integrate and dump mode of operation, the main factor that will be influence the selection of the sampling moment will be the time required by the dump gate to discharge the capacitor so as to avoid overlap between successive bits. So as to obtain 100% Bit period integration time, two integrators are normally used.

Table I

P_e vs. SNR as a function of τ (Integrator time constant), expressed as a multiple of the Bit period.

SNR(db)	τ					
	0.5	0.7	1.0	1.5	2.0	2.5
0	0.01254	0.01049	0.01136	0.01626	0.02337	0.03142
1	0.00596	0.00479	0.00529	0.00822	0.01283	0.01842
2	0.00241	0.00184	0.00208	0.00358	0.00619	0.00963
3	0.00077	0.00055	0.00064	0.00126	0.00246	0.00426
4	0.00019	0.00013	0.00015	0.00035	0.00080	0.00158
5	0.000035	0.00002	0.000025	0.00007	0.00020	0.00046
6	---	---	---	0.00001	0.000035	0.00010

Table II

P_e vs. SNR as a function of T, (Sampling time), expressed as a fraction of the Bit period.

SNR(db)	T					
	0.5	0.6	0.7	0.8	0.9	1.0
0	0.07812	0.05200	0.03484	0.02361	0.01624	0.01136
1	0.05584	0.03407	0.02092	0.01299	0.00821	0.00529
2	0.03724	0.02041	0.01124	0.00628	0.00357	0.00208
3	0.02249	0.01076	0.00516	0.00262	0.00124	0.00064
4	0.01222	0.00493	0.00200	0.00080	0.00034	0.00015
5	0.00580	0.00190	0.00062	0.00021	0.000069	0.000025
6	0.00229	0.00057	0.00014	0.000037	0.00001	----

Table III

P_e vs. SNR as a function α.

SNR(db)	α				
	1	2	3	4	5
0	0.01136	0.01252	0.02039	0.03126	0.04309
1	0.00529	0.00597	0.01086	0.01832	0.02710
2	0.00208	0.00241	0.00503	0.00956	0.01544
3	0.00064	0.00077	0.00191	0.00422	0.00763
4	0.00015	0.00019	0.00058	0.00156	0.00323
5	0.000025	0.000035	0.000135	0.00046	0.00113
6	---	----	0.00002	0.00010	0.00030

From the curves shown in Figure 5 and the values in Table III we see that the best performance is obtained with $\alpha = 1$, this means an infinite resistor in parallel with C. This value is not obtainable but if R_2 is much larger than R_1, α can approach a value of 1.0.

Up to this moment, nothing has been said about the type of PCM code being processed as we have always normalized the values of T and τ as a function of the Bit period. To see the effect of the code being used on the values of P_e, we will calculate P_e for two ideal PCM DHE equipment. One will process split-phase data as NRZ-C at double the nominal bit rate and the other one will have a split-phase multiplier which will convert the incoming split-phase data to NRZ-C data at the nominal bit rate. The value of f_n will be set in both cases to 2π·(Bit rate, nominal); T will be equal to 100% (Bit period, processed) and τ will also be equal to 1.0 (Bit period, processed). The results of this calculations are shown in Figure 6 and in Table IV.

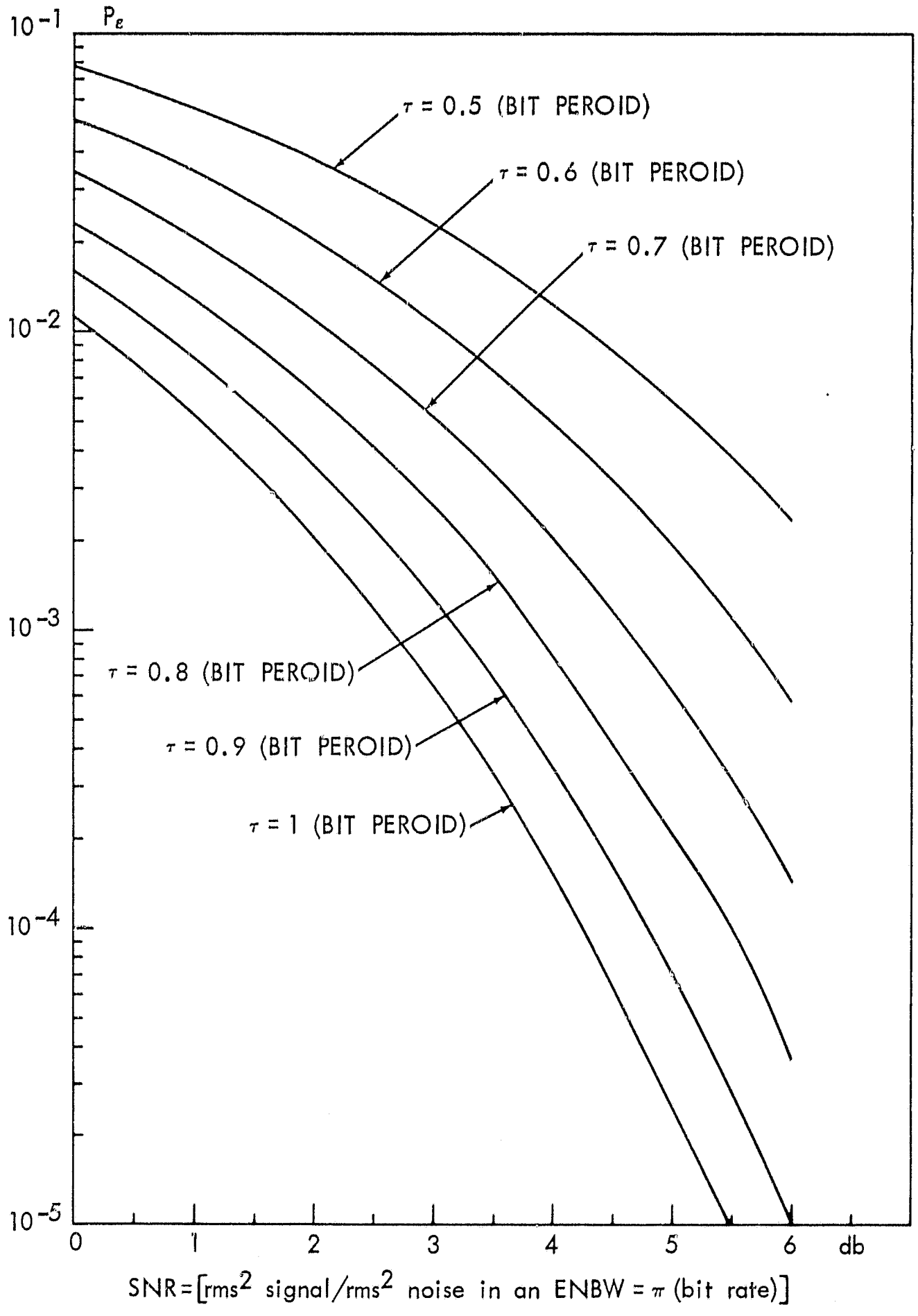

Figure 4-P_e vs. SNR as a Function of τ.

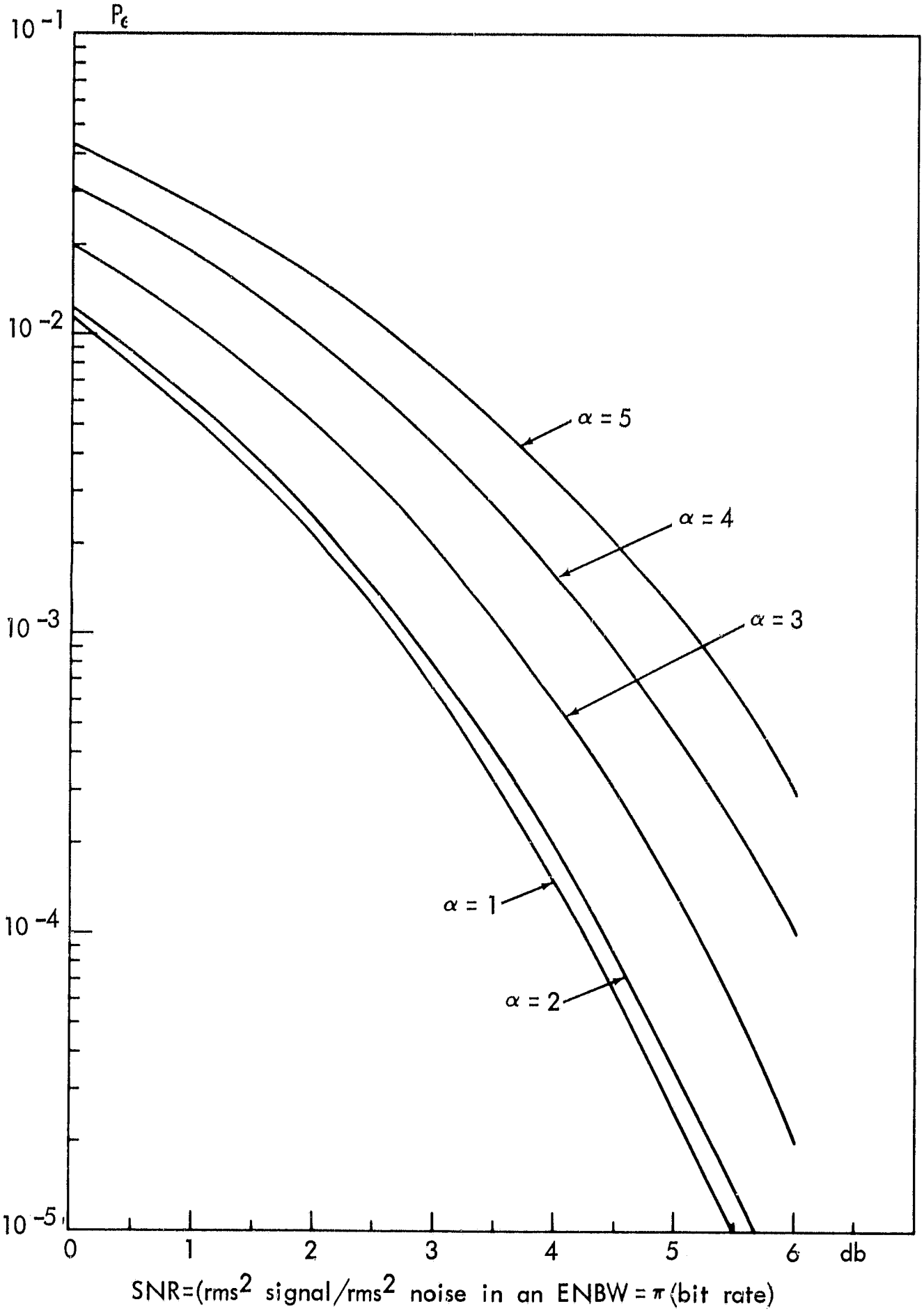

Figure 5-P_e vs. SNR as a Function of α.

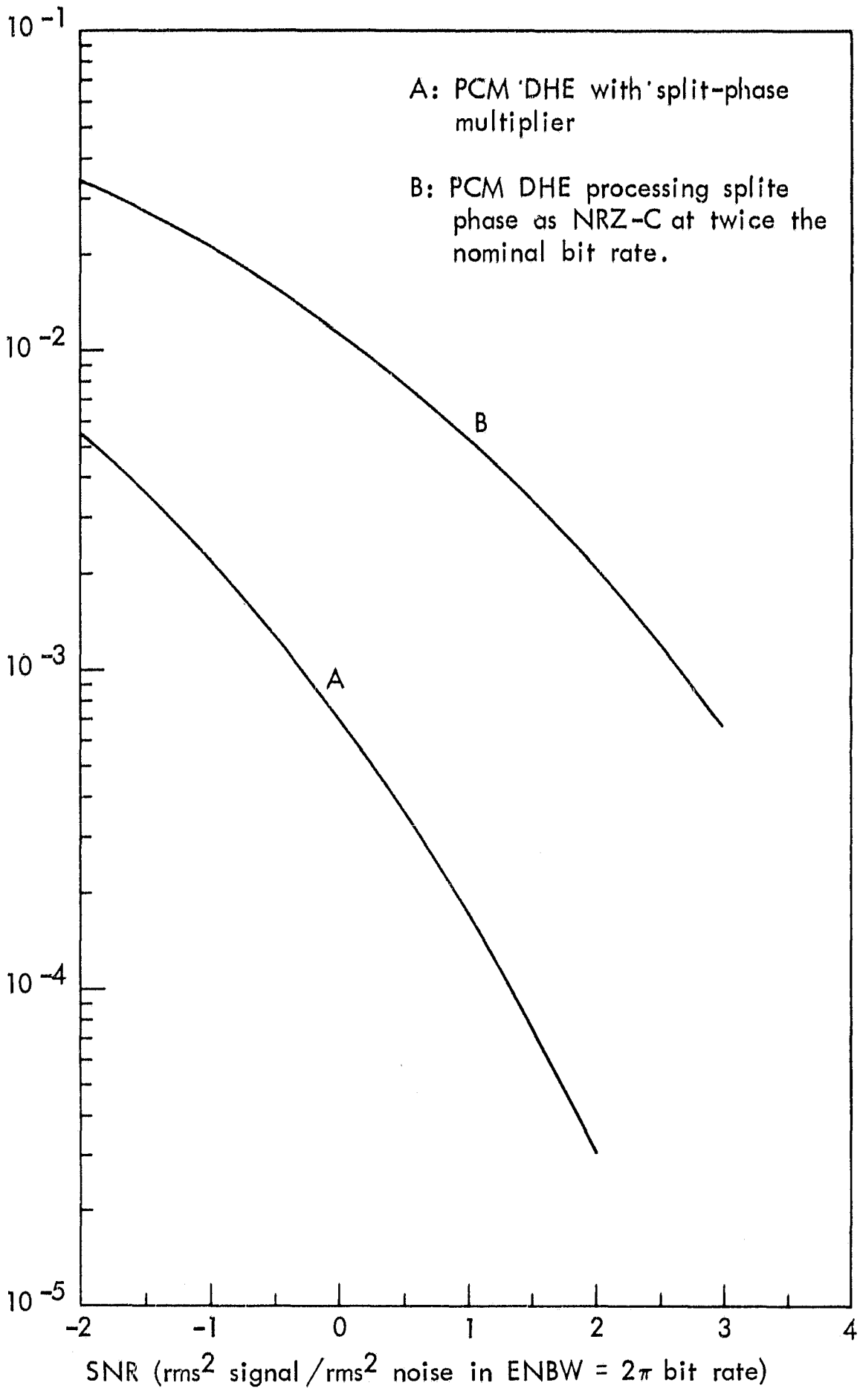

Figure 6-P_e vs. SNR.

Table IV

P_e vs. SNR for two PCM DHE equipment.
("A" is with the split-phase multiplier and "B" is for the equipment that processes the split-phase data as NRZ-C at twice the nominal bit rate)

SNR(db)	A	B
-2	0.00557	0.03520
-1	0.00221	0.02117
0	0.00070	0.01137
1	0.00017	0.00530
2	0.00003	0.00208
3	---	0.00064

From the curves in Figure 6 as well as from the values in Table IV we see that an improvement of practically 3 db is obtained by using the split-phase multiplier.

Throughout this paper, no distortion in the data has been considered as well as perfect bit synchronization.