RYAN REPORT NO. 59867-1
ENGINEERING MODEL
OF AN
ELECTRONICALLY SCANNED
PHASED ARRAY ANTENNA SYSTEM

FINAL REPORT

MAY 1969

CONTRACT NO. NAS 9-7626

PREPARED FOR: NASA MANNED SPACECRAFT CENTER
GENERAL RESEARCH PROCUREMENT BRANCH
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NASA CR 99698

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SECTION 1

INTRODUCTION

Ryan Electronics and Space Systems, a facility of Ryan Aeronautical Company, has developed and delivered an engineering model of an electronically scanned phased antenna system. This program was supported by NASA Manned Spacecraft Center, Contract No. NAS 9-7626. This final report describes the development and test phases of the engineering model.

The objective of this program was to establish, through test, the integrity and reliability of electronically phased array antennas with the ultimate goal of integrating a phased array antenna with the electronics of a radar system. This objective has been accomplished and demonstrated by the 4 x 4, C-Band, Transmitting/Receiving, Phased Array Antenna Assembly shown in Figure 1. Electronic beam steering has successfully been demonstrated for both transmitting and receiving functions by using the Step Recovery Diode (SRD) as a simultaneous microwave multiplier and phase shifter. This method of microwave phase shift is a Ryan invention which has been patented.

In accordance with MSC Contract No. NASA 9-7626, the following development tasks have been completed and are discussed in this report.

Task I - Develop and test 4 x 4, C-Band, Transmitting/Receiving Phased Antenna Assembly (Section 4).

Task II - Develop a Polarization Control and T-R Switch (Section 5)

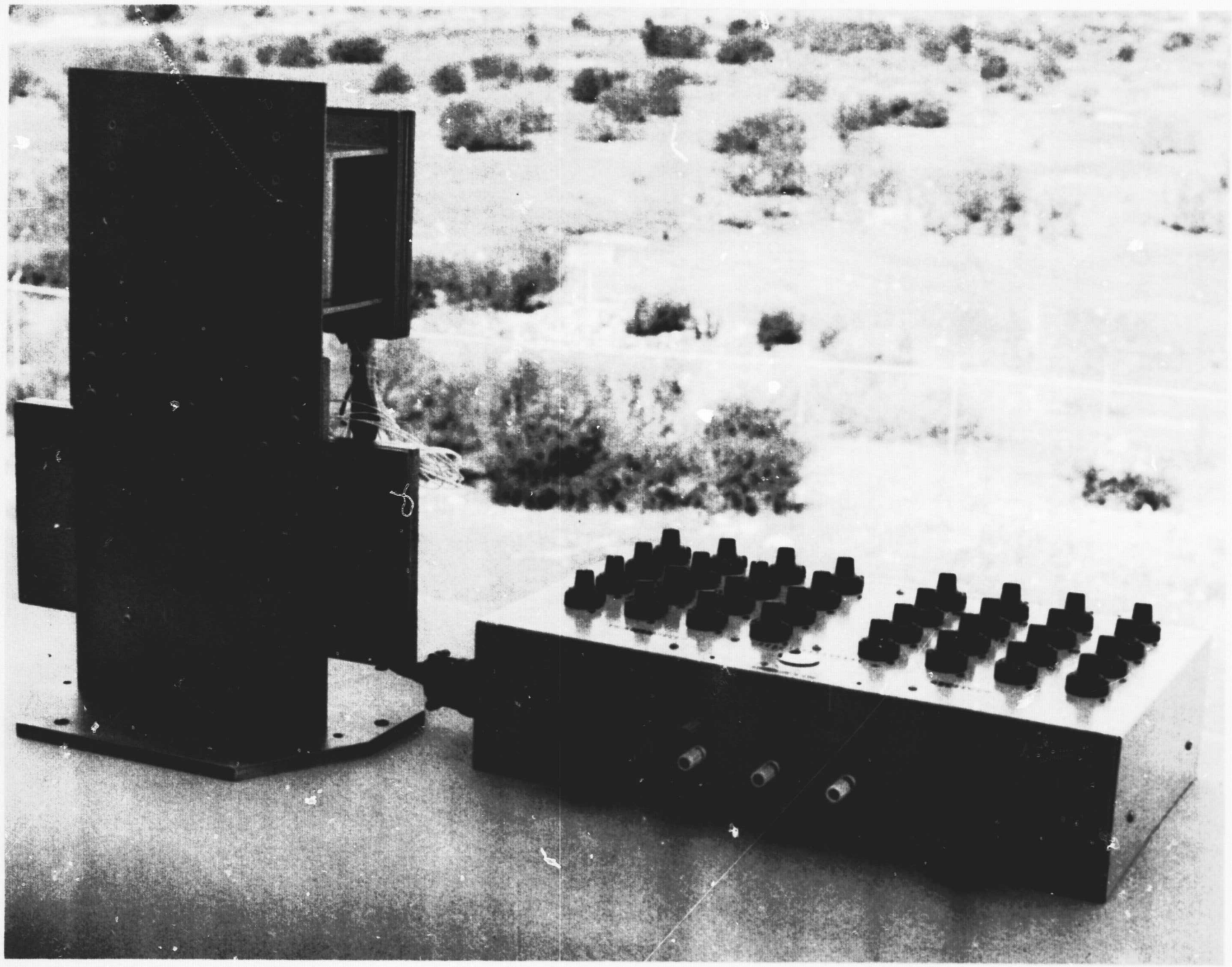


Figure 1 C-Band 4 x 4 Phased Array Antenna System

Task III - Develop a High-Power Element (Section 6)

This report is organized so the program conclusions are discussed in Section 2 and Ryan recommendations are listed in Section 3.

SECTION 2

CONCLUSIONS

The basic objectives of this engineering model development of a transmit/receive phased array antenna assembly have been achieved. It has been shown that the SRD does offer an excellent, simplified method of microwave phase shifting as required to steer an antenna beam electronically.

Comments regarding the conclusions of each of the tasks listed in the previous section are given in the following paragraphs.

2.1 4 X 4 TRANSMITTING/RECEIVING ARRAY DEVELOPMENT

Modules utilizing stripline techniques were developed to form the 4 x 4 array. The receiver portion of the module was adapted from a design for a previous Ryan program; the transmitter portion of the module was developed for this program.

Two series SRD multipliers were used in the transmitting portion of the module. The specified output power was readily achieved with all modules; some modules exceeded the required 200 milliwatts/module by 100%. Phase shift ranges in excess of 360° was readily achieved with each of the module transmitters.

Isolation between the two series multipliers was required to obtain a stable power mode for the transmitter output.

The receiver portion of the module provided satisfactory performance; however, the stripline wafer packaging technique required too many interconnections. This high number of interconnections reduced the reliability of the modules. The slope of the phase shift vs dc voltage was quite uniform

for most modules; and variation of slopes from module to module remained less than 2 to 1. It is anticipated both of these factors could be improved by Microwave Integrated Circuit (MIC) fabrication techniques.

Electronic beam s ering of the transmitter and receiver main beams was accomplished by individual open-loop phase control of each module SRD multipliers. Excellent patterns were recorded at the various scan angles in both the E and H-planes. The pattern quality, i.e., beamwidth, amplitude of side lobes, depth of difference pattern nulls, are in close agreement with theoretical values.

The advantages of the SRD as a simultaneous multiplier and phase shifter are verified by the antenna patterns measured with the array. These advantages include:

- Extremely low power required to phase steer, i.e., less than 5 milliwatts per module to change RF phase in excess of 360°.

- Simple circuitry - just one diode utilized as phase shifter and multiplier - this simplicity reduces module size and cost and significantly improves reliability over conventional methods of digital phase shifting.

- Analog beam steering has the advantage of simplicity and eliminates quantizing rate and position error associated with digital phase shifters.

- The SRD multiplier lends itself to an extremely small and simple MIC packaging configuration.

- No series loss of microwave power as occurs with the insertion loss of digital phase shifters.

2.2 POLARIZATION CONTROL AND T-R SWITCH DEVELOPMENT

Multipolarized antenna capability was developed and demonstrated. This was accomplished by fabrication of a polarization control and T-R switch breadboard. The breadboard assembly demonstrated satisfactory performance with respect to isolation and polarization capability. However, the insertion loss in the polarization control circuitry was higher than desirable for a phased array module. This was due to the number of diodes required; therefore, system requirements for more than a single polarization should be seriously considered before incorporation into system specifications.

The T-R switch demonstrated 40 db of isolation and an insertion loss of less than 1 db. A 100 nanosecond switch/time was inherent in the design. Power handling capability was limited by switching diode dissipation; the design incorporated total power handling capbility of 200 watts for each module.

2.3 HIGH POWER ELEMENT DESIGN

The Limited Space-Charge Accumulation (LSA) device was utilized to develop an engineering breadboard of a high power C-Band element. A basic in-sight into the physics of the LSA mode in bulk semiconductors was achieved.

A C-Band LSA device was injection phase locked successfully to a reference frequency source. Peak output power in excess of 40 watts was measured. This development was achieved by use of bulk type LSA devices. The output power conditions achieved included pulse widths of 100 nanoseconds and a repetition rate of 60 to 1000 Hz. The bulk LSA device had stringent driver modulation requirements to prevent the LSA from operating in the Gunn mode.

A new LSA modulator with variable repetition rate capability was developed. Injection phase lock data was measured to verify theoretical analysis regarding phase error, injection lock power ratios, and frequency pulling ranges.

Sufficient theoretical and experimental background has been gained to justify continuation of further LSA development. Additionally, one LSA supplier is developing a new line of epitaxial LSA devices (rather than of bulk type) which will improve many of the limitations experienced during this development study.

It presently appears that this new development of LSA devices will make high-power, solid state phased array radars possible.

SECTION 3

RECOMMENDATIONS

This development program and other Ryan phased array instrumentation programs have shown that the SRD provides a simple concept in electronic beam steering. It is strongly urged that the SRD concept and the transmit/receive phased array antenna technology developed by this contract be continued.

Ryan recommends that the following tasks be initiated:

a. Develop the receiver portion and portions of the x 2 transmitter multiplier in MIC. This development would provide a final configuration, C-Band module which could be used for space application. It is anticipated that the following advantages will be provided by MIC:

- Improved reliability
- Improvement in performance uniformity
- Reduce cost of fabrication
- Minimize module size and weight

b. Develop an analog closed tracking loop. Figure 2 presents an azimuth-elevation tracking system configuration which should be developed to allow measurement of radar system performance.

c. Perform operational analysis to study and define capability and application of radar system developed by items a and b listed above.

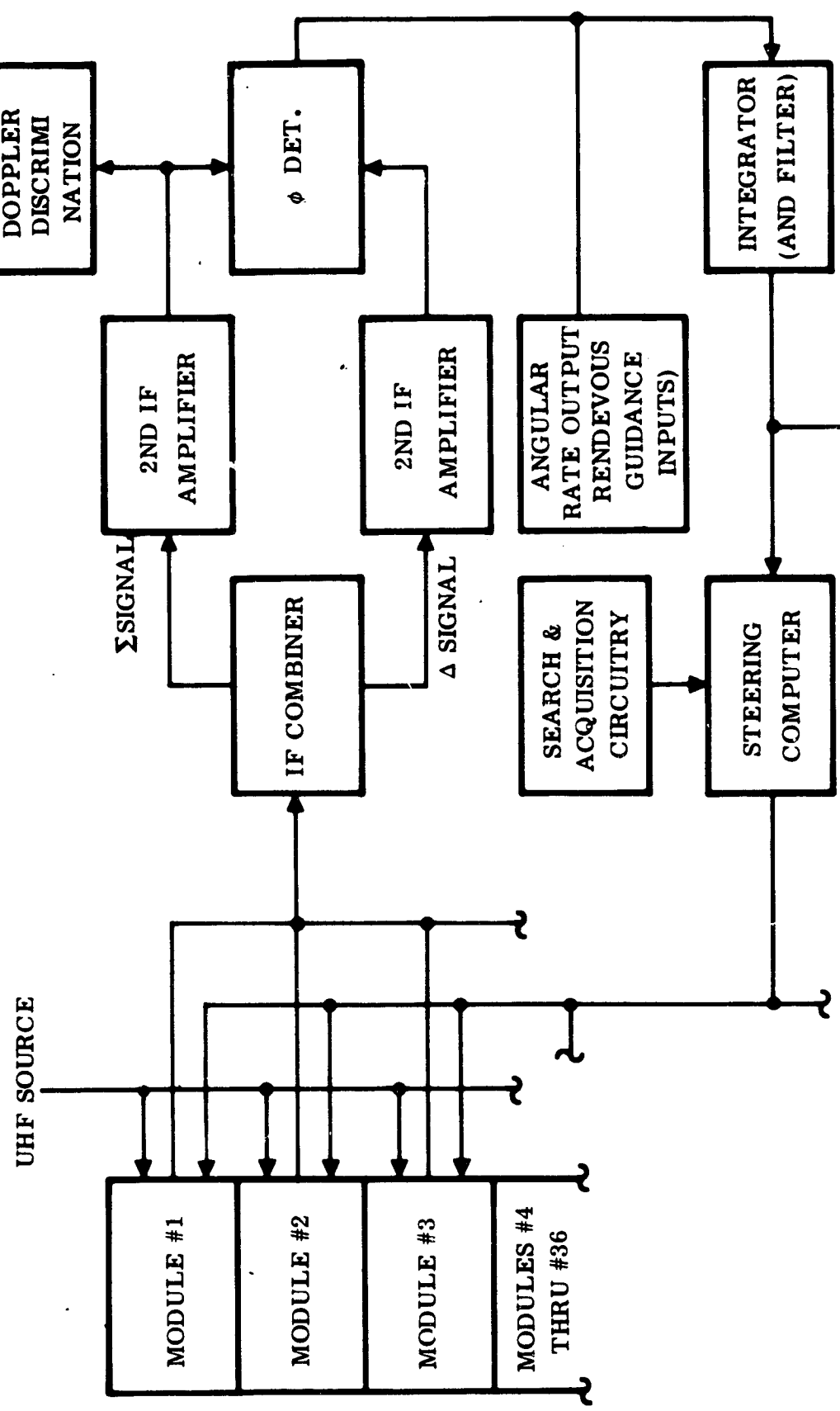


Figure 2 Block Diagram, Closed Tracking Loop (only one axis shown)

d. Continue LSA development to allow eventual consideration of this concept for very high power pulse radar application. This concept would combine the high power advantages of the LSA witn the minimal phase control power requirements of the SRD.

Continuation in these four suggested areas of effort will result in a space radar which may be conformally mounted and requires a minimum of power for electronically beam steering the transmitted and received beam patterns. The results of this program will provide the elements of an instrumentation system for rendezvous docking and space search and acquisition.

SECTION 4

TECHNICAL DISCUSSION OF THE 4 X 4 ARRAY DEVELOPMENT

The development effort accomplished on the 4 x 4 Transmitting/Receiving Array is presented in this section. The technical discussion is divided into five parts:

- System Description (Paragraph 4.1)
- Module Development (Paragraph 4.2)
- 4 x 4 Array System (Paragraph 4.3)
- 4 x 4 Array Tests (Paragraph 4.4)
- Future Array Consideration (Paragraph 4.5)

4.1 4 X 4 TRANSMITTING/RECEIVING ARRAY SYSTEM DESCRIPTION

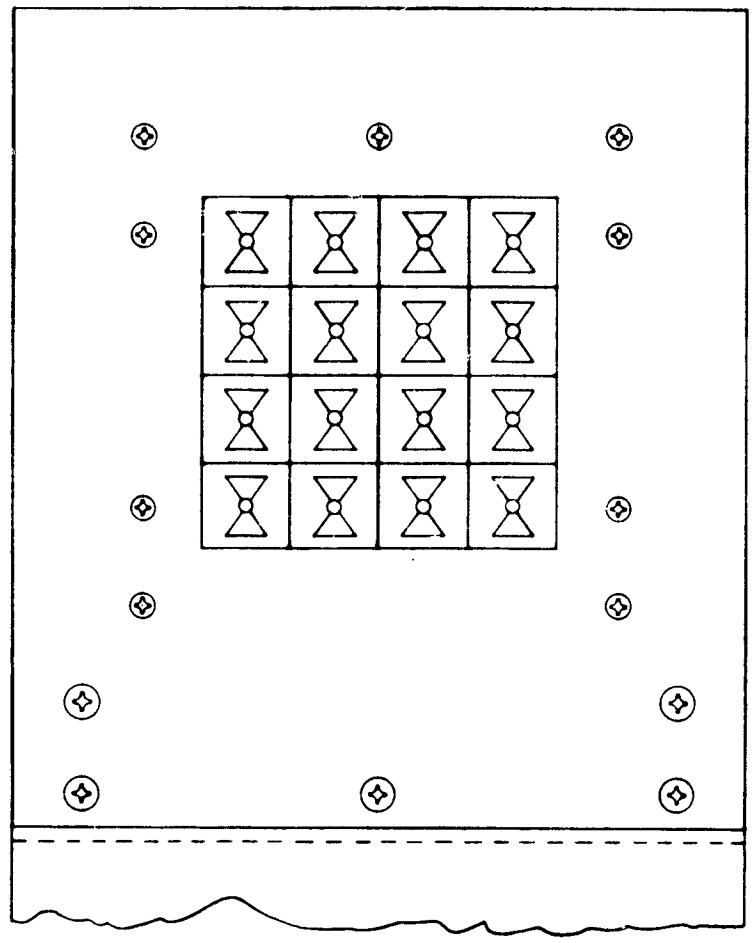
Figure 3 is a top assembly drawing showing the 4 x 4 Transmitting/Receiving Phased Array Antenna developed by Ryan. This C-Band, phased array radar consists of 16 identical transmitting/receiving modules. The radar antenna system, as shown, also includes interconnection boards to distribute the required inputs to each module and combine output signals from all modules. Additionally, a beam steering matrix box is shown which allows the transmitted and received beam patterns to be electronically steered in azimuth and elevation.

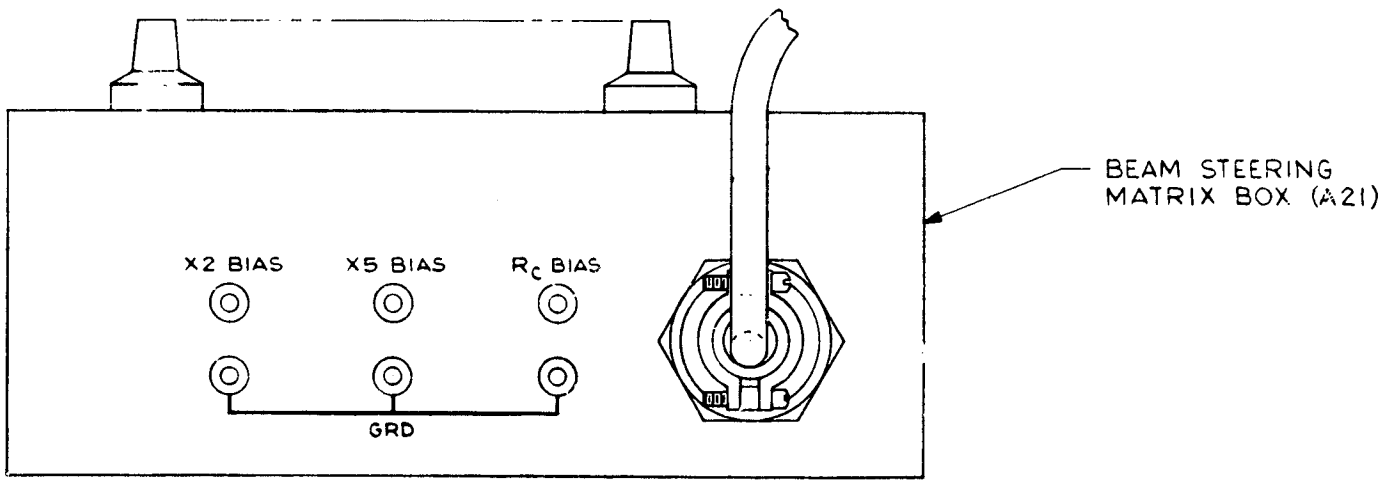
The system block diagram is shown in Figure 4. The block diagram of only one module is shown since all modules are identical. The right hand portion of Figure 4 indicates the auxiliary equipment needed to operate the 4 x 4 phased array antenna. Figure 5 is the system schematic diagram and shows each of the block diagram functions in more detail.

The transmitted energy of each module is centered at 5.75 GHz. The transmitter output is pulsed with a maximum allowable duty cycle of 0.0125. This transmitter output is generated in the following manner. One common 575 MHz signal generator supplies 64 watts of peak power. This power is divided into 16 equal parts by the 575 MHz power divider, A17. This divided power, 4 watts peak, is applied to each module. Each module transmitter has two SRD frequency multipliers in series. The phase of the transmitted power from each module is controlled by varying the dc bias across the SRD in the x 2 multiplier. This phase shift is further increased by the x 5 multiplier. The x 5 multiplier has a mechanical cavity output to select the desired harmonic. The two series multipliers have a total multiplication ratio of x 10; hence a 5.75 GHz pulsed signal of approximately 300 milliwatts is radiated from each module during the radar transmitting period.

In the receiving mode, the received signal at each module antenna is connected to the balanced mixer via the duplexer (circulator). The local oscillator (LO) signal for each module is generated by a x 8 SRD multiplier. The LO multiplier input is furnished by a 711 MHz signal generator. The required cw power amplitude at 711 MHz is 1.3 watts and this power is divided 16 ways by A18. The resultant 80 milliwatts at each A18 power divider output provides the LO multiplier drive. Each module has an isolation amplifier preceding the LO multiplier to prevent module interaction. The receiver pattern beam steering is accomplished by varying the phase of each LO output by controlling the dc bias across the SRD in the LO multiplier. The receiver LO output is passed through a bandpass filter to select the 8th harmonic and reject all others. The LO output, 4 milliwatts at 5.688 GHz, serves as the balanced mixer reference signal.

Any received signal at the antenna is mixed to a resultant 60 MHz IF voltage. This IF signal is amplified by the 60 MHz amplifier within each module. The IF outputs of each of the 16 modules in the array are processed by the IF combiner network, A20, to form a Σ (summation) signal, Δ_{AZ} (difference pattern in azimuth) and Δ_{EL} (difference pattern in elevation).





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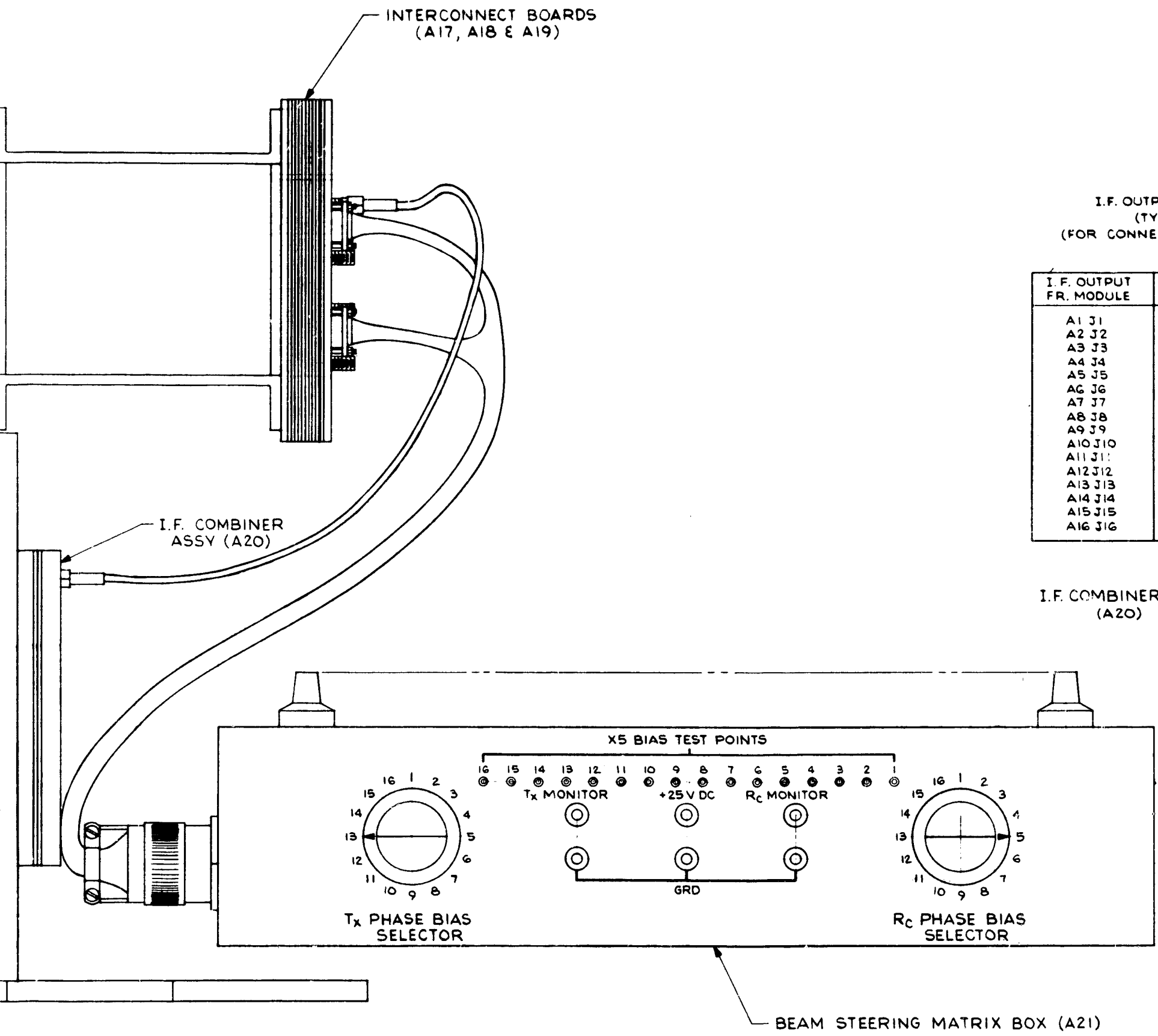


I.F. OUTPUT COA
(TYP 16 PL
(FOR CONNECTIONS

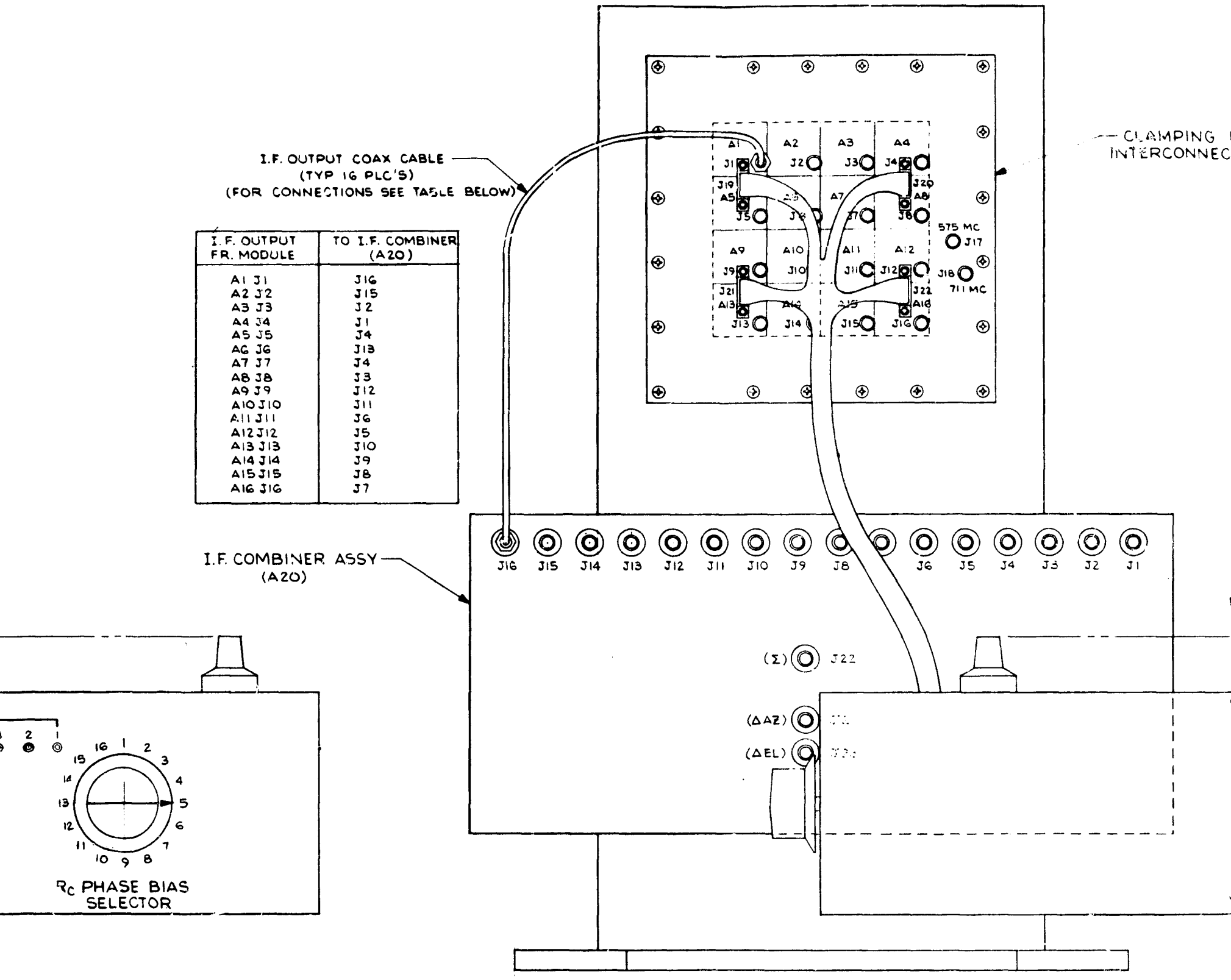
I. F. OUTPUT FR. MODULE	TO I.F. (A
A1 J1	J16
A2 J2	J15
A3 J3	J2
A4 J4	J1
A5 J5	J4
A6 J6	J13
A7 J7	J4
A8 J8	J3
A9 J9	J12
A10 J10	J11
A11 J11	J6
A12 J12	J5
A13 J13	J10
A14 J14	J9
A15 J15	J8
A16 J16	J7

I.F. COMBINER ASSY
(A20)

Foldout #2

Fold

NOTES:
1. FOR SCHEMATIC SE
2. FOR MODULE ASSY
SEE DIAGRAM 59858



Figure

Fold out #3

NOTES:
1. FOR SCHEMATIC SEE DWG 5985B114.
2. FOR MODULE ASSY & INTERCONNECTIONS, SEE DIAGRAM 5985B103.

I.F. OUTPUT FR. MODULE	TO I.F. COMBINER (A20)
A1 J1	J16
A2 J2	J15
A3 J3	J2
A4 J4	J1
A5 J5	J4
AG J6	J13
A7 J7	J4
A8 J8	J3
A9 J9	J12
A10 J10	J11
A11 J11	J6
A12 J12	J5
A13 J13	J10
A14 J14	J9
A15 J15	J8
A16 J16	J7

RELEASE & DATE	QTY REQD PER ASSY	CODE IDENT	PART NUMBER

FINAL ASSY	NEXT ASSY	NEXT ASSEMBLY	USED ON
QTY REQUIRED		APPLICATION	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEM APPLIED OR PLATED FINISHES
TOLERANCES

LINEAR		ANGULAR
X	±.1	EXCL OF SHEET
XX	±.03	METAL FLANGES
XXX	±.010	±0° 30'

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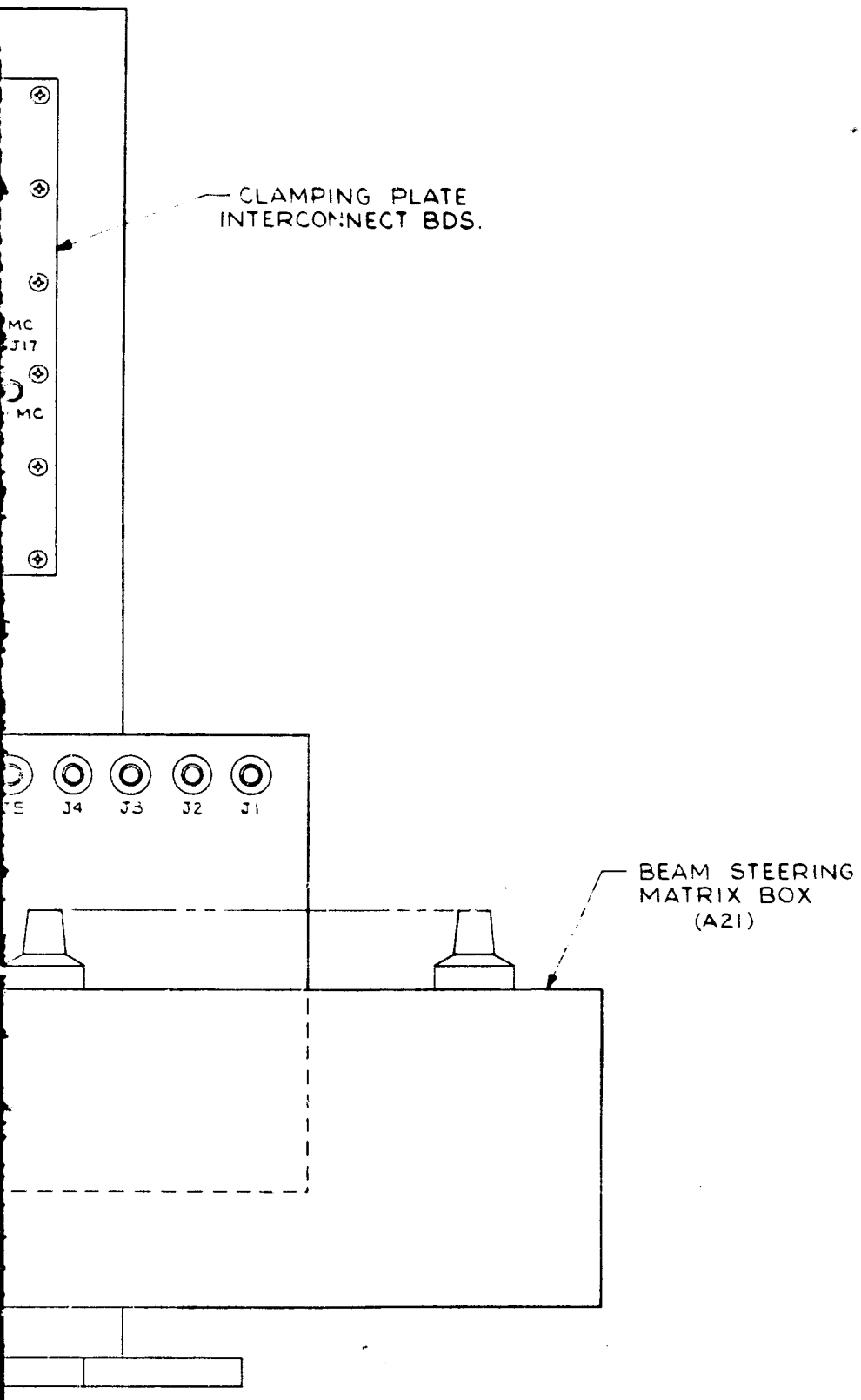

Foldout #4

Figure 3 CAT Radar 4 x 4 Array

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			LIST OF MATERIAL						

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TOLERANCES
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PROJECT	[illegible]	2/3/69

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DESIGN APPROVAL

RYAN
RYAN AERONAUTICAL COMPANY
SAN DIEGO, CALIFORNIA 92112

C.A.T. RADAR
4 × 4 ARRAY

SIZE	CODE IDENT NO.	NUMBER	REV SYM
	78022	59858000	

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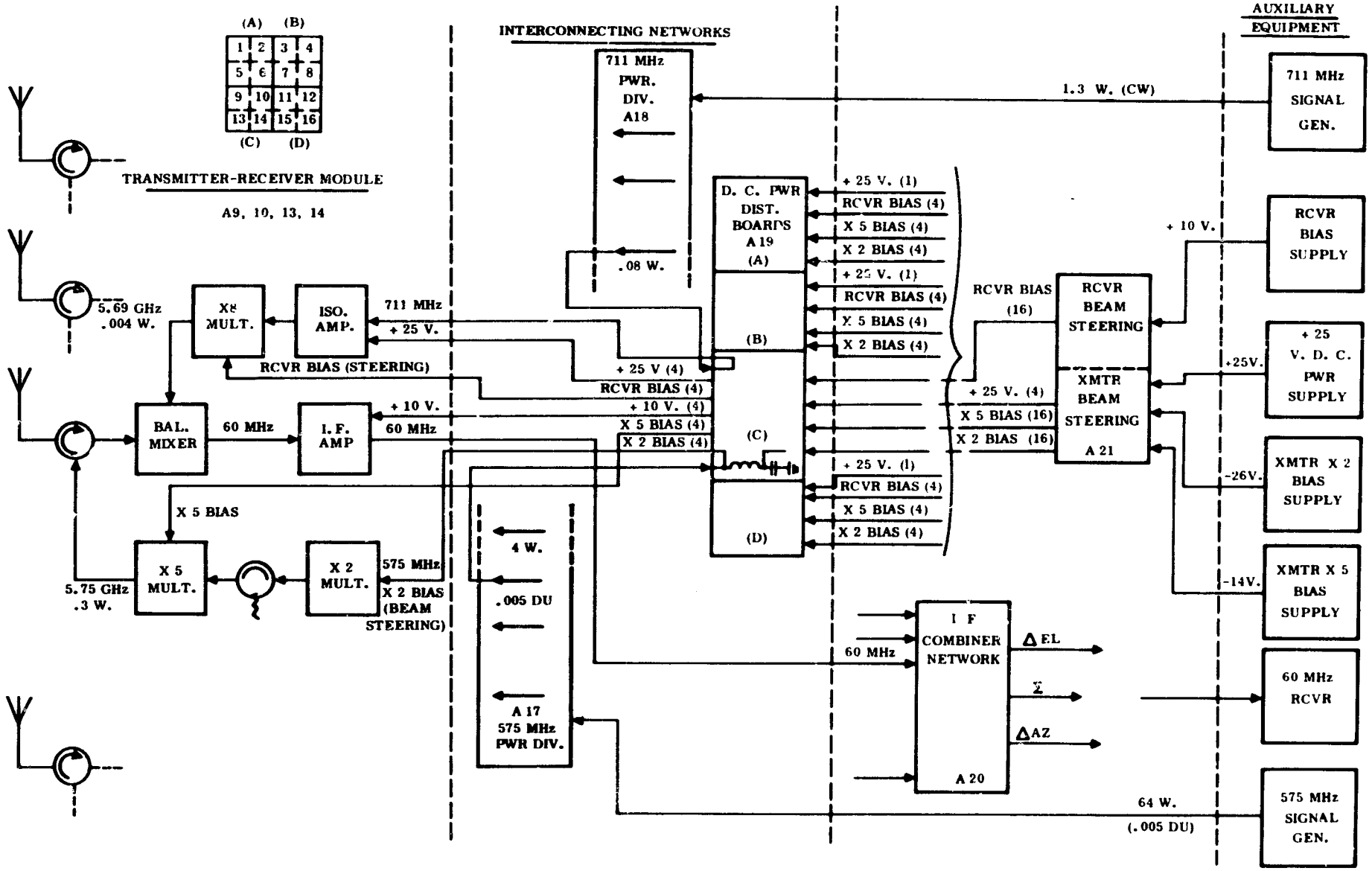
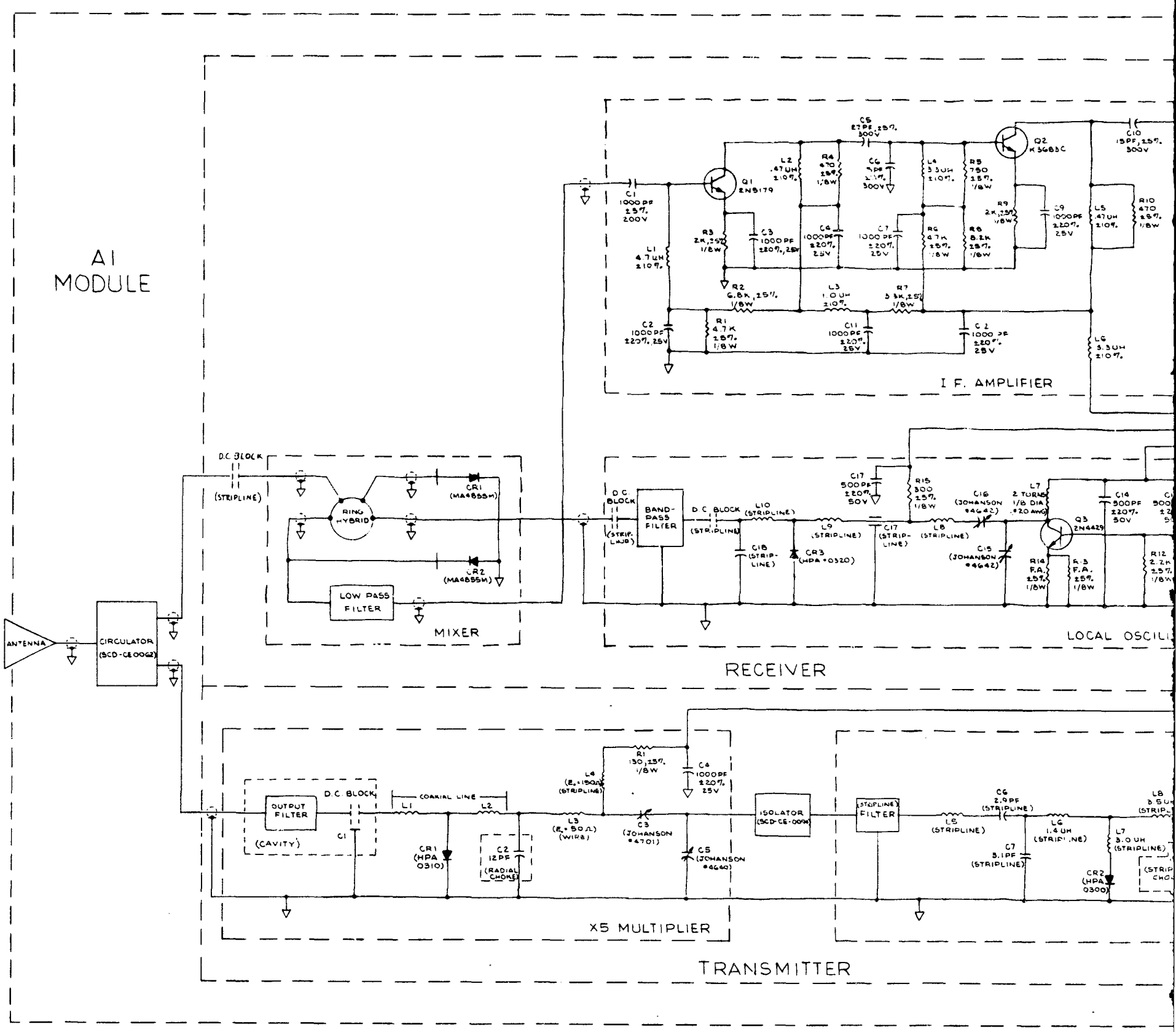


Figure 4 System Block Diagram, 4 x 4 CAT Antenna Array



A2 THRU A16 MODULE IDENTICAL TO A1

Foldout #1

A20
I.F. COMBINER

A19 PWR DISTRIBUTION BOARDS

(INTERCONNECT BDS A17, A18 & A19)

575 MC PWR DIVIDER
A17

711 MC PWR DIVIDER
A18

A16

A15
(A15 THRU A1 IDENTICAL TO A16)

J22

T_x BIAS X2 MOD A11
T_x BIAS X2 MOD A12
T_x BIAS X2 MOD A15
T_x BIAS X2 MOD A16
GRD (SHIELD)
(NOT USED)
R_c BIAS MOD A11
R_c BIAS MOD A12
R_c BIAS MOD A15
R_c BIAS MOD A16
+25V DC MOD A11, A12, A15 & A16
T_x BIAS X5 MOD A11
T_x BIAS X5 MOD A12
T_x BIAS X5 MOD A15
T_x BIAS X5 MOD A16

TO A2J1 (BEAM STEERING)

J1

(COAX CABLE - 16 PLC'S)

J19

T_x BIAS X2 MOD A6
T_x BIAS X2 MOD A5
T_x BIAS X2 MOD A2
GRD (SHIELD)
R_c BIAS MOD A6
R_c BIAS MOD A5
R_c BIAS MOD A2
R_c BIAS MOD A1
+25V DC MOD A1, A2, A5 & A6
T_x BIAS X5 MOD A1
T_x BIAS X5 MOD A2
T_x BIAS X5 MOD A5
T_x BIAS X5 MOD A6
T_x BIAS X2 MOD A1
(NOT USED)

TO A2J1 (BEAM STEERING)

J2 J3 J4 J5 J6 J7 J8 J9 J10 J11

A2 A13 A16 A5 A6 A11 A12 A9 A10 A7

FR. MODULE I.F. OUTPUT

MOD A11 MOD A12 MOD A15 MOD A16 +10V DC

+25V DC

MOD A6 MOD A5 MOD A2 +10V DC IN758 1.6K 25% 1/4W 5.3 UF 15V 1.6K 25% 1/4W

+25V DC

MOD A2 MOD A5 MOD A6

.15UH 500PF

MOD A4 MOD A8 MOD A3 MOD A7 MOD A2 MOD A6 MOD A1 MOD A5 MOD A9 MOD A13 MOD A10 MOD A14 MOD A11 MOD A15 MOD A12 MOD A16

100Ω

MOD A1 MOD A2 MOD A3 MOD A4 MOD A5 MOD A6 MOD A7 MOD A8 MOD A9 MOD A10 MOD A11 MOD A12 MOD A13 MOD A14 MOD A15 MOD A16

100Ω

MOD A5 MOD A4 MOD A7 MOD A8 +10V DC +25V

MOD A3 MOD A4 MOD A7 MOD A8

MOD A9 MOD A10 MOD A13 MOD A16 +10V

MOD A9 MOD A10 MOD A13 MOD A14 +25V

C10 15PF, ±5%, 300V

L5 47 UH ±10%

R10 470 ±5% 1/8W

L6 3.3 UH ±10%

C14 500PF ±20% 50V

C13 500PF ±20% 50V

R11 22K ±5% 1/8W

R12 2.2K ±5% 1/8W

C12 100PF ±20% 50V

CAL OSCILLATOR

R2 180, 15% 1/8W

L8 3.5 UH (STRIPLINE)

L7 3.0 UH (STRIPLINE)

L9 (STRIPLINE)

C9 (STRIPLINE)

C8 11PF (STRIPLINE)

CHOKE

C10 (STRIPLINE)

CR2 HPA 5300

X2 MULTIPLIER

R3 100Ω ±5% 1/4W

F1

E2

TP1C

R1 (VARIABLE)

R2 47Ω ±5% 1/4W

C1 (VARIABLE)

L2 4.7 UH

L1 .82 UH

J16

J15

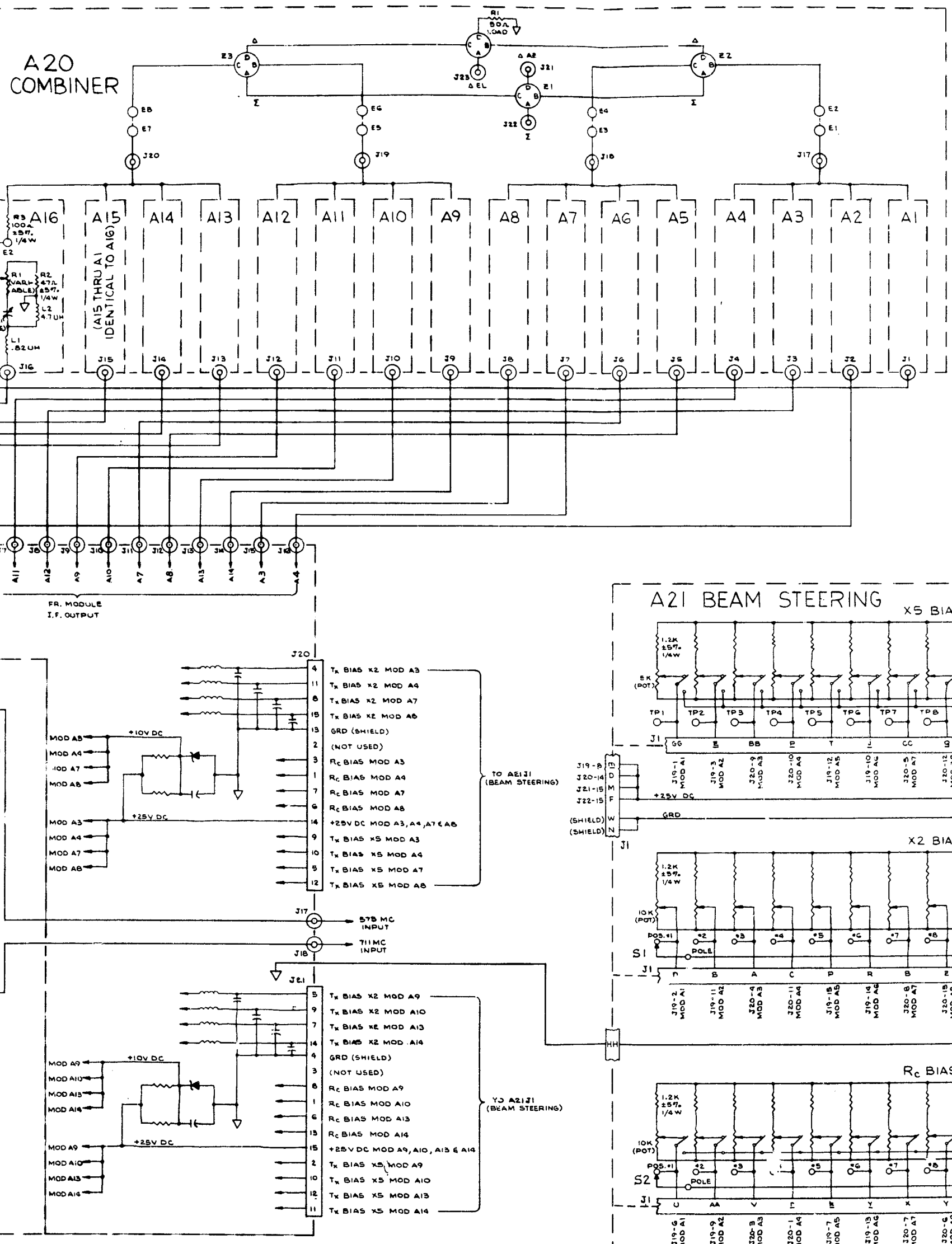
E8

E7

J2

Foldout #2

A20 COMBINER



A21 BEAM STEERING

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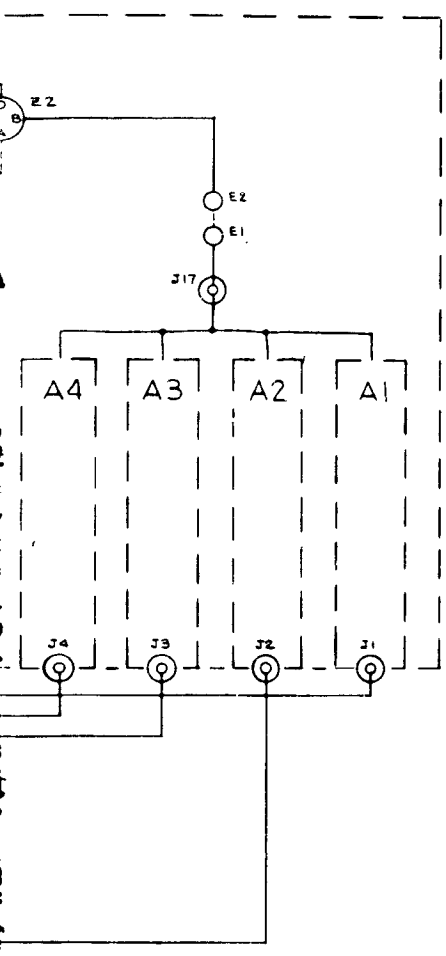

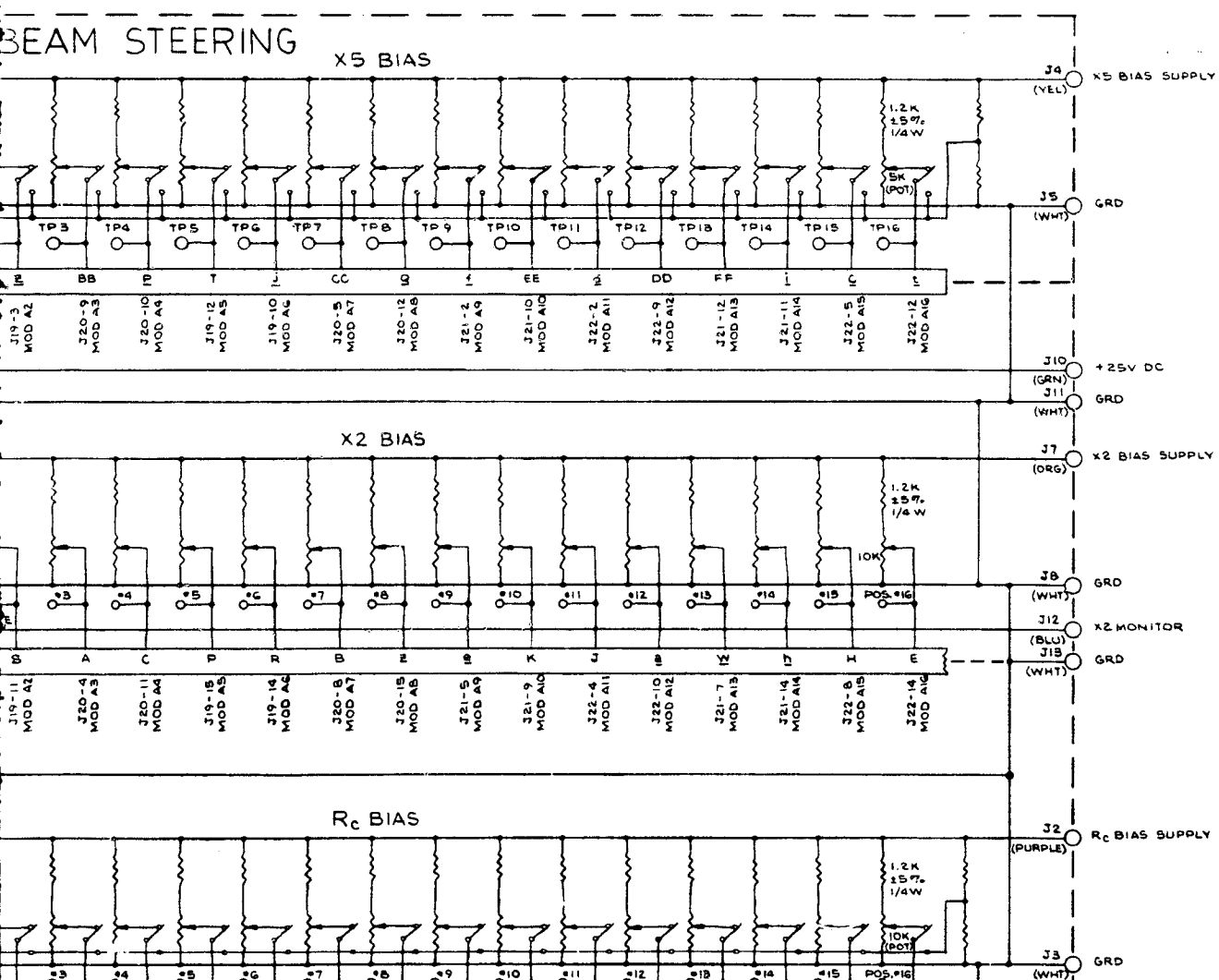

Figure 5 Schematic Diagram, CAT Rad

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Foldout #5

5 Schematic Diagram, CAT Radar 4 x 4 Array 17/18

ITEM NO.	QTY REQD PER ASSY	RELEASE & DATE

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PROJECT		

DESIGN ACTIVITY APPROVAL
DESIGN APPROVAL

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SCHEMATIC DIAGRAM, C.A[illegible] RADAR 4 x 4 [illegible]RRAY

SIZE	CODE IDENT NO.	NUMBER	REV SYS
	78022	59853114	

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Power distribution network, A19, distributes dc power to the modules as required and connects the transmitter and receiver beam steering functions.

The electronic beam steering of the array transmitter and receiver functions is accomplished in an open loop manner. The phase control for the transmitter and receiver portion of each module is generated as a variable dc voltage in A21, the beam steering matrix box. Thirty-two potentiometers are provided, i.e., sixteen phase controls for the sixteen transmitters and sixteen phase controls for the receivers.

Each potentiometer must be adjusted during beam steering to properly control the phase of each module. The next section basically develops the phase relationships between the modules within the array to achieve beam steering of either the transmitter or the receiver.

4.1.1 Beam-Steering Function, ϕ for a Planar Array

In order to beam steer the wavefront of a two dimensional array in direction $\hat{R}_T$ (see Figure 6), the phase of each (M,N) element must be controlled in accordance with the following function:

$$\phi_{(M,N)} = K(M-1)\, a_y \cos\theta_o \sin\psi_o + K(N-1)\, a_z \sin\theta_o$$

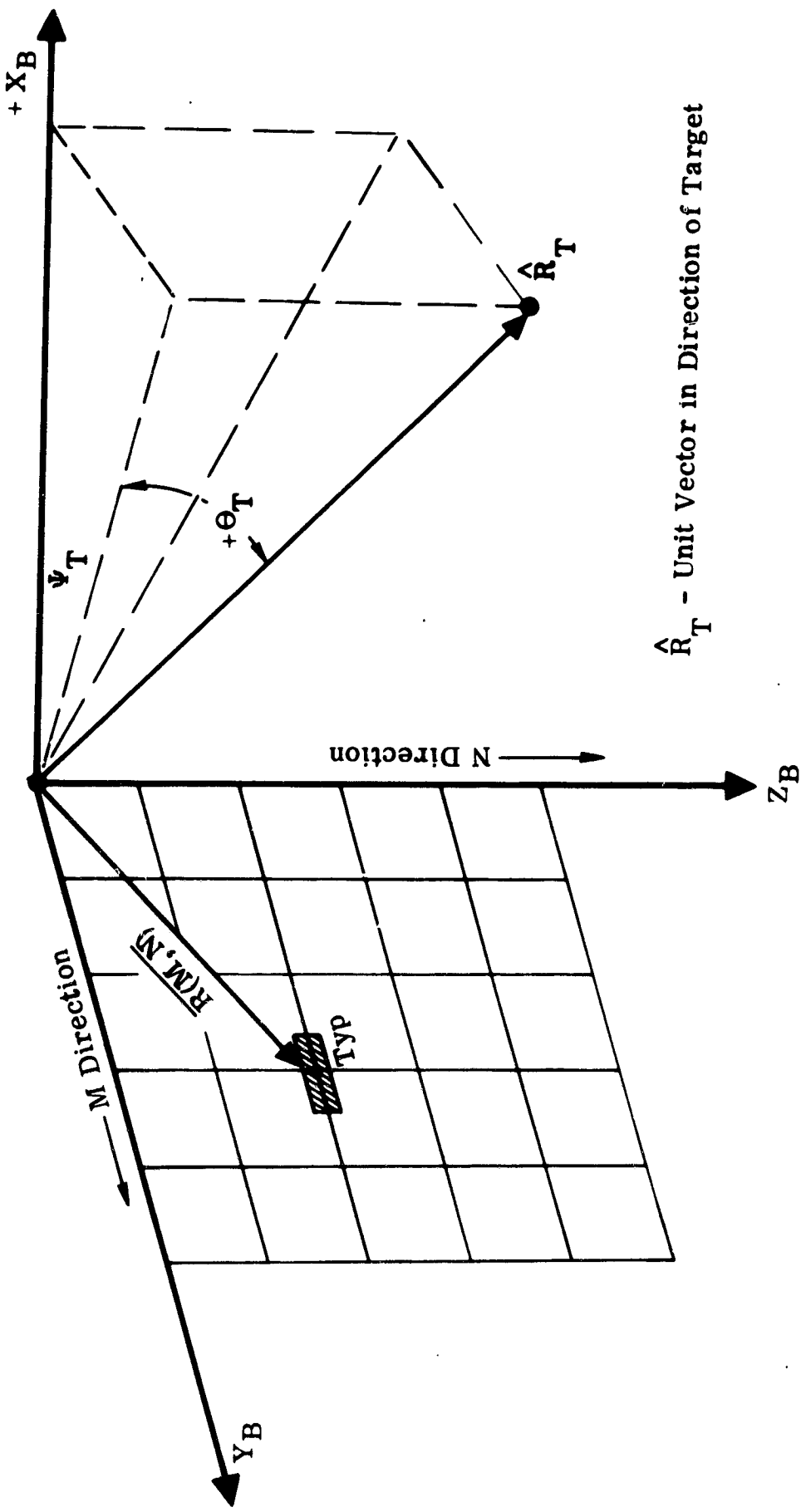
where

$\phi_{(M,N)}$ is the phase at the $(M,N)^{th}$ element

θ_o is beam pointing angle in the pitch plane

ψ_o is beam pointing angle in the yaw plane

a_y is the element spacing in the Y(M) direction of the array (Referenced to M = 1)



$\hat{R}_T$ - Unit Vector in Direction of Target

Figure 6 Phased Array Geometry

and

a_z is the element spacing in the Z(N) direction of the array (Referenced to N = 1)

Figure 7 indicates how electronic beam steering is implemented for a 4 x 1 linear array. In this example, the ϕ (N) function is referenced to the middle of the array. Design of the beam steering circuitry is simpler with this mid-array referencing.

For this array $a_z = d$

$$\phi_{(N)} = Kd \left[(N - 1) - \frac{X - 1}{2} \right] \sin \theta_o$$

where

X = total number of modules in the array

$K = \frac{2\pi}{\lambda}$

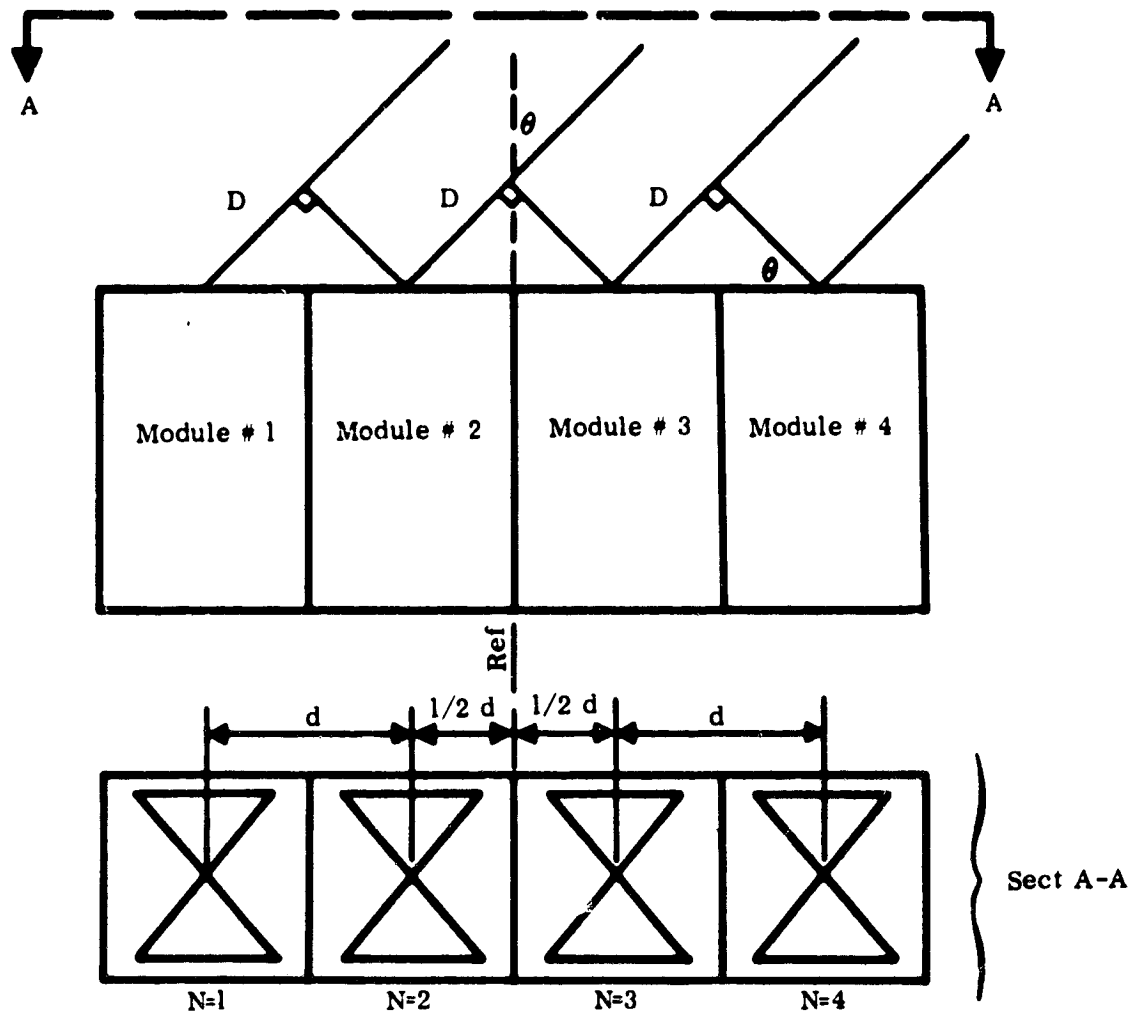
d = spacing between modules

$1 \leq N \leq 4$, for this 4 x 1 antenna

The values for ϕ are shown for each of the 4 elements, when $\theta_o = 45°$ and where the spacing is 0.47 λ.

4.1.2 Formation of the Summation Pattern

The summation pattern is formed by adding the IF outputs of each of the elements in the array. It can be noted that all element IF outputs will be of the same phase when the wavefront is beam steering in one target direction.



D = d sin θ (Delay of Received Signal in Relation to Phase of Adjacent Module)

d = Module Spacing θ_o = Beam Steering Angle

$$\text{Also } \theta(N) = 2\pi \left(\frac{d}{\lambda}\right)\left[(N-1) - \left(\frac{X-1}{2}\right)\right] \sin\theta_o \; (N=1,4)$$

Required Phase Shift to Beam Steer

MODULE	#1	#2	#3	#4
(N) Steering Command	$2\pi\left[\frac{-3/2\ d}{\lambda}\right]\sin\theta$	$2\pi\left[\frac{-1/2\ d}{\lambda}\right]\sin\theta$	$2\pi\left[\frac{+1/2\ d}{\lambda}\right]\sin\theta$	$2\pi\left[\frac{3/2\ d}{\lambda}\right]\sin\theta$
Required θ_o Shift for a 45° beam Steering Angle*	$360°\left[\frac{3(0.49\lambda)}{2}\right].707$ = 179.2°	- 59.7°	+ 59.7°	+179.2°

*Assume Module Spacing d .47 λ

Figure 7 Simple Phase Shift Computations for a 4-Element Linear Array

4.1.3 Formation of the Difference Pattern

The difference pattern is obtained by (1) dividing the aperture into two (for each axis); (2) combining the IF outputs of the elements in one-half of the aperture π radians out of phase with the other half.

4.1.4 Module Mounting Considerations

The modules have been mounted in the 4 x 4 planar array so the geometric center of each antenna element is spaced 0.47 λ from each adjacent module (in both planes).

Previous Ryan computer analysis has shown that a spacing of $\lambda/2$ (or slightly less) is needed to prevent the formation of grating lobes as the main pattern is electrically beam steered.

4.2 TRANSMIT/RECEIVER MODULE CONFIGURATION

The transmit receiver modules are all identical. Most of the module components have been developed and fabricated using stripline techniques.

Figure 8 is a block diagram of the transmit/receive module and Table I tabulates the module characteristics. Figure 9 is a photograph of one module completely assembled.

Each of the module components, as listed in Table I, is discussed in the following paragraphs.

4.2.1 Antenna Element

Figure 10 shows the "bow-tie" cavity-backed stripline dipole. A Lamicoid teflon fiberglass board, approximately $1/4\lambda$ thick, is copper plated on all sides. The radiating element is etched on the forward surface. The

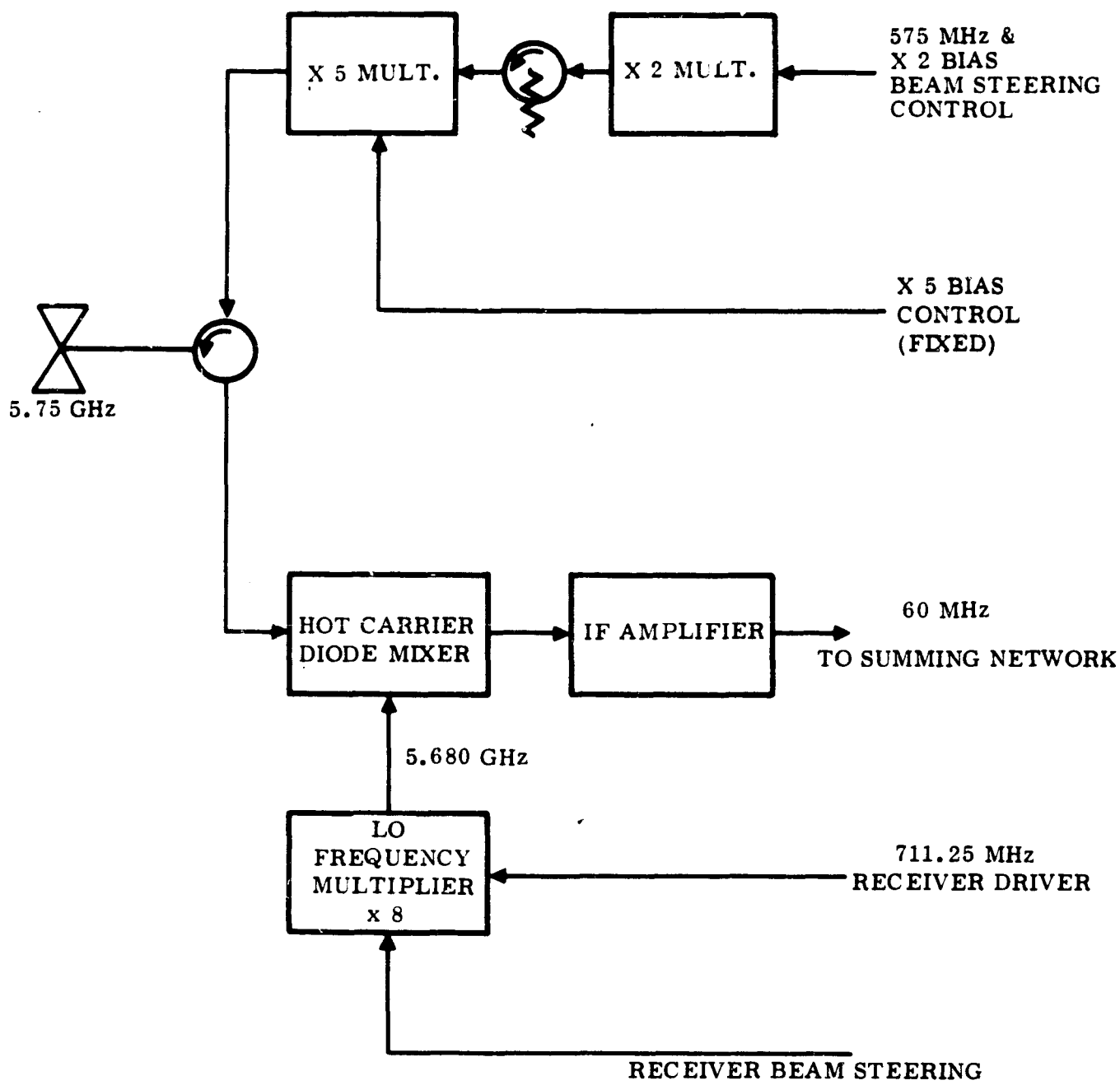


Figure 8 Block Diagram, C-Band Transmitter/Receiver Module

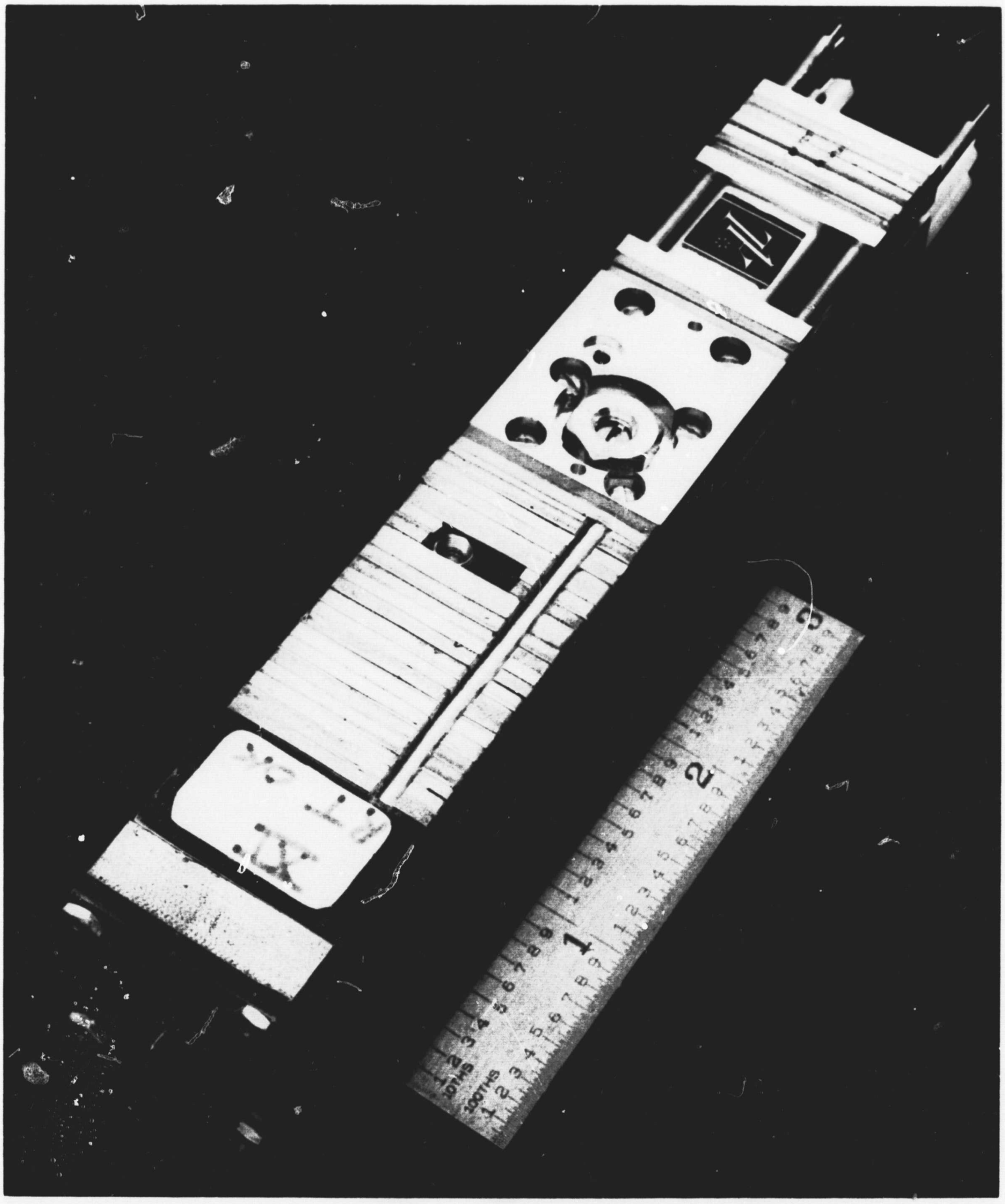


Figure 9 Assembled C-Band Transmit/Receive Module

TABLE I. MODULE CHARACTERISTICS

Carrier Frequency:		5.75 GHz ±1%
Antenna Element: - Type		"Bow-Tie" Cavity-Backed Dipole in Stripling Polarization - Linear-Vertical Gain - approx. 6 db
Duplexer:		Circulator SCD-CE-0094
Insertion loss		< 0.6 db
Isolation		> 20 db
Receiver:		
Mixer - Type		Balanced Mixer in Stripline
Diodes		Schottky - MA4855
Noise Figure		7 - 9 db
AM Rejection		≥ 22 db
Local Oscillator - Type		X8 SRD Multiplier (Shunt)
SRD Type		HPA 0320
Input Frequency		711 KHz ±1%
Output Filter		Interdigital in Stripline
IF Amplifier - Center Frequency		60 MHz
Bandwidth		19 MHz
Gain		27 db
Noise Figure		< 2 db
Transmitter:		
First Multiplier		x 2 SRD Multiplier (Shunt)
SRD Type		HPA 0300
Output Filter		Interdigital in Stripline

TABLE I. MODULE CHARACTERISTICS (CONT'D)

Transmitter: (Continued)	
Second Multiplier	x 5 SRD Multiplier (Shunt)
SRD Type	HPA 0310
Output Filter	Mechanical Cavity
Module Size:	
Aperture Area	0.940 inch square
Length	5.55 inches
Module Weight:	0.537 lb. - 8.52 oz.

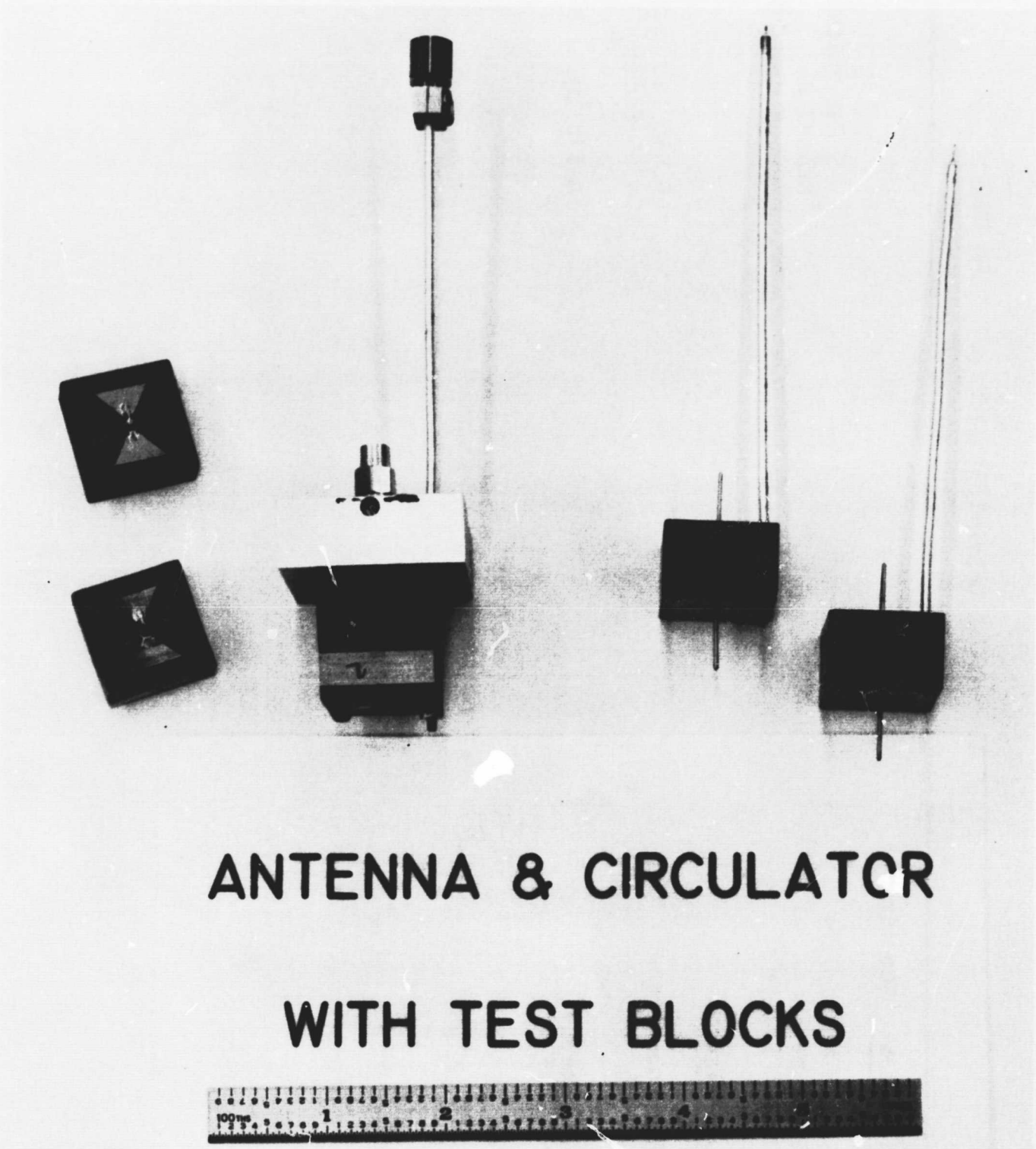


Figure 10 Antenna Element and Circulator

remaining sides form the cavity behind the radiating element. The dipole is connected to a balun, which converts the balanced output of the dipole to an unbalanced input for the hybrid ring input.

Figures 11 and 12 show typical E and H plane patterns measured with the production configuration antenna elements. Figure 13 is a Smith chart of the measured performance over the system bandwidth. Figure 14 shows acceptable VSWR over an extended frequency range. Antenna element gain measurements show the individual aperture gains to vary from 6.4 db to 7.5 db. Typical E-plane beamwidths are 125° and typical H-plane beamwidths are 77°

4.2.2 Duplexer

Figure 10 shows the circulator which was purchased from E & M Laboratories to provide the duplexing function for the transmit/receive module. Figure 15 shows typical data sheets indicating measured performance of two units.

4.2.3 Receiver

The receiver portion of the module includes:

- Balanced Mixer
- Local Oscillator
- I.F. Amplifier

Each of these items is discussed in the following paragraphs.

4.2.3.1 Balanced Mixer

Figure 16 shows the stripline wafers which are used in the balanced mixer. The upper assembly in the photograph is an assembled mixer in a test fixture. The ring hybrid and the stripline wafer with the two Schottky diodes

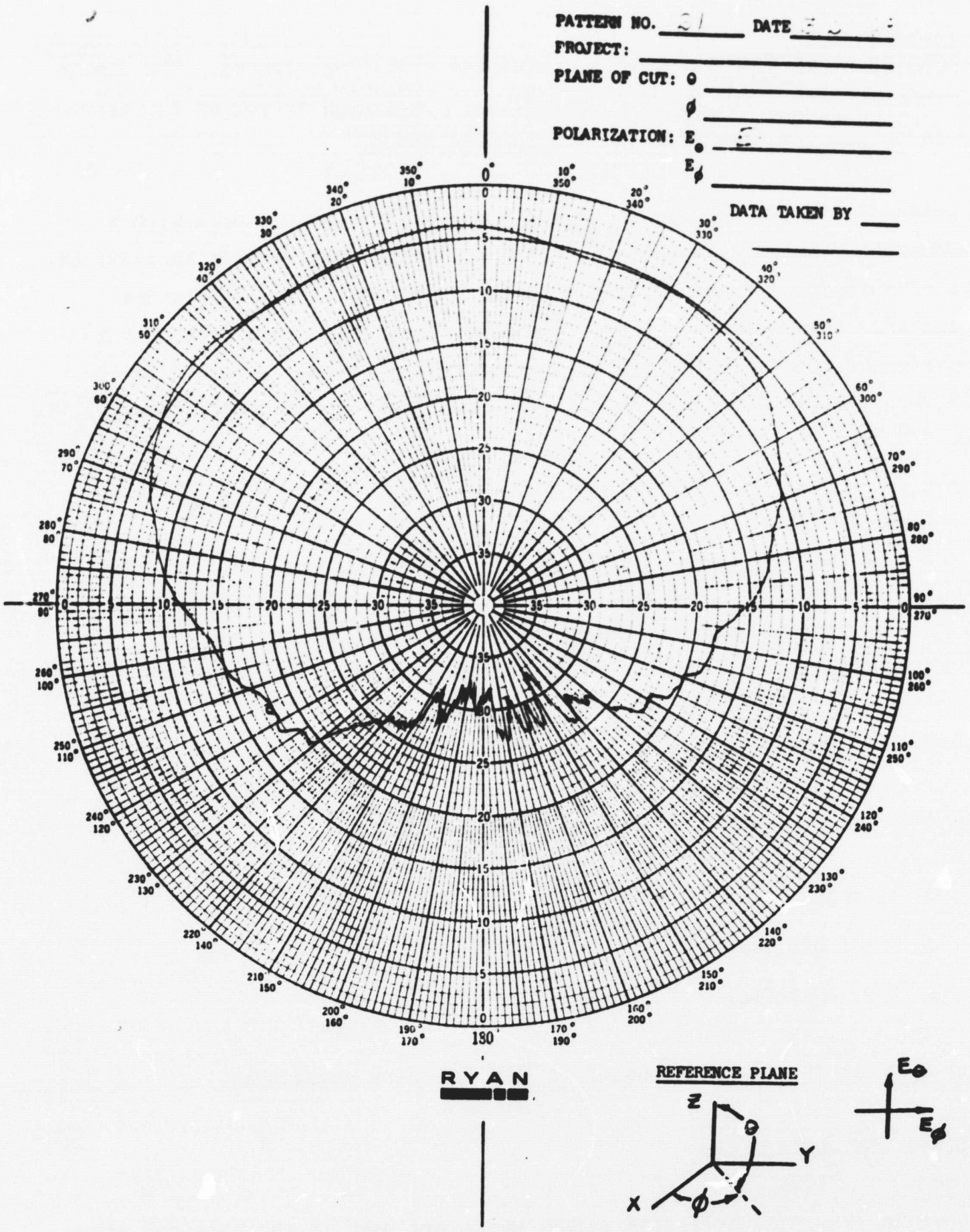


Figure 11 Typical Pattern, Antenna Element, E Plane

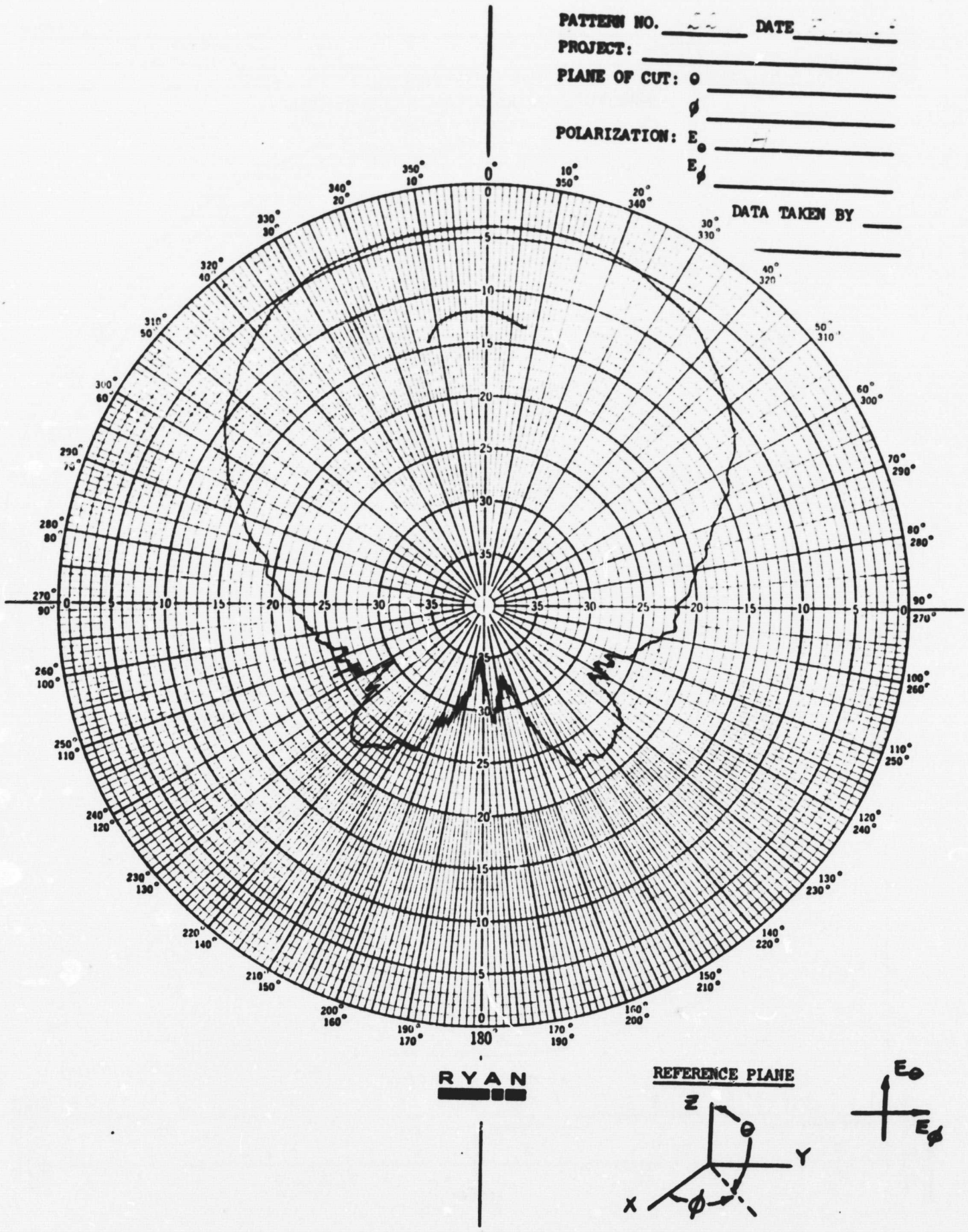


Figure 12 Typical Pattern, Antenna Element, H Plane

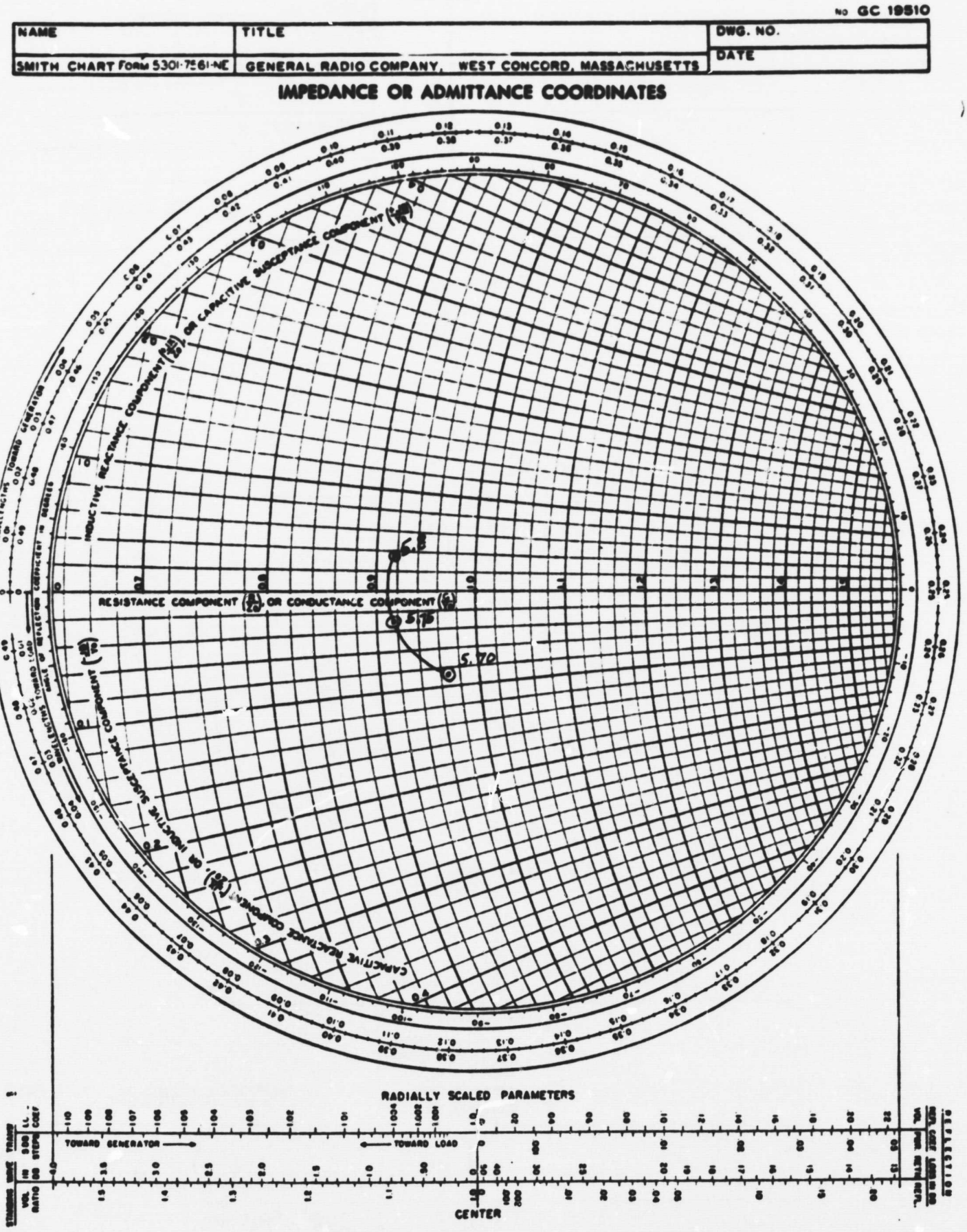


Figure 13 Impedance of Antenna Radiating Element

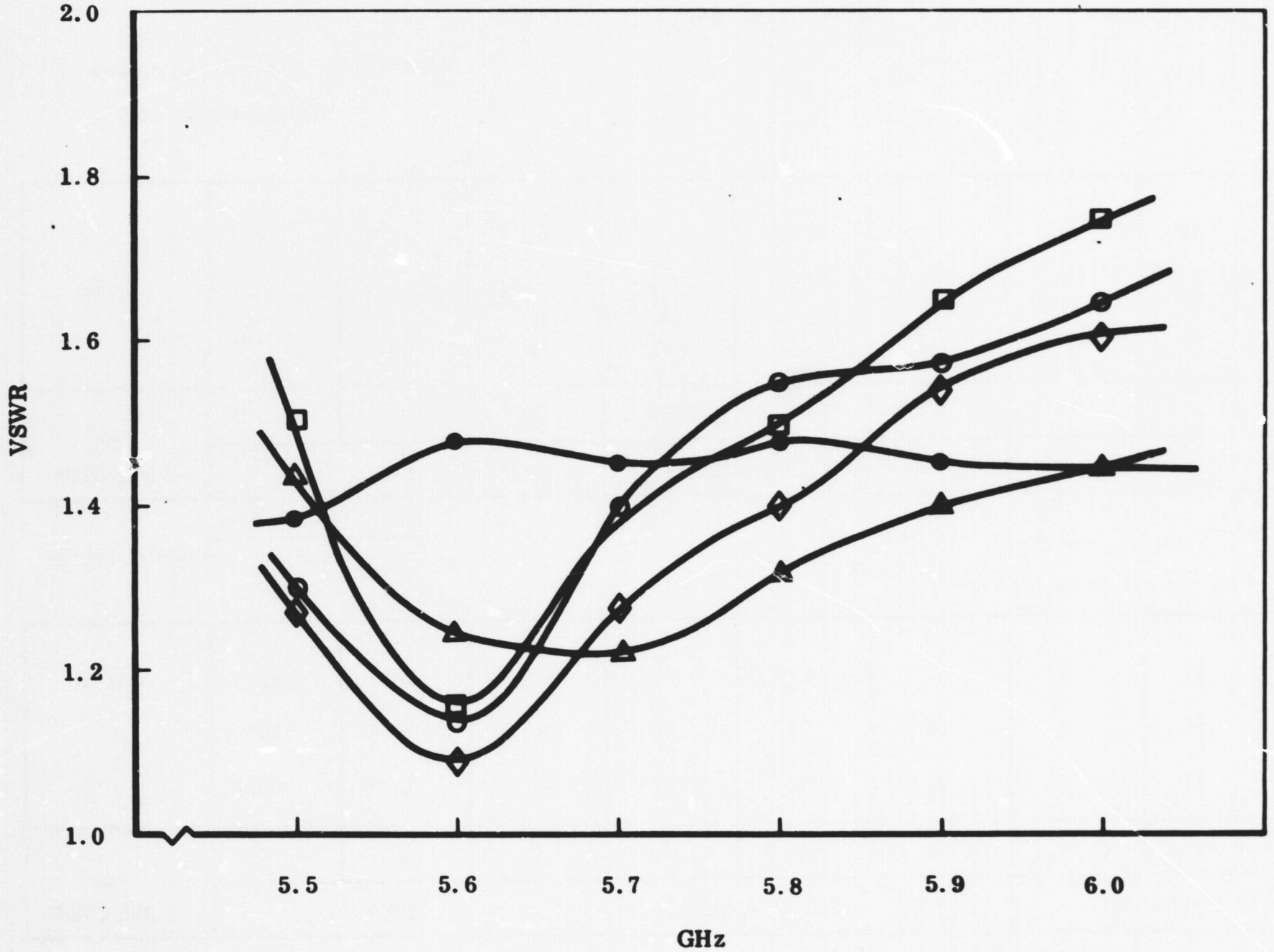


Figure 14 Antenna Element VSWR vs Frequency

TEST DATA - CIRCULATOR

Model Number C14 T12 Serial Number 112

FREQUENCY Gc	VSWR			INSERTION LOSS - DB			ISOLATION - DB		
	1	2	3	1 to 2	2 to 3	3 to 1	3 to 1	2 to 1	3 to 2
5.7	1.06	1.07	1.08	.40	.20	.40	35	41	29
5.75	1.02	1.06	1.06	.40	.15	.40	35	39	29
5.8	1.08	1.05	1.05	.40	.15	.35	34	34	23

Model Number C14 T12 Serial Number 113

FREQUENCY Gc	VSWR			INSERTION LOSS - DB			ISOLATION - DB		
	1	2	3	1 to 2	2 to 3	3 to 1	3 to 1	2 to 1	3 to 2
5.7	1.10	1.06	1.04	.50	.25	.50	23	31	22
5.75	1.09	1.05	1.05	.45	.25	.50	23	31	25
5.8	1.10	1.04	1.06	.45	.20	.45	23	31	25

E & M LABORATORIES

North Hollywood, California

Figure 15 Typical Data Sheet

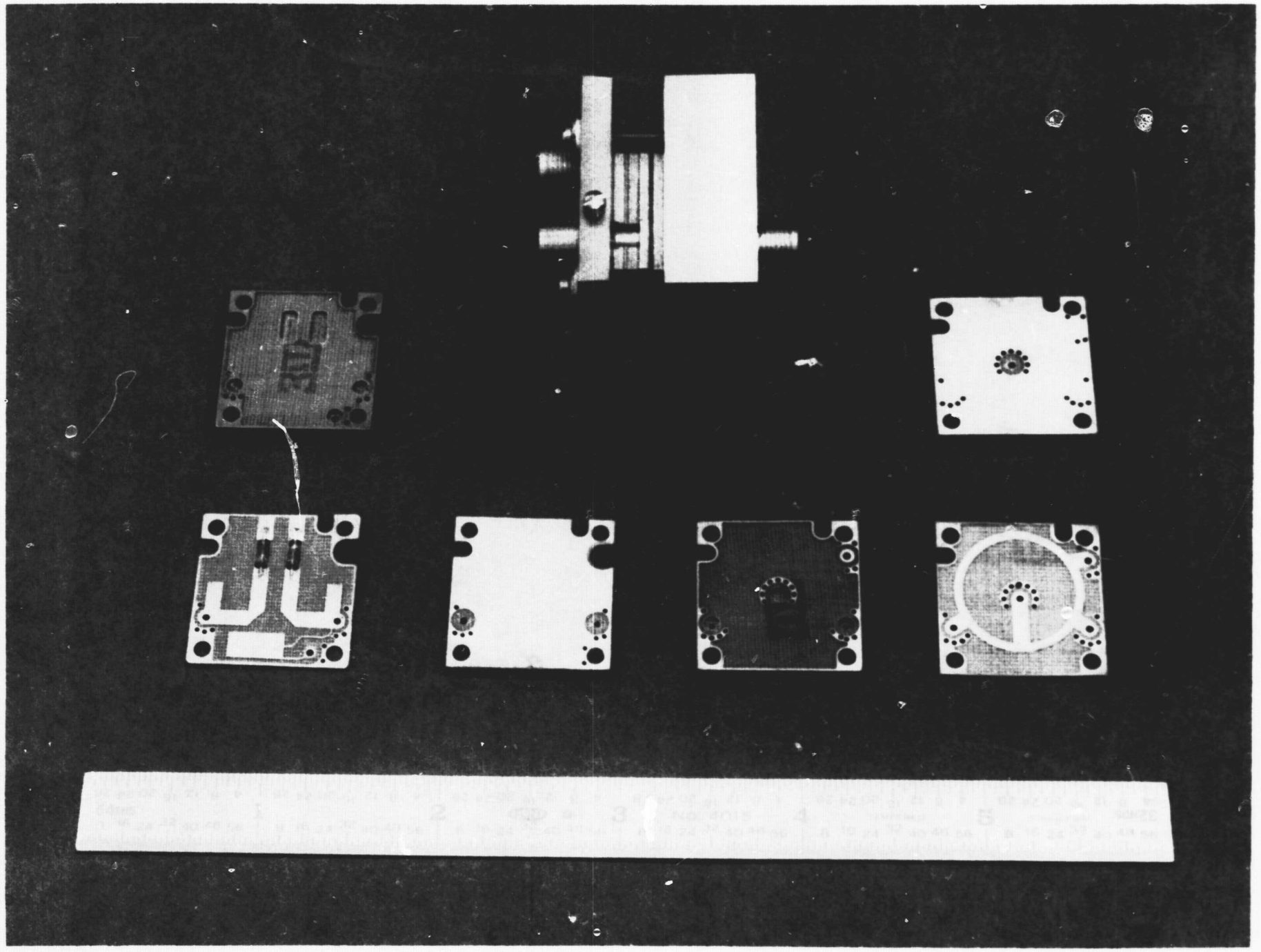


Figure 16 SDS Balanced Mixer Configuration

are in the lower row. The other four wafers provide isolation and interconnection.

Figure 17 shows typical performance measured with the stripline hybrid ring over the required frequency range. Figure 18 shows the results of diode scatter measurements of some Schottky (Microwave Associates, MA 4855) diodes.

Two tests were conducted on each of the assembled mixers. The noise figure was measured for each of the units. Figure 19 is a block diagram of the test setup used for measuring the noise figure. The HP 342A Noise Figure Meter is used in conjunction with the HP J347A Noise Tube. This noise tube is an argon gas discharge tube mounted in a waveguide section. In operation, the gas discharge tube is connected to the mixer input. The mixer output is connected to the SDS 60 MHz IF amplifier (with previously measured input noise figure). The IF amplifier output is connected to the HP 342A. The noise figure meter gates the noise source on and off. When the source is off, the noise level is that of the device and its termination. The noise figure meter automatically compares these two conditions and presents the noise figure directly. The values measured are broadband or double sideband values. Figure 20 presents noise figure data measured for five units.

Figure 21 is the block diagram for the mixer AM rejection measurement. The LO oscillator input was adjusted for 4 milliwatts. The RF signal was terminated to ground through a dc block. AM rejection was measured by alternately removing each diode of the balanced mixer and recording the ratio of the voltage output with each of the two diodes in and out of the circuit. Figure 22 shows results of some units tested over an extended frequency range.

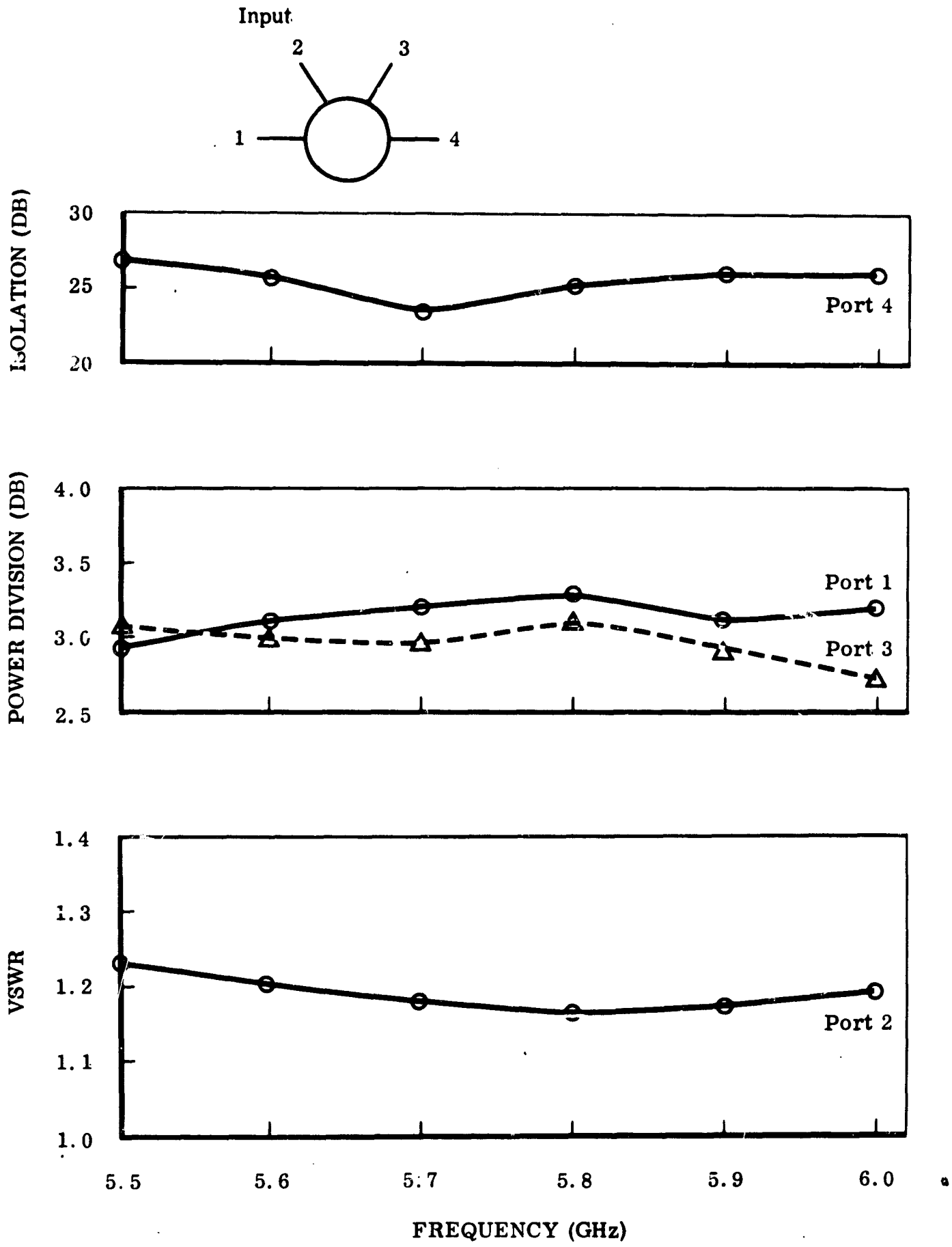


Figure 17 Typical Performance of Stripline Hybrid Ring - Model 598

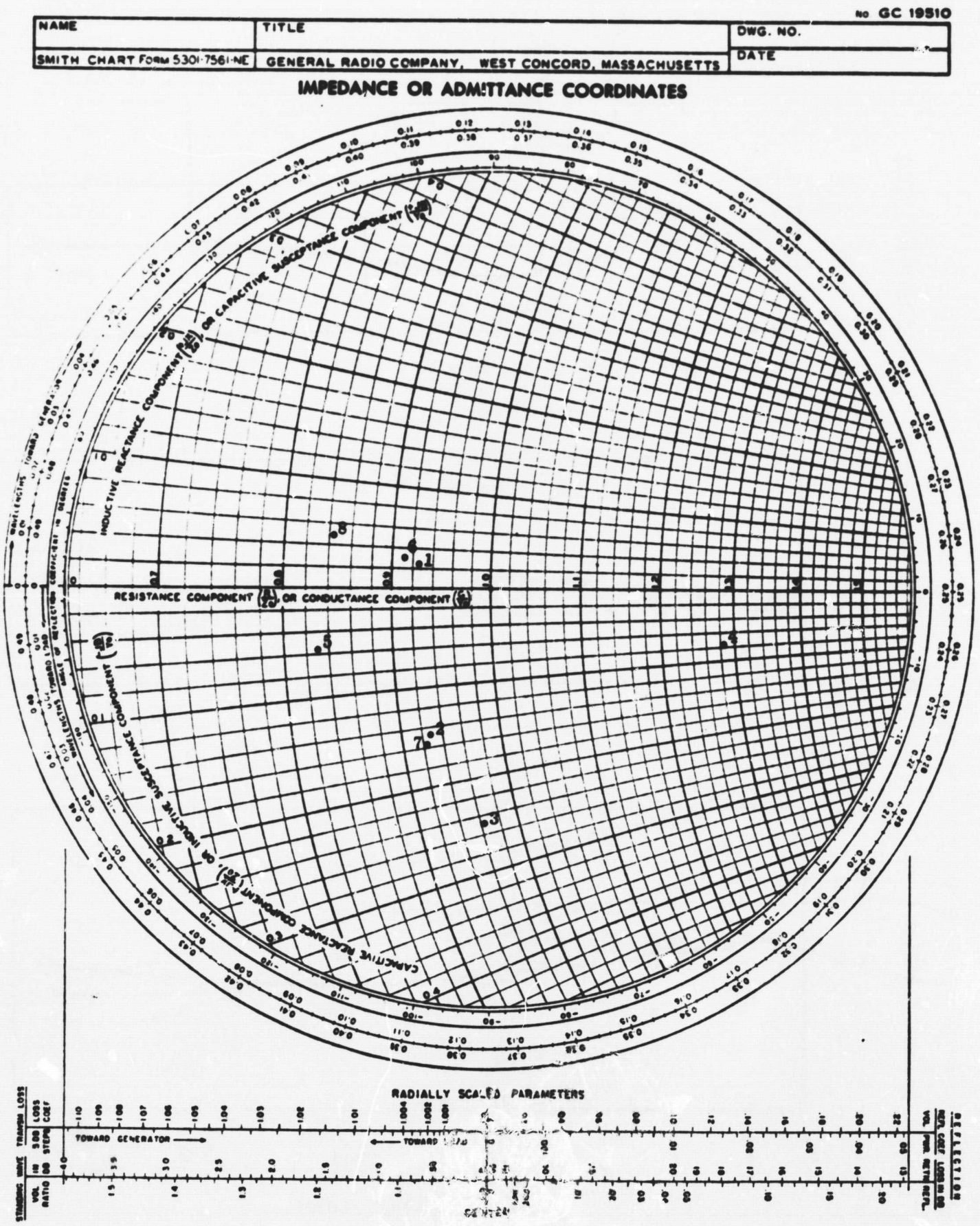


Figure 18 Impedance of MA 4855 Diodes

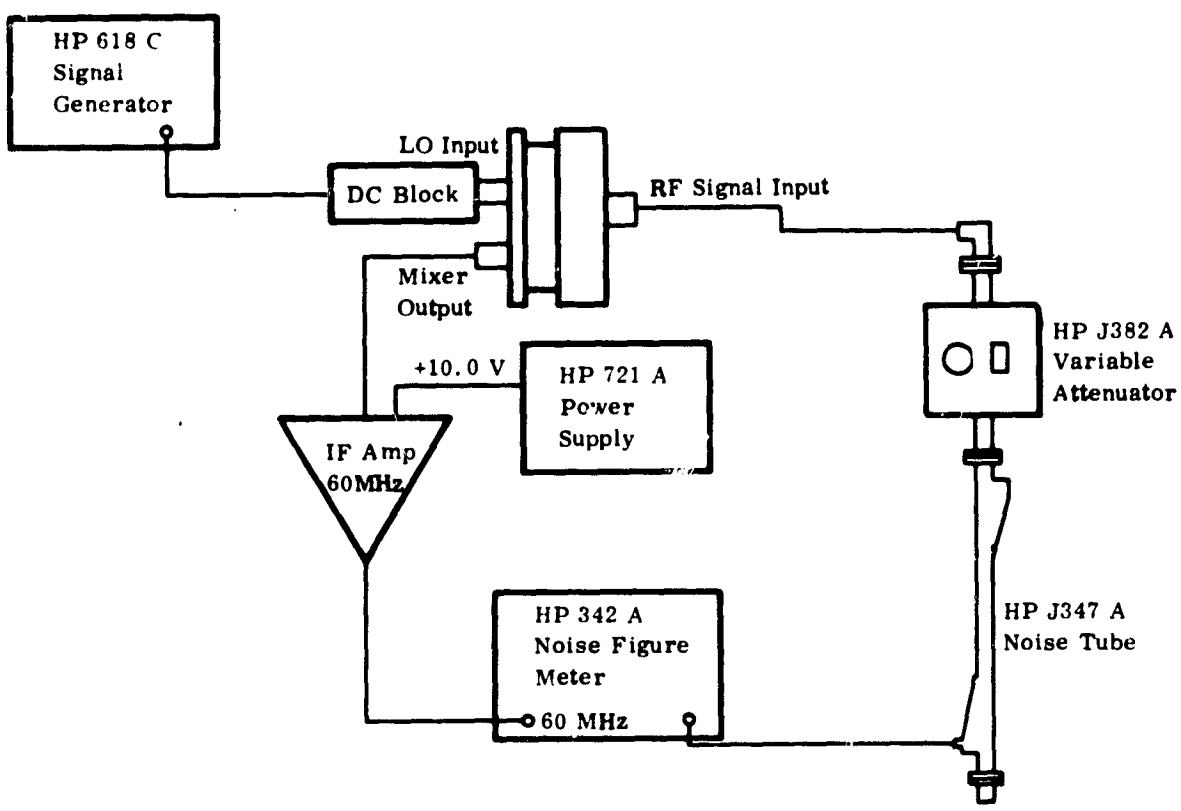


Figure 19 Mixer Noise Figure Test Setup

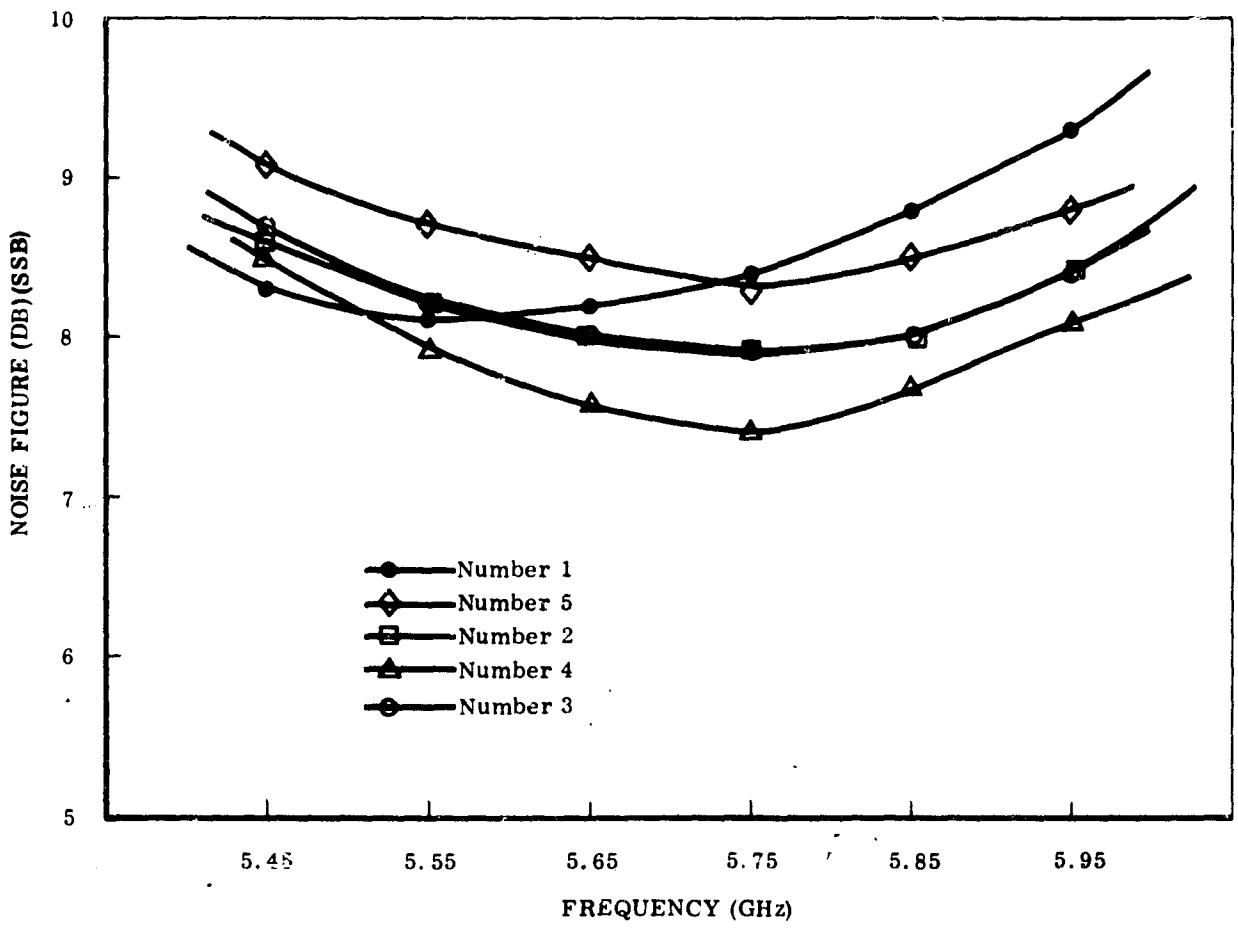


Figure 20 Balanced Mixer vs Noise Figure Characteristics

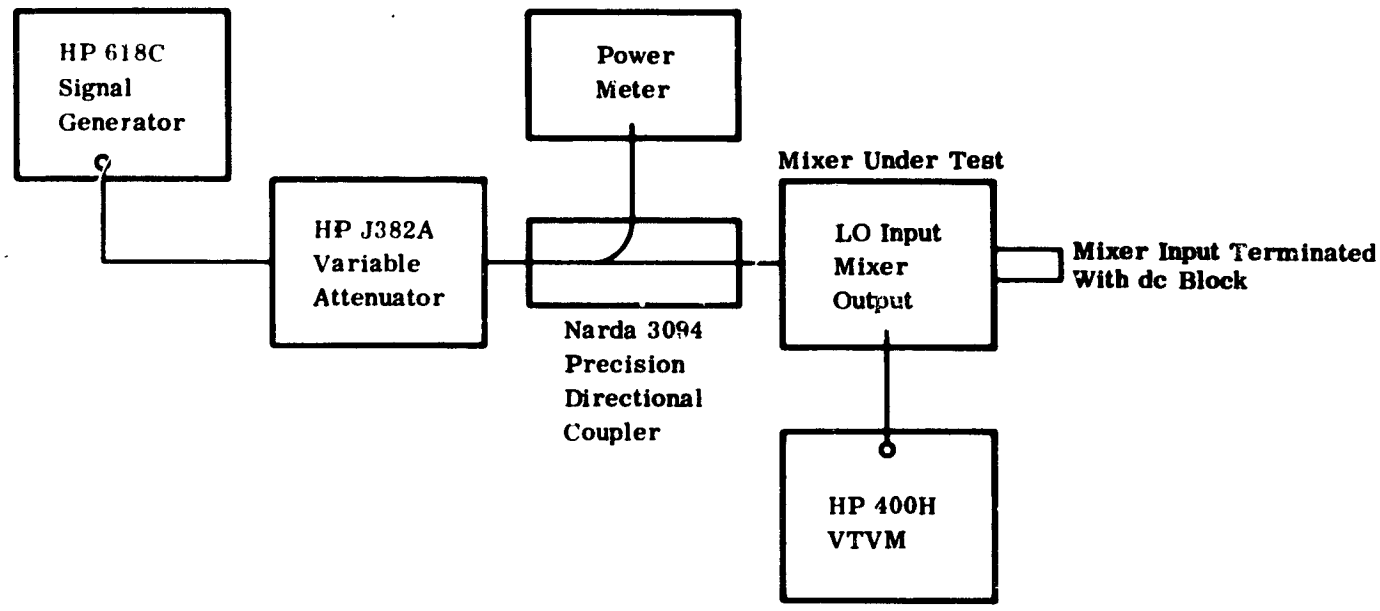


Figure 21 Block Diagram, AM Rejection Test Set

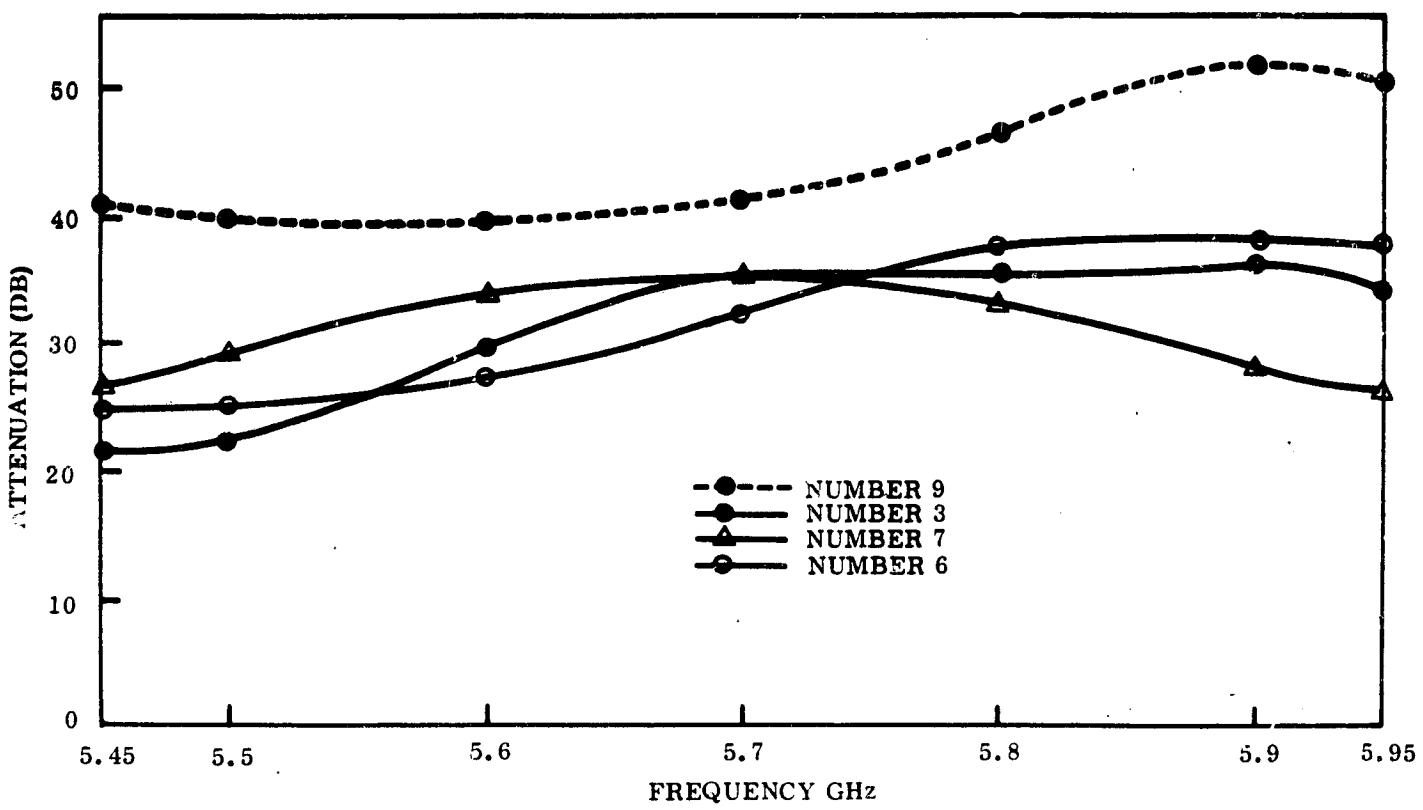


Figure 22 AM Rejection Balanced Mixers Test Results

4.2.3.2 Local Oscillator

Figure 23 shows a schematic diagram of the x 8 multiplier circuit. This figure shows additional information than that which was included in Figure 5. Figures 24 and 25 show the resultant product design and fabrication in stripline. The LO is comprised of the UHF driver, x 8 multiplier, and the output filter.

Performance of the UHF driver stage is as follows:

Frequency	711 MHz ±1%
MHF Power Input	80 milliwatts
Mode of Operation	Class A
DC Power Requirements	+25 vdc at 17 ma

Two variable capacitors (C1 and C2 of Figure 23) are used to tune the multiplier input circuit so it appears as an effective short circuit at the output frequency (x8). The multiplier inductors (L2, L3 and L4) are all fabricated in stripline.

An output filter is used to attenuate all harmonic outputs of the multiplier except the desired harmonic. Figure 26 shows typical bandpass characteristics for the output filter.

Figures 27 and 28 plot the results of measurements made to determine the limits of LO output power and its effect on the balanced mixer noise figure. Figure 27 indicates the allowable limits of LO output power, i.e., from +1 dbm to +9 dbm. It can be noted that the breadboard LO filters did not have sufficient bandpass but this was corrected with system filter No. 1. Figure 28 shows the noise figure as a function of LO power. The LO power is plotted per diode; this power must be doubled for a balanced mixer.

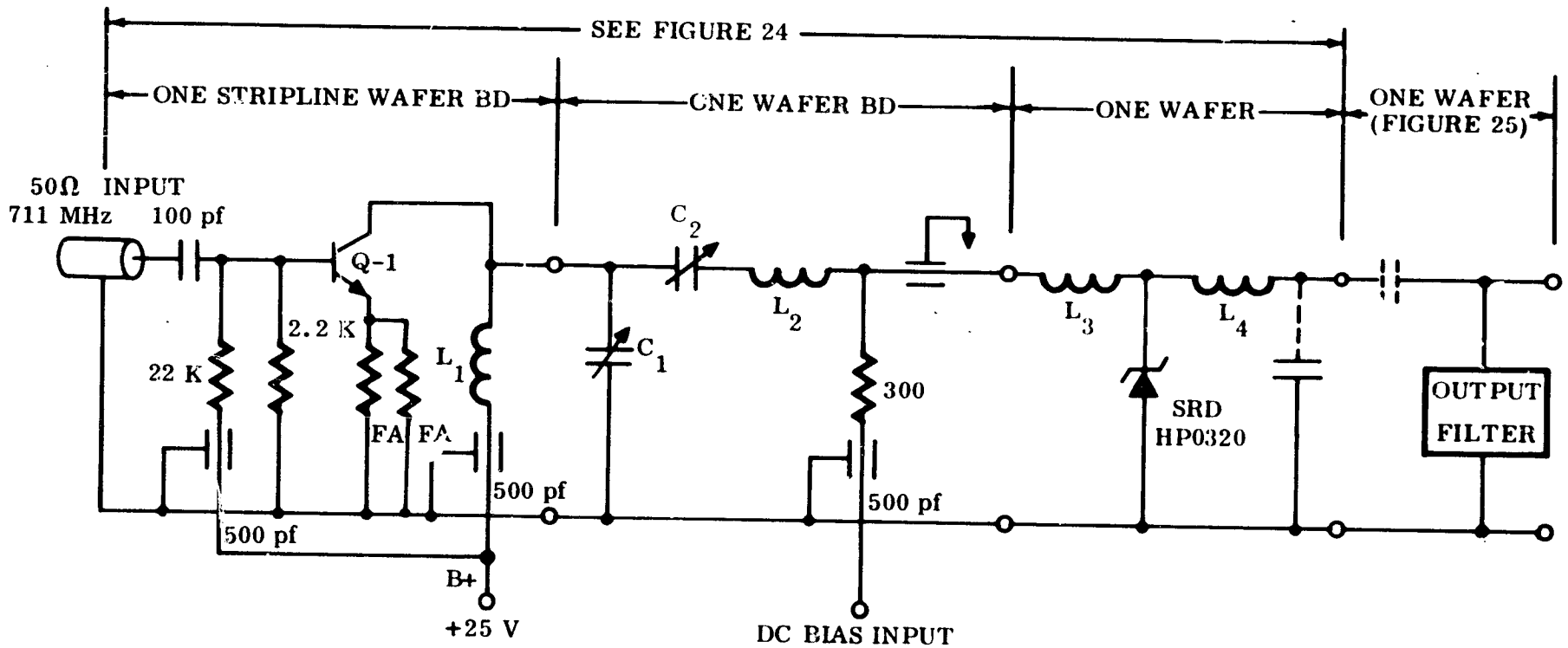


Figure 23 x 8 Multiplier Circuit

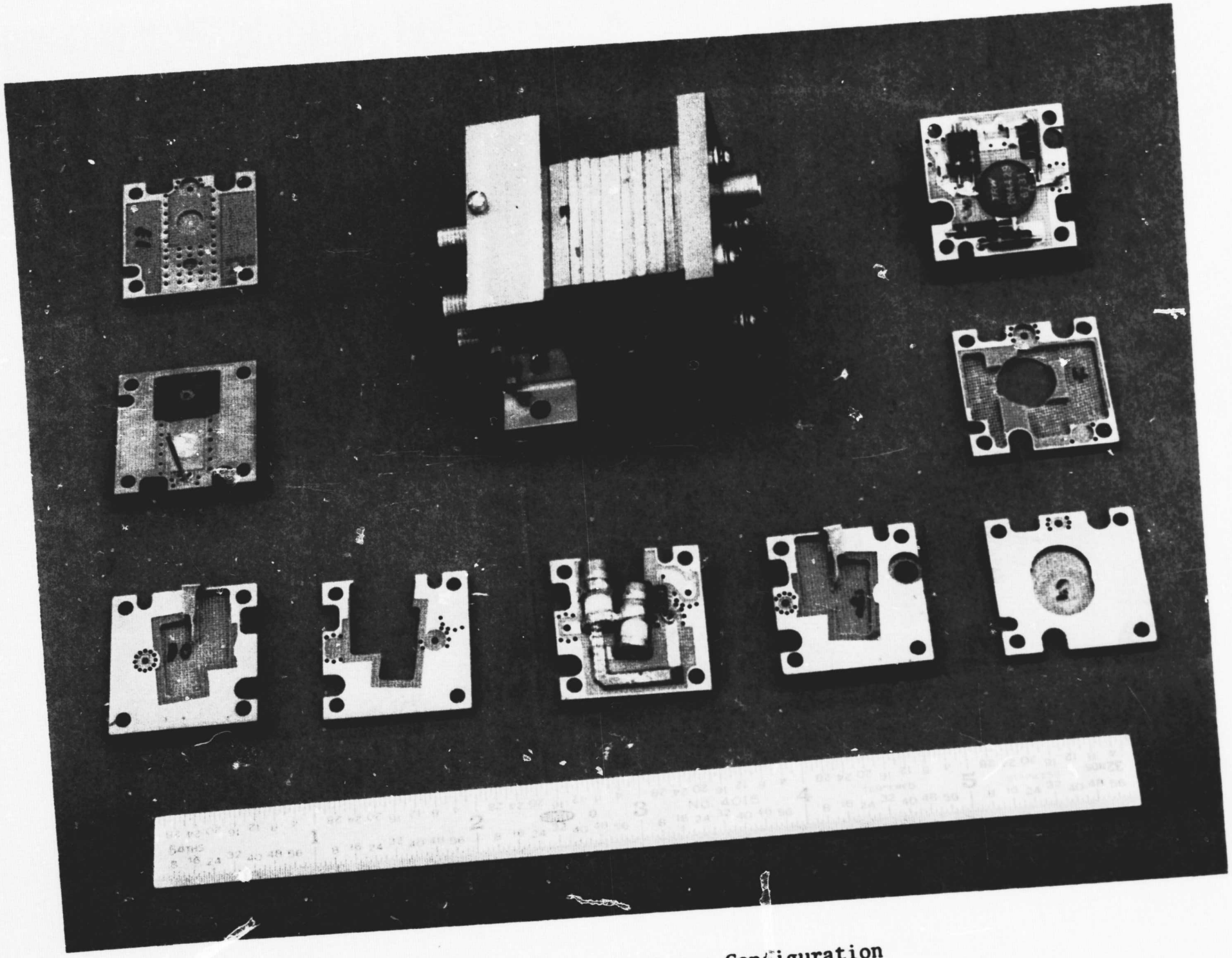


Figure 24 Local Oscillator Configuration

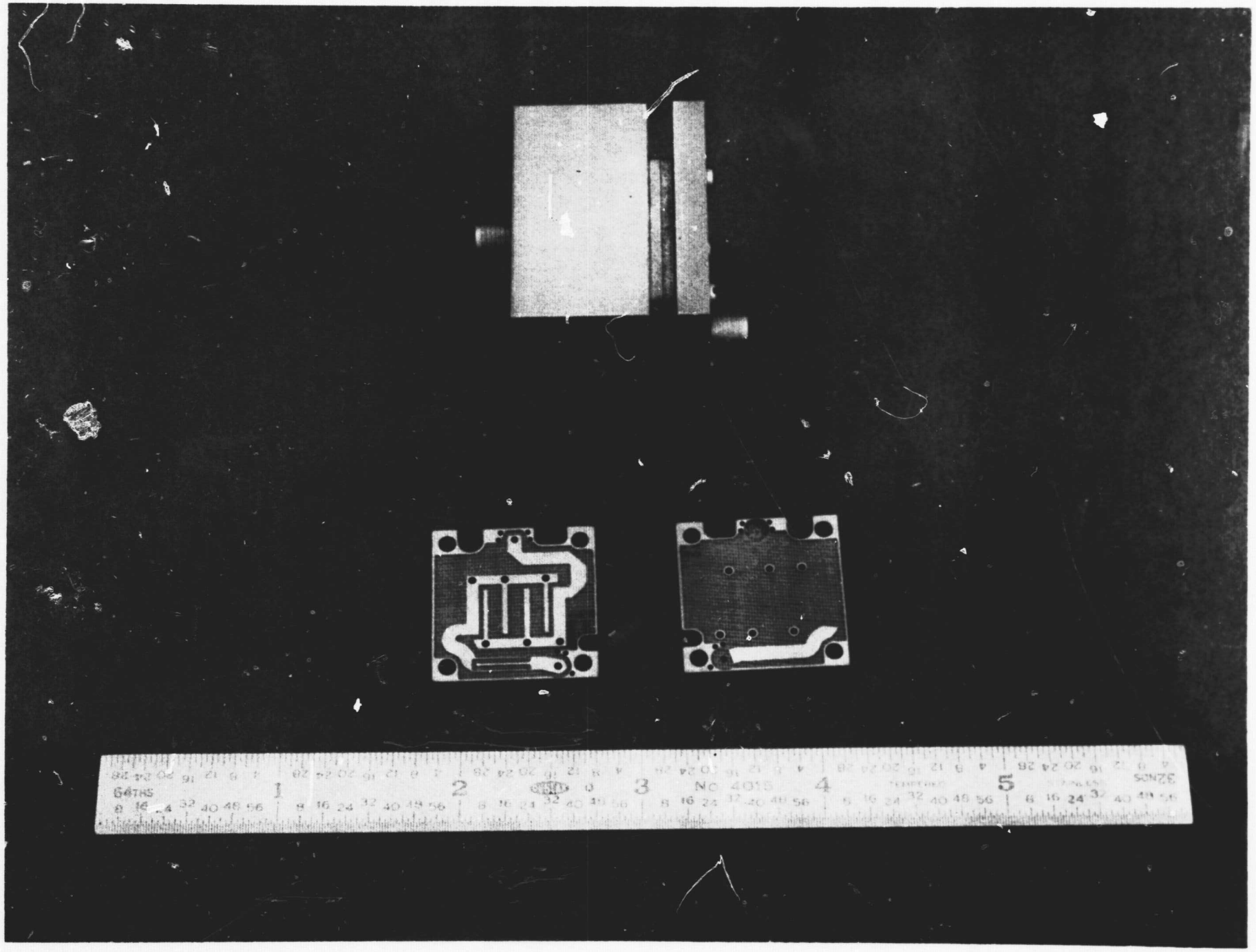


Figure 25 Local Oscillator Output Filter Configuration

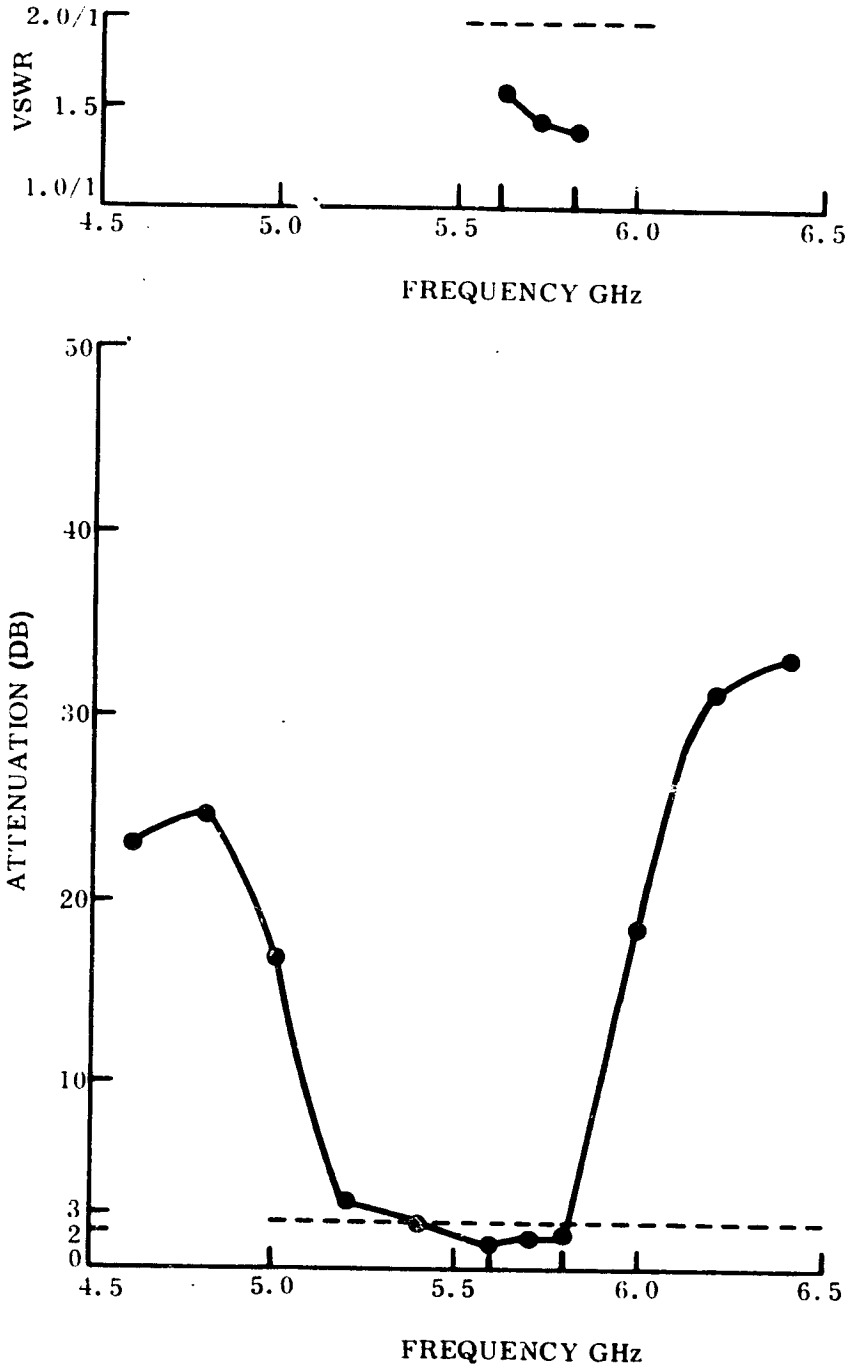


Figure 26 Typical Bandpass Characteristics of LO Filter

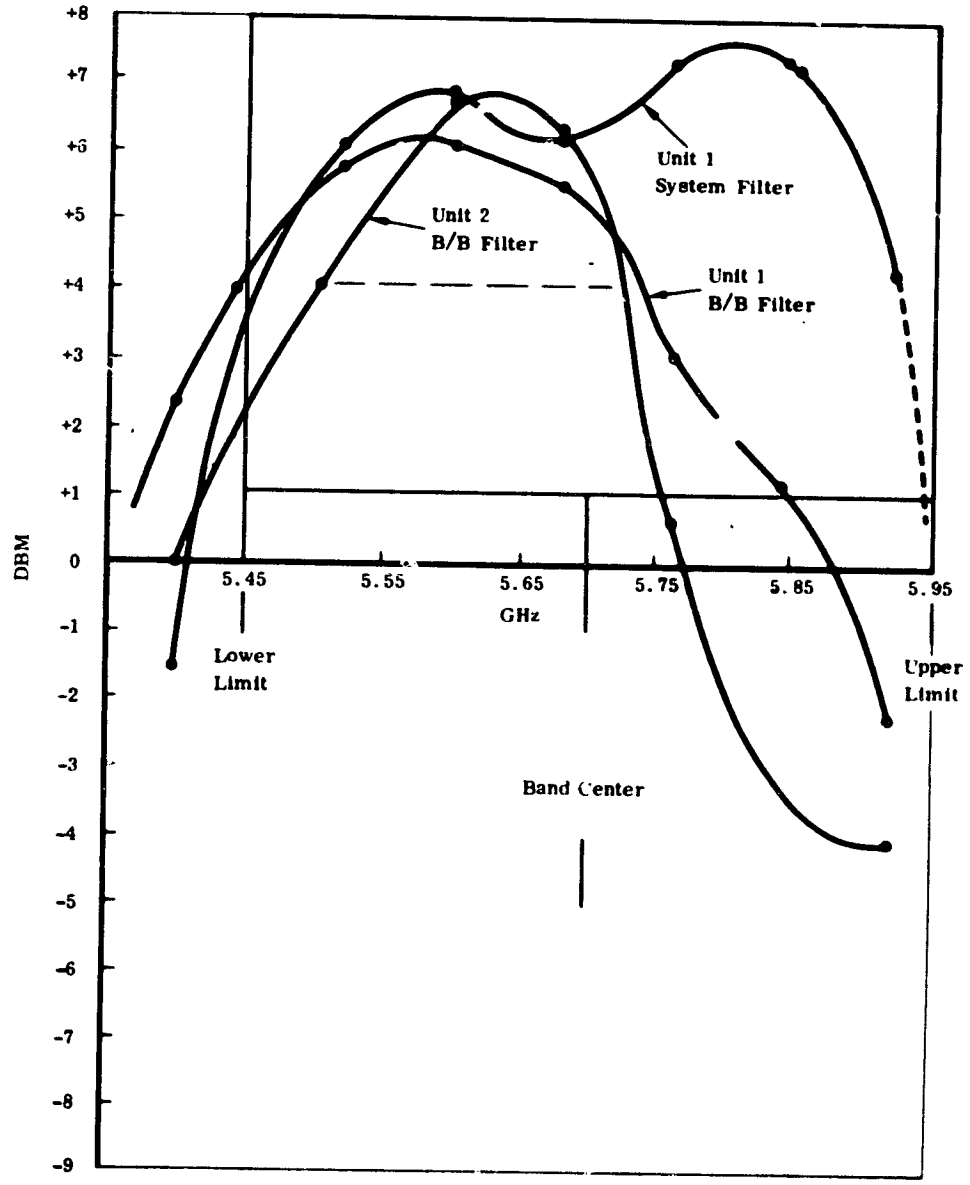


Figure 27 Allowable Limits of LO Power

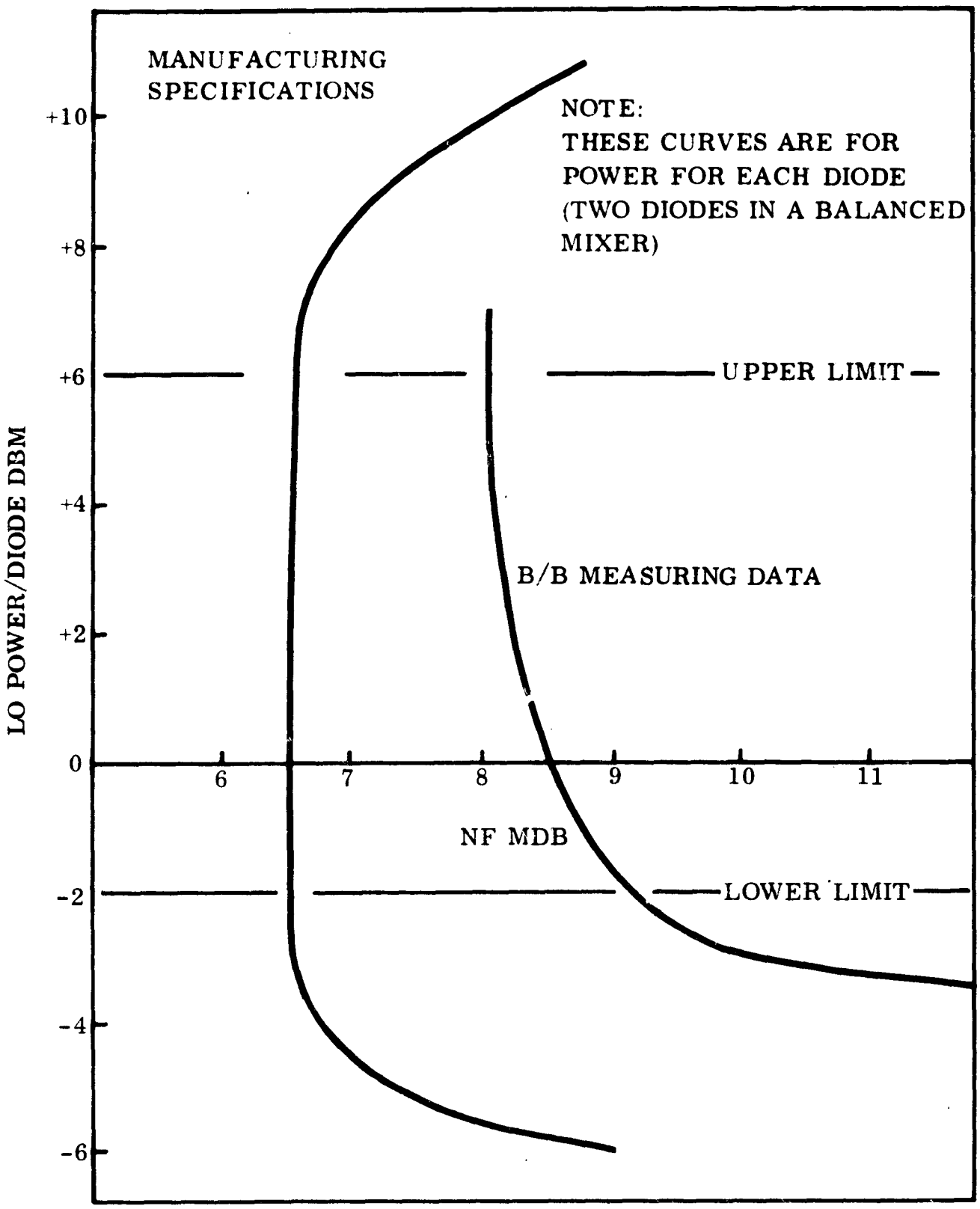


Figure 28 Noise Figure as a Function of LO Power

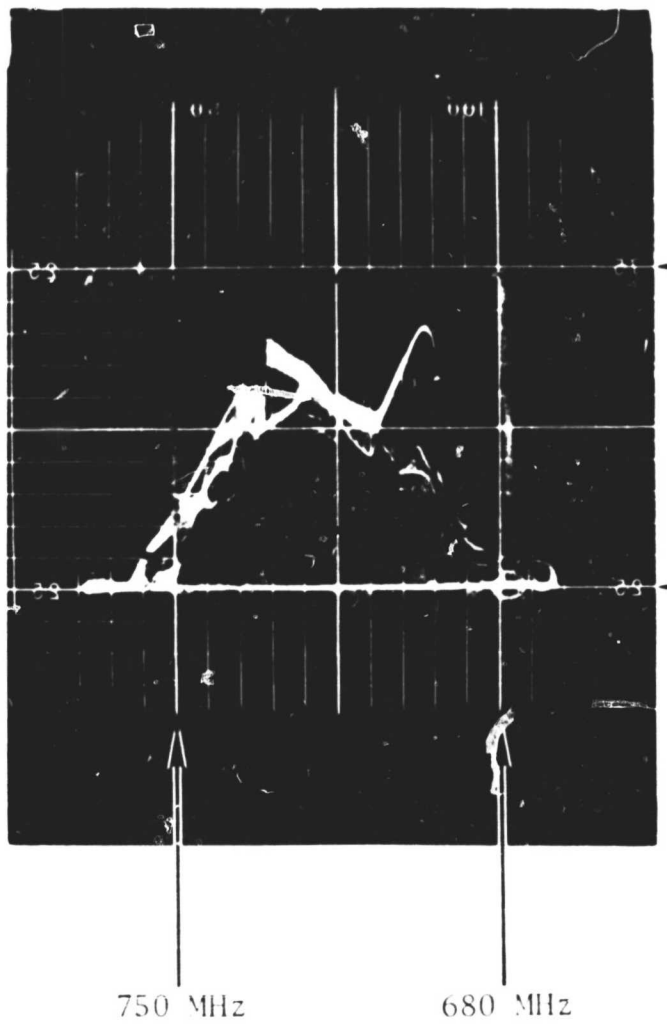
A special test bench was made to test the LO dynamically. The test set monitors the LO output power during simultaneous frequency sweeps and phase sweeps over the required ranges. The results of these frequency and phase modulations are photographed. Figure 29 shows an oscilloscope photograph taken of a typical LO response. Observation of the photograph will show that the UHF input to the LO is frequency swept over the 711 KHz ±5% range. The module output power amplitude is indicated by the y-axis of the photograph. This amplitude is calibrated on the face of the oscilloscope to be within the required limits as shown by Figure 27. Consequently, a dynamic response of the output power over the required bandwidth is photographed.

Figure 30 shows the block diagram for the test station providing this output power vs bandwidth. The 711 KHz ±5% is generated by the frequency sweeper and swept between these two limits at a 60 Hz rate. The phase modulation is generated by the HP 200 CD Oscillator at a 14 KHz rate. The HP 618C Signal Generator and the power meter are used to calibrate the Y-axis input to the monitoring oscilloscope. The spectrum analyzer at the high power output of the coupler is used to monitor the spectral purity of the module output.

4.2.3.3 I.F. Amplifier

The schematic diagram of the I.F. amplifier used for this module is shown in Figure 5. Basic characteristics are as follows:

Center Frequency	60 MHz
Bandwidth	19 MHz
Gain	28 db
Noise Figure	< 2 db



SRD Phase Modulation	-	±0.3v (p-p) @ 14 KHz
SRD Frequency Sweep	-	As noted at 60 Hz rate
LO Unit #5	-	33 ±1 mw

Figure 29 Trace Showing LO Performance

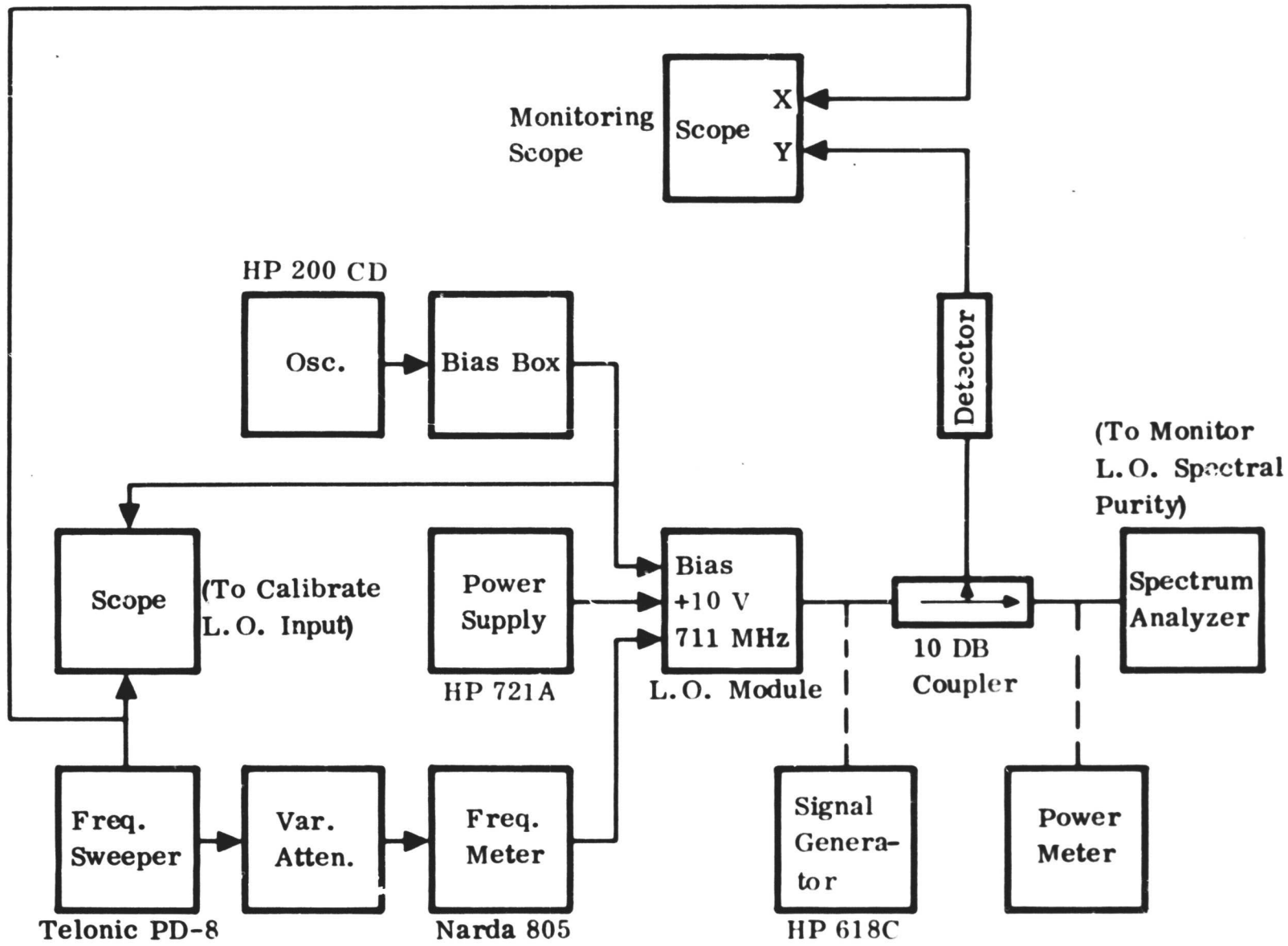


Figure 30 LO Test Setup

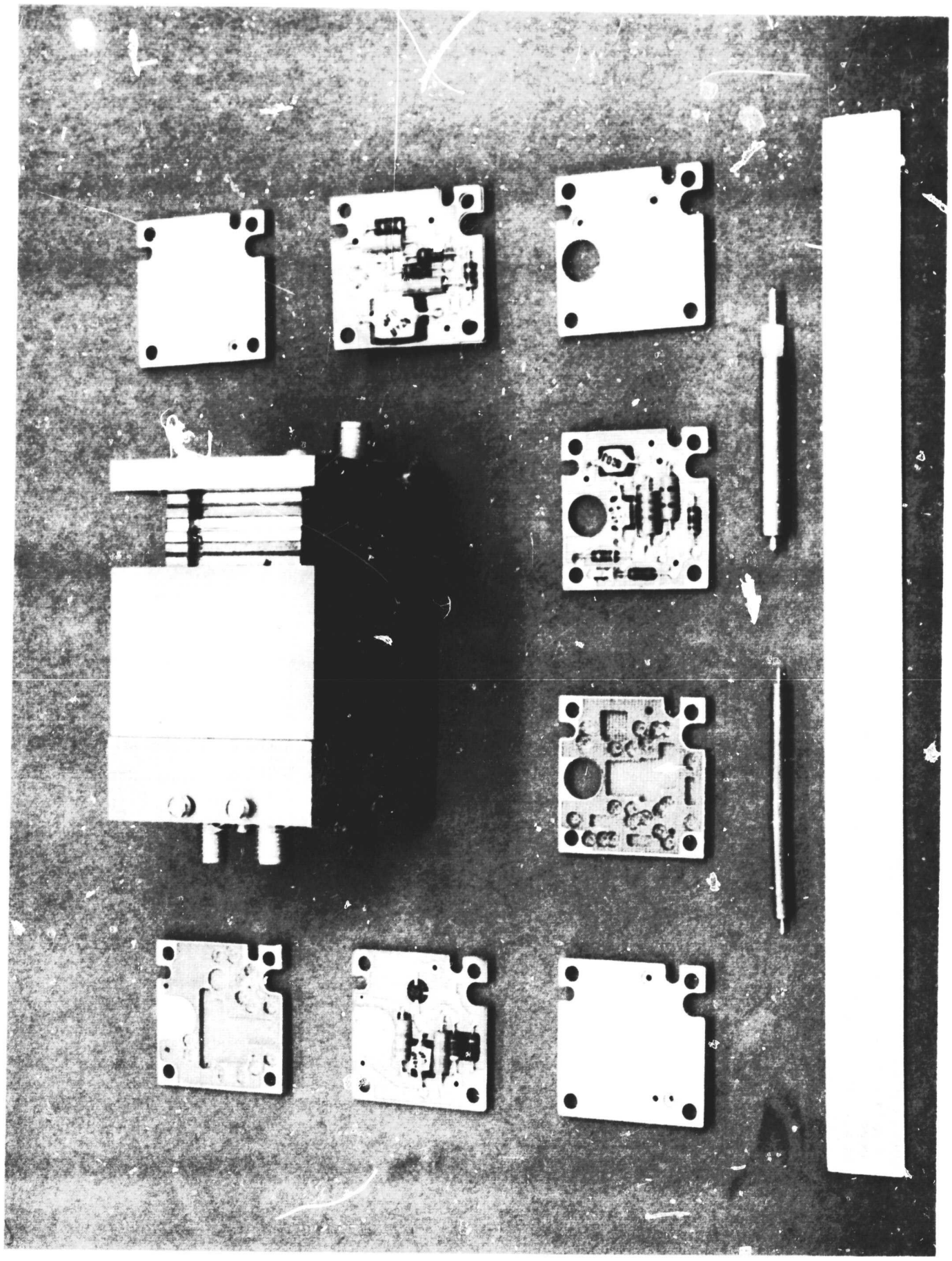


Figure 31 IF Amplifier Configuration

Figure 31 shows the IF amplifier configuration. The discrete circuit components are mounted on three stripline boards. The center upper portion of the photograph shows the test fixture used for the IF amplifier tests.

Figure 32 shows the test bench circuit constructed to measure the IF amplifier performance.

Figure 33 shows the IF amplifier power gain for four typical units.

Figure 34 presents the phase shift vs frequency characteristics as measured for some of the IF amplifiers.

Figure 35 is a plot showing the dynamic range of the IF amplifier.

Table II indicates typical IF amplifier noise figures measured for some of the units.

Table II. Typical IF Amplifier Noise Figures

UNIT NUMBER	IF AMPLIFIER NOISE FIGURE
1	1.4 db
2	1.2 db
3	1.4 db
4	1.5 db
5	1.4 db
6	1.1 db
7	1.2 db
8	0.9 db

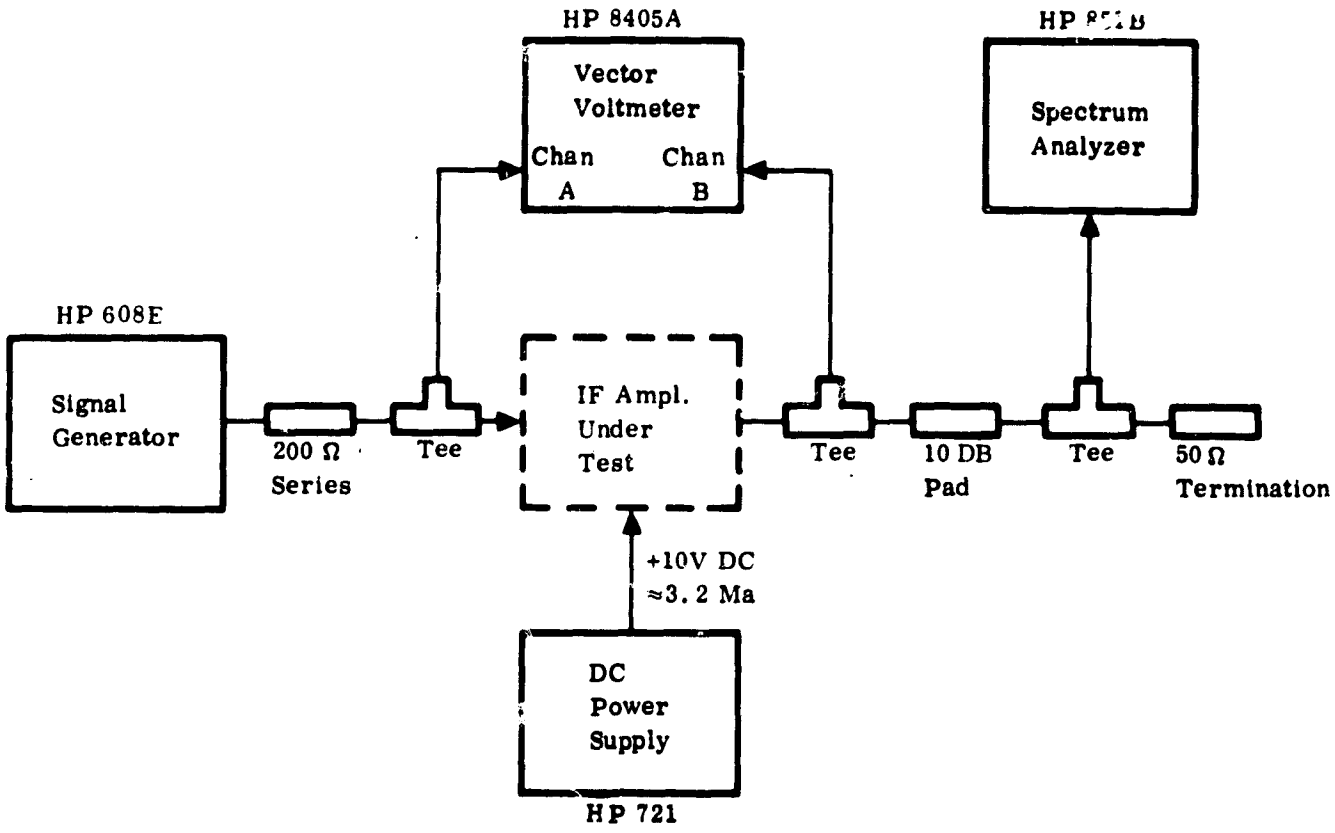


Figure 32 IF Amplifier Test Setup

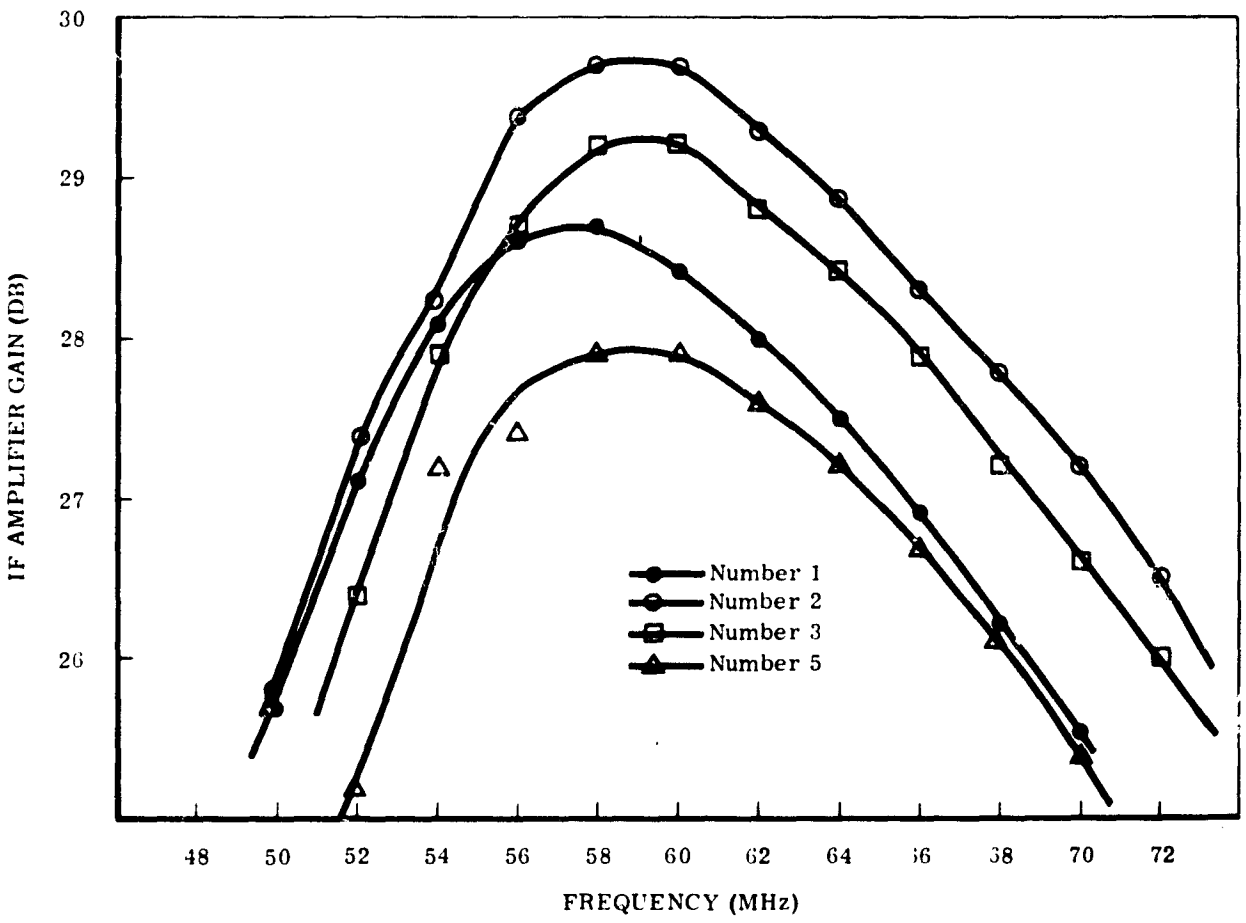


Figure 33 IF Amplifier Gain vs Frequency

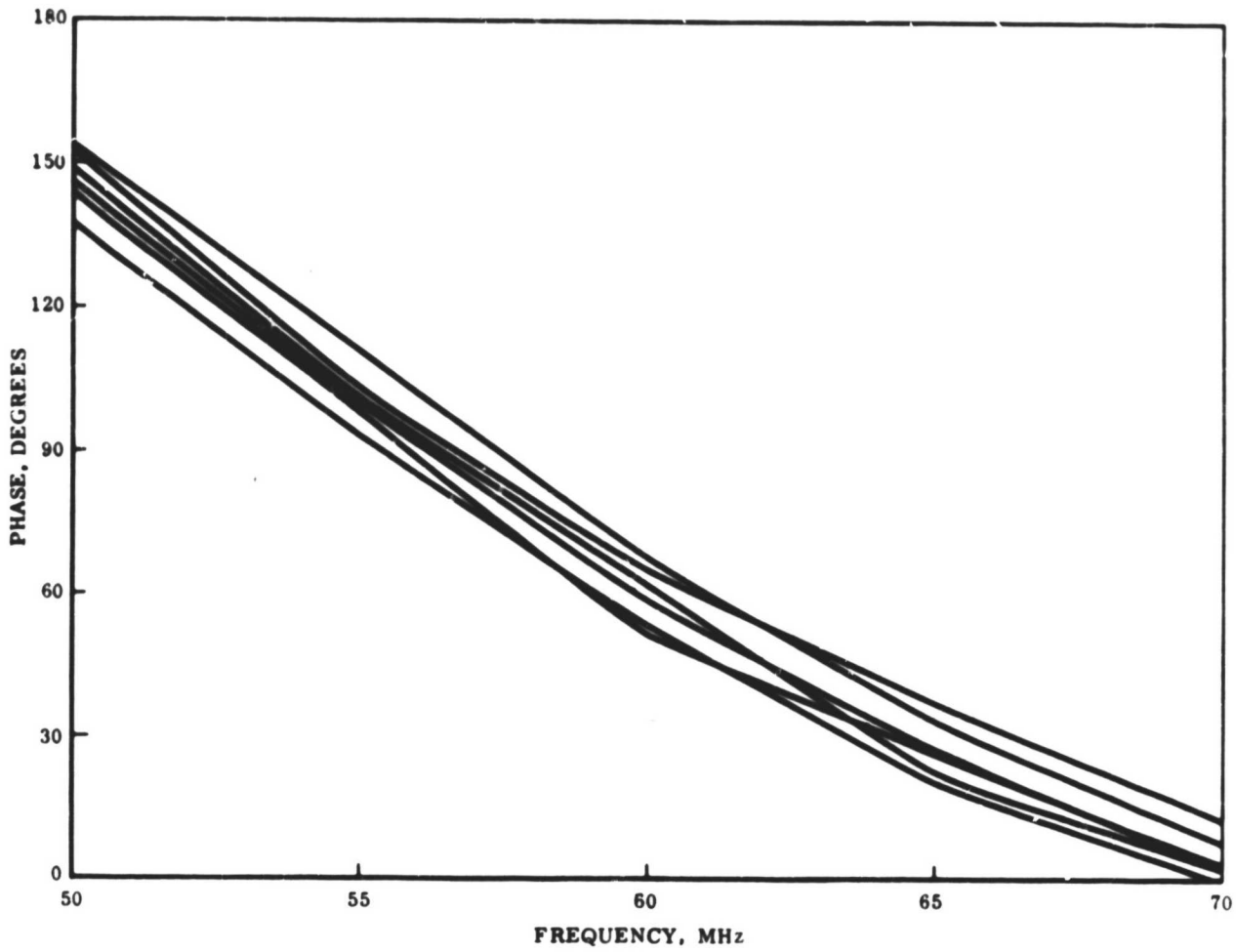


Figure 34 IF Amplifier Phase Response

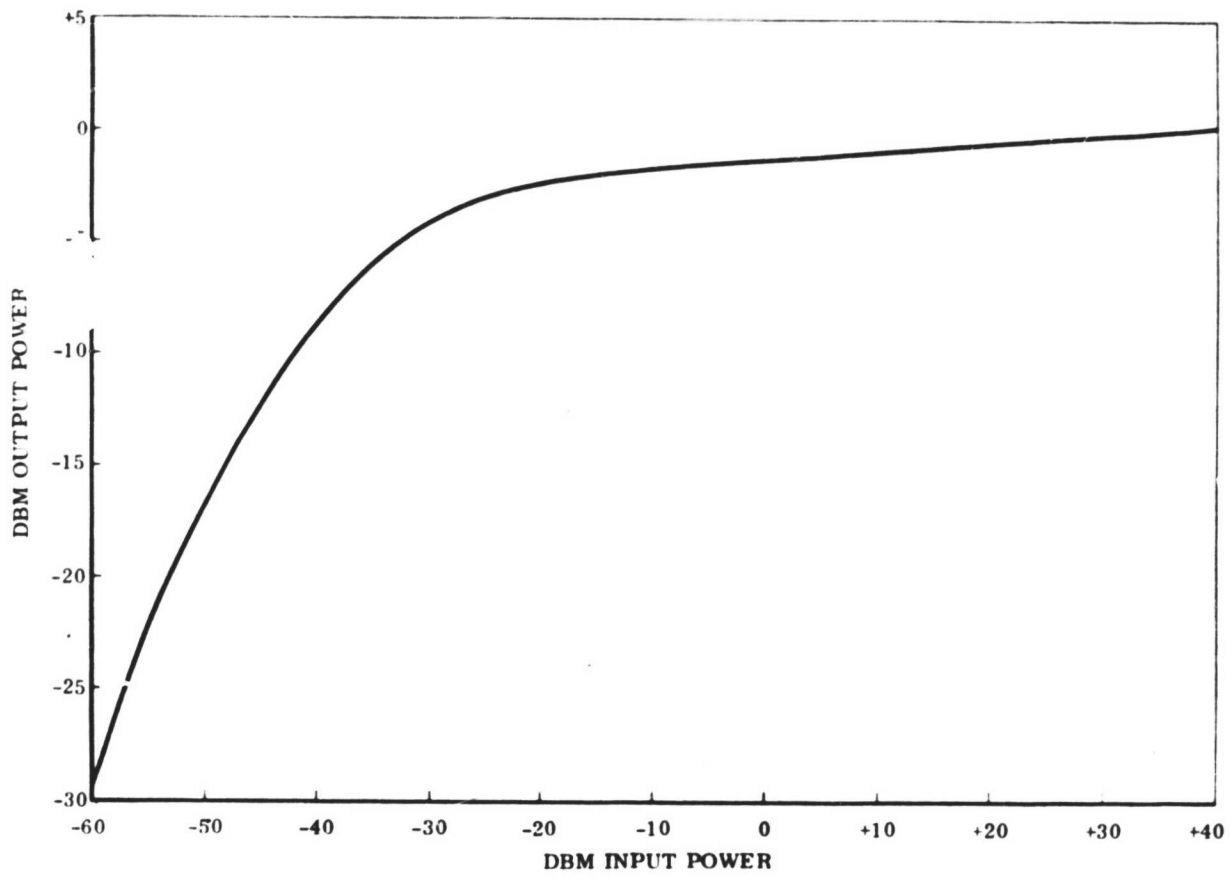


Figure 35 Dynamic Range Plot, 598 IF Amplifier Breadboard

4.2.4 Transmitter

The transmitter portion of the module includes:

- x 2 SRD multiplier
- x 5 SRD multiplier
- Multiplier isolation

Two multipliers in series were utilized in the final module configuration instead of a x 10 multiplier. Initial module development considered use of a single multiplier.

The power generation capability of the SRD is controlled by two limitations[1]:

- The power dissipation limit defined as $P_{diss\ max}$
- The power limit resulting from the height of the impulse approaching V_{BR}, the breakdown voltage.

The latter limitation is defined by:

$$P_o < 0.53 \quad f_i \; C_{VR} \; V_{BR}^{\;2} \quad \xi_{mp \rightarrow cw} \tag{1}$$

where

P_o = output power

f_i = multiplier input frequency - 575 MHz

C_{VR} = diode capacity 1.9 pf for the HP 0310

V_{BR} = diode breakdown voltage - 40v for HP 0310

---

[1]Hewlett-Packard Application Note 920 - "Harmonic Generation Using Step Recovery Diodes and SRD Modules"

$\xi_{imp \rightarrow}$ = efficiency of changing impulse waveform to cw - 42% for HP 0310

Substitution of these values in equation (1) results in:

P_o = 0.462 watts

This magnitude was not achieved in initial development effort in stripline configuration. Also, initial breadboards exhibited considerable output power variations as the bias was varied. Satisfactory x 5 performance was readily achieved using a multiplier configured with a mechanical cavity output. This configuration, driven by a x 2 multiplier with a stripline resonator, was successfully employed for the module development.

The components of the transmitter portion of the module are discussed in the following paragraphs.

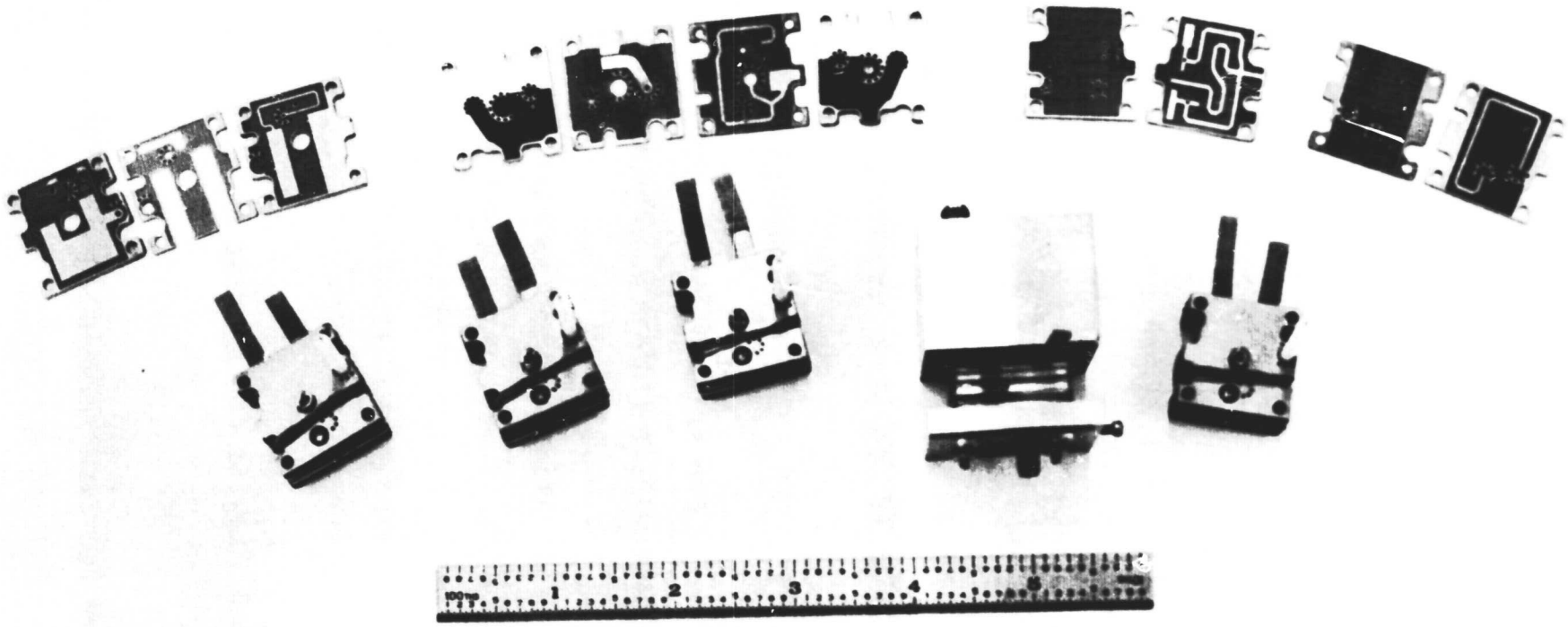
4.2.4.1 x 2 SRD Multiplier

Figure 36 shows the x 2 SRD multiplier circuit configuration and the schematic diagram is shown in Figure 5. The three stripline wafers shown on the left comprise the multiplier input. Variable capacitors, C9 and C10, are adjusted by positioning the two Lamicord tabs to vary the capacitance, the proper tuning is achieved and the tab is locked and cut off.

The middle group of stripline wafers (four) mount the SRD. The right hand group of wafers (four) are the output stripline filter.

Figure 37 is a block diagram of the test circuit used to measure multiplier performance.

Table III tabulates the data measured for the 4 x 4 array modules.



X2 MULTIPLIER

Figure 36 x 2 SRD Multiplier Configuration

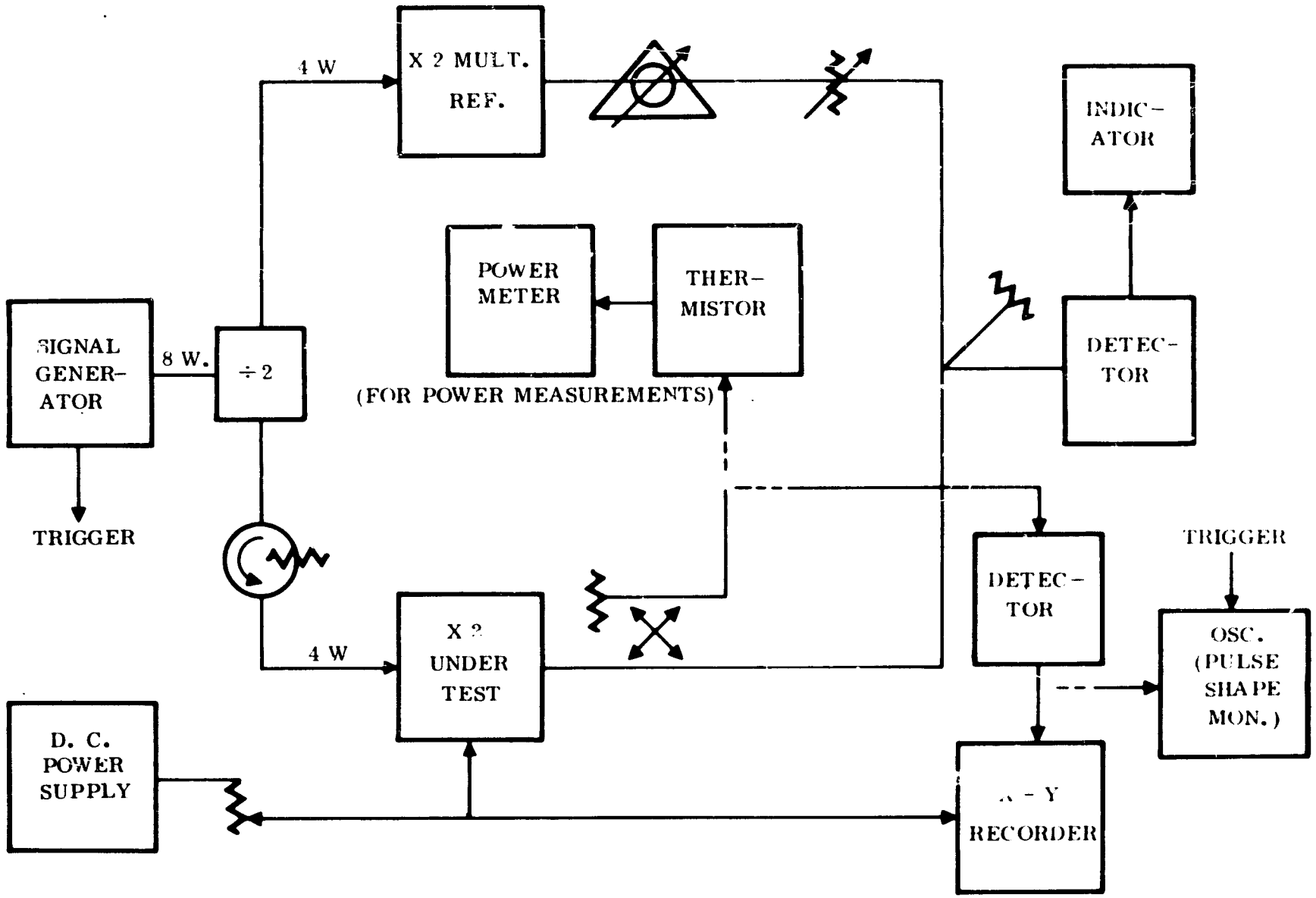


Figure 37 x 2 Multiplier Test Equipment Setup

TABLE III. POWER AND PHASE RANGE FOR X 2 MULTIPLIER

Driver Power: 4 watts (CW) Drive Frequency: 575 MHz

Output Frequency: 1150 MHz

SERIAL NUMBER	POWER OUTPUT (MAX.) (WATTS-CW)	PHASE SHIFT RANGE TO 1 DB POWER POINTS	BIAS RANGE VOLTS (NEGATIVE)
1	1.80	86°	8.5 to 20.5
2	1.80	94°	6 to 22
3	1.50	100°	11 to 20.5
4	1.50	88°	6.5 to 19
5	1.40	90°	10.5 to 18
6	1.35	84°	8 to 18.5
7	1.53	94°	8 to 20.5
8	1.80	78°	12.5 to 17.5
9	1.68	87°	13.5 to 18.5
10	1.80	98°	8.5 to 18.5
11	2.00	94°	7 to 16
12	1.80	84°	11 to 21
13	1.55	102°	8 to 19
14	1.60	95°	9.5 to 21
15	1.55	96°	9.5 to 20
16	1.50	115°	8.5 to 18.5
17	1.80	100°	10.5 to 20.5

4.2.4.2 X 5 SRD Multiplier

Figure 38 shows the x 5 SRD multiplier circuit configuration and the schematic diagram is shown in Figure 5. The mechanical cavity, with its tuning rod, is apparent.

Figure 39 is a block diagram of the test circuit used to measure the x 5 multiplier performance. It should be noted that the x 2 multiplier, through an isolator, is used on the driver.

The peak output power as measured for each of the modules of the 4 x 4 array is tabulated in Table IV. It can be observed that all modules generate 50% above required output and some have a 100% power margin over the module specification.

The dc bias control is not used to phase steer the x 5 multiplier. This value is adjusted to optimize the output power mode of the entire transmitter.

4.2.4.3 Transmitter Isolation

Isolation between the x 2 SRD mutiplier and the x 5 SRD multiplier was found to be necessary to prevent mismatch before the two units.

The isolators used were supplied to Ryan by Addington Laboratories under Specification Control Drawing, SCD-CE-0094. Specified performance includes:

Insertion Loss	< 0.6 db
Isolation	> 20 db
VSWR (both input and output)	< 1.2:1

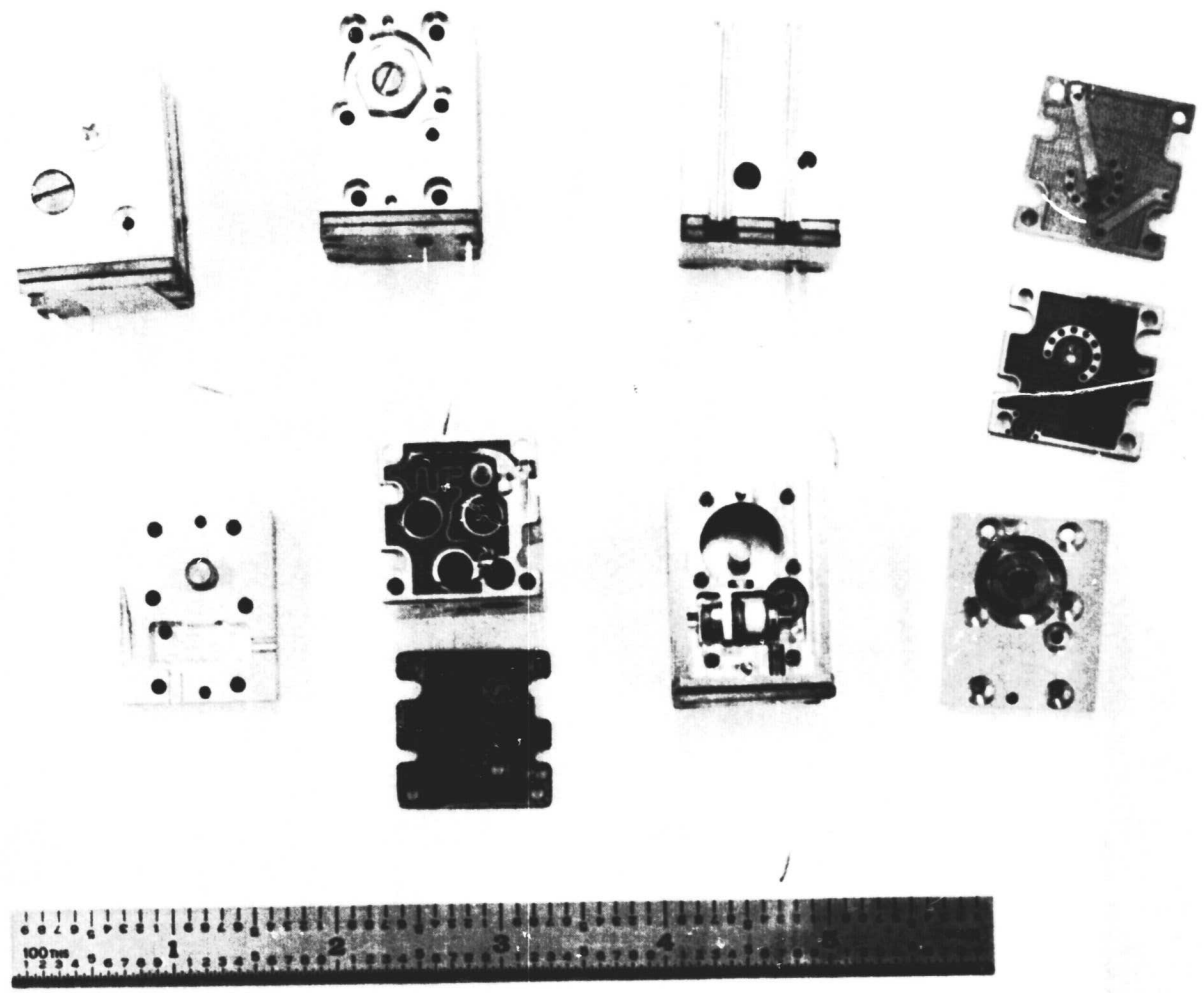


Figure 38 x 5 SRD Multiplier Configuration

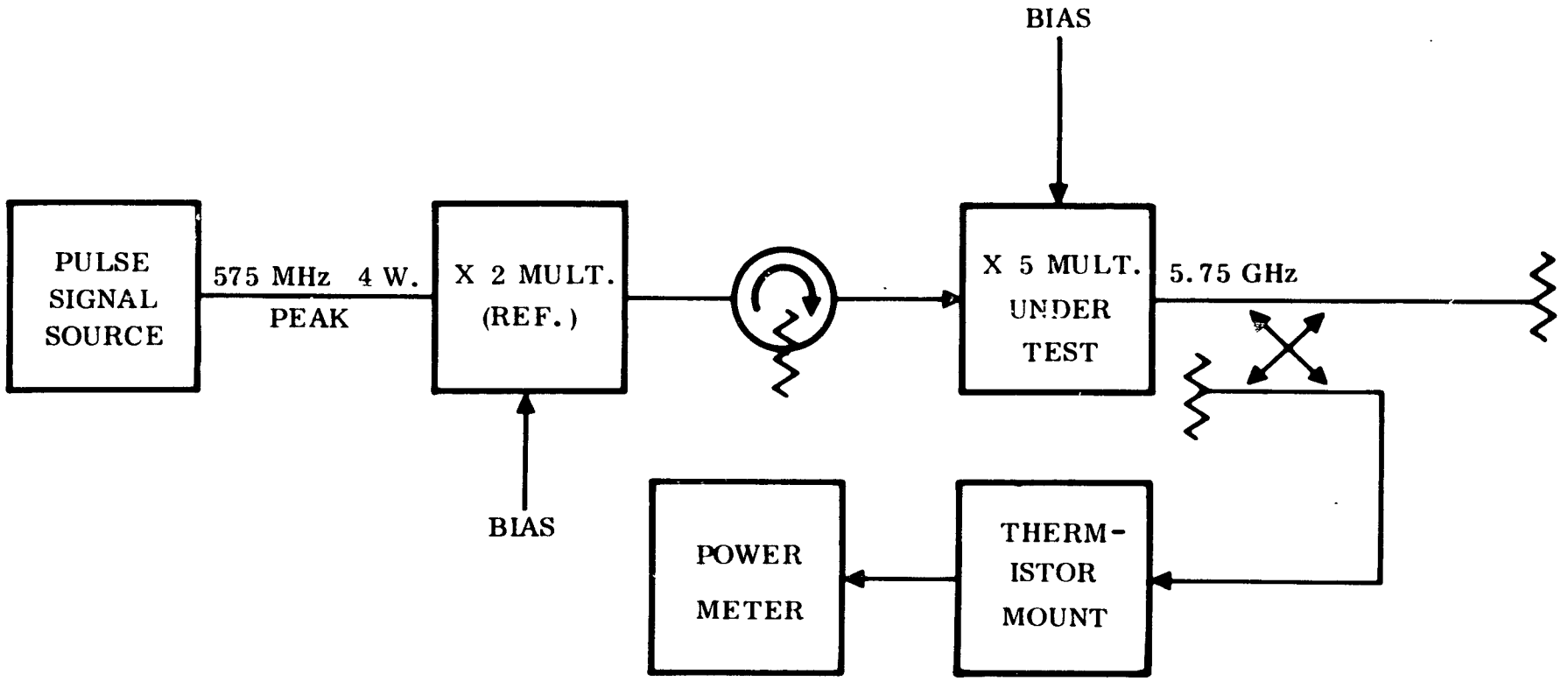


Figure 39 x 5 Multiplier Evaluation Test Setup

TABLE IV. POWER OUTPUT OF X 5 MULTIPLIER

Input Power to x 2: 4 watts, peak. Duty cycle: 0.005

SERIAL NUMBER	PEAK POWER OUTPUT WATTS	BIAS VOLTAGE (NEGATIVE)
1	0.44	8.3
2	0.38	7.7
3	0.37	8.9
4	0.44	7.4
5	0.36	7.8
6	0.37	7.1
7	0.38	7.9
8	0.32	6.4
9	0.38	7.6
10	0.42	7.3
11	0.40	7.6
12	0.38	7.3
13	0.47	8.4
14	0.34	7.1
15	0.34	6.9
16	0.38	7.3
17	0.38	7.3

4.2.5 Module Tests

The modules were assembled after completion of subcomponent tests. The antenna aperture was not initially installed so an RF signal source could be directly applied to the duplexer to measure the receiver and the duplexer output could be monitored during module transmitter tests.

Figure 40 is block diagram of the circuit used to test the receiver channels. Figure 41 is a typical plot measured with the Moseley X-Y Recorder showing output phase shift/output power vs dc bias characteristics. The phase shift plot has a fly-back every 360°. This results from the HP 8405A Vector Voltmeter which is used as the phase detector. Observation of Figure 41 indicates that the receiver portion of module No. 15 has nearly 720° of phase shift range before the output power varied 3 db (and approximately 540° within 1 db power variation). Similar plates were recorded for each module fabricated. The extreme variation of phase shift slope vs dc bias varied from 555°/volt to 1160°/volt.

Figure 42 is a block diagram of the circuit used to test the transmitter channels. Figure 43 is a typical response showing transmitter output power/ phase shift vs dc bias voltage. Maximum output power of this module, No. 3, was 400 milliwatts. Phase range with the 1 db power range is in excess of 360°. Similar plots were recorded for each module fabricated.

4.3 4 X 4 ARRAY SYSTEM

Figure 3 is the top assembly drawing for the 4 x 4, C-Band array system. Figure 4 is the block diagram for the array and Figure 5 is the schematic diagram for the entire system.

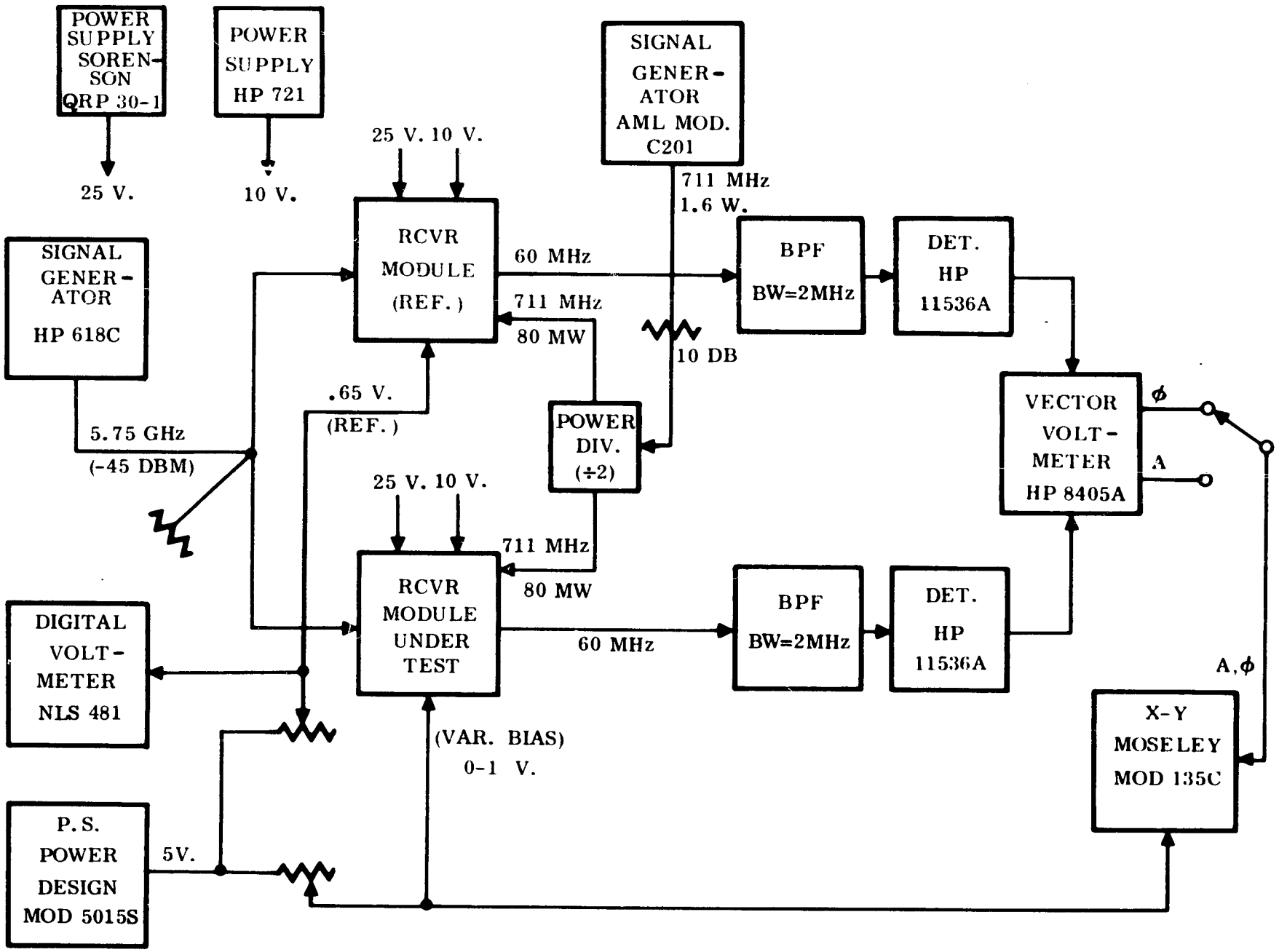


Figure 40 Test Equipment Setup and Circuit Arrangement for Receiver Phase and Amplitude Measurement vs Bias Voltage

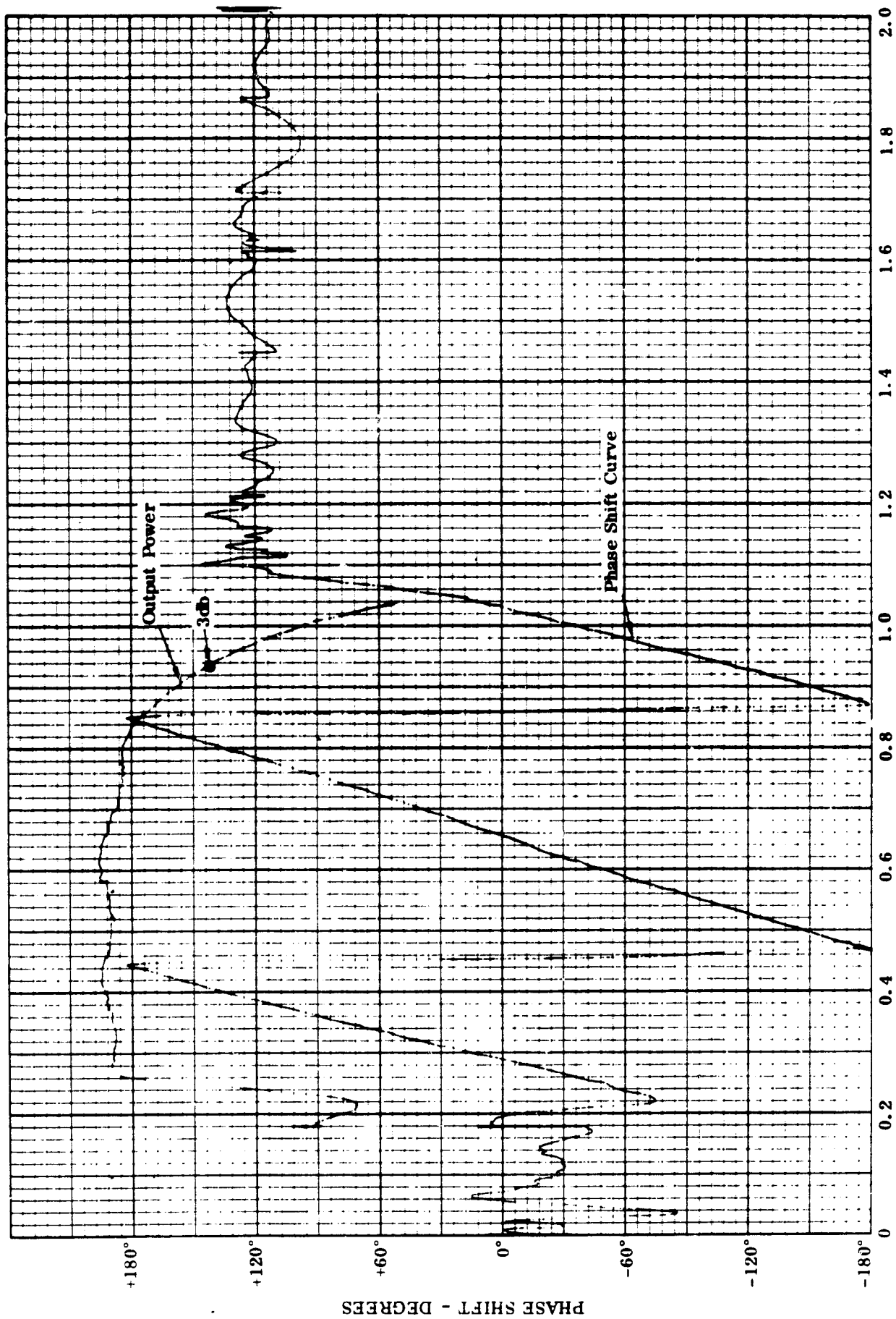


Figure 41 Graphic Representation of Receiver Phase and Amplitude Measurement vs Bias Voltage

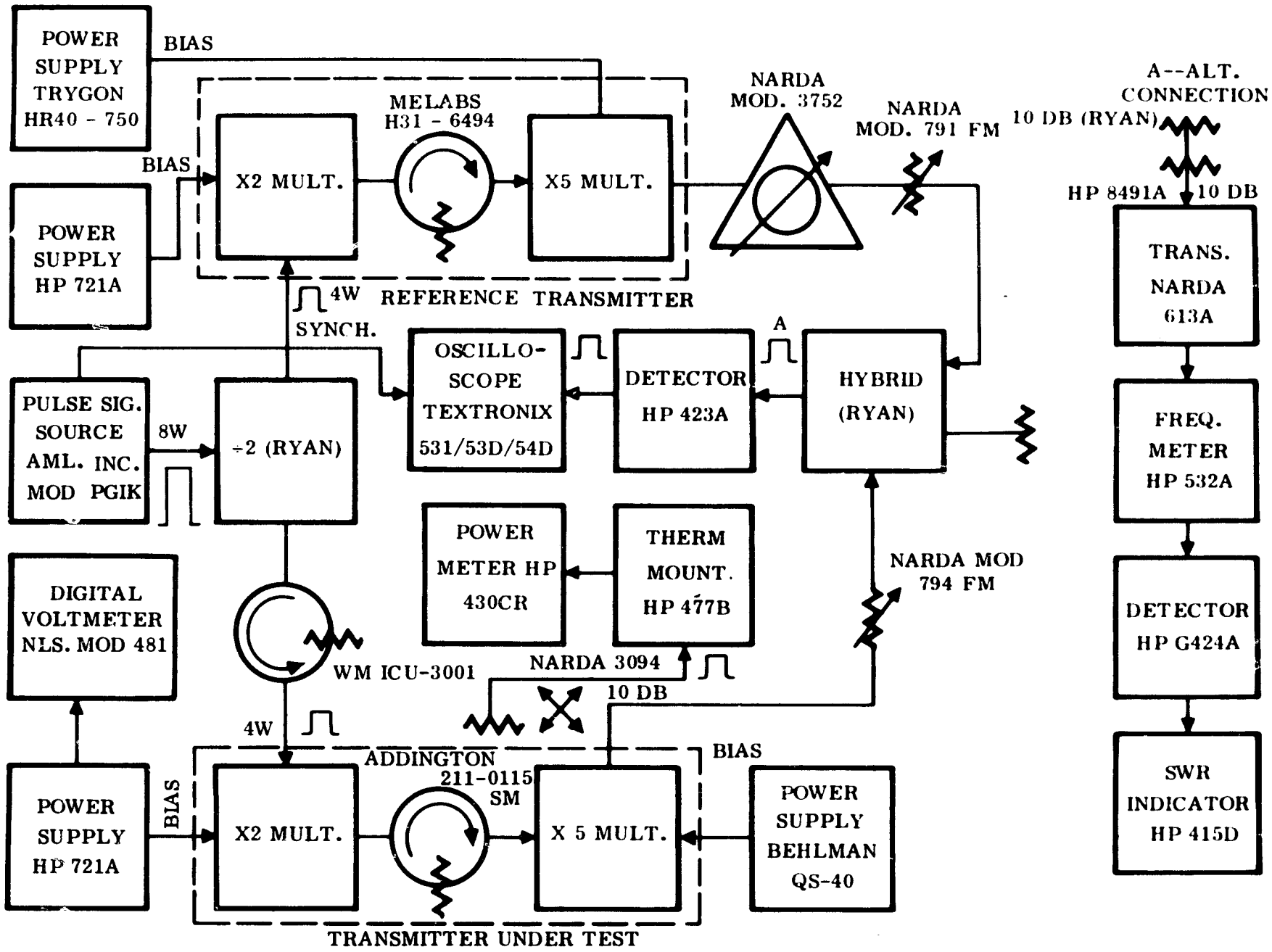


Figure 42 Test Setup for Transmitter Power and Phase Measurements

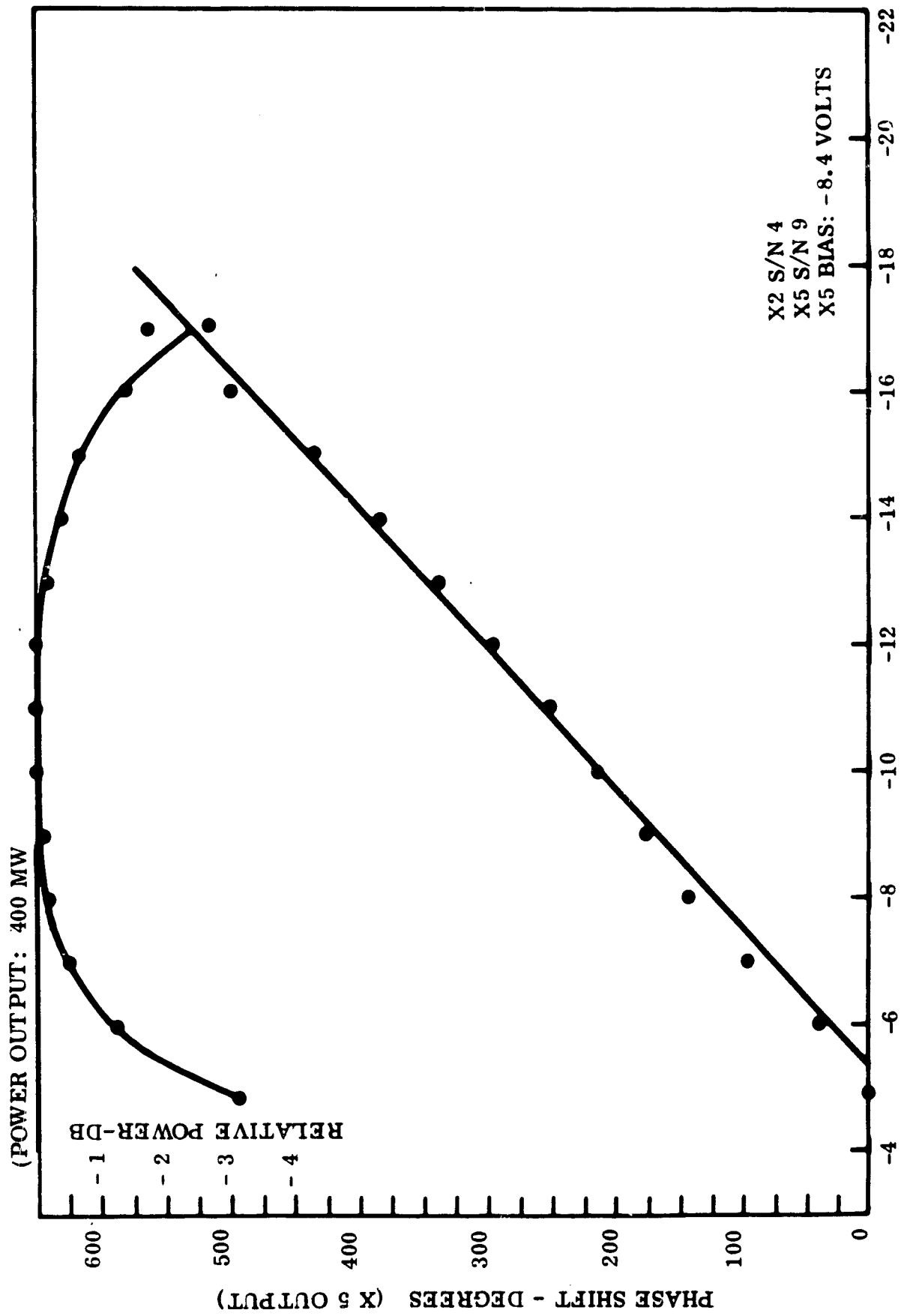


Figure 43 Grahpic Representation of Transmitter Power and Phase Measurements

The array system components, other than the modules previously discussed, include:

- A17 575 MHz power divider (Paragraph 4.3.1)
- A18 711 MHz power divider (Paragraph 4.3.2)
- A19 power distribution boards (Paragraph 4.3.3)
- A20 IF combiner (Paragraph 4.3.4)
- A21 beam steering unit (Paragraph 4.3.5)

4.3.1 A17 - 575 MHz Power Divider

Figure 44 shows the 575 MHz power divider configuration and Figure 5 shows the schematic diagram. The stripline T's were developed such that output part isolation between all output parts is 25 db or greater.

4.3.2 A18 - 711 MHz Power Divider

Figure 45 shows the 711 MHz power divider configuration and Figure 5 shows the schematic diagram. This power divider is similar to the 575 MHz divider except that dc blocks are not required to block the x 2 dc bias current.

4.3.3 A19 Power Distribution Board

Figure 46 shows the dc power distribution board configuration and Figure 5 shows the schematic diagram. This assembly contains four Zener diode circuits to drop the input from +25 vdc to +10 vdc in order to supply the module IF amplifier B+.

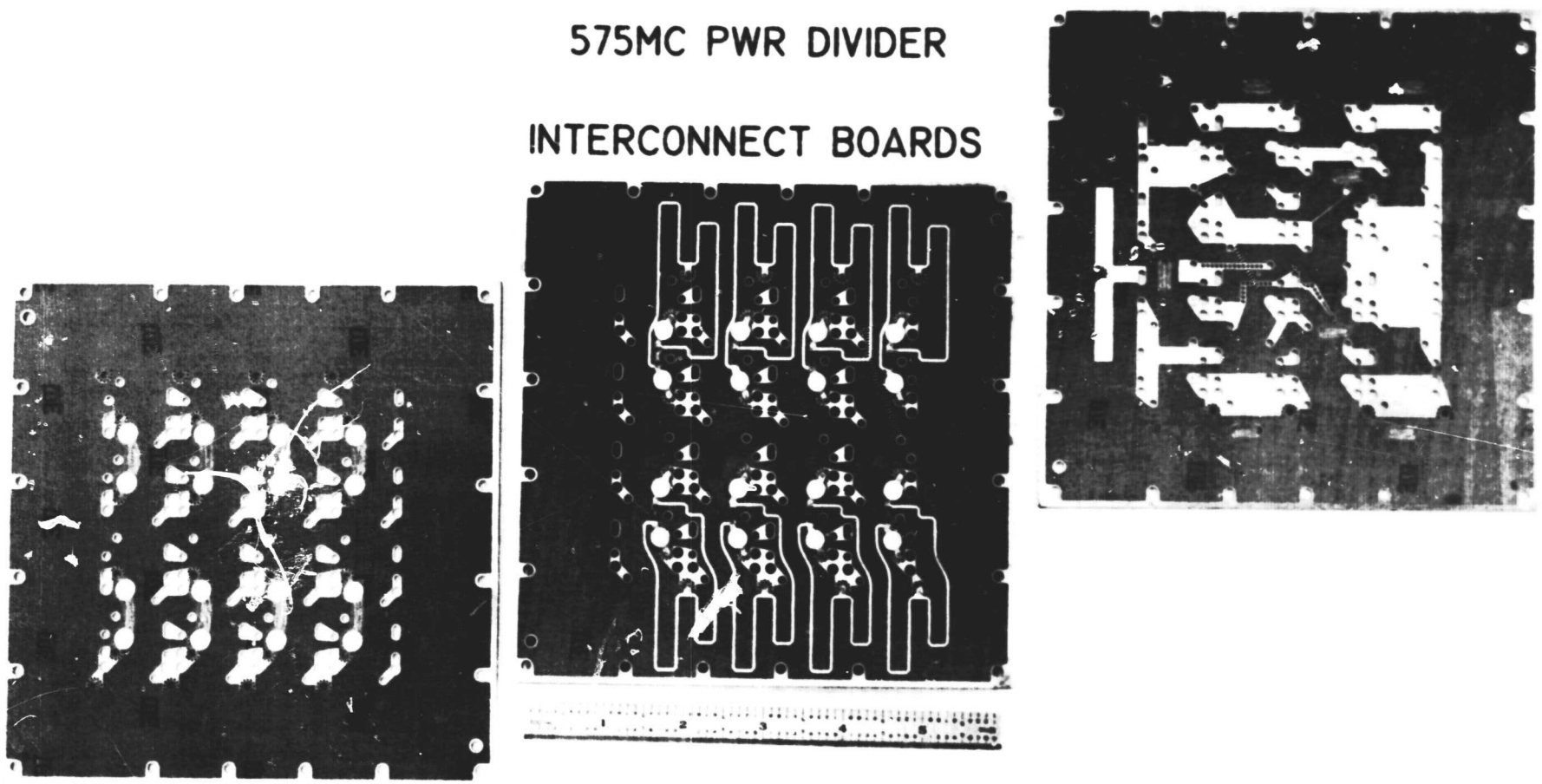


Figure 44 A17 - 575 MHz Power Divider Configuration

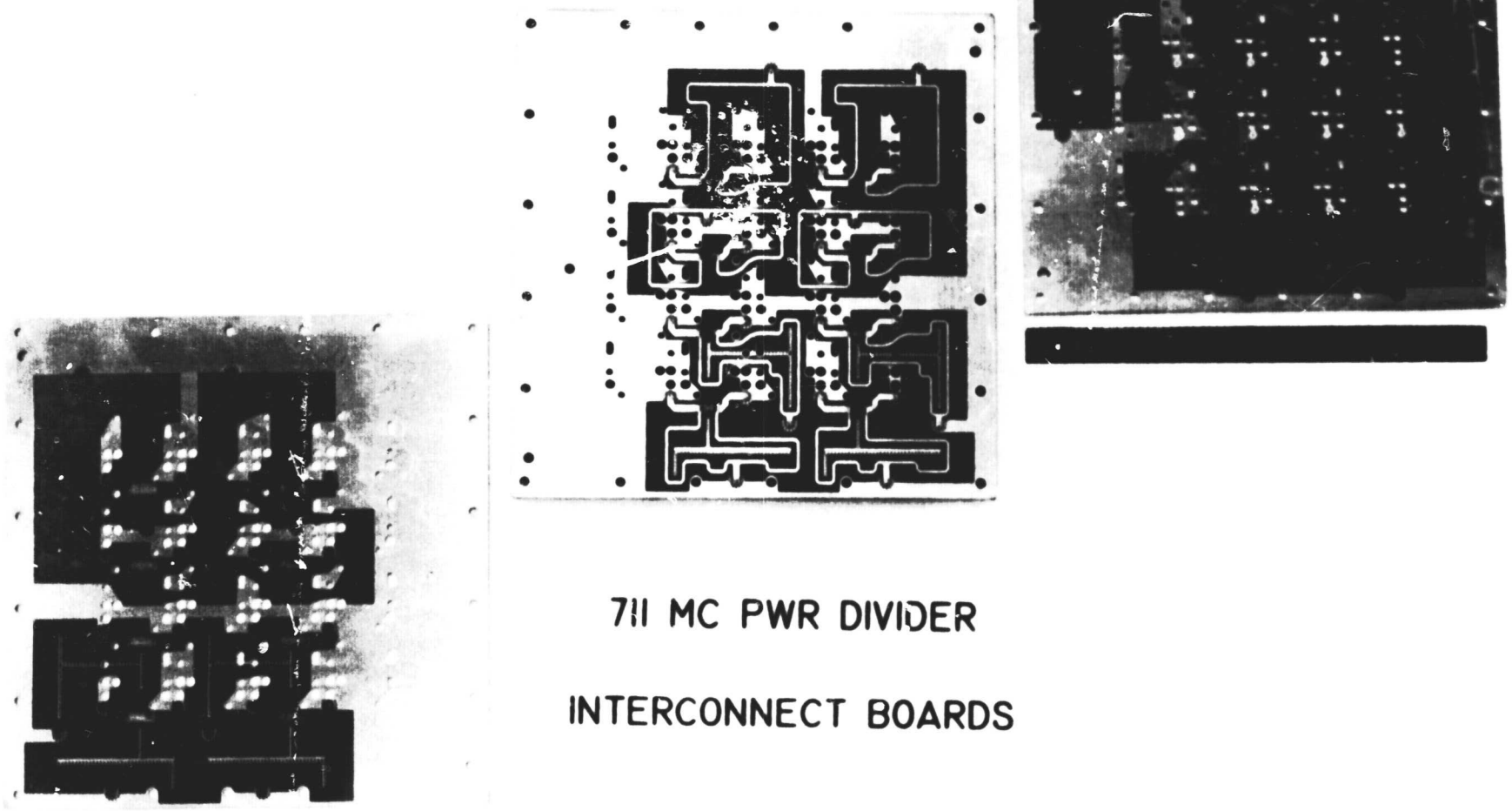


Figure 45 A18 - 711 MHz Power Divider Configuration

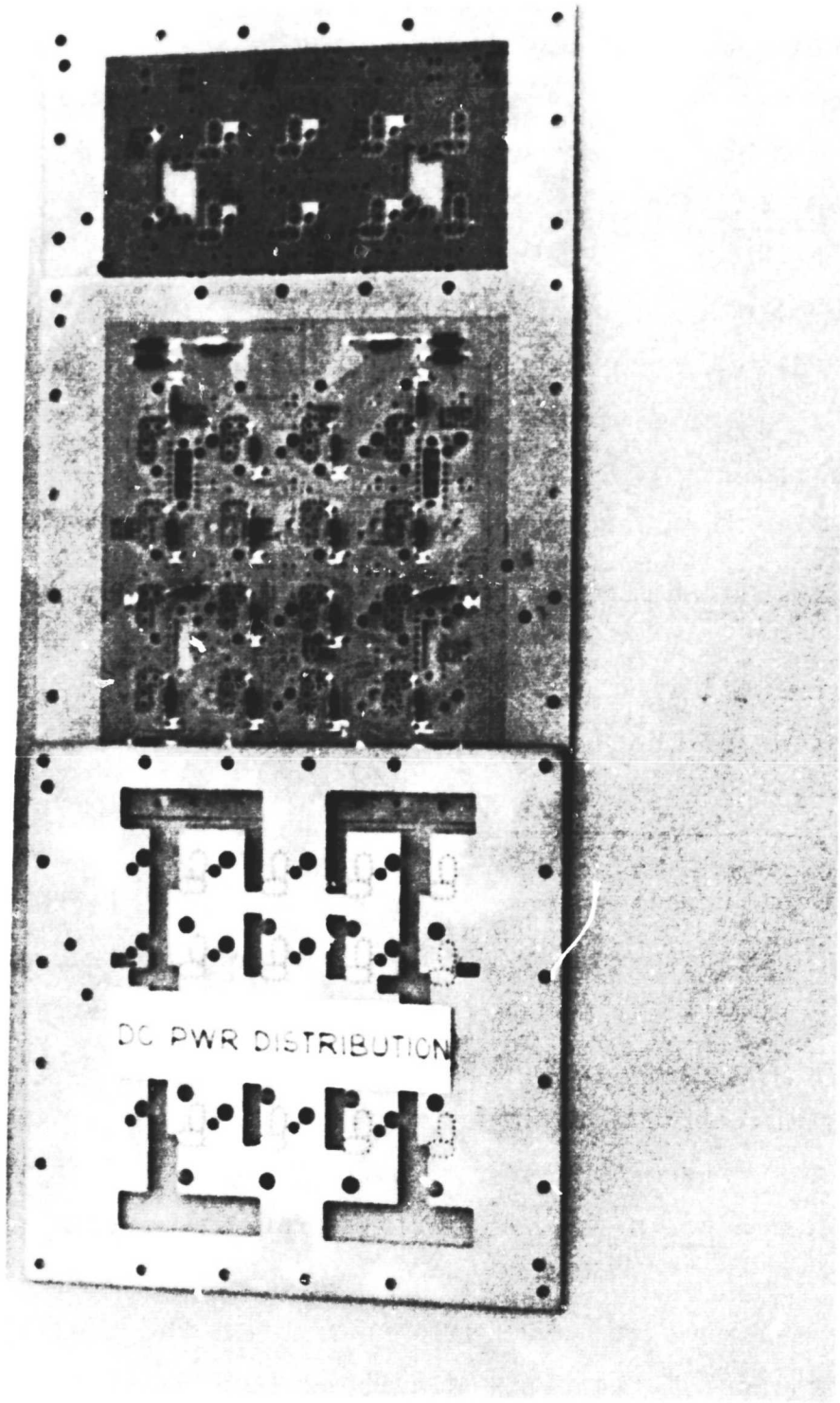


Figure 46 A19 - Power Distribution Board Configuration

4.3.4 A20 IF Combiner

Figure 47 is a rear view photograph of the 4 x 4 array. The IF combiner can be noted directly below the 4 x 4 module array. Figure 5 shows the schematic diagram. An amplitude control and an individual phase shift control is provided for each module IF output signal. These two controls provide a method of readily optimizing the receiver pattern at boresight. These controls are not to be readjusted after the initial boresight calibration.

The IF combiner also has four 3 db hybrids, Z-1 through Z-4, which are used to combine all sixteen module IF output signals to form a Σ (summation pattern), a Δ_{AZ} (difference pattern in azimuth) and a Δ_{EL} (difference pattern in elevation).

4.3.5 A21 Beam Steering Unit

The beam steering unit with its forth-eight potentiometers is shown at the right hand side of the 4 x 4 array structure shown in Figure 47. Figure 5 shows the schematic diagram.

Thirty-two potentiometers are mounted on the top of this unit. Sixteen of the controls (x 2 bias) steer the main beam of the transmitter and sixteen of the controls (R_c bias) steer the main beam of the receiver. Sixteen screwdriver adjust potentiometers (x 5 bias) are used to set the x 5 transmitter multipliers at proper bias level to achieve the best power output mode as the drive from the x 2 multiplier is varied in phase. The preset values should not be varied during transmitter beam steering.

Test monitoring switches are available to measure the amplitude of dc bias voltage for each of the above mentioned functions.

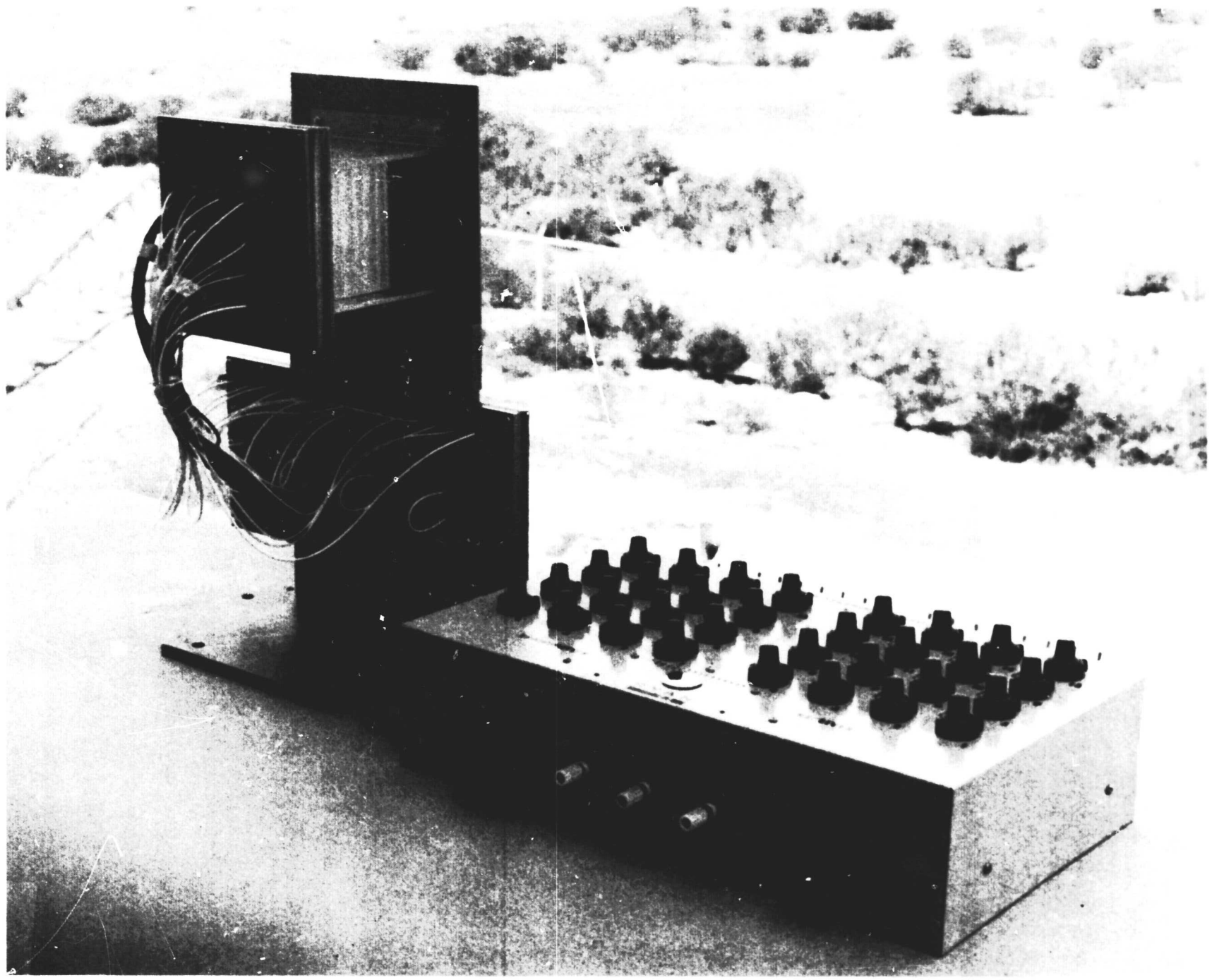


Figure 47 Rear View of 4 x 4 C-Band Array

4.4 4 X 4 ARRAY TESTING

The pattern measurements of the 4 x 4 transmitter/receiver array were made in an aneochoic chamber. The dimensions of the chamber permitted the test horn to be 12 feet from the aperture, which provides for field operation at 5.75 GHz.

The 4 x 4 array was mounted on a Scientific-Atlanta 5505B, three axis antenna positioner. Figure 48 is a block diagram of the test circuit used to measure the receiver patterns. A signal generator, HP 618, was used to drive a test horn for these tests.

Figure 49 is a block diagram of the test circuit used to measure the patterns for the transmitter. For these tests, the standard test horn was used to measure 4 x 4 array radiated power.

Table V tabulates the various patterns which were measured. Receiving and transmitting patterns were measured in both E and H planes.

The receiver patterns have the Σ (summation) and Δ (difference patterns) shown on the same plot. The transmitter pattern has just the one pattern where all module outputs are combined at the same effective phase front.

Observation of the receiver patterns, Figures 50 through 69 will show that the summation pattern at boresight has a beamwidth of approximately 26° (this corresponds to the $101/\eta$ relationship where η is the number of modules in a row or column). The second side lobes are more pronounced for the H-plane cut than for the E-plane. The gains between the various patterns are not necessarily the same so should not be compared. Patterns do start to degrade at ±45° beam steering angle but the difference pattern null is still believed to be sufficient to allow adequate system tracking function.

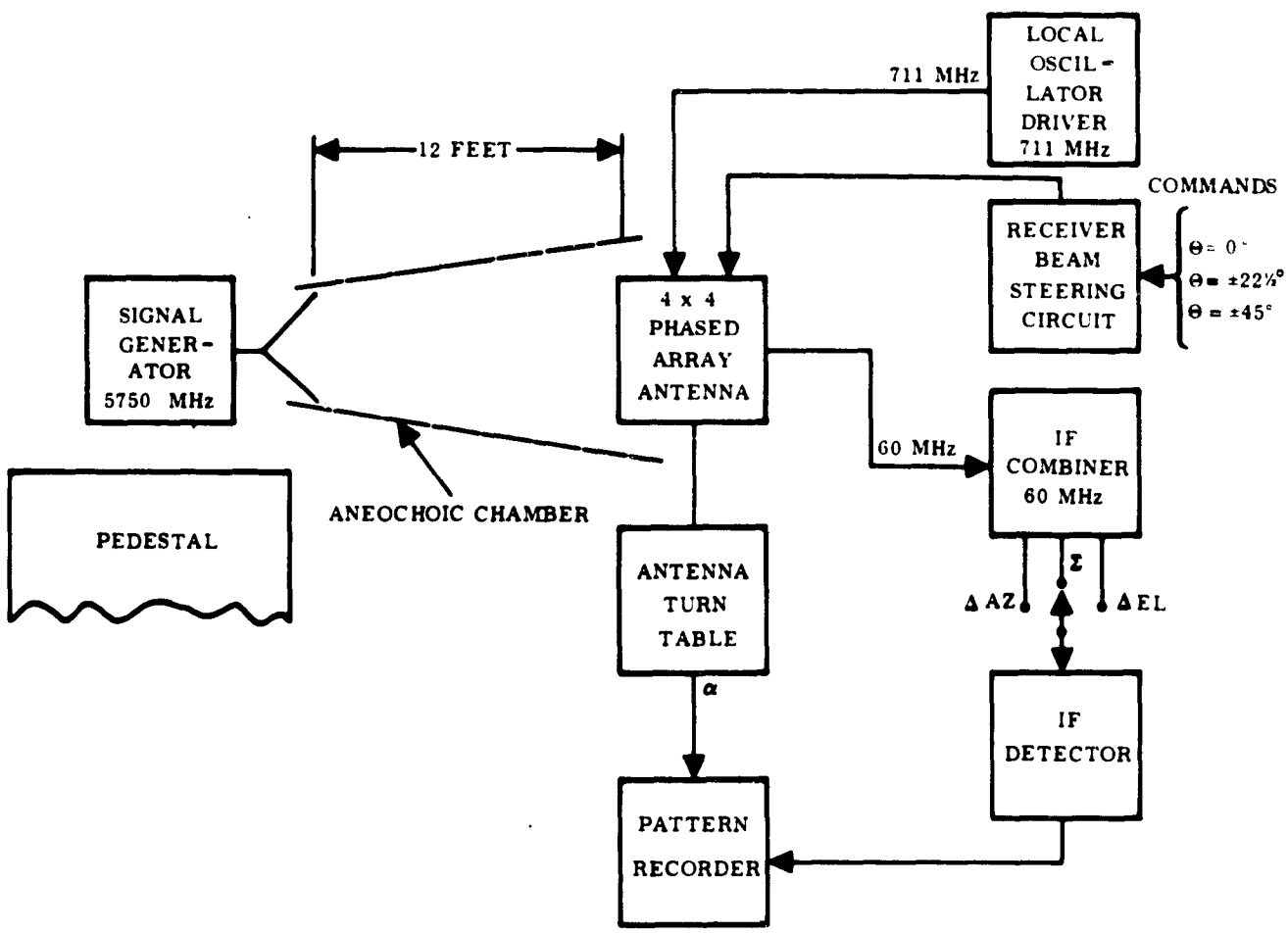


Figure 48 Equipment Arrangement for Evaluating Performance of Receiving Antenna

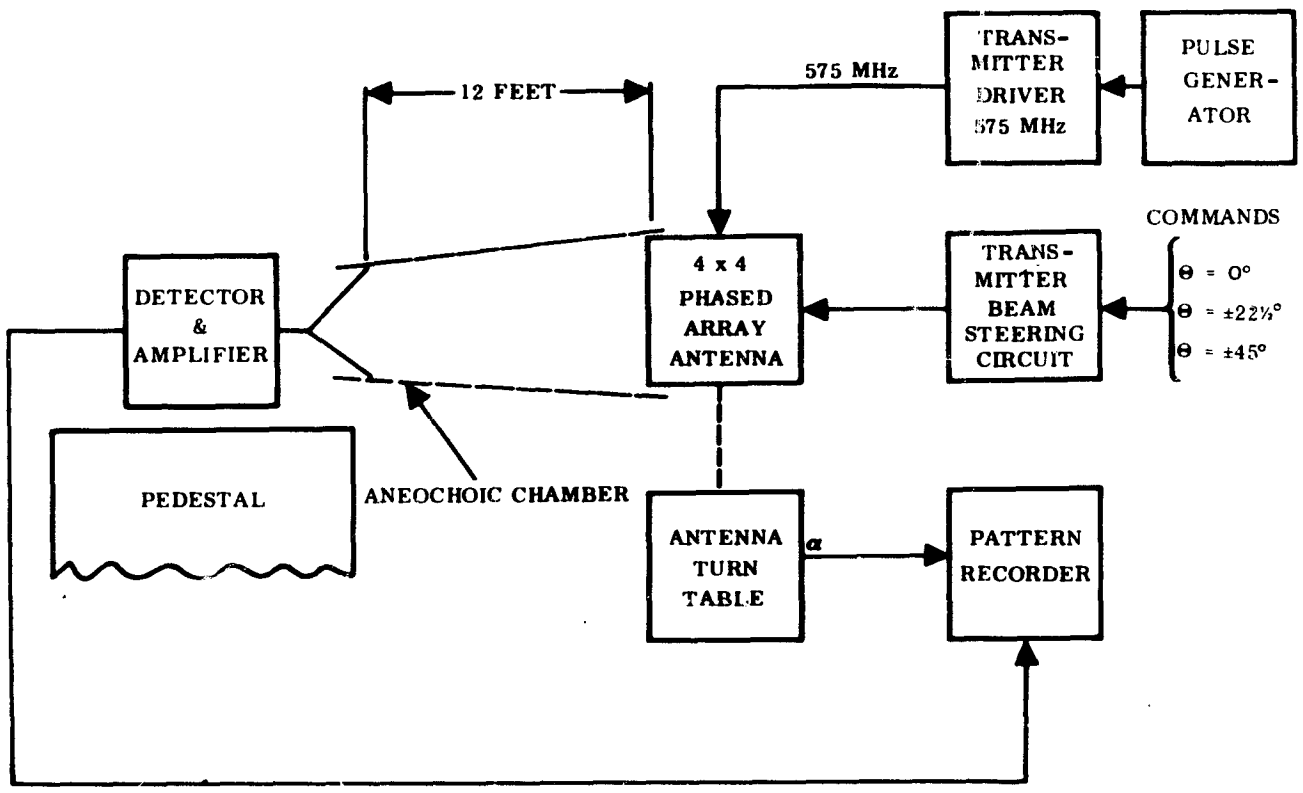


Figure 49 Equipment Arrangement for Evaluating Performance of Transmitter Antenna

TABLE V. 4 X 4, C-BAND, TRANSMITTING/RECEIVING ARRAY PATTERN MEASUREMENTS

FIGURE	ARRAY MODE	PLANE	BEAM STEERING ANGLE DEGREES
50	Receiver Patterns	E	Boresight
51	Receiver Patterns	E	+22½
52	Receiver Patterns	E	+45
53	Receiver Patterns	E	-22½
54	Receiver Patterns	E	-45
55	Receiver Patterns	H	Boresight
56	Receiver Patterns	H	+22½
57	Receiver Patterns	H	+45
58	Receiver Patterns	H	-22½
59	Receiver Patterns	H	-45
60	Transmitter Patterns	E	Boresight
61	Transmitter Patterns	E	+22½
62	Transmitter Patterns	E	+45
63	Transmitter Patterns	E	-22½
64	Transmitter Patterns	E	-45
65	Transmitter Patterns	H	Boresight
66	Transmitter Patterns	H	+22½
67	Transmitter Patterns	H	+45
68	Transmitter Patterns	H	-22½
69	Transmitter Patterns	H	-45

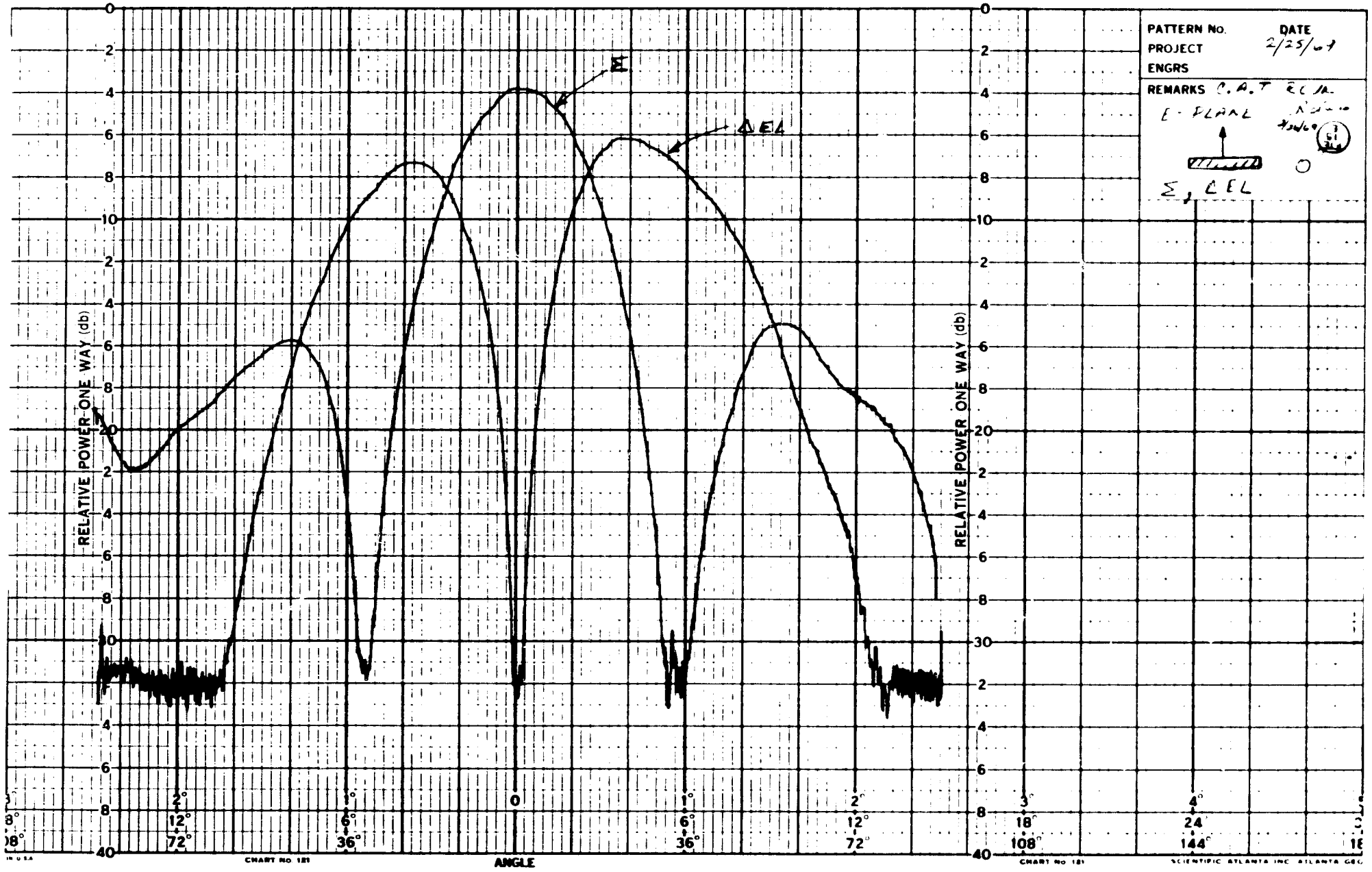


Figure 50 Receiver Pattern, E Plane, Boresight (0°)

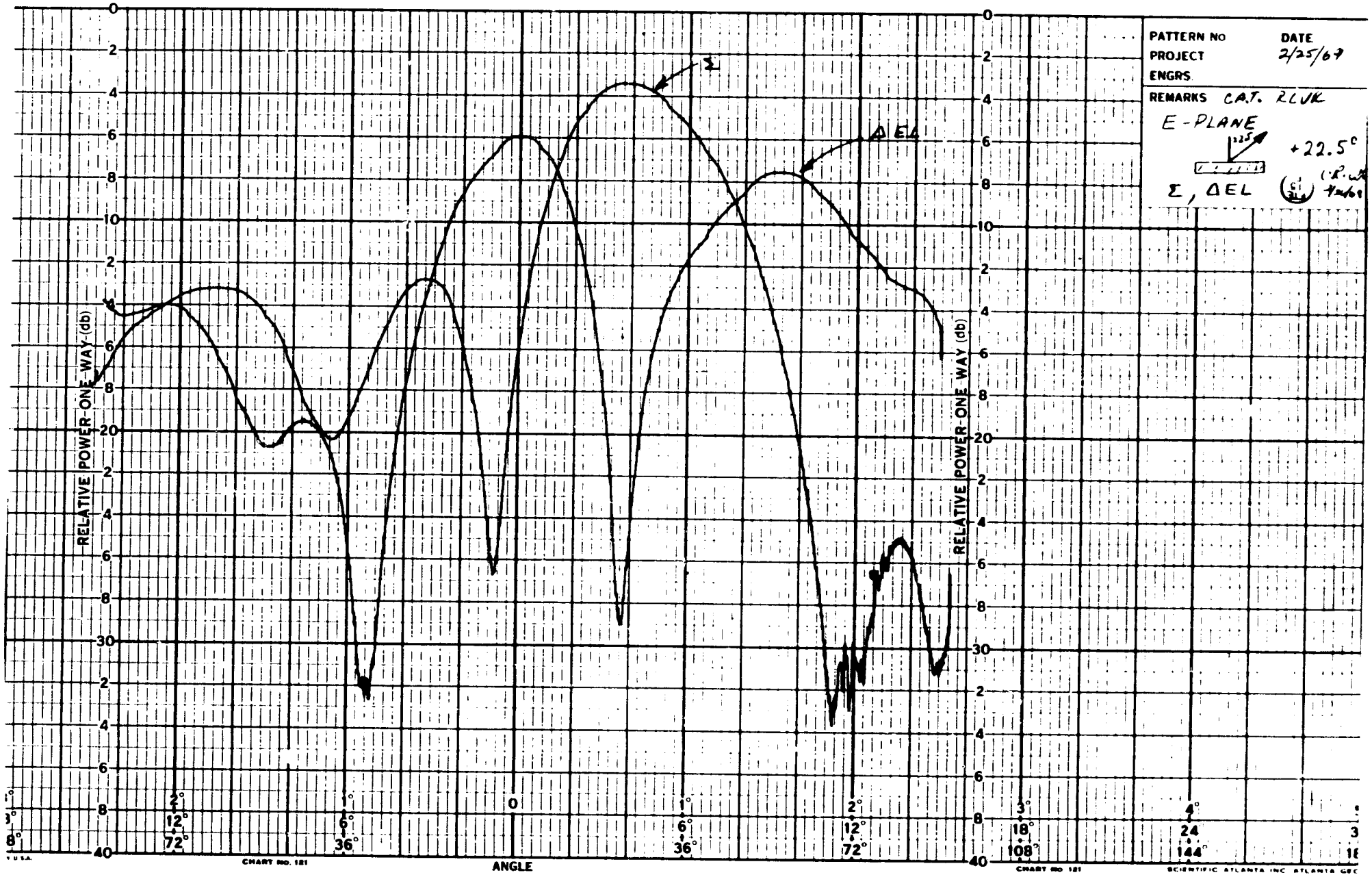


Figure 51 Receiver Pattern, E Plane, +22.5°

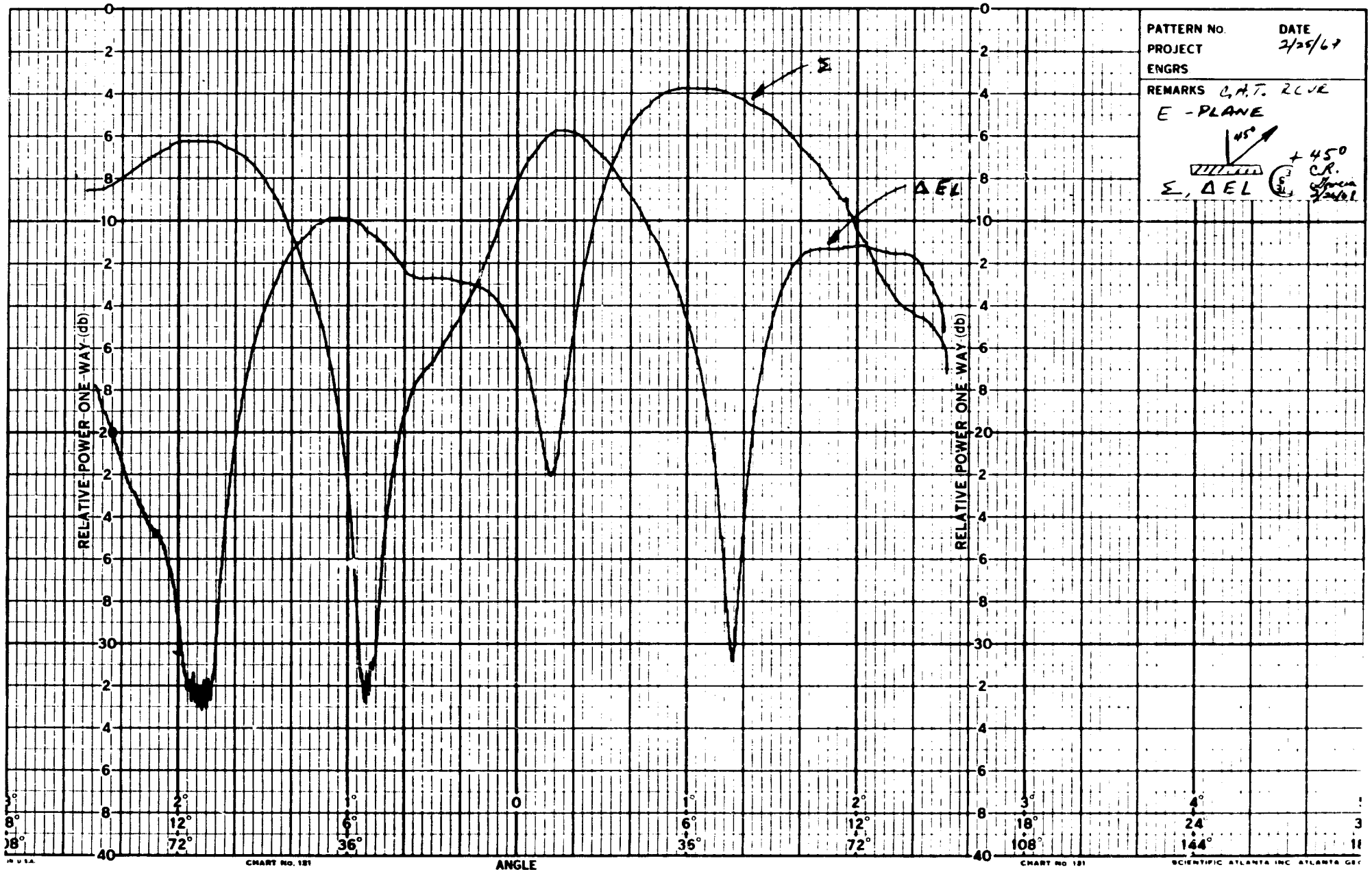


Figure 52 Receiver Pattern, E Plane, +45°

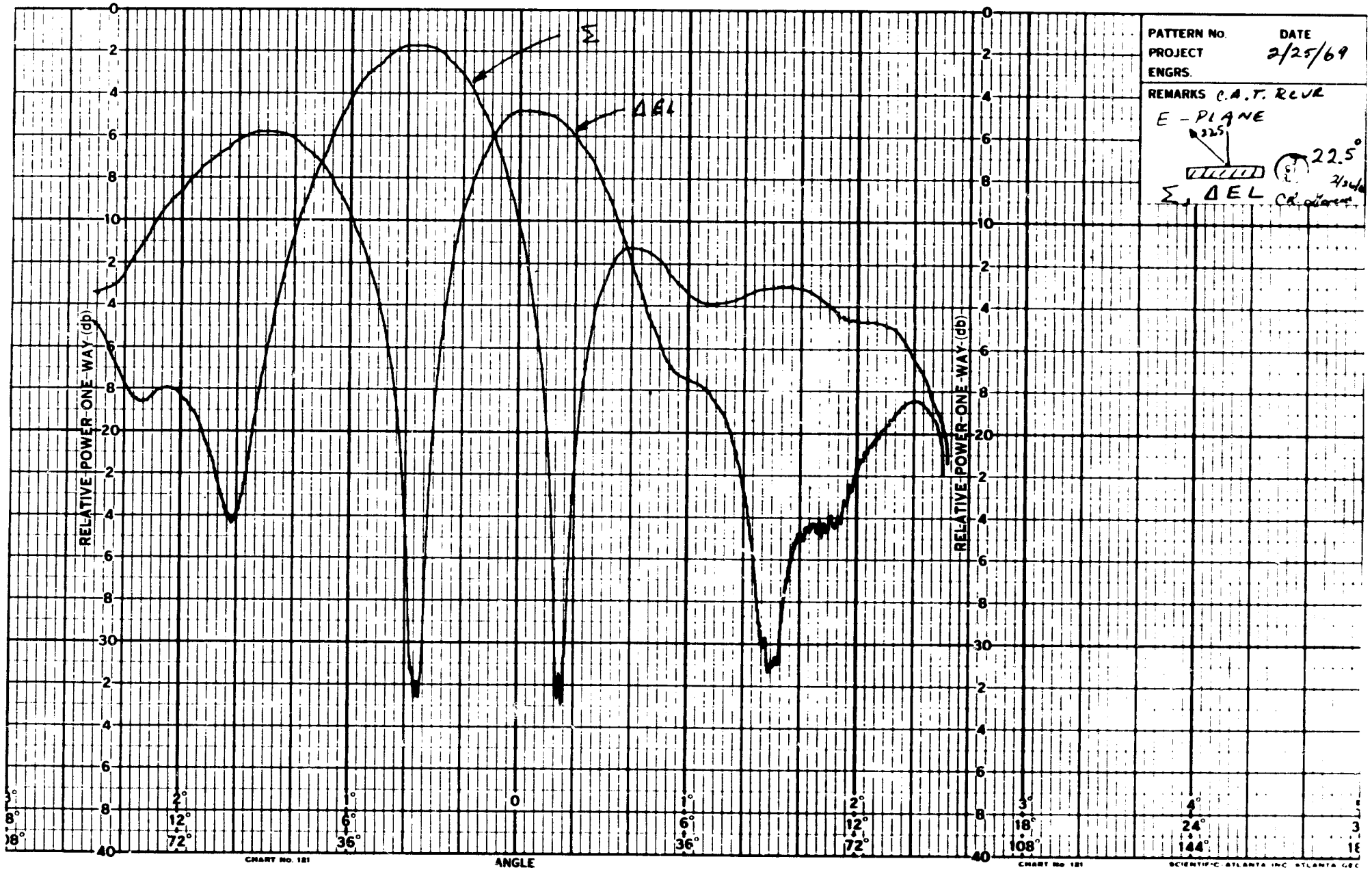


Figure 53 Receiver Pattern, E Plane, -22.5°

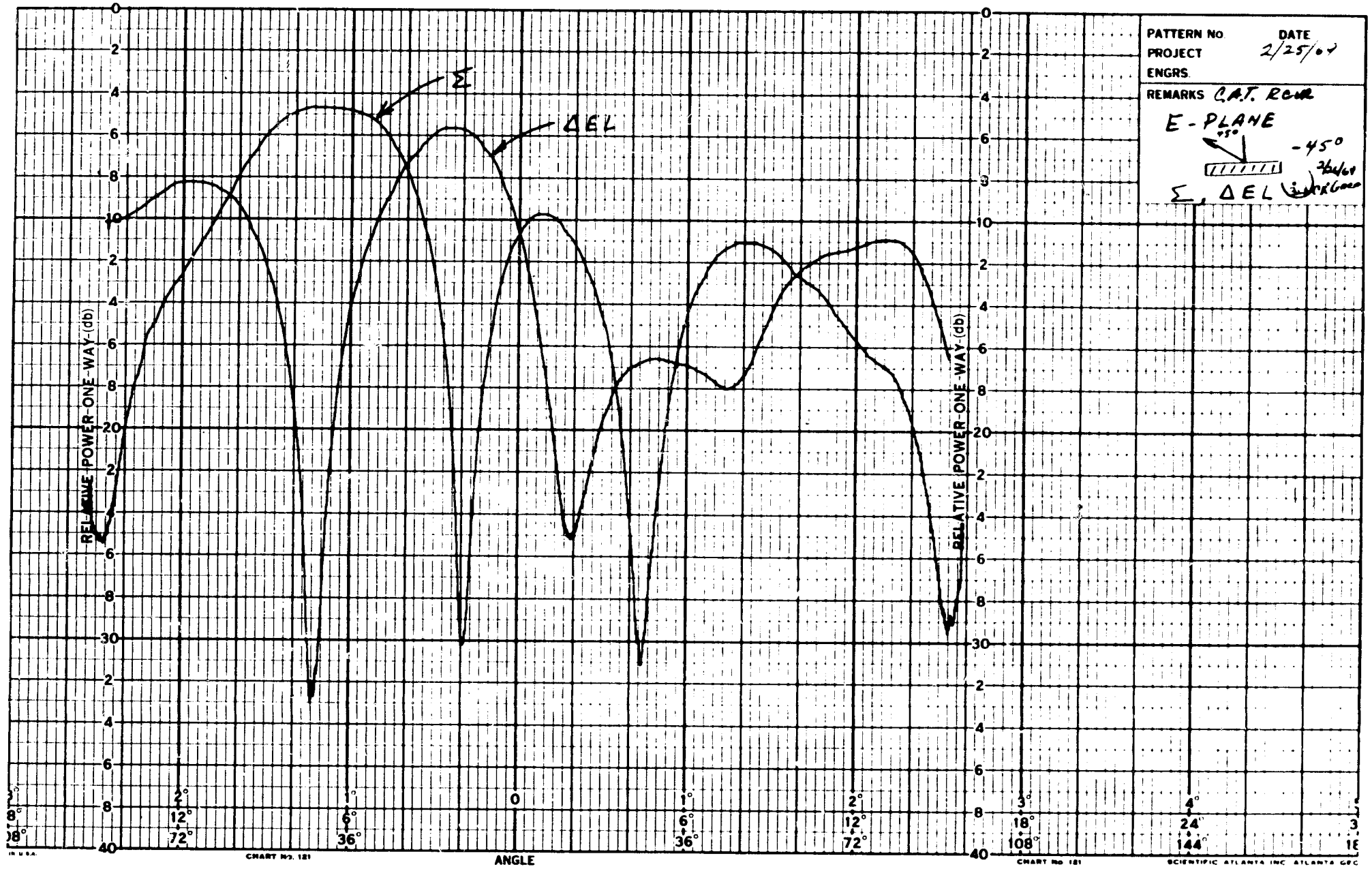


Figure 54 Receiver Pattern, E Plane, -45°

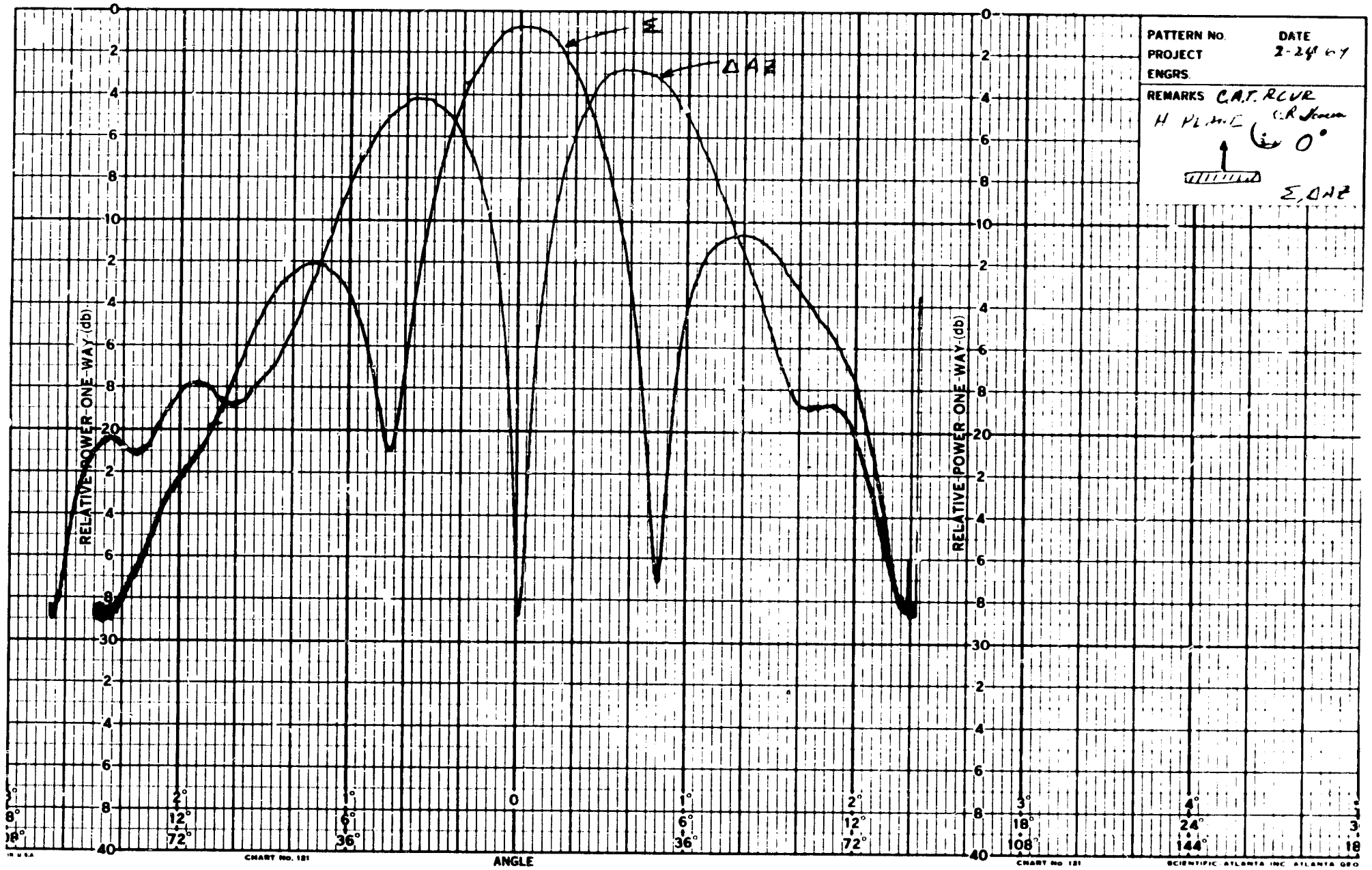


Figure 55 Receiver Pattern, H Plane, Boresight (0°)

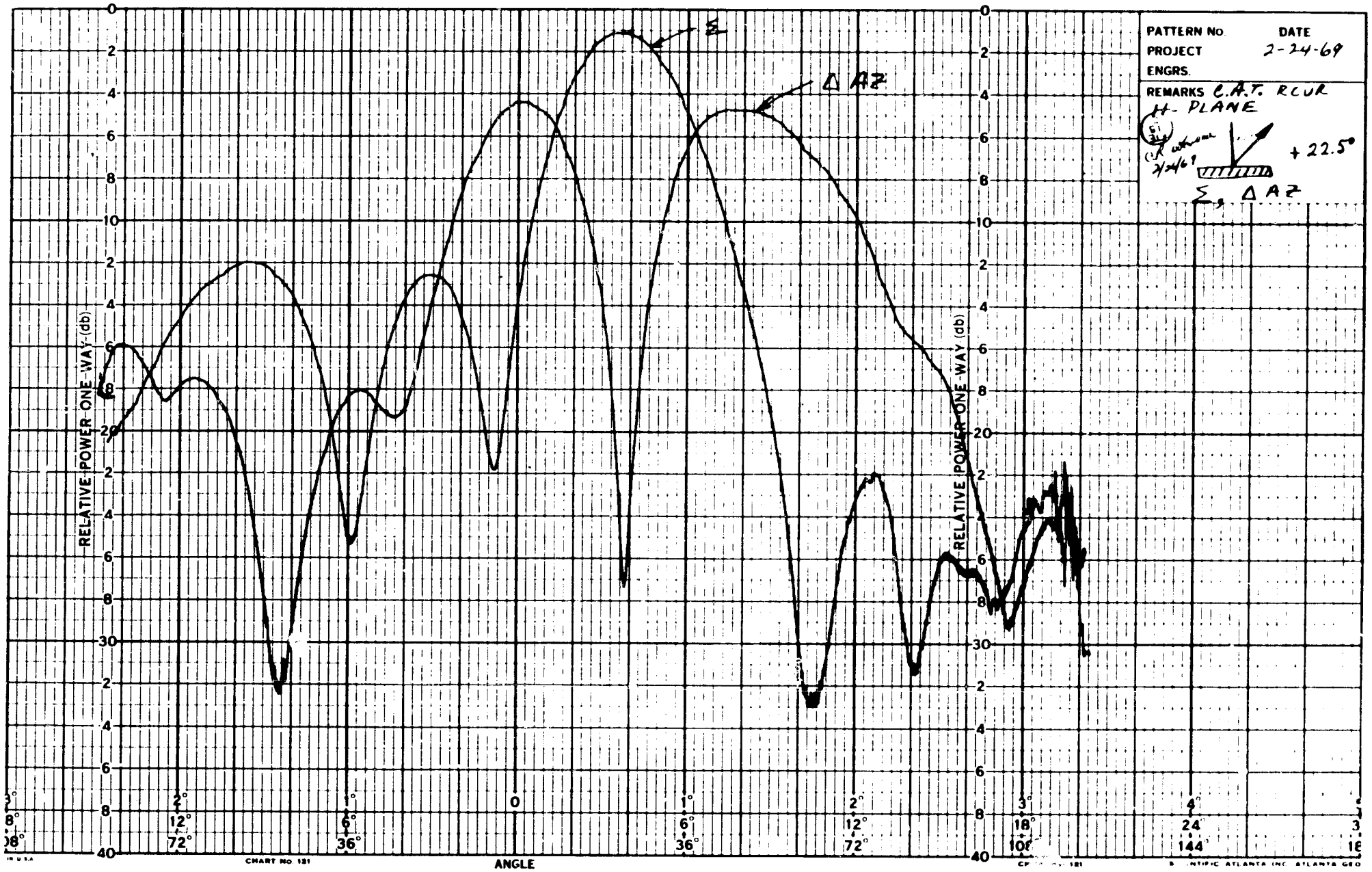


Figure 56 Receiver Pattern, H Plane, +22.5°

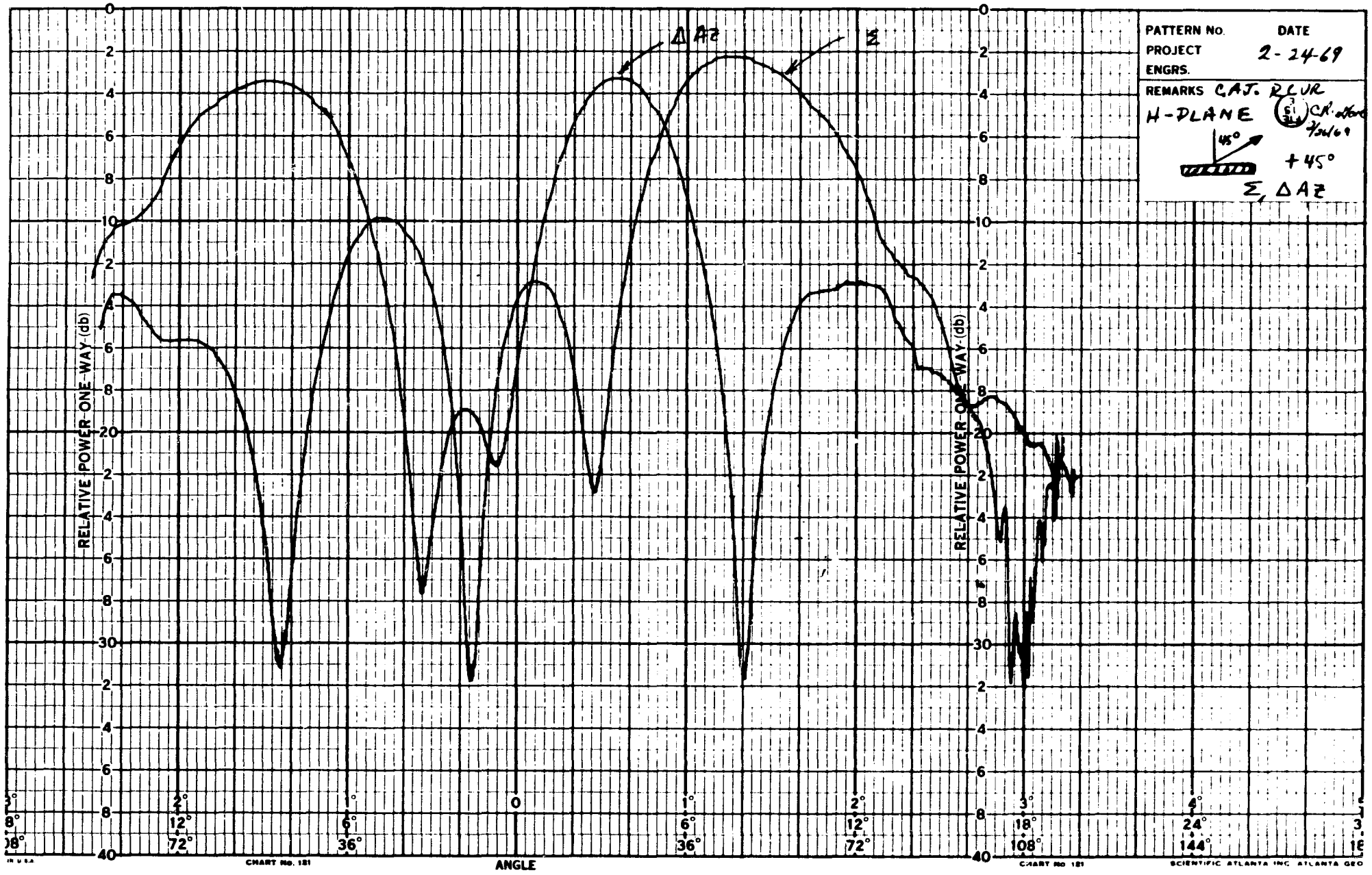


Figure 57 Receiver Pattern, H Plane, +45°

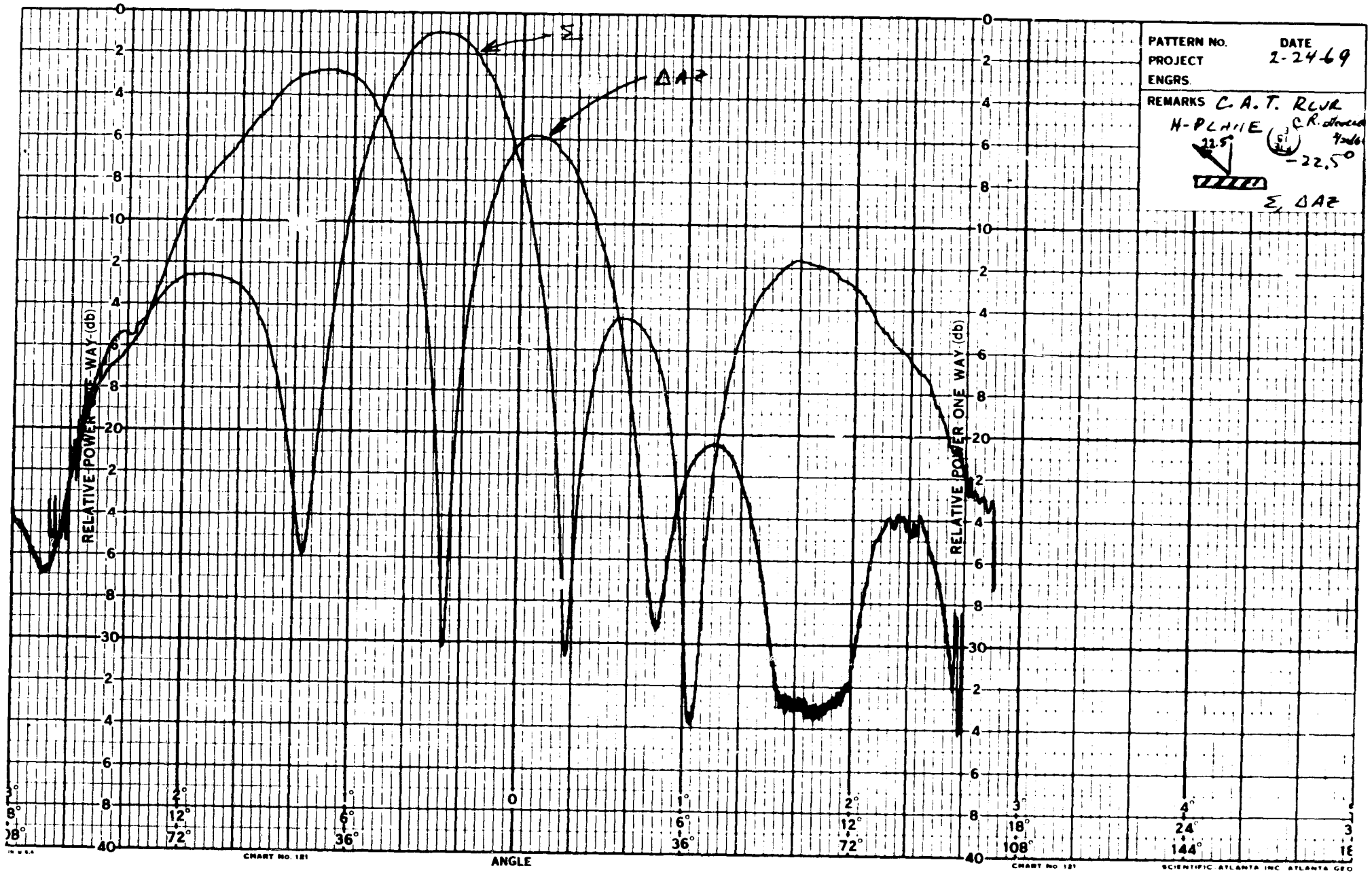


Figure 58 Receiver Pattern, H Plane, -22.5°

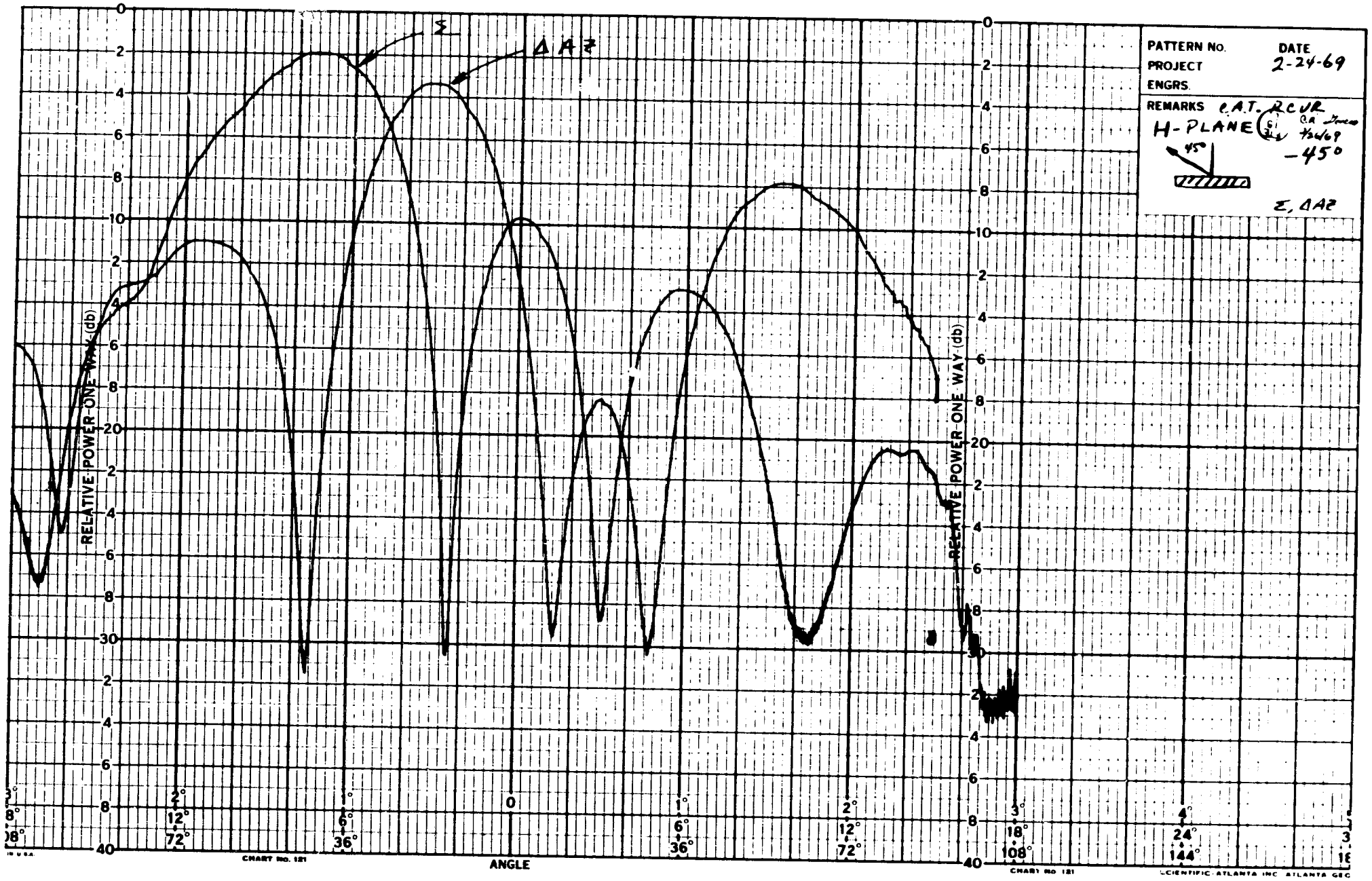


Figure 59 Receiver Pattern, H Plane, -45°

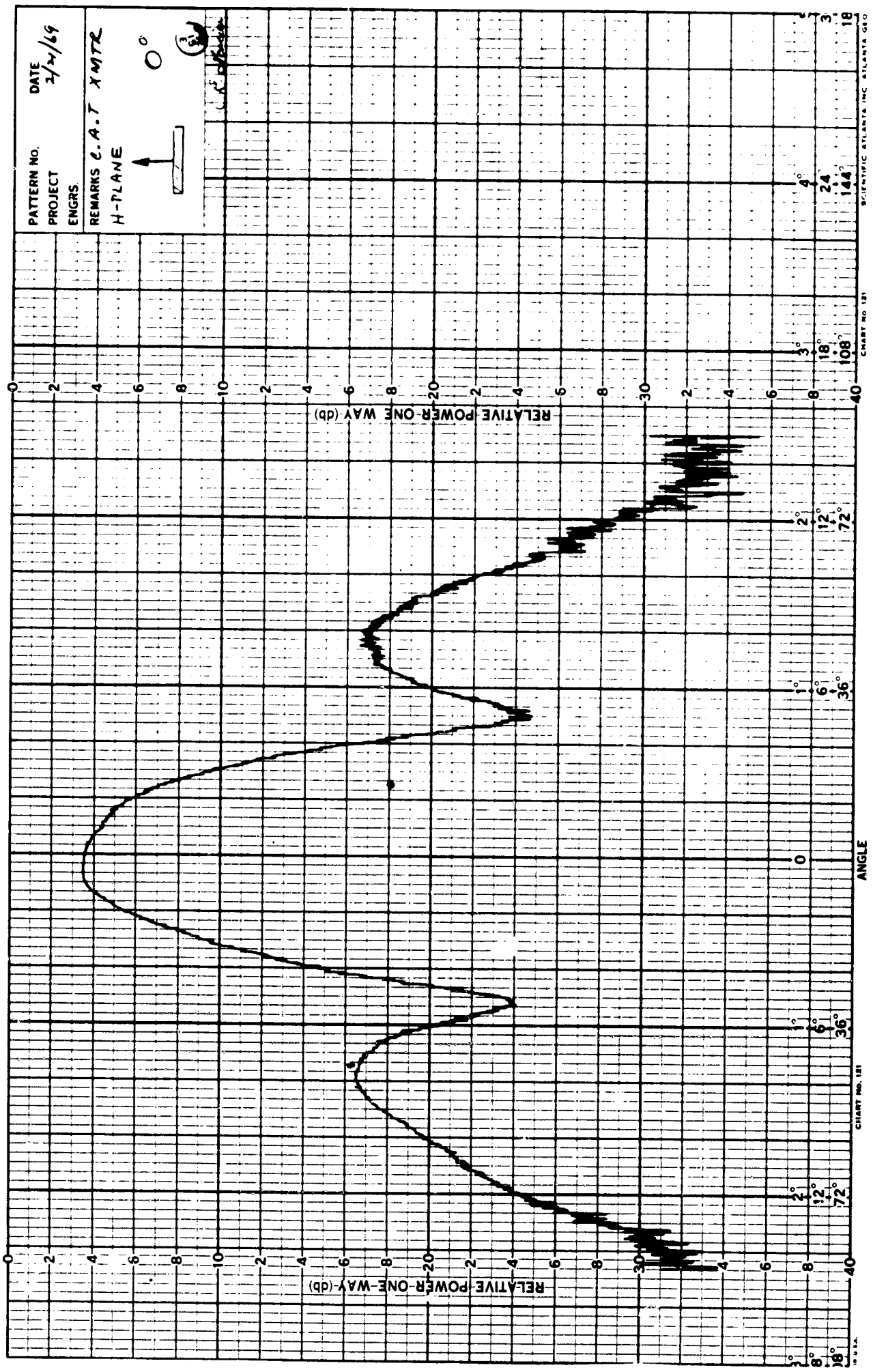


Figure 60 Transmitter Pattern, E Plane, Boresight (0°)

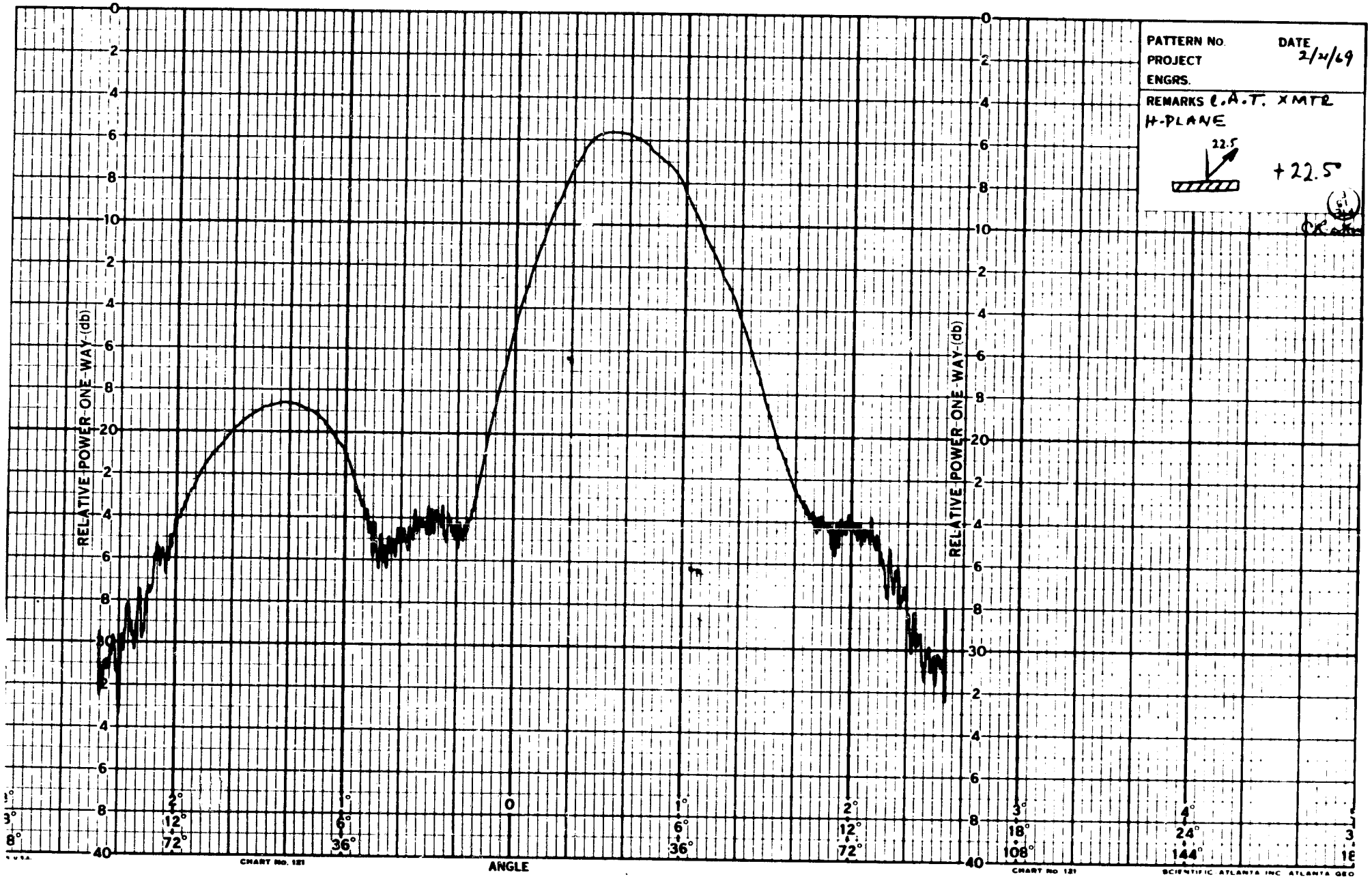


Figure 61 Transmitter Pattern, E Plane, +22.5°

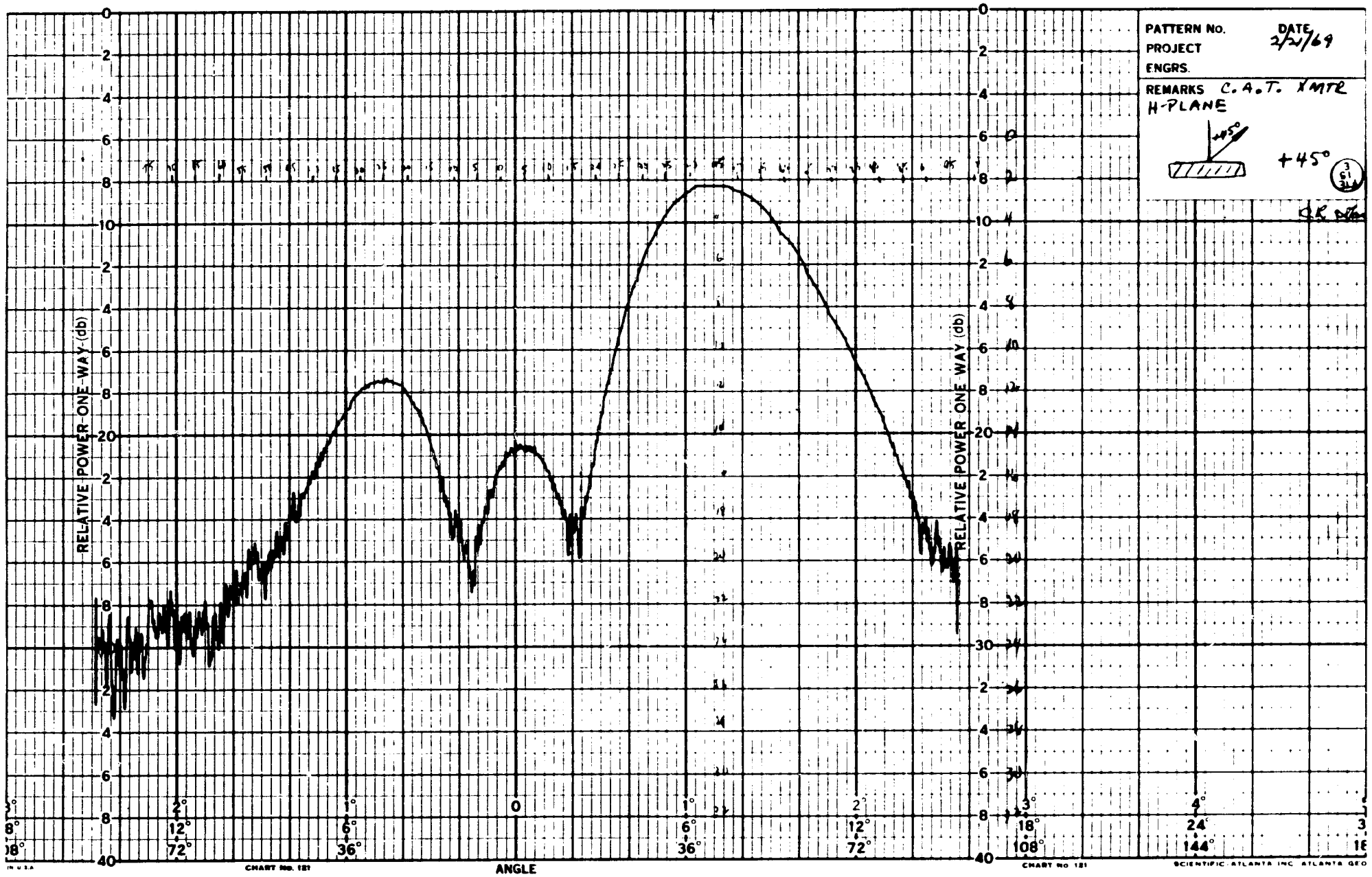


Figure 62 Transmitter Pattern, E Plane, +45°

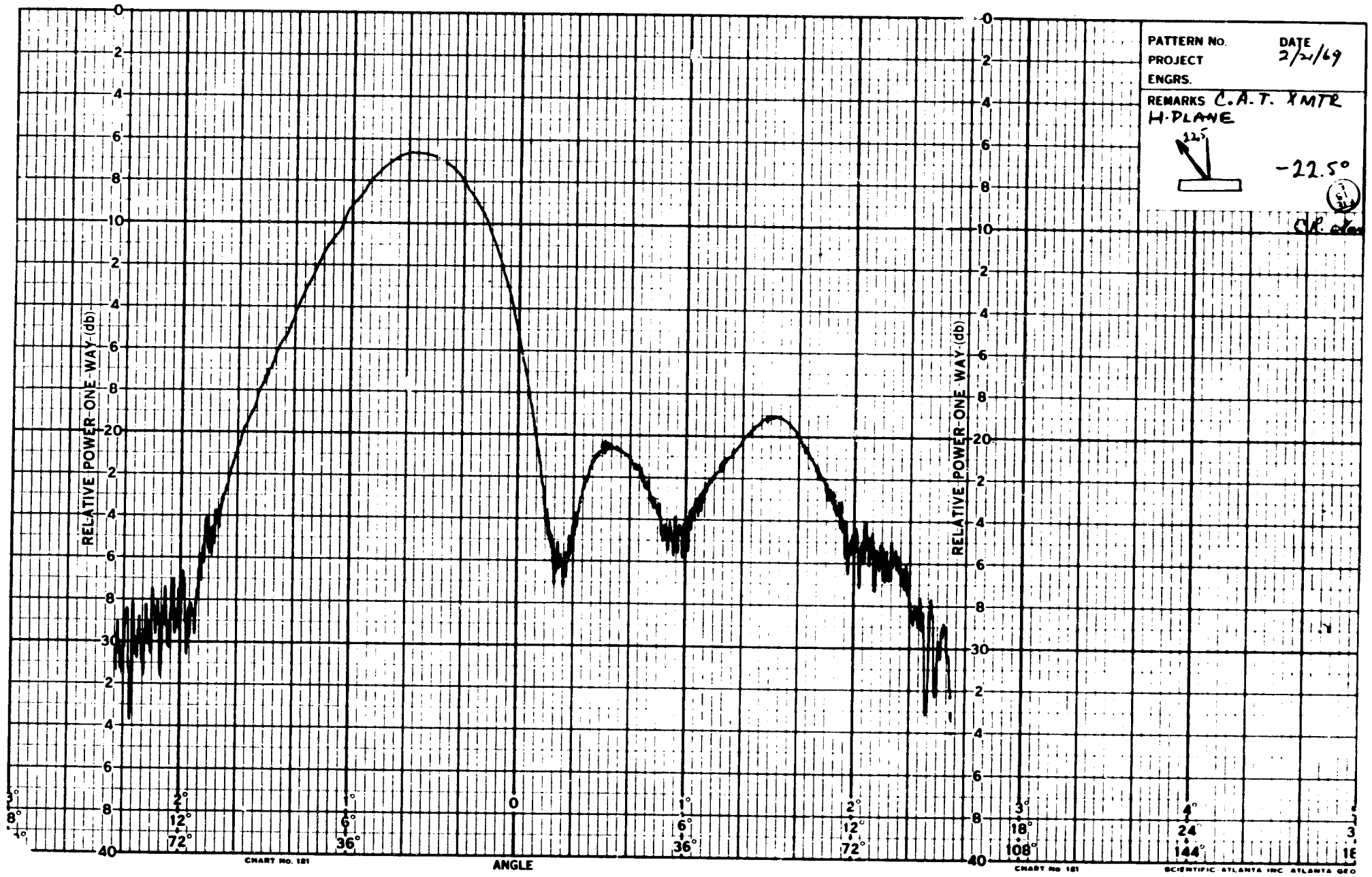


Figure 63 Transmitter Pattern, E Plane, -22.5°

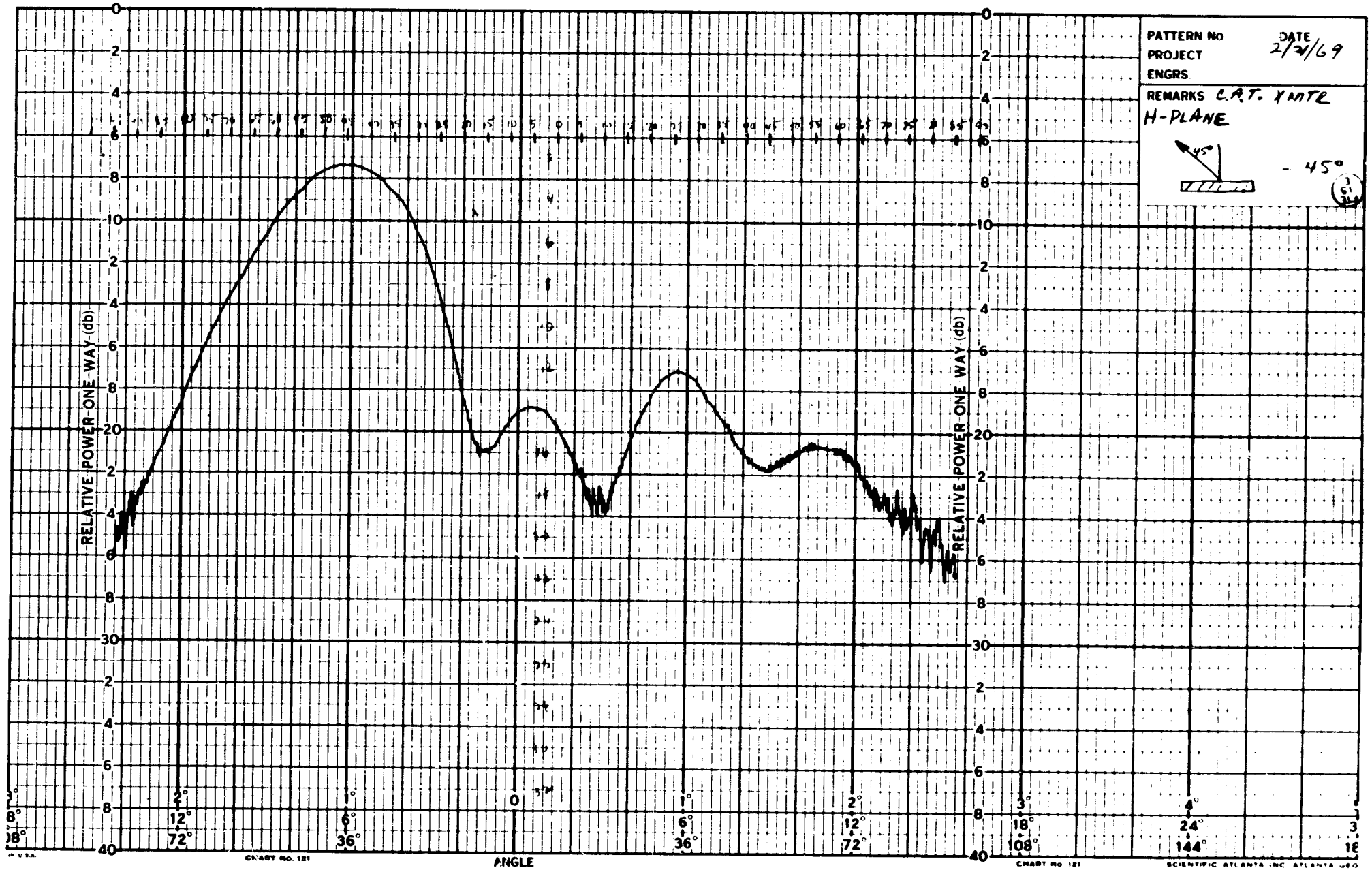


Figure 64 Transmitter Pattern, E Plane, -45°

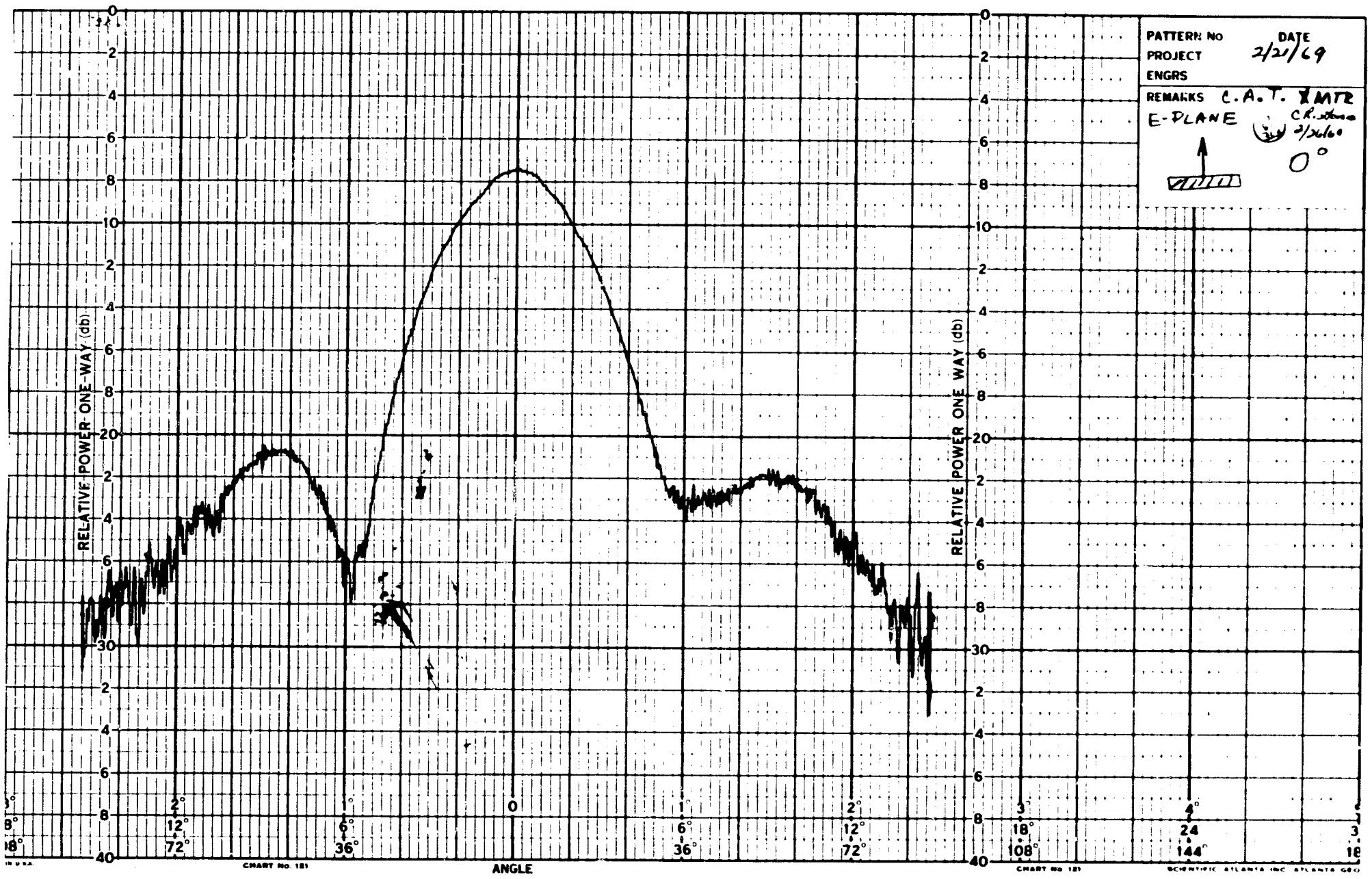


Figure 65 Transmitter Pattern, H Plane, Boresight (0°)

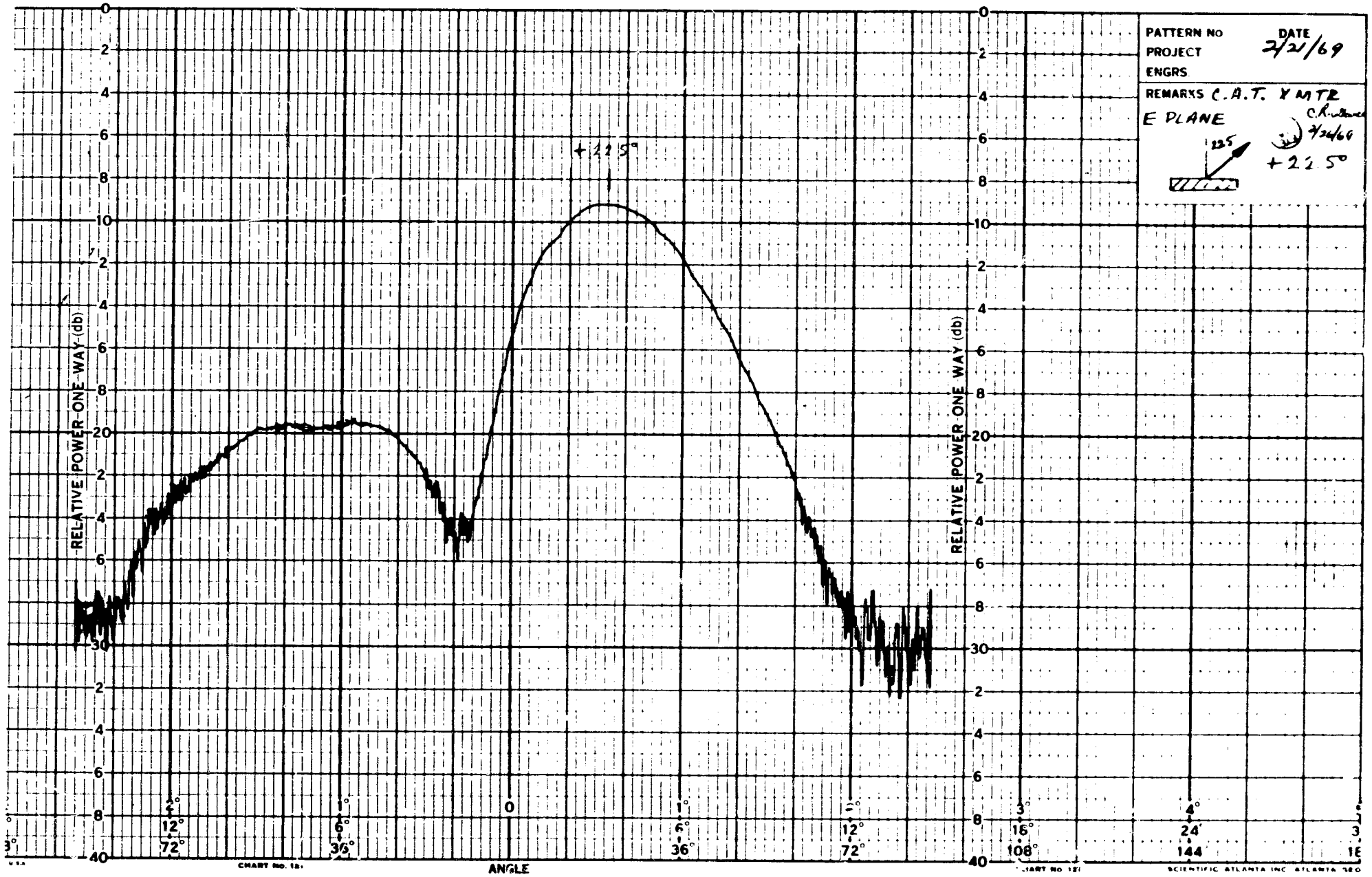


Figure 66 Transmitter Pattern, H Plane, +22.5°

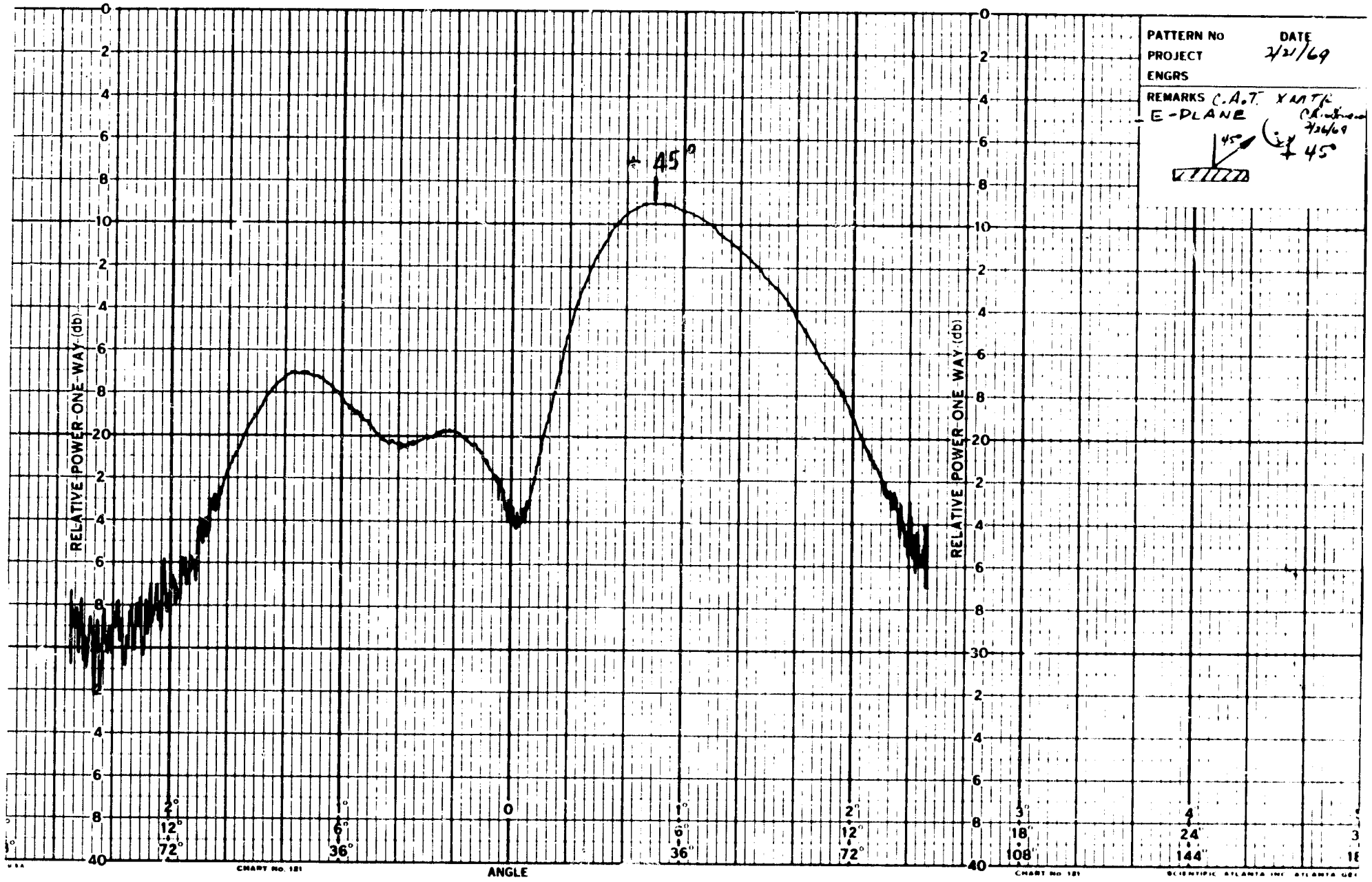


Figure 67 Transmitter Pattern, H Plane, +45°

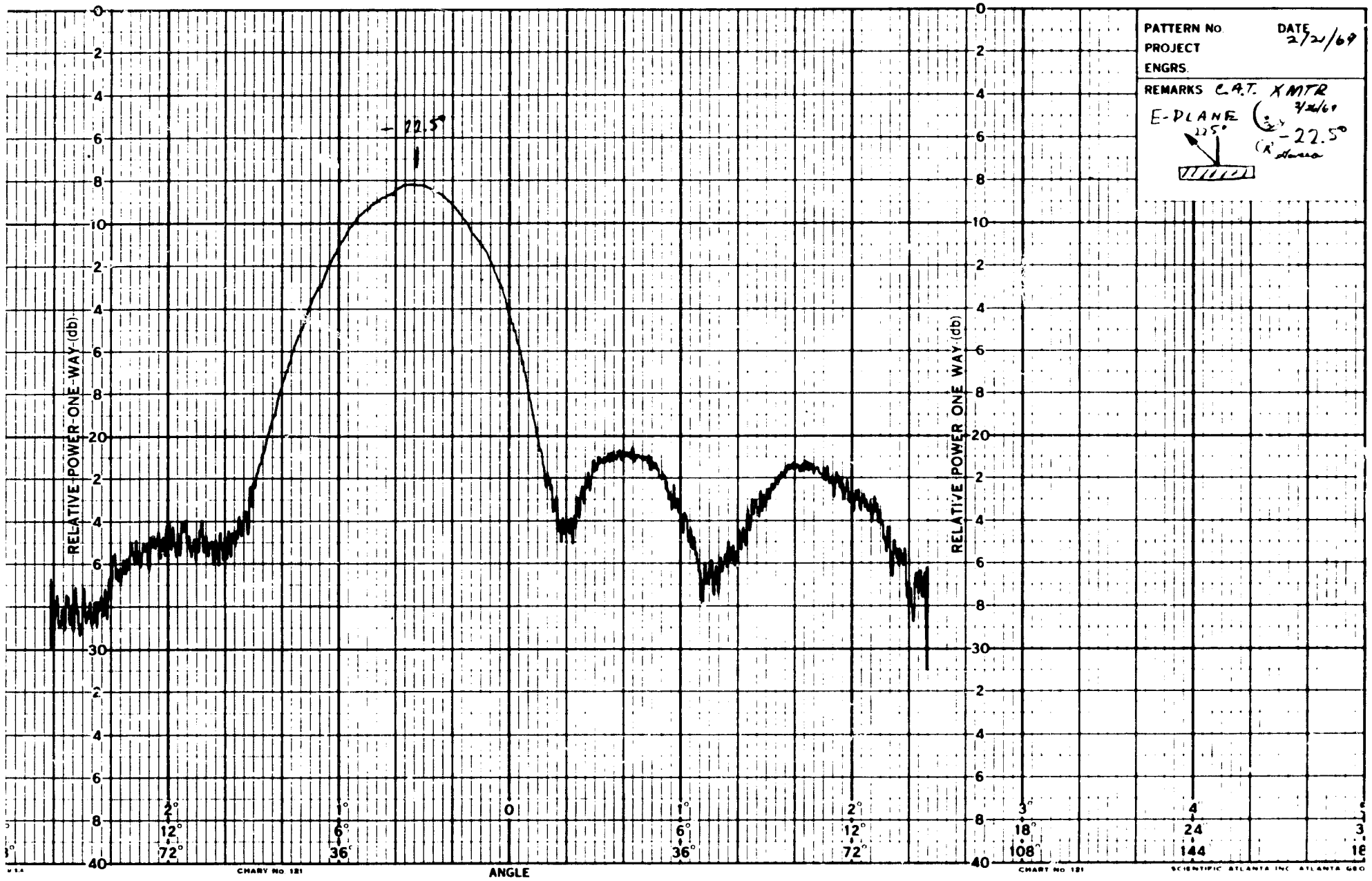


Figure 68 Transmitter Pattern, H Plane, -22.5°

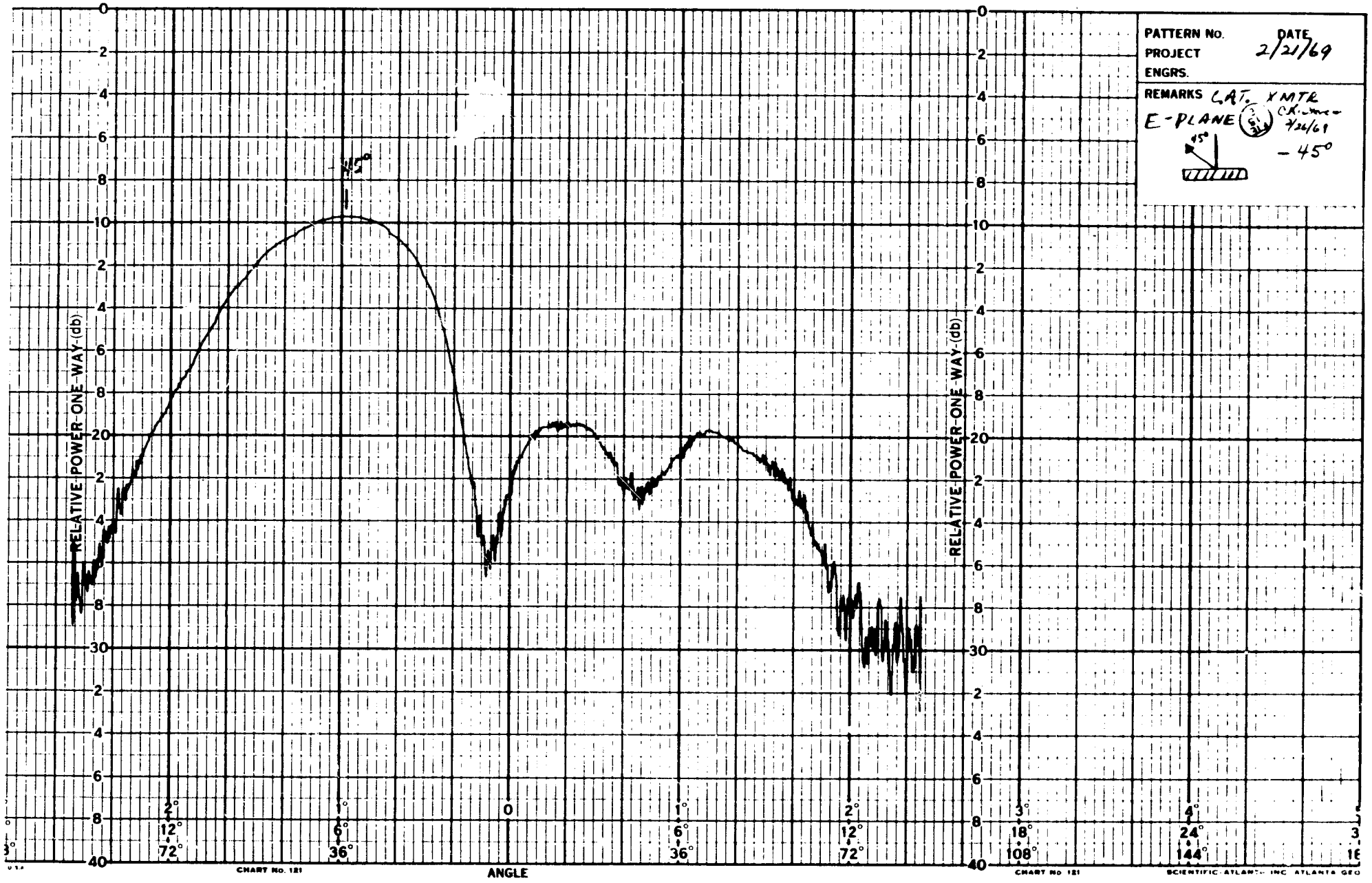


Figure 69 Transmitter Pattern, H Plane, -22.5°

Observation of the transmitter patterns at boresight show the first sidelobe amplitudes to be ≈ -13.5 db as expected.

4.5 WEIGHT AND SIZE ESTIMATE OF FUTURE ARRAY

This section presents a weight and size estimate of a 20 x 20 module array.

4.5.1 Future System Weight Considerations

The measured weights of hardware developed for this program will serve as the basis for estimating the weight of a 20 x 20 module array.

Each present stripline module weights 0.533 pound. Subsequent weight reductions will now be considered.

4.5.1.1 Receiver Weight Reduction

Some preliminary effort has been done to develop the entire receiver portion of the module in MIC. The weight of the engineering prototype of this entire receiver module, including the stripline antenna aperture is 0.06 pound. The entire receiver portion of the stripline module weighs 0.165 pound. Thus, the MIC receiver will reduce module weight by 0.105 pound.

The stripline antenna aperture could be repackaged in MIC eliminating an additional estimated 0.025 pound.

4.5.1.2 Transmitter Weight Reduction

Three areas of weight reduction should be possible with the transmitter portion of the module:

- Eliminate isolation between two multipliers. This should be possible by additional development to properly match the input/output VSWR and thereby reduce isolator requirements. This would reduce module weight by 0.12 pound.

- Redesign the x 2 multiplier circuitry to eliminate the interconnection wafers. Based on MIC receiver development, it is estimated that 0.03 pound can be eliminated.

- Change the present finite circulation to a ferrite service in MIC. The present finite circulation weighs 0.07 pound. It is estimated that an MIC circulator would weight 0.025 pound, thereby saving 0.045 pound.

Combination of these module improvement results in the following:

Present stripline transmit/receive mode	-	0.533 pound
Less MIC Receiver	-	0.105 pound
Less MIC Antenna Aperture	-	0.025 pound
Less Transmitter Isolation	-	0.120 pound
Less repackaged x 2 multiplier	-	0.030 pound
Less MIC circulator	-	0.045 pound
Estimated weight/module		0.208 pound

4.5.1.3 Estimated System Interconnect Weight

The present system interconnect weight has been calculated to be 0.132 pound/module. It is anticipated that this can be improved to 0.07 pound/module. Redesign of the IF combiner would provide the most benefit.

4.5.1.4 Combined 20 x 20 Array Antenna System Weight

The above paragraphs can be combined as follows:

Per Module Weight	0.208 pound
Per Module System Interval	0.070 pound
Total Array Weight	0.278 pound/module

Therefore a 20 x 20 array would weigh 0.278 pound/module x 400 modules ≈ 111 pounds.

4.5.2 Future System Volume Considerations

The present module length is 5.55 inches. The present interconnect board assembly, A17, A18 and A19, is approximately 0.625 inch.

It is estimated that MIC receiver redesign will reduce receiver module length by 0.8 inch. Eliminating the isolation reduces the transmitter length by 0.6 inch. Changing the circulator from finite to MIC configuration should reduce length by 0.5 inch. Redesign of the x 2 multiplier should reduce length by 0.25 inch. This results in a module length of:

Present module length	5.55 inches
Less MIC receiver length reduce	-0.80 inch
Less isolation	-0.60 inch
Redesign of circulator	-0.50 inch
Redesign of x 2 multiplier	-0.25 inch
Resultant module length	3.40 inches

It is anticipated that all antenna system functions could be configured in a system interconnect assembly 1.0 inch in length. This would result in a total antenna system depth of 4.40 inches.

A 20 x 20 C-Band array (5.75 GHz) spaced at 0.965 inch would result in a total volume of 0.965 inch/module x 20 modules = 19.3 inches x 19.3 inches x 4.40 inches = 1640 cubic inches, less mounting structure.

SECTION 5

TECHNICAL DISCUSSION - POLARIZATION CONTROL AND TR SWITCH DEVELOPMENT

5.1 INTRODUCTION

In accordance with the requirements of contract NAS 9-7626 for the Engineering Model of an Electronically Scanned Phased Array System, Ryan Aeronautical developed, fabricated and tested a breadboard model of a polarization control and TR switch.

The purpose of the breadboard model was to demonstrate with hardware the the operation of a TR switching device and polarization control circuitry having capabilities for transmitting and receiving linearly or circularly polarized waves. The performance goals were as follows:

Transmit:	Vertical Polarization
	Horizontal Polarization
	Right Hand Circular Polarization (RHCP)
	Left Hand Circular Polarization (LHCP)
Receiver:	Vertical Polarization
	Horizontal Polarization
	RHCP
	LHCP
Isolation:	40 db between transmitter and receiver

5.2 TECHNICAL DESCRIPTION

In order to fabricate a breadboard model of a polarization control and TR switch it was necessary to develop (1) the basic microwave circuit; and (2) develop the components needed to mechanize the circuit. The basic

circuit used for the TR switch and polarization changer is shown in the simplified schematic of Figure 70. In this circuit the transmitter and receiver are connected to two of the terminals of a 90° hybrid power divider. The power divider functions such that when power enters the transmitter terminals (arm 4) it is divided equally at the output arms (2 and 3) as shown in Figure 70; and no power is delivered to the arm 3. In addition to power division the wave appearing in arm 1 is advanced 90° in phase over that in arm 2. Isolation between arms 3 and 4 is a nominal 20 db. Additional isolation between the transmitter and receiver is obtained by adding switches which disconnect the receiver from the hybrid and antenna when the transmitter is energized. When in the receiving mode, the receiver is reconnected, and the transmitter is then disconnected from the hybrid. These switches thus perform the transmit-receive functions. Polarization control of radiated waves from the antenna is obtained by adding 180° and 90° phase shifts between the 90° hybrid power divider and the two spatially orthogonal antennas. By inserting or removing these phase shifters from the circuit, any of the desired polarizations may be obtained. The circuit conditions of the phase shifters for various polarizations for transmitting or receiving modes are given in Table VI.

An overall schematic of the polarization control and TR switch is shown in Figure 71. The components developed for the polarization control and TR switch consisted of the following items:

- TR switch circuit
- 90° hybrid
- 180° and 90° phase shifters

The simplified TR switching circuit is shown in Figure 72. Four diodes are used in a stripline network. The diodes having grounded anodes are Hewlett Packard Model Number 5082-3040 PIN diodes. Grounded cathode types were HP 5082-8828/8836. The diodes are packaged in a stripline

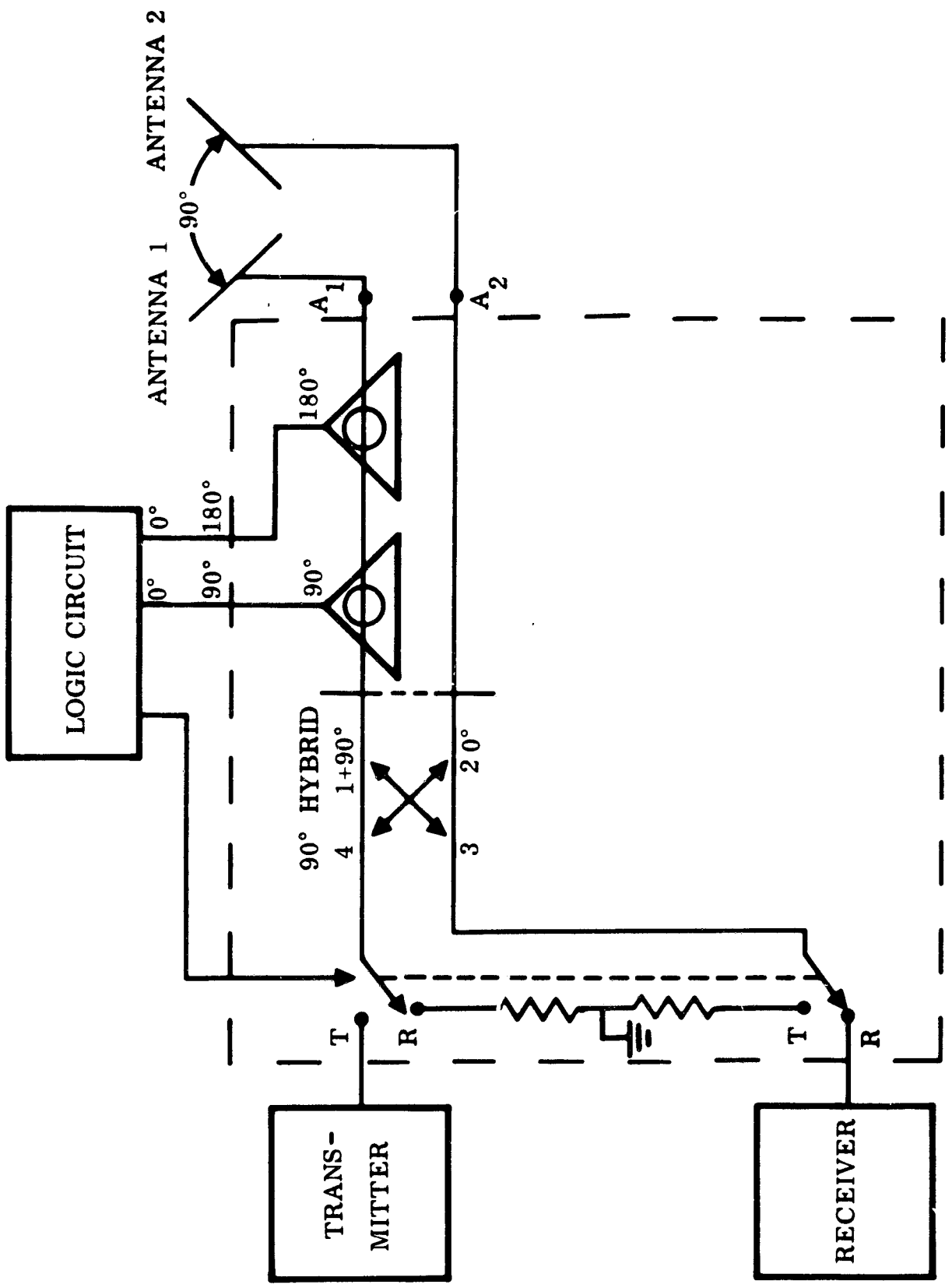


Figure 70 Simplified Schematic Diagram, Polarization Control and T/R Switch

TABLE VI. CIRCUIT CONDITIONS OF PHASE SHIFTERS FOR VARIOUS POLARIZATIONS - TRANSMITTING OR RECEIVING MODES

TRANSMITTING POLARIZATION	PHASE OF RADIATED WAVE AT ANTENNA 2 WITH RESPECT TO ANTENNA 1	CIRCUIT CONDITION 90° PHASE SHIFTER	CIRCUIT CONDITION 180° PHASE SHIFTER
Vertical	In-Phase	IN	OUT
Horizontal	180° out of phase	IN	IN
RHCP*	Lags 90°	OUT	OUT
LHCP	Leads 90°	OUT	IN

RECEIVING POLARIZATION	PHASE OF RECEIVED WAVE AT ANTENNA 2 WITH RESPECT TO ANTENNA 1	CIRCUIT CONDITION 90° PHASE SHIFTER	CIRCUIT CONDITION 180° PHASE SHIFTER
Vertical	In-Phase	IN	IN
Horizontal	180° out of phase	IN	OUT
RHCP	Leads 90°	OUT	IN
LHCP	Lags 90°	OUT	OUT

*For an observer looking in the direction of propagation, the rotation of the electric vector in a transverse plane is clockwise for right-hand polarization; a counter clockwise rotation would be left-hand polarization.

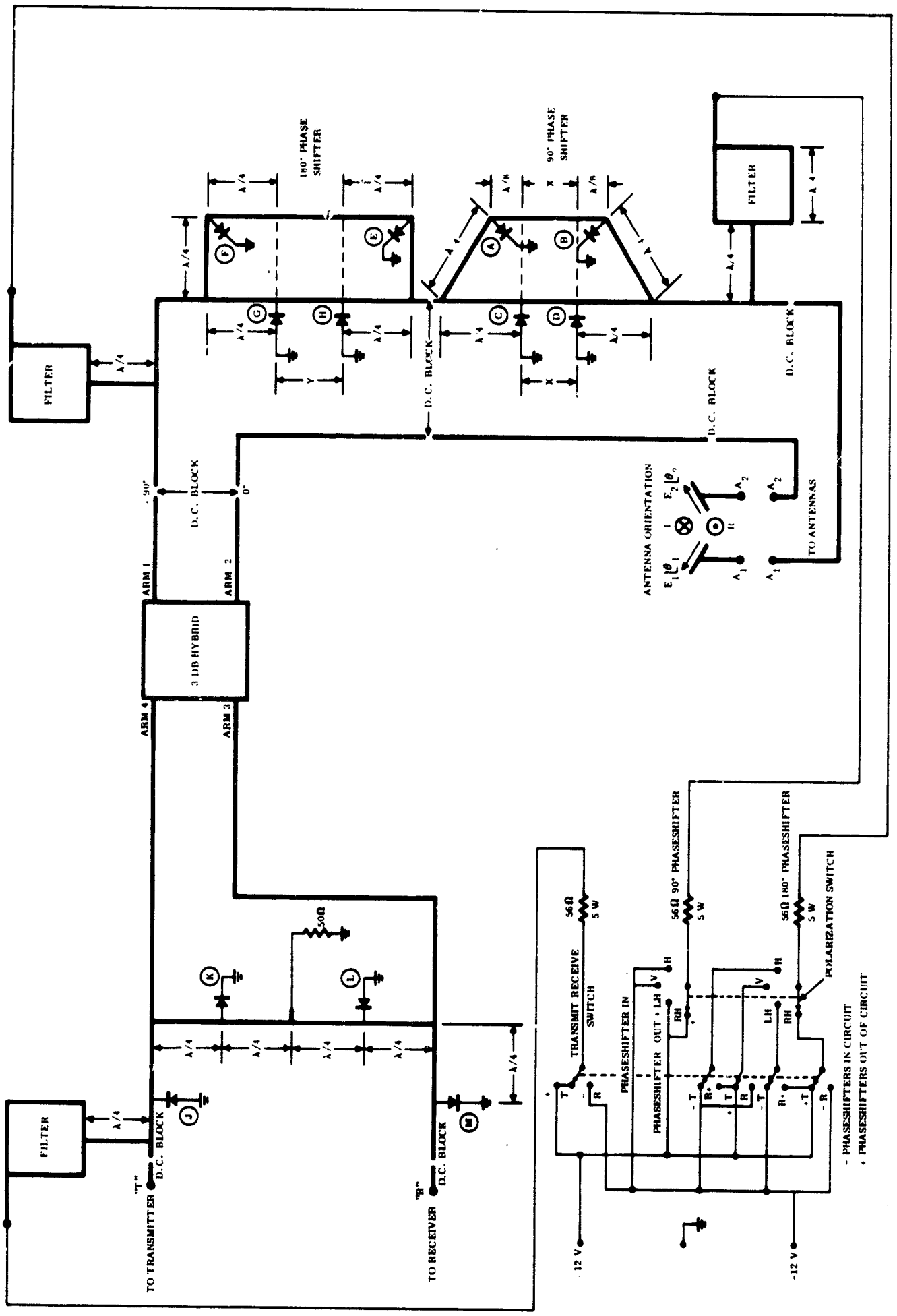


Figure 71 Schematic Diagram, Polarization Control and T/R Switch

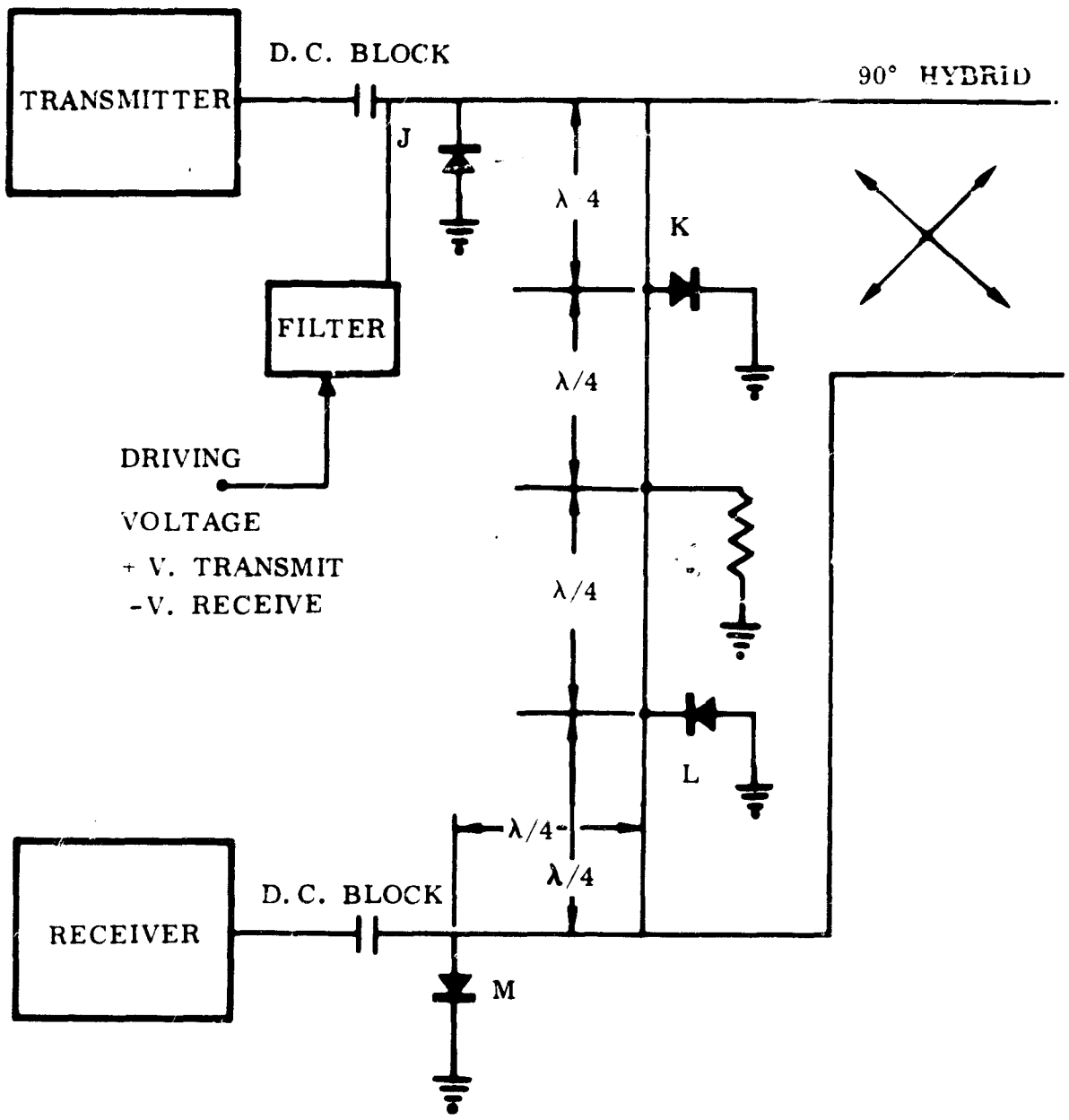


Figure 72 Simplified Schematic Diagram of T/R Switch

package and internally matched for a 50 ohm stripline. By applying a positive dc voltage, diodes J and L are reversed biased, and diodes K and M are forward biased. When this occurs, the transmitter is electrically connected to the hybrid and, in turn, to the antenna terminals. At the same time the receiver is disconnected from the hybrid. When a negative voltage is applied, the reverse action takes place; the receiver is connected to the hybrid, and the transmitter disconnected. In either state the arm of the hybrid which is disconnected from receiver or transmitter is automatically terminated in a 50 ohm load.

The 180° and 90° phase shifter were made in stripline and design concepts are illustrated in the overall schematic. The same types of diodes are used, as for the TR switch, and the operation of the diodes is similar to that of the TR switch. To obtain 180° phase shift an additional half-wave length of transmission line is added to the path from arm 1 of the hybrid to terminal A2. A 90° phase shift is obtained by switching in an additional quarter wavelength of line. The 180° and 90° phase delays are introduced in the transmission line by applying a negative voltage to the phase shifters.

Positive voltages remove the phase shifter by forward biasing diodes F, E, A and B and reverse biasing diodes G, H, C and D. Bias voltages are introduced via stripline filters which prevent the escape of any RF energy from the transmission paths, by way of the bias leads. The filters consist of two quarter wavelengths of line in series connection. The line closest to the main transmission path is made to have a very high impedance through its narrow width and as a result of the transforming, the low impedance filter section is one-quarter of a wavelength away.

DC blocks are used to isolate the bias voltages from one section to another. The dc blocks chosen for the polarization control and TR switch were 500 pf ceramic chip capacitors, type ULA 102, manufactured by Aerovox.

The overall schematic diagram shows the logic circuitry necessary to achieve the various antenna polarizations for transmitting and receiving modes. The individual components such as the TR switch and phase shifters were assembled separately and joined together by coaxial cables. The hardware built up for the polarization control and TR switch is shown in Figure 73. In the illustration, the transmitting and receiver terminals R and T and antenna terminals A2 and A1 may be seen as well as the hybrid and phase shifters. The switching box is also illustrated.

The breadboard circuitry was tested by measuring VSWR at the inputs to each port (R, T, A2 and A1), insertion loss from R to A2 and A1 and T to A2 and A1. The relative phases and amplitudes of the wave appearing at the output ports was also measured. The results of these measurements are shown in Table VII.

5.3 TEST RESULTS

The test data shows that the total insertion loss in the path from transmitter and receiver to the sum of the outputs at A1 and A2 amounted to 3.75 and 2.94 db, respectively. This loss is due to losses in the diodes which amount to about 0.5 db each. Since there are two diodes per component (TR switch, 90° and 180° phase shifters) always in a forward bias state, each component would have a loss of about 1 db. Hence, the three components will amount to nearly 3 db. Because of the method of assembly, each circuit could be tested separately and the component test data verified the losses of the assembled circuits. During component testing of the phase shifters, line lengths in the phase shifters were adjusted, reducing phase errors to less than 5°. The results of the phase tests on the completed polarization control circuit showed a maximum of 5° error.

As can be seen in Table VII, the paths T to A1 and R to A1 had greater insertion loss than the T to A2 and R to A2 paths. This unbalance could be relieved by placing the 180° phase shifter in the A2 path. This would

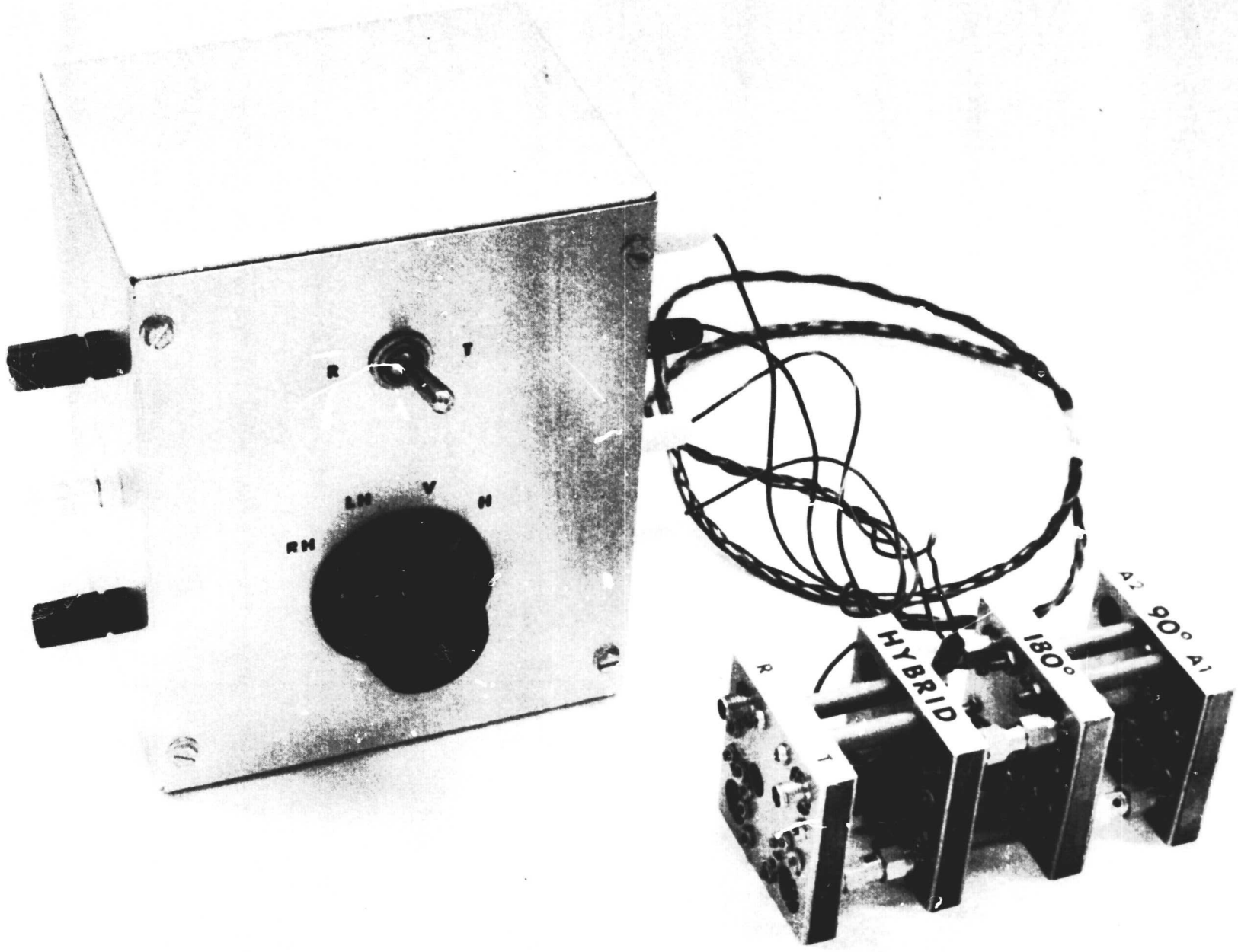


Figure 73 T/R Switch and Polarization Control Hardware

TABLE VII. POLARIZATION CONTROL AND TR SWITCH DATA

F = 5,750 GHz

SWITCH POSITIONS		VSWR				INSERTION LOSS IN DB				PHASE AT A2 IF	AXIAL RATIO
		A1	A2	T	R	T A1	T A2	R A1	R A2	A1 = 0°	
T	V	1.12	1.80	1.75		-7.6	-6.2			+3°	
T	H	1.10	1.82	1.69		-7.9	-6.5			+175°	
T	RH	1.10	1.86	1.80		-7.0	-6.0			-85°	.89
T	LH	1.16	1.80	1.75		-7.3	-6.2			+90°	.88
R	V	1.06	2.0		1.46			-7.8	-4.5	-4°	
R	H	1.03	2.0		1.54			-7.8	-4.7	-175°	
R	RH	1.13	2.0		1.56			-7.6	-4.7	-95°	.72
R	LH	1.08	2.0		1.61			-7.5	-4.9	+85°	.74

Isolation: Port "T" to Port "R" -40 db

Average Loss	-7.4	-6.2	-7.7	-4.7
Combining in space		-3.75 db		-2.94 db

require a modification to the phase shifter design but no change in the switching logic. The changes could be accomplished in a straightforward manner. The improved balance would help to improve the axial ratios which were .89 for transmitting and .73 in the receive mode.

5.4 CONCLUSIONS

The polarization control and TR switch developed and fabricated in a breadboard configuration showed that a multipolarization antenna can be achieved. In addition, by applying standard design approaches, a TR switch demonstrated 40 db isolation between receiver and transmitter. Although high speed switching was not tested on the breadboard, the diodes selected should provide switching times as short as 100 nanoseconds. Power handling capacity is limited by the diode dissipation which is 2.5 watts. With an insertion loss of 0.5 db across the diode then a total power handling of about 20 watts could be expected.

The breadboard assembly design demonstrated good performance or capability with respect to power handling, switch speed, isolation, and polarization capability. The insertion losses observed, however, would tend to discourage the incorporation of polarization control circuit in a practical system since 2 db or more of the transmitter power would be lost. In addition, the same losses in the receive path would severly penalize receiver noise figure. It is doubtful if the losses could be reduced to below 1 db which would be about the maximum allowed in a system designer's attenuation budget. Therefore, one should consider seriously the need for more than one antenna polarization. If satisfactory system results could be obtained with only one polarization, then the 1 db budget could be applied to the TR switch. The TR switch design employed in the breadboard model could easily meet a 1 db insertion loss requirement and provide 40 db or higher isolation between transmitter or receiver.

SECTION 6

TECHNICAL DISCUSSION - HIGH POWER ELEMENT DEVELOPMENT

This discussion presents Ryan effort in developing the use of the Limited Space-Charge Accumulation (LSA) device. The LSA shows great promise in generating extremely high peak powers from C to Ka Band.

The goals of the development effort were to demonstrate injection locking of an LSA diode. This goal was achieved and a peak power output of 50 watts was obtained at 7.8 GHz. These results confirmed the design approach, and accordingly, the design of a high power source using LSA is based upon the block diagram of Figure 74. The design of the receiver portion of the module would be similar to that discussed in Paragraph 2.5, wherein microwave integrated circuitry was proposed. The transmitter portion would contain a phase controlled SRD multiplier as the phase shifter and injection locking stage in a two-stage power source. The size of the module for phased array application is related to frequency in that module cross sections must be less than $\lambda/2$ on each side. Thus, at 7.8 GHz the module cross section would be 0.75 x 0.75 inch. The estimated overall length would be about 5 inches, which would include the two stages of injection locked oscillators. The total weight of the module would amount to an estimated 0.3 pound, exclusive of interconnecting stages

The subsequent paragraphs describe the work performed at Ryan on the development of an ejection locked, LSA power source having the output phase controlled by an SRD multiplier.

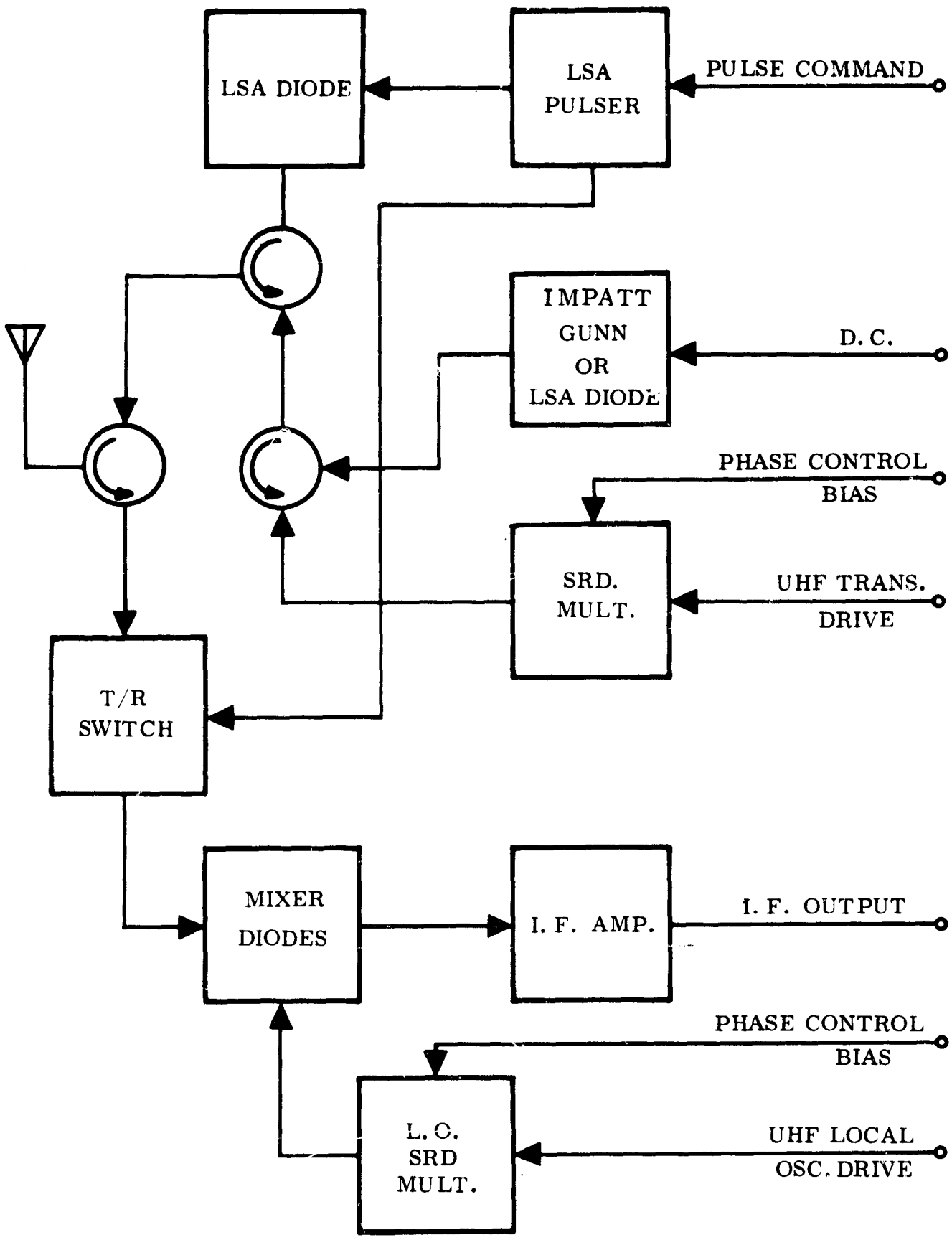


Figure 74 Block Diagram, High Power T/R Module

6.1 INTRODUCTION TO LSA DEVICE PROGRESS

The search for solid state microwave power sources has produced a wide variety of oscillators including the tunnel diode, Gunn effect device, avalance diode, IMPATT and LSA devices. Among these, the LSA device has provided the highest peak power output. Units delivering 500 watt pulses in X-band are available in 1N23 type package and units delivering 1200 watts peak power have been demonstrated by Cayuga Associates.

A new mode of operation for bulk negative resistance devices was described by J. A. Copeland of Bell Telephone Laboratories in October 1966.[1] The characteristics of the LSA were enumerated by Copeland as, "(1) the frequency of operation is higher than the reciprocal of the carrier transit time, (2) The frequency of oscillation is determined by the frequency of the circuit, and (3) The power output and efficiency are equal to or higher than when the same device is operated in the transit time frequency mode described by Gunn and others, or in the quenched domain mode described by Carroll."

To produce operation in the LSA mode, the ratio of crystal-doping level to operating frequency must lie within a certain range, and the swing of the RF voltage across the device must be large enough to dip below the threshold voltage for part of each cycle.

Several semiconductors are known to exhibit a negative differential resistance when biased above their individual threshold electric fields, (GaAs is the most widely studied), and it is this property which makes possible bulk negative-resistance oscillators. Figure 75 is a graph of the carrier drift velocity versus applied electric field.[2] The behavior of the semiconductor up to the vicinity of the peak or threshold is similar to a linear positive resistance. To the right of the threshold lies the power generating, or negative resistance region.

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[1]J. A. Copeland, "A New Mode of Operation for Bulk Negative Resistance Oscillators," Proc. IEEE, Vol. 54, October 1966, pp 1479-1480.

[2]J. A. Copeland, "LSA Oscillator-diode Theory, J", Appl. Phys., Vol. 38, Aug. 1967 pp. 3096-3101.

In addition to generating power, the negative resistance region tends to be unstable within the semiconductor. When the applied electric field is above the threshold, space charge fluctuations begin to grow, causing appreciable distortion of the electric field within the semiconductor. The result is lower device efficiency because all regions of the semiconductor do not contribute energy to the RF output.

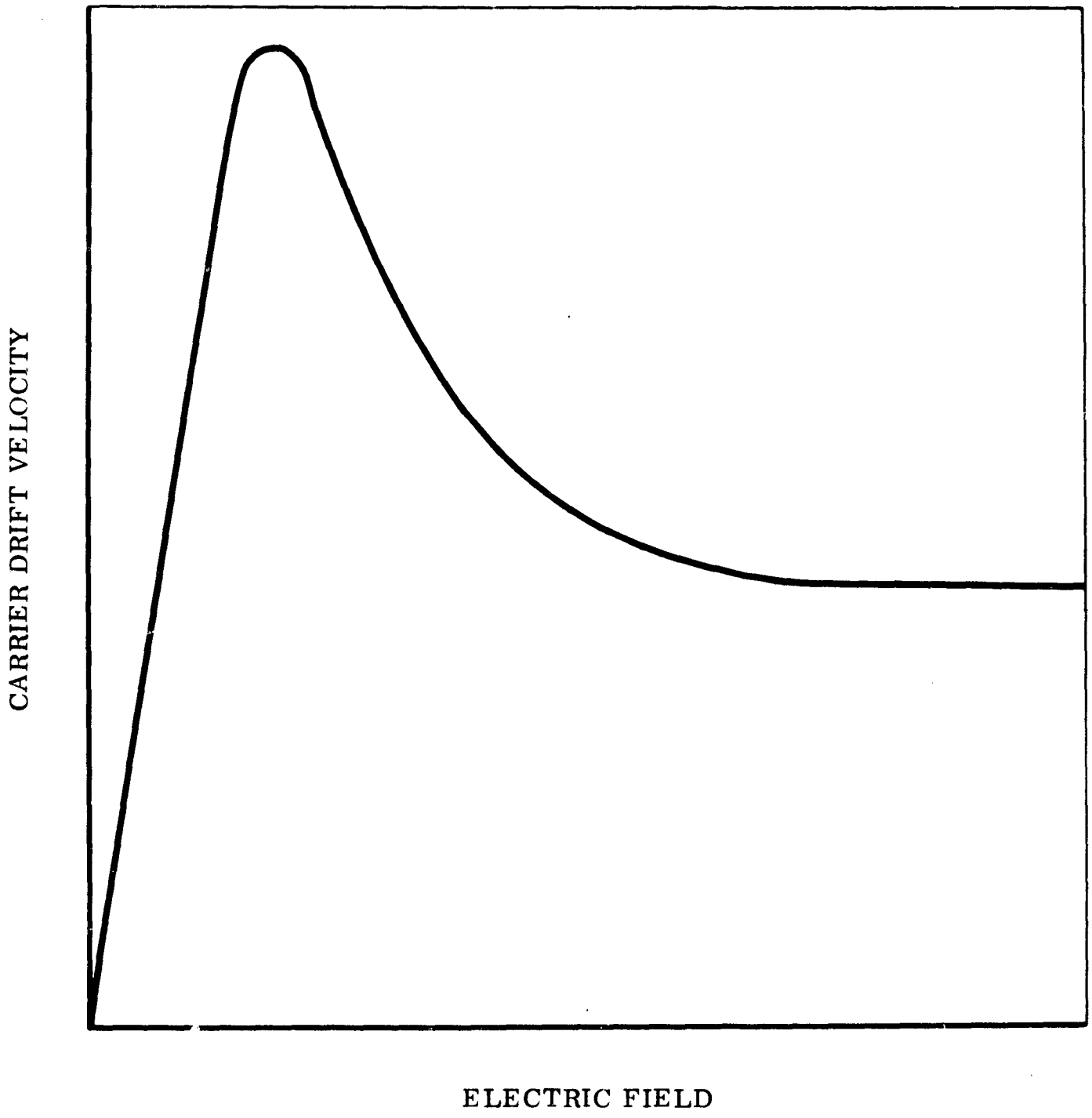

Figure 75 Carrier Drift Velocity vs Electric Field Strength

The growth of the space charge, when the electric field is above the threshold, must be cancelled by a decay of space charge when the electric field is below the threshold during part of each cycle. This prevents space charge accumulation over many cycles. This requirements can be satisfied[1] if the ratio of doping to frequency of operation (h) is

$$2 \times 10^4 < h < 2 \times 10^5 \text{ sec. cm}^2$$

The LSA is a large signal mode[2] which means that LSA oscillations do not build up from small perturbations similar to other oscillations. The LSA device requires a very fast rise time, (one nanosecond or less), to initiate the LSA mode of operation. Failure to initiate the LSA mode results in rapid device failure. Therefore, a high quality modulator must be available before the advantages of the LSA can be realized.

6.2 LSA OPERATIONS

Initially Ryan successfully operated an X-band LSA device in early December 1967. Preliminary observations were made of operating characteristics and circuit requirements. Several C-band devices have now been operated. Figure 76 shows the I-V characteristics of a typical LSA device. Notice the correspondence to Figure 75. In Figure 76, curve A is the linear positive resistance or low-field region, and Curve C corresponds to the nearly constant high-field carrier drift velocity. Curve B shows the modulator load line. Threshold voltage for this sample is 130 volts. Oscillations can be generated only on Curve C. A modulator was used which consisted of a mercury-wetted reed relay, discharging a transmission line. The basic test arrangement is shown in Figure 77. Peak output powers of the devices operated vary from 40 to 50 watts. This power has been measured with a calibrated detector as shown in Figure 77. Operating frequencies have been at high C-Band, 7.8 to 7.9 GHz.

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[1]J. A. Copeland; LSA Oscillator-diode Theory, "J. Appl. Phys., Vol. 38, Aug. 1967 pp. 3096-3101.

[2]W. R. Day, "Stabilization of Microwave Oscillators by Injection Phase Locking", The Microwave Journal, March 1967, pp. 35-39

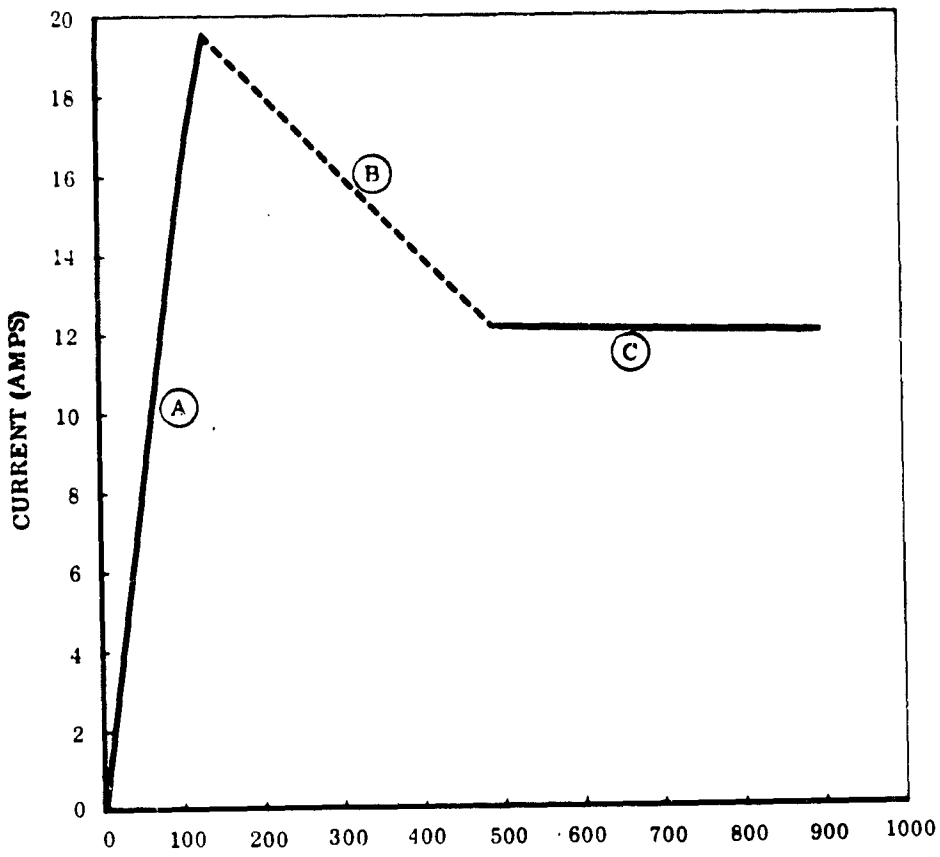

Figure 76 I-V Characteristics of LSA-111

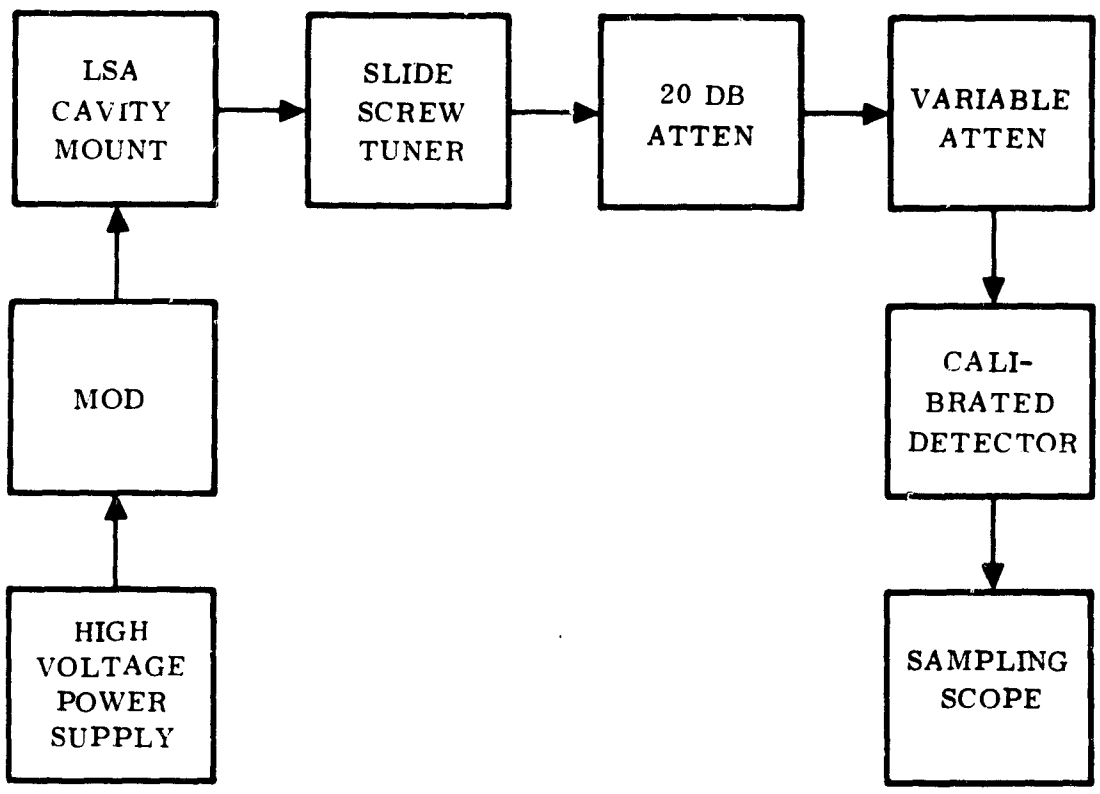

Figure 77 LSA Test Arrangement

6.3.1 Laboratory Type Modulator

As a first objective, a laboratory-type, solid-state modulator was designed. The motivating purposes were to provide a modulator which could be used for gathering detailed information about the system aspects of LSA operation without the penalty of miniaturization, and to provide for gathering detailed information about the system aspects of LSA operation without the penalty of miniaturization, and to provide insight into the more difficult and final problem of miniaturization.

Avalanche operation of transistors was investigated as a means for providing the very fast and high voltage pulses required. Several progressively larger output breadboards were constructed leading up to the present modulator.

Two different type modulators were considered. Each type used the avalanche mode in transistors for switching, but one used a delay line, and the other used a step recovery diode for pulse length control.

The delay line type modulator offered a relatively simple circuit which could be rapidly developed, while the storage diode type could be made more efficient and smaller.

The present delay line type modulator can produce up to 800 volt pulses (into a 50 ohm load) 20 nanoseconds wide with a rise time of 1.6 nanoseconds. Fall time is 4 nanoseconds, and "backporch" is 15%. The pulse repetition rate can be adjusted to any value between 265 and 1000 per second. This range can be extended in either direction by changing one component. The output waveform of this modulator is shown in Figure 78.

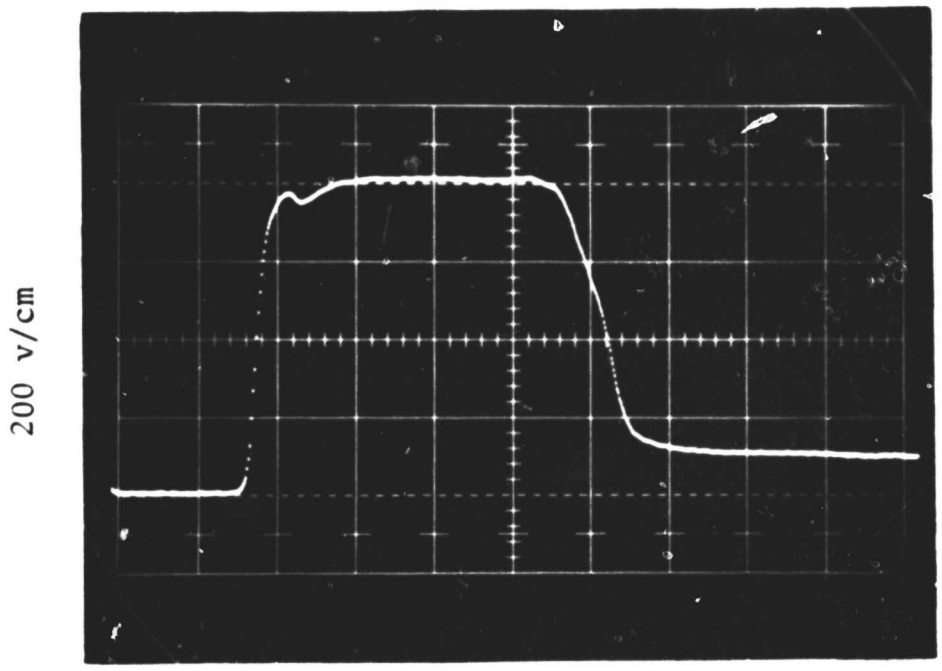

Figure 78 Typical Modulator Waveform

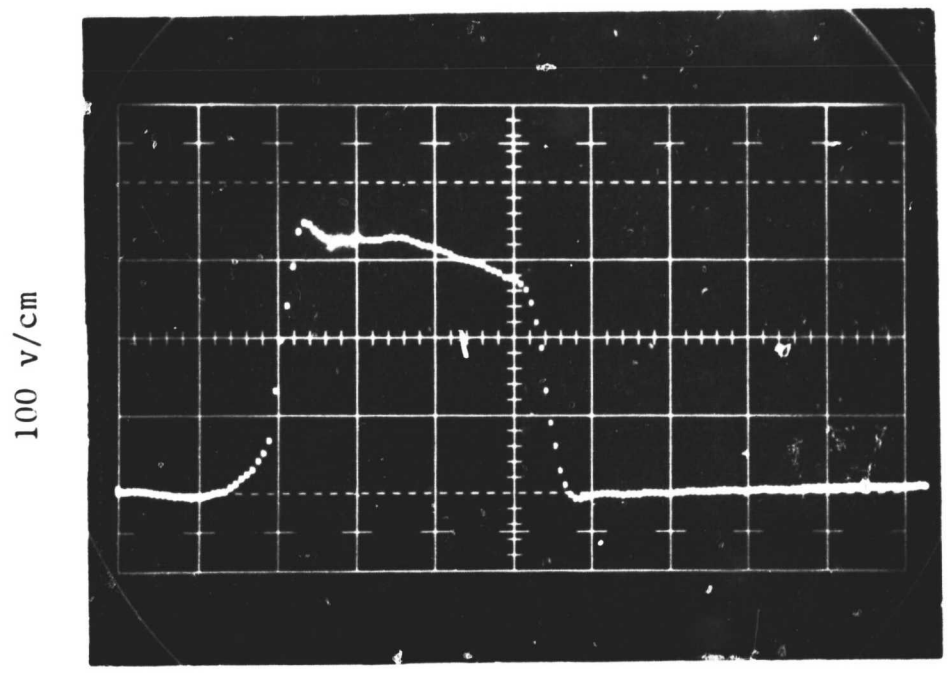

Figure 79 Experimental Modulator Waveform

6.3.2 Array-Sized Modulator

Based on the work accomplised on the laboratory-type modulators, it should be possible to construct a delay line type modulator in less volume than a cubic inch, which will deliver 450 volts by 20 nanosecond pulses into 50 ohms. The success of designing a modulator into a cubic inch or less would depend on designing a compact stripline delay line, and possibly assembling the transistors by hybrid-chip circuit techniques.

An even smaller volume and more efficient modulator could result from the development of the step recovery diode approach. Experimental versions, (operated into 50 ohms), have produced as much as 300 volt pulses, 15 nanoseconds wide, with rise and fall times of 1 to 2 nanoseconds, (see Figure 79). Progress with this technique will be geared closely to development of suitable storage diodes and fast recovery rectifiers. The circuit design is more involved for this type modulator, but one may obtain greater pulse length for a given volume.

It is possible that one modulator could power more than one LSA oscillator, thereby relieving the miniaturization problem at the expense of increasing modulator output power.

It should be noted here that this development effort was accomplished during the summer and fall of 1968. This development, as described, was accomplished with bulk type LSA devices.

Cayuga, Associates is presently developing a new line of epitaxial LSA's. Numerous benefits will be offered by this new line. These benefits include:

- Anticipated efficiency - -15%
- Pulse width - 0.45 microsecond
- One power dissipation - 0.5 watt
- Rise time requirements - The rapid rise-time requirements are relaxed.

The stringent modulator design will therefore be alleviated by this new line of LSA's and the average power per unit is of the magnitude as required for pulse radar application. Consequently, it is believed that the LSA has great potential for future solid state, phased array radars.

6.4 INJECTION LOCKING

Phase control of radiation from each element in the matrix of an "integrated antenna" is necessary. The possibility of controlling the phase of the LSA oscillator output has been studied.

The phase locking of an oscillator by an injected reference signal has been treated by a number of authors. Both locked and unlocked, CW and pulsed operation have been studied.[1], [2], [3], [4] It has been found that phase locking can be attained when the injected signal power is considerably below that of the oscillator, and locking can be maintained over a significant bandwidth. Under appropriate conditions, the oscillator behaves like an amplifier, and is capable of reproducing frequency and phase modulated signals.

Adler[2] has shown that, subject to certain restrictions, the time derivative of the phase difference between the injected signal and the oscillator output is,

$$\frac{d\alpha}{dt} = -B \sin \alpha + \Delta\omega_o \qquad (1)$$

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[1]F. M. Magalhaes and W. O. Schlosser, "Synchronization of Pulsed Oscillators", Proc. IEEE, April 1968, pp. 766-768.

[2]R. Adler, "A Study of Locking Phenomena in Oscillators", Proc. IRE, Vol. 34, June 1946, pp. 351-357.

[3]R. C. Mackey, "Injection Locking of Klystron Oscillators", IRE Trans-MTT, July 1962, pp. 228-235.

[4]W. R. Day, "Stabilization of Microwave Oscillators by Injection Phase Locking", The Microwave Journal, March 1967, pp. 35-39.

where

$\Delta\omega_o$ = $\omega_o - \omega_1$

ω_o = free-running oscillator frequency

ω_1 = frequency of injected signal

α = phase difference between the injected signal and oscillator output

B = $E_1/E \cdot \omega_o/2Q$

E = oscillator output voltage

E_1 = injection signal voltage

Q = figure of merit of loaded resonator

The conditions for synchornization of the oscillator to the injected signal result when $d\alpha/dt = 0$; then equation (1) reduces to

$$\sin \alpha = 2Q \frac{\Delta\omega_o}{\omega_o} \cdot \frac{E}{E_1} \tag{2}$$

Since sin α must be equal to or less than unity, the stability condition can be written, according to Mackey,[1] as

$$\left[\frac{2Q\ \Delta f_o}{f_o} \left(\frac{P}{P_1}\right)^{1/2}\right] < 1 \tag{3}$$

Mackey was able to verify the usefulness of equation (3) with tests on several X-band reflex klystrons.

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[1]R. C. Mackey, "Injection Locking of Klystron Oscillators", IRE Trans-MTT, July 1962, pp. 228-235.

Equations (2) and (3) can be rewritten and converted into a convenient nomogram, per Figure 80. The solution to equation (3) results by taking $\alpha = 90°$. Setting α equal to other values gives a solution to equation (2). Equation (2) is interesting because it allows calculation of the phase difference between the injected signal and oscillator output signal when the fractional frequency shift is known.

Day[1] has slightly modified Adler's theory and developed a relation useful in predicting the locking bandwidth of two-cavity klystrons. He also reports of phase locking of a Backward Wave Oscillator (BWO) and cites work done with magnetrons, bulk GaAs, read diode and tunnel diode oscillators.

A useful analysis of pulsed phase locked oscillators is given by F.M Magalhaes and W. O. Schlosser.[2] Reference is made to the frequency and time domain behavior as a criterion for distinguishing locked from unlocked operation. Results are given for the case of a pulsed avalanche diode oscillator locked to a CW-operated klystron. Their conclusions is that the pulsed behavior of locked and unlocked oscillators can be predicted with a slight modification to the CW theory of Stover.[3]

Injection phase locking of an LSA device has been demonstrated by Eastman.[4] His results are shown in Figure 81. Figure 82 represents a basic setup for obtaining locking performance data in accordance with Magalhaes and Schlosser. Eastman's data departs from theory, particularly in the region of low injection gain. However, two facts should be emphasized. First, the theory is valid only when the injected signal is small in comparison to the oscillator output (approximately 15 to 20 db locking gain or more); secondly, these results are only preliminary.

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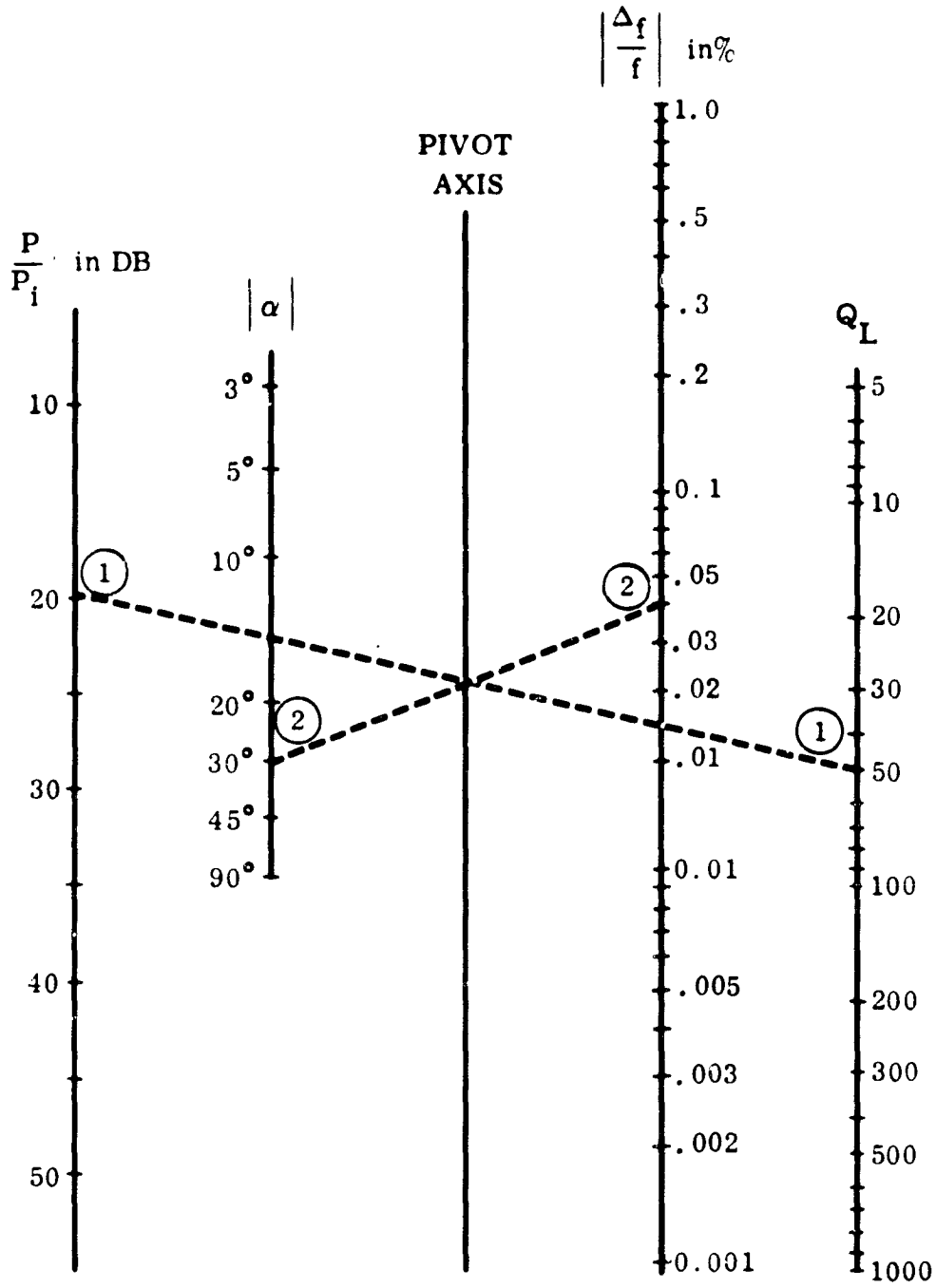
[1]W. R. Day, "Stabilization of Microwave Oscillators by Injection Phase Locking", The Microwave Journal, March 1967, pp. 35-39

[2]F. M. Magalhaes and W. O. Schlosser, "Synchronization of Pulsed Oscillators", Proc. IEEE, April 1968, pp. 766-768.

[3]H. L. Stover, "Theoretical Explanations for the Output Spectra of Unlocked Driven Oscillators", Proc. IEEE (letters), Vol. 54, Feb. 1966, pp. 310-311.

[4]L. F. Eastman, described in a letter to T. R. Mayberry of Ryan Aeronautical Company.



$\frac{P}{P_i}$ = Ratio of oscillator power output to injection signal input

α = Phase angle between oscillator and injection signal

$\frac{\Delta_f}{f}$ = Ratio of capture range to free running frequency

Q_L = Loaded figure of merit of resonator

Figure 80 Nomogram of Injection Locking

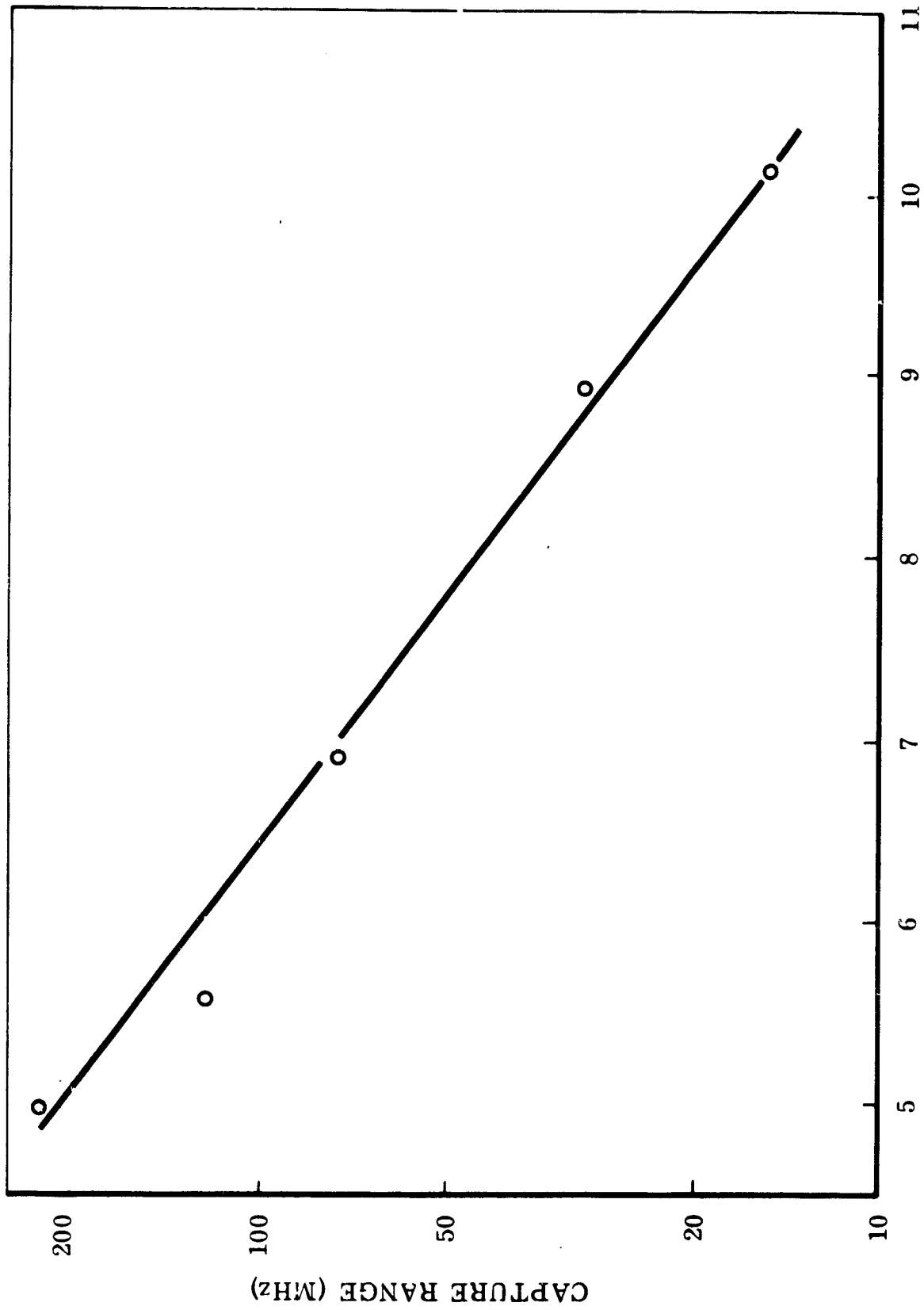


Figure 81 LSA Injection Locking Performance
(Reproduced from data supplied by Cayuga Associates)

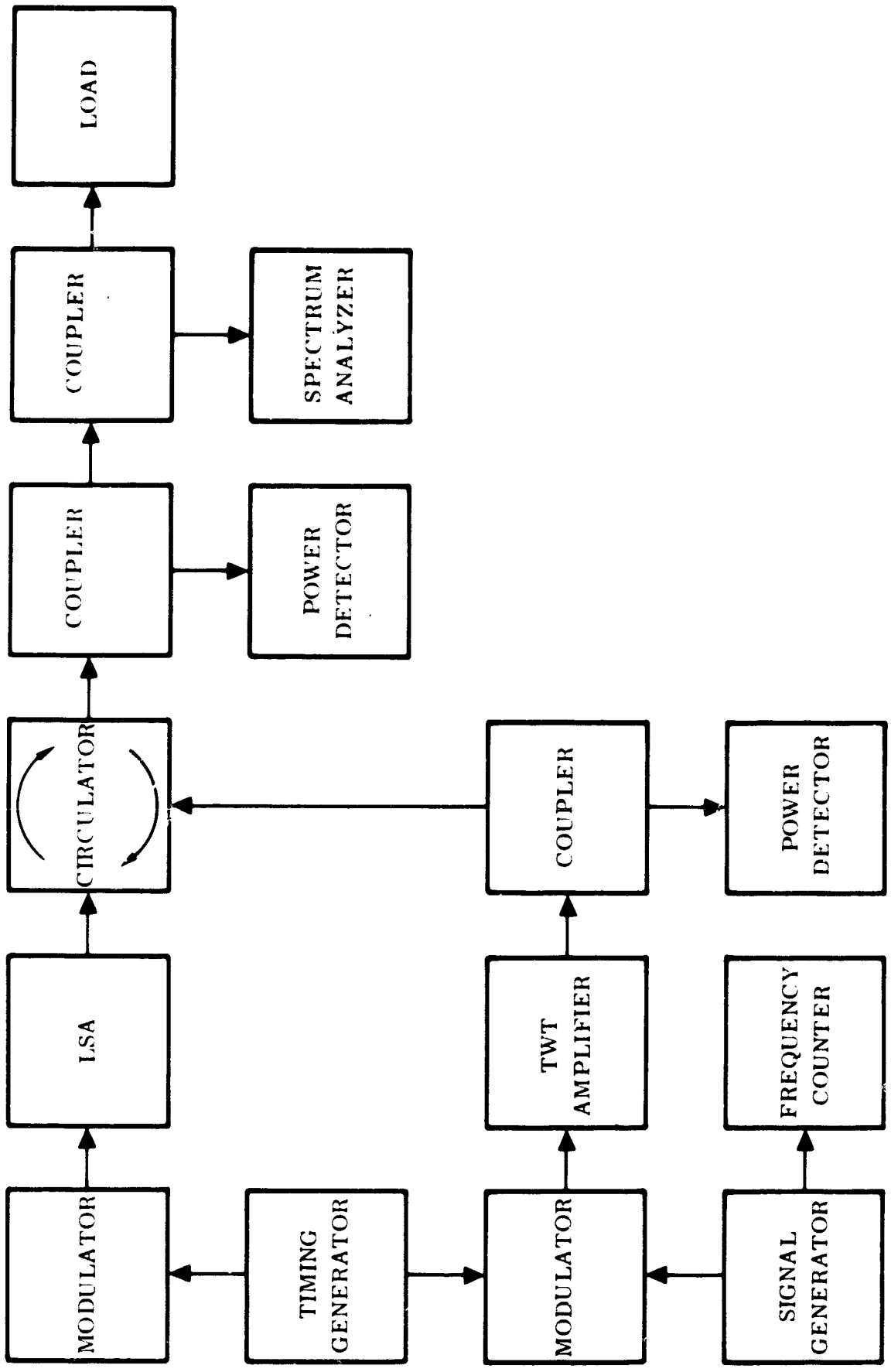


Figure 82 Locking Performance Block Diagram