PROCESS TECHNIQUES STUDY OF INTEGRATED CIRCUITS INTERIM SCIENTIFIC REPORT NO. 2

By
J.V. Brandewie and P.H. Eisenberg

June 1969

Prepared under Contract No. NAS 12-4 by
NORTH AMERICAN ROCKWELL CORPORATION
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CONTENTS

CONTENTS (Cont)

ILLUSTRATIONS

TABLES

INTRODUCTION

This Second Interim Scientific Report prepared under NASA Contract No. NAS 12-4 describes the program effort for the period May 1968 to February 1969. The objectives of this effort were to discover why structural defects are produced in thermally grown oxides and to learn how they may be prevented. In order to reach these objectives it was first necessary to develop a tool (described in Appendix A) for the reliable location and identification of oxide defects. This technique was then successfully utilized to isolate those process and structural considerations which contribute significantly to increased defect densities. Early program results confirmed that the inherent thermal mismatch between silicon and silicon dioxide was a significant cause of oxide defects and provided a lower limit of defects which could not be reduced by processing changes. It was later determined that one of the most critical process related factors is the initial condition of the silicon surface in terms of cleanliness and smoothness. As a result, an improved surface preparation technique was developed which significantly reduced defect densities. At least two major semiconductor manufacturers are presently using the defect detection technique developed on this program.

One of the most frustrating and widespread problems in planar technology is that caused by dielectric defects, or "pinholes," in oxide layers. The characteristic failure mode introduced by oxide defects is an electrical discharge through the defect from an overlying metallization to the substrate. The metallization need not fill the hole for failure to occur; plasma breakdown can occur in the intervening space. In the case of very small diameter holes, the discharge current may not be large enough initially to constitute a failure. But redistribution of metallization throughout the hole as a result of prolonged plasma discharge ultimately may create a much more highly conductive path and a clearly defined failure. This supports the fact that not all pinhole failures are recognized as such at initial burn-in or early systems test stages but show up later as long term effects in the field. The importance of eliminating this processing problem is clearly evident, not only for high reliability guidance systems, but also for increasing component yields, particularly in the case of LSI and MOSFET gate oxides.

Although numerous remedial innovations in materials and process techniques have been attempted, no reliable solution to this problem has yet been found. Because of the general convenience and superiority of thermally grown oxides for most masking and passivating purposes, and because this application of silicon dioxide has been successfully optimized in most other respects, it seems important to take full advantage of these characteristics by determining the process requirements needed to remove this remaining major problem in its use.

Initial activity on this program sought to relate the origin of dielectric defects to various process factors and structural considerations. These results may be summarized as follows:

1. Factors tending to increase dielectric defects.

    a. Extended processing (generally)

    b. Higher compressive stress in the oxide

c. Embedded lapping grains in the substrate

d. Superficial HF etching

e. Abrupt oxide steps

f. Thermal cycling

g. Mechanical wiping

h. Removal of back oxide layers

2. Factors tending to decrease dielectric defects.

a. Growth of oxide to higher thicknesses

b. Chemical etch of initial wafer

c. Pyrolytic oxide, uniformly applied and properly densified

d. Additives tending to reduce bond strain in silica glass

e. Addition of steam to oxidation process gas

The results noted above are consistent with a compressive stress model as the principle source of dielectric defects in oxide layers. The compressive stress in the oxide layer is introduced during cooling from the oxidation temperature as a result of an approximately tenfold mismatch in thermal expansion coefficients between substrate and dielectric. This model was confirmed in a number of subsequent experimental observations. Replicate electron microscopy of a known defect revealed oxide outcroppings suggestive of a compressive stress relief process. Measurements of the compressive stress gave values of the order of 4×10^4 psi. Quantitative comparison of oxide defect densities before and after cooling to room temperature demonstrated that the bulk of the defects (90 to 98 percent) were introduced during the cooling process. Removal of one oxide layer from a wafer introduced a significant warping of the wafer which resulted in an increase in the measured defect population in the remaining oxide layer.

A tool developed on this program for locating and identifying oxide defects is based on a functional test originated by James Lytle of Westinghouse. This test, known as "Electrophoretic Decoration," is particularly applicable to wafers in the beginning stages of manufacture. The test utilizes the oxidation of a metal anode to form positively charged colloidal particles which are propelled through an organic electrolyte toward cathodic sites on an oxide coated silicon wafer situated below the anode. The accumulation and discharge of the colloidal salt particles around oxide defect sites occurs as a result of electron transfer through the defects from the negatively charged silicon wafer. Thus the functional mode of the test is identified with the failure mode sought. The accumulated insoluble matter surrounding each defect serves as a many-fold magnification of the defect location which, for documentary purposes, is readily photographed at low magnifcation. (A detailed description of the test developed is given in Appendix A.)

The following report indicates that this technique has been used successfully on two kinds of investigations. The first investigation is an evaluation of oxides from various sources for silicon wafer lots oxidized to 10,000 Å by three different processors. The second investigation assesses the effect of various wafer pretreatments, reflecting various methods of preparing the wafer prior to oxidation and yielding thereby essential process control information.

Appendixes B, C, and D have been repeated from Interim Scientific Report No. 1 as a convenience to the reader for reference purposes.

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SUMMARY

Several experiments were conducted to more clearly define the origin of oxide defects in terms of processes and to ascertain the dependence of oxide defects on various process steps. Figure 1 is a summary of the results obtained, indicating the defect decay curves as a function of oxide thickness for four basic processes. Curve A represents initial wafer treatments as grown early in the program. Curves B and C are subsequent improvements in terms of reduced oxide defects (at low thicknesses) vs wafer surface pretreatments. From these mechanistic studies it was postulated that the primary local cause of dielectric defects is physical promontories in the silicon substrate which result in stress concentrations on the grown oxide after cooling to room temperature. The shear component of these stresses is believed to result in the defect occurrence at these sites. A recommended optimum oxide growth process for minimizing dielectric defect densities in thin oxide regions was defined. Utilization devices especially with the advent of thin MOS capacitor regions.

A series of wafers were obtained from three different vendors for comparison purposes. The defects are indicated in the graph at the 10,000 A level. It is believed that the superiority of vendor A is due to the utilization of a wafer pretreatment similar to that developed on curve C (HCl vapor etch).

A special program was also performed to test the developed wafer pretreatment in an actual pilot line operation. The standard pilot line process was compared with two process modifications. The effect of wafer pretreatment on the final oxide integrity was also evaluated. The data obtained at two oxide thicknesses (1400 and 14,000 Å) using a test pattern are also shown in Figure 1. The 14,000 Å data is obviously much higher than any of the other results obtained when extrapolated to comparable thicknesses. These data are comparable, it is felt, since the oxide has been through several thermal cycles which will cause additional defects as determined previously on this program.

The 1400 Å thickness, however, is a regrown area and has seen fewer thermal excursions. These data appear to be comparable with the vendor oxide data except for Vendor A, which is clearly superior. (In this comparison it is necessary to extrapolate using the same decay constant as either curve B or C.)

Further experiments are recommended to implement the developed process modifications on actual production devices. Also other reliability testing is needed to ensure that other problems are not introduced as a result of the changes made.

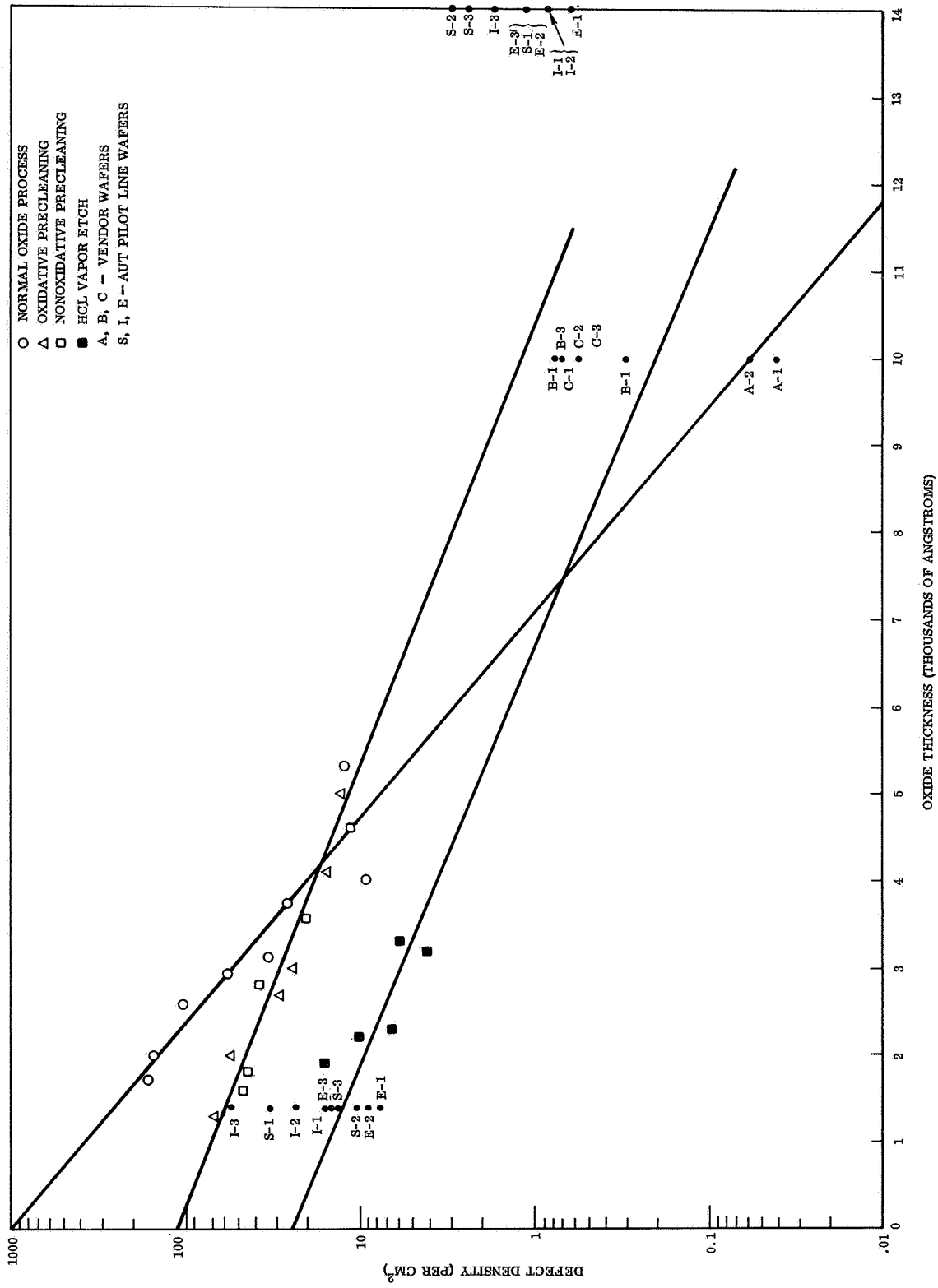

Figure 1. Oxide Defect Dependence on Processing

MECHANISM RESEARCH

A series of experiments were conducted in an attempt to determine the mechanism and thus the origin of oxide dielectric defects. As previously discussed, tests conducted in this laboratory and confirmed by other work established beyond reasonable doubt that the origin of physical forces were due to the thermal mismatch compressive stress in the coated oxide. However, no direct indication of the local factors contributing to their formation was known.

Effects of Oxide Thickness and Stress

Additional experiments were undertaken to examine in detail the kinetics of the oxidation process. Investigations were conducted to compare defect densities at no stress (before cooling), at full stress (after cooling), and at partial stress relief (after removal of the back oxide layer). These data are listed in Table I Appendix A), and Figure 2 for a series of oxide thicknesses. Conventional oxide growth technique was used (N_2:245 cc/min; O_2:245 cc/min passed through water at slightly less than 100 C; temperature: 1180 C) followed by HCℓ-He etching before removal from the growth zone. Defect densities were evaluated by standard etch pit and decoration counts. The exponential decrease in the number of defects with oxide growth is apparent from Figure 2. Decay of this number, N, may be expressed in terms of layer thickness

$$N = N_z e^{-\phi z} \tag{1}$$

where N_Z is the preexponential factor (ordinate intercept) and ϕ is the decay factor. Decay factors appropriate to Figure 2 are 2.22, 1.08 and 0.83 respectively for no stress, full stress, and partial stress.

The decay factors followed an exponential law and were largest prior to wafer cooling (unstressed condition) and smallest after warping the wafer by removal of one oxide layer. The general nature of these results indicated the existence of latent defects in the oxide prior to cooling which were progressively strengthened and rendered less vulnerable to rupture as oxide thickness was increased. The assumed presence of such latent defects, however, implied the existence of structural or distributional irregularities in the oxide-substrate system introduced either before or during the oxidation process.

The existence of a virtual defect density (N of Eq 1) of the order of $10^3/cm^2$ is significant. However, one must still assume a very large defect density at some small $t > 0$ which increases exponentially with thinner oxides. This problem is especially critical to MOSFET technology where gate oxides of 1000 Å, or less, are generally required. It seems more important, therefore, to understand the physical basis for the virtual defect density, so that it can be manipulated downwards, rather than attempting to increase defect decay factors.

TABLE I
CORRELATION OF DEFECT DENSITIES WITH VARIOUS STRESS CONDITIONS

Oxide (Å) Thickness	Run No.	Oxidation Time, t (minutes)	$t^{1/2}$	Defects: Per cm^2 *		
				No Stress (vapor etch pits)	Full Stress (decorated)	Partial Stress (decorated)
1720	A	5	2.24	39	161	292
1995	B**	10	3.16	10	151	190
2590	C	15	3.87	3.0	101	142
3125	D	20	4.47	1.5	33	43
2945	EJ	25	5.00	1.2	55	93
3760	I	25	5.00	1.2	26	40
4010	F**	40	6.32	0.3	9	42
5325	G	60	7.81	0	12	29

*All entries represent an average of four wafers - data in Appendix E-1
**Runs selected for initial Proficorder study

Silicon Surface and Initial Oxidation Aspects

Further investigation revealed that a kinetic anomaly in oxide growth rate existed at the beginning of oxidation (during the first 300 to 600 Å) after which a square root law characteristic of a diffusion controlled process was followed. Attention, therefore, was focused on the beginning phase of oxidation in the expectation that moderation of the reaction kinetics at this point might remove an assumed distributional irregularity in the oxide and thereby reduce the latent defect density. Such a moderation was achieved (and kinetically demonstrated) by application of an oxidative pretreatment (using hot nitric acid) which developed a very thin oxide layer on the wafers prior to high temperature oxidation. A significant drop in the latent defect density (extrapolated to oxidation time zero) was observed as a result of this treatment.

Accordingly, wafers were pretreated in a manner designed to produce diffusion attenuation layers on the surfaces. These layers consist primarily of silicon dioxide in the 200 Å or less thickness range produced by a wet chemical method consisting of treating the wafers with HF (to remove old oxide), KOH solution (to remove residual fluoride), and hot concentrated nitric acid (to remove residual KOH and initiate uniform oxidation). Each step was followed by thorough rinsing with distilled water. The exact nature of the layers so produced still is unknown. Boundaries in such layers

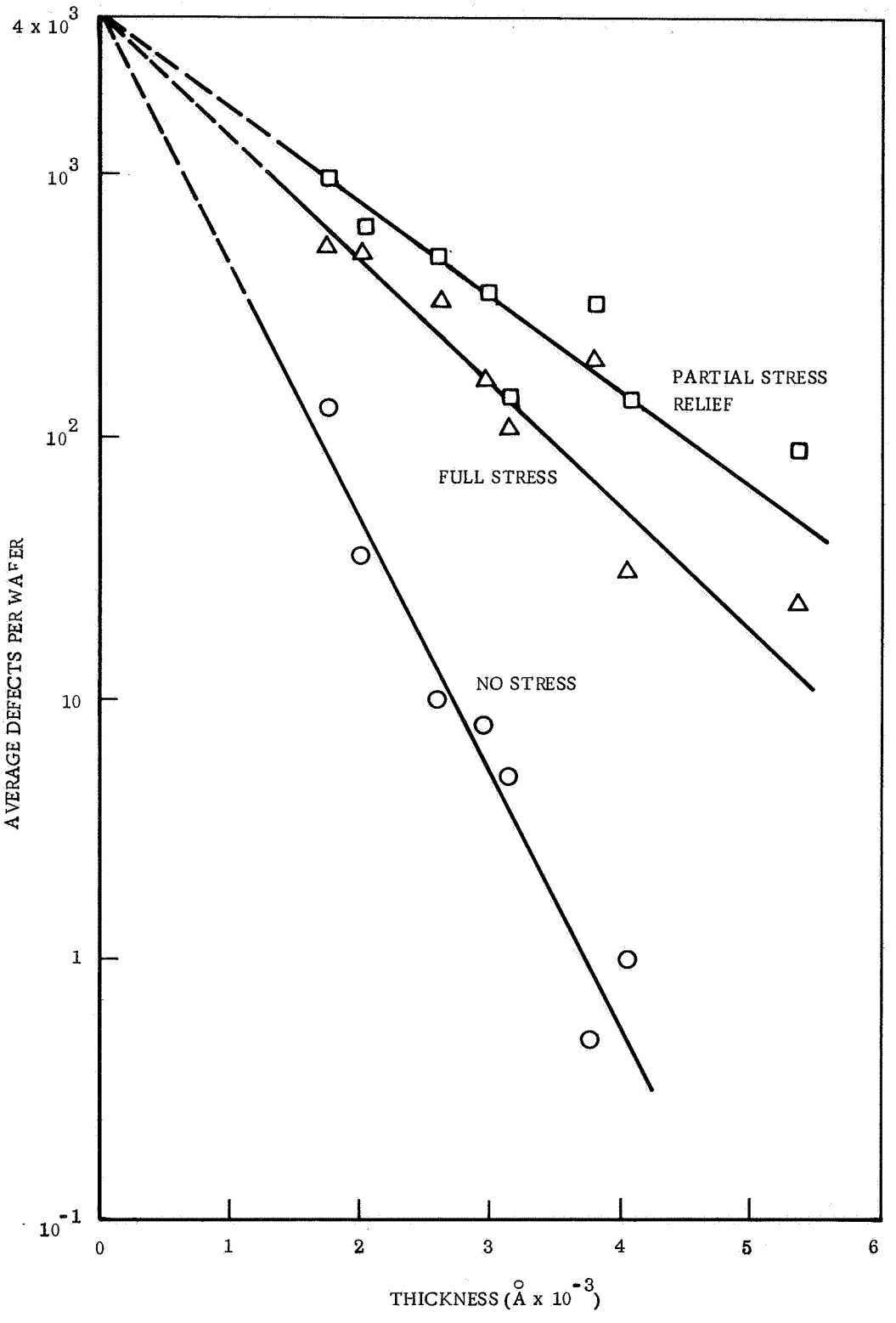

Figure 2. Defects as a Function of Oxide Thickness For Various Stress Conditions

produced by controlled (masked) HF etching are readily revealed by moisture condensation from a humid environment. Attempts to measure the thickness of the layers by Proficorder and Tally-Surf tracing, and by interferometry, however, failed. Although the layers are suspected of being a porous and partly hydrated silicon dioxide, the possibility of a small component of nitride cannot be ruled out.

High temperature oxide defect densities on wafers so treated (termed hereinafter "oxidative precleaning") were found to be practically nonexistent, even for oxidation time as short as 2.5 min. Room temperature decorated defects, however, were significant. The corresponding defects densities are shown as Set A in Table II.

Nonoxidative vs Oxidative Cleaning

It was not clear from these results whether the decrease in defect density was due solely to the initial oxidative attack on the substrate or to an additional "cleansing effect" caused by the nitric acid treatment. Therefore a "nonoxidative" precleaning technique was developed. In this case the wafers were "nonoxidatively" precleaned using a swabbing technique with HF, preceded and followed by water and alcohol rinses.

Slow oxide growth was achieved by limiting the oxygen to 4 percent of the process gas composition and by reducing the temperature of the water reservoir. The oxidation temperature, however, remained at 1180 C.

All data were taken as a function of oxide thickness grown, as measured (in most cases) by Proficorder tracing. All defect readings are recorded on a cm^{-2} basis. In addition the ratio of etch pits (high temperature defects) to decorations (room temperature defects) were computed for each series, where applicable, as a further test of internal consistency. The "nonoxidative" results are shown as Set B in Table II.

Comparison of Sets A and B in Table II plotted against oxide thickness (Figure 3) indicates that there may be little or no difference in how the initial oxidation rate is moderated. The effect of both on the virtual defect density appears to be significant. Compared with earlier results, which yield a virtual defect density of $\sim 4 \times 10^3$ per wafer ("Full Stress" curve, Figure 2), or $>10^3$ cm^{-2}, the present treatments yield an order of magnitude improvement ($\sim 1.1 \times 10^2$ cm^{-2}). Although the defect decay rate is somewhat smaller than that applicable to Figure 2, this potential modification in process technique may have important implication for thin oxide applications, such as MOS gates. At 1000 Å oxide thickness, for example, Figure 2 yields a density of 410 defects cm^{-2} (taking the wafer area as 3.2 cm^2) while Figure 3 yields a density of 70 cm^{-2}.

This result was taken as potential confirmation that the assumed initial inhomogeneities associated with latent defect densities were, in fact, related to the observed kinetic anomaly at the beginning of oxidation. Further attention was given, therefore, to the effects of the various process parameters on defect densities in the first few hundred Angstroms of growth. It was shown that the nonoxidative precleaning treatment was superior to the oxidative treatment in reducing defect densities in this

TABLE II
DEFECT DENSITIES AS A FUNCTION OF PRETREATMENTS AND GROWTH RATE

Set	Wafer Precleaning	Water Temperature (Deg C)	Oxide Growth Rate	Oxide Thickness (Angstroms)	Etch-Pit Density (cm^{-2})	Decoration Density (cm^{-2})	Etch-Pits/ Decorations
A	Ox.	95	Normal	1300		67.0	
	Ox.			2000		54.0	
	Ox.			2700		27.6	
	Ox.			3000		23.5	
	Ox.			4100		15.7	
	Ox.			5000		12.6	
B	Non-Ox.	34-35	Slow to 400 Å then Normal	1600	0	47.4	
	Non-Ox.			1800	0.079	43.6	0.0018
	Non-Ox.			2800	0	37.7	
	Non-Ox.			3600	0.079	20.0	0.004
	Non-Ox.			4600	0	11.3	

Data in Appendix E-2

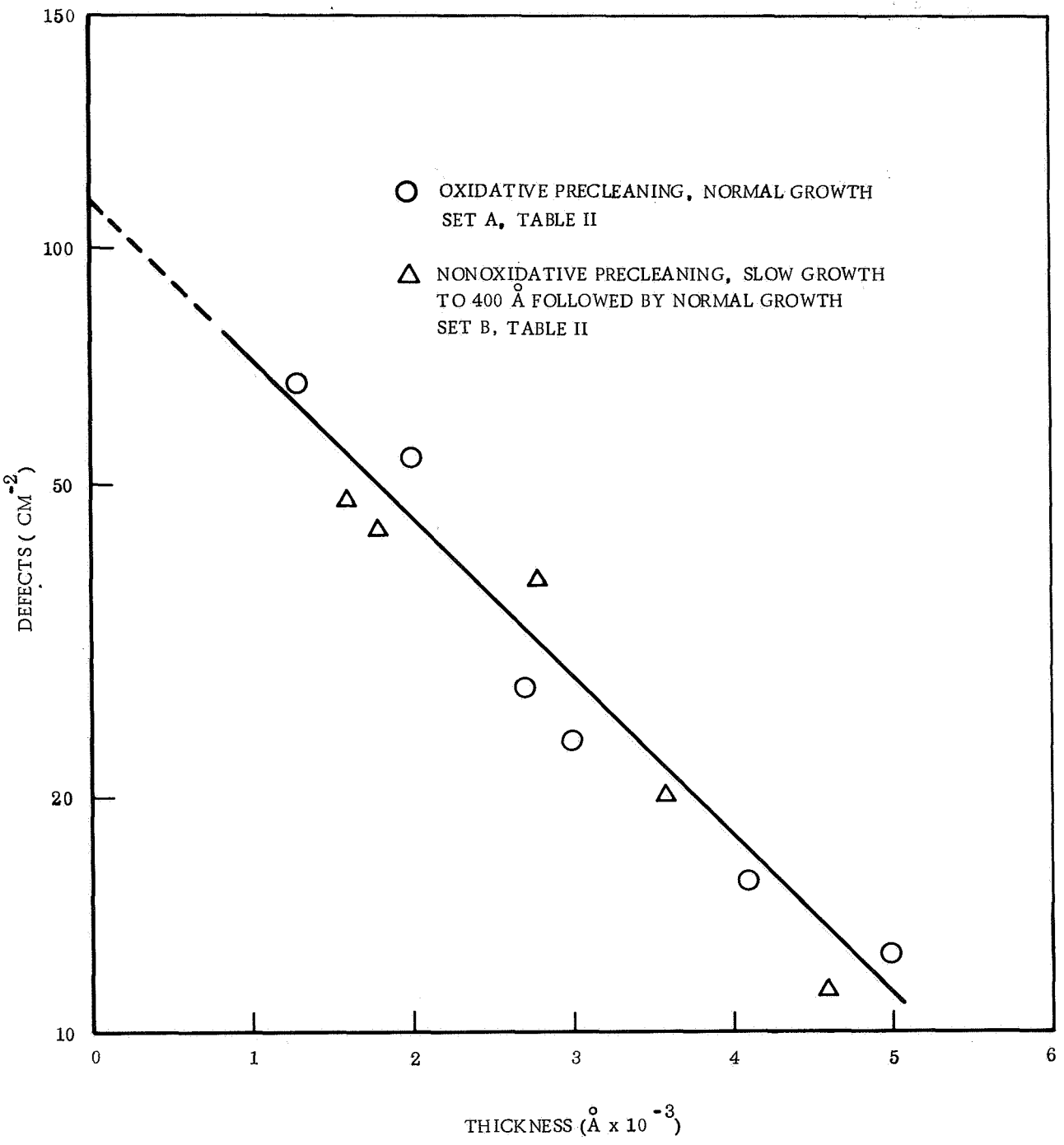

Figure 3. Comparison of Oxidative Precleaning With Nonoxidative Precleaning Plus Initial Slow Growth

region. It also was shown that initial slow thermal oxidation after the nonoxidation precleaning produced additional oxide improvement if dry, rather than wet, oxygen was used. It was possible at this point, therefore, to formulate a tentative set of optimum process conditions for oxide growth. These included an initial nonoxidative precleaning of the wafers (using a wiping technique with HF, as previously described) and an extremely slow initial growth of thermal oxide using dry oxygen, followed by conventional growth with moist oxygen.

In attempting to adduce a physical basis for the effects described above, it became evident that the controlling process parameter might be one of equilibration rather than of oxygen diffusion attenuation. That is, the inhomogeneities determining defect loci might as well be purely structural instead of being confined to the result of kinetic irregularities in the initial oxide distribution. In either case, then, the initial slow oxidation might provide the necessary conditions for the equilibrium distribution of either oxide or substrate material, whereas oxygen diffusion attenuation alone would affect only the oxide distribution. The participating physical irregularities of the oxide-substrate system, regardless of origin, would be in the submicron range; e.g., a significant fraction of the oxide layer thickness and several orders of magnitude greater than the substrate lattice parameter. The appearance of a defect in the oxide layer (after cooling) then would become a function of the particular local stress conditions associated with the radius of curvature of the presumed structural irregularity. As more oxide is grown the ratio of the radius of curvature to the oxide thickness will decrease exponentially with oxide thickness, thus accommodating the corresponding disappearance of dielectric defects. In addition to accounting for the localization of oxide defects a model of this type is more susceptible to physical verification.

The nitric acid pretreatment would be expected to attack microscopic promontories on the silicon surface more rapidly than surrounding smooth areas, thus reducing their effectiveness in creating localized stress anomalies in the subsequent oxide layers. Reconsideration of the "nonoxidative" pretreatment discloses that the opportunity for limited oxidation occurs here, too, because the HF wiping procedure is done in the presence of air. In other words, the treatment is nonoxidative only in the sense that it leaves no additional oxide layer on the silicon surface. The wiping process therefore can be regarded as a chemical lapping in which promontories are more susceptible to erosion than surrounding flat areas. The HF serves the familiar function of removing silicon dioxide as it is formed.

HCℓ Wafer Pretreatment

The above concept was subjected to further test by applying an HCℓ vapor etch to wafers (four sets of four each) immediately prior to oxidation. * This idea is not novel, as it has been recently learned that Semimetals (q.v., below) employs the

*This treatment differs from one investigated earlier at the Qualification and Standards Laboratory, NASA-ERC, where HCℓ was admitted during oxidation in an attempt to modify the composition and structure of the oxide layers as they were grown.

same treatment prior to wafer oxidation. The decoration densities resulting from the inclusion of this treatment are compared in Table III with a similar set in which the HCℓ pretreatment was omitted. It is clear than an improvement was thereby achieved (in the 500 Å thickness range) even though both sets of wafers also were pretreated by the chemical lapping ("nonoxidative") method.

Continuing further with the equilibration approach, tests were designed to maximize the redistribution of assumed structural irregularities both in "bare" silicon and in very thin initial oxide layers using various heat-soak periods at the oxidation temperature (1180 C). Because this temperature is well above the set temperature of silica (1000 C) it was felt that the oxide would be sufficiently plastic to conform to any interfacial energy-reducing material migrations. In consideration of the number of process variables of interest a simple matrix was designed in which the normal oxidation periods were given only two values (5 min and 20 min, Table IV). These process variables included a comparison of the effects of initial oxide layers produced by oxidative precleaning technique with those produced by initial thermal oxidation (using 4 percent dry O_2 diluted with helium) (sets C and D), time of heat soak in nitrogen (two values) (sets E and F), and comparison of dynamic with essentially static nitrogen flow during heat-soak (sets D and E). A control omitting the major variable was included with each run. Each charge consisted of four wafers whose etch-pit and decoration counts were averaged to yield the data in the last two columns of Table IV.

TABLE III
*EFFECT OF HCℓ PRE-ETCHING ON
SUBSEQUENT OXIDE DEFECT DENSITIES

Set	Wafer Precleaning	HCℓ Pre-treatment	Water Temperature (Deg C)	Oxygen Conc. (Percent)	Oxide Thickness (Ångstroms)	Decoration Density (cm^{-2})
A	Non-Ox	None	50	4	470	860
	Non-Ox	None	50	4	480	390
	Non-Ox	None	50	4	600	314
	Non-Ox	None	50	4	650	121
B	Non-Ox	1 min	50	4	500	201
	Non-Ox	1 min	50	4	500	144
	Non-Ox	1 min	50	4	510	278
	Non-Ox	1 min	50	4	560	46

*Data in Appendix E-3

TABLE IV
HIGH TEMPERATURE HEAT-SOAK EFFECTS ON SUBSEQUENT DEFECT DENSITIES*

Set	Wafer Precleaning	Thermal Pre-Oxidation (Min)	Heat-Soak in N_2 (Hrs)	N_2 Flow (cc/min)	Normal Oxidation (Min)	Oxide Thickness (Angstroms)	Etch-Pits (cm^{-2})	Defect Decorations (cm^{-2})
C	Ox	None	2	480	5	1400	9.4	161
	Non-Ox**	None	2	480	5	1400	9.3	61
	Ox	None	2	480	20	3000	2.5	29
	Non-Ox**	None	2	480	20	3100	3.1	12
D	Non-Ox	5	2	480	5	1300	0.63	37
	Non-Ox**	None	2	480	5	1550	8.06	31
	Non-Ox	5	2	480	20	3200	0	19
	Non-Ox**	None	2	480	20	2900	0.08	4.4
E	Non-Ox	5	2	10	5	1700	0.63	17
	Non-Ox**	None	2	10	5	1400	----	15
	Non-Ox	5	2	10	20	3000	1.57	15
	Non-Ox**	None	2	10	20	3100	0.24	9.4
F	Non-Ox	5	16	10	5	2200	1.8	10.3
	Non-Ox**	None	16	10	5	1200	18.3	82
	Non-Ox	5	16	10	20	3300	0	5.7
	Non-Ox**	None	16	10	20	2700	0.6	15.7

*Data in Appendix E-4
**Control: Initial thin oxide omitted

The results obtained are generally superior to the best data previously obtained by HNO_3 treatment (Figure 3), with the exception of the first value of set C. In sets C, D, and E the controls (in which the introduction of a first thin oxide layer was omitted) consistently yielded lower defect densities, whereas the reverse is true for set F in which the heat-soak period was increased to 16 hrs. These results appear to indicate a substrate surface redistribution process at 1180 C which is hindered by the presence of a thin oxide layer unless sufficient time is allowed for the highly viscous accommodation by the oxide. In comparing the results of sets C and D the oxidative precleaning again is shown to be inferior to the HF lapping and appears to be sufficient reason for abandoning further work with the nitric acid pretreatment. Analysis of sets E and F shows a slight improvement from a prolonged heat-soak, set F being superior to all previous runs. Comparison of sets D and E indicate that a slow nitrogen flow rate results in fewer defects than the normal flow rates used throughout the bulk of these investigations. An unidentified component of the nitrogen source may contribute to this effect. The relatively high defect densities from the control runs of set F, where the heat-soak was relatively prolonged, further suggests this possibility. In conclusion, it appears that treatments tending to promote greater smoothness of the substrate surfaces, as well as prolonged periods of equilibration to enhance initial oxide uniformity, may have an important bearing on the reduction of oxide defects.

In continuing experiments all wafers were precleaned by HF wiping, as described previously, and all were exposed to a five-minute treatment with four percent dry O_2 immediately prior to a 16-hour heat-soak in nitrogen. Process variables and resulting defect counts are summarized in Table V.

TABLE V
EFFECTS OF HCl PRETREATMENT AND HEAT-SOAK ON DEFECTS*

HCl Pre-treatment (Min)	N_2 Heat-Soak (Hrs)	Normal Oxidation (Min)	Oxide Thickness (Angstroms)	Defects (cm^{-2})
None	16	10	2600	12.3
None	16	40	4500	6.0
None	16	80	6100	3.7
1	16	5	1900	15.8
1	16	20	3300	5.7
2	16	5	2300	6.4
2	16	20	3200	4.0

*See Appendix A-5

A log plot of the first three defect counts yields approximately 1 defect/cm^2 when extrapolated to 10,000 Å, which compares with results from Vendors B and C wafers grown to 10,000 Å (see below). The second set of data, which includes a one-minute HCℓ treatment prior to the dry O_2 preoxidation, when similarly plotted yields less than 0.1 defects/cm^2 at 10,000 Å. The effect of the HCℓ appears to be to cause a significantly higher defect decay rate with oxide thickness as a result of reducing initial wafer surface irregularities. Increasing the HCℓ treatment to two minutes produced a further reduction of defect densities as shown in Table V.

The results are clearly superior to those obtained with a shorter HCℓ pretreatment. Extrapolation to 10,000 Å again yields a defect density of the order of 0.1/cm^2.

This HCℓ pretreatment, however, was distinctly less than optimum because it introduced clearly visible (at 100 X) etch pits in the wafers. Etch pit sizes lay in the micron and submicron range. A comparison of etch pit counts with defect counts revealed a distinct correlation as shown in Table VI.

The only anomalous results in this progression are the ones starred. This is the first known direct evidence that depressions in the silicon surface, in the micron and submicron range, give rise to subsequently grown oxide irregularities which are incapable of withstanding the compressive stress introduced on cooling from the oxidation temperature. It is well known that vitreous silica is remarkably resistant to compressive stress but yields readily to tension and shear. The abrupt changes in oxide curvature caused by the etch pits introduce tension and shear vectors as resultants of the existing compressive stress.

TABLE VI
OXIDE DEFECTS AS A FUNCTION OF PREVIOUSLY INTRODUCED ETCH PITS

HCℓ Etch Pits (per wafer)	Ultimate Defects (per wafer)
72	20
77	45*
82	27
98	34
116	16*
125	40
174	58
233	115

Dielectric Defects - Vendor Survey

Defect analyses of 10,000 Å oxides prepared by three manufacturers was performed for comparison with the Autonetics laboratory results obtained. The results obtained are summarized in Table VII.

The superiority of the Vendor A product is clearly evident with 80 percent of the wafers having no defects at all. A Vendor Representative indicated to Autonetics that its oxidations were preceded by an HCℓ etch; no other vendor made this claim. In view of the results tabulated in the preceding section of this report it seems likely that neither Vendor B nor Vendor C employ a pre-etch with HCℓ. The defect levels of the latter two manufacturers are characteristic of those obtained on this program prior to the use of an HCℓ etch.

Also of interest is the variation represented by Vendor C's lot number 3, indicating a lot-to-lot control problem. This is common to the entire lot, with a standard deviation of ± 1.64 defects/cm^2 (±46 percent). NASA centers would be well advised to require a test wafer for defect analysis after the first oxidation prior to purchasing planar devices from a given lot. It also would seem prudent for manufacturers to adopt some embodiment of the electrophoretic decoration test (as described in Appendix A of this report) not only to inform themselves of lot-to-lot control problems but also of their standing with the oxide quality of other vendors.

TABLE VII
DEFECT LEVELS IN 10,000Å OXIDES FROM VARIOUS SOURCES*

Company	Number of Wafers	Average Defects (cm^{-2})	Wafers With Zero Defects (%)	Maximum Count (wafer $^{-1}$)
Vendor A				
Lot 1	10	0.040	80	1
Lot 2	28	0.057	79	2
Vendor B				
Lot 1	10	0.29	30	9
Lot 2	10	0.69	0	19
Lot 3	10	0.72	10	13
Vendor C				
Lot 1	30	0.73	3.3	11
Lot 2	10	0.55	20	10
Lot 3	10	3.55	0	41

*See Appendix F for data

Dielectric Defects - Pilot Line Test

Standard Rel-chip wafers were fabricated on the Autonetics pilot line by three process modifications designated as "Standard," "Interim," and "Experimental." Each modification was represented by 18 wafers which additionally were divided into three pretreatment subgroups of six each comprising standard pretreatment, HF wiping, and HCℓ pre-etching. Final window opening and metallization was omitted in five out of each set of six wafers and were defect counted by electrophoretic decoration. The sixth wafer was carried through metallization and electrically tested for dielectric breakdown in the capacitor area which was 0.008 in. x 0.008 in. x 1400 Å thick. The wafers contained an average of 435 Rel-chip integrated circuits; all of the IC's on each of the five wafers of each group were defect counted. The results for each process modification and each wafer pretreatment are summarized in Table VIII.

Histograms of the data are presented in Appendix G. The information summarized in the first histograms indicates a "tighter" distribution for the thin oxides of all wafers with a mode of 2 defects per wafer. The thick oxides show a greater spread on the average with a mode also at 2 defects per wafer. (The thick oxide area is of course much larger than the thin oxide layer.) Other histograms in Appendix G show the data for thin and thick oxides as a function of process and pretreatment. The thin oxide distribution by process show a considerable spread for the interim process and thus a possible out-of-control situation. There was also a considerable spread in all of the thick oxide data.

The data summary (average values) shown in Table VIII indicate no significant trends in thick or thin oxide defect density as a function of the variables examined. The additional pretreatments appear to have produced some improvement in the thin (1400 Å) oxide produced by the "Standard" process but this relationship was reversed on the Interim and Experimental process. Both of the pretreatments were accompanied by increased defects on the thick oxides. It appears that more data are needed in order to arrive at statistically significant conclusions. Other factors appeared to be present which confounded the data obtained. This is indicated in Figures 4 and 5 which show respectively a random and nonrandom distribution of defects on two wafers examined.

An attempt was made to compare these data with those previously obtained on this program for three vendor oxides. It was necessary to extrapolate the data since the pilot line oxides were 1400 and 14,000 Å while the vendor oxides were 10,000 Å. By use of the decay constants (slopes) for curves B or C in Figure 1 extrapolation would reveal that the pilot line thin oxides are comparable with Vendors B and C while Vendor A is an order of magnitude better. Also the pilot line oxides were subjected to several thermal excursions not represented in the sample growth of the vendor oxide.

The above results were substantiated by electrical tests on the metallized wafers. Among all capacitors tested not a single electrical breakdown was induced under an applied potential of 100 v. In the present case this amounts to a field of 0.07 v/Å which is about 70 percent of the breakdown strength of sound oxide and considerably higher than fields sustained in normal operation.

TABLE VIII
VARIATION OF DEFECT DENSITIES WITH
PROCESSING AND PRETREATMENTS*

Process	Pretreatment		
	Standard	HF Wiping	HCℓ Pre-etch
Standard			
Thick oxide** (cm^{-2})	1.1	2.9	2.3
Capacitor *** (cm^{-2})	32.4	10.2	13.1
Oxide step (cm^{-1})	0.10	0.09	0.09
Interim			
Thick oxide (cm^{-2})	0.9	0.8	1.7
Capacitor (cm^{-2})	14.8	23.5	52.5
Oxide step (cm^{-1})	0.06	0.15	0.16
Experimental			
Thick oxide (cm^{-2})	0.6	1.0	1.1
Capacitor (cm^{-2})	7.5	8.9	14.2
Oxide step (cm^{-1})	0.02	0.02	0.07

*See data in Appendix G
**14,000 Å
***1,400 Å

Terms Used in Table

Standard Pretreatment	Standard Pilot Line cleansing of wafers prior to initial oxidation. (Solvent, HF "rinse" 10 percent dilution.)
HF Wiping Pretreatment	HF experimental technique. (HF swabbing in transverse directions prior to initial oxidation.)
HCℓ Pre-etch Pretreatment	HCℓ experimental technique. (Pre-clean No. 1 followed by HCℓ etching of wafer at oxidation temperature followed by immediate initial oxidation in same furnace.)

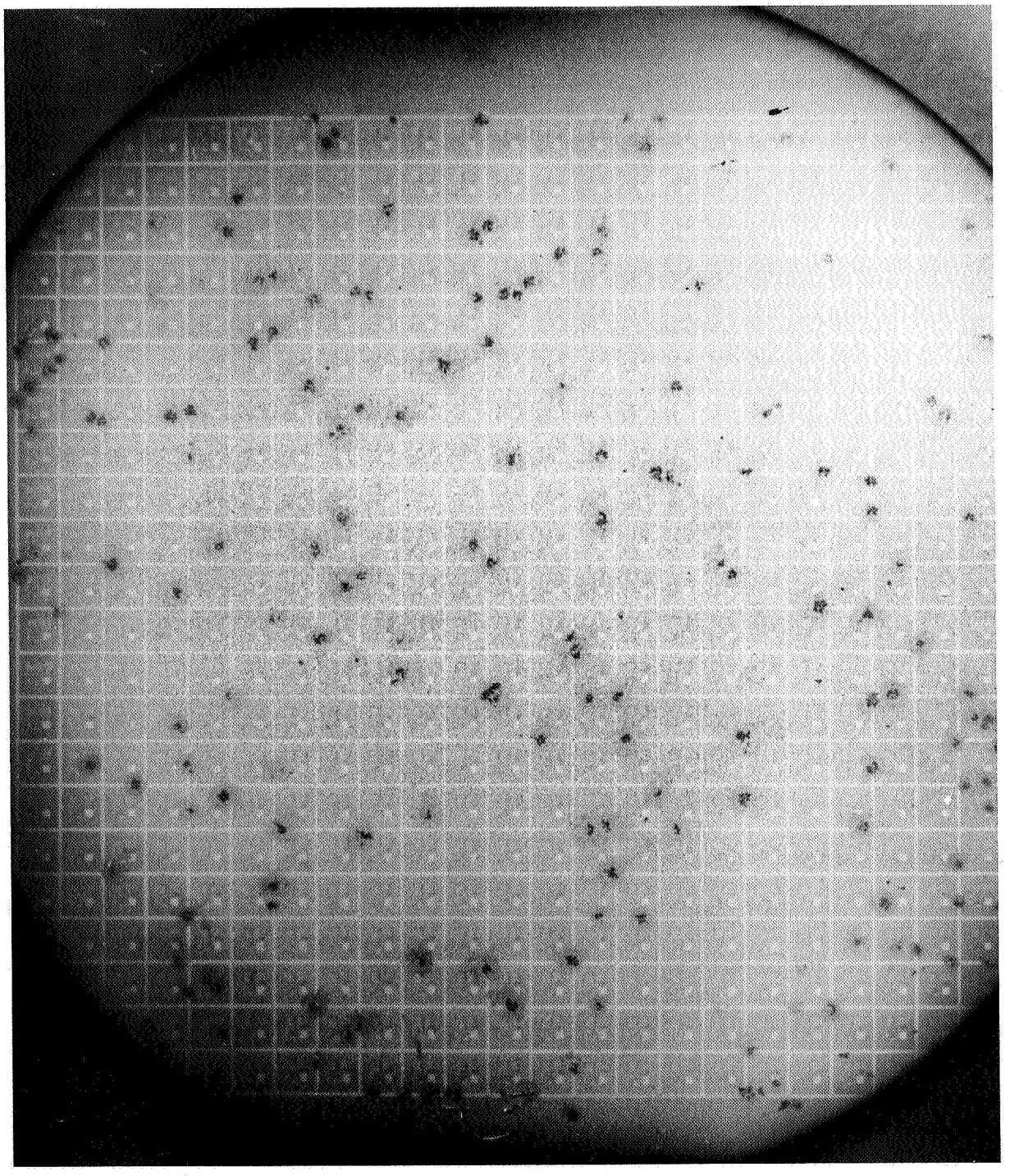

Figure 4. Test Wafer Showing Random Distribution of Dielectric Defects

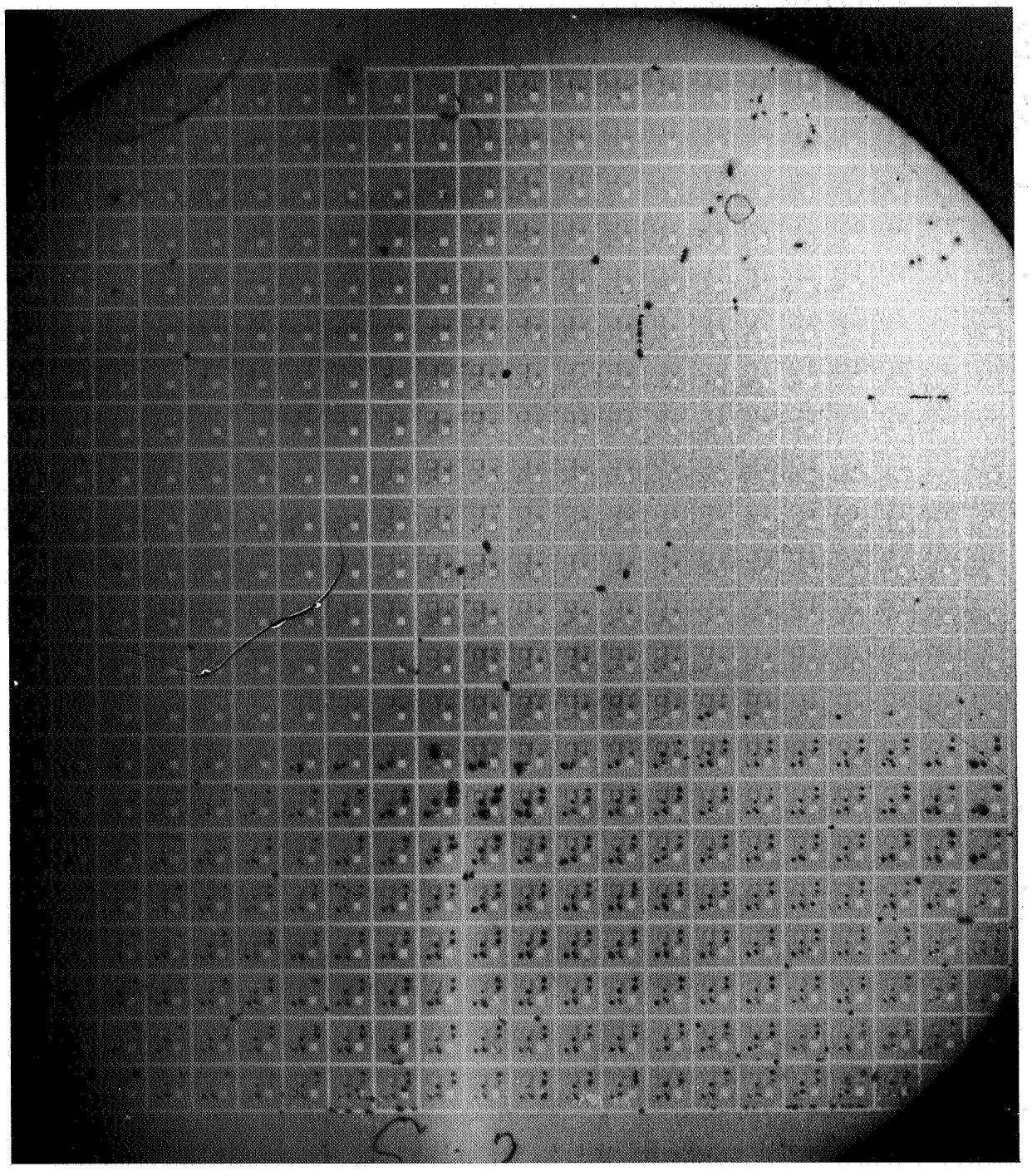

Figure 5. Test Wafer Showing Non-Random Distribution of Dielectric Defects

As observed in the past, a substantial proportion (greater than 50 percent) of the total defects were situated along oxide steps. The linear densities given in Table VII were derived only from the peripheries of the large capacitor regions. It was not determined whether these defects were actually on the step or possibly in a trough of extremely thin oxide believed to be at the base of the step. No vendor step data is currently available for comparison.

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BIBLIOGRAPHY ON SILICON SURFACE PASSIVATION

This program has been directed toward an understanding of the interrelationship of semiconductor device processing and the resultant reliability. Specifically, the role of surface passivation and related process variables has been studied.

In conjunction with the research carried out on this program, a continual literature review was made, with a goal of relating other findings to the results of this program. Also searched for were improved passivation techniques which might reduce or eliminate the problems defined for currently used Si-SiO_2 systems. The following is a synopsis of some of the pertinent information which is applicable to the research performed. The information is presented in several related sections.

Preparation of Oxide Layers

A comprehensive report on the process parameters for oxidized silicon was prepared by the Research Triangle Corporation (Ref 1). A more detailed analysis of the kinetics of the growth process has been presented in several articles by Deal (Ref 2) and Burkhardt and Gregor (Ref 3). The parabolic growth rate constants as a function of various process variables was explored by Ainger (Ref 4). The oxidation kinetics of silicon were studied by Law (Ref 5) at temperatures from 1000 to 1300K and pressures from 10^{-3} to 5 x 10^{-2} mm. This information confirmed the parabolic growth rate, with the rate constant being markedly pressure dependent.

It has been demonstrated that hydroxyl groups can be introduced into silica by high temperature exposure to water vapor (Ref 6), that oxides grown in steam or wet ambients contain measurable amounts of hydrogen (Ref 7, 8, 9), and that thermally grown oxides incorporate varying amounts of the substrate dopant into the oxide structure (Ref 10, 11). Investigators have shown that the growing oxide has an affinity for boron but rejects phosphorus and antimony (Ref 11).

Nossibian and Whiting (Ref 12) showed that particulate contaminations on the oxide surface act as loci for the formation of high concentration regions of P_2O_5 during a deposition of phosphorus. In the subsequent diffusion, the phosphorus is considered to penetrate the oxide preferentially beneath these high concentration sources, doping the silicon substrate in localized regions under the oxide.

Several low temperature techniques have been proposed for forming silicon oxide films. These methods are of special interest in that they reduce the thermal stress problem possibilities.

Thin oxide films were formed by dilute HNO_3 and studied (Ref 13). The formation of SiO_2 films by the low temperature (750 C) decomposition of tetraethoxysilane in an evacuated system was studied (Ref 14). The performance of the system was investigated and the film characteristics evaluated. Most of the properties of the deposited oxides were similar to those of thermally grown oxides after a thermal treatment. Hennisch (Ref 15) devised a closed tube method for deposition of SiO_2 via decomposition of tetraethoxysilane.

The growth of SiO_2 in a microwave discharge was investigated by Kraitchman (Ref 16). This technique provided rapidly oxidized silicon at temperatures estimated to be 500 C or lower.

Ing and Davern (Ref 17) described a process for the formation of silicon oxide thin films by the low temperature decomposition of tetraethoxysilane in an a-c glow discharge. It was shown that films produced in this manner can be used effectively as the dielectric in thin film capacitors. The resultant capacitors have low dielectric losses and are very stable under various life test conditions.

Other Passivation Techniques

Several other materials or combinations of materials have been investigated in an attempt to eliminate some of the objectionable problems detected for the $Si-SiO_2$ system.

Aboaf (Ref 18) experimented with amorphous aluminum oxide films deposited at 420 C by thermal decomposition of an aluminum alkoxide. The dielectric and moisture resistance properties were favorable when compared with conventional SiO_2.

MOS transistors with aluminum oxide gate dielectric were fabricated and tested by Waxman and Zaininger (Ref 19). Their films are formed by anodizing aluminum in an oxygen plasma. The radiation resistance of these devices appeared excellent.

The most promising substitute and the one with extensive work involves various types of silicon nitride films. Typically silicon nitride films have been deposited on silicon by reacting $SiCl_4$ and NH_3 at 550 - 1250 C (Ref 20). One important finding is that the deposited films are extremely effective diffusion masks for sodium.

Amorphous silicon nitride films have been deposited in a gas flow system by the ammonolysis of silicon tetrachloride and the nitridation of silane with ammonia (Ref 21, 22). The substrate temperature during the deposition process appeared to have the most significant influence on the film properties. It has been shown that such amorphous nitride films can be converted to anodic SiO_2 (Ref 23).

Amorphous films of silicon nitride-silicon dioxide mixtures were deposited and evaluated by Chu and coworkers at Westinghouse (Ref 24). The technique utilized was the pyrolysis of silane in ammonia-oxygen mixtures in a gas flow system. Heat treatment of silicon nitride films (Ref 25) was found to result in severe structural changes resulting in fractured layers.

Passivation Layer Mechanical Aspects

Mechanical rupturing of the oxide film has been related in this report and by others (Ref 26) to the difference in coefficient of thermal expansion between silicon and the passivation layers utilized.

The evidence as reported (Ref 27, 28) indicates that dielectric failures are a result primarily of actual physical openings in the insulating layer rather than regions of enhanced conductivity in uniformly thick oxide.

The silicon-silicon oxide stress has been experimentally measured (Ref 27, 29) and was found to be in the range from 30,000 to 60,000 psi. The expansion characteristics of silicon apparently exhibit unusual behavior (Ref 30) above ~ 1000 C.

The effect of structural defects such as hydroxl groups and network forming or other modifications is to alter the silica structure producing a less rigid network. This alteration is reflected in changed physical and electrical properties. For example, the introduction of either boron (Ref 31) or hydroxl (Ref 32) into the SiO_2 structure increases the thermal expansion coefficient and decreases the viscosity of the modified material relative to the intrinsic oxide. Strains at the Si-SiO_2 interface were measured by Joecodine and Schlegel (Ref 33) and Whelan (Ref 34). Besser and Eisenberg (Ref 35) and Lopez (Ref 36) studied the factors that affect the density of defects in SiO_2 films. Lane (Ref 37) has recently correlated stress in the Si-SiO_2 interface to surface state density.

Lopez (Ref 38) found that defect density for a particular thickness was greater for the thinned oxide than for the unaltered oxide.

It has been shown that mechanical polishing results in a certain amount of structural damage to the silicon surface and may leave particles of the polishing compound embedded in the polished surface. This was recently confirmed (Ref 39) by electron microprobe analysis performed by Cocca and Carroll at NASA-ERC. This may be the origin of the somewhat higher defect density in the oxide grown on such wafers.

Fisher and Amick (Ref 40) detected defect structures on silicon surfaces after oxidation which were partially due to stresses induced by the oxidation processes. Slip in Si crystals has also been suggested. Recently Drum and Rand reported (Ref 41) a method of reducing stress by using a silicon oxide-silicon nitride combination. Stresses of the order of 10^7 dynes/cm^2 were obtained which is 2 to 3 orders of magnitude lower than usually obtained.

Techniques utilized by other investigators were evaluated for use on this program for the detection of dielectric defects. Techniques such as a high temperature HCℓ etch (Ref 42) or Cℓ etching around 900 C (Ref 43, 44) were found to be not conveniently applicable. The results obtained earlier on this contract have been reported (Ref 27) and two techniques which were found to be suitable, electrophoretic decoration and electrochemical autograph, were utilized in this study for the observation of oxide defects.

Passivation Layer Properties and Evaluation Techniques

Techniques for the physical and chemical evaluation of silicon oxide films formed by a wide variety of techniques have been developed (Ref 45). Silicon oxide films were characterized on the basis of refractive index, etch rate, infrared spectra, stoichiometry, passivation efficiency and thermal densification. It was found that films formed by low temperature techniques generally had properties inferior to oxides formed by conventional high temperature techniques.

Worthing (Ref 46) and Klein (Ref 47) made evaluations of dielectric breakdown in thin oxide films. At positive silicon potentials, Worthing found that dielectric breakdown occurred abruptly with no detectable conduction at lower voltages. At negative silicon potentials, conduction in the nanoamp range and time dependence of dielectric breakdown was detected. Klein confirmed that breakdown starts on electric field induced thermal instability at flaws in the dielectric resulting in a hole through the oxide.

The properties of silicon nitride-silicon oxide mixtures were obtained by Chu, Szedon, and Lee (Ref 24).

The electrical properties of both silicon nitride and silicon oxide were investigated by Deal, Fleming and Castro (Ref 48). As contrasted to the thermal oxides, the silicon nitride films are characterized by polarization and room temperature trapping instabilities, relatively high conductance, and high surface state charge densities. The vapor-deposited oxides were found to resemble the nitrides in those properties which were associated with the silicon-dielectric interface, but the bulk properties were more like those of thermal oxides. The properties of a $SI_xO_yN_z$ film on Si was investigated by Brown and others at G. E. Research, Schenectady (Ref 49). These films were formed by the pyrolysis of various mixtures of SiH_4, NH_3, and NO.

Several investigators have utilized the MOS test structure as a means for electrical evaluation of silicon oxide films. Typical reviews by Fairchild personnel describe impurity distributions of oxidized silicon and ion migration kinetics (Ref 50, 51).

A method of doping the oxide film with (DEP) diethylphosphate-nitrate-tetrahydrofuryl alcohol alcohol was studied for use in device diffusion of phosphorus (Ref 52). The fabrication of simple device structures by controlled out-diffusion of phosphorous from the oxide was evaluated.

References

1. R. P. Donavon, "Oxidation," Integrated Silicon Device Technology Ser. Vol. 7, Research Triangle Inst. Durham, N.C., Report No. ASD-TDR-63-316, DDC-AD-618-704, 1965.

2. B. E. Deal, "The Oxidation of Silicon in Dry Oxygen, Wet Oxygen, and Steam," J. Electrochem. Soc, Vol. 110, 1963, pp 527-533.

3. P. J. Burkhardt and L. V. Gregor, "Kinetics of the Thermal Oxidation of Silicon in Dry Oxygen," Trans. Met. Soc, AIME, Vol. 236, 1966, pp 299-305.

4. F. W. Ainger, "The Formation and Devitrification of Oxides of Silicon," Journal of Materials Science 1 (1966).

5. J. T. Law. "The High Temperature Oxidation of Silicon," Journal of Physical Chemistry, Vol. (61).

6. R. W. Lee, Physics and Chemistry of Glasses, 5, 35 (1964).

7. J. E. Meinhard, Electrochemical Society Spring Meeting, 1966, Cleveland, Ohio, Recent News Paper No. 19.

8. T. E. Burgess and F. M. Fowkes, Extended Abstracts of the Electronics Division of the Electrochemical Society 15, No. 1, 110 (1966).

9. P. J. Burkhardt, Electrochemical Society Spring Meeting, 1966, Clevelend, Ohio, Recent News Paper No. 18.

10. M. M. Atalla and E. Tannebaum, Bell Systems Techn. J. 39, 933 (1960).

11. A. S. Grove, O. Leistiko, Jr., and C. T. Sak, J. Appl. Phys. 35, 2695 (1964).

12. A. G. Nossibian and G. Whiting, Solid State Electronics, 7, (1964).

13. W. B. Glendinning, S. Marshall, A. Mark, "Thin Films Grown on Silicon Surfaces by Excess Nitric Acid Process," J. Electrochem. Soc., 112, No. 12, (1965).

14. J. Orashnik and J. Kraitchman, "Pyrolytic Deposition of Silicon Dioxide in an Evacuated System," J. Electrochem. Soc. Vol 115, No. 6 (1968).

15. G. W. Hennisch, "Closed Tube Apparatus for the Deposition of Silicon Oxide," J. Electrochem. Soc., Vol. 114, No. 6, (1967).

16. J. Kraitchman, J. Appl. Physics, V. 38 (1967).

17. S. W. Ing, Jr. and W. Davern, "Glow Discharge Formation of Silicon Oxide and the Deposition of Silicon Oxide Thin Film Capacitors by Glow Discharge Techniques," J. Electrochem. Soc., V. 1112, (1965).

18. J.A. Aboaf, "Deposition and Properties of Aluminum Oxide Obtained by Pyrolytic Decomposition of an Aluminum Alkoxide," J. Electrochem. Soc., Vol. 114 (1967).

19. A. Waxman and K.H. Zaininger, "$A\ell_2O_3$ - Silicon Insulated Gate Field Effect Transistors," Applied Physics Letters, Vol. 12, No. 3 (1968).

20. M.J. Grieco, F.L. Worthing, and B. Schwartz, "Silicon Nitride Thin Films from $SiC\ell_4$ Plus NH_3; Preparation and Properties," J. Electrochem. Soc., Vol. 115 (1968).

21. T.L. Chu, C.H. Lee, and G.A. Gruber, "The Preparation and Properties of Amorphous Silicon Nitride Films," J. Electrochem. Soc., Vol. 114, No. 7, (1967).

22. T. Sugano, K. Hirai, K. Kuroiwa, and K. Hoh, "Vapor Deposition of Silicon Nitride Film on Silicon and Properties of MNS Diodes."

23. P.F. Schmidt and D.R. Wonsidler, J. Electrochem. Soc., Vol. 114, No. 6 (1967).

24. T.L. Chu, J.R. Zedon, and C.H. Lee, "Films of Silicon Nitride-Silicon Dioxide Mixtures," J. Electrochem. Soc., Vol. 115, No. 3 (1968).

25. D.J.D. Thomas, "The Effect of Heat Treatment on Silicon Nitride Layers on Silicon," Physica Status Solidi, Vol. 20, No. 1-2 (1967).

26. A.N. Saxena and O. Tkal, J. Electrochem. Soc., Vol. 115, No. 2 (1968).

27. P.J. Besser and J.E. Meinhard, Proceedings of Symposium on Manufacturing In-Process Control and Measuring Techniques for Semiconductors, Phoenix, Arizona, March 1966, Vol. II.

28. R.L. Nolder, "Defects in Silicon Oxide Films on Integrated Circuits," 1966 Fall Meeting of Electrochem Soc., Philadelphia, Pa., Abstract 179.

29. S.S. Baird, Annals New York Academy of Sciences, 101 (1963).

30. H.A. Robinson, Jr., Phys, Chem. Solids 26 (1965).

31. Corning Glass Works, "Properties of Selected Commercial Glasses," pp 8-83, Corning, New York (1961).

32. G. Hetherington and K.H. Jack, Phys, Chem. Glasses, 5, 35 (1964).

33. R.S. Joccodine and W.A. Schlegel, "Measurement of Strains at $Si-SiO_2$ Interface," J. Appl. Phys., Vol. 37 (1966).

34. M.U. Whelan, A.H. Goemans, L.M.C. Goossens, "Residual Stress at an Oxide-Silicon Interface," Appl. Phys. Lett., Vol. 10 (1967).

35. P.J. Besser and P.H. Eisenberg, "Factors Influencing Dielectric Defects in Silicon Oxide Layers," 1966 Fall Meeting of Electrochem. Soc., Philadelphia, Pa., Abstract 178.

36. A.D. Lopez, "Fast Etching Imperfections in Silicon Dioxide Films," J. Electrochem Soc., Vol. 113 (1966).

37. C.H. Lane, "Stress at the Si-SiO_2 Interface and its Relationship to Interface States," IEEE Transactions on Electron Devices, Vol. ED-15, No. 12 (1968).

38. A.D. Lopez, J. Electrochem. Soc., 113 (1966).

39. F.J. Cocca and K.G. Carroll, "Electron Microprobe Analysis of Impurity Heterogeneities in Thermally Grown Silicon Oxide," IEEE Transactions on Electron Devices, Vol. ED-15, No. 12 (1968).

40. A.W. Fisher and J.A. Amick, "Defect Structure on Silicon Surfaces After Thermal Oxidation," J. Electrochem. Soc., Vol. 113, No. 10 (1966).

41. C.W. Drum and M.H. Rand, "A Low-Stress Insulating Film on Silicon by Chemical Vapor Deposition," J. of Applied Physics, Vol. 39, No. 9 (1968).

42. "Manufacturing In-Process Control and Measuring Techniques for Integral Electronics, "No. 4, IR-8-140(IV), Motorola, Inc., Jan. 1965 1 97.

43. E.F. Duffek, E.A. Benjamini, and C. Mylroie, Electrochem Tech. 3, 75 (1965).

44. S.W. Ing, R.E. Morrison, and J.E. Sandor, J. Electrochem, Soc., 109, 222 (1962).

45. W.A. Pliskin and H.S. Lehman, "Structural Evaluation of Silicon Oxide Films," J. Electrochem. Soc., Vol. 112, No. 10 (1965).

46. F.L. Worthing, "D.-C. Dielectric Breakdown of Amorphous Silicon Dioxide Films at Room Temperature," J. Electrochem. Soc., Vol. 115, No. 1, (1968).

47. N. Klein, "The Mechanism of Self-Healing Electrical Breakdown in MOS Structures," IEEE Transactions on Electron Devices, Vol. ED-13, No. 11 (1966).

48. B.E. Deal, P.J. Fleming, and P.L. Castro, "Electrical Properties of Vapor-Deposited Silicon Nitride and Silicon Oxide Films on Silicon," J. Electrochem. Soc., Vol. 115, No. 3 (1968).

49. D.M. Brown, P.V. Gray, F.K. Heumann, H.R. Philipp, and E.A. Taft, "Properties of $Si_xO_yN_z$ Films on Si," J. Electrochem. Soc., Vol. 115, No. 3 (1968).

50. A.S. Grove, B.E. Deal, E.H. Snow, and C.T. Sah, Solid-State Electronics, Vol. 8 (1965).

51. B.E. Deal, E.H. Snow, and A.S. Grove, "Properties of the Silicon Dioxide-Silicon System," SCP and Solid State Technology, No. 1968.

52. P.F. Schmidt, T.W. O'Keeffe, J. Oroshnik, and A.E. Owen, J. Electrochem. Soc., Vol. 112, No. 8 (1965).

APPENDIX A

OXIDE DEFECT TEST PROCEDURE

Scope

The purpose of this test procedure is to detect the locations of dielectric defects in layers of silicon dioxide grown on silicon wafers and to provide a semiquantitative estimate of such defects per unit area. The test is applicable to an oxide thickness range of 1000 to 15,000 Å. It also is applicable to pyrolytic oxide layers provided they have been adequately densified. Poorly densified layers are disrupted by the test.

Specimen

The specimen shall consist of a silicon wafer derived from any planar processing step, prior to metallization, in which new oxide has been grown or where bare silicon has not been intentionally exposed, as in window etching.

Apparatus

The apparatus consists of a microscope, test cell, anode clamp, and power supply. Auxiliary equipment includes a hand counter and a diamond scribe.

The microscope to which this procedure applies is a Leitz Ortholux, fitted with a mechanical stage. If another microscope is substituted, the wafer area subtended by the 50X optics must be recomputed to give accurate defect densities. Alternatively, a defect count of the entire wafer may be taken which is then divided by the wafer area to give defect density. This alternative is impractically slow for high defect counts, such as those encountered with thin oxide layers.

The test cell consists of a heavily gold-plated brass cup affixed to an insulating substrate which can be conveniently clamped by the mechanical stage. The cup is circular with an inner diameter at least 3/16 in. greater than the largest diameter wafer to be counted. The present cup, with an i.d. of 1-3/4 in., is adequate for all wafers normally encountered. A small radius filet is machined into the wall-bottom intersection to reduce electrochemical erosion. The cell depth is 1/4 in. A binding post of electrical connection to the power supply is mounted on the external wall of the cup.

The anode for the cell consists of an independently mounted wire loop with provision for lowering it in a precisely parallel orientation over the wafer contained in the cell. The wire loop at its end, is formed in such a manner that it clears both the microscope objective and the upper edge of the cell wall, yet permits a limited vertical traverse for precise adjustment of displacement over the wafer. The wire is affixed to a metal arm pivoted at its other end for movement in a vertical arc and mounted in a block fashioned from insulating material, such as lucite. Also mounted in the block is a rotatable shaft, parallel to but displaced from the pivot axis. The rotatable shaft

carries an insulating cam in contact with the metal arm which, by means of an external insulating knob, can be manually rotated to adjust the height of the metal arm supporting the wire loop. Means for locking the rotatable shaft in place is provided by a set screw in the insulating block. Electrical connection to the power supply is made directly to the metal arm or to the pivot shaft on which it is mounted. The insulating block on which the adjustable anode is mounted is supported independently of the microscope stage or test cell.

The power supply shall consist of a 50v dc source with 10 to 15K impedance. Provision for the selection of other voltages is desirable if deviations in electrode spacing from that specified herein are anticipated (Note 1).

The hand counter shall consist of a mechanical key type register, or equivalent.

Reagents

Methanol (anhydrous, Reagent Grade)

Hydrofluoric acid (48 percent, Reagent Grade)

Hydrochloric acid (Reagent Grade)

Water (distilled or deionized)

Apiezon wax (or equivalent, for masking)

Trichlorethylene (or other solvent for Apiezon wax)

Procedure

Preparation of sample. -- Keep wafers protected in suitable containers at all times. Handle only at extreme edges, preferably with plastic-tipped tweezers and preferably only in the zone making contact with the quartz boat during oxidation. Avoid as much as possible all mechanical contacts to the surface to be tested (Note 2). Open the back oxide for electrical connection by scribing with a diamond stylus. Alternatively, remove a small area of oxide using Apiezon wax as a mask and hydrofluoric acid (diluted 1:1) as an etchant (Note 3). Carefully rinse off acid, dry, dissolve off Apiezon wax with solvent, follow with isopropanol or acetone rinse, blot dry.

Performance of test (bubble mode). --

1. Set microscope for 50X magnification. Connect the wire loop to the positive terminal of the power supply. Insert wire loop anode into the field and adjust level, by means of the cam control knob, until the top of the loop is exactly in focus. Secure it in this position using the set screw provided.

2. Clamp gold plated brass dish on microscope stage below anode. Connect to the negative terminal of the power supply. Fill dish approximately 3/4 full of methanol from a polyethylene dispensing bottle.

3. Insert wafer into center of dish with scribed (or etched) surface down. Add methanol to top of dish.

4. Slowly raise stage carrying the dish until the previously positioned wire loop anode is immersed and just touches the oxide surface to be tested.

5. Note the fine-adjust drum reading on the vertical traverse mechanism, then lower stage 300μ from this position. This should place the surface of the wafer in focus, rather than the loop anode, because of the refractive effect of the added methanol. For this reason, replace any methanol lost by evaporation over extended periods in order to maintain proper focus (Note 4). Do not readjust stage level, as gap between anode loop and wafer should remain relatively constant (Note 5).

6. Turn on voltage supply. Defects in the oxide are observed as emissions of fine trains of hydrogen bubbles (Note 6) from the wafer surface. Count each emission site as a single oxide defect. Occasionally emission will occur only a short time from a particular site and then stop. This probably is due to gas polarization which prevents fresh methanol from penetrating to the exposed silicon. Count as a defect even if only a momentary emission is observed.

Low counts. -- If less than five counts per field at 50X are observed this is arbitrarily classed as a low count wafer. In this case scan the entire wafer using the x-y adjustment of the mechanical stage to reveal successive fields. Record bubble emission sites on the hand counter. Where extreme variations in defect densities are observed on a single wafer, as sometimes occurs, report only the defect density characteristic of the wafer as a whole, omitting anomalous regions. This may be done using the high count method described below. The reason for this is that anomalously high regions usually are indicative of local irregularities, such as scratches or deformations in the silicon, and are not generally characteristic of the oxidation procedure itself. The presence of anomalous regions, however, should be recorded and the sources sought if recurrent. For analogous reasons the outer edges of the wafer and the portion previously in contact with the quartz boat also should be omitted. A correction for these areas is therefore estimated and deducted from the total area of the wafer. Divide the total count tallied on the counter by the corrected wafer area and report as defects/cm^2.

High counts. -- When five or more counts per field at 50X are observed proceed as follows: count fifteen (15) separate fields located by successive x-y adjustments of the mechanical stage, taking care to avoid anomalous regions. Report the entire tally as defects/cm^2, as there are 15.1 fields (at 50X on the Leitz Ortholux Microscope) per cm^2. Alternatively, count any number or fields not less than ten, maintaining an accurate count of the number of fields. Divide the total defect tally by the number of fields counted, then multiply by 15.1 to obtain defects/cm^2. To obtain standard deviation, record the count of each field independently, sum, take the average and compute average percent deviation therefrom.

7. Turn off voltage supply and lower stage to a point where the cell can be conveniently removed. Grasp wafer carefully with tweezers and lay face up on blotting paper to dry. If three successive tests have been performed,

discard the methanol, which has picked up moisture from the atmosphere and electrolysis products from the test (Note 4). At the same time, clean the test cell and the wire loop electrode as follows: Rinse with hydrochloric acid (diluted with water 1:1) to remove accumulated metal salts; rinse with water; rinse with methanol and allow to dry, or reassembly for next test (Note 7). If wafer is to be reclaimed for further investigation, allow to stand 10 minutes in hydrochloric acid (diluted with water 1:1) to remove deposited salts; rinse thoroughly with water, then with methanol. Allow to dry in dust free environment.

Performance of test (decoration mode). -- In the decoration mode a wire loop electrode of copper, nickle or nichrome is used because the decoration depends on the anodic attack of this electrode. This attack may be accompanied, or preceded, by anodic oxidation of the methanol to formic acid. Thus, the metal salts formed may be hydrates or hydrated formates. Regardless of their exact composition these salts are insoluble in the methanol and, being positively charged, are propelled as colloidal particles away from the wire loop anode. They are attracted to, and collected by, cathodic sites on the wafer surface, namely, oxide defect sites where silicon is exposed as a negative electrode. The process is analogous to electrophoresis and, for this reason, is often referred to as "electrophoretic decoration." The colloidal salts collect in the form of rosettes around each functional defect, thereby providing an enormously magnified marker at the defect site. The defect sites are conveniently observed under low magnification (10X to 20X) and may be counted or photographed. Metal residues corresponding to the anode used remain at the defect sites even after an acid wash, as confirmed by electron microprobe examination. The microprobe therefore can be used as an alternative defect detection method after decoration. The metal residues render the decoration mode unfit for screening purposes but convenient for control and documentation purposes.

Follow steps (1) through (5) as defined for the bubble mode test.

6a. Turn on voltage supply. Slowly traverse the entire wafer by means of the x-y adjustment control knobs of the mechanical stage. Continue until visible build-ups of metal salts have collected around defect sites (approximately ten minutes) using the 50X magnification to monitor the process.

7a. Turn off voltage supply and lower stage to a point where the cell can be conveniently removed. Carefully drain off the methanol, taking care not to disturb the decorations. Using tweezers, gently remove the wafer from the cell and place face up on blotting paper to dry. Clean the cell and electrode as described in previous Step (7). Count the defects according to the most appropriate of the methods described in previous Step (6).

For low defect densities where the entire wafer is counted use wide angle low magnification. Alternatively, photograph the wafer at 3X to 5X magnification and perform the counting analysis on the photograph. Convert all counting data to defects/cm^2. If recovery of the wafer for other investigations is anticipated, clean as described in previous Step (7).

Safety precautions. -- Voltage: The exposed metal surfaces of the test cell and of the wire loop anode and supporting arm, particularly in close proximity to metal parts of the microscope, may constitute a hazard at a potential of 50 v dc. Apply voltage

only during performance of the test, taking care not to touch any charged metal surface. Avoid touching the microscope, or any other metallic object, with the exposed metal surfaces either of the test cell or the wire loop anode. Always check for clearances before turning on voltage. Avoid touching the test cell directly with the wire loop anode while potential is applied. Sparks are produced which damage the plating of the test cell.

Hydrofluoric Acid: Concentrated hydrofluoric acid is a highly caustic liquid, penetrating the skin rapidly and causing deep and painful wounds. It also acts as a systemic poison. Use only in a hood provided with adequate rinsing facilities. Use of rubber gloves is not recommended unless a rigid glove inspection procedure prior to use is adopted.

Solvents: Avoid extended or copious inhalation of methanol vapors which are poisonous. Similarly avoid inhalation of trichlorethylene which may induce temporary "black-out" and has been known to cause liver damage.

Precision

Repeatability generally is within five percent with one operator and one apparatus except for very thin oxides. With different operators using the same apparatus reproducibility may vary as much as 20 percent but can be brought down to around five percent with careful coordination and duplication of test conditions. Reproducibility on different apparatus is not known.

Accuracy

No assessment of accuracy can be made without an exact definition of what constitutes an oxide flaw. Such flaws can be defined functionally on the basis of dielectric breakdown during systems use. Such breakdowns, however, are determined by the path length and the applied voltage, factors which cannot be standardized. The test method likewise makes use of dielectric breakdown at the site of the oxide flaw, standardized empirically at a potential well below the dielectric strength of the oxide but high enough to constitute a significant indicator of oxide quality. In general this potential will exceed by some variable amount the gradients to be encountered in future systems use. Accuracy, therefore, will tend to err on the positive side in inverse proportion to the rigors of use conditions.

Dimensional Limits

Defect size resolution is estimated at 0.5 μ on the basis of electron microscopic evidence. Gas polarization at very small defects often interferes with their detection.

Notes

1. Adjustments in voltage may be required for other variations in test conditions (see Note 4) or for samples where the oxide layers are extremely thin.

2. Gentle wiping of an oxide surface with a cotton swab has been found to increase the defect count, probably by mechanically dislodging some silica fracture chips that would otherwise except detection.

3. Do not remove entire back oxide, as this introduces warp in the wafer and increases the density of observable defects in the remaining oxide layer.

4. Anhydrous methanol absorbs moisture from the air and should be replaced periodically, as detailed in Step (7), rather than made up to volume with incremental additions. Moisture, and accumulated electrolysis products, tend to increase the conductivity which results in increased fields across the oxide under test. Voltage adjustments which could be used to offset these effects cannot be accurately selected on the basis of percent information.

5. The spacing of 300μ was selected to bring the wafer surface into focus at 50X when covered by methanol to the total cup depth. The spacing is somewhat arbitrary with respect to actual current flow and total defect count, effects which are governed mainly by defect diameter and fluid transport to the cathodic silicon surface. Recent evidence indicates the spacing may vary by as much as -30 and +300 percent without seriously affecting the analysis.

6. Identified by gas chromatography.

7. Exercise extreme care in preventing contact of acids or acid fumes with the microscope. Conduct all acid treatments a safe distance from the microscope, preferably in a hood.

APPENDIX B. SUMMARY - FACTORS INFLUENCING DIELECTRIC DEFECTS IN SILICON OXIDE LAYERS*

BY
P. J. BESSER, J. E. MEINHARD, AND P. H. EISENBERG

Abstract

The incidence of dielectric defects in thermally grown silicon oxide films has been investigated utilizing previously developed defect detection techniques. The oxide layers exhibited a strong dependence of dielectric defect density on film thickness, on moisture content of the oxidizing ambient and on type and concentration of the substrate dopant. Characterization of the defects indicates that they are primarily pores in the oxide layer. Mechanical stress resulting from the mismatch in thermal expansion characteristics of the silicon and the oxide is postulated as an important defect-producing mechanism and the experimental results are interpreted on this basis.

Procedures. -- Silicon wafers with various dopant concentrations and procedures were procured and thermally oxidized at temperatures from 1050 C to 1180 C in various ambients. Films were grown in the thickness range from 850 Å to 12,000 Å. Two techniques were utilized for defect detection - electrophorite decoration and electrochemical autograph.

Results. -- Application of previously developed methods for the detection of dielectric defects to silicon oxides formed on silicon wafers has made possible a determination of the dependence of dielectric integrity on various factors involved in device fabrication. Most of the results can be consistently explained by a model which postulates the mechanical stress developed as a result of the thermal expansion mismatch between Si and SiO_2 as a principal source of dielectric failures by the mechanism of film rupture. Other possible defect origins are being investigated but have not been verified.

Below is a detailed discussion of the results obtained in terms of various parameters.

Film thickness. -- The experimental data demonstrated that the dielectric integrity of virgin thermal oxides is strongly thickness dependent. This variation with thickness is shown in Figure B-1 for the average of a typical group of samples oxidized under the same conditions. All of the oxides studied show this same functional dependence of defect density and thickness; but the position and shape of the curve are influenced by a number of factors, some of which are considered in this paper. The number of defects is relatively independent of thickness in the range greater than 4000 Å but generally begins to increase gradually in the 2000-4000 Å range with a very rapid increase below 2000 Å.

*Appendix B is a summary of a paper delivered at the 1966 Fall meeting of the Electrochemical Society, Philadelphia, Pa.

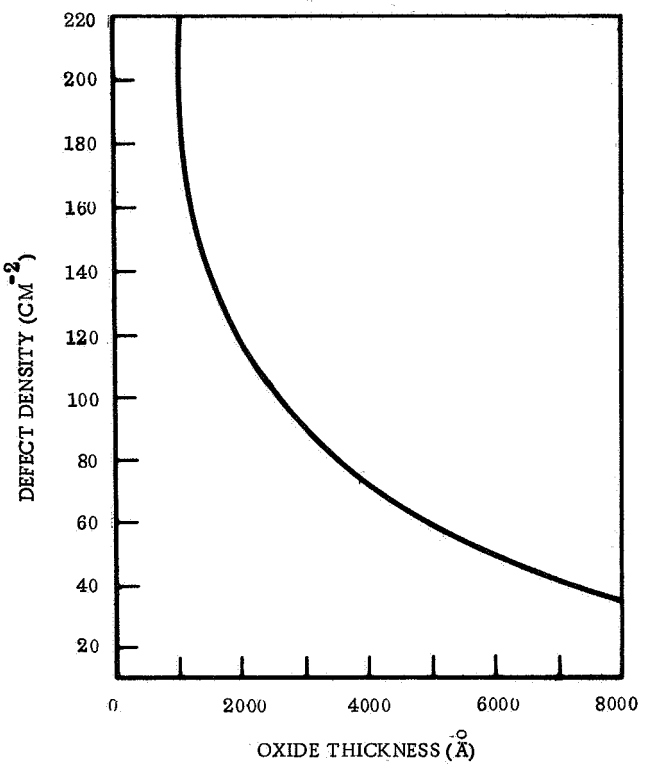

Figure B-1. Defect Density Variation in Virgin Thermal Oxide

Moisture content of oxidizing ambient. -- For oxides of a given thickness, the number of defects/cm^2 was found to be dependent on the amount of water vapor in the oxidizing ambient.

Etched oxide layers. -- The same functional dependence of defect density on thickness that was determined on virgin oxides was also observed in oxide layers as they were thinned by etching. However, the defect density at a particular thickness was greater for the thinned oxide than for the unaltered oxide. When the etched layer is regrown to successively greater thicknesses, the defect density decreases in a manner closely approximating the etch-back curve rather than the curve for the as-grown oxides.

Silicon surface preparation. -- The effect of preoxidation surface treatment of a silicon substrate on defect density was also investigated. The wafers were oxidized under identical conditions and the defects measured on each group. The oxide thickness was 1200 Å and the results indicate that the effect on surface preparation on oxide dielectric integrity is relatively small in this thickness range. The general trend, however, was that oxides grown over surfaces in which the chemical polish was the final step contained fewer defects than those grown on wafers with a final mechanical or mechanical-HCℓ vapor polish.

Oxidation temperature and growth rate. -- A dependence of dielectric integrity upon growth temperature (or growth rate) was observed for oxide layers less than 2000 Å thick grown in dry O_2 over heavily boron-diffused regions. The layers grown at lower

temperatures contained more defects than those of the same thickness grown at higher temperatures. The variation with growth temperature became less as the film thickness increased. The results of the stem and wet N_2 oxidations also indicate an absence of growth rate effects in thicker layers although it may be that the presence of moisture is the dominant influence in wet oxides.

Substrate impurity type and concentration. -- Preliminary work in other phases of this investigation indicated that oxides grown over heavily boron-doped regions in dry O_2 were more defect-free than those grown over regions of low boron concentration or over phorphorous-doped regions. This suggested a possible influence of substrate impurity type and concentration on the integrity of the grown oxide. Since the amount of impurity incorporated in the oxide and the degree of partition of impurity between the oxide and silicon are partially dependent on the growth conditions, it was decided to vary impurity type, impurity concentration, and oxidation conditions on a group of samples to determine the combined influences of impurity and oxidation procedure, densities found and the poorer quality of the etched layers. Also, from previous discussion, terminating with a wet (rapid) oxidation step may produce in the lower portion of the film a higher incidence of substrate-related oxide defects.

Discussion

Consideration of the experimental data from this investigation in conjunction with the present knowledge and conception of the silicon oxide structure and the results of other studies on the properties of SiO_2 and silicate glasses leads to a consistent picture of the nature, structural roots, and process origins of regions of anomalously low dielectric breakdown.

Most of the experimental data can be explained by considering oxide dielectric defects to result from microscopic cracks or fissures in the layer produced by the mechanical stress resulting from the differential thermal expansion characteristics of the Si-SiO_2 system. It should be pointed out that glass always fails from a tensile component of stress even when the loading is compressive. Since the stress originates at the interface between the silicon and the oxide, it is expected that ruptures in the oxide will occur at this boundary and propagate toward the outer surface of the oxide. In thicker films the propagating stress, which should be partially relieved by the rupture of the oxide, may not be sufficient to allow all the defects to penetrate the entire thickness of the layer. This could account for the observed decrease in defect density with increasing oxide thickness. In an oxide grown to any thickness on a silicon wafer, there is presumably a distribution in the local stress levels. Those regions which are just below the rupture level or see only compressive components of stress would be attacked more rapidly by chemical etching. This is thought to be the basis of the higher density of defects in an etched film as compared to a virgin layer of the same thickness. The ineffectiveness of thermal regrowth of oxide as a defect elimination technique is apparently a result of the appearance of additional defects in previously sound oxide as a result of the thermal (and stress) cycling. This was demonstrated by measuring the defects on an initial oxide, taking the wafer through five temperature cycles from room temperature to 1150 C in an inert atmosphere, and remeasuring the defect density. It was found that the temperature cycling produced an order to magnitude increase in the number of dielectric flaws.

The beneficial effect of moisture in the oxidizing ambient is attributed to the incorporation of hydroxyl groups in the oxide and the resulting improvement in the oxide thermal expansion characteristics relative to the silicon. The contribution of this factor to improved oxide dielectric quality can be partly offset by the ion trapping characteristic associated with the exchange of protons for other positive ions at these sites. The variation of the defect density versus thickness characteristic with growth temperature can be explained on the basis of incorporation of more boron in the oxide grown at the higher temperature. This is a result of the increased ratio of oxidation rate constant to diffusion coefficient of the impurity in the silicon as the temperature is increased. Since the setting point of the oxide is ~ 1000 C, the temperature range over which the mechanical stress develops is the same for each oxidation temperature and may even be less for the more heavily boron-doped oxide. The 1100 C oxide should also have a higher expansion coefficient resulting in a lower stress level and fewer ruptures in the film as experimentally observed. Also, as shown in Figures B-2 and B-3, the impurity profile in the oxide is such that the best match in expansion characteristics occurs at the oxide-silicon interface where the stress originates.

The data indicate that the surface preparation techniques investigated had relatively little influence on the oxide integrity. Preliminary work on wafers deliberately contaminated with particles at levels differing by an order of magnitude has shown little variation of oxide integrity with particulate contamination.

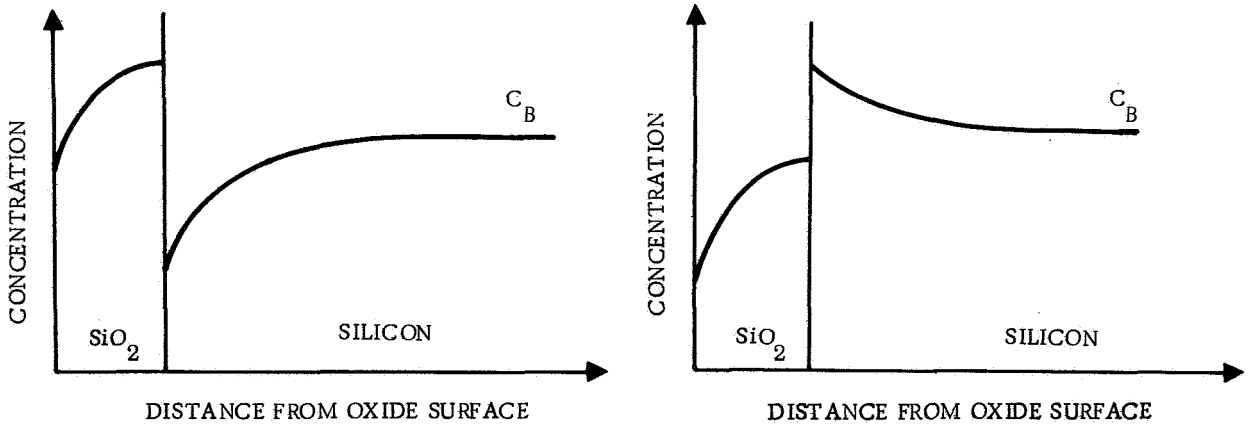

Figure B-2. Impurity Profiles in Oxidized Silicon Wafers. C_B Denoted Bulk Impurity Concentration (From Grove, et al, Ref 20)

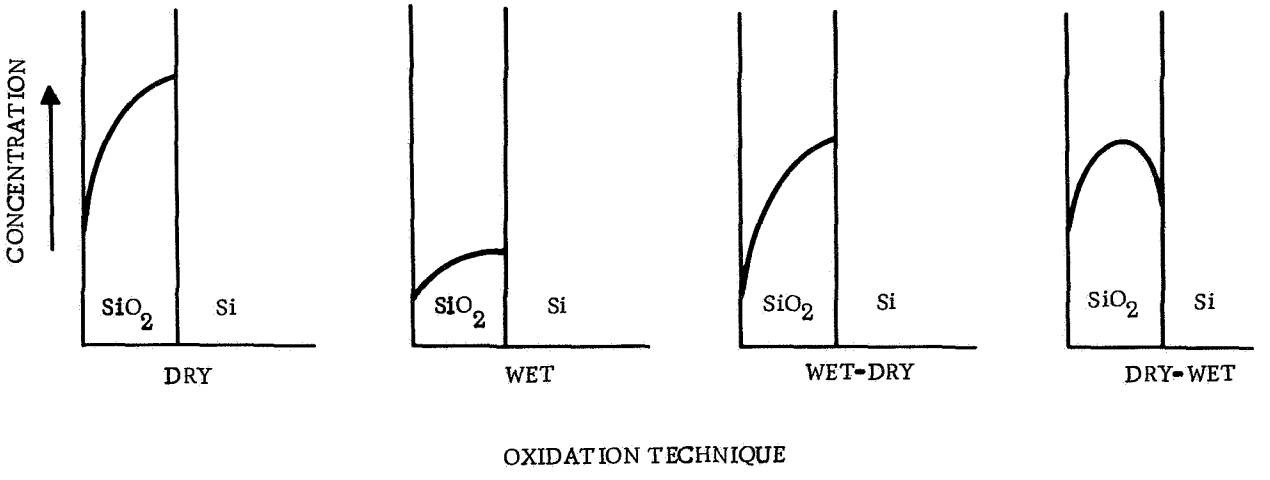

Figure B-3. Postulated Boron Distributions in Thermally Grown Oxides

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APPENDIX C
EVIDENCE OF MECHANICAL STRESS AS A CAUSE OF DIELECTRIC DEFECTS IN SILICON DIOXIDE LAYERS

The presence of compressive stress in room temperature specimens of silicon dioxide grown on silicon at elevated temperatures has been previously recognized (Ref C-1). The effect of this stress has been considered insufficient to affect the band gap and, therefore, the performance of planar silicon devices passivated by such oxide layers (Ref C-2), and correlations with other effects, such as the presence of interface surface states, have been regarded as purely conjectural (Ref C-3). More recently the existence of residual mechanical stress in oxide layers grown on silicon has been confirmed (Ref C-4), and evidence has been advanced implicating this stress in the formation of structural defects in the oxide that are susceptible to dielectric breakdown under the influence of a potential gradient (Ref C-4, C-5). Such defects have the practical effect of severely limiting the fabrication of large area planar arrays on a single silicon chip. Until now no single definitive experiment associating oxide dielectric defects with mechanical stress has been performed.

Compressive stress in grown silicon dioxide layers originates in the fact that the coefficient of linear thermal expansion of silicon is a factor of ~ 10 higher than that of vitreous silica, and in the fact that oxide layers are grown at temperatures ≥ 1000 C followed by cooling to room temperature. Therefore, an etching test for defects on freshly grown oxide prior to cooling, followed by a decoration test (Ref C-4) of defects present after cooling, should yield a direct indication whether a correlation exists between dielectric defect incidence and thermal contraction-induced mechanical stress.

Eight mechanically polished silicon wafers with (111) surfaces were oxidized in a conventional processing furnace in a 1:1 O_2/N_2 atmosphere. Water vapor was carried by the O_2 stream from a reservoir maintained at 100 C. The treatment was continued for 1.5 hr at a temperature of 1150 C producing 8000 Å vitreous oxide layers as determined subsequently be conventional optical interference technique. Water injection then was discontinued and HCℓ gas introduced into the N_2 line at a flow rate sufficient to provide a 0.1 mole ratio in the process gas. However, residual water in the system was present during this treatment. Vapor phase etching in this ambient was continued for 10 min followed by a 40 min flush with N_2 alone. Wafer temperature was held constant within ±0.5 C during the entire sequence, after which the oxide-coated wafers were cooled to room temperature in an inert ambient. Dielectric defects in the oxide layers of each wafer were revealed by a previously developed (Ref C-4) electrophoretic decoration procedure. The defect locations appear as roughly circular deposits. After photographing and counting the defects on each wafer, the decorations were removed with an acid rinse and the vitreous silica layers with hydrofluoric acid. The thoroughly cleansed wafers were then examined microscopically for etch-pits that may have formed in the silicon during the HCℓ treatment.

The results of electrophoretic oxide defect decorations are given in Table C-1. However, in all of the wafers only one etch-pit in the silicon was found by microscopy after removal of the oxide layers. A photomicrograph (Nomarsky phase contrast) of the etch-pit is shown in the center area of Figure C-2. This etch-pit corresponds to one of the total of 195 decorated spots and may have originated from one or more

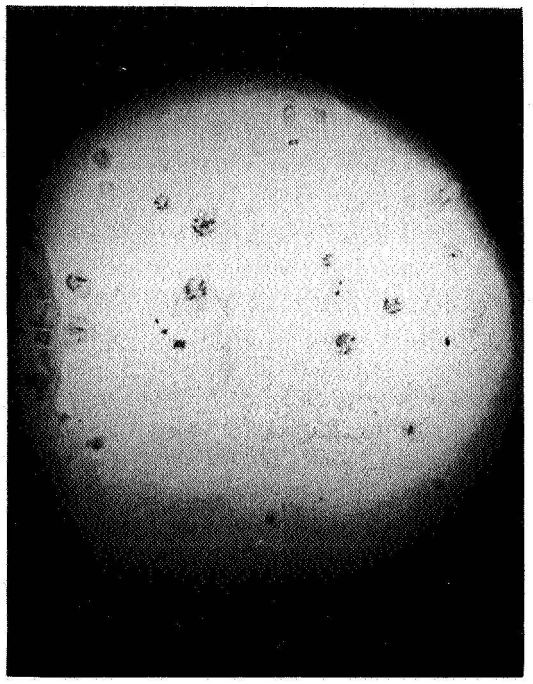

Figure C-1. Oxide Defect Decorations on Silicon Wafer Specimen No. 4 of Table C-1 (Outer Diameter 2.3 cm.)

TABLE C-1
OXIDE DIELECTRIC DEFECTS LOCATED BY ELECTROPHORETIC DECORATION*

Wafer Specimen	Total Defects
1	33
2	27
3	15
4	24
5	28
6	18
7	13
8	27
Total	195

*Procedure given in Reference C-4.

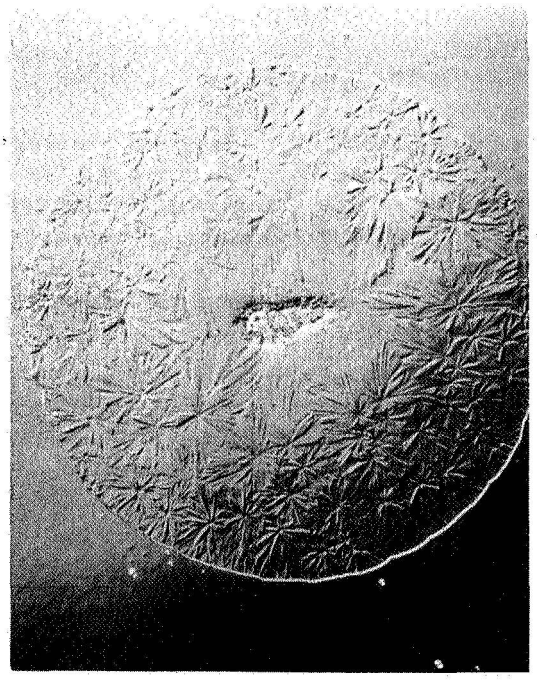

Figure C-2. Etch Pit in Silicon (Center) and Surrounding Structure (Outer Diameter 600μ)

lapping grits originally embedded in the wafer. At present, the crow-foot structure surrounding this pit is an unexplained experimental artifact. However, this pattern has been observed previously (Ref C-6) in studies of HCℓ etching at 1150 C through oxide "pinholes" deliberately introduced by photolithographic procedure. In these previous studies a 5 min rather than a 10 min treatment with HCℓ was used. The structure appears to adopt a three-fold symmetry pattern induced by the (111) surface orientation and may be a region of redeposited (epitaxial silicone). No evidence of the more characteristic triangular etch-pits was found.

It is clear from the foregoing results that there is a better than 99 percent correlation between the formation of silicon dioxide structural defects and the process of wafer cooling from > 1000 C to room temperature. The only obvious origin of this effect is the thermal contraction mismatch between the respective layers. A substantial amount of less direct evidence exists (Ref C-4, C-5) in support of this conclusion.

References

C-1. S.S. Baird, Ann. N.Y. Acad. Sci. 101, 869 (1963).

C-2. J.J. Wortman, J.R. Hauser and R.M. Burger, J. Appl. Phys. 35, 2122 (1964).

C-3. Research Triangle Institute, "Integrated Silicon Device Technology" VII, 143, Technical Report ASD-TDR-63-316 (1965).

C-4. P.J. Besser and J.E. Meinhard, Proceedings of the Symposium on Manufacturing In-Process Control and Measuring Techniques for Semiconductors, Phoenix, Arizona, March 1966, Vol. II, p. 16-1.

C-5. P.J. Besser, J.E. Meinhard and P.H. Eisenberg, Electrochemical Society Meeting, Philadelphia, Pennsylvania, October 10-14, 1966. (To be published.)

C-6. Manufacturing In-Process Control and Measuring Techniques for Integral Electronics, No. 4, IR-8-140 (IV), Motorola, Inc., January, 1965, p 97.

APPENDIX D
MEASUREMENT OF COMPRESSIVE STRESS IN OXIDE LAYERS

The compressive stresses associated with oxide layers of various thicknesses and defect densities are listed in Table D-1. Determinations were made by Proficorder tracing arranged to give both the step thickness of an etch mark and the delta curvature, or deflection, over a given trace distance produced by removal of an oxide layer. From the deflection data the compressive stress is computed using the following relation:

$$\theta_o = 4E_s Z_s^2 d_s / 3Z_o 1^2 \qquad \text{(D-1)}$$

where E_s is the modulus of elasticity of silicon (27.3×10^6 psi), Z_s and Z_o are the thicknesses (inches) of the silicon and oxide layers respectively, d_s is the deflection

TABLE D-1
CORRELATION OF DEFECT DENSITIES WITH OXIDATION AND STRESS

Run	Oxidation		Defects vs Stress (No./Wafer)			Measured Stress[d] (Psi x 10^{-3})
	Time, $t^{1/2}$ (Min)	Thickness (Angstroms)	No Stress[a]	Full Stress[b]	Partial Stress[c]	
A	2.24	1720	131	545	987	40.3
B	3.16	1995	35	511	644	49.5
C	3.87	2590	10	343	479	36.8
D	4.47	3125	5	111	146	40.0
E	5.00	2945	8	170	353	42.1
J	5.00	3760	0.5	205	333	37.3
F	6.32	4010	1	31	140	41.4
G	7.81	5325	0	24	90	42.6
					Av:	41.3 ±6.4%

a. Silicon etch pit count produced before cooling.
b. Decoration count after cooling.
c. Decoration count after removal of back oxide layer.
d. By Proficorder trace method described in text.

produced by oxide removal and 1 is the length of Proficorder traverse, yielding the compressive stress, θ_o, in psi. Mutually perpendicular Proficorder traces were made on each wafer.

Error in these measurements arose from two sources: step thickness determinations (±250 Å) and curvature irregularities in about 50 percent of the Proficorder traces. The thickness error is apparent from Table D-1 where the calculated stresses deviate from the average most for the thinner oxides (i.e., where the measurement error is proportionately greater). There is, however, no apparent change in stress with oxide thickness, as was deduced earlier from more limited evidence. Curvature irregularities were dealt with by area summation technique applied to the regions enclosed by the pre- and post-oxide removal curve traces. This resulted in an improvement of about 50 percent (to 6.4 percent) over earlier computations.

The magnitude of the compressive stress in the oxide (4×10^4 psi) is considered substantial enough to rupture a large proportion of existing thin spots in the oxide in cooling from the oxidation temperature. Other thin spots, although fractured, may be held together by the residual compressive stress and escape detection by electrophoretic decoration. These spots appear in turn to be opened up (i.e., they become detectable by decoration) by the convex curvature and relief of stress introduced by back oxide removal. The convex curvature is, of course, readily apparent from the Proficorder traces.

APPENDIX E. WAFER OXIDE DEFECT DATA (AUTONETICS M&P LABORATORY EXPERIMENTAL WAFERS)

TABLE E-1
DEFECT DENSITIES AS A FUNCTION OF WAFER STRESS

Wafer No.	Oxide Thickness (Å)	Oxidation Time (Min)	No Stress Etch Pits/Wafer	Full Stress Defects/Wafer	Partial Stress Defects/Wafer
1	1720	5	147	900	1436
2	1720	5	108	275	840
3	1720	5	96	338	480
4	1720	5	173	666	1193
1	1995	10	33	284	600
2	1995	10	38	637	786
3	1995	10	31	580	463
4	1995	10	36	543	817
1	2590	15	12	337	479
2	2590	15	14	295	507
3	2590	15	9	401	403
4	2590	15	6	338	527
1	3125	20	6	107	171
2	3125	20	5	101	110
3	3125	20	4	148	132
4	3125	20	4	87	172
1	2945	25	11	174	413
2	2945	25	11	158	291
3	2945	25	8	238	397
4	2945	25	3	110	313

TABLE E-1 (Cont)
DEFECT DENSITIES AS A FUNCTION OF WAFER SITES

Wafer No.	Oxide Thickness (Å)	Oxidation Time (min)	No Stress Etch Pits/Wafer	Full Stress Defects/Wafer	Partial Stress Defects/Wafer
1	3760	25	1	302	379
2	3760	25	0	195	283
3	3760	25	1	158	331
4	3760	25	0	165	308
1	4010	40	0	57	94
2	4010	40	0	27	145
3	4010	40	4	32	118
4	4010	40	0	10	102
1	5325	60	0	88	116
2	5325	60	0	25	104
3	5325	60	0	22	89
4	5325	60	0	26	78

Wafer Area - 3.3 cm^2

TABLE E-2
DEFECT DENSITIES AS A FUNCTION OF PREOXIDATION TREATMENT AND INITIAL OXIDATION RATE

Wafer No.	Oxide Thickness (Å)	Oxidation Time (Min)	Water Temp. (°C)	Defects/Wafer	Slow Oxidation to ~400Å
1	1300	2.5	95	185	No
2	1300	2.5	95	218	No
3	1300	2.5	95	206	No
4	1300	2.5	95	243	No
1	2000	5	95	143	No
2	2000	5	95	143	No
3	2000	5	95	196	No
4	2000	5	95	208	No
1	2700	10	95	109	No
2	2700	10	95	81	No
3	2700	10	95	88	No
4	2700	10	95	73	No
1	3000	15	95	180	No
2	3000	15	95	85	No
3	3000	15	95	72	No
4	3000	15	95	69	No
1	4100	20	95	50	No
2	4100	20	95	56	No
3	4100	20	95	46	No
4	4100	20	95	49	No

TABLE E-2 (Cont)
DEFECT DENSITIES AS A FUNCTION OF PREOXIDATION TREATMENT AND INITIAL OXIDATION RATE

Wafer No.	Oxide Thickness (Å)	Oxidation Time (Min)	Water Temp. (°C)	Defects/Wafer	Slow Oxidation to 400Å
1	5000	30	95	91	No
2	5000	30	95	36	No
3	5000	30	95	42	No
4	5000	30	95	42	No
1	1600	4	37	199	Yes
2	1600	4	37	120	Yes
3	1600	4	37	144	Yes
4	1600	4	37	141	Yes
1	1800	4	32	221	Yes
2	1800	4	32	86	Yes
3	1800	4	32	131	Yes
4	1800	4	32	117	Yes
1	2800	9	34	121	Yes
2	2800	9	34	115	Yes
3	2800	9	34	102	Yes
4	2800	9	34	143	Yes
1	3600Å	16	33	58	Yes
2	3600Å	16	33	76	Yes
3	3600Å	16	33	53	Yes
4	3600Å	16	33	68	Yes

TABLE E-2 (Cont)
DEFECT DENSITIES AS A FUNCTION OF PREOXIDATION TREATMENT AND INITIAL OXIDATION RATE

Wafer No.	Oxide Thickness (Å)	Oxidation Time (Min)	Water Temp. (°C)	Defects/Wafer	Slow Oxidation to 400Å
1	4600	25	35	34	Yes
2	4600	25	35	40	Yes
3	4600	25	35	37	Yes
4	4600	25	35	32	Yes

TABLE E-3
HCl PRE-ETCH DATA

Wafer No.	Estimated Oxide Thickness	Defect Count/Wafer	Etch Pit Count/Wafer	Wet Oxidation 4% O_2 (Min)	HCl Treatment (Min)
1	470Å	3380	142	30	-
2	470Å	3890	50	30	-
3	470Å	1820	71	30	-
4	470Å	1860	119	30	-
1	480Å	1004	14	30	-
2	480Å	1080	3	30	-
3	480Å	1265	21	30	-
4	480Å	2113	6	30	-
1	600Å	1348	20	60	-
2	600Å	820	7	60	-
3	600Å	1570	17	60	-
4	600Å	860	9	60	-
1	650Å	395	0	120	-
2	650Å	380	0	120	-
3	650Å	475	0	120	-
4	650Å	303	0	120	-
1	500Å	633	14	60	1
2	500Å	654	13	60	1
3	500Å	991	16	60	1
4	500Å	283	14	60	1

TABLE E-3 (Cont)
HCℓ PRE-ETCH DATA

Wafer No.	Estimated Oxide Thickness	Defect Count/Wafer	Etch Pit Count/Wafer	Wet Oxidation 4% O_2 (Min)	HCℓ Treatment (Min)
1	500Å	678	8	60	1
2	500Å	410	3	60	1
3	500Å	403	11	60	1
4	500Å	350	5	60	1
1	510Å	880	39	60	1
2	510Å	1120	31	60	1
3	510Å	659	16	60	1
4	510Å	871	40	60	1
1	560Å	144	48	60	1
2	560Å	66	4	60	1
3	560Å	244	9	60	1
4	560Å	194	41	60	1

Wafer Area - 3.18 cm^2
H_2O Temperature - 50 C
Wafer Source - TI.
N_2 Flow Rate - 480 cc/min
Wafer Preclean - HF swab

TABLE E-4
HIGH TEMPERATURE SOAK DATA

Wafer No.	Estimated Oxide Thickness	Defect Count/Wafer	Etch Pit Count/Wafer	~4% Dry O_2 Treatment (min)	Wet Oxidn. (min)	Heat Soak Time (hrs)	Wafer Source	N_2 Flow Rate (cc/min)	Conc. HNO_3 Oxidation	
									Time (min)	Temp (°C)
1	2700Å	59	3	-	20	16	Repolished TI	10	-	-
2	2700Å	41	0	-	20	16	Repolished TI	10	-	-
3	2700Å	51	0	-	20	16	Repolished TI	10	-	-
4	2700Å	48	0	-	20	16	Repolished TI	10	-	-
1	3300Å	9	0	5	20	16	Repolished TI	10	-	-
2	3300Å	20	0	5	20	16	Repolished TI	10	-	-
3	3300Å	39	0	5	20	16	Repolished TI	10	-	-
4	3300Å	4	0	5	20	16	Repolished TI	10	-	-
1	1400Å	69	42	-	5	2	Repolished TI	10	-	-
2	1400Å	37	68	-	5	2	Repolished TI	10	-	-
3	1400Å	43	137	-	5	2	Repolished TI	10	-	-
4	1400Å	35	47		5	2	Repolished TI	10	-	-
1	1550Å	135	25	-	5	2	TI (orig.)	480	-	-
2	1550Å	102	21	-	5	2	TI (orig.)	480	-	-
3	1550Å	107	35	-	5	2	TI (orig.)	480	-	-
4	1550Å	55	22	-	5	2	TI (orig.)	480	-	-
1	1400Å	155	17	-	5	2	TI (orig.)	480	-	-
2	1400Å	146	31	-	5	2	TI (orig.)	480	-	-
3	1400Å	77	28	-	5	2	TI (orig.)	480	-	-
4	1400Å	396	43	-	5	2	TI (orig.)	480	-	-
1	1400Å	857	10	-	5	2	TI (orig.)	480	15	90
2	1400Å	411	77	-	5	2	TI (orig.)	480	15	90
3	1400Å	456	26	-	5	2	TI (orig.)	480	15	90
4	1400Å	327	6	-	5	2	TI (orig.)	480	15	90

TABLE E-4 (Cont)
HIGH TEMPERATURE SOAK DATA

Wafer No.	Estimated Oxide Thickness	Defect Count/Wafer	Etch Pit Count/Wafer	~4% Dry O_2 Treatment (min)	Wet Oxidn. (min)	Heat Soak Time (hrs)	Wafer Source	N_2 Flow Rate (cc/min)	Conc. HNO_3 Oxidation	
									Time (min)	Temp (°C)
1	1300Å	136	2	5	5	2	TI (orig.)	480	-	-
2	1300Å	144	3	5	5	2	TI (orig.)	480	-	-
3	1300Å	140	0	5	5	2	TI (orig.)	480	-	-
4	1300Å	55	3	5	5	2	TI (orig.)	480	-	-
1	3200Å	89	0	5	20	2	TI (orig.)	480	-	-
2	3200Å	20	0	5	20	2	TI (orig.)	480	-	-
3	3200Å	64	0	5	20	2	TI (orig.)	480	-	-
4	3200Å	64	0	5	20	2	TI (orig.)	480	-	-
1	1200Å	226	43	-	5	16	TI_{225}	480	-	-
2	1200Å	257	37	-	5	16	TI_{225}	480	-	-
3	1200Å	310	57	-	5	16	TI_{225}	480	-	-
4	1200Å	256	96	-	5	16	TI_{225}	480	-	-
1	2200Å	35	7	5	5	16	TI_{225}	480	-	-
2	2200Å	36	4	5	5	16	TI_{225}	480	-	-
3	2200Å	16	3	5	5	16	TI_{225}	480	-	-
4	2200Å	44	9	5	5	16	TI_{225}	480	-	-

Wafer Area - 3.18 cm^2
H_2O Temperature - 90 -94°C
Wafer Preclean - HF swab

TABLE E-4 (Cont)
HIGH TEMPERATURE SOAK DATA

Wafer No.	Estimated Oxide Thickness	Defect Count/Wafer	Etch Pit Count/Wafer	~4% Dry O_2 Treatment (min)	Wet Oxide (min)	Heat Soak Time (min)	Wafer Source	N_2 Flow Rate (cc/min)	Conc. HNO_3 Oxidation	
									Time (min)	Temp (°C)
1	3100Å	52	2	-	20	2	TI (orig.)	480	-	-
2	3100Å	35	16	-	20	2	TI (orig.)	480	-	-
3	3100Å	33	10	-	20	2	TI (orig.)	480	-	-
4	3100Å	33	11	-	20	2	TI (orig.)	480	-	-
1	3000Å	80	11	-	20	2	TI (orig.)	480	15	90
2	3000Å	140	13	-	20	2	TI (orig.)	480	15	90
3	3000Å	45	1	-	20	2	TI (orig.)	480	15	90
4	3000Å	105	9	-	20	2	TI (orig.)	480	15	90
1	3100Å	23	0	-	20	2	TI (orig.)	10	-	-
2	3100Å	35	0	-	20	2	TI (orig.)	10	-	-
3	3100Å	112	147	-	20	2	TI (orig.)	10	-	-
4	3100Å	32	2	-	20	2	TI (orig.)	10	-	-
1	3000Å	18	3	5	20	2	TI (orig.)	10	-	-
2	3000Å	32	0	5	20	2	TI (orig.)	10	-	-
3	3000Å	60	1	5	20	2	TI (orig.)	10	-	-
4	3000Å	75	1	5	20	2	TI (orig.)	10	-	-
1	2900Å	13	1	-	20	2	TI (orig.)	480	-	-
2	2900Å	22	0	-	20	2	TI (orig.)	480	-	-
3	2900Å	9	0	-	20	2	TI (orig.)	480	-	-
4	2900Å	12	0	-	20	2	TI (orig.)	480	-	-
1	1700Å	99	0	5	5	2	TI (orig.)	10	-	-
2	1700Å	29	1	5	5	2	TI (orig.)	10	-	-
3	1700Å	57	7	5	5	2	TI (orig.)	10	-	-
4	1700Å	32	0	5	5	2	TI (orig.)	10	-	-

TABLE E-5
HCℓ PRETREATMENT DATA

Wafer No.	Estimated Oxide Thickness	Defect Count/Wafer	Etch Pit Count/Wafer	Wet Oxidn. (Min)	cm^2/Wafer	Wafer Source	HCℓ Treatment (Min)
1	3200Å	27	82	20	5.4	TI_{225}	2
2	3200Å	16	116	20	5.4	TI_{225}	2
3	3200Å	58	174	20	5.4	TI_{225}	2
4	3200Å	115	233	20	5.4	TI_{225}	2
1	2300Å	20	72	5	5.4	TI_{225}	2
2	2300Å	34	98	5	5.4	TI_{225}	2
3	2300Å	40	125	5	5.4	TI_{225}	2
4	2300Å	45	77	5	5.4	TI_{225}	2
1	3300Å	16	48	20	5.4	TI_{225}	1
2	3300Å	44	120	20	5.4	TI_{225}	1
3	3300Å	43	76	20	5.4	TI_{225}	1
4	3300Å	20	37	20	5.4	TI_{225}	1
1	1900Å	91	129	5	5.4	TI_{225}	1
2	1900Å	85	87	5	5.4	TI_{225}	1
3	1900Å	74	47	5	5.4	TI_{225}	1
4	1900Å	92	50	5	5.4	TI_{225}	1

TABLE E-5 (Cont)
HCℓ PRETREATMENT DATA

Wafer No.	Estimated Oxide Thickness	Defect Count/Wafer	Etch Pit Count/Wafer	Wet Oxidn. (Min)	cm^2/Wafer	Wafer Source	HCℓ Treatment (Min)
1	2600Å	75	-	10	5.4	TI_{225}	-
2	2600Å	52	-	10	5.4	TI_{225}	-
3	2600Å	70	-	10	5.4	TI_{225}	-
4	2600Å	68	-	10	5.4	TI_{225}	-
1	4500Å	22	-	40	3.18	Repolished TI	-
2	4500Å	26	-	40	3.18	Repolished TI	-
3	4500Å	15	-	40	3.18	Repolished TI	-
4	4500Å	13	-	40	3.18	Repolished TI	-
1	6100Å	18	-	80	3.18	Repolished TI	-
2	6100Å	6	-	80	3.18	Repolished TI	-
3	6100Å	11	-	80	3.18	Repolished TI	-
4	6100Å	12	-	80	3.18	Repolished TI	-

Wafer Area - 5.4 cm^2
H_2O Temperature - 90 C
Wafer Preclean - HF swab
Heat Soak Time - 16 hr
4% Dry O_2 Treatment - 5 minutes

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APPENDIX F
WAFER OXIDE DEFECT DATA
(VENDOR WAFERS)

VENDOR A. OXIDIZED WAFERS (10,000Å)

Lot No.	Wafer No.	Defect Count/Wafer	Lot No.	Wafer No.	Defect Count/Wafer
63574	2	0	62575	1	0
	3	0		2	0
	4	1		3	0
	5	1		4	0
	6	0		5	0
	7	0		6	0
	8	0		7	0
	9	0		8	0
	11	0		9	0
	12	0		10	0
				11	0
				12	0
				13	1
				14	0
				15	1
				16	0
				17	0
				18	2
				19	0
				20	0
				21	0
				22	0
				23	1
				24	0
				25	2
				26	0
				27	0
				28	1

VENDOR B. OXIDIZED WAFER (10,000Å)

Lot No.	Wafer No.	Defects/Wafer
E915	1	11
	2	3
	3	5
	4	4
	5	4
	6	10
	7	10
	8	6
	9	5
	10	8
	11	19
473	1	3
	2	4
	3	9
	4	0
	5	5
	6	0
	7	0
	8	1
	9	6
	10	7
511	1	8
	2	11
	3	13
	4	4
	5	5
	6	0
	7	13
	8	8
	9	11
	10	7
	11	8

VENDOR C. OXIDIZED WAFERS (10,000Å)

Lot No.	Wafer No.	Defects/Wafer	Lot No.	Wafer No.	Defects/Wafer
SO-20225	1	8	SR-5818	1	2
	2	9	(Ox. Date	2	0
	3	1		3	4
	4	1		4	5
	5	3		5	2
	6	1		6	10
	7	7		7	1
	8	1		8	0
	9	3		9	2
	10	5		10	0
	11	2			
	12	3			
	13	3	(Ox. Date	11	14
	14	4		12	17
	15	7		13	6
	16	2		14	19
	17	7		15	36
	18	1		16	41
	19	10		17	4
	20	9		18	11
	21	3		19	15
	22	11		20	14
	23	1			
	24	2			
	25	1			
	26	2			
	27	2			
	28	7			
	29	4			
	30	4			

APPENDIX G
WAFER OXIDE DEFECT DATA
AUTONETICS MOS DEVICE PILOT LINE

Ref. Code	Wafer No.	Thick	Thin	Edge	Ckt Count
		E-1			
E-1	1	0	1	0	454
	2	4	1	0	454
	3	1	2	0	453
	4	3	2	2	438
	5	2	1	1	450
		E-2			
E-2	1	5	1	0	430
	2	1	1	1	437
	3	5	3	1	437
	4	2	1	1	436
	5	3	2	0	428
		I-3 Interim			
I-3	1	7	7	4	449
	2	2	13	8	481
	3	4	10	6	480
	4	13	7	6	432
	5	2	13	6	465
		S-3 Std.			
S-3	1	9	2	5	435
	2	11	2	3	456
	3	1	0	1	429
	4	10	3	2	434
	5	6	5	6	459
		E-3			
E-3	1	3	4	3	435
	2	5	7	4	449
	3	24	1	3	430
	4	3	0	2	434
	5	3	1	1	470
		I-1 Interim Process			
I-1	1	1	2	1	404
	2	6	5	2	426
	3	1	3	1	408
	4	2	2	4	481
	5	3	1	2	411

Ref. Code	Wafer No.	Thick	Thin	Edge	Ckt Count
		I-2			
I-2	1	4	7	3	463
	2	4	4	5	402
	3	0	3	7	398
	4	3	1	4	454
	5	2	6	7	446
		S-1 Std. Process			
S-1	1	1	9	4	468
	2	9	8	4	435
	3	2	6	6	486
	4	2	4	3	453
	5	4	2	1	380
		S-2 Std. Process			
S-2	1	9	2	6	412
	2	11	2	2	478
	3	16	2	5	437
	4	4	3	3	384
	5	5	0	0	470

Thick Oxide

Ref. Code	Thick Oxide Area (sq. cm./ circuit)	Number Circuits	Total Thick Oxide Area per Wafer (sq. cm.)	Defects per Wafer	Defects/sq. cm.
			I-1 Interim		
I-1	7.14×10^{-3}	4.04×10^{2}	2.88	1	
	7.14×10^{-3}	4.26×10^{2}	3.04	6	
	7.14×10^{-3}	4.08×10^{2}	2.92	1	13/15.21 = 0.85
	7.14×10^{-3}	4.81×10^{2}	3.43	2	
	7.14×10^{-3}	4.11×10^{2}	2.94	3	
			15.21	13	
			I-2 Interim		
I-2	7.14×10^{-3}	4.62×10^{2}	3.31	4	
	7.14×10^{-3}	4.02×10^{2}	2.88	4	
	7.14×10^{-3}	3.98×10^{2}	2.84	0	13/15.45 = 0.84
	7.14×10^{-3}	4.54×10^{2}	3.24	3	
	7.14×10^{-3}	4.46×10^{2}	3.18	2	
			15.45	13	
			S-1 Standard		
S-1	7.14×10^{-3}	4.68×10^{2}	3.34	1	
	7.14×10^{-3}	4.35×10^{2}	3.10	9	
	7.14×10^{-3}	4.86×10^{2}	3.46	2	18/15.84 = 1.14
	7.14×10^{-3}	4.53×10^{2}	3.23	2	
	7.14×10^{-3}	3.80×10^{2}	2.71	4	
			15.84	18	
			S-2 Standard		
S-2	7.14×10^{-3}	4.12×10^{2}	2.94	9	
	7.14×10^{-3}	4.78×10^{2}	3.41	11	
	7.14×10^{-3}	4.37×10^{2}	3.12	16	45/15.57 = 2.89
	7.14×10^{-3}	3.84×10^{2}	2.74	4	
	7.14×10^{-3}	4.70×10^{2}	3.36	5	
			15.57	45	

Thick Oxide

Ref. Code	Thick Oxide Area (sq. cm./ circuit)	Number Circuits	Total Thick Oxide Area per Wafer (sq. cm.)	Defects per Wafer	Defects/sq. cm.
		E-1			
E-1	7.14×10^{-3}	4.54×10^{2}	3.24	0	
	7.14×10^{-3}	4.54×10^{2}	3.24	4	
	7.14×10^{-3}	4.53×10^{2}	3.23	1	10/16.05 x 0.623
	7.14×10^{-3}	4.38×10^{2}	3.13	3	
	7.14×10^{-3}	4.50×10^{2}	3.21	2	
			16.05	10	
		E-2			
E-2	7.14×10^{-3}	4.30×10^{2}	3.07	5	
	7.14×10^{-3}	4.37×10^{2}	3.12	1	
	7.14×10^{-3}	4.37×10^{2}	3.12	5	16/15.48 = 1.03
	7.14×10^{-3}	4.36×10^{2}	3.11	2	
	7.14×10^{-3}	4.28×10^{2}	3.06	3	
			15.48	16	
		I-3 Interim			
I-3	7.14×10^{-3}	4.49×10^{2}	3.20	7	
	7.14×10^{-3}	4.81×10^{2}	3.42	2	
	7.14×10^{-3}	4.80×10^{2}	3.42	4	28/16.44 = 1.70
	7.14×10^{-3}	4.32×10^{2}	3.08	13	
	7.14×10^{-3}	4.65×10^{2}	3.32	2	
			16.44	28	
		S-3 Standard			
S-3	7.14×10^{-3}	4.35×10^{2}	3.10	9	
	7.14×10^{-3}	4.56×10^{2}	3.25	11	
	7.14×10^{-3}	4.29×10^{2}	3.06	1	37/15.79 = 2.34
	7.14×10^{-3}	4.34×10^{2}	3.10	10	
	7.14×10^{-3}	4.59×10^{2}	3.28	6	
			15.79	37	
		E-3			
E-3	7.14×10^{-3}	4.35×10^{2}	3.10	3	
	7.14×10^{-3}	4.49×10^{2}	3.20	5	
	7.14×10^{-3}	4.30×10^{2}			14/12.76 = 1.1
	7.14×10^{-3}	4.34×10^{2}	3.10	3	
	7.14×10^{-3}	4.70×10^{2}	3.36	3	
			12.76	14	

Thin Oxide

Ref. Code	Wafer No.	Capacitor Area (sq. cm.)	Number Circuits	Total Cap. Area per Wafer (sq. cm.)	Defects/ Wafers	Defects/sq. cm.
			E-1			
E-1	1	4.13×10^{-4}	4.54×10^{2}	18.7×10^{-2}	1	
	2	4.13×10^{-4}	4.54×10^{2}	18.7×10^{-2}	1	
	3	4.13×10^{-4}	4.53×10^{2}	18.7×10^{-2}	2	$7/92.8 \times 10^{-2} = 7.54$
	4	4.13×10^{-4}	4.38×10^{2}	18.1×10^{-2}	2	
	5	4.13×10^{-4}	4.50×10^{2}	18.6×10^{-2}	1	
				92.8×10^{-2}	7	
			E-2			
E-2	1	4.12×10^{-4}	4.30×10^{2}	17.7×10^{-2}	1	
	2	4.12×10^{-4}	4.37×10^{2}	18.1×10^{-2}	1	
	3	4.12×10^{-4}	4.37×10^{2}	18.1×10^{-2}	3	$8/89.7 \times 10^{-2} = 8.92$
	4	4.12×10^{-4}	4.36×10^{2}	18.1×10^{-2}	1	
	5	4.12×10^{-4}	4.28×10^{2}	17.7×10^{-2}	2	
				89.7×10^{-2}	8	
			I-3 Interim			
I-3	1	4.13×10^{-4}	4.49×10^{2}	18.5×10^{-2}	7	
	2	4.13×10^{-4}	4.81×10^{2}	19.8×10^{-2}	13	
	3	4.13×10^{-4}	4.80×10^{2}	19.8×10^{-2}	10	$50/95.2 \times 10^{-2} = 52.52$
	4	4.13×10^{-4}	4.32×10^{2}	17.9×10^{-2}	7	
	5	4.13×10^{-4}	4.65×10^{2}	19.2×10^{-2}	13	
				95.2×10^{-2}	50	
			S-3 Standard			
S-3	1	4.13×10^{-4}	4.35×10^{2}	18.0×10^{-2}	2	
	2	4.13×10^{-4}	4.56×10^{2}	18.8×10^{-2}	2	
	3	4.13×10^{-4}	4.29×10^{2}	17.7×10^{-2}	0	$12/91.4 \times 10^{-2} = 13.1$
	4	4.13×10^{-4}	4.34×10^{2}	17.9×10^{-2}	3	
	5	4.13×10^{-4}	4.59×10^{2}	19.0×10^{-2}	5	
				91.4×10^{-2}	12	
			E-3			
E-3	1	4.13×10^{-4}	4.35×10^{2}	18.0×10^{-2}	4	
	2	4.13×10^{-4}	4.49×10^{2}	18.5×10^{-2}	7	
	3	4.13×10^{-4}	4.30×10^{2}	17.8×10^{-2}	1	$13/91.6 \times 10^{-2} = 14.19$
	4	4.13×10^{-4}	4.34×10^{2}	17.9×10^{-2}	0	
	5	4.13×10^{-4}	4.70×10^{2}	19.4×10^{-2}	1	
				91.6×10^{-2}	13	

Thin Oxide

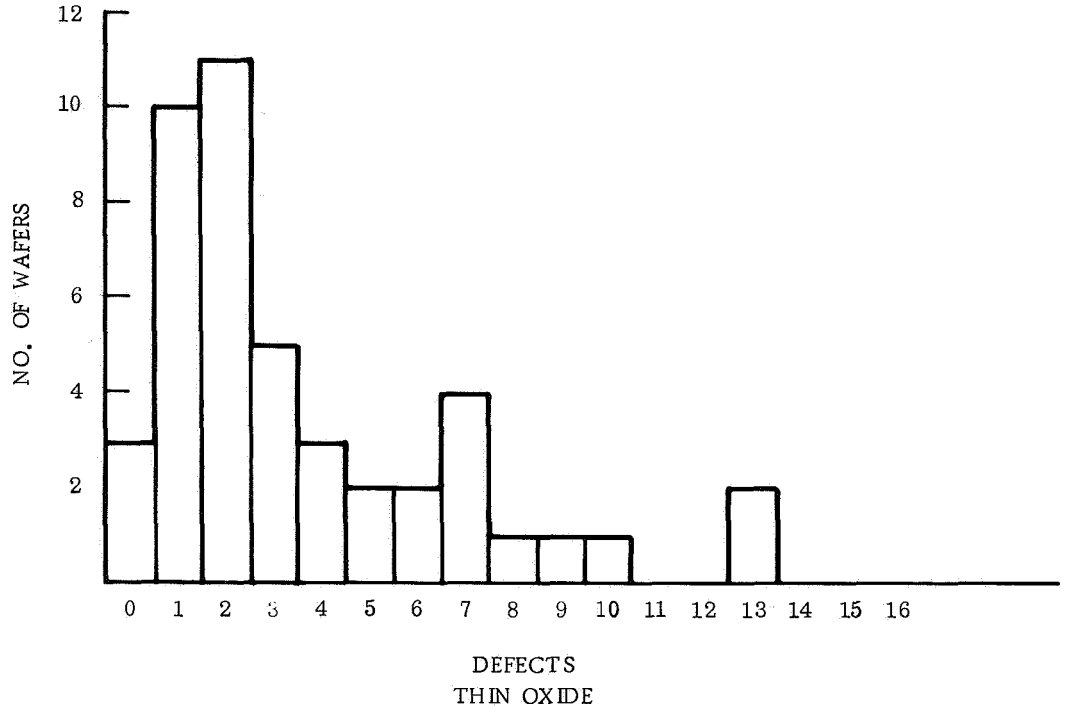
Ref. Code	Wafer No.	Capacitor Area (sq. cm.)	Number Circuits	Total Cap. Area per Wafer (sq. cm.)	Defects/ Wafers	Defects/sq. cm.
			I-1 Interim			
I-1	1	4.13×10^{-4}	4.04×10^{2}	16.7×10^{-2}	2	
	2	4.13×10^{-4}	4.26×10^{2}	17.6×10^{-2}	5	
	3	4.13×10^{-4}	4.08×10^{2}	16.8×10^{-2}	3	$13/87.8 \times 10^{-2} = 14.81$
	4	4.13×10^{-4}	4.81×10^{2}	19.8×10^{-2}	2	
	5	4.13×10^{-4}	4.11×10^{2}	16.9×10^{-2}	1	
				87.8×10^{-2}	13	
			I-2 Interim			
I-2	1	4.13×10^{-4}	4.63×10^{2}	19.1×10^{-2}	7	
	2	4.13×10^{-4}	4.02×10^{2}	16.6×10^{-2}	4	
	3	4.13×10^{-4}	3.98×10^{2}	16.4×10^{-2}	3	$21/89.2 \times 10^{-2} = 23.54$
	4	4.13×10^{-4}	4.54×10^{2}	18.7×10^{-2}	1	
	5	4.13×10^{-4}	4.46×10^{2}	18.4×10^{-2}	6	
				89.2×10^{-2}	21	
			S-1 Standard			
S-1	1	4.13×10^{-4}	4.68×10^{2}	18.9×10^{-2}	9	
	2	4.13×10^{-4}	4.35×10^{2}	17.5×10^{-2}	8	
	3	4.13×10^{-4}	4.86×10^{2}	19.6×10^{-2}	6	$29/89.6 \times 10^{-2} = 32.37$
	4	4.13×10^{-4}	4.53×10^{2}	18.3×10^{-2}	4	
	5	4.13×10^{-4}	3.80×10^{2}	15.3×10^{-2}	2	
				89.6×10^{-2}	29	
			S-2 Standard			
S-2	1	4.13×10^{-4}	4.12×10^{2}	16.6×10^{-2}	2	
	2	4.13×10^{-4}	4.78×10^{2}	19.3×10^{-2}	2	
	3	4.13×10^{-4}	4.37×10^{2}	17.6×10^{-2}	2	$9/87.9 \times 10^{-2} = 10.2$
	4	4.13×10^{-4}	3.84×10^{2}	15.5×10^{-2}	3	
	5	4.13×10^{-4}	4.70×10^{2}	18.9×10^{-2}	0	
				87.9×10^{-2}	9	

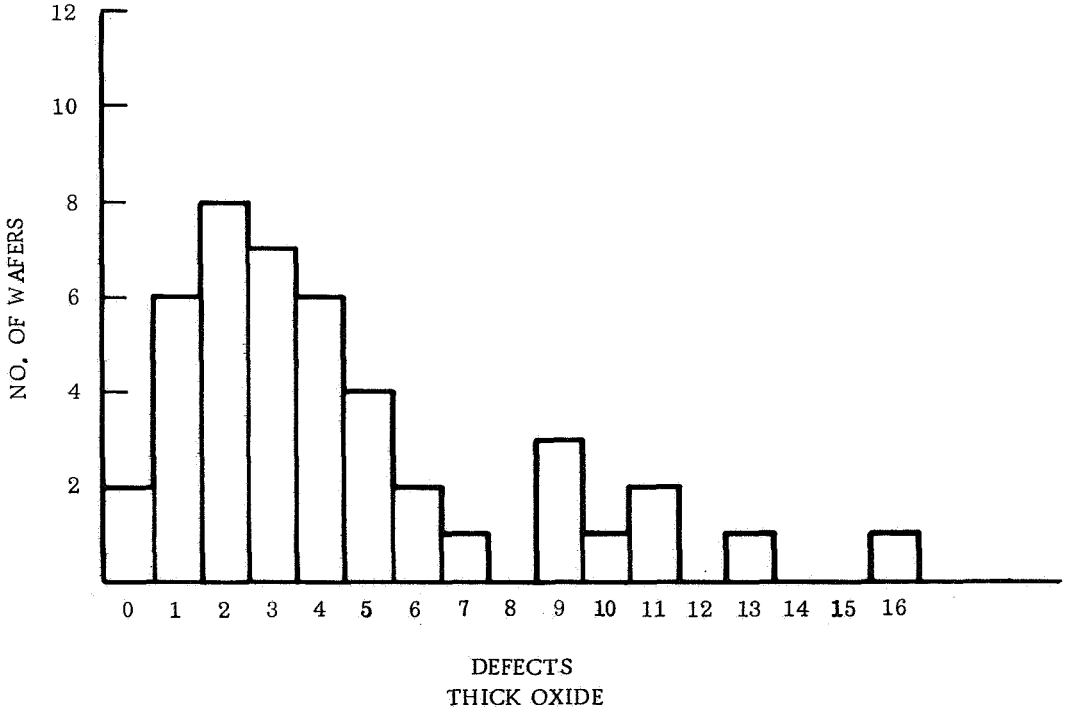
Oxide Step

Ref. Code	Wafer No.	Lineal Length per Capacitor (cm)	Number Circuits	Total Lineal Length/Wafer (cm)	Defects per Wafer	Defect per cm. Lineal Length $\times 10^{-2}$
			I-1 Interim			
I-1	1	8.13×10^{-2}	4.04×10^{2}	32.8	1	3.05×10^{-2}
	2	8.13×10^{-2}	4.26×10^{2}	34.6	2	5.78×10^{-2}
	3	8.13×10^{-2}	4.08×10^{2}	33.2	1	3.02×10^{-2}
	4	8.13×10^{-2}	4.81×10^{2}	39.1	4	10.2×10^{-2}
	5	8.13×10^{-2}	4.11×10^{2}	33.4	2	6.0×10^{-2}
			I-2 Interim			
I-2	1	8.13×10^{-2}	4.63×10^{2}	37.7	3	7.98×10^{-2}
	2	8.13×10^{-2}	4.02×10^{2}	32.7	5	15.3×10^{-2}
	3	8.13×10^{-2}	3.98×10^{2}	32.4	7	21.6×10^{-2}
	4	8.13×10^{-2}	4.54×10^{2}	36.9	4	10.9×10^{-2}
	5	8.13×10^{-2}	4.46×10^{2}	36.3	7	19.3×10^{-2}
			S-1 Standard			
S-1	1	8.13×10^{-2}	4.68×10^{2}	38.1	4	10.5×10^{-2}
	2	8.13×10^{-2}	4.35×10^{2}	35.4	4	11.3×10^{-2}
	3	8.13×10^{-2}	4.86×10^{2}	39.5	6	15.2×10^{-2}
	4	8.13×10^{-2}	4.53×10^{2}	34.8	3	8.63×10^{-2}
	5	8.13×10^{-2}	3.80×10^{2}	30.9	1	3.24×10^{-2}
			S-2 Standard			
S-2	1	8.13×10^{-2}	4.12×10^{2}	33.5	6	17.9×10^{-2}
	2	8.13×10^{-2}	4.78×10^{2}	38.8	2	5.15×10^{-2}
	3	8.13×10^{-2}	4.37×10^{2}	35.6	5	14.0×10^{-2}
	4	8.13×10^{-2}	3.84×10^{2}	31.2	3	9.64×10^{-2}
	5	8.13×10^{-2}	4.70×10^{2}	38.2	0	0.0

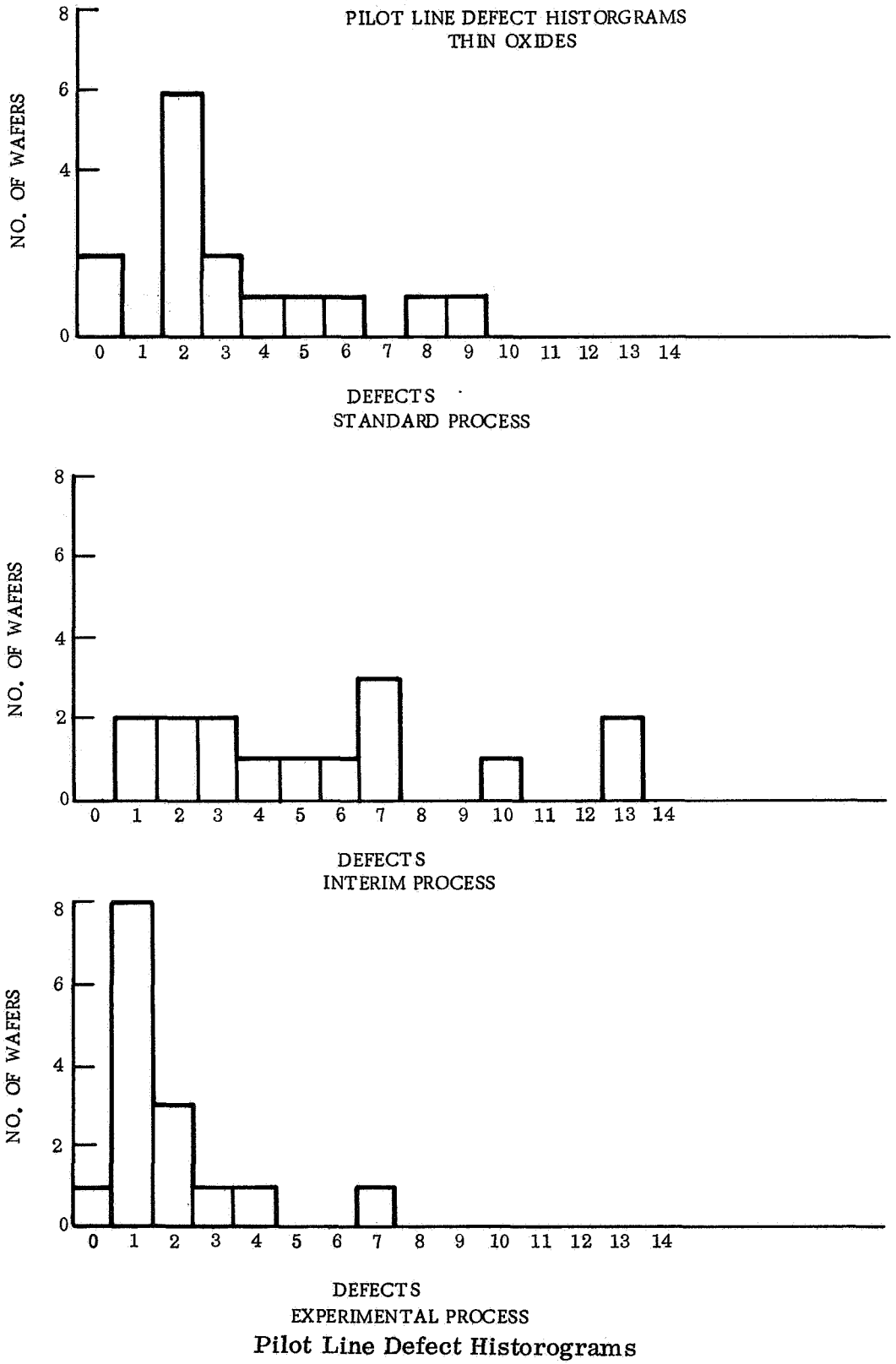
Oxide Step

Ref. Code	Wafer No.	Lineal Length per Capacitor (cm)	Number Circuits	Total Lineal Length/Wafer (cm)	Defects per Wafer	Defects per cm. Lineal Length x 10^{-2}
			E-1			
E-1	1	8.13×10^{-2}	4.54×10^{2}	36.9	0	0
	2	8.13×10^{-2}	4.54×10^{2}	36.9	0	0
	3	8.13×10^{-2}	4.53×10^{2}	36.8	0	0
	4	8.13×10^{-2}	4.38×10^{2}	35.6	2	5.6×10^{-2}
	5	8.13×10^{-2}	4.50×10^{2}	36.6	1	3.0×10^{-2}
			E-2			
E-2	1	8.13×10^{-2}	4.30×10^{2}	34.9	0	0
	2	8.13×10^{-2}	4.37×10^{2}	35.5	1	2.82×10^{-2}
	3	8.13×10^{-2}	4.37×10^{2}	35.5	1	2.82×10^{-2}
	4	8.13×10^{-2}	4.36×10^{2}	35.4	1	2.83×10^{-2}
	5	8.13×10^{-2}	4.28×10^{2}	34.8	0	0
			I-3 Interim			
I-3	1	8.13×10^{-2}	4.49×10^{2}	36.5	4	11.0×10^{-2}
	2	8.13×10^{-2}	4.81×10^{2}	39.1	8	20.5×10^{-2}
	3	8.13×10^{-2}	4.80×10^{2}	39.0	6	15.4×10^{-2}
	4	8.13×10^{-2}	4.32×10^{2}	35.0	6	17.1×10^{-2}
	5	8.13×10^{-2}	4.65×10^{2}	37.8	6	15.9×10^{-2}
			S-3 Standard			
S-3	1	8.13×10^{-2}	4.35×10^{2}	35.3	5	14.2×10^{-2}
	2	8.13×10^{-2}	4.56×10^{2}	37.1	3	8.1×10^{-2}
	3	8.13×10^{-2}	4.29×10^{2}	34.9	1	2.87×10^{-2}
	4	8.13×10^{-2}	4.34×10^{2}	35.2	2	5.68×10^{-2}
	5	8.13×10^{-2}	4.59×10^{2}	37.3	6	16.1×10^{-2}
			E-3			
E-3	1	8.13×10^{-2}	4.35×10^{2}	35.4	3	8.5×10^{-2}
	2	8.13×10^{-2}	4.49×10^{2}	36.4	4	11.0×10^{-2}
	3	8.13×10^{-2}	4.30×10^{2}	35.0	3	8.6×10^{-2}
	4	8.13×10^{-2}	4.34×10^{2}	35.3	2	5.67×10^{-2}
	5	8.13×10^{-2}	4.70×10^{2}	38.2	1	2.62×10^{-2}

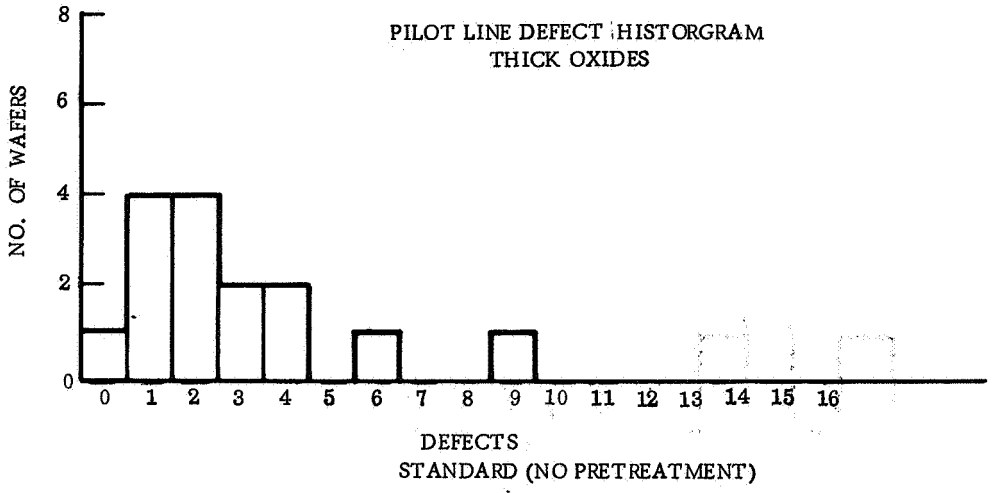


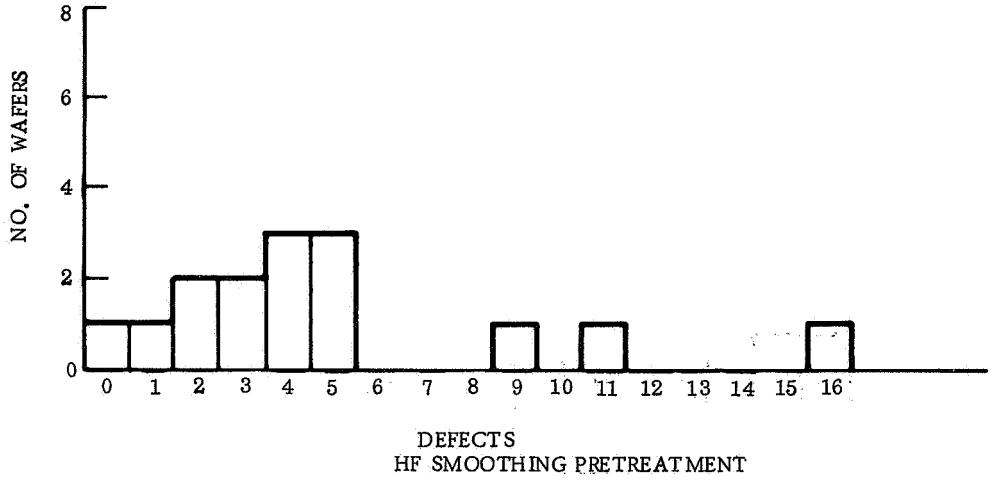


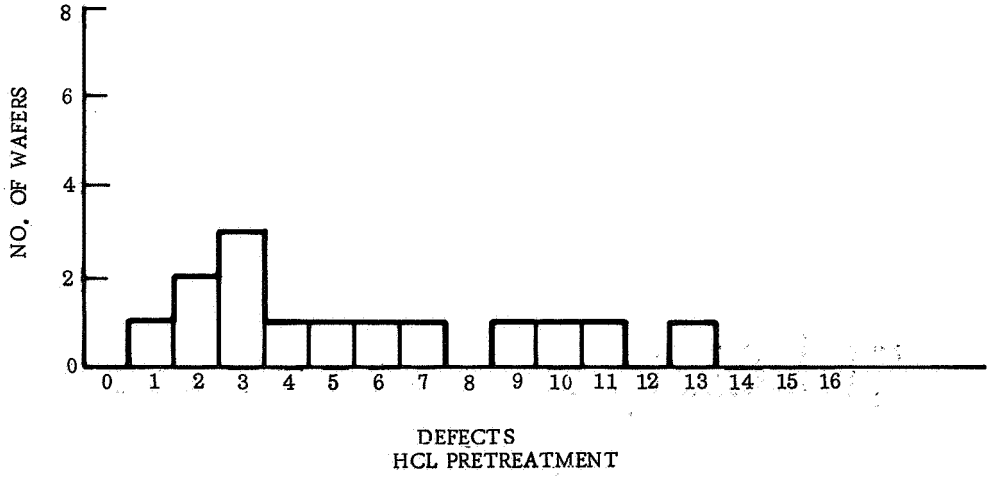
Pilot Line Defect Historograms



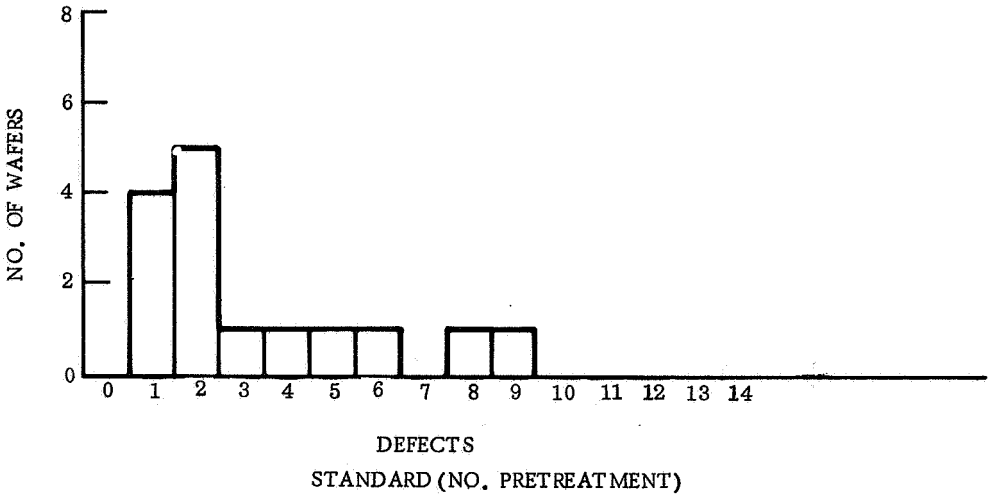
Pilot Line Defect Historograms

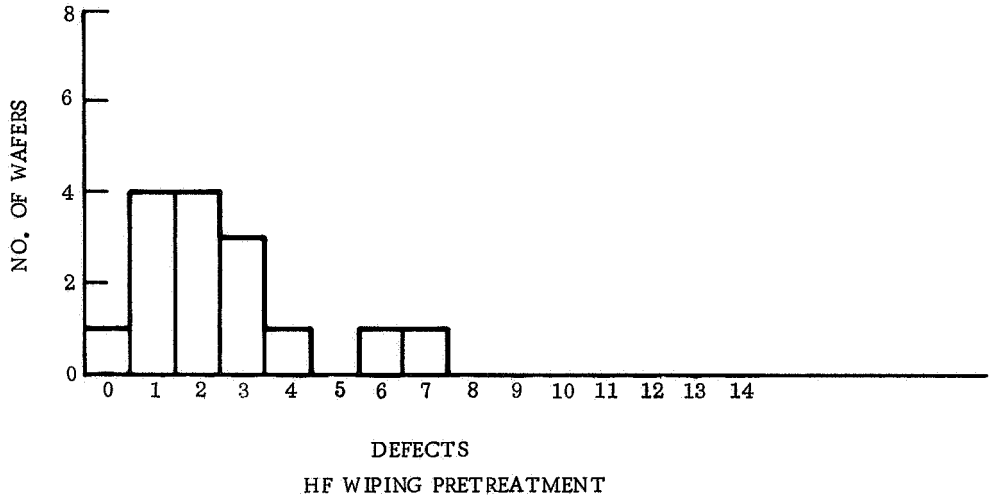


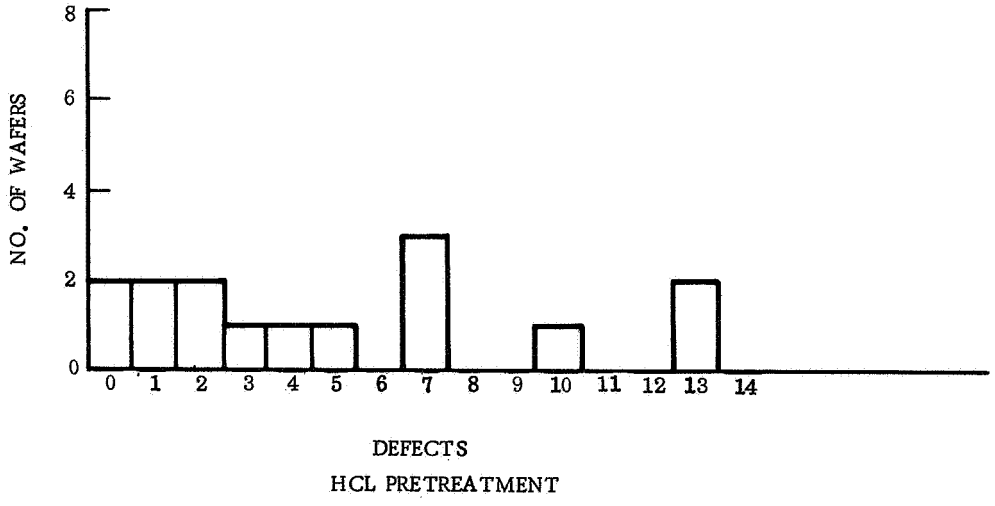




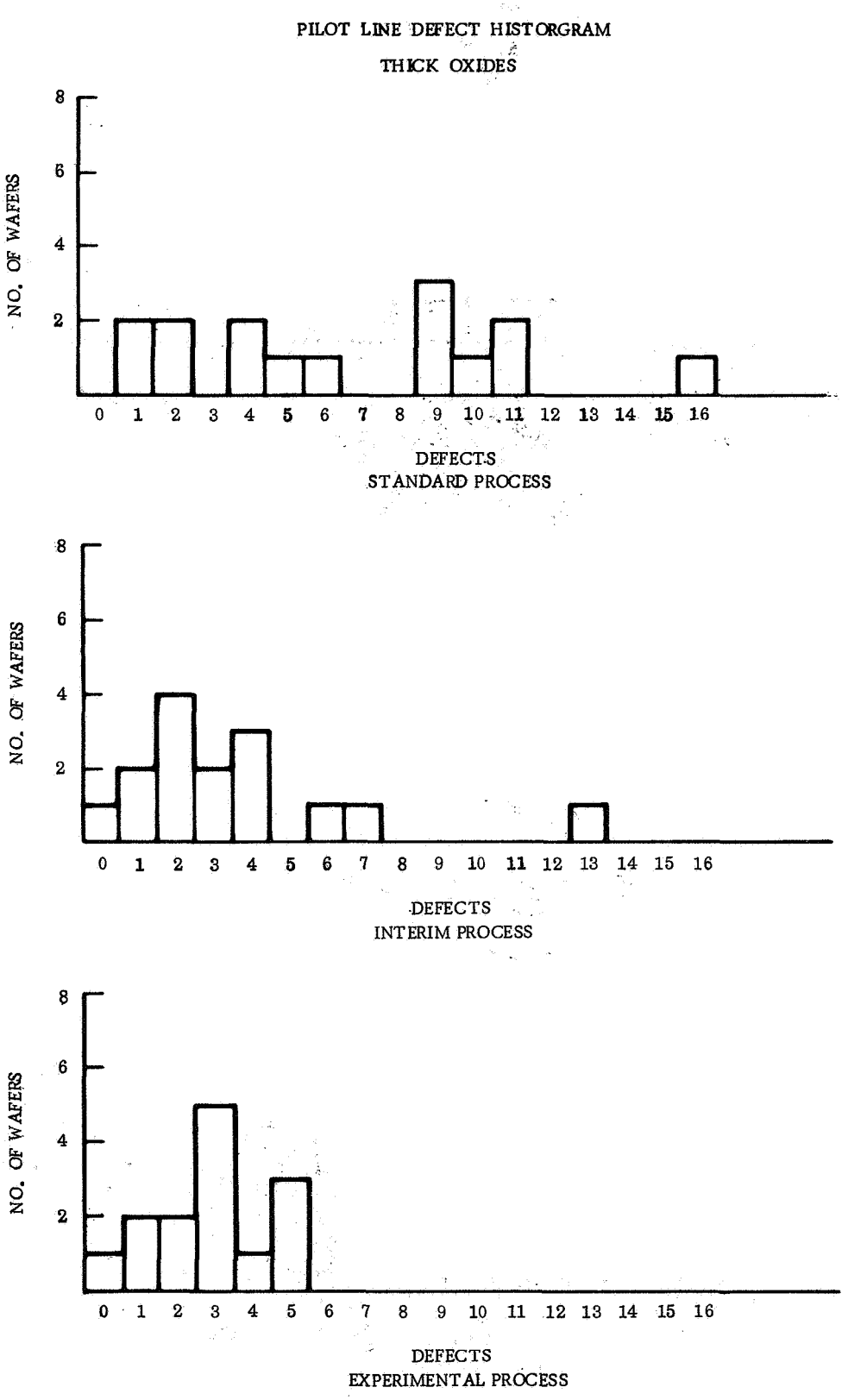
Pilot Line Defect Historograms







Pilot Line Defect Historograms



Pilot Line Defect Historograms