RESEARCH FOR DEVELOPMENT OF THIN-FILM SPACE-CHARGE-LIMITED TRIODE DEVICES (U)

By
Kenneth G. Aubuchon, Peter Knoll and Rainer Zuleeg

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ABSTRACT

Silicon-on-sapphire space-charge-limited triodes were designed and fabricated. The silicon films were grown on $(01\bar{1}2)$ oriented sapphire (α-Al_2O_3) wafers by the pyrolysis of silane (SiH_4) at temperatures between 1000° and 1150°C and were investigated by X-ray diffraction methods and by Hall effect measurements. The films with the best structural perfection, having hole mobilities of essentially single crystal silicon, were grown at 1050°C. Higher as well as lower pedestal temperatures resulted in a poorer deposit. The high temperature limitation for the film growth apparently is due to a chemical reaction between silicon and sapphire which is enhanced with increasing temperature. The films used for device fabrication were p-type and were polished to 2μ thickness. The SCL-triodes are similar to off-set gate n-channel MOS transistors and the processing is the same except for an initial masking step which isolates silicon islands on the sapphire substrate. The feed-back capcaitance of the SCL-triodes was calculated to be 0.12 pf, and the TO-5 headers contribute an additional 0.2 pf. The maximum frequency of oscillation obtained was 3 to 4 GHz for a source-drain spacing of approximately 4 μm. Higher frequencies should be obtainable with further reduction in source-drain spacing. Both enhancement and depletion mode devices were obtained. It is shown that a higher frequency response is expected from the positive gate (enhancement mode) operation. Results of radiation tests with doses up to 2×10^5 rads are presented, along with comparative tests on MNS and MOS capacitors which indicate that silicon nitride is much less sensitive to ionizing radiation than SiO_2.

FOREWORD

This report was prepared by the Solid State Research Center and the Applied Solid State Research Department, Hughes Aircraft Company, Newport Beach, California, for the National Aeronautics and Space Administration on Contract NAS 12-144: "Research for Development of Thin-Film Space-Charge-Limited Triode Devices". The report covers the period 1 June 1966 to 1 April 1967. The work was administered by the Electronics Research Center of NASA, Cambridge, Massachusetts, under the direction of Dr. K. Behrndt and Dr. Kazi E. Haq.

The objectives of this contract were the development and electrical evaluation of silicon-on-sapphire thin-film devices operating in the space-charge-limited mode with respect to temperature and radiation sensitivity, high frequency response, and noise suppression. By mutual agreement, the emphasis during the last three months of the contract period was shifted toward process control and material perfection.

The principal investigator of the contract studies was Mr. R. Zuleeg. Authors of this report were Mr. K. G. Aubuchon (III, IV and V), Dr. P. Knoll (I) and Mr. R. Zuleeg (II and IV). The authors would like to acknowledge the valuable services of Mr. J. F. Ryan for the growth of the silicon films, Mr. N. Nicolson for photolithography, Mr. B. F. Rowland and Mr. R. P. Totah for diffusion, Mrs. A. P. Brown, Mr. F. Rhoads and Mr. M. Siracusa for electrical evaluation, and Mr. H. G. Dill for many helpful suggestions.

This report was submitted in May 1967.

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Cont'd)

I. MATERIAL PREPARATION AND ANALYSIS

A. INTRODUCTION

Integrated circuits with active and passive components on a semiconductor wafer have gained much attention in recent years. However, the single wafer approach has a disadvantage, since all the components are electrically coupled via the conductive substrate. The coupling limits the high frequency operation of the integrated circuits. It can be eliminated when the devices are made of a thin silicon film deposited on an insulating substrate. There are several methods for the thin-film deposition of silicon, e.g., evaporation in vacuo, sputtering, or the reaction of gaseous silicon compounds, but device quality silicon films have so far only been produced by the pyrolysis of silane (SiH_4). The experimental setup with its open tube system and the r-f heated pedestal is practically the same which is used for the epitaxial deposition of silicon-on-silicon.

Several materials have been considered as substrates. In the following chapter, a selection of publications is presented in which the usefulness of dielectric materials for silicon deposition is discussed. The emphasis is placed on those methods which result in device quality silicon.

B. LITERATURE SURVEY

Silicon deposition on single crystal quartz was reported in 1963 by Joyce, Bicknell, Charig and Stirland (Ref. 1) who used the hydrogen reduction of $SiHCl_3$. In the following years, single crystal as well as amorphous quartz was mentioned occasionally (Ref. 2, 3, 4). The lack of interest in this substrate material probably stems from the fact that silicon has a thermal expansion coefficient which is almost one order of magnitude larger than that of quartz. This leads to severe stress problems in the film.

Rasmanis (Ref. 5) used a "rheotaxial" method to deposit silicon onto glazed alumina. The deposit could be obtained as a single crystal in certain discrete areas. However, constituents of the molten glaze can diffuse into the silicon film during the growth process, thereby

limiting its usefulness for device fabrication. The uneveness of the glaze surface can present another problem.

A rather inexpensive method seems to be the deposition of silicon on sintered alumina wafers, as suggested by Doo (Ref. 6). In spite of the polycrystalline nature of the substrate material, comparatively large silicon single crystal areas up to 0.5 x 3 mm could be obtained by a melting and regrowth technique. However, the heat treatment caused aluminum ions to diffuse from the substrate into the molten film and hence only a low resistivity material could be formed. Doo grew an epitaxial film on top of the first silicon layer which had been polished and etched. The second film had a thickness of 5-8 μ. With phosphorus diffusion, a good quality mesa diode could be made. But the original film, recrystallized or not, did not appear to be useful for the fabrication of operational thin-film devices.

The deposition of silicon on a substrate of magnesium aluminate spinel, as reported by Seiter and Zaminer (Ref. 7), Manasevit and Forbes (Ref. 8), and Schlötterer and Zaminer (Ref. 9) is of interest because this material has a cubic structure like silicon. Studies with spinel were made in this laboratory (Ref. 10). Good quality p-type silicon films were obtained with values of room temperature carrier mobility approaching those of single crystal silicon with the same resistivity. The limited thermal stability of spinel, however, particularly in a hydrogen atmosphere, makes this material less suitable for thin film active device fabrication.

Beryllium oxide has a high thermal conductivity. It also has a high electrical resistivity and it is very resistant to ionizing radiation. These properties make BeO a preferred substrate material for thin-film semiconductor devices, particularly for power devices. Successful epitaxial deposition of silicon on several natural faces of BeO was reported by Manasevit, Forbes and Cadoff (Ref. 11). Difficulties, however, are encountered with the material preparation. The largest BeO single crystals which have been obtained are only 5 or 10 mm in diameter (Ref. 12). Production of larger crystals has been hampered by a severe polynucleation apparently caused by uncontrolled impurities. The extreme toxicity of beryllium requires special precautionary measures which present another

problem. The price for larger pieces of single crystal BeO is about $1000 per gram. These factors have at least temporarily limited the usefulness of BeO as a substrate material.

The pyrolysis of SiH_4 for the epitaxial deposition of device quality silicon on silicon carbide was reported by Tallman et al (Ref. 13). However, SiC is not a good electrical insulator, and it is difficult to machine and thus has limited usefulness as a substrate material.

The material which so far has attracted the most attention is single crystal corundum (α-Al_2O_3) or, by its engineering name, sapphire. This material has proven useful for silicon deposition for several reasons:

1. Compatibility of its thermal expansion coefficient with that of silicon.
2. Good insulating properties.
3. Chemical stability in hydrogen or in an inert gas atmosphere at the silicon growth temperature.

There is no structural match between sapphire and silicon, but this apparently does not hinder epitaxial growth.

Successful epitaxial deposition of device quality silicon on this substrate material was first reported by Manasevit and Simpson (Ref. 14, 15) in 1963 and 1964. A selection of papers which other research groups have presented in the following years is given in References 16 through 26.

C. EXPERIMENTAL

As already pointed out in the previous Final Report (Ref. 10), silicon halides seem to be inadequate for the thin-film growth of silicon on sapphire substrates because of a high temperature reaction between the halide vapor and the substrate. All the samples prepared for this contract, therefore, were made with silane pyrolysis. The silane-hydrogen mixture was used in an open tube system similar to that described by Mueller and Robinson (Ref. 16, 22). A diagram of the system is presented in the Figure 1.

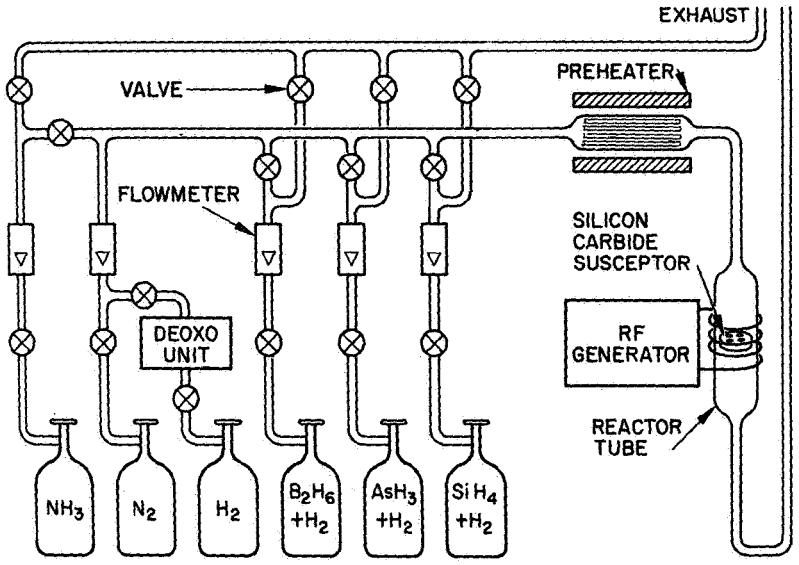


Figure 1. Silicon thin-film deposition apparatus

The silane, diluted with hydrogen, was furnished byThe Matheson Company in a steel tank, together with the following analysis (values are in volume percent):

silane	14.6
disilane less than	0.020
N_2 less than	9.1 ppm
CO_2	0.0004
H_2	balance

The pressure of the tank was about 100 atmospheres. Hydrogen-diluted arsine (AsH_3) could be fed into the system for n-type doping as indicated in the Figure 1. A tank of hydrogen-diluted diborane (B_2H_6) was provided as p-type dopant. However, this gas was used only infrequently, because

the silicon films usually were found to be of p-type conductivity when no dopant was intentionally added during growth. Nitrogen was used as the purging gas. The hydrogen passed through a Deoxo Dual Puredryer before entering the system. A tank of ammonia was provided for the growth of silicon nitride films. The silicon depositions were performed in a vertical quartz reactor tube with an internal diameter of 7.5 cm. The round silicon carbide-coated susceptor measured 5.4 cm across. The water-cooled coil around the reactor tube was connected to a 10 kW r-f generator of 450 kHz. Between the flowmeter panel and the reactor, a preheater furnace was installed for the purpose of purifying the hydrogen-silane gas mixture. It was hoped that traces of oxygen and nitrogen could be deposited as silicon oxides and nitrides, thus reducing the contamination level of the hydrogen.

The sapphire substrates were bought from several suppliers. The diameter of the wafers was between 13 and 16 mm, and the thickness 0.38 mm. All the substrates which were used for device fabrication were of $(01\bar{1}2)$ orientation. This plane was suggested by Manasevit, Miller, Morritz, and Nolder (Ref. 17), and by Larssen (Ref. 24). The notation refers to the structural unit with the c/a ratio of 2.73, described in detail by Kronberg (Ref. 27). Some runs were also performed with (0001) oriented substrates, but no devices were fabricated.

The sapphire wafers were bought with a fine polish, applied by the supplier. The mechanical finish of the substrates is very important. Growth of a silicon layer on a poorly polished substrate often takes place preferentially along scratches. In fact, one of the best tests for the quality of a finished sapphire surface is the uniformity of a 2000Å thick silicon film. Uniform silicon film growth requires sapphire substrates with the highest polish commercially available.

A certain number of specimens received an additional surface treatment. Some were etch-polished with a silica slurry by an outside company, a procedure which removed 25 to 50 μm of material. Some other wafers were etch-polished for more than 400 hours on a wheel covered with paper which was soaked in KOH solution. The other samples did not receive an etch treatment. Prior to the silicon deposition, all

specimens were cleaned with methanol in an ultrasonic bath, boiled in HCl, and then annealed in the reactor for 5 hours in a hydrogen atmosphere at 1300°C (temperature indicated by optical pyrometer). Heating of a mechanically polished sapphire surface in hydrogen results in an improvement in the single-crystal surface. This can be shown by electron diffraction patterns, as was pointed out by Robinson and Mueller (Ref. 22) who stated that the original ring-type Laue pattern changed to a single-crystal pattern with Kikuchi lines. This significant change in surface structure occurs either by a thermal etching or by some surface rearrangement or by some combination of these two processes. The best silicon films usually are deposited on prefired sapphire substrates.

D. RESULTS

A series of 14 wafers was used for four runs (408 to 411) where the only parameter change from run to run was the susceptor temperature ranging from 1000°C to 1150°C (indicated by pyrometer). Table 1 is a compilation of the results of this investigation. Some of the specimens, as designated with "ep", were etch-polished for 80 hours with KOH, all others were only mechanically polished. The reaction time was 30 min. for all runs. The thickness of the deposits ranged from 3.9 to 6.0 μm.

The value of the Hall mobility at room temperature has been used to determine the layer perfection. The investigation of the Hall effect was performed on 2500 and 100 μm wide silicon strips which were etched out after a standard wax evaporation through metal masks. Photographs of the Hall samples are presented in Figures 2 and 3. The 100 μm mask was designed such that it could be used on a previously etched 2500 μm wide sample. In this way, the carrier mobility could be determined on the same specimen, first with a 2500 and then with a 100 μm wide strip.

The resistivity ranged from 160 to 0.09 Ω-cm, the lower pedestal temperature resulting in the higher resistivity. The concentration of the carriers, which were all p-type, was found to be about $10^{15}cm^{-3}$ for the 1000°C specimens and higher than $10^{17}cm^{-3}$ for those which were prepared at 1150°C. The mobility values ranged from 41 to 227 $cm^2/Vsec$. They were compared with the values given by Morin and Maita (Ref. 28)

Run No.	Susc. Temp (°C)	Thickness (μm)	Growth Rate (μm/min)	ρ (Ω-cm)	2500 μm mask n (cm^{-3})	μ ($cm^2/V/sec$)	μ_{M+M} ($cm^2/V/sec$)	Qual. fact. (%)	100μ mask μ ($cm^2/V/sec$)	$\frac{\mu_{2500}}{\mu_{100}}$	(111)	(220)	(311)	(400)	Posit.
408															
A ep	1000	3.9	0.13	14.7	$4 \cdot 10^{15}$	106	348	31	99	1.07	-	?	-	213	a
B ep		4.0	0.13	-	-	-	-	-	-	-	2	?	-	~400	a
C		4.2	0.14	16.3	$3 \cdot 10^{15}$	124	349	36	127	0.98	-	?	2	~400	a
D		4.0	0.13	160	$9.5 \cdot 10^{14}$	41	352	12	35	1.17	-	?	-	-	a
409															
A ep	1050	3.9	0.13	0.19	$1.5 \cdot 10^{17}$	227	230	99	231	0.98	-	?	-	-	a
C		4.5	0.15	0.24	$1.2 \cdot 10^{17}$	225	244	92	215	1.05	-	?	2	~400	a
D		4.2	0.14	0.21	$1.3 \cdot 10^{17}$	223	235	95	204	1.09	2	-	-	~400	a
410															
A ep	1100	5.2	0.17	0.25	$3.2 \cdot 10^{17}$	77	248	31	-	-					
B ep		5.2	0.17	0.36	$2.9 \cdot 10^{17}$	57	262	22	53	1.08	85	?	7	38	a
											10	9	2	-	na
C		6.0	0.2	0.55	$2.4 \cdot 10^{17}$	46	286	16	-	-	130	?	-	6	a
											63	47	3	18	na
D		6.0	0.2	0.29	$2.4 \cdot 10^{17}$	86	252	34	106	0.81	9	?	1	1	a
											10	3	1	59	na
411															
A ep	1150	5.0	0.17	0.24	$3.7 \cdot 10^{17}$	71	248	29	58	1.23					
B		5.0	0.17	0.24	$3.1 \cdot 10^{17}$	81	248	33	53	1.53	200	?	3	10	a
											53	39	5	7	na
C		4.8	0.16	0.21	$4.1 \cdot 10^{17}$	72	235	29	69	1.05					
D		5.1	0.17	0.09	$3.8 \cdot 10^{17}$	170	188	90	157	1.08	~400	115	2	8	a
											15	6	191	-	na
ASTM X-ray powder data card file											100	60	35	8	-

Table I. Results of Hall effect and X-ray diffraction measurements on p-type silicon-on-sapphire films

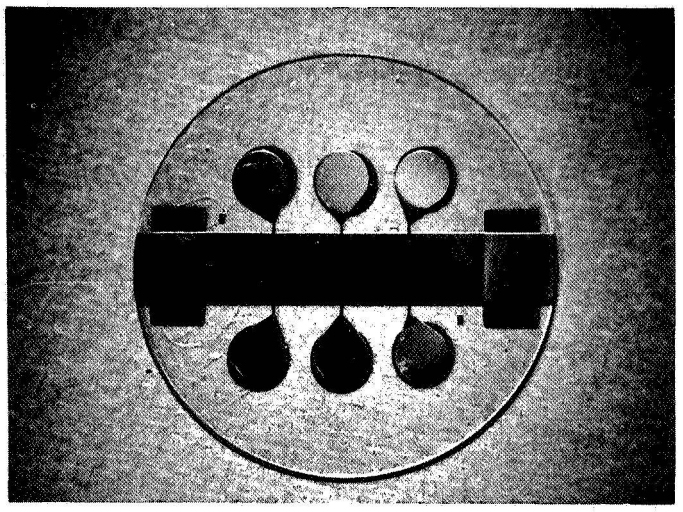


Figure 2. Strip of silicon film 2500 μm wide for Hall effect measurements.

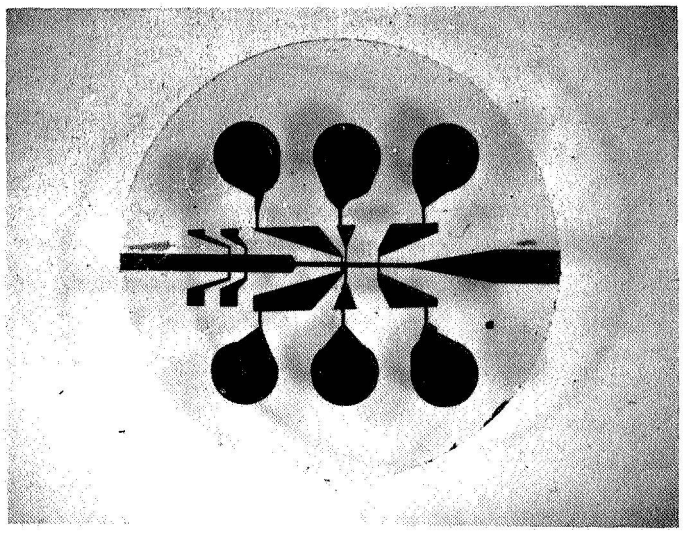


Figure 3. Strip of silicon film 2500 μm wide for Hall effect measurements.

for single crystal p-type silicon with the same resistivity. The ratio of the experimentally determined mobility values for silicon-on-sapphire samples to the mobility values of single crystal bulk silicon with the same resistivity can be used to asses the quality of the thin-film specimens. This procedure was used by Robinson and Mueller (Ref. 22). The quality factors ranged from 12% to 99% for the 14 specimens. In Figure 4, the averaged values of the quality factor are plotted as a function of the uncorrected deposition temperature.

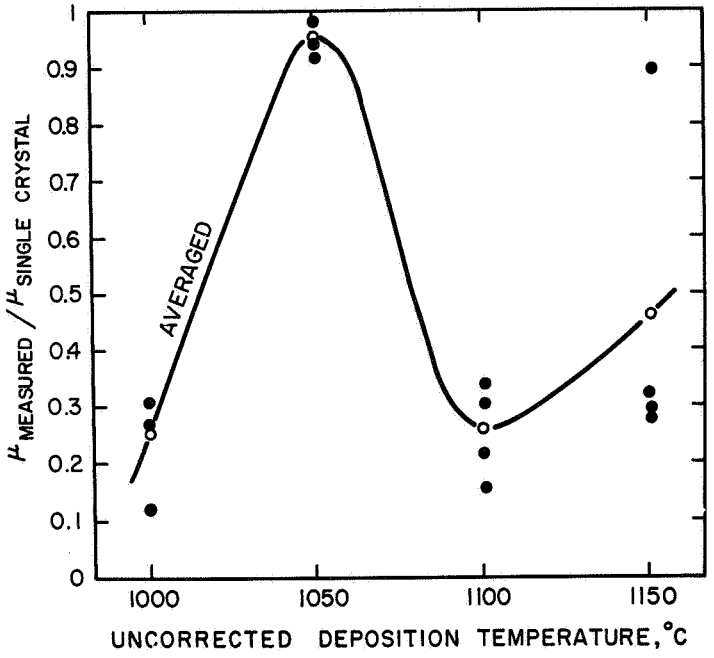


Figure 4. Hall mobility of 14 p-type specimens in relation to the mobility of single crystal silicon with the same resistivity. The values are plotted as a function of the uncorrected deposition temperature.

The curve has a maximum for the specimens prepared at 1050° where the mobility values reach almost 100% of the respective single crystal values.

The mobility values, determined with the 100 μm wide silicon strip, are compared in Table 1 with those values which were obtained with the standard 2500 μm configuration. The ratio of the mobilities

scatters in a rather random manner between 0.81 and 1.53. This indicates that there exists no significant difference between the mobility measured on a 2500 and on a 100 μm wide sample. The statistical deviations probably have to be attributed to random errors in the apparatus as well as to irregularities in the geometrical shape of the 100 μm wide strip.

The last columns in Table 1 refer to results which were obtained by means of X-ray diffraction. The investigation was made with a Norelco Geiger Müller counter wide angle X-ray diffractometer with a copper tube. The recordings showed the silicon reflections together with the $(01\bar{1}2)$ peak of α-Al_2O_3 and the higher order reflections of the $(01\bar{1}2)$ peak. The numbers in the table are peak heights in millimeters as they appeared on the chart. In most cases, a scale factor of 64 was used. Whenever a lower factor was employed, the intensity of the peaks was calculated for a value of 64. When a peak exceeded the range of the chart, its magnitude was estimated.

The recordings of some of the specimens did not show any peaks at all when the substrate was clamped to the sample holder reference plane of the goniometer in the usual way. Neither the silicon nor the corundum reflections appeared. Some other specimens yielded only silicon peaks but none of the substrate. Since the counter tube can pick up diffracted energy only when a crystallographic plane of the specimen is in a position parallel to the reference plane of the sample holder, the complete lack of the corundum peaks is evidence of a crystallographic misorientation of the substrate surface. The $(01\bar{1}2)$ peak can be picked up by the counter tube only when the substrate wafer is cut in such a way that the $(01\bar{1}2)$ plane makes an angle of smaller than one degree with the surface. Whenever this angle is larger, it is unlikely that peaks from the substrate will appear. However, silicon reflections may appear, depending on the film structure. In order to account for any possible small misorientation of the substrate, a special sample holder was used. With this sample holder, the wafer could be rotated around the normal axis of the surface and the wafer could be tilted.

Two positions of the wafers were of interest. In the aligned position "a" in Table 1, the goniometer was put in the 2θ angle for the $(01\bar{1}2)$

reflection, then the sample was rotated and tilted until maximum output of the counter was observed. The sample was left in this position while the scanning was made. In the "na" position, the sample was placed with its surface as close to the reference plane of the goniometer as possible, but now for minimum output of the counter with the goniometer at the same 2θ angle.

When the substrate was in the "a" position, those specimens which were deposited at 1000° and 1050°C showed essentially only the (400) silicon peak. The (111) and (311) did not appear. The copper Kβ $(01\bar{1}2)$ α-Al_2O_3 reflection could not be suppressed completely, not even with the nickel-filter, because of the high intensity of its Kα partner. The Kβ peak coincides with the (220) silicon reflection. Therefore, the intensity of a possible (220) silicon peak was sometimes questionable. The 1100 and 1150°C samples gave quite a different picture. In the "a" as well as in the "na" position the (111) silicon peak was very strong. Besides this peak, other silicon reflections appeared, making the recording similar to a silicon powder pattern. The height of the (111) peak, relative to the other silicon peaks, was generally larger in the aligned position than in the unaligned position. In the last line of Table 1, the intensities of the silicon powder pattern are given for a comparison. A selection of the X-ray diffraction recordings is illustrated in Figure 5.

Seven wafers were etch-polished with KOH solution for more than 400 hours. These wafers were used for silicon deposition together with untreated wafers from the same shipment. Mobility measurements on the etch-polished samples did not reveal an improvement in comparison with the untreated samples.

The preheater furnace, shown in Figure 1, was used in some runs. It was found somewhat difficult to establish unambiguously the effectiveness of this installation. The reason for this was that the growth rate of the silicon film in the main reactor was influenced severely by the temperature of the preheater. A considerable quantity of silane can be decomposed in the preheater thus lowering the concentration of silane available for silicon deposition in the reactor. Since the quality of the silicon films can depend very much upon the growth rate, more investigation will be required to

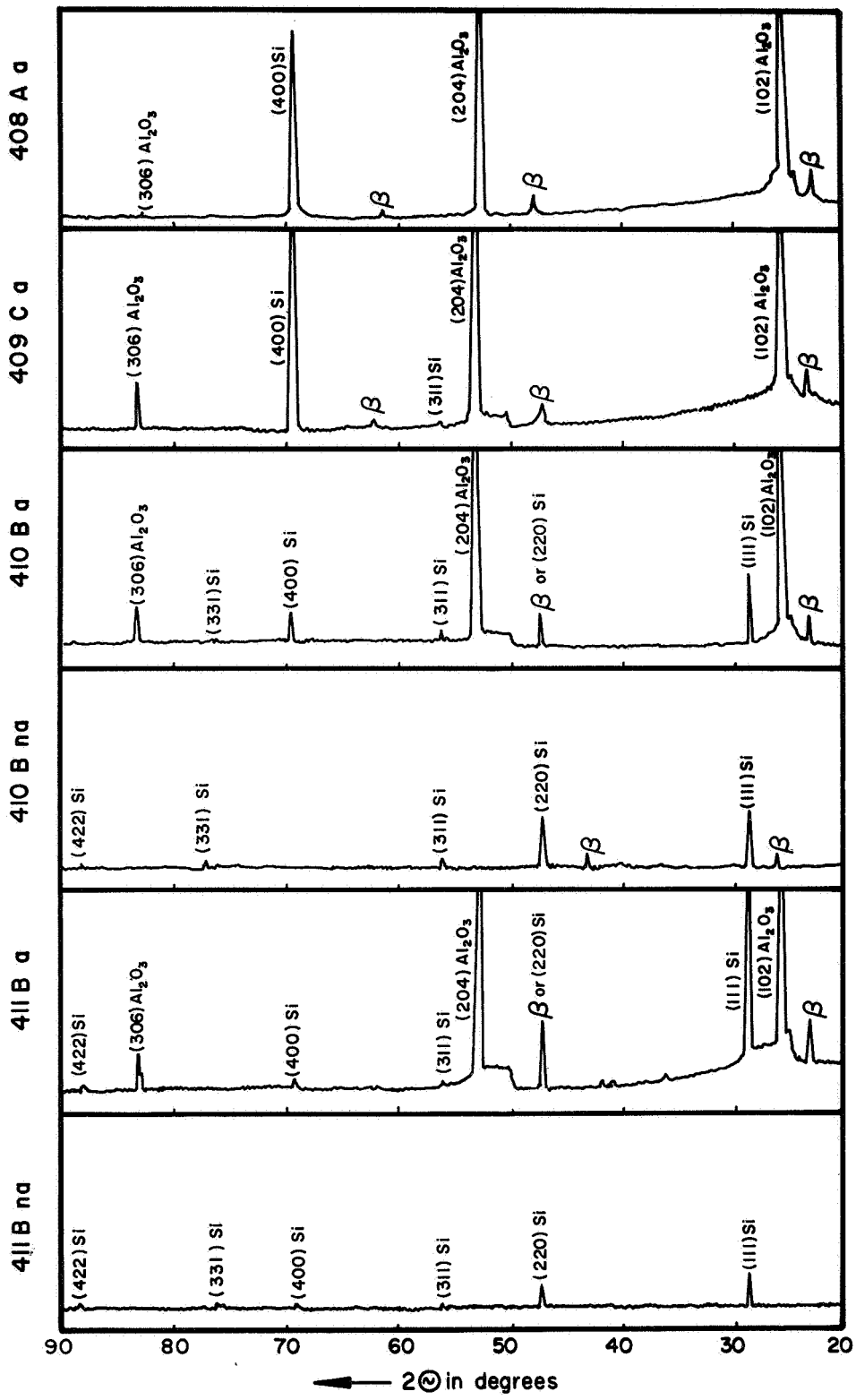


Figure 5. X-ray diffraction recordings of several silicon-on-sapphire specimens. Aligned position = a, non-aligned position = na.

find whether an improvement in film structure was caused by a more favorable growth rate or by a possible purification action in the preheater. Preliminary runs do not rule out the possibility that the quality of the silicon deposits can be somewhat improved by the presence of the preheater.

E. DISCUSSION

The diffractometer recordings of the specimens which were prepared at 1000° and 1050°C showed essentially only the (400) peak of silicon in the aligned position and no reflection at all when the specimen was tilted slightly out of alignment. These types of diffractometer recordings indicate a layer with a very high degree of orientation. The silicon is oriented such that the (001) direction is parallel to the $(01\bar{1}2)$ direction of the sapphire substrate. An epitaxial relationship of this kind was shown by Manasevit et al (Ref. 17) who reported (100) silicon to be parallel to $(1\bar{1}02)$ sapphire. It should be noted here that the $(01\bar{1}2)$, $(1\bar{1}02)$ and $(\bar{1}012)$ indices of sapphire describe planes which are equivalent. In this report the notation $(01\bar{1}2)$ was used in order to be consistent with the ASTM X-ray powder data card file, where the principal reflection for α-Al_2O_3 was named (012) on the card No. 10-173. (This card replaced No. 5-0712 where the (102) was listed.)

The $(01\bar{1}2)$ plane of α-Al_2O_3 has a four-fold symmetry. This is the reason why the (001) plane of silicon grows epitaxially on that plane. The lattice misfit of six percent per silicon unit mesh (Ref. 24) is no obstacle for an epitaxial growth.

According to the goniometer recordings, the samples prepared at 1100° and 1150°C do not have the same structure as the samples prepared at lower temperatures. Primarily, the silicon film has an (111) orientation, but some parts of the layer are randomly oriented, since a powder pattern appears when the specimen is not aligned. Apparently the (111) plane, which is the most densely populated plane of the silicon lattice, has a tendency to orient itself to the flat substrate at higher temperatures, regardless of the structure of the substrate. This conclusion seems to be in contradiction to the behavior of other epitaxial systems. The structual perfection of an epitaxial layer, deposited on a single crystal substrate,

usually depends mainly upon the deposition temperature. The general rule is that the crystallinity of the layer is improved by increasing the deposition temperature leaving other parameters constant. At low temperatures, a deposited layer often is either amorphous or it is polycrystalline with a small crystallite size. An increase in temperature will increase the size of the crystallites. When the substrate is heated above the so-called epitaxial temperature, a single crystal layer is formed. The epitaxial temperature is a function of the growth rate. At higher growth rates, the epitaxial temperature is increased. This interdependence between temperature, growth rate, and crystallinity seems to be applicable for homoepitaxial as well as for heteroepitaxial systems.

Theuerer (Ref. 29) investigated the silicon deposition on a silicon substrate with the decomposition of $SiCl_4$. At a substrate temperature of 895°C, he found the deposit to consist of gray, polycrystalline silicon, but at higher temperatures a perfect single crystal silicon layer was obtained. Similar results were obtained by Bylander (Ref. 30) who observed a silicon whisker growth at about 900° and a mirror-like surface of the layers at temperatures which were some hundred degrees higher.

An example of the heteroepitaxial growth was given by Krikorian and Sneed (Ref. 31) who evaporated germanium onto CaF_2 substrates. At constant growth rates, the structure of the germanium film undergoes two transitions when the temperature is increased, first from amorphous to polycrystalline and then from polycrystalline to monocrystalline.

This growth rate-temperature law seems to be applicable no matter whether vapor phase transportation, sputtering, or evaporation in vacuo is employed. The use of an inert carrier gas with its impurities might interfere with the layer growth but, generally, the growth rate law will not be affected. Higher temperatures increase the mobility of adsorbed molecules and this increases the rate at which adsorbed atoms enter ordered positions. As long as this rate is not lower than the adsorption rate, epitaxial growth can be achieved.

The general rule for epitaxial growth, of course, is applicable only in the absence of a chemical reaction between the substrate and the

deposited material. This is not the case for silicon and sapphire. The reaction (Ref. 7)

$$2Si + Al_2O_3 \rightleftharpoons 2SiO(g) + Al_2O(g)$$

has an equilibrium at 1100° which is weighted toward the left side. However, even at this temperature, it can be shifted to the right when the SiO evaporates. This chemical reaction, which takes place between the adsorbed silicon molecules and the substrate, is an obstacle to the growth of a well oriented epitaxial film. With increasing temperature, the reaction is accelerated and the likelihood of the formation of an epitaxial layer is further decreased, although the higher mobility of the silicon molecules on the substrate surface would actually favor the oriented growth. At temperatures around 1400°C, the reaction can be so intense that silicon, fed into the reactor in the form of silane, can be used to etch the sapphire at a rate of 0.5 μm/min (Ref. 32). Since the effectiveness of this etching process is enhanced by higher temperatures, a certain temperature range exists where optimum epitaxial growth can be expected.

Besides the reaction between silicon and sapphire, another mechanism has to be considered which can influence the structure of the epitaxial film. The silane-hydrogen mixture is unstable at higher temperatures. In the vicinity of a heated surface, a gas phase decomposition can occur where a fine powder of amorphous silicon is formed (Ref. 33). When the powder particles can reach the substrate by diffusion and are incorporated into the growing silicon layer, the deposit will exhibit a high defect concentration or it might even become polycrystalline. The intensity of the gas phase reaction and with it the concentration of defects in the silicon film is increased with a higher susceptor temperature, with a higher concentration of silane, and with lower flow rates. Since the preheater furnace causes a large quantity of silane to be decomposed, the concentration of silane in the reactor was unknown in all those experiments where the preheater furnace was used. For this reason, it was not possible to compare the obtained results with data from the literature.

The gas phase reaction as well as the reaction of silicon with sapphire are enhanced with increasing temperature. Both reactions work against the "epitaxial temperature law" which increases the structural perfection with

increasing temperature. The data we obtained so far are not yet sufficient to draw a final conclusion as to what primarily affects the film structure at the higher side of the employed temperature range.

The influence of the deposition parameters upon the film quality can be monitored by means of Hall effect measurements. The mobility values are a very sensitive indicator of the structural perfection of the silicon films. Since the semiconductor is deposited on an insulating substrate, the interpretation of the measured values is easier in comparison with silicon films on a silicon substrate. A conductive substrate might lead to ambiguities when the electrical properties of an epitaxial layer are investigated. Robinson and Mueller (Ref. 22) have reported mobility values for p- and n-type silicon layers on sapphire substrates with several orientations. The hole mobilities ranged from 18 to 88 percent of the bulk mobility with the same resistivity. The n-type values were found to be between 10 and 55 percent of the bulk mobility.

The relative mobility values of our samples are plotted in Figure 4. They show the silicon to attain a maximum structural perfection with a growth temperature of 1050°C, which is in accordance with the result of the X-ray diffraction investigation. The distorted structure, obtained at higher temperatures, reduces the mobility considerably in comparison to the bulk value. These findings are not in agreement with Robinson and Mueller (Ref. 22) who reported 1100° to 1130°C (uncorrected) as the best growth temperature. At lower temperatures they found a polycrystalline growth and at 1000°C a black, loosely packed amorphous film. In making such a comparison, however, one has to take into account the fact that the growth rate can have a large influence on the layer perfection. Our films grew at about 0.15 μm/min. Increasing the growth rate usually results in a poorer film. With the employment of silane, the growth rate of the silicon film cannot be increased to very large values. For every mole of silane which travels towards the surface and which is decomposed, two moles of hydrogen are generated. The hydrogen, which flows away from the substrate surface, limits the number of silane molecules which can diffuse to the substrate.

Because of the lattice misfit between the (001) silicon plane and the $(01\bar{1}2)$ plane of sapphire, it is not possible to grow a silicon layer which is as defect-free as an epitaxial silicon layer on a silicon substrate. The growth starts with the formation of individual nuclei which grow larger and larger until they finally touch each other, forming a continuous layer. Where the crystallites grow together, translation boundaries are formed. These can be considered as the origin of a defect structure, as the silicon film grows thicker. By means of an annealing or recrystallization process, these defects can be corrected to a certain extent. However, this requires the specimens to be heated to temperatures at which a large quantity of aluminum diffuses from the substrate into the silicon. The annealing improves the structure but lowers the resistivity to values in the neighborhood of 0.1 Ω-cm. Defects caused by the translation boundaries act as scattering centers which can influence the carrier mobility, provided the free path length of the carriers is larger than the diameter of the areas between the translation boundaries. The mobility values obtained on 2500 and 100 μm wide silicon strips were found to be essentially the same for all deposition temperatures. Therefore, it can be assumed that the dimensions of the coherent ranges between the translation boundaries are well below the 100 μm of the investigated silicon strips.

The relative mobility values for n-type silicon films generally are lower than those for p-type. Robinson and Mueller (Ref. 22) reported 10 percent for an n-type silicon film on a 0° oriented substrate and 45 to 55 percent on a $(1\bar{1}02)$ oriented substrate. Our runs yielded n-type specimens which were typically between 0.04 and 0.12 Ω-cm, with relative mobility values between 10 and 50 percent. The highest absolute mobility value we have measured was 420 $cm^2/Vsec$. The resistivity of this sample was 0.13 Ω-cm and the carrier concentration about $10^{17}/cm^{-3}$.

When intentional doping is not applied, the silicon films grow p-type. This p-type impurity has been identified as aluminum (Ref. 23). To obtain n-type films, the addition of an n-type impurity (arsenic) will compensate for the p-type impurity and render the film n-type. This procedure introduces additional scattering centers which reduce the mobility considerably.

II. DEVICE THEORY

The theory of a space-charge-limited dielectric triode was derived by Wright (Ref. 34) and discussed in the application for a dielectric triode (Ref. 35). The theoretical current-voltage characteristics are represented by:

$$I_D = \frac{\epsilon_i \epsilon_o \mu_n W}{2h L_D} \left(V_G + \frac{V_D}{m} \right)^2 \qquad (1)$$

where the amplification factor, m, is related to the geometrical parameters of the device by:

$$m \simeq 4 \left(\frac{4L_D^2}{9ht} \right) \qquad (2)$$

Space-charge-limited currents were included in a theory of the insulated-gate field-effect transistor by Geurst (Ref. 36), who also pointed out that the space-charge-limited current between two knife-like contacts is given by:

$$I = \frac{2\mu_n \epsilon_s \epsilon_o}{\pi} \left(\frac{V_D^2}{L^2} \right) \qquad (3)$$

Equation (3) was further founded theoretically and discussed with respect to space-charge-limited currents in thin semiconductor layers (Ref. 37). The relation of I proportional to L^{-2} instead of the relation of I proportional to L^{-3} as predicted by the Mott-Gurney relation:

$$I = \left(\frac{9}{8} \right) \frac{\mu_n \epsilon_s \epsilon_o A}{L^3} V_D^2 \qquad (4)$$

was experimentally reported to exist by Polke, Stuke and Vinaricky (Ref. 38) on thin layers of crystalline Se.

The theory of the surface gate dielectric triode was developed by Rittner and Neumark (Ref. 39) as an extension of the theoretical work by Geurst (Refs. 36, 37) and predicts triode-like characteristics with voltage-current characteristics of:

$$I_D \simeq \frac{\pi \mu_n \epsilon_s \epsilon_o W}{2h^2} \left[(V_D/m_o)^2 - \sqrt{2}(V_D/m_o)(V_G - V_o) + (1/3)(V_G - V_o)^2 \right] \quad (5)$$

This equation is valid for $m_o >> 1$ and the amplification factor at cut-off for a finite source and drain electrode thickness (r in the analytical theory) was given as:

$$m_o = 1/2 \left[\exp.\ (\pi L/2h) \right] \left[\ln(4h/\pi r) \right] - 1 \quad (6)$$

and the pinch-off potential, V_o, per unit width, W, was defined by:

$$V_o = \frac{qN_o Lh}{2\epsilon_s \epsilon_o} \quad (7)$$

It should be pointed out that both of the SCL-triode theories apply to true dielectric triodes, where the electron injecting contact is an ohmic, metallic contact to the high resistivity semiconductor and the gate covers completely the source to drain gap. The lateral thin-film SCL-triode in silicon-on-sapphire structure, however, contains pn-junctions of finite cross section for source and drain contacts and due to charge accumulation or depletion, the boundary at the electron injecting source pn-junction is not fixed and is moving with respect to applied gate potentials. In spite of the differences in the geometrical models of Wright (Ref. 34) and Rittner and Neumark (Ref. 39) in comparison to the structure of the silicon-on-sapphire SCL-triode (Ref. 40), reasonable assumptions have been made to allow a comparison of both theories with the experimental voltage-current characteristics of SCL-triodes under investigation.

III. DEVICE DESIGN AND FABRICATION

A. MASK DESIGN

Figure 6 shows the basic set of masks used to fabricate the space-charge-limited triodes. The masks were fabricated by Electro-Mask Corporation in Van Nuys, California and were received on September 21, 1966. Mask No. 5 was later replaced by another mask (received on December 16 and designated No. 8) which left a wider bridge to the gate contact pad. Mask No. 3, which removes the oxide only over that portion of the channel which is to be covered by the gate, was later replaced by another mask (designated No. 7) which removed the oxide over the entire channel. Mask No. 7 was used only once, after which it was decided to strip all the oxide from the wafer at this point.

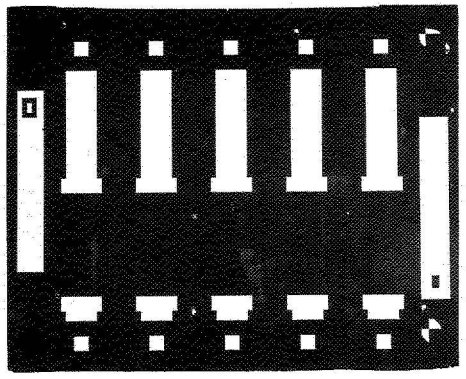
Mask No. 6 was designed to remove the oxide layer between the edge of the gate and the drain pn-junction and thus eliminate the formation of a "floating" channel when the device is exposed to ionizing radiation. Figure 7 shows both the standard structure and the radiation-hardened design of a space-charge-limited triode.

A 1/2 inch diameter sapphire substrate with approximately 300 isolated SCL-triodes is shown in Figure 8. Also shown is a sapphire chip 50 mils x 70 mils with 10 triodes of various geometries. This chip was separated from the master wafer by diamond scribing.

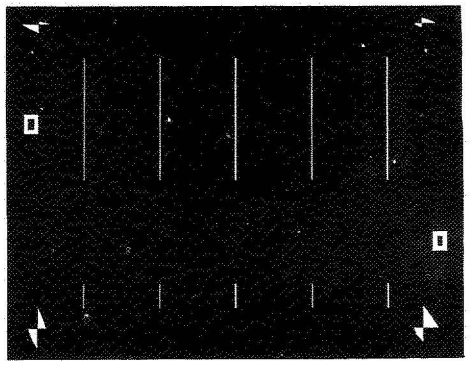
Of the 10 triodes on a chip, five have a channel width of 5 mils, and the other five have a channel width of 25 mils. Only the larger devices (those with the 25 mil channel width) were used for the work done on this contract.

The nominal dimensions of the five devices are given below. L_D is the source-drain distance, and L_G is the length of the channel which is covered by the gate.

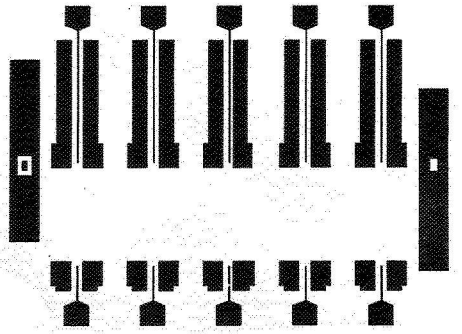
Device	L_D	L_G
1	10μ	5.0μ
2	10μ	2.5μ
3	6μ	5.0μ
4	6μ	3.0μ
5	6μ	3.0μ



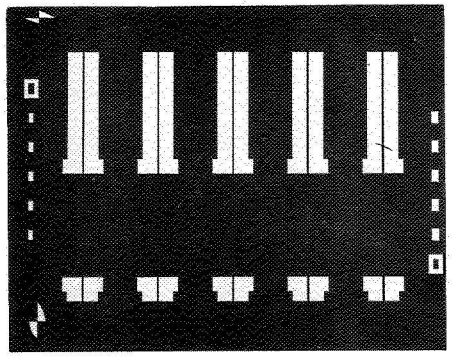
Silicon Isolation
Mask 1



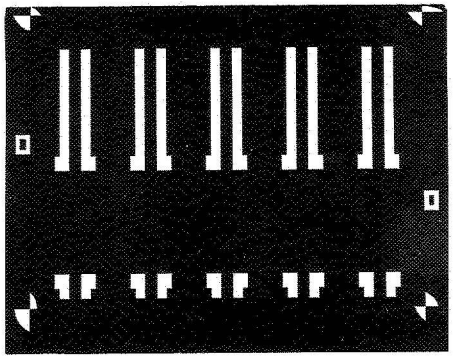
Gate Oxide Area
Mask 3



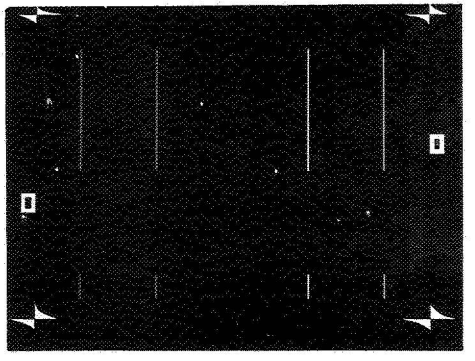
Aluminum Contact Pattern
Mask 5



Source-Drain Diffusion
Mask 2

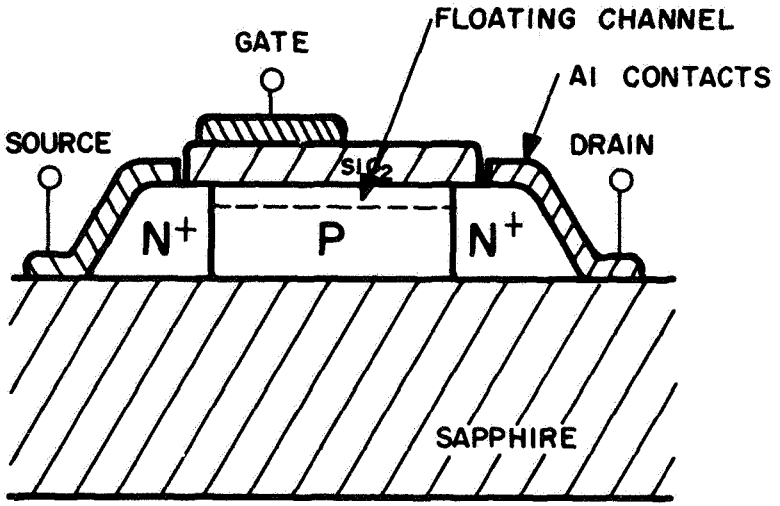


Contact Area Opening
Mask 4

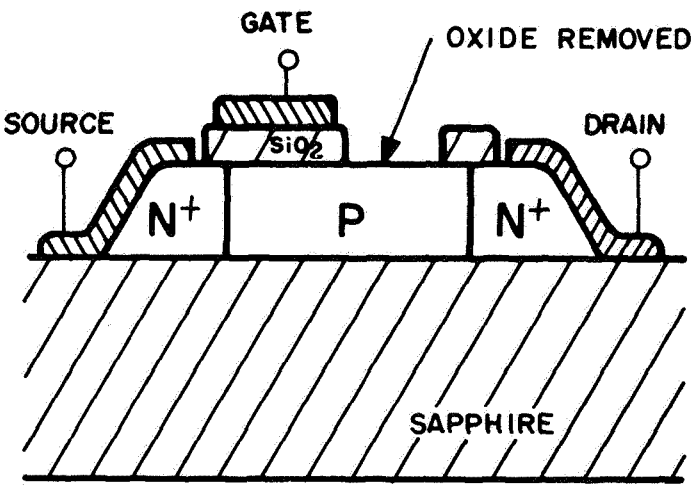


Supplemental Oxide Removal
Mask 6

Figure 6



STANDARD DESIGN OF SCL-TRIODE

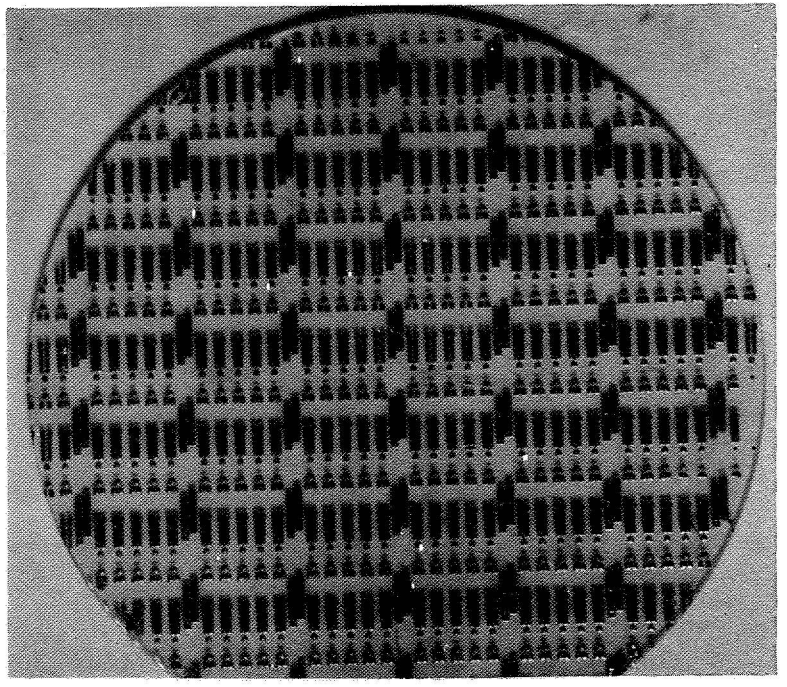


RADIATION HARDENED DESIGN OF SCL-TRIODE

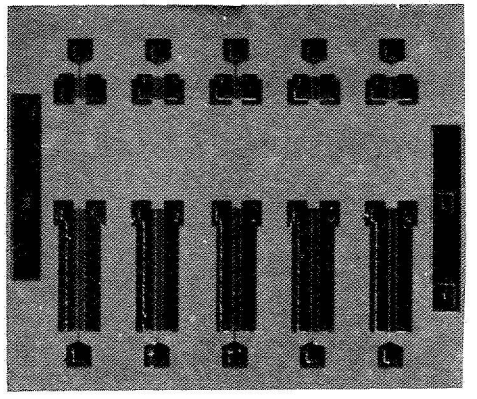
Figure 7 Cross Section of Thin-Film Space-Charge Limited Triodes in Standard Design and Radiation Hardened Design.

THIN-FILM SPACE-CHARGE-LIMITED TRIODES

(Silicon-on-Sapphire)



1/2 inch diameter Sapphire Substrate
with approximately 300 isolated devices.



Sapphire Chip (50 x 70 mil^2)
with 10 SCL-Triodes

Figure 8

The values given for L_D and L_G are those which would be obtained with no lateral spreading of the diffusion. The actual values of L_D and L_G on the finished devices are generally less than this, depending on the diffusion cycle used and on the quality of the silicon film (see discussion in Part E of this Section). The actual value of L_G can also be affected by errors in mask alignment.

B. SILICON PROCESSING

The starting material for the SCL-triodes is normally 2 to 20 Ω-cm p-type silicon on a half-inch diameter sapphire substrate. (The growth of the epitaxial silicon is described in Section I of this Report.) The silicon is always mechanically polished to the desired thickness (~2μ) before being used for device fabrication.

1. Isolation Mask (Mask No. 1). This mask is used to obtain complete isolation of each device from all other devices. After standard masking procedures, the excess silicon is etched away with a combination of HF, HNO_3, and acetic acid in such a way as to obtain a tapered edge (rounded corners) on the silicon islands. This taper is a result of combined masking techniques and the etchant used. After etching, the photo-resist is stripped with hot H_2SO_4 and HNO_3.
2. Clean in deionized water.
3. Grow 5000Å of SiO_2 - 5 minutes dry, 50 minutes wet, 15 minutes dry at 1150°C. The wet cycle consists of steam, introduced into the quartz tube at about 1 atmosphere pressure.
4. Source-Drain Mask (Mask No. 2). Standard photolithographic techniques used to open windows in the oxide for source-drain diffusion.
5. Clean in hot H_2SO4, HNO_3, and deionized water, then rinse to purity (using pH meter) in running deionized water.

6. Source-drain deposit, $POCl_3$ at 930°C, 3 minutes dry, 10 minutes wet, 3 minutes dry - resultant surface concentration $5 \times 10^{19}/cm^3$.

7. Source-drain drive, 2 microns deep, 35 minutes wet, 10 minutes dry at 1150°C.

8. Oxide Removal Mask (Mask No. 3 or No. 7). Standard photolithographic techniques used to remove the oxide over the channel. Alternatively, all the oxide on the wafer can be removed.

9. Grow gate oxide - 10 minutes wet, 10 minutes dry at 1025°C.

10. Apply P_2O_5 glass layer - $POCl_3$ for 15 minutes at 930°C.

11. Clean in hot deionized water to remove excess phosphorus.

12. Contact Mask (Mask No. 4). Standard photolithographic techniques used to open windows in the oxide for the source and drain contacts.

13. Clean in running deionized water a minimum of 10 minutes, and blow dry with nitrogen jet.

14. Evaporate aluminum, 4000 to 6000Å. Done in diffusion-pumped vacuum system with liquid nitrogen cold trap and a pressure of about 1×10^{-6} mm Hg. Ion bombardment used for 20 minutes prior to evaporation of aluminum.

15. Contact Pattern Mask (Mask No. 5 or No. 8). Standard photolithographic techniques used. Strip off undesired aluminum.

16. Alloy aluminum -546°C for 10 minutes.

C. DISCUSSION OF PROCESSING PROBLEMS

The processing of silicon-on-sapphire field-effect devices leads to difficulties which are not normally encountered in the fabrication of such devices on bulk silicon. The main difficulty arises from the quality of the silicon. Although some of the silicon films have essentially bulk

mobilities, they are in general far from being single crystals. The structural defects in the film may cause irregularities in the diffusion process, so that the diffusions may go deeper than intended. A very large number of source-drain shorts have indeed been observed on the devices fabricated for this contract. This problem is discussed in another part of this Report.

Another difficulty is due to the fact that the sapphire is not an inert substrate at elevated temperatures. At elevated temperatures, it appears that aluminum diffuses out of the sapphire and into the silicon (Ref. 23). Films which are grown at higher temperatures (e.g. 1150°C) tend to be low resistivity p-type, while films grown at lower temperatures are somewhat higher in resistivity. Also, heat treatments in hydrogen at 1000 - 1200°C produce a decrease in resistivity of the p-type silicon films. It was therefore assumed that the resistivity of the silicon should decrease during the processing of the SCL-triodes.

In order to obtain a measure of the change in resistivity during processing, two silicon-on-sapphire samples of known resistivity were oxidized and their resistivities measured again after removing the oxide. Contrary to what was expected, the resistivity of the first sample increased from 5.4 Ω-cm to 11.1 Ω-cm, and that of the second from 4.86 Ω-cm to 12.1 Ω-cm. The first sample was then re-oxidized, after which the resistivity was 19.4 Ω-cm. In each case, the oxidation cycle was 5 minutes dry, 85 minutes wet, and 25 minutes dry at 1150°C, and the resultant oxide thickness was about 8000Å . This oxidation cycle closely simulates that used in the actual processing of the SCL-triodes.

Since this result could be explained simply by a decrease in mobility with no change in carrier concentration, the experiment was repeated on two Hall samples so that both ρ and μ could be measured.

Sample	ρ(Ω-cm)		μ(cm^2/Vsec)	
	Before	After	Before	After
S-469B	1.98	7.6	175	148
S-469A	5.4	27.3	151	95

The results do indeed show a decrease in mobility, but the change in ρ is mainly due to a decrease in carrier concentration. It is known (Refs. 41, 42) that p-type dopants are strongly depleted from an oxidized silicon surface. The depth to which the depletion extends can be comparable to the thickness of the silicon films used in this experiment, so that a large decrease in the concentration of the aluminum acceptor atoms results. This seems to be the most reasonable explanation for the observed changes in resistivity.

Another potential problem area is the formation of surface states at the silicon-sapphire interface, as reported by Heiman (Ref. 43). In depletion-mode devices, these surface states can prevent complete pinch-off from occurring. Heiman has observed the formation of donor surface states during heating in hydrogen, and acceptor states during heating in dry oxygen.

D. SUMMARY OF LOTS FABRICATED

The total number of lots processed during the period of this contract was 15, starting with lot NAS-5. In general, the lots NAS-5 through NAS-9 yielded very few operable devices due to problems in etching and mask design. The old masks (Series 4565 and 81113) were used while awaiting delivery of the new series (81172).

Lots NAS-6 and NAS-8 yielded a few good triode units which were mounted and bonded for measurements. Lots NAS-5, -7 and -9 (none of which yielded any devices) were used to evaluate various types of deposited gate insulators.

NAS-10, started 9-19-66: 4 wafers, using mask set 81172 which is shown in Figure 6. Normal diffusion and oxidation cycles were used but the run was split into two lots to try to determine the feasibility of applying the isolation etching before and after the diffusion step. NAS-10A was diffused first and then isolated, whereas 10B was isolated first and then diffused. Lot 10B was damaged at the contact mask step by extreme under-cutting. Lot 10A finished processing on 10-24-66 and units were diced and mounted for measurements.

NAS-11, started 10-11-66: 3 wafers, using mask set 81172 and a higher surface concentration ($\approx 7 \times 10^{19} cm^{-3}$) for the source-drain

diffusion. One wafer was separated for testing isolation versus diffusion as in lot 10. NAS-11A, 2 wafers, diffusion as first step, had bad undercutting at the contact mask step but some of the devices survived the alloying and were mounted. NAS-11B was destroyed at the contact mask step again. Two attempts were made to salvage this lot but were unsuccessful.

NAS-12, started 10-15-66: 2 wafers with boron diffusion (p-channel devices) using mask set 81113 from the previous contract NAS 12-5, with L_D from 10 to 25 μm. One wafer sent to Malibu (M. Braunstein) for special gate insulation. The remaining wafer was processed normally but the undercutting problem occurred at the contact mask step again. All units were shorted because the wrong mask numbers were specified on the processing sheet.

NAS-13, started 11-23-66: 2 wafers with a higher surface concentration for the source-drain diffusion. Specified surface concentration ($\approx 4 \times 10^{19} cm^{-3}$) was not as high as NAS-11. The mask with the wider bridging of the silicon step (no. 8) was used for the aluminum electrodes. One wafer was badly undercut and all units were shorted (gate-to-source and gate-to-drain). The other wafer showed extremely severe undercutting after contact masking, so it was reworked, but without success.

NAS-14, started 11-28-66: 2 wafers, a repeat of lot NAS-12 (p-channel devices) with the correct mask numbers specified on the processing sheet. The wafer with the thermally grown oxide completed processing. Some good devices were found on this wafer. Some devices showed microplasmas.

NAS-15, started 12-2-66: 3 wafers using mask series 81172 and a normal source-drain diffusion ($\approx 2 \times 10^{19} cm^{-3}$). One wafer (S-297D) was rejected after source-drain diffusion because of poor Si characteristics (gross crystalline imperfections). The remaining 2 wafers completed processing with the gate oxide having been re-grown twice (second time after removing all oxide on wafer). Both wafers yielded some good units. The new mask (81172-8) was used for aluminum electrodes.

NAS-16, started 12-19-66: 2 wafers, mask series 81172 and normal source-drain diffusion. The new mask 81172-7 was used to open the area for the gate oxide growth. Some undercutting occurred on one

wafer and both were re-worked by stripping all oxide off before growing gate oxide. Both wafers were rejected due to gate shorts and high leakage currents.

NAS-17, started 1-20-67; 2 wafers, mask series 81172 and source-drain diffusion surface concentration of $\approx 5 \times 10^{19}/cm^3$. All oxide was removed prior to gate oxide growth. The original mask (81172-5) was used for the aluminum electrodes to determine if the tapering of the edges of the silicon islands was as good as it looked. The devices worked and a fair yield from both wafers was realized. Devices were mounted and bonded.

NAS-18; By mistake, no wafers were processed using this lot number.

NAS-19, started 2-22-67: 2 wafers, mask series 81172, diffusion concentration $\approx 5 \times 10^{19}/cm^3$. All oxide was removed prior to gate growth and mask No. 8 was used for aluminum electrodes. Neither wafer yielded any good devices - all had high leakage currents or leaky gate insulation.

NAS-20, started 2-23-67: 2 wafers, mask series 81172 and diffusion concentration $5 \times 10^{19}/cm^3$. The processing was essentially the same as for NAS-19. Both wafers yielded some good devices although the gate oxide on wafer S-421D exhibited a low breakdown voltage. Devices were mounted and bonded.

E. DISCUSSION OF YIELD

As may be gathered from the preceding section, the yield from the 15 lots processed under this contract was very low. Many of the wafers were a complete loss, and only a few had a reasonable number of good devices. The total number of operable devices on hand at the end of the contract period was about 50, with only about 10 of them having geometries 4 or 5.

The low yield can be attributed mainly to three factors:

1. The quality of the material is not adequate to achieve well-controlled diffusions. This can be concluded from the presence of a large number of source-drain shorts on devices 1 and 2. The source-to-drain distance, L_D, for these

geometries is nominally 10μ, and so one would not ordinarily expect many source-drain shorts to occur. Indeed, devices fabricated from the same set of masks on bulk silicon as part of another program exhibited very few source-drain shorts. The fact that the source-drain shorts occur in the thin-film silicon-on-sapphire but not in the single-crystal bulk silicon suggests that the shorts are due to the structural imperfections in the thin-film silicon. It is speculated that diffusion of impurity atoms proceeds more rapidly through imperfections in the film (e.g., along grain boundaries). Anomalously deep diffusions and irregular diffusion fronts have, in fact, been observed (Ref. 23) in silicon-on-sapphire films which have not been heat-treated after growth.

2. The source-drain spacing of devices 3, 4 and 5 was chosen too small. Virtually all of the devices fabricated under this contract with these geometries had source-drain shorts. The mask dimensions are such that L_D, the source-drain spacing, is 6μ-2D, where D is the lateral diffusion depth. The diffusion-drive cycle chosen was such as to give D = 2μ in single-crystal silicon. This diffusion depth was chosen because the thickness of the silicon films was typically 2μ, and it was required that the diffusion go all the way down to the sapphire so as to minimize capacitances. If the lateral diffusion is the same as the vertical diffusion depth, this sets an upper limit (with the present masks) of 2μ on L_D, which is hardly sufficient. If, on the other hand, the vertical diffusion depth is larger than the lateral diffusion depth, as has been reported (Ref. 44) it should be possible to obtain $L_D > 2\mu$, providing that the drive cycle is just sufficient to drive the diffusion all the way to the sapphire substrate.

3. Considerable experimentation (e.g., with other types of gate insulator) was done on some of the lots processed early in the contract period. In addition, there were etching problems which were later resolved.

As a result of improvements in processing made during the contract period, the yield on the last five lots was considerably higher than on the earlier lots. With increased knowledge of the diffusion process in silicon-on-sapphire, further improvements can be expected. The fundamental limitation at this time seems to be the structural quality of the silicon films.

IV. DEVICE EVALUATION

A. CORRELATION BETWEEN THEORY AND EXPERIMENT

To compare the theories of dielectric triodes and the space-charge-limited current components which are expected for the silicon-on-sapphire structure, the following parameters were used:

W	$= 6.25 \times 10^{-2}$ cm	(Width of device)
L_D	$= 8 \times 10^{-4}$ cm	(Length between source and drain)
h	$= 2 \times 10^{-4}$ cm	(thickness of semiconductor)
t	$= 1 \times 10^{-5}$ cm	(thickness of insulator)
r	$= 2 \times 10^{-4}$ cm	(thickness of electrodes)
$\epsilon_i \epsilon_o$	$= 1/2 \times 10^{-12}$ F/cm	(absolute dielectric constant for SiO_2)
$\epsilon_s \epsilon_o$	$= 1 \times 10^{-12}$ F/cm	(absolute dielectric constant for Si)
μ_n	$= 500$ cm^2/Vsec	(mobility of electrons)

These geometrical parameters resemble the experimental devices used for correlation. The electron mobility of 500 cm^2/Vsec is representative of the present film material and was confirmed by Hall Measurements. (See Section II, Material Preparation.) Figure 9 presents the voltage-current relation using the parameters listed above for:

A. The space-charge-limited current relation according to Geurst and Equation 3.

B. The space-charge-limited current relation according to Mott-Gurney and Equation 4.

C. The current component at gate voltage equal to zero according to Wright and Equation 1.

D. The current component at gate voltage equal to zero according to Rittner-Neumark and Equation 5.

One experimental point is shown in Figure 9 for SCL-triode NAS 3-7 with $V_G = 0$ at $V_D = 30$ volts. The actual current values for the triodes are confined to the region between curve B and C. With reasonable adjustments in L_D, h and μ_n, the current in silicon-on-sapphire films can be expressed

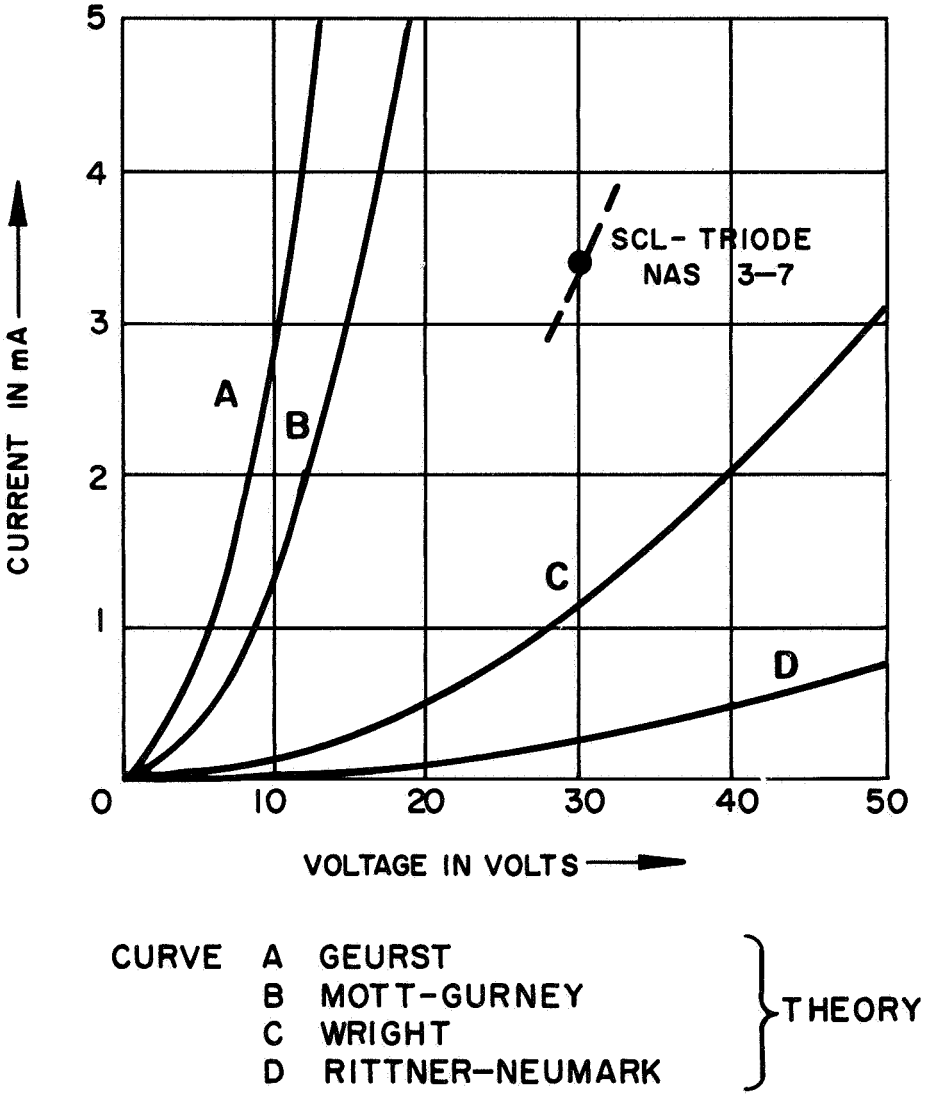


Figure 9: Voltage Current Characteristics of Two-Terminal Devices According to Various Theories at $V_G = 0$

by the Mott-Gurney relation for space-charge-limited current in a solid. Since the silicon film has a length to thickness ratio of 4 to 1, one would expect a closer approximation from the Geurst theory (Ref. 37) and curve A. Adjusting μ_n and L_D in Equation (3) to fit the experimental point for device NAS 3-7 requires either very low mobility values, which are unlikely, or L_D values much larger than the actual separation of source and drain contact. Further investigations are needed to clarify the applicability of either Equations (3) or (4) to describe the zero-gate bias current in the silicon-on-sapphire structure.

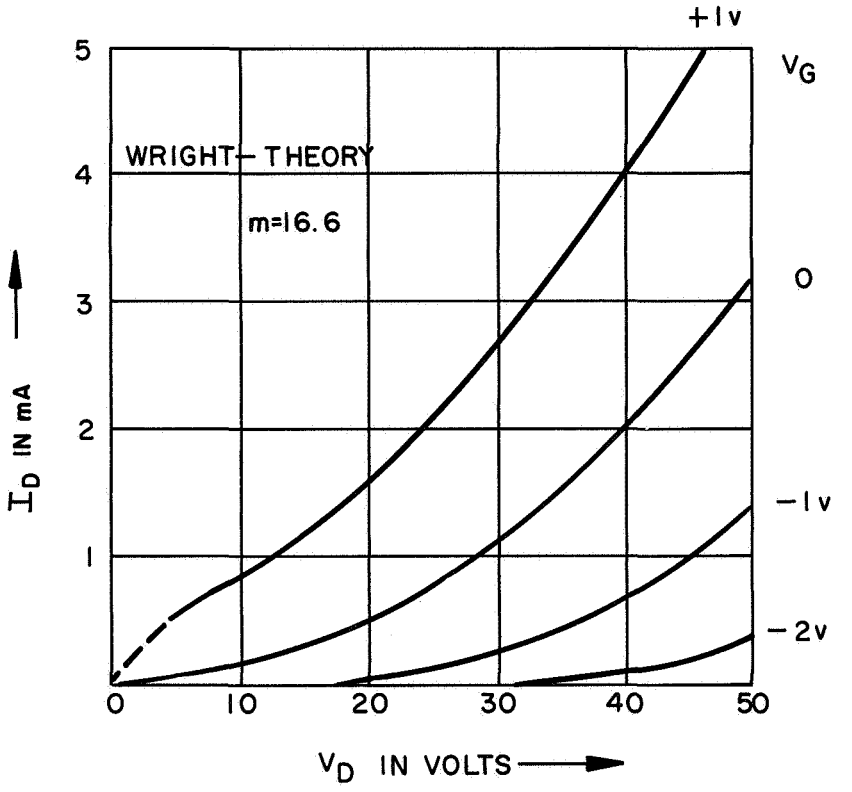
Figure 10 presents computed triode characteristics with the listed parameters according to the Wright theory and Equation (1) and the Rittner-Neumark theory (Ref. 39) according to Equation (5). The magnitudes of the currents and the amplification factors for both theories differ by roughly a factor of 4 for the identical geometry. When compared with the experimental voltage-current characteristics of SCL-triode NAS 3-7, which are shown in Figure 11, the Wright theory is off by a factor of 3 and the Rittner-Neumark theory by more than an order of magnitude. In particular, the amplification factor $m_o = 64$, which was obtained from Equation (6), is very high and not realistic. Although the Wright theory can be adjusted to give agreement with the experimental point at $V_G = 0$, the geometrical values cannot explain the low amplification factor of 5 for the experimental triode. To obtain m = 5 from Equation (2) with reasonable values of h and t, L_D would have to be unreasonably short, e.g., 0.5 to 1.5 μm.

A reasonable agreement between theory and experiment was obtained by using a first order theory which is based upon charge-control and transit time concepts. (Ref. 10) The current-voltage relation is:

$$I_D = \frac{\mu_n \epsilon_s \epsilon_o h W}{L_D^3} \left(V_D - |V_G| \right)^2 \left[1 - \left(\frac{L_D}{L_G} \right)^2 \frac{|V_G|}{(V_D - |V_G|)} \right] \quad (8)$$

and the amplification, m_o, at cut-off is:

$$m_o = 1 + \left(\frac{L_D}{L_G} \right)^2 \quad (9)$$


+1v
V_G
WRIGHT– THEORY
m=16.6
0
−1v
−2v
I_D IN mA
V_D IN VOLTS
0
10
20
30
40
50
1
2
3
4
5

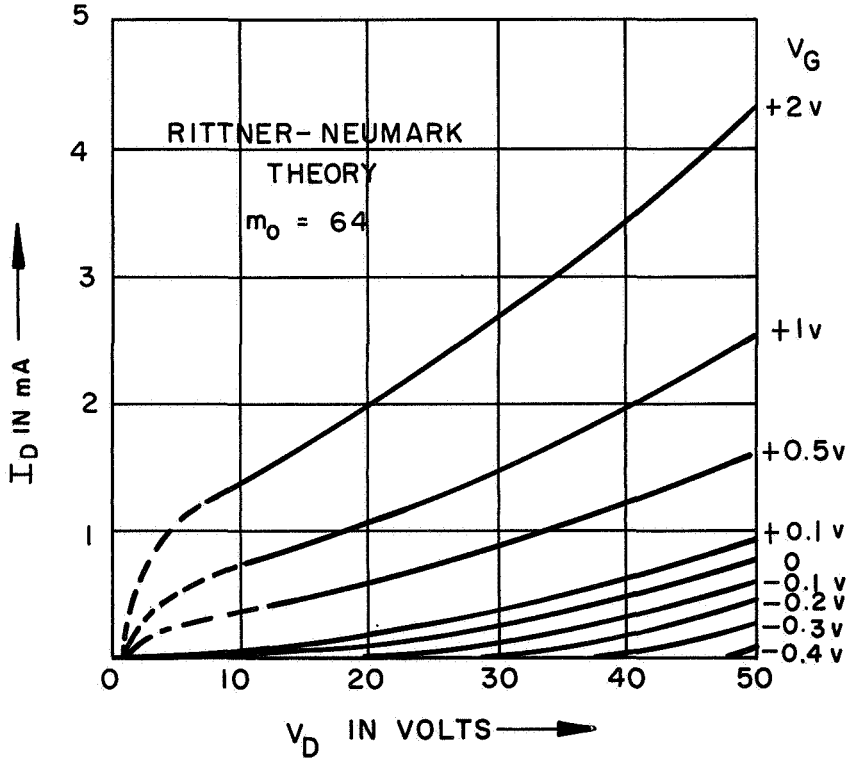
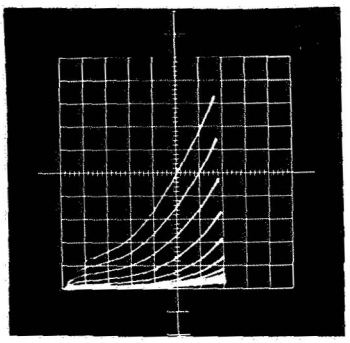

V_G
+2v
RITTNER– NEUMARK
THEORY
m_o = 64
+1v
+0.5v
+0.1v
0
−0.1v
−0.2v
−0.3v
−0.4v
I_D IN mA
V_D IN VOLTS
0
10
20
30
40
50
1
2
3
4
5

Figure 10



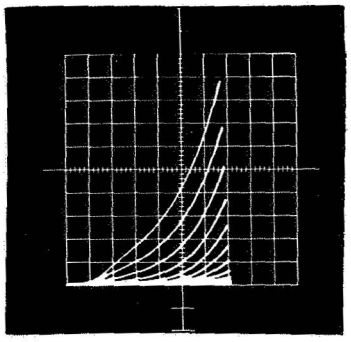
$V_G = 0$

↓

$-V_G$

300°K

Identical Scales:
Horiz. V_D in 5 V/DIV.
Vert. I_D in 0.5 mA/DIV.
Neg. Gate Voltage in 1 V /STEP



$V_G = 0$

↓

$-V_G$

77°K

SCL-TRIODE NAS 3-7
$V_D I_D$ - CHARACTERISTIC AT 300°K AND 77°K
WITH V_G AS PARAMETER

Figure 11

The theoretical curves in Figure 12 were matched to the experimental data of Figure 11 at the operating point $V_D = 0$ by adjusting the mobility value, which was selected to equal 610 $cm^2/Vsec$. In the recessed gate structure of the triode, $2L_G = L_D$, and from Equation (9) we obtain then $m_o = 5$. For the experimental triode at $V_D = 30$ volts, m_o is approximately 5. The deviation of the experimental curves from the theoretical curves at drain voltages below 30 volts stems from a residual conduction current, which has disappeared at 77°K (see Figure 11) owing to carrier freeze-out.

The first order modulation effect caused by the applied transverse gate voltage in the SCL-triode is the charge distribution in the vicinity of the source pn-junction. For a negative gate voltage, electrons leaving the n^+ source region are opposed by an electric field and the current is decreased until at a sufficiently high negative bias the electron flow is halted and the cut-off condition is reached. In the case of a positive gate voltage the electrons leaving the n^+ source region are accelerated and the drain current increases. This increase in current (and in turn the modulation efficiency of a recessed gate structure) will cease when, at a sufficiently high positive gate voltage, the "virtual" cathode has moved to the edge of the gate electrode on the side looking towards the drain pn^+-junction. This effect was experimentally verified and typical device characteristics are shown in Figure 13. At $V_G >> V_D$ the triode becomes essentially a space-charge-limited diode and the current is given by

$$I_D = \frac{\mu_n C_D}{(L_D - L_G)^2} V_D^2 \qquad (10)$$

The envelope of the limiting current gives a square-law characteristic according to Equation (10). Specific charge distributions for the positive and negative gate voltage operation of the SCL-triode are schematically shown in Figure 14. The equipotential lines for the recessed gate structure were plotted on conductivity paper (Teledeltos of 10 K-Ω/□ sheet resistivity) similar to the method applied by Rittner and Neumark (Ref. 39) for the surface gate dielectric triode. The dielectric material of the insulated

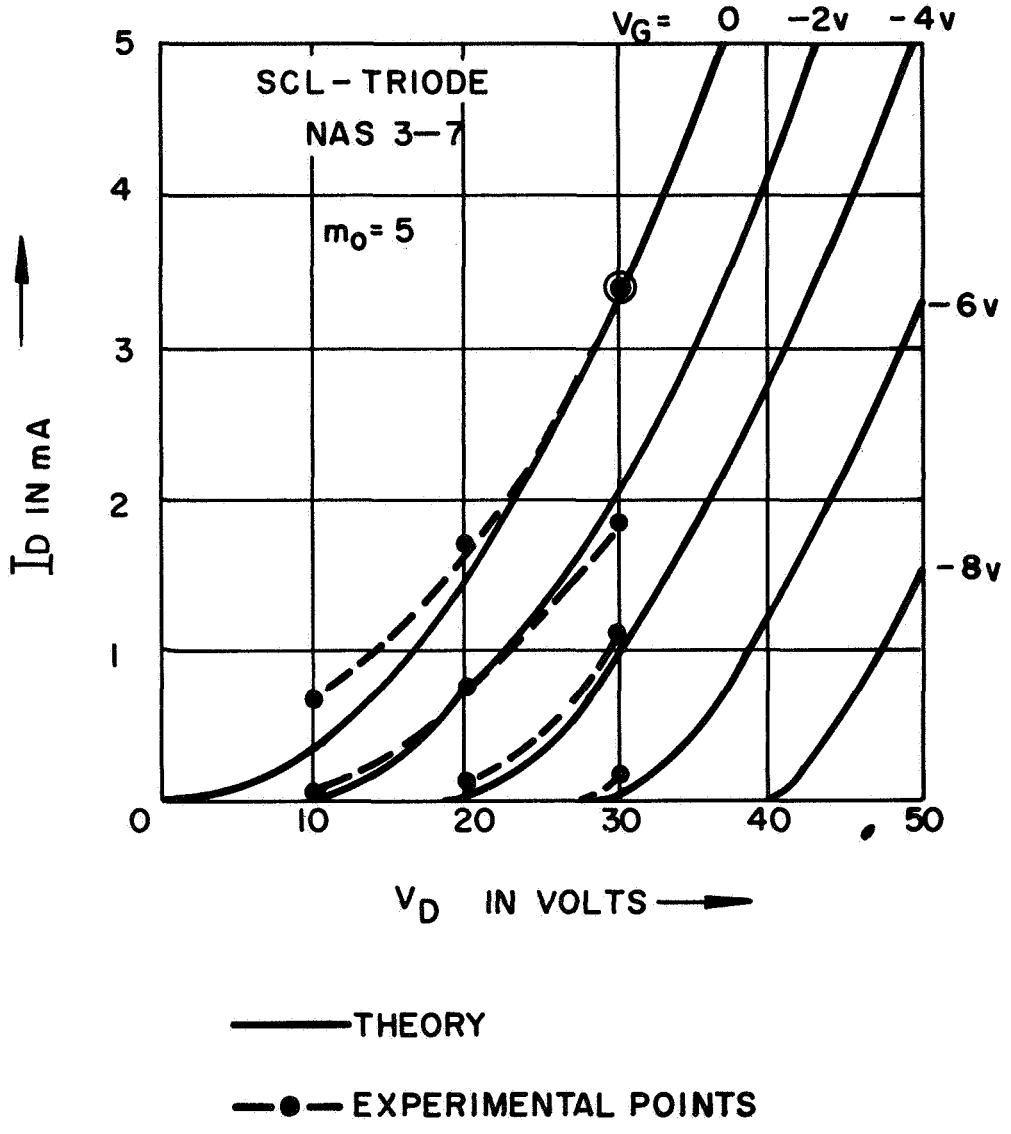
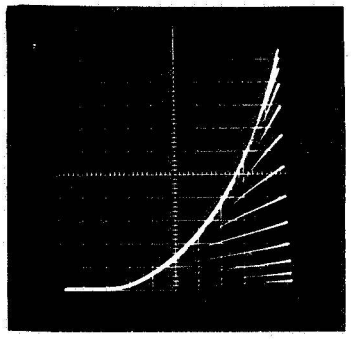


Figure 12: First Order Theory and Experimental Data From Figure 9 for SCL-Triode

V_D I_D - CHARACTERISTIC OF SCL-TRIODE

(P Silicon-on-Sapphire Structure)

Si Film Thickness	1μ
SiO_2 - Gate Oxide	1000 Å
Channel Length	L_D = 10μ
Channel Width	W = 625μ
Gate Width	L_G = 5μ



Device NAS 4-1

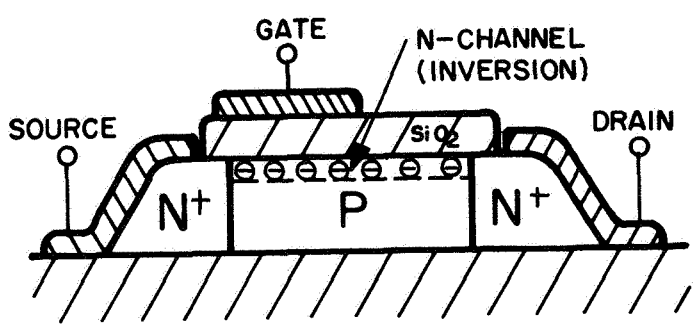
Scales:

Horizontal V_D in 10V/DIV.

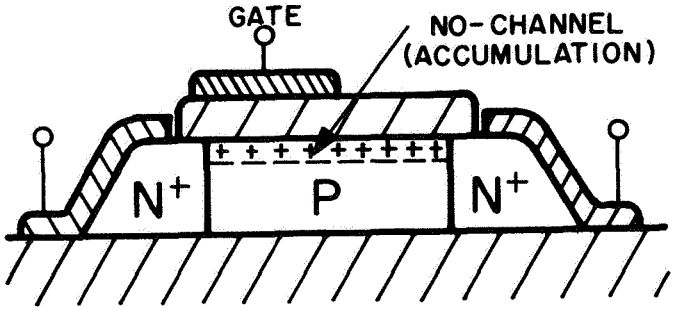
Vertical I_D in 1mA/DIV.

Positive Gate in 1V/STEP

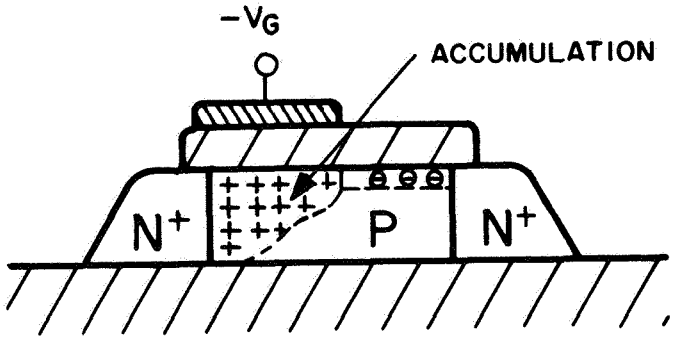
Figure 13



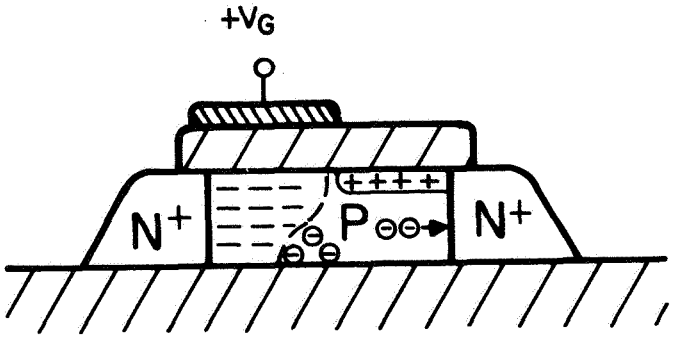
a) ZERO GATE BIAS



c) ZERO GATE BIAS



b) CUT-OFF CONDITION

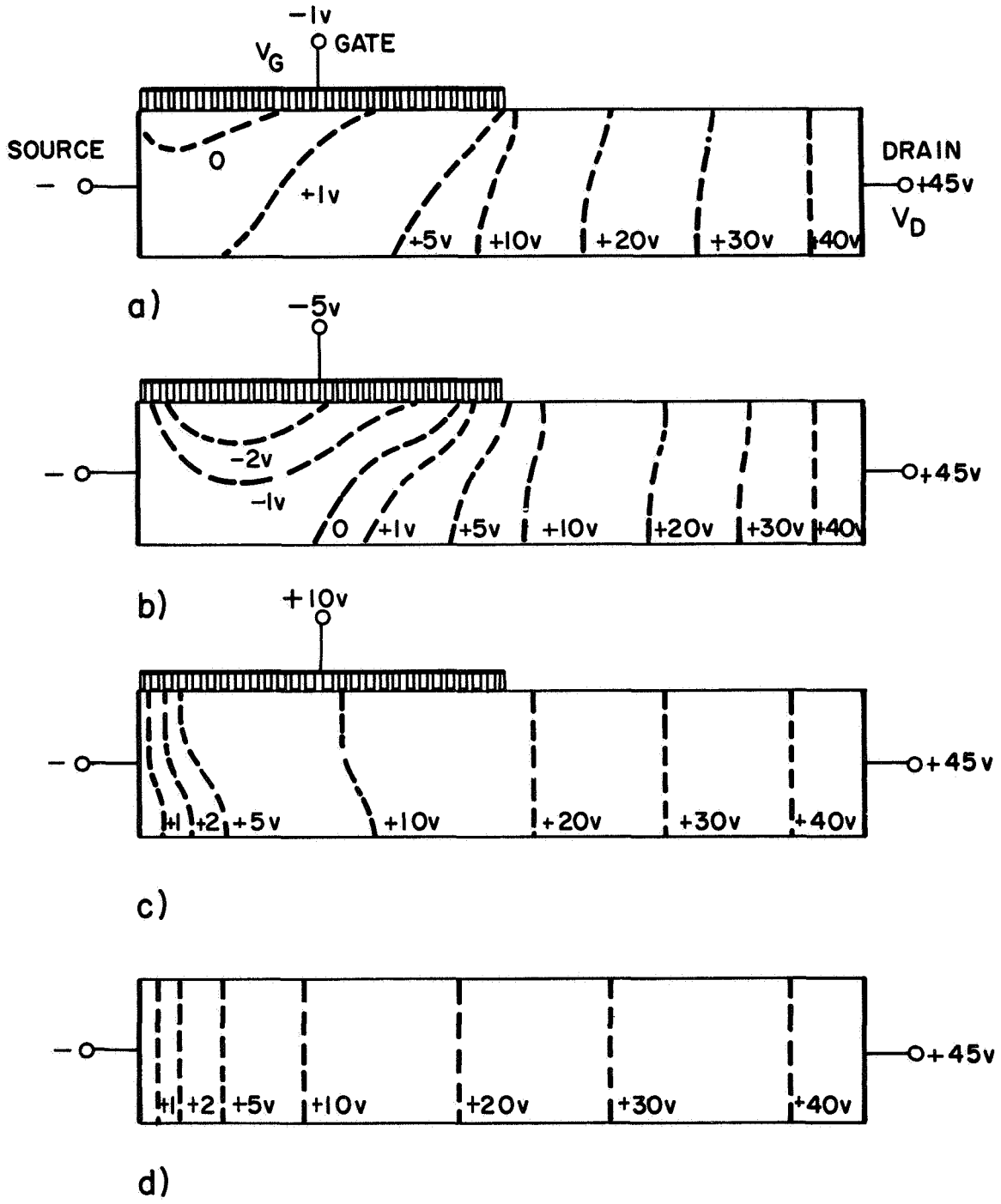


d) ENHANCEMENT CONDITION

NEGATIVE GATE OPERATION

POSITIVE GATE OPERATION

Figure 14 Charge Distribution for Negative and Positive Gate Operation.



EQUIPOTENIAL LINES ON 10 KΩ/□ TELETELDOS PAPER FOR VARIOUS GATE POTENTIALS

Figure 15

gate in the silicon-on-sapphire structure was simulated by cutting slots into the paper with a 4 to 1 length-to-width ratio. This geometrical modification reduces the dc current flowing in the gate loop. Figure 15 gives the equipotential lines for a device geometry with $L_D/h = 5$ and $h/t = 8$. The drain voltage was +45 volts in all cases. Figure 15(a) with $V_G = -1$ v shows the opposing field action to electrons emanating from the source contact. Figure 15(b) with $V_G = -5$ v demonstrates the cut-off condition for electron flow. The positive gate voltage operation with $V_G = +10$ v is shown in Figure 15(c) indicating the acceleration of electrons in the vicinity of the source-gate region. The uniformity of the conductivity paper, with removed gate contact and simulated insulation, is shown in Figure 15(d).

B. HIGH FREQUENCY PERFORMANCE

The devices mounted on TO-5 headers from lot NAS-10A were electrically evaluated. These devices exhibit dc transconductances of 4 to 6 mA/volt for a drain separation of 4 to 6 μm. The devices from contract NAS 12-5 measured dc transconductances of 1 to 2 mA/volt for a drain separation of 8 to 10 μm. Since the transconductance increase should be inversely proportional to the square of the source-drain spacing, a reduction of L_D by a factor of two should increase the transconductance by a factor of four. If the feedback capacitance, C_{12}, is then the same, the maximum frequency of oscillation

$$f_{max} \simeq \frac{g_m}{2\pi C_{12}} \tag{11}$$

should also be increased by a factor of four. This was confirmed by measurements of Y-parameters and power gain. For comparison a set of Y-parameters for SCL-triode NAS 3-6 with $L_D \simeq 8$ μm is shown in Figure 16 and for SCL-triode NAS-10A with $L_D \simeq 4$ μm is shown in Figure 17. The device NAS 3-6 with $L_D = 8$ μm has a $f_{max} \simeq 1$ GHz and the device NAS-10A with $L_D = 4$ μm has a $f_{max} \simeq 4$ GHz as expected from the reduction of L_D and the resulting increase in g_m. It is striking and should be remarked that the feedback capacitance C_{12}, where $Y_{12} = \omega C_{12}$, is the same for both devices

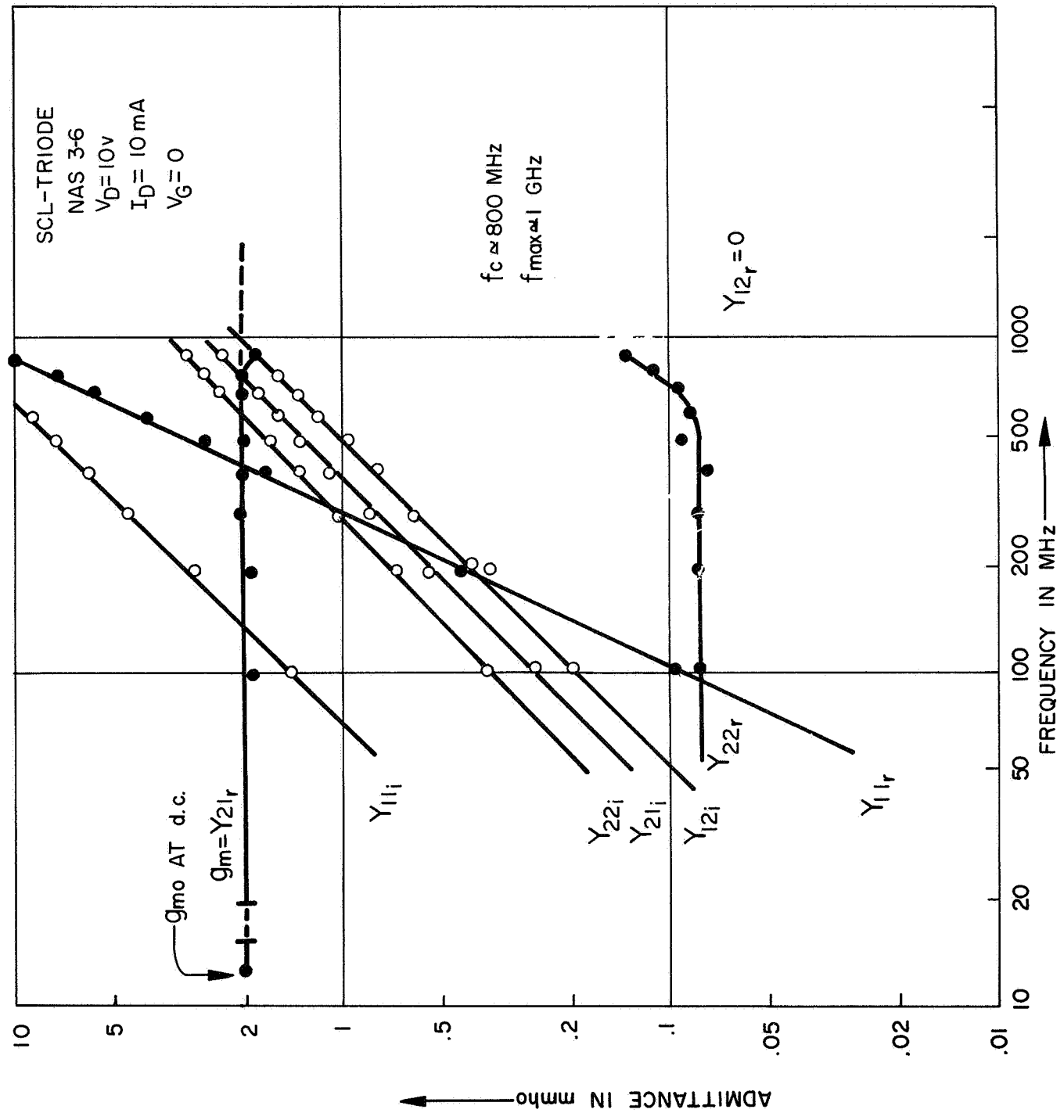

SCL-TRIODE
NAS 3-6
V_D= 10v
I_D= 10 mA
V_G= 0
$f_c \approx 800$ MHz
$f_{max} \approx 1$ GHz
$Y_{12_r}=0$
g_{mo} AT d.c.
$g_m=Y_{21_r}$
Y_{11_i}
Y_{22_i}
Y_{21_i}
Y_{12_i}
Y_{22_r}
Y_{11_r}
ADMITTANCE IN mmho
FREQUENCY IN MHz
10
5
2
1
.5
.2
.1
.05
.02
.01
10
20
50
100
200
500
1000

Figure 16

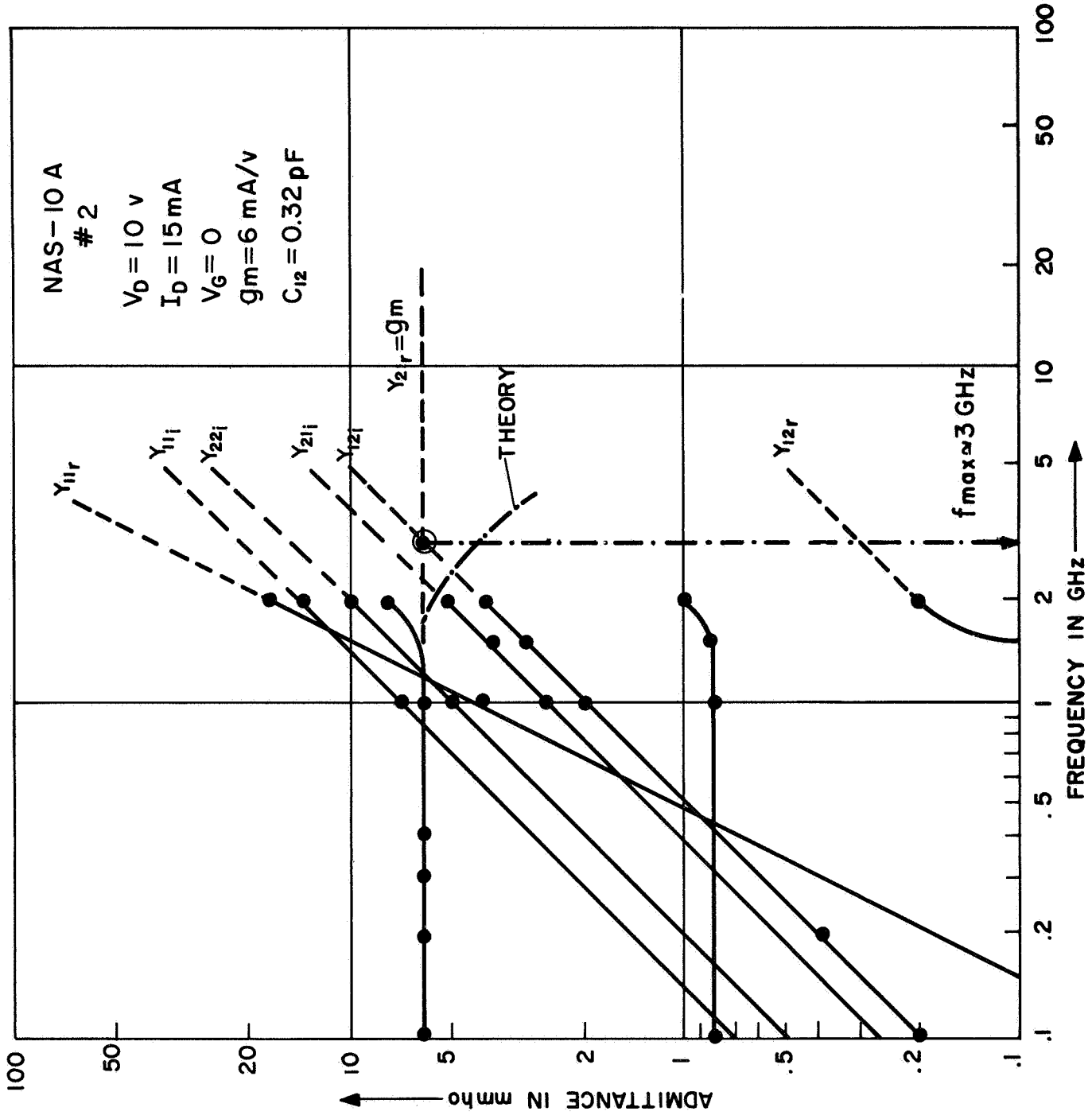

NAS-10 A
#2
V_D = 10 v
I_D = 15 mA
V_G = 0
gm = 6 mA/v
C_{12} = 0.32 pF
Y_{11r}
Y_{11i}
Y_{22i}
Y_{21i}
Y_{12i}
Y_{2r}=gm
THEORY
Y_{12r}
fmax≈3 GHz
ADMITTANCE IN mmho
FREQUENCY IN GHz
100
50
20
10
5
2
1
.5
.2
.1
.1
.2
.5
1
2
5
10
20
50
100

Figure 17

having the same width w = 6.25×10^{-2}cm (25 mils). Since this capacitance in combination with the transconductance according to Equation 11 gives the frequency limitation of the device, it was further analyzed to determine its physical origin. Compared to a regular MOS-transistor with full gate extending from source to drain, the recessed or offset gate structure (Ref. 40) has the advantage of presenting the lowest possible dielectric feedback capacitance. The capacitance can be given by two conducting plates (the drain and source electrodes) in one plane. The solution for the capacitance of such a configuration leads to elliptic integrals, but by expanding the complete elliptic integral in series and neglecting terms of higher order, the following equation was derived:

$$C_f \simeq \frac{\varepsilon \varepsilon_o W}{\pi} \ln\left(\frac{4b}{a}\right) \qquad (12)$$

where W is the width of the gate and drain electrodes, $a = (L_D - L_G)/2$ and $b = (L_D + L)/2$. With $L_D = 10$ μm, $L_G = 5$ μm and electrode length $L = 2.5 \times 10^{-2}$cm (10 mils), Equation (12) gives for the present devices with $W = 6.25 \times 10^{-2}$cm and $\varepsilon = 11$

$$C_f \simeq .12\text{pF}$$

Changing L_D or L_G in the device structure produces only small changes in C_f, since the logarithmic function varies very slowly when $\frac{a}{b} > 10$. The constant device capacitance, in spite of the geometrical variations from the 10 μm to the 5 μm source-drain spacing, is therefore attributed to the capacitance derived from W, a, and b plus the parasitic header capacitance, C_p, which was measured at 100 MHz and amounts to 0.2 pF. From the Y_{12i} measurement a total capacitance of 0.3 pF is calculated which is approximately the sum of the theoretical feedback capacitance $C_f \simeq .12$ pF and the measured parasitic header capacitance $C_p \simeq .2$ pF. This low feedback capacitance, C_{12}, renders the SCL-triode unconditionally stable up to the maximum frequency of oscillation. The device structure is suitable for distributed amplifier design and could lead eventually to a

traveling-wave transistor as described by McIver (Ref. 46) for a bulk silicon MOS-structure.

Microwave properties of SCL-triodes, when mounted in TO-5 encapsulations, cannot be realized above 1 GHz since the package has a self-resonance frequency anywhere from 800 MHz to 2 GHz depending upon the parasitic device capacitance plus the header capacitance and the lead inductance of the wirebond. For the present devices $f_{res} \simeq 1.5$ GHz. The resonance effect causes $Y_{21r} = g_m$ to increase, rather than decrease, at the resonance frequency, as indicated by the measurement in Figure 17. The power-gain of device NAS-10A at 1, 1.5 and 2 GHz was measured in the GR-Transfer Function Bridge at a perfect $\lambda/4$ - tuning of the input and output line without compensation of the parasitic elements of the device itself, and with compensation by tuning the lines slightly to obtain matched and maximum available power gain. Both measurements are presented in Figure 18 and reveal a 6db/octave power-gain fall-off with extrapolated maximum frequencies of oscillation of 3.2 GHz and 4 GHz respectively. This value is in good agreement with the Y-parameter measurement of the same device in Figure 17, where at $Y_{21r} = Y_{12i}$ a frequency of 3 GHz is obtained.

The frequency response of SCL-triodes with the recessed gate structure was investigated with respect to optimal geometrical control using photolithographic techniques and the silicon-on-sapphire material. Experimental points for f_{max} vs. L_D for device structures with varying L_D, the distance separating source and drain contact, are presented in Figure 19. Present state-of-the-art photolithographic technologies have produced devices with $L_D = 4\ \mu m$ ($.4 \times 10^{-4}$ cm). With a transconductance of 5 mA/volt and a feedback capacitance of 0.3 pF at $V_D = 10$ volts and $I_D = 10$ mA, the maximum frequency of oscillation was 4 GHz. For devices with larger L_D values, transit time effects reveal a theoretical relation of

$$f_{max} = \frac{1}{2\pi\tau} \tag{13}$$

where

$$\tau = \frac{L_D^{\,2}}{\mu V_D} \tag{14}$$

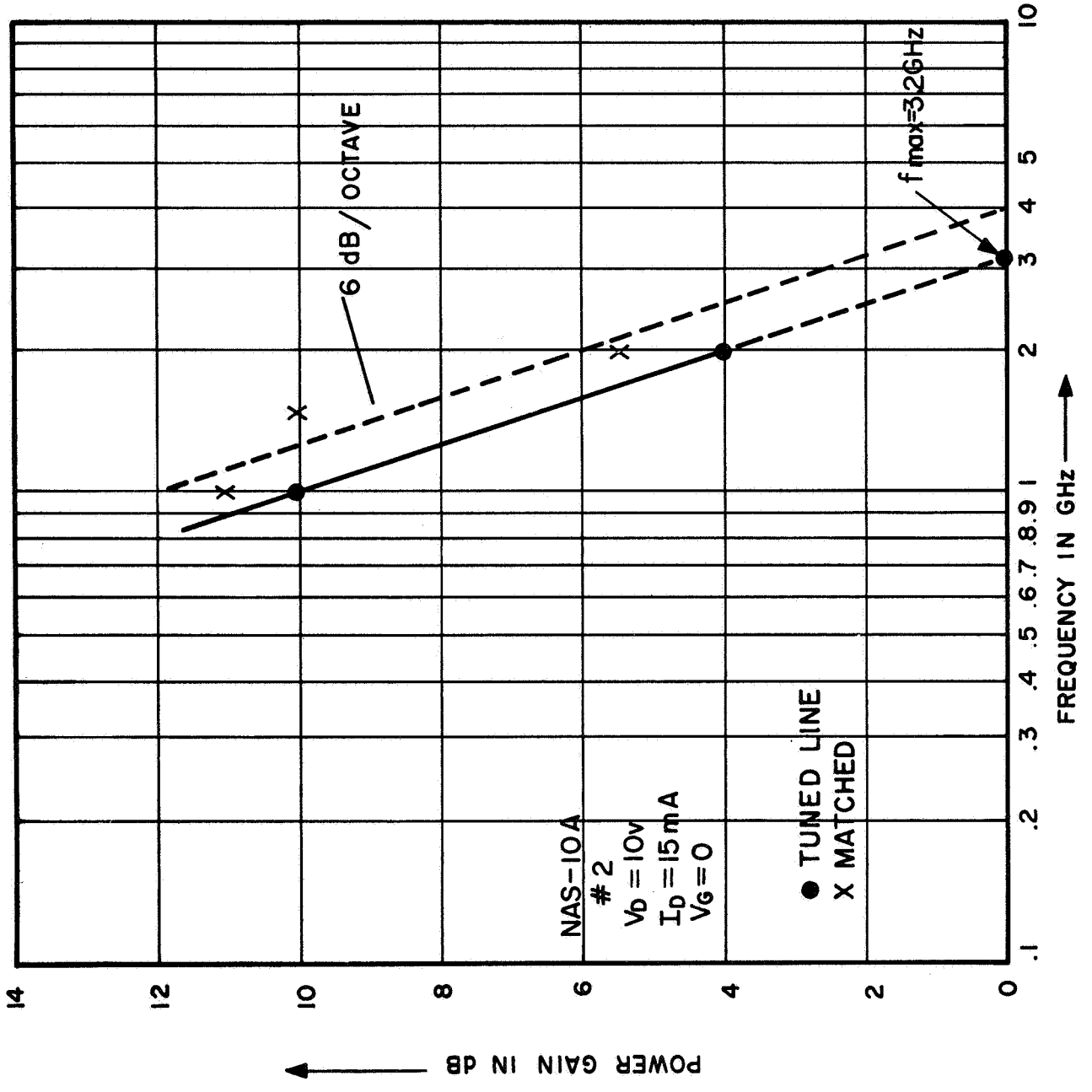

f max=32GHz
6 dB/OCTAVE
NAS-104
#2
V_D = 10v
I_D = 15 mA
V_G = 0
● TUNED LINE
X MATCHED
FREQUENCY IN GHz
POWER GAIN IN dB
14
12
10
8
6
4
2
0
.1
.2
.3
.4
.5
.6
.7
.8
.9
1
2
3
4
5
10

Figure 18

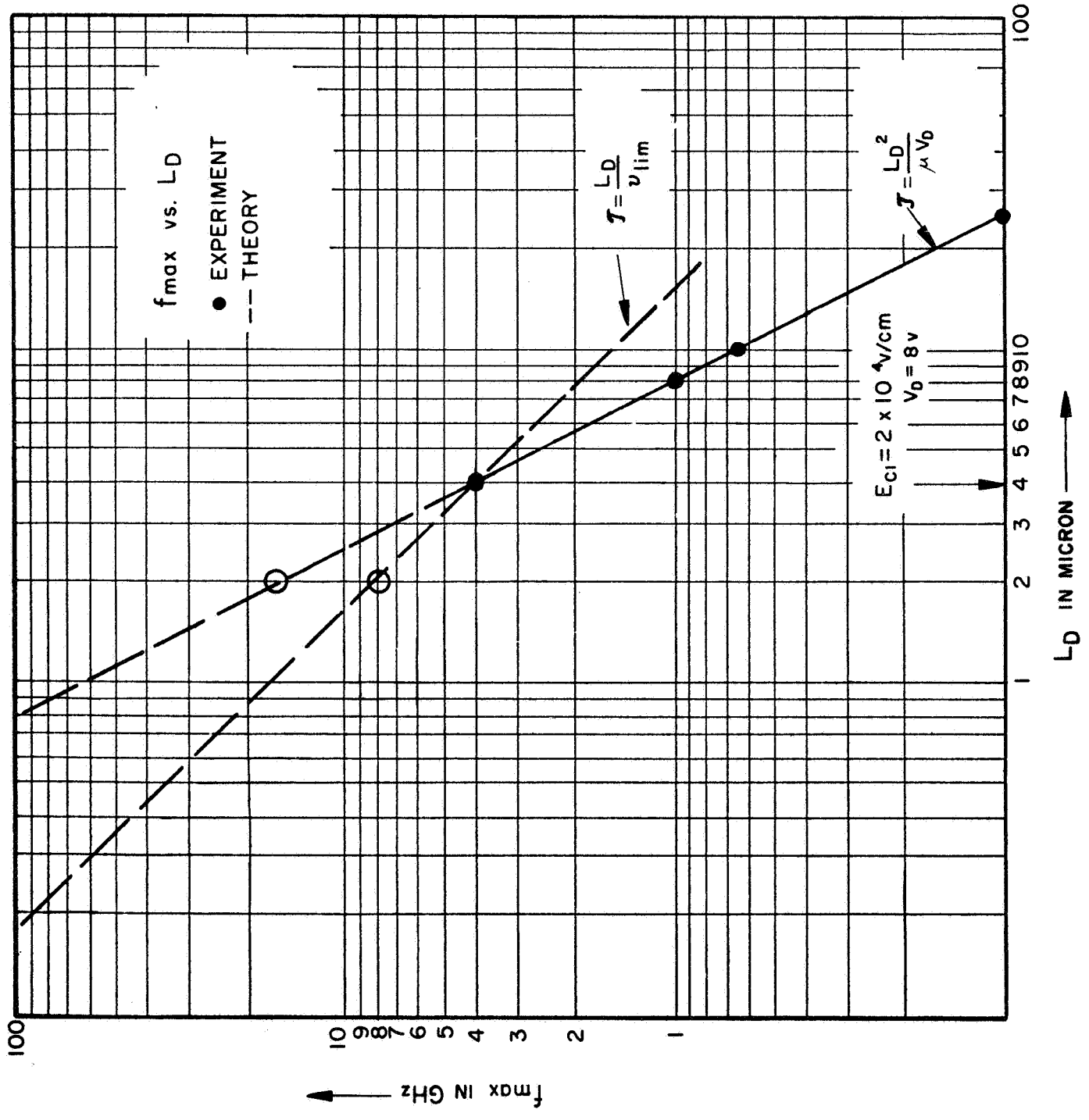

f_{max} vs. L_D
● EXPERIMENT
— — THEORY
$\tau = \frac{L_D}{v_{lim}}$
$\tau = \frac{L_D^2}{\mu V_D}$
$E_{C1} = 2 \times 10^4$ v/cm
$V_D = 8$ v
f_{max} IN GHz
L_D IN MICRON
100
10
9
8
7
6
5
4
3
2
1
100
1
2
3
4
5
6
7
8
9
10

Figure 19

This relation is experimentally confirmed (see Figure 19) for L_D values larger than 4 μm. For devices with L_D smaller than 4 μm the onset of hot electron behavior at an electric field, E, greater than 2×10^4 V/cm will result in a transit time of

$$\tau = \frac{L_D}{v_{lim}}$$

where v_{lim} is the limiting velocity of the hot electrons. The maximum frequency of oscillation, f_{max}, is therefore proportional to L_D^{-1} in this range of electric fields according to Equation (13). With improved photolithographic techniques and silicon-on-sapphire material, device structures with $L_D \simeq 2$ μm should be possible with a visualized potential application in the microwave frequency region up to 8 GHz.

C. MODES OF OPERATION

In a first order approximation the current-voltage characteristics of the thin-film space-charge limited triode with dielectric surface gate can be represented by:

$$I_D = \frac{\mu_n C_D}{L_D^2} (V_D + V_G)^2 \left[1 + \left(\frac{L_D}{L_G} \right)^2 \frac{|V_G|}{(V_D + |V_G|)} \right] \qquad (15)$$

for the positive gate operation. Equation (15) reduces to:

$$I_D \simeq \frac{\mu_n C_D}{(L_D - L_G)^2} V_D^2 \left[1 + \left(\frac{L_D}{L_G} \right)^2 \frac{|V_G|}{(V_D + |V_G|)} \right] \qquad (16)$$

when the virtual cathode for electrons moves close to the edge of the gate electrode on the side of the drain contact. For the negative gate operation the drain-current is given by:

$$I_D = \frac{\mu_n C_D}{L_D^2} (V_D - V_G)^2 \left[1 - \left(\frac{L_D}{L_G} \right)^2 \frac{|V_G|}{(V_D - |V_G|)} \right] \qquad (17)$$

It is evident when comparing Equation (16) with (17), that the positive gate operation should have the higher frequency response, since the electron

transit time is always less in this mode of operation compared to a geometrically equal structure operating with negative gate voltage. This was confirmed experimentally by measuring the cut-off frequency of the transconductance $g_m = Y_{21r}$.

To explain the positive and negative gate operation of the space-charge-limited triodes, the built-in voltage at the SiO_2-Si interface has to be taken into consideration, which also gives an indication of the band bending in the "floating"channel. The "floating" channel is the portion between the edge of the gate electrode extending over to the drain pn-junction. The built-in voltage is given by:

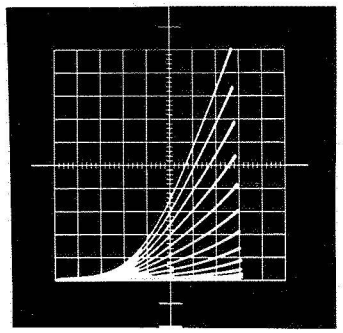
$$V_o = \pm \frac{qN_{CH}}{C_G} \tag{18}$$

where q is the electron charge and N_{CH} is the charge in the channel and C_G the gate capacitance. The positive sign of this voltage applies to an inversion layer and the negative sign to an accumulation layer for a p-type substrate. For standard MOS-transistors, V_o is identical to the threshold voltage V_{TH}, which can be easily determined from drain current-voltage characteristics in saturation as a function of applied gate voltage. This measurement is, however, not possible and meaningful for the space-charge-limited triode. The positive and negative gate operation of device NAS 2-9 and NAS 3-7, whose current-voltage characteristics at room temperature and liquid nitrogen temperature are shown in Figure 20 were correlated with gate capacitance versus gate voltage measurements. The C-V measurement on the space-charge-limited triodes replaces the dc method used with the pentode-like MOS-T with full gate, since the flat-band voltage V_{FB}, which can be determined from these measurements, is related to the threshold voltage V_{TH} and the built-in voltage V_o. When the conduction and valence bands are flat out to the SiO_2-Si interface, there is zero space-charge within the Si. The capacitance per unit area of the silicon surface at this "flat-band" condition is given by:

$$C_{SFB} = q(\epsilon\epsilon_o N/kT)^{1/2} \tag{19}$$

VOLTAGE-CURRENT CHARACTERISTICS OF THIN-FILM SPACE-CHARGE LIMITED TRIODES (SILICON ON SAPPHIRE)

POSITIVE GATE VOLTAGE OPERATION
(Cut-Off at V_G = O)

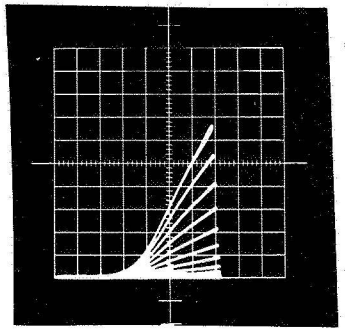


V_G = +12V

Temp = 300°K

V_G = O

DEVICE NAS 2-9



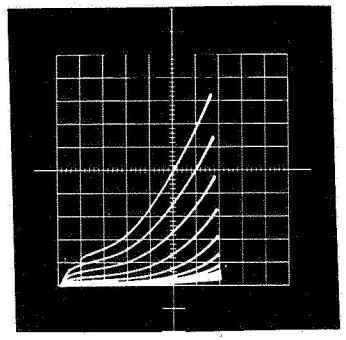
V_G = +12V

Temp = 77°K

V_G = O

IDENTICAL SCALES:
Vert. I_D in 0.5 mA/DIV.
Horiz. V_D in 5V/DIV.
Pos. V_G in 1V/STEP

NEGATIVE GATE VOLTAGE OPERATION
(Conducting at V_G = O)

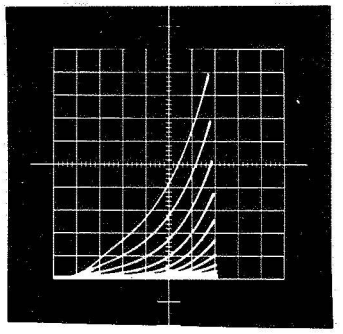


V_G = O

Temp = 300°K

V_G = -12

DEVICE NAS 3-7



V_G = O

Temp = 77°K

V_G = -12V

IDENTICAL SCALES:
Vert. I_D in 0.5 mA/DIV.
Horiz. V_D in 5V/DIV.
Neg. V_G in 1 V/STEP

Figure 20 Voltage-Current Characteristics of Thin-Film Space-Charge-Limited Triodes in Positive and Negative Gate Operation at 300°K and 77°K.

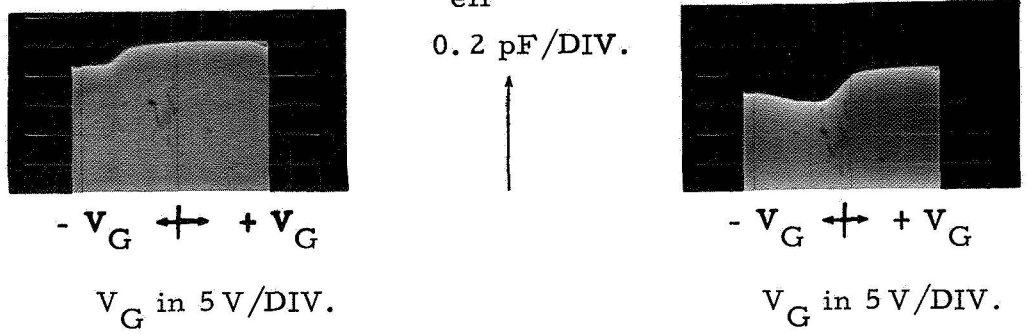
where q is the electron charge, $\epsilon\epsilon_o \simeq 10^{-12}$ F/cm for silicon and N is the bulk carrier concentration. This capacitance is in series with the SiO_2 dielectric capacitance C_G and gives a fractional device capacitance decrease of

$$\frac{\Delta C}{C_G} = \frac{C_G}{C_G + q(\epsilon\epsilon_o N/kT)^{1/2}} \qquad (20)$$

in going from the maximum capacitance of the accumulation condition to the flat-band point. The C-V measurements for devices NAS 2-9 and NAS 3-7, whose output characteristics are presented in Figure 20, are shown in Figure 21. For this measurement a 500 KHz ac signal was used and the gate voltage was swept from positive to negative polarity with a triangular wave form of 5 Hz.

From these measurements it is concluded that negative gate voltage operation of device NAS 3-7 is caused by a positive built-in voltage of about seven volts, and the positive gate voltage operation of device NAS 2-9 is possible when the built-in voltage is zero or negative. The charge distribution of electrons and holes at zero gate bias condition and cut-off condition for the negative gate operation is shown in Figure 14. Since negative gate operation has a conducting channel at $V_G = 0$ (Figure 14a), sufficient negative gate bias is required to cut off the device by depleting the surface under the gate electrode from electrons and accumulating holes to prevent the space-charge region from punching through the p-layer (see Figure 14b). In the positive gate operation, the surface condition is near flat-band or slightly depleted of negative charges at zero gate bias (see Figure 14c). Applying a positive gate voltage will cause n-type inversion under the gate p-region and electron accumulation. The virtual cathode for electrons moves closer to the drain. At very high gate voltages, the transconductance starts to "crowd" and modulation from the gate bias becomes ineffective. This was experimentally verified and indicates space-charge-limited operation of a diode with the electron source located at the gate edge.

The operation as positive or negative gate space-charge-limited triode can be controlled by processing. To obtain the devices with zero



Device NAS 3-7
$V_{FB} \simeq +7$ volts

Device NAS 2-9
$V_{FB} \simeq 0$

Figure 21 Capacitance vs. Voltage Measurements of Device NAS 2-9 and NAS 3-7.

built-in voltage a P_2O_5 treatment of the thermally grown SiO_2 gate oxide is used. The standard cycle is carried out at 930°C for 15 minutes in an atmosphere of $POCl_3$.

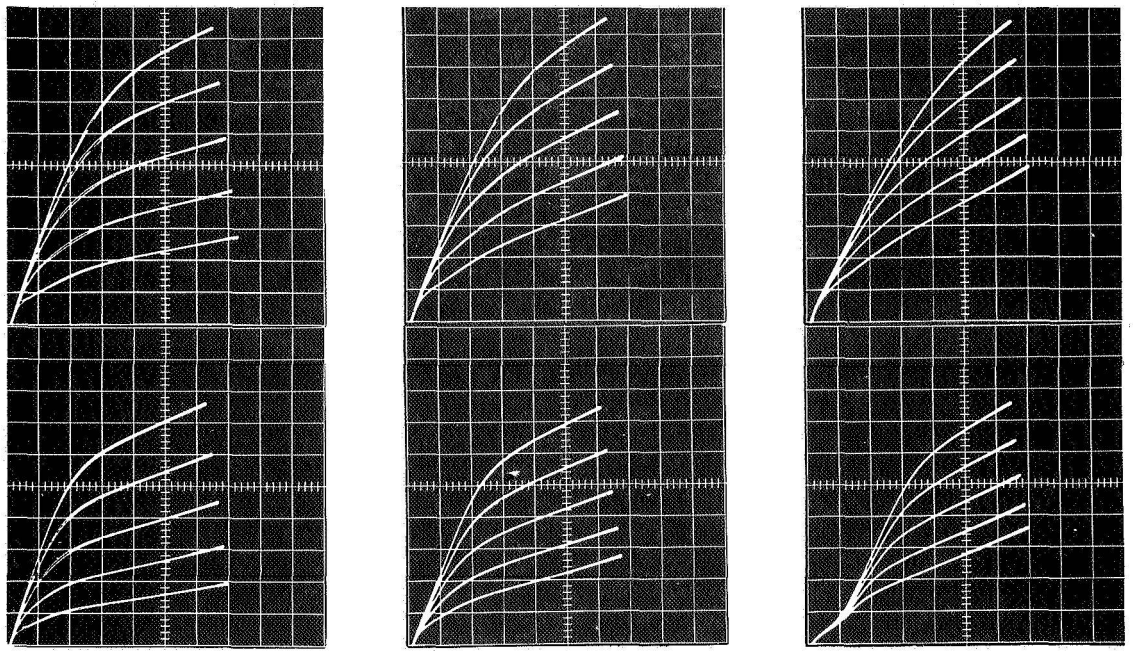
The devices with a positive built-in voltage are fabricated by using a prolonged P_2O_5 treatment of the SiO_2 gate oxide. Since phosphorus is an n-type impurity, diffusion takes place into the silicon surface through the thin SiO_2 and a fixed n-type channel is created by pn-junction formation.

D. HIGH TEMPERATURE STABILITY

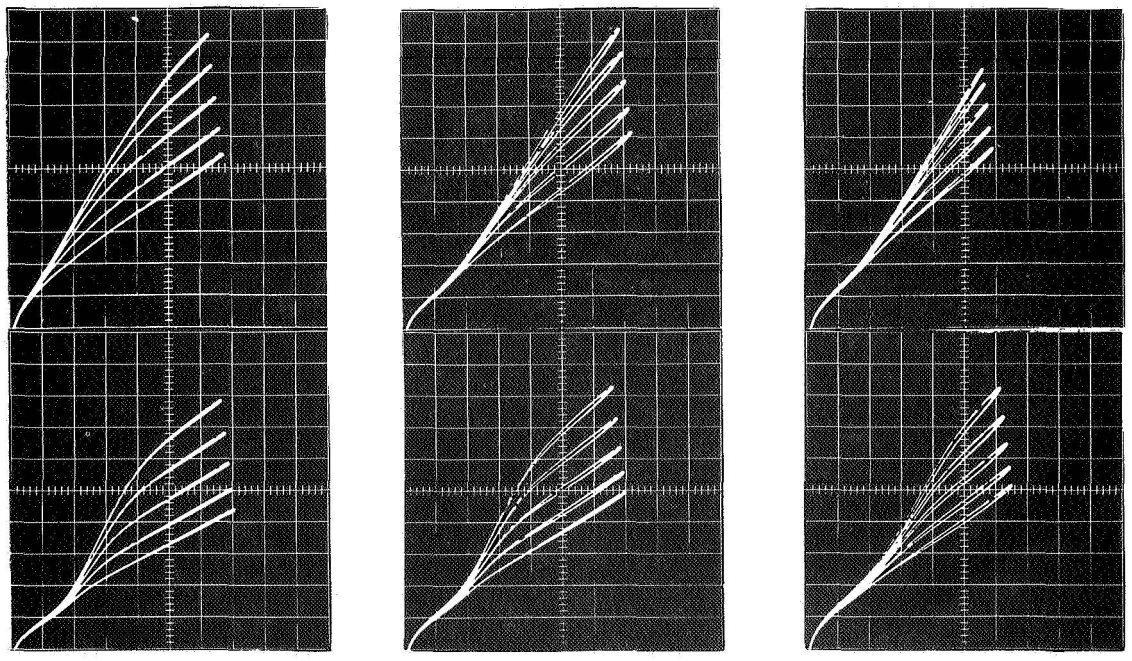
In order to determine how well the SCL-triodes perform at elevated temperatures, two devices from lot NAS-17 were placed in a temperature chamber and their characteristics observed as the temperature was raised. The devices were not continuously biased, but were turned on briefly to obtain photographs from the curve tracer at 25° intervals up to a maximum temperature of 250°C. Figure 22 shows the characteristics observed at the various temperatures. The upper device in each set of photographs has geometry No. 2, while the lower has geometry No. 1. The devices were operated in the enhancement mode (positive gate voltage). As can be seen in Figure 22(e) and (f), the devices exhibit some hysteresis at 225° and 250°. But a more serious problem is the appearance of what appears to be an increase in the drain series resistance. This first occured at 125°C in the device with geometry No. 1. Figure 23 shows the characteristics of the devices after cooling down to room temperature. It is obvious that permanent changes have occurred in both devices. Since the source-drain doping level is not high enough to assure good ohmic contacts, the most obvious explanation for the changes observed is an increase in drain series resistance. However, the fact that the contacts become worse at high temperatures throws some doubt upon this explanation.

E. RADIATION EFFECTS

The major effect of γ-radiation on the thin-film space-charge-limited triode with dielectric surface gate is a shift in gate threshold voltage, V_0, as in the case of insulated gate pentodes. A change in V_0 by γ-radiation is usually caused by creation of positive charges in the SiO_2 near the



a) T = 25°C b) T = 100°C c) T = 150°C



d) T = 200°C e) T = 225°C f) T = 250°C

Scale: 2 ma/division vertical
5 volts/division horizontal
1 volt/step

Figure 22: Voltage Current Characteristics of Devices NAS 17B-2A and NAS 17B-2B at Various Operating Temperatures

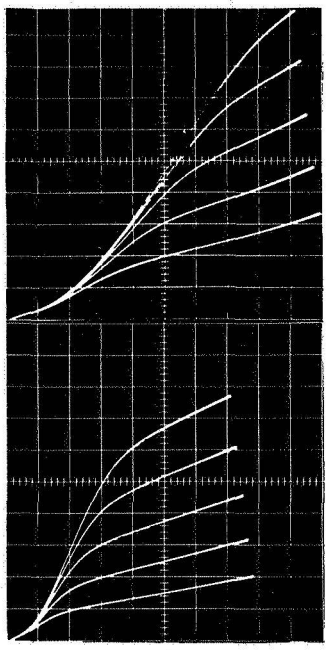


Figure 23: Voltage Current Characteristics of Devices NAS 17B-2A and NAS 17B-2B at 25°C Showing Permanent Changes After Operation at Elevated Temperatures

$Si\text{-}SiO_2$ interface, which induce negative charges at the silicon surface. Because of the functional relation between the drain current and drain and gate voltage, the triode device is less sensitive to a given dose of radiation than the equivalent pentode, operated at the same current. In the saturated MOS-transistor the changes in the channel are entirely controlled by the gate voltage so that the drain saturation current is independent of drain voltage and is given by:

$$I_{DS} = \frac{\mu_n C_G}{2L_D^2} \quad (V_G + V_0)^2 \tag{21}$$

At a particular operating point, the change of I_{DS} as a consequence of V_0 changes is given by:

$$\Delta I_{DS} = + \frac{2I_{DS}}{(V_G + V_0)} \quad \Delta V_0 \tag{22}$$

In the space-charge-limited triode the space charge is controlled not only by the gate voltage but also by the drain voltage. The current-voltage characteristics are given by:

$$I_D = \frac{\mu_n C_D}{2L_D^2} \left[(V_D+V_G+V_0)^2 + \left(\frac{L_D}{L_G}\right)^2 (V_D+V_G+V_0)(V_G+V_0) \right] \tag{23}$$

The change of I_D as a function of V_0 is then approximately:

$$\Delta I_D \simeq + \frac{2I_D}{(V_D + V_G + V_0)} \quad \Delta V_0 \tag{24}$$

To compare the two devices, we assume that both operate at the same current, that is, $I_D = I_{DS}$, and that for an equal exposure dose, ΔV_0 will be the same; then by equating Equations (22) and (24), we obtain:

$$\Delta I_D = \Delta I_{DS} \frac{V_G + V_0}{V_D + V_G + V_0} \tag{25}$$

For V_D greater than zero, the change in drain current of the triode, ΔI_{DS}, is smaller than the drain current change ΔI_{DS} of the pentode by a factor of:

$$F = \frac{V_G + V_0}{V_D + V_G + V_0} \qquad < 1$$

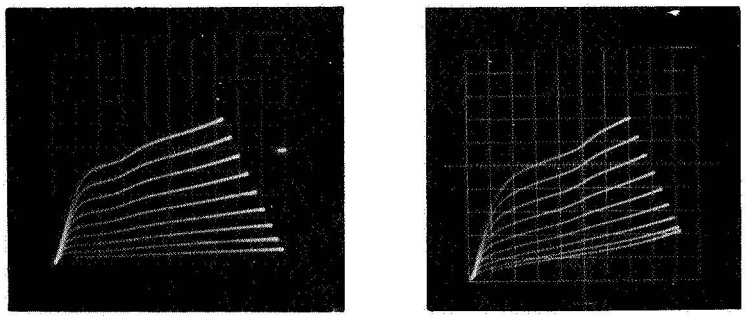
The first radiation tests performed under this contract were performed on a full-gate thin-film MOST and a half-gate thin-film SCL-triode (NAS 1-7). Figure 24 shows the current-voltage characteristics of both devices before and after being exposed to a total dose of 10^4 rads from the LINAC. Some change is seen in the characteristics of each device, but the changes are not large enough for any conclusion to be drawn regarding the relative radiation sensitivities of the pentode and triode.

The next radiation experiments were carried out on device NAS 6-10, geometry 4. The current-voltage characteristics before and after radiation exposure are shown in Figure 25. After a total dose of 2×10^5 rads from the LINAC, a positive ΔI_D of about 0.2 mA is observed for every operation point. It was not determined whether this change of I_D arose from a change of V_0, or if it arose from an ohmic leakage current introduced in the floating channel or across the drain pn-junction in parallel with the normal current.

A radiation-hardened version of the SCL-triode was designed (see Figure 7) but was not fabricated. It was felt that, although some increase in radiation resistance might result, this would be attained at the price of instabilities due to the nonpassivated channel region. In addition, the phosphorus-doped oxide etches extremely rapidly, so that some etching of the oxide under the gate would certainly occur, resulting in many shorted gates. There are, however, some other approaches to radiation-hardening which appear promising.

Early in the contract period, several attempts were made to fabricate devices with insulators other than thermally grown SiO_2. The search for other suitable insulators is motivated primarily by a desire for increased radiation resistance. Silicon nitride, in particular, has attracted considerable interest as a radiation-resistant insulator for field-effect devices. Unfortunately, the silicon nitride cannot be etched with standard photoresist techniques because the etch rate is so slow that the photoresist lifts off before the

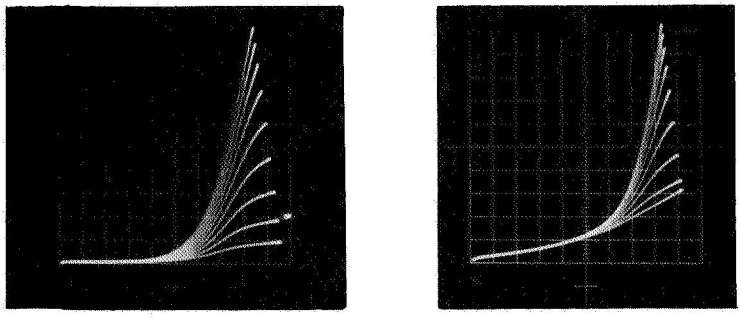
RADIATION EXPOSURE OF THIN-FILM MOST WITH FULL GATE AND THIN-FILM SCL-TRIODE WITH HALF GATE



Before Irradiation

After

1 Vert I_D = 2mA/DIV
Horiz. V_D = 5V/DIV
Gate V_G = +1V/STEP



Before Irradiation

After

2 Vert. I_D = 1mA/DIV
Horiz. V_D = 10V/DIV
Gate V_G = +1V/STEP

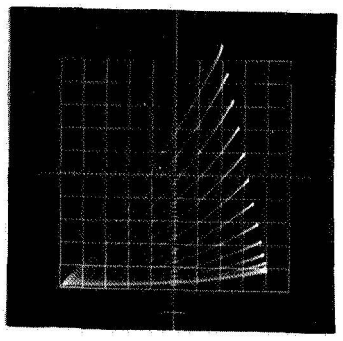
Exposure to a total dose of 10^4 RADS from LINAC

Figure 24

THIN-FILM SPACE-CHARGE-LIMITED TRIODE

(NAS 6-10, Geometry 4)

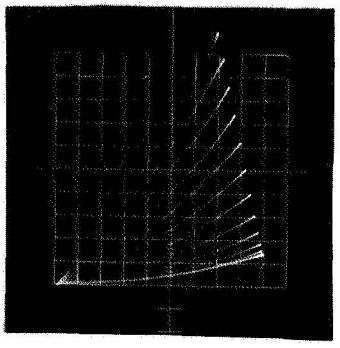
Before Radiation



Identical Scales of

Vert. I_D in 0.5 mA/DIV.
Horiz. V_D in 5 V/DIV.
Positive Gate Voltage in 1 V/STEP

After Radiation



Total Dose of 2×10^5 rads (from LINAC)

Figure 25 Voltage-Current Characteristics of Space-Charge-Limited Triode NAS 6-10 before and after Exposure to γ-Rays. Total Dose 2×10^5 RADS.

silicon nitride is completely etched through. There is also considerable difficulty in forming nitride layers which are polarization-free. Because of these difficulties, no SCL-triodes were fabricated using silicon nitride as the gate insulator. However, some MNS (Metal-nitride-silicon) capacitors were fabricated.

In order to evaluate the silicon nitride insulator, comparative radiation damage experiments on supplied MNS- and MOS-capacitors were performed by Dr. C. W. Perkins of the Radiation Effects Research Department of Hughes Aircraft Company, Fullerton, California. The MNS capacitors were irradiated using the cobalt-60 facility at the Hughes Radiation Effects Research Laboratory. The following biases were applied in a sequence of irradiations, each of which incurred a maximum dose of 6×10^6 r: 0V, +2V, $\pm$20V. In all cases, except -20V, there was only a slight shift of 1-2 volts in the positive bias direction of the principal dips in the C-V and G-V curves for both p and n-types, and these shifts disappeared after a day or two or after heat treatment. The nature of the hysteresis in the p-types, however, changed considerably. The changes occurred in the positive direction of the bias sweep. In the inversion region, the C-V dip and the G-V peak broadened greatly. However, this effect is also seen in non-irradiated samples under prolonged biasing alone. These effects are attributed to accumulated negative charge on the insulator surface near the metal electrode, and are completely removed by heat treatment at 250°C. The irradiation at -20V up to 3×10^5 r resulted in a negative shift in the C-V dip and G-V peaks in a p-type capacitor indicating accumulated positive charge in the insulator as reported in the literature by other experimenters. More striking, however, was the complete disappearance of the G-V inversion peak and of the capacitance rise after the dip in the inversion region. This result indicates complete wiping out of the naturally occurring inversion layer at the silicon surface near the metal electrode. Partial recovery was achieved by heat treatment but some changes in the C-V and G-V curves appear to be permanent. Similar effects by prolonged bias of -20 volts alone were produced in another p-type unit; but in this case complete recovery by heat treatment was possible.

MOS n-type capacitors showed the usual negative shift in the C-V and G-V curves. The C-V dip was broadened, and the G-V peak both

broadened and increased in magnitude. The MOS types are nuch more sensitive to radiation than the MNS types. A 20-volt shift was produced by an accumulated dose of about 10^5r with a bias of +5 volts.

The superior radiation resistance of the silicon nitride is clear. The use of nitride appears to be the most promising method of radiation-hardening field-effect devices. However, considerable effort is needed before satisfactory silicon nitride layers can be reproducibly deposited. Some of the problems are:

1. There is a natural oxide skin which is always present between the silicon and the silicon nitride unless special precautions are taken. This oxide layer causes a hysteresis in the threshold voltage as a function of applied voltage (Ref. 45).
2. There is a bulk polarization which apparently depends on the relative amounts of silane and ammonia present during growth. It is difficult to control the flow rates of these gases with sufficient accuracy to eliminate the polarization.
3. Pure silicon nitride is not a good insulator. It can be made a good insulator by adding O_2 during growth.

F. NOISE

The noise in solid-state space-charge-limited diodes was theoretically investigated by Webb and Wright (Ref. 46), Sergiescu (Ref. 47) and van der Ziel (Ref. 48). Although the theories of these authors do not agree in their final results, they have in common a prediction of shot noise suppression in solid-state space-charge-limited diodes. A stronger noise suppression in the solid-state over the vacuum tube diode is ascribed to the fact that in vacuum diodes the velocity distribution of emitted electrons is preserved throughout their passage, whereas in the solid-state diode this velocity distribution is altered by collisions of the carriers with the lattice. This leads to the conclusion that convection current fluctuations at the potential minimum of the solid-state diode can be neglected. It is therefore speculated that the noise in solid-state diodes is more suppressed

by the presence of the space-charge than is the noise in vacuum diodes. This, of course, raises the hope that very low-noise operation of solid-state space-charge-limited triodes can be achieved.

Van der Ziel (Ref. 48) has shown that the short-circuited noise current in a space-charge-limited diode is given by:

$$\overline{i_a^2} = 8kT\, g\, \Delta f \qquad (26)$$

which is twice the thermal or Nyquist noise of the high frequency conductance g. In a space-charge-limited triode, one would consequently expect a noise current of:

$$\overline{i_a^2} = 8kT\, g_m\, \Delta f \qquad (27)$$

where g_m is the transconductance of the three terminal device.

A bulk silicon space-charge-limited triode (Ref. 49) was investigated with respect to its noise performance according to Equation (27)(Ref. 50). Although the devices under test showed 1/f noise, which arises possibly from surface states at the SiO_2-Si interface around the metal contacts in the planar structure, above 50 MHz the measured values $\overline{i_a^2}$ approach the values predicted by Equation (27). This indicates that the limiting noise in space-charge-limited solid-state triodes is thermal noise as was observed experimentally. Additional noise in an actual amplifier which uses the space-charge-limited triode will arise from the gate circuit elements.

CONCLUSION

The design and fabrication of a space-charge-limited triode has been presented, and the measured characteristics and parameters of the devices have been reported.

The silicon-on-sapphire used for the device fabrication has an (100) orientation, and the best films were grown at an indicated temperature of 1050°C. Films grown at higher temperatures were less oriented and exhibited lower mobilities. The high temperature limitation for the film growth apparently is due to a chemical reaction between silicon and sapphire which is enhanced with increasing temperature.

The yield of operable devices was generally low, and is attributable to source-drain shorts caused by defects in the silicon films. Considerable improvement in the structural quality of the films is needed in order to obtain controllable diffusions, and in turn, higher yields. Such improvements should be forthcoming in the near future. It should be borne in mind, however, that because of the lattice mismatch between silicon and sapphire, the structural perfection of the films will probably not approach that obtained with silicon-on-silicon epitaxial layers.

It was found that the p-type films increase in resistivity upon being oxidized, probably due to depletion of the aluminum dopant from the films.

Problems were initially encountered due to fracturing of the aluminum gate electrodes at the edge of the silicon islands, but these problems were solved by obtaining a tapered edge on the islands.

It was found that the zero-gate-voltage currents drawn by the devices as a function of drain voltage were less than those predicted by the Guerst and Mott-Gurney theories, but larger than those predicted by the Wright and Rittner-Neumark theories.

The maximum frequency of oscillation obtained was 3 to 4 GHz, which agreed with the predicted frequency obtained from the transconductance of the device and the feed-back capacitance. The feed-back capacitance of the device was calculated to be 0.12 pf, and the parasitic header capacitance was measured to be 0.2 pf. The total feed-back capacitance of 0.3 pf renders the SCL-triode unconditionally stable up to the maximum frequency of

oscillation. An increase in frequency response should be obtainable with a further reduction in source-drain spacing. However, TO-5 headers have a self-resonance frequency of about 1.5 GHz, so the SCL-triode would have to be designed as a distributed amplifier in order to be useable at microwave frequencies. The sapphire substrate is especially well suited for such a design.

The SCL-triodes can be either enhancement mode or depletion mode, depending on the built-in voltage. A higher frequency response is expected from the positive gate (enhancement mode) operation.

An analysis was made which indicated that the SCL-triode should be somewhat less sensitive to ionizing radiation than the full-gate MOST, but this was not verified experimentally. Comparative radiation tests on MOS and MNS capacitors showed that silicon nitride is much less sensitive to ionizing radiation than silicon dioxide. However, there are serious problems in reproducibly obtaining good silicon nitride layers, thus limiting its application at the present time.

In conclusion, it appears that the space-charge-limited triode has considerable potential as a microwave amplifier. Better silicon films should be obtained in the near future, and will result in better reproducibility and higher yields.

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