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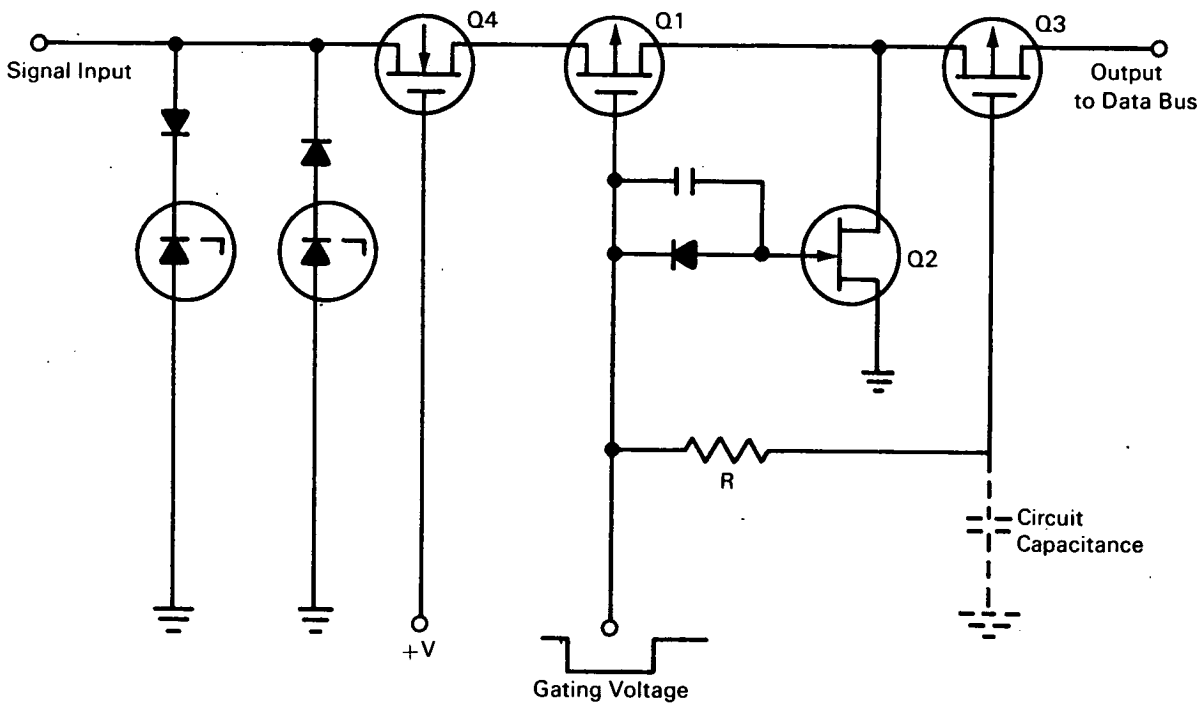
Brief 70-10022

NASA TECH BRIEF

Solid State Switch Provides High Input-to-Output Isolation



The problem:

To design a solid state switch capable of interrupting electronic signals in the 10 mV to 80 V peak-to-peak range, with input-to-output isolation of 80 db, at a rate of 50,000 samples per sec.

The solution:

A solid state switch using a combination of N- and P-channel metal oxide semiconductor field effect transistors (MOSFET) to obtain a normally open switch with no power applied. High input-output isolation is achieved through the use of series-shunt-series MOSFET switching.

How it's done:

As shown in the schematic, a P-channel MOSFET (Q1) accomplishes the primary purpose of disconnecting the input signal voltage from the output without introducing an objectional level of offset voltage. An N-channel junction MOSFET (Q2) provides a rapid turnoff capability because of its low "on" resistance. In order to prevent a short circuit, another MOSFET (Q3) is used to switch simultaneously with Q1, thus isolating the output from the shunt element. This leaves the output voltage at the cutoff level.

The switching voltage waveform is delayed for a few nanoseconds before it is applied to the gate of Q3,

(continued overleaf)

allowing the voltage charge on the load reactance to discharge through Q3 and Q2 to ground, turning off Q3, and disconnecting the load from the switch. This procedure energizes other switches connected to the same load, allowing measurements to be made of signals from other sources in rapid succession. The switch must remain off when no power is applied to the driver. This is accomplished by adding another MOSFET (Q4) to the circuit, ahead of Q1. Q4 has an opposite polarity to that of Q1 and Q2; therefore, any input voltage that would turn Q1 or Q2 on will turn Q4 off and never reach Q1.

Two zener diodes are connected to each input line to protect the switches from overvoltage due to surges, noise spikes, or accidentally applied power inputs in excess of ratings.

Note:

Requests for further information may be directed to:
Technology Utilization Officer
Headquarters
National Aeronautics and
Space Administration
Washington, D.C. 20546
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Patent status:

Inquiries about obtaining rights for the commercial use of this invention may be made to NASA, Code GP, Washington, D.C. 20546

Source: R. L. Magee and L. E. Trowbridge of
General Electric Co.
under contract to
NASA Headquarters
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