NASA TECH BRIEF

Transistor Bonding Pad Configuration for Uniform Injection and Low Inductance

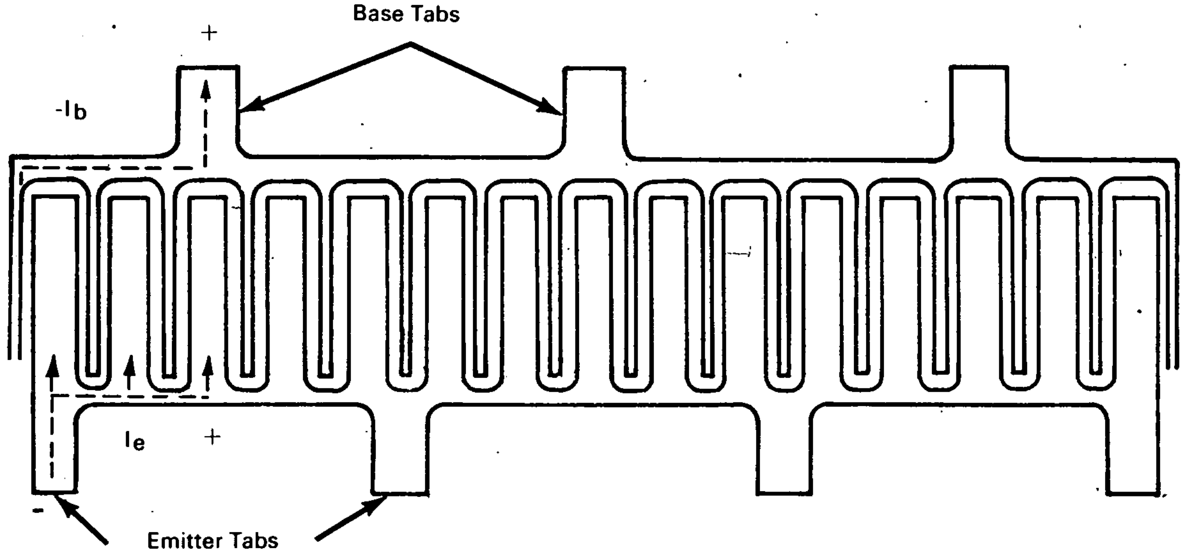

Figure 1. Pattern of Bonding Tabs for Overlay or Interdigitated Transistor

The problem:

To devise a means of improving the uniformity of carrier injection in transistors, and of reducing lead inductances at their base-emitter terminals.

The solution:

A modification of the standard process for fabricating transistors, which comprises a metallization-pattern design for emitter and base areas together with a double bonding configuration for each emitter and base-bonding lead.

How it's done:

A pattern of metallization was designed for application to either overlay- or interdigitated-type structures, in which the bonding tabs on the base side of the pattern are located approximately halfway between the bonding tabs on the emitter side of the pattern. Figure 1 illustrates this arrangment of base- and emitter-bonding tabs in an interdigitated (comb) structure. This configuration will make possible a more uniform injection from each metallized finger of the emitter because the resistive- and inductive-voltage drops in the pad connecting the emitter fingers are offset by the voltage drops in the base-connecting pad, causing a relatively constant bias across the emitter-base junction at each metallized finger. In an n-p-n transistor, the potential in the emitter-bonding pad becomes more positive as the current travels from

(continued overleaf)

the bonding lead at the tab to the third finger of the emitter. At the same time, however, the electrons in the base pad flow in the manner indicated in Figure 1, also causing the base potential to become positive in the third emitter finger. Consequently, the bias across the emitter-base junction remains relatively constant for each metallized finger of the emitter.

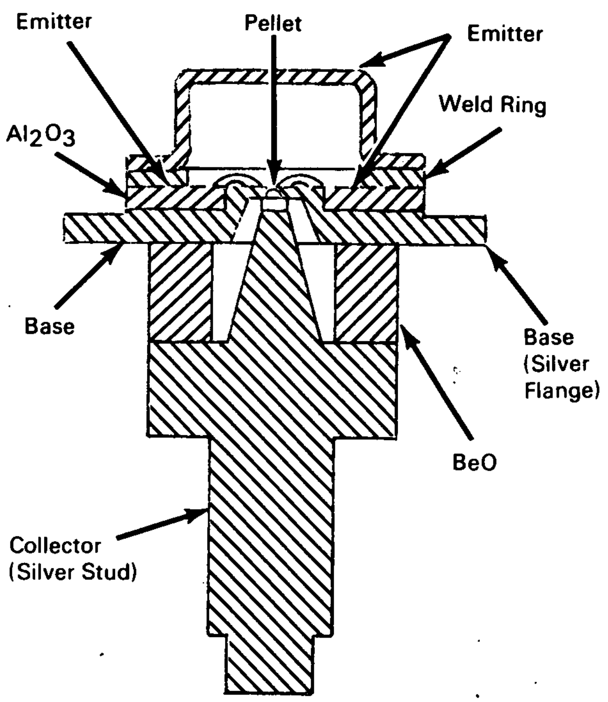

Figure 2. Cross Section of Transistor Showing Double Bonding Configuration

A second advantage of this bonding-tab configuration is its capacity to permit a double bonding of emitter- and base-bond leads. Figure 2 illustrates this concept in a coaxial package in which two terminals for the emitter and base leads are provided. This technique will give a substantial reduction in lead inductances, as compared with the single bond configuration. This reduction in the common-terminal-lead inductance will bring about improved gains in power at high frequencies and stability in the common base mode.

Notes:

1. This innovation is in the production state of development and represents a major improvement in transistor design. It is novel in that it provides an effective method to minimize parasitic losses in high-frequency transistors. The inductive, resistive, and capacitive losses are due to the effect of high-frequency operation with transistors of interdigitated metallization structure.
2. This information may be of interest to designers and manufacturers of semiconductor devices and VHF and UHF communication systems.
3. No additional documentation is available. Specific questions, however, may be directed to:
   Technology Utilization Officer
   Goddard Space Flight Center
   Greenbelt, Maryland 20771
   Reference: B70-10181

Patent status:

No patent action is contemplated by NASA.

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