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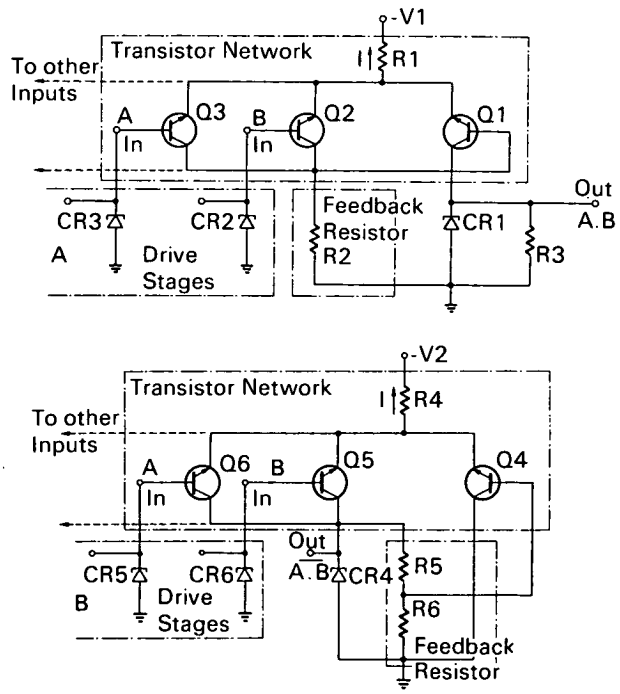
Switching Circuits with Fast Response and Low Power Drain

A new family of logic circuits have response times no longer than 10 nanoseconds and drain only milliwatts of power. The family includes AND and NAND gates with their associated monostables, bistables, delays, and oscillators. The basic circuits form the basis of all logic functions; thus they can be used in various types of digital-data-processing systems.



Circuits of AND Gate (A) and NAND Gate (B)

The input signals of an AND circuit (Fig. 1A) are derived across tunnel diodes CR2 and CR3 and applied to transistors Q2 and Q3. The output is taken across CR1 which is connected to the voltage source through Q1. Transistors Q1, Q2, and Q3 form a transistor network. In operation, when both driving tunnel diodes CR2 and CR3 are in their high-voltage state, both input transistors Q2 and Q3 are cut off. The resultant low voltage across R2, a series feedback resistor, allows Q1 to carry all current I. The collector current of Q1 now switches CR1 to its high-voltage state, creating a high voltage at the output terminal A•B. When CR2 or CR3, one or both, is in the low-voltage state, its associated input transistor (Q2 or Q3) conducts all current I from -V1. The resultant voltage across series feedback resistor R2 is applied to the base of and cuts off Q1; thus no current flows through CR1 with the result that the output voltage is essentially zero. Thus this circuit provides an AND-gate logic function. Suitable choice of components can make the power drain on the gate $\leq$ 2 mW; the response time, $\leq$ 10 nanoseconds.

In a NAND gate (Fig. 1B) the input signals are taken across tunnel diodes CR5 and CR6 and applied to input transistors Q5 and Q6. The output is taken across CR4. A state of high-voltage output exists across CR4 whenever both driving tunnel diodes CR5 and CR6 are not in the high-voltage state; more specifically, when one or both are in a low-voltage state, the associated input transistor conducts current I. This conduction causes CR4 to be in its high-voltage state and generate an output signal. The voltage under this condition at the junction of R5 and R6, which form a series feedback resistor, is applied to the base of and cuts off Q4. However, when all the driving tunnel diodes are in the high-voltage state, none of the input transistors conducts and CR4 is in its low-voltage state; zero voltage at the junction of R5 and R6 allows Q4 to conduct all current I. Thus the circuit acts as a NAND gate.

(continued overleaf)

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A circuit is provided having low output impedance and high input impedance whereby it can be used in a logic chain without need of coupling elements with their inherent disadvantages. Moreover the system operates from a single-level voltage source and has a substantially constant current drain, so that noise spikes and need for a multilevel-voltage source are eliminated.

Note:

Requests for further information may be directed to:

Technology Utilization Officer
Goddard Space Flight Center
Code 207.1
Greenbelt, Maryland 20771
Reference: TSP70-10250

Patent status:

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Source: C. A. Cancro
Goddard Space Flight Center
(GSC-10878)