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Two Techniques for Digital Filter Design

There are several ways to achieve digital compensation. First, sample-and-hold circuitry may be used to generate a compensation transfer function within the system; second, general or special-purpose computers may simulate the transfer function and interface with the system; and third, various analog and digital circuits, converters, summing amplifiers, constant multipliers, and delay lines may be interconnected to form a digital filter.

Reports have been made on two generalized third-order digital controllers designed around the last two techniques, one using a special-purpose computer, and the other using a combination of digital and analog techniques.

Two mathematical formulations of the transfer function of a digital controller exist, called the direct form and the canonical form. In both designs, the canonical form is used. This form calls for the solution of the two equations

$$m(k) = e_i(k) - b_1 m(k-1) - b_2 m(k-2) - b_3 m(k-3)$$

and

$$e_o(k) = a_o e_i(k) + c_1 m(k-1) + c_2 m(k-2) + c_3 m(k-3)$$

where

$$c_j = a_j - a_o b_j \; (j = 1, 2, 3), \; a_o, \; a_j \text{ and } b_j$$

are constants, $e_i(k)$ is the digitized sample of the input signal, $e_o(k)$ is the output signal in digital form, and $m(k-j)$ is the time-delayed $m(k)$ of the jth past sample.

In the first design, the special-purpose computer is described in four blocks, each of which performs specific functions in the solution of the transfer equation. The first block, input-output equipment, contains a successive approximation-type analog-to-digital (A/D) converter and a digital-to-analog (D/A) converter. The A/D converter provides the input signal $e_i(k)$ by digitizing samples of the input analog waveform $e_i(t)$. The input voltage is divided into 2^{10} - 1024 distinct magnitude levels, represented by a 10-bit binary word. The D/A converter restores $e_o(k)$ into the output analog waveform $e_o(t)$. Individual compensators may require different D/A devices to correctly interface with different overall systems.

The second block, memory, provides the time delay needed for the functions of k-1, k-2, and k-3; stores the various constants b_1, b_2, a_o, c_1, etc.; and holds the intermediate variables m(k-1), m(k-2), etc. Storage of the constants is provided by mechanical switches, so that they may be changed easily to modify the compensation function. The variables are stored in flip-flops in signed-magnitude form.

The third block, the arithmetic unit, performs the various addition and multiplication steps needed to solve the two equations. The circuit used consists of a parallel binary accumulator logically coupled to two shift registers.

The final block, the control unit, synchronizes the operation of the other three blocks. It contains a function generator to produce the master clock and other required timing signals, and also the transfer logic circuit, which governs the exchange of quantities between the memory and arithmetic units.

The second design is described as a "hybrid digital controller," because both analog and digital circuits are used. The input analog signal $e_i(t)$, together with three time-delayed intermediate signals, is fed into a loop which starts with a summing amplifier. The output of the summing amplifier is coupled through an A/D converter, and the digital signal fed through three successive buffer registers, producing three

(continued overleaf)

different time-delayed signals m(k-1), m(k-2), and m(k-3). These are reconverted to analog signals in three separate D/A circuits, fed through phase-splitting operational amplifiers to allow switch-selection of the correct arithmetical signs, and through three precision resistors to affix the correct value for b_1, b_2, and b_3. These intermediate signals are then fed back into the first summing amplifier, closing the loop. Thus the loop provides the solution to the first equation.

Outputs are taken from the A/D converter ($e_i(k)$ signal) across a phase-splitting operational amplifier, and also from each of the three delayed signals, fed through four precision resistors to attach the appropriate value of a_j, and then fed through manual sign-selecting switches into a second summing amplifier from which the analog output $e_o(t)$, the already reconverted solution of the second equation, is taken. Thus the combination of digital and analog circuits serves to solve the same equations as the special purpose digital computer.

Because of their generality, either of these two designs may be easily applied to a wide variety of digital compensation applications.

Note:

Requests for further information may be directed to:

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