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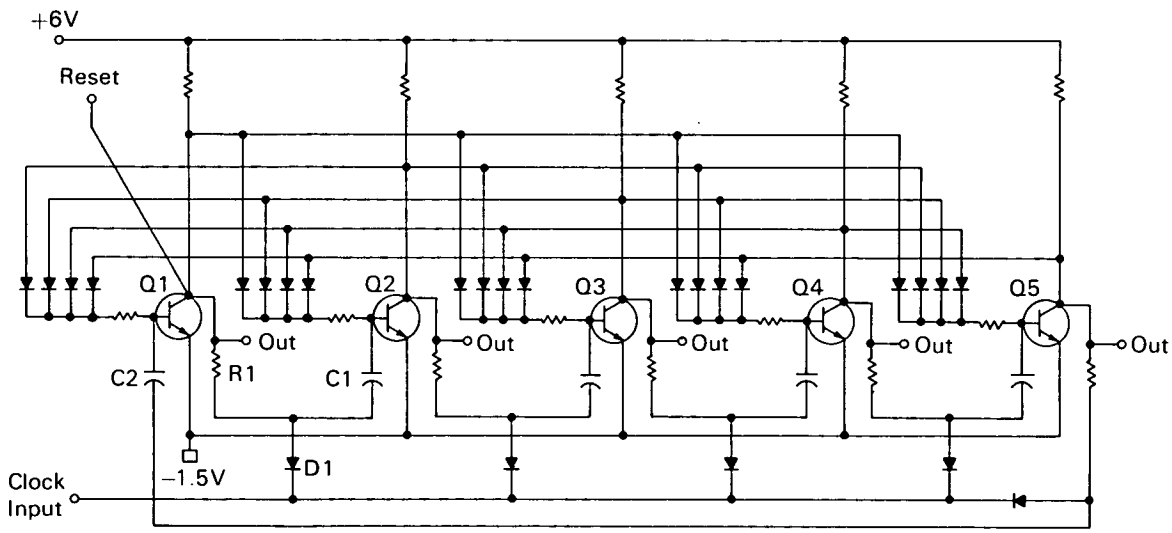
NASA TECH BRIEF

Pental Circuit May be Used in Conversionless Decimal Counter



Schematic Diagram of the Pental Counter Circuit

The pental counter circuit, a schematic diagram of which appears above, its an extension of the principles of the standard binary, two-state circuit, the flip-flop. Essentially a five-stage ring of NOR gates, the pental circuit was designed to eliminate the conversion circuitry which must be used when binary circuits are employed to generate or process numeric information, as for example, decimal timing waveshapes. A decimal counter may be simply constructed from one pental circuit, one standard flip-flop, and several AND gates.

The pental has five stable states, each with four transistors on and one transistor off. The triggering circuit provides trailing edge logic, and sequentially steps the off position from left to right in synchronism with the input clock pulses.

When the first transistor (Q1) is off (high collector voltage), its base current, through the associated diode network, maintains the other four transistors (Q2 through Q5) in the on state (low collector voltage).

The trailing edge of the clock pulse fires the trigger circuit (R1 C1 D1). Capacitor C1, which has been charged through resistor R1 to the high collector voltage of Q1, discharges through diode D1. The resultant negative spike on the base of Q2 back-biases the transistor and turns Q2 off, permitting its collector voltage to rise. The base current of Q2 then maintains Q3, Q4, and Q5 in the on state and also turns Q1 on. On the next clock pulse, the trigger circuit associated with transistor Q2 is fired, and Q3 is turned off. Succeeding pulses step the off position farther to the right. The cycle is completed by connecting capacitor C2 (in the

(continued overleaf)

trigger circuit of Q5) to the base of Q1, allowing the sequence to be fed back from Q5 to Q1.

When the pental circuit is used in a decimal counter, the trigger circuit of Q5 is also used to set the flip-flop (not shown in the illustration). The counter may be reset to zero by applying a positive pulse to the collector of Q1 and to the base of the transistor associated with the on state of the flip-flop.

Note:

No additional documentation is available. Specific questions, however, may be directed to:

Technology Utilization Officer
Headquarters
National Aeronautics
and Space Administration
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Patent status:

No patent action is contemplated by NASA.

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