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NASA TECH BRIEF

Laser Scribing of Silicon Wafers

A laser has been used as a scribing tool to improve silicon wafer dicing. Results show that laser scribing can eliminate microcracking at scribe line intersections, minimize or eliminate preparation of the scribe channels, and increase yield during the breaking process. For this experiment, silicon wafers .006-in. to .007-in. thick, with various circuitry on one side and gold plate on the back, were used. A focused yttrium aluminum garnet (YAG) laser was employed to partially penetrate a silicon wafer on the back side. The wafers were then broken in the standard manner.

The first method involving a series of distinct spots separated by intervals of unlased silicon did not prove feasible because the scribe was not defined well enough for the break to follow.

A second, successful, method utilized overlapping spots. Back side cutting with a continuous line scribe resulted in a well defined break. Since only a small fraction of a watt impinges on the wafer, no heating problems were anticipated with epitaxial circuits. Microcracking, normally found at the junctions of conventionally scribed wafers, was not prevalent with this method.

Sufficiently rapid overlapping of spots in the form of a line may permit the attainment of high scribing speeds. Laser pulse rates of 50 pulses per second resulted in scribing speeds of 1.5 to 2.5 in./sec. With 200 pulses per second, the cutting speed should approach 6 to 10 in./sec.

The sample quantity of wafers scribed did not permit defining a yield factor. However, cleanliness of the break, complete elimination of chipped scribe lines, and relatively large penetration through the wafer promised a considerable increase in yield over present scribing methods. Additionally, this technique eliminated any preparation of the scribed channel. Further experiments using pure silicon (without gold plate) yielded even better results.

Notes:

1. This YAG laser system should successfully compete with existing techniques as a high-speed production tool for scribing silicon wafers and should interest semiconductor manufacturers.
2. Requests for further information may be directed to:

   Technology Utilization Officer
   Headquarters
   National Aeronautics
   and Space Administration
   Washington, D.C. 20546
   Reference: B70-10437

Patent status:

Inquiries about obtaining rights for the commercial use of this invention may be made to NASA, Code GP, Washington, D.C. 20546.

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Category 01