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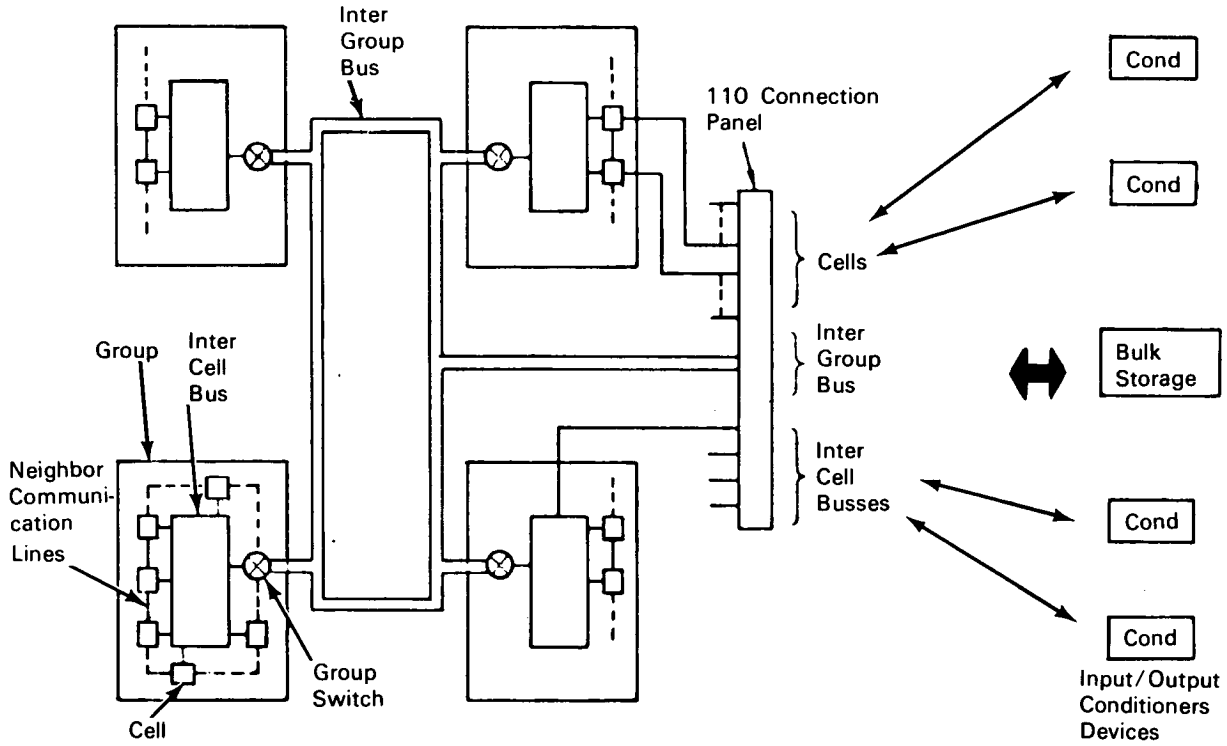
NASA TECH BRIEF

Concept for a Distributed Processor Computer

A concept has been developed for the organization of a future generation computer. At the bottom organizational level is a cell, a single metal oxide semiconductor (MOS) wafer containing a general purpose processor section and a small memory (approximately 512 words of 16 bits each). The cells are organized into groups and the groups interconnected to form the computer.

The cells within each group communicate with each other by an intercell bus and by neighbor communication lines. One cell in the group is designated as the controller; the remaining cells are either operated independently or subordinated to the controller. Thus, this highly reliable organization has the advantage of both applied parallelism (global control) and natural parallelism (local control) within computations. Since there can be many levels of degradation, it is implied that the computer system will tolerate numerous internal single-point failures before system failure occurs. Cells may be switched on and off to match varying computational requirements, and the number of cells and groups can be varied according to the desired application.



(continued overleaf)

Notes:

1. A computer based on this organizational concept would find application in such diverse fields as real-time hospital patient monitoring, process control, and weather forecasting.
2. The following documentation may be obtained from:
   National Technical Information Service
   Springfield, Virginia 22151
   Single document price $3.00
   (or microfiche $0.65)

   Reference:
   NASA -CR-1446 (N70-20606), Study of Spaceborne Multiprocessing-Phase I.

   NASA-CR-1158 (N68-31499), Study of Spaceborne Multiprocessing, Phase II.

Patent status:

No patent action is contemplated by NASA.

Source: L. J. Koczela, P. N. Bogue, and G. J. Burnett of
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