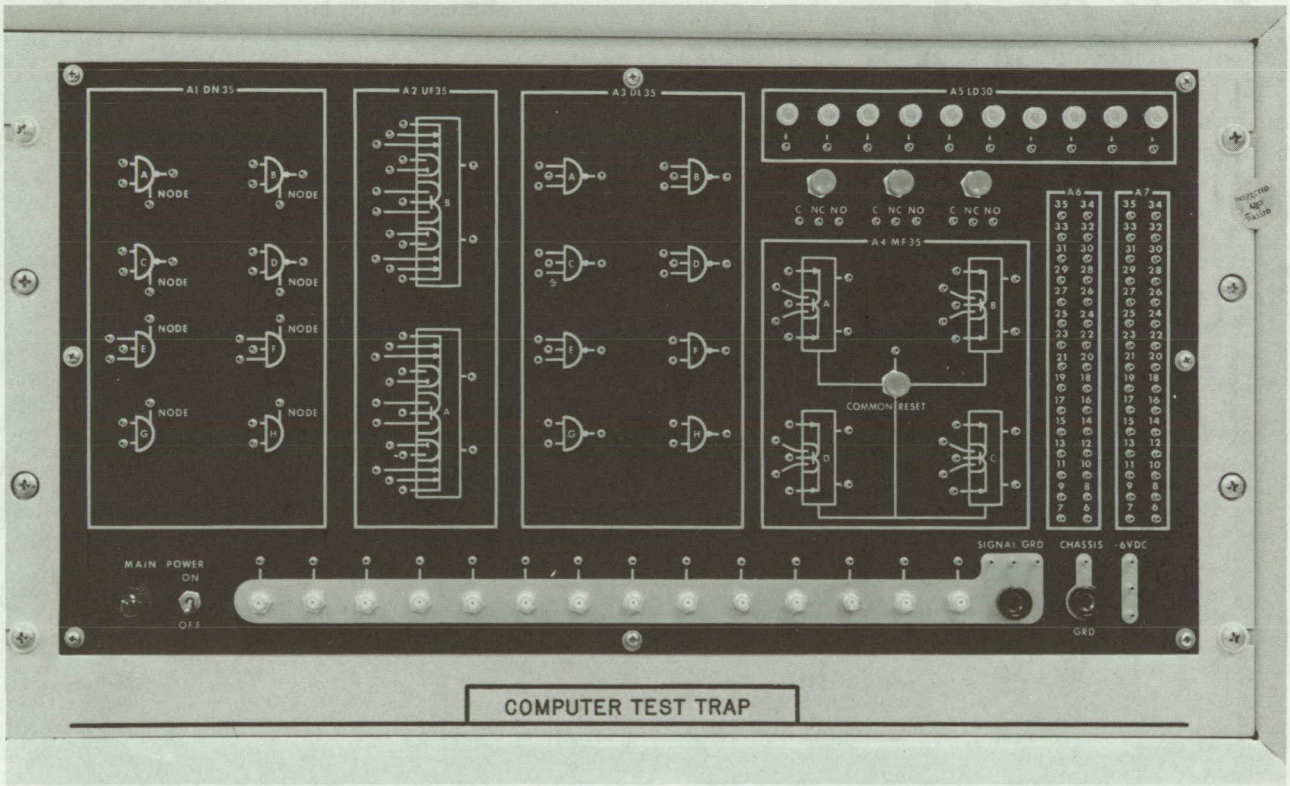
November 1970 Brief 70-10561

NASA TECH BRIEF

Ground Computer Test Trap



Isolating problems in a ground support display computer is difficult and time consuming using conventional methods and test equipment. Oscilloscopes and meters are helpful but not adequate. The most difficult problems are the intermittent computer logic failures that can vary at any time between each recurrence. Because of parallel operation within the computer, one or more suspected areas of logic could give indications of being the source of malfunction. As an aid in evaluation, the status of certain logic elements, flip-flops, gates, etc. needs to be retained.

The Computer Test Trap was designed to retain failure indications and monitor more than one logic area simultaneously. In addition, the device duplicates existing logic elements in question such as flip-flops, gates, and drivers; gives a visual display of a detected error; operates at computer speed; offers ease of connection; maintains readily available logic

(continued overleaf)

description of cards used; is compatable with existing computer circuitry; and is portable.

The test trap operates on logic levels from +15 V to -6.5 V, making it useful in many other digital equipment areas.

The capabilities listed above were achieved by using a single logic nest of five printed circuit (PC) boards and a power supply within the unit. The front panel has the logic symbol and type of each PC board etched on the surface for immediate recognition; three momentary switches to generate pulses; one momentary switch to provide a common reset to four flip-flops; ten lamps to indicate the detected errors; jacks for signal and chassis ground from computer to test trap to minimize ground loops; and the capability to connect 14 signals as source input, patched by jumpers to any or all of the test logic.

Two slots within the logic nest do not contain printed circuit boards. However, they are wired to the front panel to permit utilizing any other type of PC board in the computer that requires unique operating conditions.

When a failure is detected, the signals creating the failure will indicate the logic area requiring further investigation. Reconfiguration may be necessary several times to pinpoint the failing element.

Notes:

1. Details concerning the front panel of this item can be found in NASA Tech Brief B70-10560.
2. No additional documentation is available. Specific questions, however, may be directed to:
   Technology Utilization Officer
   Kennedy Space Center
   Code AD-PAT
   Kennedy Space Center, Florida 32899
   Reference: B70-10561

Patent status:

No patent action is contemplated by NASA.

Source: P. H. Higgins and D. G. Fondrie of
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under contract to
Kennedy Space Center
(KSC-10574)