November 1970

Brief 70-10562

NASA TECH BRIEF

Digital Input Is Buffered to Real-Time Analog Display

The problem:

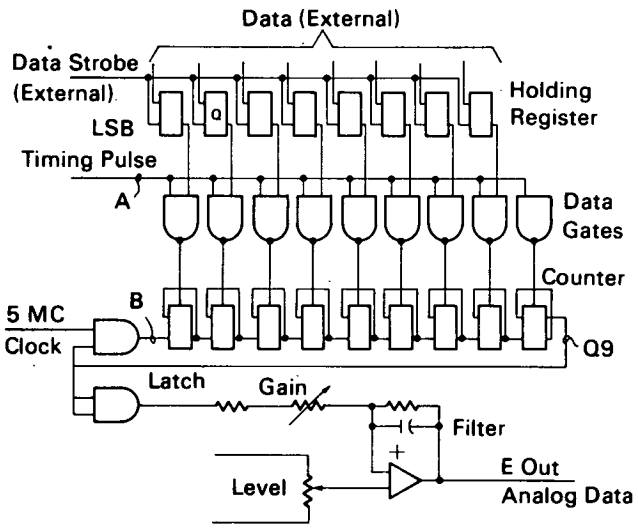
The presently-used method of digital-to-analog conversion of telemetry data involves the superimposing of weighted currents that are fed through a single resistor. Voltage drop across this resistor is used to derive the analog output. While relatively simple in concept, this approach has placed a high premium on component quality. For instance, trim pots must be incorporated in all but the least significant precision current sources and individual adjustment of these pots becomes a task. Additionally, the problem of crosstalk at the summing resistor and its solution by precision elements is a serious constraint to miniaturization.

The solution:

A buffering technique that modifies digital input to a form readily treated by well known analog techniques. The analog techniques are then used to complete the conversion to a real-time display.

How it's done:

In the present prototype, the timing system is a nine-bit, ripple-carry binary counter, that counts from zero through 256 and then resets. It therefore generates, at the Q output of the most significant flip-flop of the counter, a train of pulses at a rate of one timing pulse for each group of 257 clock cycles. As shown in the figure, the eight flip-flops forming the holding register form the memory device that allows precise asynchronous conversion of the digital source data. At some convenient point in time, the counter has a value of all zeroes with the least significant bit at the left. Assuming that data in the holding register have a value of three, the logic level at the point labeled B is



logic one, since the Q9 input to the latch gate is a logic zero. At this time, a timing pulse appears at point A and a low input to the preset terminal sets the flip-flops used in the counter to logic one; those flip-flops with high inputs at the preset terminal remain reset. The counter, therefore, is set to a value of 001111111, the one's complement of the data, with the most significant bit of the counter (Q9) being unconditionally set to logic one.

With Q9 as a logic one, the clock is gated to point B and the counter is energized. The counter counts until it overflows. At that time Q9 returns to zero, point B is latched to logic one, and the counter has returned to its initial condition (reset). The waveform at Q9, therefore, has a duty cycle directly related to the initial data. By passing this waveform through a low pass filter, the data are recovered in analog form.

(continued overleaf)

Note:

Requests for additional information may be directed to:

Technology Utilization Officer
Kennedy Space Center
Code AD-PAT
Kennedy Space Center, Florida 32899
Reference: TSP70-10562

Patent status:

This invention is owned by NASA, and a patent application has been filed. Royalty-free, nonexclusive licenses for its commercial use will be granted by NASA. Inquiries concerning license rights should be made to NASA, Code GP, Washington, D. C. 20546.

Source: K. F. Bower
Kennedy Space Center
(KSC-10397)