NOTICE

The invention disclosed in this document resulted from research in aeronautical and space activities performed under programs of the National Aeronautics and Space Administration. The invention is owned by NASA and is therefore available for licensing in accordance with the NASA Patent Licensing Regulation (14 Code of Federal Regulations 1245.200).

To encourage commercial utilization of NASA-owned inventions, it is NASA policy to grant nonexclusive, royalty-free, revocable licenses to any company or individual desiring to use the invention while the patent application is pending in the U.S. Patent Office and within a specified period, presently two years, after issuance of the patent to NASA. If commercial use of the invention does not occur during this period, NASA may grant a limited exclusive, royalty-free license thereby adding an incentive to further encourage commercial development. Any company desiring to make, use, or sell this invention is encouraged to obtain a royalty-free license from NASA.

Address inquiries and all requests for licenses to Assistant General Counsel for Patent Matters, Code GP-1, National Aeronautics and Space Administration, Washington DC 20546.

NASA Case No. ERC-10072

NASA/Electronics Research Center
Patent Application Abstract
~~NASA Case No. ERC-10072~~

A METHOD FOR

SELECTIVE GOLD DIFFUSION OF MONOLITHIC SILICON DEVICES AND/OR CIRCUITS

A method for preparing compatible switching and nonswitching amplifier devices/circuits and/or linear and digital logic circuits on the same monolithic chip of semiconductor material is disclosed. The gold is selectively diffused through the device side (front side) of the semiconductor chip. Selective diffusion of gold cannot be accomplished by the prior art method of diffusing gold through the collector side (back side) of the semiconductor chip. Gold is diffused through the entire device by this prior art method. Thus, the disclosed invention permits the fabrication of switching and nonswitching devices on the same chip of semiconductor material. The devices so produced can be used in electronic circuitry utilized in the space program.

FIGURES 1(a) through 1(e) of the drawing show the steps of carrying out the invention. FIGURE 1(a) of the drawing shows a chip of silicon 1 containing a first diffused device 2 and a second diffused device 4. The diffused devices 2 and 4 may typically be bipolar or unipolar transistors, diodes, and integrated circuits. The silicon slice 1 with the diffused devices 2 and 4 may be prepared by any known method of preparing such semiconductor devices. A layer of Si_3N_4 is deposited over the oxide on the device side of the silicon slice 1. Instead of the single layer 3 of Si_3N_4, layers of Si_3N_4 and SiO_2 or silicon oxynitride can be used. The layer 3 of Si_3N_4 is then etched away at desired places by using conventional photoresist and etching techniques. This step of selectively opening windows is shown in FIGURE 1(b) which shows the Si_3N_4 layer removed only over the area of the diffused device 2. A thin film 5 of gold is then deposited over the Si_3N_4 layer and over the area of the diffused device 2 as is shown in FIGURE 1(c). The gold is then diffused into area 2 by heating the slice in a furnace at a controlled temperature for a controlled time and the excess gold is etched off the Si_3N_4 layer 3 to give the resultant product shown in FIGURE 1(d). Gold is diffused only into area 2 because the Si_3N_4 layer 3 acts as a barrier to the gold, thereby preventing diffusion into the rest of the semiconductor. The final product shown in FIGURE 1(e) is obtained by opening a window over the diffused device 4 using conventional photoresist and etching techniques and then a pair of electrical contacts 6 are attached to the devices 2 and 4.

The novelty of the invention resides in the method of diffusing gold only in selected areas. The disclosed method is applicable not only to the silicon specifically described but can also be used with germanium, gallium aresenide and other III-V semiconductor compounds. With this invention completely new types of circuits can be designed and optimized without regard to the prior art limitations of switching and nonswitching. Thus, the need for many previously required hybrid circuits is obviated. In addition, the disclosed invention provides a lower collector series resistance than in the present buried layer devices because gold is diffused through the device side, and it does not have to go through the buried layer to get to the desired base and collector areas as is the case in the prior art method. Also, the present invention provides for better control of the amount of gold diffused. This is important since too little gold produces slow switching parameters and too much gold produces high series resistance parameters.

INVENTOR: Ronald A. Cohen

EMPLOYER: National Aeronautics and Space Administration/ERC

CONTRACT NO: N/A

~~EVALUATOR: Mr. Seymour Schwartz, NASA/ERC~~

PATENT APPLICATION NO: 845972

FILING DATE: JUL 30 1969

NASA Case No.: ERC-10072 ~~Herbert E. Farmer/Kor-S&H~~

APPLICATION FOR LETTERS PATENT

TO ALL WHOM IT MAY CONCERN:

BE IT KNOWN THAT Ronald A. Cohen

a citizen of the United States of America, an employee of the United States Government

and resident of South Acton, Massachusetts

has invented certain new and useful improvements in A METHOD FOR SELECTIVE GOLD DIFFUSION OF MONOLITHIC SILICON DEVICES AND/OR CIRCUITS

of which the following is a specification:

A METHOD FOR SELECTIVE GOLD DIFFUSION
OF MONOLITHIC SILICON DEVICES
AND/OR CIRCUITS

Abstract of the Disclosure

Origin of the Invention

The invention described herein was made by an employee of the United States Government and may be manufactured and used by or for the Government for governmental purposes without the payment of any royalties thereon or therefor.

Background of the Invention

Monolithic integrated circuits at present are necessarily designed around either switching or nonswitching (amplifier) transistors due to the incompatibility of both types on the same chip of silicon. This is due to the fact that gold diffusion cannot be controlled to produce both types of transistors on the same chip. Accordingly, present methods have not solved this problem; present methods merely circumvent the problem by either using hybrid circuits (combinations of chip elements to achieve a definite circuit design) or by design sacrifice (modification of the circuit design

to perform the desired function satisfactorily although not optimum).

The preparation of monolithic switching and nonswitching (amplifier) transistors and therefore the preparation of linear and logic circuits requires control of the lifetime lowering diffusant utilized. Lifetime here means the time injected carriers exist. Presence of certain metals, such as gold, nickel and copper reduce this time by capturing injected carriers and thus decrease the switching time in a desired manner. At the present time gold is the diffusant most commonly used in the preparation of these devices. Unfortunately, selective diffusion of gold cannot be performed with silicon dioxide passivated integrated circuits because gold penetrates SiO_2. In addition, it is difficult to mask and etch gold on SiO_2. Due to these factors, gold, at the present time, is put in a semiconductor through massive diffusion in the collector side of the semiconductor slice. Therefore, the entire slice contains diffused gold. Thus, the only choice is a slice having gold or not having gold. This is why a slice of semiconductor material in which only a selected area contains gold cannot be produced by the prior art method of diffusing gold from the back side of the semiconductor slice. Similarly, attempts to selectively diffuse gold in the device side of a semiconductor chip on which SiO_2 is used as a passivation have not been successful because the gold penetrates the silicon dioxide.

Summary of the Invention

This invention permits the selective diffusion of gold through the device side of the semiconductor chip and thereby enables one to prepare compatible switching and amplifier devices/circuits on the same monolithic chip of semiconductor material

Selective gold diffusion through the device side of the semiconductor chip is achieved in the following manner: A thin layer of Si_3N_4 is deposited over the semiconductor and/or passivated semiconductor surface. Windows are opened in the Si_3N_4 and other dielectric layers, if any, at selected areas by using conventional photomasking and etching techniques. A thin film of gold is then deposited over the Si_3N_4 layer and the gold is diffused into the semiconductor in the areas where the Si_3N_4 was removed. The excess gold is then etched off and a standard planar processing technique is used to complete the device.

It is therefore an object of this invention to provide a method for the selective diffusion of gold into a chip of semiconductor material.

It is another object of this invention to provide a method for the preparation of compatible switching and non-switching devices/circuits on the same monolithic chip of semiconductor material.

It is a further object of this invention to provide a method of selectively diffusing gold through the device side of a slice of semiconductor material.

Brief Description of the Drawing

The above mentioned and other objects of the invention will become apparent from the following detailed description of the invention when read in conjunction with the annexed drawings in which FIGURES 1(a) through 1(e) pictorially show the steps used in carrying out the invention.

Description of the Invention

Referring now to the drawing, FIGURE 1(a) shows a chip of silicon 1 containing a first diffused device 2 and a second

diffused device 4. The diffused devices 2 and 4 may typically be bipolar or unipolar transistors, diodes and integrated circuits. The silicon slice 1 with the two diffused devices 2 and 4 can be prepared by any known method of preparing such semiconductor devices (Integrated Circuits, Design Principles and Fabrication, Editors, R.M. Warner and J.N. Fordenwalt, McGraw Hill Book Co., New York, 1965). A layer of Si_3N_4 is deposited over the oxide on the device side of the silicon slice 1 and the diffused areas 2 and 4. It is to be understood that instead of the single layer 3 of Si_3N_4, layers of Si_3N_4 and SiO_2 or silicon oxynitride can be used.

The layer 3 of Si_3N_4 is then etched away at desired places by using conventional photoresist and etching techniques for Si_3N_4 (Etching of Silicon Nitride (Si_3N_4) in Phosphoric Acid Using Silicon Dioxide as a Mask, W. Vangelder and V. E. Hauser, 1966, Fall, Meeting of Electrochemical Society, Philadelphia, Pa. Recent News Paper No. 5). This step of selectively opening windows in the Si_3N_4 is shown in FIGURE 1(b). As shown in FIGURE 1(b) the Si_3N_4 is removed only over the area of the diffused device 2.

A thin film of gold 5 is then deposited over the Si_3N_4 layer and over the area of the diffused device 2 where the Si_3N_4 has been removed as shown in FIGURE 1(c). The gold is then diffused into the area 2 by heating the slice in a furnace at a controlled temperature for a controlled time (Gold Diffusion Process for Reducing Switching Times in Diffused Silicon Transistors, C.J. Uhl, Western Electric Engineer, Jan., 1963) and the excess gold is etched off the Si_3N_4 layer to give the resultant product shown in FIGURE 1(d). All the gold not diffused into silicon will be etched off. The gold that is diffused will not

be affected by the etching. The method of depositing and diffusing the gold is carried out in two separate steps: (1) evaporate gold onto entire slice area and (2) diffuse gold into slice areas desired. However, no matter how the gold is diffused into the area 2, only this area receives gold because the Si_3N_4 layer acts as a barrier to the gold, thereby preventing gold diffusion into the silicon slice 1 and into the diffused device 4. The fact that gold is diffused only into the diffused device 2 is shown in FIGURES 1(d) and 1(e).

The final product is shown in FIGURE 1(e). The product shown in FIGURE 1(e) is obtained from the product shown in FIGURE 1(d) by opening a window over the diffused device 4 using conventional photoresist techniques (Effect of Diffused Oxygen and Gold on Surface Properties of Oxidized Silicon, A.G. Nassibian, Solid State Electronics, Vol. 10, pp. 879-890, 1967) and etching away the Si_3N_4 covering the device 4. A pair of suitable contacts 6 are then attached to the devices 2 and 4 and a pair of electrical leads (not shown) are attached to the contacts 6.

From the foregoing description of the invention, it is obvious that a method of selectively diffusing gold has been disclosed. As is shown in FIGURES 1(d) and 1(e), gold was diffused only into the device 2. No gold was diffused into the device 4. Therefore, switching and nonswitching devices can be prepared on the same monolithic chip of semiconductor material.

The drawing only shows one area with gold and one area without gold; however, it is obvious that any number of areas with gold and without gold can be produced on the same chip of semiconductor material by using the method of this invention. In addition it should also be obvious that this invention is

applicable not only to the silicon specifically disclosed but can also be used with germanium, gallium arsenide and other III-V semiconductor compounds. In addition it should be apparent that the method disclosed applies to the preparation of both integrated circuits and to the preparation of individual devices such as diodes, transistors and the like.

While the invention has been described with reference to a specific embodiment, it will be obvious to those skilled in the art that completely new types of circuits can be designed and optimized without regard to prior art limitations (switch or nonswitch). Thus, the need for many previously required hybrid circuits is now obviated. Also, the present invention provides a lower collector series resistance than in the present buried layer devices. Since gold is diffused through the device side, it does not have to go through the buried layer to get to desired base and collector areasof device as in prior art. This prior art method will cause collector series resistance to increase since gold will compensate the buried layer to some extent. In addition, much better control of gold diffusion will result because short diffusion with small amount of gold from device side will give same amount of gold in desired regions (Base and Epitaxial Collector) as prior art method of massive amounts of gold diffused in from collector side. Gold will reside only in portions of device desired. Note there will be no massive gold in the collector side of device. Maximum control is desirable since too little gold produces slow switching parameters, for example, storage time and fall time, and too much gold produces high series resistance parameters, for example saturation voltage, collector assistance.

N70-11148

Fig. 1a.

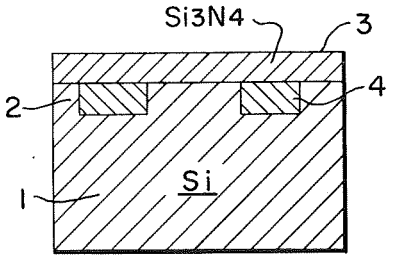


Fig. 1b.

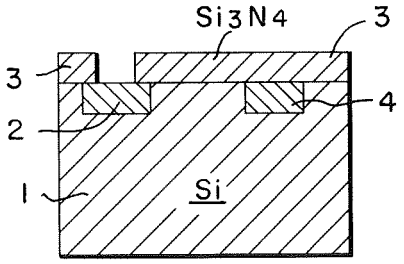


Fig. 1c.

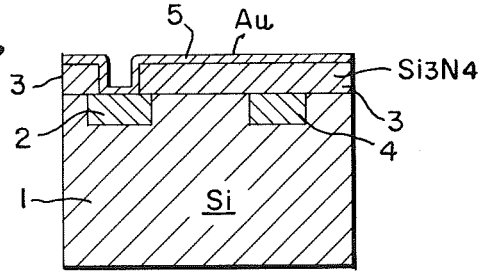


Fig. 1d.

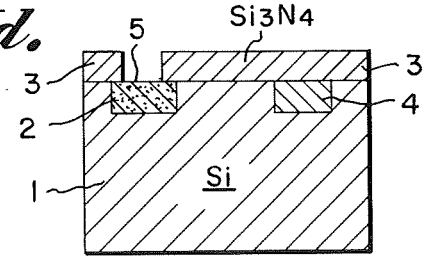
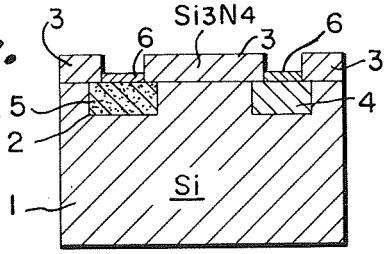


Fig. 1e.



N70-11148

N70-11148 '40%

INVENTOR
RONALD A. COHEN

BY Herbert E. Hamer
ATTORNEYS

NASA - CASE NO. ERC-10072
SHEET 1 OF 1

A22