NASA CR-66848

DEVELOPMENT OF QUALIFICATION TEST PROGRAM FOR MICROELECTRONIC DEVICES

By Walter D. Binelli &
Richard H. Soltau

SEPTEMBER 1969

Prepared Under Contract No. NAS1-8714

by

PHILCO-FORD CORPORATION
Microelectronics Division
Blue Bell, Pennsylvania

for

Langley Research Center

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

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National Aeronautics and Space Administration
Langley Research Center
Langley Station
Hampton, Virginia 23365

Final Report

This report describes studies performed in accordance with Contract No. NAS1-8714, dated 29 October 1968. The report covers work performed between 1 November 1968 and 3 July 1969.

Submitted by:

Walter D. Binelli
Program Supervisor

Approved by:

Richard H. Soltau
Program Manager
Philco-Ford Corporation
Microelectronics Division

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SECTION I

SUMMARY and CONCLUSIONS

1.1 SUMMARY

The National Aeronautics and Space Administration - Langley Research Center (NASA-LRC), in attempting to develop a more meaningful qualification program for digital monolithic integrated circuits contracted with Philco-Ford to:

1. Select test vehicles representative of their entire digital production.

2. Step-stress test these vehicles to failure or to equipment limitations in key environments.

3. Measure specified electrical parameters initially and after each stress step.

4. Perform hermeticity tests on all vehicles initially and for selected environmental tests, after each stress step.

5. Analyze all catastrophic failures.

1.2 DOCUMENTATION OF THE PROGRAM

The product of the program is the following documentation which has been presented to the Langley Research Center in this report or otherwise as noted:

1. Design appraisals of the test vehicles.

2. Summary of the catastrophic failures.

3. Summary and discussion of the failure analysis and failure modes for the catastrophic failures.

4. Summary of the catastrophic and degradation failures at each stress test.

5. Summary of the number of hermeticity failures.

6. Submission of the collated electrical test data and hermeticity test data.

    a. Submitted in three separate volumes entitled - Program Test Data for Contract NASI-8714, Development of Qualification Test Program for Microelectronic Devices.

7. Submission of the data punch cards.

   a. Submitted under separate cover.

8. Failure analysis reports.

   a. Submitted with the interim reports.

9. Test vehicles which may be further tested and the catastrophic failures.

   a. Submitted packaged by type.

1.3 DATA ANALYSIS

NASA-LRC will analyze the data in detail and develop distribution curves for all electrical parameters. Upon completion of this analysis, NASA-LRC will publish a report with final conclusions concerning the value of this type of a qualification program.

1.4 CONCLUSIONS and RECOMMENDATIONS

The bulk of the failures occurred at stress levels well in excess of those in general usage for evaluating the product. Product improvements at Philco-Ford have been the result of repeated internal testing at levels well in excess of maximum ratings. The fact that failures did not occur under certain environments, or that more failures did not occur at intermediate levels does not necessarily imply that the stress test is not useful. The quality of the test vehicle, as developed through corrective actions resulting from severe stress testing, must be considered when assessing the value of the particular environments used in the program. Testing of competitive types under the same conditions may be necessary for a complete assessment.

SECTION II

TEST VEHICLE SELECTION & IDENTIFICATION

2.1 Test Vehicle Selection

Eight hundred and forty devices were selected from existing logical groupings of monolithic microcircuits as the test vehicles. These groupings, as families, have in common the following:

Design Rules

Manufacturing Processes

Mode of Operation

Level of power dissipation or applied voltage

The family groupings include the following:

1. Diode-Transistor Logic (DTL)
2. Resistor Transistor Logic (RTL)
   a. Milliwatt RTL (mWRTL)
   b. Milliwatt III (mW_3)
   c. Super RTL (SRTL)
3. Transistor - Transistor Logic (TTL)

The three families are the 'groups' which Philco-Ford used for the evaluation of the qualification test program. The devices selected to represent a given family were chosen to reflect a wide range of factors pertinent to reliability. For example, devices were selected which operate with the highest current densities in the metal patterns, resistors, diodes or transistors or which represent any unusual design feature.

In keeping with the idea of developing an effective but economical qualification program, Philco-Ford used representative packages for each group.

Since defects due to packaging are easily analyzed as such, it did not appear necessary to run parallel tests on a group which differed only in package configuration. Each group was assigned a specific package. For this study, this was the package in which the device is most generally manufactured at Philco-Ford.

The devices selected are listed in Table 2.1. All devices conform to the following fabrication categories:

Fabrication:

Double Diffused
Single Epitaxial
Diffused Buried Layer

Description:

Low voltage, high speed,
saturated switching,
gold doped circuits

Transistors:

Bi-Polar

Metallic System:

	*CERPAC & **CERDIP	TO-5
Die Metallization:	Aluminum	Aluminum
Wire Leads:	Aluminum	Aluminum
Package Bonding Pad:	Aluminized	Gold Plated Post

Table 2.1 - DEVICE SELECTION and GROUPING

Family	Device	Function	Package	Glass Passivated	Total Sample
DTL	PL9932	Buffer	TO-86		
	PL9945	RS/JK Flip Flop	*Cerpac		
	PL9962	Triple 3-Input Gate		Yes	315
mW RTL	PL9909	Gate			
	PL9910	Dual 2-Input Gate	TO-5	No	315
	PL9913	Register			
TTL	PD9624	J/K Flip Flop	TO-116		
	PD9625	Single 8-Input Gate	**Cerdip	No	210

*Cerpac: Ceramic Flat Package
**Cerdip: Ceramic Dual-In-Line

2.2 Procurement of the Test Vehicles

One hundred and five devices, each of eight types from the three general product lines or families were procured within the Philco-Ford Microelectronics Division. The devices were standard production through the sealing operation, but the normal preconditioning procedure was eliminated to provide "raw" devices for evaluation. The purpose of using "raw" devices was to obtain a representative sample of the product line so that the data generated would result in unbiased failure distributions. However, the normal 25°C electrical characteristics tests and hermiticity tests were performed to insure initially good devices and remove any effects due to leakers, respectively.

2.3 Test Vehicle Traceability

The test vehicles were branded with the normal Philco-Ford identification and the seal code as given in Table 2.2.

Table 2.2 - DEVICE TYPE IDENTIFICATION

Type	Electrical Specification	Seal Code
PL9909	u7219	51-8-50
PL9910	u7220	42-8-47
PL9913	u7032	37-8-47
PL9932	u7330	06-8-50
PL9945	u7332	20-8-51
PL9962	u7374	07-8-51
PD9624	u7938	04-8-47
PD9625	u7942	02-8-49

A selected number of test vehicles from eight types was subjected to each of the particular step-stress tests. Electrical characteristics tests were performed initially and after each stress level for each of the seven stress tests. Hermeticity tests were also performed at the same intervals for two of the seven stress tests.

Each device was serialized and the same block of numbers used for a particular stress test as given in Table 2.3. This serves to easily identify the particular device with a given stress test.

TABLE 2.3 - SERIAL NUMBERS and STRESS TESTS

Stress Test	Serial Numbers
Storage Life	1 - 20
Operating Life	21 - 40
Reverse Bias	41 - 60
Constant Acceleration	61 - 75
Pneupactor Shock	76 - 90
Thermal Shock	91 - 102
Lead Fatigue	103 - 105

SECTION III

DISCUSSION OF THE FAILURE MODES

3.0 SUMMARY OF FAILURE MODES

All failures are tabulated in Section IV.

3.1 Elevated Temperature Storage Life

3.1.1 General Discussion:

The 24 hour per step stress temperature storage produced the greatest number of catastrophic and degradation failures. See Table 4.1 and 4.4 in Section IV. Table 4.4 indicates that a degradation type failure is a useful indication of the level of reliability because it occurs at an early point in the stress testing. The catastrophic type can also occur early especially when it is of an intermittent nature such as could be the case for a pinhole in the oxide.

As expected, the majority of failures occurred at the higher temperature levels (above 375°C) where device destruction became evident.

3.1.2 Failure Modes:

The failure modes are summarized in Table 4.8, Section IV.

The failure modes that occurred at the intermediate temperatures included bond separations at $\geq$300°C at the Au-Al interface. Device external lead oxidation also occurred as low as 275°C and also at the 300°C and 400°C steps on tinned Kovar lead devices. All types of leads are normally cleaned prior to electrical test to remove any oxides that may have formed. Several devices with tinned leads were removed as electrical catastrophic failures. It was later determined (during failure analysis) that although cleaned, these devices had more than normal oxidation (due to the high temperatures). Following subsequent testing, devices were chemically, as well as mechanically, cleaned to insure low contact resistance at leads.

At high temperatures Au-Al compound formation appears more readily at the TO-5 device post bonds as well as some evidence of diode degradation within the die

structure. At the high end of the temperature range device destruction occurs in the form of seal frit softening (Cerpac and Cerdip), and header bond separation (TO-5). The header bond separation (TO-5) occurs simply due to the exceeding of the Au-Si eutectic temperature followed by lifting of the chip. (All the TO-5's were stored for stress in trays vertically, leads down). Both PL9909 and PL9913 had approximately 50% of devices fail for header bond separation.

The softening of the seal frit and subsequent uncontrolled rehardening does apply mechanical stresses to the lead wires which can cause bond separation or wire breakage. Whether or not the separation or breakage occurs is a function of the extent to which the lead wires are encased by the glass sealing frit.

3.2 Operating Life at Elevated Temperature

3.2.1 General Discussion:

The 125°C step-stress operating life test was conducted at increasing levels of dissipation from 200 to 1000 milliwatts in 100 milliwatt steps. The first catastrophic failure occurred at the 700 milliwatt stress step - see Table 4.5. As in the case of storage life, the degradation type failure is a sensitive indication of reliability. The table also indicates that there were no failures of either type for the mWRTL family. This is due to larger base widths, deeper diffusions and higher voltage isolation diodes than is characteristic of the other families. High power stress testing for longer times would be necessary to generate failures for this family.

3.2.2 Failure Modes:

At 700 milliwatts the failure mode for the two PD9625 devices was shorted junctions due to metal migrating along single crystal planes at the Si - SiO_2 interface. Misaligned contact cuts which placed Al-Si contacts closer to diffused junctions than the design allowance, may have helped cause the failure when electrical stress was applied.

At 900 milliwatts, open metallization occurred in the PD9625's. Grain boundary formation and electro-migration of aluminum due to device temperature at this dissipation were factors contributing to the failures.

3.3 Reverse Bias at Elevated Temperature

3.3.1 General Discussion:

The step temperature stress reverse bias (at rated voltage) test did not generate any catastrophic failures. However, three PL9962's did degrade outside the initial limits for IRB2 at the 150°C or final step. (See Table 4.7, Section IV).

3.4 Constant Acceleration, Y_1 Plane

3.4.1 General Discussion:

The step stress constant acceleration test in the Y_1 plane did not generate any catastrophic failures. One PL9932 did degrade outside the initial limit for IRD. (See Table 4.6, Section IV).

3.5 Pneupactor Shock, Y_1 Plane

3.5.1 General Discussion:

The step-stress pneupactor shock test in the Y_1 plane did not generate any catastrophic electrical failures. It did generate package failures at the higher G levels indicating that the packages require extensive protection to avoid deformation or bending stresses or multiple, uncontrolled shocks due to reactions at high G levels of short duration. (See Table 4.6, Section IV).

3.6 Thermal Shock, -65°C to +200°C

3.6.1 General Discussion:

The step-stress thermal shock test consisting of 20 cycle steps from -65°C to +200°C did not generate any catastrophic electrical failures. One device, a PD9624 degraded for I_F. Also a PL9945 drifted outside the initial limit for V_{OH} for the third reading (See Table 4.7, Section IV).

Leak testing, both Helium fine and Fluorocarbon indicated a varying number of observed leak rates for several devices at each thermal stress step. (See Table 4.2, Section IV).

All the observed fine leakers from the thermal shock stress test had readings near 1 x 10^{-8} ATM cm^3/sec and are undoubtedly not bonafide leakers. The Helium detected was probably entrapped by the silicon oil used in this test, which had become occluded in pores, crevices, and other irregularities. This same occluded oil can also serve to entrap Fluorocarbon that that may appear during the detection procedure. Normally suitable cleaning techniques are not adequate after many repeated immersions in the oil.

No device was removed from any test for several reasons. First, there was no program criteria for removal of detected leakers. Secondly, only one device exceeded 3.6 x 10^{-8} ATM cm^3/sec for Helium fine leak, although a few of these devices emanated bubbles during the Fluorocarbon gross test. Finally, it was decided that more information could be obtained by subjecting these devices to further stress testing because none had failed the program's electrical criteria.

A selected number of these devices including all the apparent gross leakers were subjected to the penetrant dye test as a verification measure. None of the devices subjected to this test revealed any evidence of the dye internally for either type of failure. This confirmed that both the Fluorocarbon and Helium detected were entrapped or occluded in the device surface.

3.7 Lead Fatigue

3.7.1 General Discussion:

The step stress lead fatigue consisted of lead bending each device lead to failure. The data, Table 4.3, Section IV, indicates a marked difference for the TO-5 family in the number of bends to failure. This is probably due to lot variation in the TO-5 header.

The leak test portion of the procedure proved to be inconclusive since the number of failures varied at each stage, as in the case of thermal shock, paragraph 3.6.1.

3.8 Overall Discussion:

The data does show clearly how far one can go in a stress-to-failure program with increasing levels of stress and still generate meaningful failures. Even though meaningful failures were not generated in some of the test groups, the stress levels achieved are still ones which could have been meaningful had serious reliability hazards existed in the test vehicles and does not imply that a particular stress test is not useful. The quality of the test vehicle, as developed through corrective actions resulting from similar severe stress testing, must be considered when assessing the value of the particular environments used in the program. Testing of competitive types under the same conditions may be of value for further assessment of the procedure.

From the data generated in the program it will be possible for NASA-LRC to:

a. Draw conclusions about the reliability of the devices tested.

b. Design a practical stress-to-failure test program for short time product evaluation that would serve to monitor shifts in device quality as well as to actually assess device quality, especially if supplemented by a less frequent but larger scale testing at closer to maximum rated stress levels.

c. Compare the Philco-Ford designs with equivalent designs of other vendors to help determine the value of this type of test program as a qualification concept.

SECTION IV

SUMMARY OF FAILURES GENERATED

4.0 The following tables summarize the test results as follows:

4.1 Table 4.1 lists the serial numbers of the catastrophic electrical failures, by stress test and device type. It also gives the failure mode and the serial number of the failure analyses that were submitted with the interim reports.

4.2 Table 4.2 lists the leak test failures by type that were detected at the thermal shock stress step intervals for both helium and gross leak tests.

4.3 Table 4.3 lists the number of lead failures at the lead fatigue stress test intervals as well as the number of leakers that were detected.

4.4 Table 4.4 summarizes the number of electrical and degradation failures that occurred at each level of the storage life stress test for each device type.

4.5 Table 4.5 serves the same purpose as table 4.4 for the operating life stress test.

4.6 Table 4.6 serves the same purpose as table 4.4 for the constant acceleration and pneupactor stress tests.

4.7 Table 4.7 summarizes the number of electrical degradation failures for each device type that occurred at each level of the thermal shock and reverse bias tests. There were no catastrophic failures.

4.8 Table 4.8 summarizes the failure modes as determined through analysis of the catastrophic electrical failures.

Table 4.1 - CATASTROPHIC FAILURES, ELECTRICAL TEST

STRESS TEST	TEST CONDITIONS	TOTAL NO. TESTED	NO. FAILED	TYPE	SERIAL NO.	FAILURE MODE	FAR NO.
Storage Life 24 hours per step	75°C	160	0				
	125°C	160	1	u7330 PL9932	11	Pinhole in Oxide	9-0031
	175°C	159	0				
	225°C	159	0				
	250°C	159	0				
	275°C	159	1	u7938 PD9624	5	Oxidized Device Leads	9-0061
	300°C	158	1	u7032 PL9913	12	Post Bond Separation	9-0060
			2	u7938 PD9624	2,8	Oxidized device leads	9-0061
	375°C	155	2	u7032 PL9913	5,10	Au-Al formation at post	9-0064
	400°C	153	1	u7942 PD9625	14	Oxidized device leads	9-0061
			1	u7938 PD9624	16	Oxidized device leads	9-0061
			1	u7032 PL9913	7	Au-Al formation at post	9-0083
	425°C	150	2	u7032 PL9913	2,18	Diode degradation	9-0073
	450°C	148	1	u7220 PL9910	8	Post bond separation	9-0065
			1	u7032 PL9913	4	Post and chip to header bond separation	9-0084
			1	u7938 PD9624	11	Diode degradation	9-0085
	475°C	145	12	u7942 PD9625	2,3,4,7,8,9,10, 11,13,15,16,17, 19	Seal Frit softened (A)	9-0098
			9	u7219 PL9909	2,3,4,5,79,12, 17,18	Post and chip to header bond separation	9-0089
			4	u7938 PD9624	4,9,18,20	Seal Frit softened (A)	9-0088
			9	u7032 PL9913	1,3,8,9,14,15, 16,19,20	Post and chip to header bond separation	9-0089
			13	u7332 PL9945	2,4,5,6,8,9,10 11,12,13,14,19, 20	Seal Frit softened (A)	9-0090
			5	u7330 PL9932	4,5,7,19,20	Post Bond separation	9-0087

Table 4.1 - CATASTROPHIC FAILURES, ELECTRICAL TEST (Cont'd)

STRESS TEST	TEST CONDITIONS	TOTAL NO. TESTED	NO. FAILED	TYPE	SERIAL NUMBER	FAILURE MODE	FAR NO.
Operating Life at 125°C 24 hrs/step	200 mW	160	0				
	300 mW	160	0				
	400 mW	160	0				
	500 mW	160	6	u7374 PL9962	22,27,28,29 31,36	Excessive Dissipation not device failures	9-0079
	600 mW	154	0				
	700 mW	154	5	u7942 PD9625	24,37	Shorted Junctions	9-0095
					23,31	Excessive dissipation not device failures (B)	
					36	Mechanical damage not a device failure	
	800 mW	139	0				
	900 mW	139	2	u7942 PD9625	28,39	Open Metalization	9-0062
			1	u7332 PL9945	33	Electromigration of metalization	9-0099
	1000 mW	136	9	u7332 PL9945	24,26,27,28, 32,36,37,38 40	Electromigration of metalization	9-0100
			4	u7330 PL9932	21,22	Excessive dissipation not a device failure	9-0086
					29,39	Electromigration of metalization	
			1	u7942 PD9625	32	Electromigration of metalization	9-0091
Reverse Bias at max.rated voltage 200 hrs/step	75°C	160	0				
	100°C	160	0				
	125°C	160	0				
	150°C	160	0				
Constant Accelera-tion YI Plane	20KG	120	0				
	40KG	120	0				
	60KG	120	0				
	80KG	120	0				
	100KG	120	0				

Table 4.1 - CATASTROPHIC FAILURES, ELECTRICAL TEST (Cont'd)

STRESS TEST	Test Conditions	No. Tested	NO. FAILED	TYPE	SERIAL NO.	FAILURE MODE	FAR NO.
Pneupactor Shock YI Plane	20KG	120	0				
	40KG	120	0				
	60KG	120	1	u7032 PL9913	82	Fixture Problem: Flexture of TO-5 package resulting in damage to chip (C)	9-0039
	80KG	119	5	u7032 PL9913	76,78,79 80,83		9-0039
			6	u7220 P19910	76,77,79, 84,87,88	Fixture Problem (C)	9-0039
			4	u7219 PL9909	76,85,87,89	Fixture Problem (C)	9-0070
			1	u7942 PD9625	87	Package damage	9-0093
	100KG	40 (D)	1	u7220 PL9910	78	Fixture Problem (C)	9-0082
			1	u7374 PL9962	85	Package damage	9-0093
			3	u7332 PL9945	78,84,88	Package damage	9-0093
			1	u7330 PL9932	83	Package damage	9-0093
Thermal Shock Cumulative Cycles -65°C 5 min. transfer 3 sec. +200°C 5 min.	20 ∿	96	0				
	40 ∿	96	0				
	60 ∿	96	0				
	80 ∿	96	0				
	100 ∿	96	0				
	120 ∿	96	0				
	140 ∿	96	0				
	160 ∿	96	0				
	200 ∿	96	0				

(A) Rehardening of sealing frit caused post bond separations.
(B) Current "runaway" during setup
(C) Failure Mode - Pneupactor Shock: Package damage - fixture design inadequate for high number of blows and consecutive testing at high "G" levels. Not a device failure.

(D) Testing on TO-5 and Cerdip Packaged devices was terminated at the 80 KG level due to missile breakage. Some of these devices had been subjected to the 80 KG level before missile breakage occurred.

TABLE 4.2 - THERMAL SHOCK (a) - LEAK TEST FAILURES (b)

TYPE	Leak Test	No. of Devices	Number of Completed Thermal Shock Cycles 20∿	40∿	60∿	80∿	100∿	120∿	140∿	160∿	180∿	200∿
CERPAC												
PL9932	He	12	0	0	0	0	0	0	0	0	0	0
	Freon		0	0	0	0	0	0	0	0	0	0
PL9945	He	12	0	0	0	0	0	0	0	0	0	0
	Freon		0	0	0	0	0	1	0	0	0	0
PL9962	He	12	0	0	0	0	0	0	0	0	0	0
	Freon		0	0	0	0	0	0	0	0	0	2
TO-5												
PL9909	He	12	0	0	0	6	12	12	12	12	0	6
	Freon		0	0	0	0	0	0	0	0	0	0
PL9910	He	12	0	0	4	10	11	7	9	4	4	4
	Freon		0	0	0	0	0	0	0	0	0	0
PL9913	He	12	0	0	5	5	1	5	7	11	3	4
	Freon		0	0	0	0	0	5	0	2	4	1
CERDIP												
PD9624	He	12	6	4	2	8	10	7	6	3	0	10
	Freon		0	0	0	0	0	0	0	0	0	0
PD9625	He	12	9	8	5	12	12	12	12	12	0	2
	Freon		0	0	0	0	0	0	0	0	0	1

(a) Cumulative cycles, -65°C 5 min., 25°C 3 sec., +200°C 5 min.

(b) Helium Fine: All devices indicated as 'failed'had measured leak rate $>1 \lesssim 2 \times 10^{-8}$ ATM cm^3/sec except PD9625's leak rate $>1 \lesssim 3.6 \times 10^{-8}$ ATM cm^3/sec. These are probably due to entrapment of Helium by occluded silicon oil used for cycling.

Fluorocarbon Gross: One or more bubbles fails device. A subsequent penetrant dye check showed that none of these devices were actual gross leakers into the inner cavity.

Table 4.3 - LEAD FATIGUE - FAILURES, MECHANICAL OR LEAK TEST (c)

TYPE	No. of Devices	Total No. of Leads	Cumulative number leads failed at or before cycle no. 5∿ 10∿ 15∿ 20∿ 40∿ 60∿ (b)	No. of Devices	Cumulative no. of devices Failing Leak Test at Cycle No. (c) 5∿ 10∿ 15∿ 20∿ 40∿ 60∿ (b)
CERPAC					
PL9932	3	42	0 25 30(a) - - -	3	0 0 0 - - -
PL9945	3	42	0 23 36 - - -	3	0 0 0 - - -
PL9962	3	42	0 23 30(a) - - -	3	0 0 0 - - -
TO-5					
PL9909	3	24	0 0 2 5 21 24	3	0 3 3 1 2 3
PL9910	3	24	0 0 1 2 16 24	3	0 3 3 2 3 3
PL9913	3	24	0 0 0 0 6 24	3	0 2 3 3 0 3
CERDIP			9∿ 18∿ 27∿ (b)		9∿ 18∿ 27∿ (b)
PD9624	3	42	0 0 42	3	2 0 3
PD9625	3	42	0 0 42	3	0 0 2

(a) All leads off except corner leads

(b) Number of arcs shown, or to destruction One cycle (∿) or arc consists of a 90° bend and return.

(c) Fluorocarbon and helium fine leak tests - Devices indicated as "failed" had measured leak rates between 1 and 2 x 10^{-8} ATM cm^3/sec. except #103, PL9910 read 4.4, 32, 18 and 24 ATM cm^3/sec. at the 10th, 20th, 40th and 60th cycle respectively and it also failed freon bubble at the 60th cycle. A subsequent penetrant dye check showed that none of these devices were actual leakers into the inner cavity.

Table 4.4 - SUMMARY OF CATASTROPHIC (C) AND DEGRADATION (D) FAILURES

STEP STRESS STORAGE LIFE - 24 HOURS PER STEP

TEMPERATURE °C			75	125	175	225	250	275	300	325	350	375	400	425	450	475	TOTAL (a)
TYPE	Initial No.	Type Fail.															
DTL CERPAC																	
PL9932	20	C	0	1	0	0	0	0	0	0	0	0	0	0	0	5	6
		D	0	0	0	0	0	0	0	0	1	4	7	9	18	13	13
PL9945	20	C	0	0	0	0	0	0	0	0	0	0	0	0	0	13	13
		D	0	0	0	0	0	0	0	0	1	0	0	1	12	6	6
PL9962	20	C	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		D	0	0	0	0	0	0	0	0	1	1	2	7	16	19	19
mW RTL TO-5																	
PL9909	20	C	0	0	0	0	0	0	0	0	0	0	0	0	0	9	9
		D	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PL9910	20	C	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1
		D	0	0	0	0	0	0	0	0	0	0	0	0	1	5	5
PL9913	20	C	0	0	0	0	0	0	1	0	0	2	1	2	1	9	16
		D	0	0	0	0	0	0	0	0	0	0	2	12	9	2	2
T^2L CERDIP																	
PD9624		C	0	0	0	0	0	1	2	0	0	0	1	0	1	4	9
		D	0	0	1	1	1	2	0	0	0	2	3	10	11	7	7
PD9625		C	0	0	0	0	0	0	0	0	0	0	1	0	0	13	14
		D	0	0	0	0	0	0	0	0	0	0	0	1	1	3	3

(a) Total devices out of test limits at test conclusion

Table 4.5 - SUMMARY OF CATASTROPHIC (C) AND DEGRADATION (D) FAILURES
STEP STRESS, 125°C OPERATING LIFE - 24 Hours per Step

Dissipation, mW			200	300	400	500	600	700	800	900	1000	TOTAL (a)
Type	Initial No.	Type Failure										
DTL CERPAC												
PL9932	20	C	0	0	0	0	0	0	0	0	2	2
		D	0	0	0	0	0	0	0	0	0	0
		B*	0	0	0	0	0	0	0	0	2	2
PL9945	20	C	0	0	0	0	0	0	0	1	9	10
		D	0	0	0	0	0	0	0	0	0	0
PL9962	20	C	0	0	0	0	0	0	0	0	0	0
		D	0	0	0	3	3	3	3	4	7	7
		B*	0	0	0	6	0	0	0	0	0	6
mW RTL TO-5												
PL9909	20	C	0	0	0	0	0	0	0	0	0	0
		D	0	0	0	0	0	0	0	0	0	0
PL9910	20	C	0	0	0	0	0	0	0	0	0	0
		D	0	0	0	0	0	0	0	0	0	0
PL9913	20	C	0	0	0	0	0	0	0	0	0	0
		D	0	0	0	0	0	0	0	0	0	0
T^2L CERDIP												
PD9624	20	C	0	0	0	0	0	0	0	0	0	0
		D	0	0	0	0	0	0	6	10	11	11
PD9625	20	C	0	0	0	0	0	2	0	2	1	5
		D	0	0	0	0	0	0	0	0	4	4
		B*	0	0	0	0	0	3	0	0	0	3

(a) Total devices out of test limits at test conclusion.

*B Burnout during setup. (Includes one mechanical damage)

Table 4.6 - SUMMARY OF CATASTROPHIC (C) AND DEGRADATION (D) FAILURES

			1. Step Stress Constant Acceleration YI Plane						2. Step Stress Pneupactor Shock, YI Plane					
Acceleration x 1000G:			20	40	60	80	100	Total(a) Failure	20	40	60	80	100	Total(a) Failure
TYPE	No. Devices	Type Fail.												
CERPAC														
PL9932	5	C	0	0	0	0	0	0	0	0	0	0	0	0
		D	1	0	1	1	1	1	0	0	0	0	0	0
		P							0	0	0	0	1	1
PL9945	5	C	0	0	0	0	0	0	0	0	0	0	0	0
		D	0	0	0	0	0	0	0	0	0	0	0	0
		P							0	0	0	0	3	3
PL9962	5	C	0	0	0	0	0	0	0	0	0	0	0	0
		D	0	0	0	0	0	0	0	0	0	0	0	0
		P							0	0	0	0	1	1
TO-5														
PL9909	5	C	0	0	0	0	0	0	0	0	0	0	-	0
		D	0	0	0	0	0	0	0	0	0	0	-	0
		P							0	0	4	0	-	4
PL9910	5	C	0	0	0	0	0	0	0	0	0	0	-	0
		D	0	0	0	0	0	0	0	0	0	0	-	0
		P							0	0	6	0	1	7
PL9913	5	C	0	0	0	0	0	0	0	0	0	0	-	0
		D	0	0	0	0	0	0	0	0	0	0	-	0
		P							0	0	1	5	-	6
CERDIP														
PD9624	5	C	0	0	0	0	0	0	0	0	0	0	-	0
		D	0	0	0	0	0	0	0	0	0	0	-	0
		P							0	0	0	0	-	0
PD9625	5	C	0	0	0	0	0	0	0	0	0	0	-	0
		D	0	0	0	0	0	0	0	0	0	0	-	0
		P							0	0	0	1	-	1

P - Package Damage caused by fixture problem.

(a) Total devices out of test limits at test conclusion.

Table 4.7 - SUMMARY OF DEGRADATION FAILURES *

1. Thermal Shock and 2. Reverse Bias Tests

1. Thermal Shock: -65°C 5 Min., +25°C 3 sec., +200°C 5 min. per cycle

No. Thermal Cycles		20	40	60	80	100	120	140	160	180	200	Total (a)
TYPE	No. of Devices											
CERPAC												
PL9932	12	0	0	0	0	0	0	0	0	0	0	0
PL9945	12	0	1	0	0	0	0	0	0	0	0	0
PL9962	12	0	0	0	0	0	0	0	0	0	0	0
TO-5												
PL9909	12	0	0	0	0	0	0	0	0	0	0	0
PL9910	12	0	0	0	0	0	0	0	0	0	0	0
PL9913	12	0	0	0	0	0	0	0	0	0	0	0
CERDIP												
PD9624	12	0	0	0	1	1	1	1	1	1	1	1
PD9625	12	0	0	0	0	0	0	0	0	0	0	0

2. Reverse Bias at maximum rated voltage - 200 hours per step

Temperature °C:		75	100	125	150	Total(a)
Type	No. of Devices					
CERPAC						
PL9932	10	0	0	0	0	0
PL9945	10	0	0	0	0	0
PL9902	10	0	0	0	3	3
TO-5						
PL9909	10	0	0	0	0	0
PL9910	10	0	0	0	0	0
PL9913	10	0	0	0	0	0
CERPAC						
PD9624	10	0	0	0	0	0
PD9625	10	0	0	0	0	0

* No catastrophic Failures
(a) Total devices out of test limits at test conclusion

Table 4.8 - SUMMARY OF CATASTROPHIC FAILURE MODES

Device Type Test	Initial No. Devices	DIE					PACKAGE					HANDLING DAMAGE	
		Oxide Defect	Open Metal	Diode Degrad.	Shorted Junc.	Electro-migration	Oxidized Leads	Au-Al Post	Bond Separation		Seal Frit Soften	Fixture	Burn-out
									Post	Post & Header			
STORAGE LIFE													
CERPAC													
PL9932	20	1									5		
PL9945	20										13		
PL9962	20												
TO-5													
PL9909	20									9			
PL9910	20								1				
PL9913	20			2				3	1	10			
CERDIP													
PD9624	20			1			4			4			
PD9625	20						1			13			
OPERATION LIFE *													
CERPAC													
PL9932	20					2							2
PL9945	20					10							
PL9962	20												6
CERDIP													
PD9624	20												
PD9625	20		2		2	1						1	2
PNEUPACTOR SHOCK													
CERPAC													
PL9932	15											1	
PL9945	15											3	
PL9962	15											1	
TO-5													
PL9909	15												
PL9910	15											4	
PL9913	15											7	
												6	
CERDIP													
PD9624	15												
PD9625	15											1	

* No TO-5 failures

SECTION V

TEST VEHICLE DESCRIPTION AND DESIGN APPRAISAL

5.1 Device Description

5.1.1 Diode Transistor Logic (DTL)

a. The PL9932 is a dual four input buffer circuit featuring a pull-up emitter follower output that permits high capacitive loading and a high current output transistor providing high fan-out capability. The technical specifications are given in Fig. 5.1.

b. The PL9945 is a RS/JK master-slave clocked flip-flop. Input data is stored when the clock is high and is transferred to the slave when the clock goes low. An improved direct set and clear design allows asynchronous entry irrespective of signals applied to any other input. An output buffer provides isolation between the "slave" and the output load, improving signal line noise immunity. The technical specifications are given in Fig. 5.2.

c. The PL9962 is a triple three input gate circuit. Fan-out capability is 8 for each output. The outputs may be connected to perform collector OR logic. The technical specifications are given in Fig. 5.3.

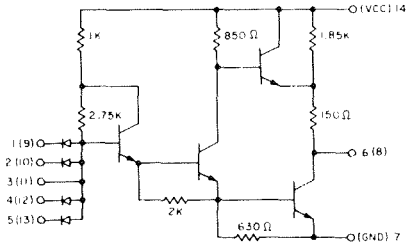
5.1.2 Milliwatt RTL (mWRTL)

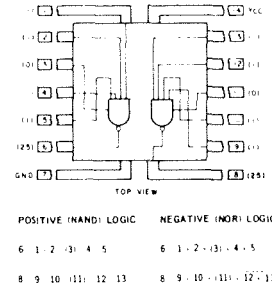
a. The PL9909 buffer is a low impedance driver having higher fan-out capability than the basic RTL gate. An internal timing resistor is available to permit capacitive coupling for use in monostable and astable multivibrators and in pulse differentiation. The technical specifications are given in Fig. 5.4.

b. The PL9910 dual gate is a dual two input NAND/NOR gate which may be used as a set-reset flip-flop, a double inverter, or a pair of inverters. With an expander, it can provide a dual NAND/NOR with increased fan-in. The technical specifications are given in Fig. 5.5.

c. The PL9913 register is a set-reset "D" flip-flop for use in shift register or counter applications. When T is high, direct set and reset inputs, S and R, control the output state. If S & R are low, the state preset at A_0 will be stored when T goes from high to low. A change in A_0 while T is low will not affect the output. The technical specifications are given in Table 5.6.

Figure 5.1 – 9932 DUAL FOUR INPUT BUFFER CIRCUIT





Fan-in and fan-out units are shown in parentheses.

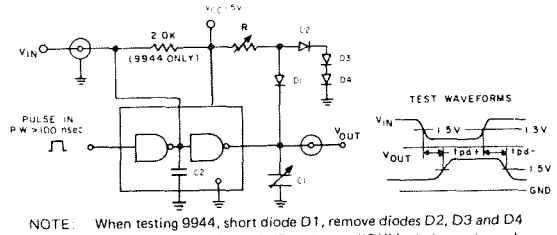
CHARACTERISTIC	SYMBOL	SENSE	TEST CONDITIONS					NOTE	FULL TEMP RANGE (-51)						UNIT	LIMITED TEMP RANGE (-59)					
			DIODE INPUTS		EXPANDER INPUTS	OUTPUTS	SUPPLY (PIN 14)		-55°C		+25°C		+125°C			0°C		+25°C		+75°C	
			SINGLE	OTHER					MIN	MAX	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX	MIN	MAX
OUTPUT LOW VOLTAGE	VOL	VOUT	VIH		–	IOL	VCL	2		0.40		0.40		0.45	Vdc		0.45		0.45		0.50
OUTPUT HIGH VOLTAGE	VOH	VOUT	VIL			IOH	VCL	3	2.5		2.6		2.5		Vdc	2.6		2.6		2.5	
					VX	IOH	VCL				2.6							2.6			
INPUT REVERSE CURRENT	IR	IIN	VR	GND			VCH	4		2		2		5	μAdc		5		5		10
INPUT FORWARD CURRENT	IF	IIN	VF	VR			VCH	5		-1.60		-1.60		-1.50	mAdc		-1.40		-1.40		-1.33
OUTPUT LEAKAGE CURRENT	ICEX	IOUT	GND			VCEX	VCL	6				50			μAdc				50		
OUTPUT SHORT CIRCUIT CURRENT	ISC	IOUT	GND			GND	VCH	6	-16		-18		-16		mAdc	-16		-16		-14	
POWER DRAIN CURRENT	IPD	ICC					VPD					26.6			mAdc				30.0		
	IMAX		GND				VMAX	6				6							8		
SWITCHING TIME PROPAGATION DELAY	tpd+	VIN (t)	R = 510Ω, C = 500 pF					7			25	80			nsec			25	80		
	tpd-	VOUT (t)	R = 150Ω, C = 500 pF								15	40						15	40		

CIRCUIT TEMPERATURE RANGE	TEST TEMPERATURE	VIH	VIL	VX	VR	VF	IFD	VCEX	IOL	IOH	IOL	ICE	VCL	VCH	VPD	VMAX
		Vdc	Vdc	Vdc	Vdc	Vdc	mAdc	Vdc	mAdc 9932	mAdc 9932	mAdc 9944	mAdc	Vdc	Vdc	Vdc	Vdc
Full (-51)	-55°C	2.1	1.40		4.0	0	2.0		34	-2.0	36		4.5	5.5		
	+25°C	1.9	1.10	1.8	4.0	0	2.0	4.5	36	-2.5	40	5.0	4.5	5.5	5.0	8.0
	+125°C	1.7	0.80		4.0	0	2.0		32	-4.0	36		4.5	5.5		
Limited (-59)	0°C	2.0	1.20		4.0	0.45	2.0		36	-2.0	40		5.0	5.0		
	+25°C	1.9	1.10	1.8	4.0	0.45	2.0	5.0	36	-2.5	40	5.0	5.0	5.0	5.0	8.0
	+75°C	1.8	0.95		4.0	0.45	2.0		34	-3.0	38		5.0	5.0		

TEST NOTES

1. Tests are identical for each circuit element. Pin 7 is grounded for all tests.
2. VIH is simultaneously applied to all diode inputs of the circuit element being tested.
3. VIL is sequentially applied to single diode inputs of the circuit element being tested. The other diode inputs of that circuit element are open.
4. VR is sequentially applied to single diode inputs of the circuit element being tested. The other diode inputs of that circuit element are grounded.
5. VF is sequentially applied to single diode inputs of the circuit element being tested. VR is simultaneously applied to the other diode inputs of that circuit element.
6. Ground is simultaneously applied to one diode input of each circuit element.
7. Refer to Switching Time Test Circuit for additional information.
8. Ground is sequentially applied to single diode inputs of the circuit element being tested. The other diode inputs of that circuit element are open.

SWITCHING TIME TEST CIRCUIT

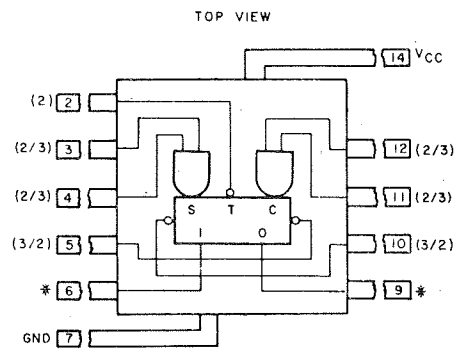


NOTE: When testing 9944, short diode D1, remove diodes D2, D3 and D4 and add capacitor C2 = 20 pF as shown. "C1" includes probe and jig capacity.

Figure 5.2

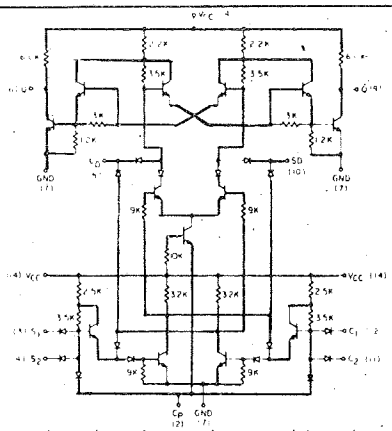
9945 RS/JK MASTER-SLAVE CLOCKED FLIP FLOP

LOADING DIAGRAM



Fan-in and fan-out units are shown in parentheses.
(*) 9945-51(10); 9945-59(12)

CIRCUIT DIAGRAM



Pin numbers shown in parentheses, resistor values are approximate.

ELECTRICAL CHARACTERISTICS (Note 1)

CHARACTERISTIC	SYMBOL	SENSE	FORCING CONDITIONS (Note 1)											NOTE	TEST LIMITS						UNITS	TEST LIMITS					
			CP (2)	S_1 (3)	S_2 (4)	C_D (5)	Q (6)	$\bar{Q}$ (9)	S_D (10)	C_2 (11)	C_1 (12)	Vcc (14)			-55°C		+25°C		+125°C			0°C		+25°C		+75°C	
															MIN	MAX	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX	MIN	MAX
OUTPUT LOW VOLTAGE	VOL	VOUT	CPc	GND	–	–	IOL	–	*	–	–	VCL		2 4	–	.40	–	.40	–	.45	Vdc	–	.45	–	.45	–	.50
OUTPUT HIGH VOLTAGE (DATA INPUTS)	VOH	VOUT	CPa	VIH	VIH	*	IOH	–	–	–	VIL	VCL		2 3 7	3.1	–	3.1	–	3.1	–	Vdc	3.1	–	3.1	–	3.1	–
OUTPUT HIGH VOLTAGE (SET-RESET INPUTS)	VOH	VOUT	CPa	GND	GND	VCL	IOH	–	VILS	–	–	VCL		3	3.1	–	3.1	–	3.1	–	Vdc	3.1	–	3.1	–	3.1	–
INPUT REVERSE CURRENT (DATA INPUTS)	IR	IIN	GND	VR	–		–	–	–	–	–	VCH		5	–	20	–	20	–	50	μAdc	–	50	–	50	–	100
INPUT REVERSE CURRENT (SET RESET INPUTS)	IR	IIN	CPa	GND	GND	VR	–	–	VCH	–	–	VCH		3	–	20	–	20	–	50	μAdc	–	50	–	50	–	100
INPUT FORWARD CURRENT (DATA INPUTS)	2/3 IF	IIN	VR	VF	VR	–	–	–	–	–	–	VCH		6	–	-1.07	–	-1.07	–	-1.00	mAdc	–	-.95	–	-.95	–	-.90
INPUT FORWARD CURRENT (SET RESET INPUTS)	IFS	IIN			–	VF	–	–	–	GND	GND	VCH		–	–	-2.4	–	-2.4	–	-2.1	mAdc	–	-2.1	–	-2.1	–	-2.0
INPUT REVERSE CURRENT (CLOCK INPUT)	IRCP	ICP	VR	GND	GND	GND	–	–	–	–	–	VR		–	–	10	–	10	–	20	μAdc	–	20	–	20	–	30
INPUT FORWARD CURRENT (CLOCK INPUT)	IFCP	ICP	VF	–	–	VILS	–	–	–	–	–	VCH		–	–	-3.2	–	-3.2	–	-2.8	mAdc	–	-2.8	–	-2.8	–	-2.66
OUTPUT SHORT CIRCUIT CURRENT	ISC	IOUT	VCH	–	–	GND	GND	–	GND	–	–	VCH		–	-.70	-1.33	-.70	-1.33	-.625	-1.30	mAdc	-.59	-1.41	-.59	-1.41	-.55	-1.38
POWER DRAIN CURRENT	IPD	IVC	VPD	–	–	–	–	–	–	–	–	VPD		–	–	–	–	14.0	–	–	mAdc	–	–	–	15.0	–	–
POWER DRAIN CURRENT	IMAX	IVC	GND	GND	GND	GND	–	–	GND	GND	GND	VMAX		–	–	–	–	16.0	–	–	mAdc	–	–	–	17.0	–	–
SWITCHING TIME PROPAGATION DELAY	t_{pd+}	VIN (t)	R = 2.0K, C = 30 pF											8	–	–	–	75	–	–	nsec	–	–	–	80	–	–
	t_{pd-}	VOUT (t)	R = 330Ω, C = 50 pF												–	–	–	75	–	–		–	–	–	80	–	–

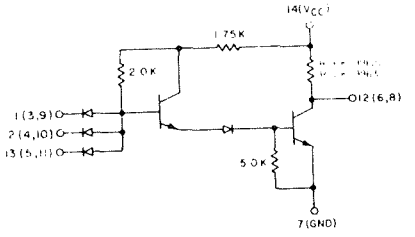
TEST NOTES

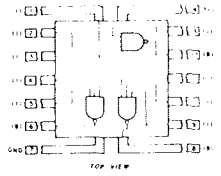
1. Pin 7 is grounded for all tests. All tests except IPD and IMAX are symmetrical with respect to Q and $\bar{Q}$: That is, all tests are illustrated on one side of the flip flop only. Corresponding tests are made by interchanging S_1, S_2, CD, and Q with C_1, C_2, SD and $\bar{Q}$ respectively.
2. The * means momentary ground prior to clock pulse.
3. CPa goes from VOH to VF.
4. CPc goes from VOH to VCPTH.
5. VR is applied individually to one input each test. Other inputs are open.
6. VF is applied individually to one input each test. Other inputs are open.
7. VIL is applied individually to one input each test. Other inputs are open.
8. Refer to Switching Time Test Circuit for additional information. For design purposes a minimum propagation delay of 20 nsec may be assured.

FORCING CONDITIONS

CIRCUIT TEMPERATURE RANGE	TEST TEMP. °C	VIH	VIL	VILS	VF	VR	VCPTH	IOL	IOH	VCL	VCH	VPD	VMAX
		Vdc	Vdc	Vdc	Vdc	Vdc	Vdc	mAdc	μAdc	Vdc	Vdc	Vdc	Vdc
Full (-51)	-55	2.1	1.4	1.4	0	4.0	1.10	14.6	-120	4.5	5.5	–	–
	+25	1.9	1.1	1.1	0	4.0	.95	15.2	-120	4.6	5.6	5.0	8.0
	+125	1.7	0.8	0.8	0	4.0	.75	13.8	-120	4.5	5.5	–	–
Limited (-59)	0	2.0	1.2	1.2	.45	4.0	1.0	16.8	-120	5.0	5.0	–	–
	+25	1.9	1.1	1.1	.45	4.0	.95	16.8	-120	5.0	5.0	5.0	8.0
	+75	1.8	.95	.95	.50	4.0	.85	16.0	-120	5.0	5.0	–	–

Figure 5.3 - 9962 TRIPLE THREE INPUT GATE CIRCUIT





POSITIVE (NAND) LOGIC: $12 = 1 \cdot 2 \cdot \overline{13}$; $6 = 3 \cdot 4 \cdot \overline{5}$; $8 = 9 \cdot \overline{10} \cdot \overline{11}$

NEGATIVE (NOR) LOGIC: $12 = \overline{1 + 2 + 13}$; $6 = \overline{3 + 4 + 5}$; $8 = \overline{9 + 10 + 11}$

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST SYMBOL	SENSE	FORCING CONDITIONS: DIODE INPUTS SINGLE	FORCING CONDITIONS: DIODE INPUTS OTHER	FORCING CONDITIONS: EXPANDER INPUTS	FORCING CONDITIONS: GATE OUTPUTS	FORCING CONDITIONS: SUPPLY (PIN 14)	NOTE	FULL TEMP. RANGE (51): -55°C MIN	-55°C MAX	+25°C MIN	+25°C MAX	+125°C MIN	+125°C MAX	UNIT	LIMITED TEMP. RANGE (59): 0°C MIN	0°C MAX	+25°C MIN	+25°C MAX	+75°C MIN	+75°C MAX
OUTPUT LOW VOLTAGE	VOL	VOUT	VIH			IOL	VCL	2		0.40		0.40		0.45	Vdc		0.45		0.45		0.50
OUTPUT HIGH VOLTAGE	VOH	VOUT	VIL			IOH	VCL	3	2.50		2.60		2.50	-	Vdc	2.60		2.60		2.50	
INPUT REVERSE CURRENT	IR	IIN	VR	GND			VCH	4		2		2		5	μAdc		5	-	5		10
INPUT FORWARD CURRENT	IF	IIN	VF	VR			VCH	5	-	-1.60		-1.60	-	-1.50	mAdc	-	-1.40	-	-1.40	-	-1.33
OUTPUT LEAKAGE CURRENT	ICEX	IOUT	GND			VCEX	VCL	6				50			μAdc				50		
OUTPUT SHORT CIRCUIT CURRENT	ISC	IOUT	GND			GND	VCH	6		-1.34	-0.61	-1.34		-1.30	mAdc		-1.30	-0.61	-1.30		-1.25
POWER DRAIN CURRENT	IPD	ICC					VPD					9.75			mAdc				12		
	IMAX		GND				VMAX	6				8.25							12		
SWITCHING TIME PROPAGATION DELAY	t_{pd+}	VIN(t) VOUT(t)	R = 3.9K, C = 30 pF; R = 400Ω, C = 50 pF					7			25	80			nsec			25	80		
	t_{pd-}										10	30						10	30		
SWITCHING TIME PROPAGATION DELAY	t_{pd+}	VIN(t) VOUT(t)	R = 3.9K, C = 30 pF; R = 400Ω, C = 50 pF					7			15	50			nsec			15	50		
	t_{pd-}										10	30						10	30		

FORCING CONDITIONS

CIRCUIT TEMPERATURE RANGE	TEST TEMPERATURE	VIH Vdc	VIL Vdc	VX Vdc	VR Vdc	VF Vdc	VCEX Vdc	IOL(6K) mAdc	IOL(2K) mAdc	IOH μAdc	VCL Vdc	VCH Vdc	VPD Vdc	VMAX Vdc
Full (-51)	-55°C	2.1	1.40		4.0	0		11.4	10.0	-120	4.5	5.5	-	-
	+25°C	1.9	1.10	1.8	4.0	0	4.5	12.0	10.6	-120	4.5	5.5	5.0	8.0
	+125°C	1.7	0.8	-	4.0	0	-	10.8	9.5	-120	4.5	5.5	-	-
Limited (-59)	0°C	2.0	1.20		4.0	0.45		12.0	10.5	-120	5.0	5.0	-	-
	+25°C	1.9	1.10	1.8	4.0	0.45	5.0	12.0	10.5	-120	5.0	5.0	5.0	8.0
	+75°C	1.8	0.95		4.0	0.50		11.4	10.2	-120	5.0	5.0		-

TEST NOTES

1. Tests and test conditions are identical for each gate element. Pin 7 is grounded for all tests.
2. VIH is simultaneously applied to all diode inputs of the gate element being tested.
3. VIL is sequentially applied to single diode inputs of the gate element being tested. The other diode inputs of that gate element are open.
4. VR is sequentially applied to single diode inputs of the gate element being tested. The other diode inputs of that gate element are grounded.
5. VF is sequentially applied to single diode inputs of the gate element being tested. VR is simultaneously applied to the other diode inputs of that gate element.
6. Ground is simultaneously applied to one diode input of each gate element.
7. Refer to the Switching Time Test Circuit for additional information.

SWITCHING TIME TEST CIRCUIT

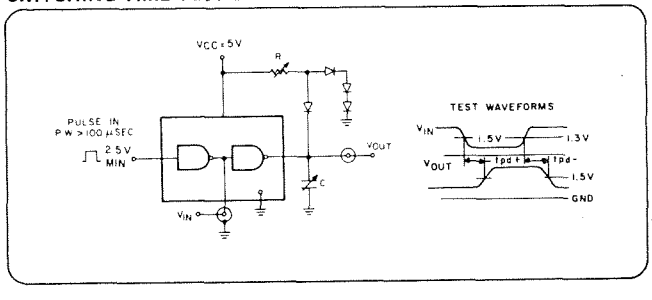
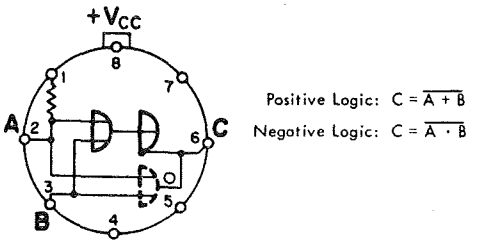


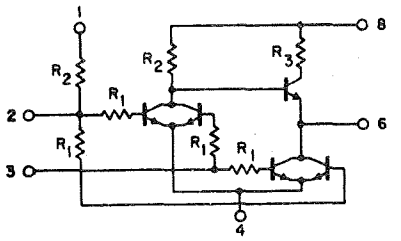
Figure 5.4

PL9909 BUFFER

LOGIC DIAGRAM



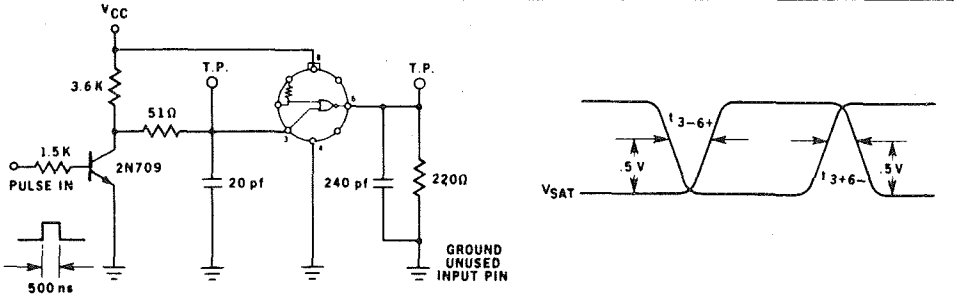
SCHEMATIC



Typical Resister Values

R_1 = 1.5 kΩ
R_2 = 3.6 kΩ
R_3 = 100Ω

SWITCHING TIME TEST CIRCUIT



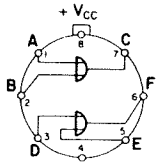
ELECTRICAL CHARACTERISTICS

TEST TITLE	TEST CONDITIONS								UNITS	TEST LIMITS	
	Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8		Min	Max
I_2		V_{IN}	V_{BOT}	GND				V_{CC}	μA		2 I_{IN}
I_3		V_{BOT}	V_{IN}	GND				V_{CC}	μA		2 I_{IN}
I_6		V_{OFF}	V_{OFF}	GND		V_{IN}		V_{CC}	mA	I_{AB}	
V_6		V_{ON}	GND	GND		V_{RH}		V_{CC}	mV		V_{OUT}
V_6		GND	V_{ON}	GND		V_{RH}		V_{CC}	mV		V_{OUT}
V_6		V_{IN}	GND	GND		V_{RH}		V_{CC}	mV		V_{CE}
V_6		GND	V_{IN}	GND		V_{RH}		V_{CC}	mV		V_{CE}
I_8		GND	GND	GND				V_{CC}	μA		I_L
t_{3+6-}		GND	Pulse in	GND		Pulse out		V_{CC}	ns		90
t_{3-6+}		GND	Pulse in	GND		Pulse out		V_{CC}	ns		70

Figure 5.5

PL9910 DUAL GATE

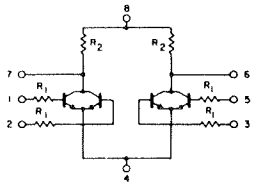
LOGIC DIAGRAM



Positive Logic: $C = \overline{A + B}$, $F = \overline{D + E}$

Negative Logic: $C = \overline{A \cdot B}$, $F = \overline{D \cdot E}$

SCHEMATIC

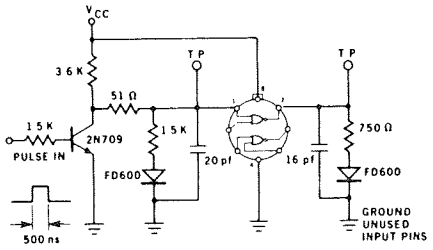


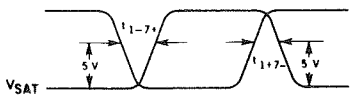
Typical Resistor Values

$R_1 = 1.5\ k\Omega$

$R_2 = 3.6\ k\Omega$

SWITCHING TIME TEST CIRCUIT



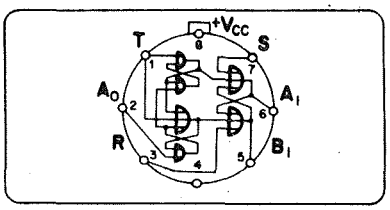


ELECTRICAL CHARACTERISTICS *

TEST TITLE	TEST CONDITIONS								UNITS	TEST LIMITS	
	Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8		Min	Max
I_1	V_{IN}	V_{BOT}	GND	GND	GND			V_{CC}	μA		I_{IN}
I_2	V_{BOT}	V_{IN}	GND	GND	GND			V_{CC}	μA		I_{IN}
I_3	GND	GND	V_{IN}	GND	V_{BOT}			V_{CC}	μA		I_{IN}
I_5	GND	GND	V_{BOT}	GND	V_{IN}			V_{CC}	μA		I_{IN}
I_7	V_{OFF}	V_{OFF}	V_{BOT}	GND	GND		V_{IN}	V_{CC}	μA	I_{A4}	I_{AM}
I_6	GND	V_{BOT}	V_{OFF}	GND	V_{OFF}	V_{IN}		V_{CC}	μA	I_{A4}	I_{AM}
V_7	V_{ON}	GND	GND	GND	GND			V_{CC}	mV		V_{OUT}
V_7	GND	V_{ON}	GND	GND	GND			V_{CC}	mV		V_{OUT}
V_6	GND	GND	V_{ON}	GND	GND			V_{CC}	mV		V_{OUT}
V_6	GND	GND	GND	GND	V_{ON}			V_{CC}	mV		V_{OUT}
V_6	GND	GND	V_{IN}	GND	GND			V_{CC}	mV		V_{CE}
V_6	GND	GND	GND	GND	V_{IN}			V_{CC}	mV		V_{CE}
V_7	V_{IN}	GND	GND	GND	GND			V_{CC}	mV		V_{CE}
V_7	GND	V_{IN}	GND	GND	GND			V_{CC}	mV		V_{CE}
I_8	GND	GND	GND	GND	GND			V_{CC}	μA		I_L
t_{1-7+}	Pulse in	GND	GND	GND	GND		Pulse out	V_{CC}	ns		40
t_{1+7-}	Pulse in	GND	GND	GND	GND		Pulse out	V_{CC}	ns		50

Figure 5.6

PL9913 REGISTER

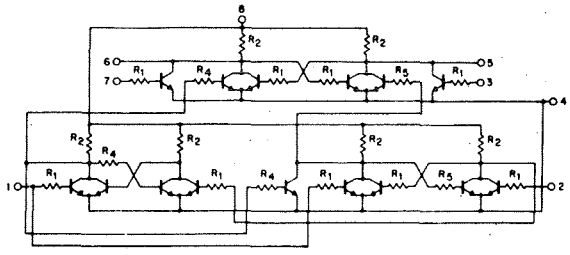


TRUTH TABLE

BIT TIME n		BIT TIME n+1					
A_1	B_1	S	R	A_0	T	A_1	B_1
Y	$\bar{Y}$	0	0	X	1	Y	$\bar{Y}$
Y	$\bar{Y}$	1	0	X	1	0	1
Y	$\bar{Y}$	0	1	X	1	1	0
X	X	1	1	X	1	0	0
1	0	0	0	1	0*	1	0
0	1	0	0	1	0*	1	0
1	0	0	0	0	0*	0	1
0	1	0	0	0	0*	0	1

Notes: Y - logical 1 or 0
X - don't care
* - for time immediately after T's 1 to 0 transition and lasting until next 1 to 0 transition

LOGIC DIAGRAM



Typical Resistor Values

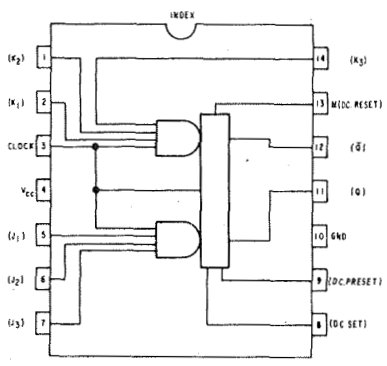
R_1 = 1.5 kΩ
R_4 = 480 kΩ
R_2 = 3.6 kΩ
R_5 = 180Ω

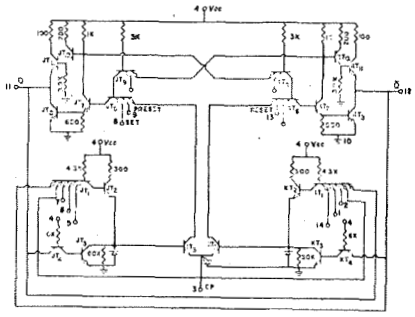
ELECTRICAL CHARACTERISTICS

TEST TITLE	TEST CONDITIONS								UNITS	TEST LIMITS	
	Pin 1	Pin 2	Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8		Min	Max
V_5	V_{BOT}	GND	V_{ON}	GND			V_{BOT}	V_{CC}	mV		V_{OUT}
V_6	V_{BOT}	GND	V_{BOT}	GND			V_{ON}	V_{CC}	mV		V_{OUT}
V_5	V_{BOT}	GND	GND	GND	"D"	V_{ON}	GND	V_{CC}	mV		V_{OUT}
V_6	V_{BOT}	GND	GND	GND	V_{ON}	"D"	GND	V_{CC}	mV		V_{OUT}
V_5	V_{BOT}	GND	V_{IN}	GND			V_{BOT}	V_{CC}	mV		V_{CE}
V_6	V_{BOT}	GND	V_{BOT}	GND			V_{IN}	V_{CC}	mV		V_{CE}
V_5	V_{BOT}	GND	GND	GND	"D"	V_{IN}	GND	V_{CC}	mV		V_{CE}
V_6	V_{BOT}	GND	GND	GND	V_{IN}	"D"	GND	V_{CC}	mV		V_{CE}
I_1	V_{IN}	GND	GND	GND			GND	V_{CC}	μA		$1.8\ I_{IN}$
I_1	V_{IN}	V_{BOT}	GND	GND			GND	V_{CC}	μA		$1.8\ I_{IN}$
I_5	V_{ON}	V_{BOT}	V_{OFF}	GND	V_{IN}		V_{BOT}	V_{CC}	μA	I_{A3}	
I_6	V_{ON}	GND	V_{BOT}	GND		V_{IN}	V_{OFF}	V_{CC}	μA	I_{A3}	
I_5	V_{OFF}*	GND	V_{OFF}	GND	V_{IN}		V_{BOT}	V_{CC}	μA	I_{A3}	
I_6	V_{OFF}*	V_{ON}	V_{BOT}	GND		V_{IN}	V_{OFF}	V_{CC}	μA	I_{A3}	
I_2	V_{OFF}*	V_{IN}	GND	GND			GND	V_{CC}	μA		I_{IN}
I_3	V_{OFF}*	V_{BOT}	V_{IN}	GND			GND	V_{CC}	μA		I_{IN}
I_7	V_{OFF}*	GND	GND	GND			V_{IN}	V_{CC}	μA		I_{IN}
V_5	V_{OFF}*	V_{ON}	GND	GND			V_{BOT}	V_{CC}	mV		V_{CE}
V_6	V_{OFF}*	V_{OFF}	V_{BOT}	GND			GND	V_{CC}	mV		V_{CE}
I_8	GND	GND	GND	GND			GND	V_{LL}	μA		I_L
t_{1-6-}	Pulse in	Tie to Pin 5	GND	GND		Pulse out	GND	V_{CC}	ns		80
t_{1-6+}	Pulse in	Tie to Pin 5	GND	GND		Pulse out	GND	V_{CC}	ns		120
t_{1-5-}	Pulse in	Tie to Pin 5	GND	GND	Pulse out		GND	V_{CC}	ns		80
t_{1-5+}	Pulse in	Tie to Pin 5	GND	GND	Pulse out		GND	V_{CC}	ns		120
t_{2+1-}	Pulse 1 in	Pulse 2 in	GND	GND		Pulse out	GND	V_{CC}	ns	60	
t_{1-2-}	Pulse 1 in	Pulse 2 in	GND	GND		Pulse out	GND	V_{CC}	ns	30	
t_{2-1-}	Pulse 1 in	Pulse 2 in	GND	GND		Pulse out	GND	V_{CC}	ns	60	
t_{1-2+}	Pulse 1 in	Pulse 2 in	GND	GND		Pulse out	GND	V_{CC}	ns	30	

Figure 5.7

9624 J-K Flip Flop





TRUTH TABLES

J	K	Qn.	Qn+1
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

LOGIC EQUATIONS

$Qn + 1 = J\bar{Q}n + \bar{K}Qn$

$\bar{Q}n + 1 = \bar{J}\bar{Q}n + KQn$

$J = J_1 \cdot J_2 \cdot J_3$

$K = K_1 \cdot K_2 \cdot K_3$

FORCING CONDITIONS

TEMPERATURE RANGE	TEST TEMPERATURE	$V_{I\,MIN}$	$V_{I\,MAX}$	$V_{I\,OFF}$	$V_{I\,ON}$	V_{OL}	V_{OH}	$V_{O\,MAX}$	$V_{O\,MIN}$	V_{CC}	$I_{I\,MIN1}$	$I_{I\,MIN2}$	$I_{O\,MIN}$	I_{OL}(P)	I_{OL}(S)	I_{OH}(P)	I_{OH}(S)	$I_{I\,MIN3}$	$V_{O\,MAXL}$
		Vdc	Vdc	Vdc	Vdc	Vdc	Vdc	Vdc	Vdc	Vdc	mA	mA	mA	mA	mA	mA	mA	mA	Vdc
Full	−55°C	0	4.5	0.45	2.8	0.45	2.5	5.5	0	5.0	1.0	2.0	0	22	12	1.5	0.7	4.0	4.5
	+25°C	0	4.5	0.45	2.8	0.45	2.4	5.5	0	5.0	1.0	2.0	0	22	12	1.5	0.7	4.0	4.5
	+125°C	0	4.5	0.45	2.8	0.45	2.7	5.5	0	5.0	1.0	2.0	0	22	12	1.5	0.7	4.0	4.5
Limited	0°C	0	4.5	0.45	3.0	0.45	2.5	5.5	0	5.0	1.0	2.0	0	22.5	12.5	1.2	0.6	4.0	4.5
	+25°C	0	4.5	0.45	3.0	0.45	2.4	5.5	0	5.0	1.0	2.0	0	22.5	12.5	1.2	0.6	4.0	4.5
	+75°C	0	4.5	0.45	3.0	0.45	2.5	5.5	0	5.0	1.0	2.0	0	22.5	12.5	1.2	0.6	4.0	4.5

(P) = Prime Fan Out (S) = Standard Fan Out

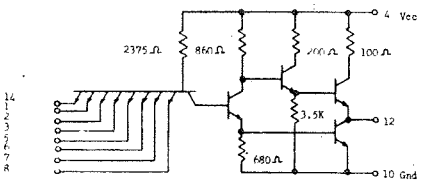
ELECTRICAL CHARACTERISTICS 9624

CHARACTERISTIC	TEST SYMBOL	FORCING CONDITIONS				NOTE	FULL TEMP RANGE						UNIT	LIMITED TEMP RANGE					
		INPUTS		OUTPUTS	SUPPLY		−55°C		+25°C		+125°C			0°C		+25°C		+75°C	
		SINGLE	OTHER				MIN	MAX	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX	MIN	MAX
INPUT LOAD CURRENT (SET, PRESET, RESET)	I_{IN}	$V_{I\,MIN}$	$V_{I\,MAX}$	$I_{O\,MIN}$	V_{CC}	1	—	2.25	—	2.25	—	2.25	mA	—	2.8	—	2.8	—	2.8
INPUT LOAD CURRENT (J & K INPUTS)	I_{IN}	$V_{I\,MIN}$	$V_{I\,MAX}$	$I_{O\,MIN}$	V_{CC}	2	—	1.33	—	1.33	—	1.33	mA	—	1.66	—	1.66	—	1.66
INPUT LOAD CURRENT (CLOCK)	I_{IN}	V_{IL}	$V_{I\,MAX}$	$I_{O\,MIN}$	V_{CC}	—	—	1.33	—	1.33	—	1.33	mA	—	1.66	—	1.66	—	1.66
INPUT LEAKAGE CURRENT (EXCEPT CLOCK)	I_{IN}	$V_{I\,MAX}$	$V_{I\,MIN}$	$I_{O\,MIN}$	V_{CC}	3	—	0.07	—	0.07	—	0.07	mA	—	0.07	—	0.07	—	0.07
INPUT LEAKAGE CURRENT (CLOCK)	I_{IN}	$V_{I\,MAX}$	$V_{I\,MIN}$	$I_{O\,MIN}$	V_{CC}	4	—	0.14	—	0.14	—	0.14	mA	—	0.14	—	0.14	—	0.14
INVERSE BETA CURRENT (EXCEPT CLOCK)	I_{IN}	$V_{I\,MAX}$	OPEN	$I_{O\,MIN}$	V_{CC}	5	—	0.07	—	0.07	—	0.07	mA	—	0.07	—	0.07	—	0.07
INVERSE BETA CURRENT (CLOCK)	I_{IN}	$V_{I\,MAX}$	OPEN	$I_{O\,MIN}$	V_{CC}	6	—	0.14	—	0.14	—	0.14	mA	—	0.14	—	0.14	—	0.14
INPUT (OFF LEVEL) BKDN. VTG. (J & K INPUTS)	BV_{IN} "1"	$I_{I\,MIN1}$	$V_{I\,MIN}$	$I_{O\,MIN}$	V_{CC}	—	5.5	—	5.5	—	5.5	—	Vdc	5.5	—	5.5	—	5.5	—
INPUT (OFF LEVEL) BKDN. VTG. (SET, PRESET, RESET)	BV_{IN} "1"	$I_{I\,MIN2}$	$V_{I\,MIN}$	$I_{O\,MIN}$	V_{CC}	3	5.5	—	5.5	—	5.5	—	Vdc	5.5	—	5.5	—	5.5	—
INPUT (OFF LEVEL) BKDN. VTG. (CLOCK)	BV_{IN} "1"	$I_{I\,MIN2}$	$V_{I\,MIN}$	$I_{O\,MIN}$	V_{CC}	4	5.5	—	5.5	—	5.5	—	Vdc	5.5	—	5.5	—	5.5	—
INPUT (ON LEVEL) BKDN. VTG. (EXCEPT CLOCK)	BV_{IN} "0"	$I_{I\,MIN1}$	OPEN	$I_{O\,MIN}$	V_{CC}	5	5.5	—	5.5	—	5.5	—	Vdc	5.5	—	5.5	—	5.5	—
INPUT (ON LEVEL) BKDN. VTG. (CLOCK)	BV_{IN} "0"	$I_{I\,MIN2}$	OPEN	$I_{O\,MIN}$	V_{CC}	6	5.5	—	5.5	—	5.5	—	Vdc	5.5	—	5.5	—	5.5	—
LOGIC "1" THRESHOLD VTG. (SET, PRESET, RESET)	V_{MIN} "1"	—		I_{OL}, V_{OL}	V_{CC}	—	—	2.0	—	1.7	—	1.4	Vdc	—	1.9	—	1.8	—	1.7
LOGIC "0" THRESHOLD VTG. (SET, PRESET, RESET)	V_{MAX} "0"	—		I_{OH}, V_{OH}	V_{CC}	—	1.0	—	1.2	—	0.9	—	Vdc	1.0	—	1.1	—	1.0	—
OUTPUT LEAKAGE CURRENT	I_{OUT}	$V_{I\,MIN}$		$V_{O\,MAX}$	V_{CC}	—	—	2.25	—	2.25	—	2.25	mA	—	2.25	—	2.25	—	2.25
OUTPUT SHORT CIRCUIT CURRENT	I_{OUT}	$V_{I\,MIN}$		$V_{O\,MIN}$	V_{CC}	—	30	90	30	90	30	90	mA	30	90	30	90	30	90
LOGIC "0" LEVEL	V_{OUT} "0"	$V_{I\,ON}$		I_{OL}	V_{CC}	—	—	0.4	—	0.4	—	0.45	Vdc	—	0.4	—	0.4	—	0.45
LOGIC "1" LEVEL	V_{OUT} "1"	$V_{I\,OFF}$		I_{OH}	V_{CC}	—	2.8	—	3.0	—	3.0	—	Vdc	3.0	—	3.0	—	3.0	—
"0" STATE CURRENT DRAIN	I_{CC} "0"	OPEN		—	V_{CC}	7	—	14	—	14	—	14	mA	—	17	—	17	—	17
"1" STATE CURRENT DRAIN	I_{CC} "1"	OPEN		—	V_{CC}	8	—	14	—	14	—	14	mA	—	17	—	17	—	17

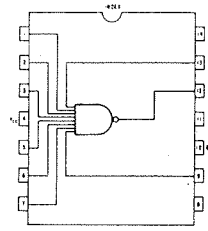
NOTES:

1. Ground set when checking reset and ground reset when checking set, preset.
2. Reset low when checking J_1, J_2, J_3 and set low when checking K_1, K_2, K_3.
3. Ground Q and leave reset open to check set and preset and ground Q and leave preset open to check reset.
4. Set, reset and present open.
5. Reset low when checking set, preset, J_1, J_2, J_3 and set low when checking reset, K_1, K_2, K_3.
6. Reset low when checking clock input at J side and set low when checking clock input at K side.
7. Reset and clock grounded.
8. Set and clock grounded.

Figure 5.8 - 9625 Single Eight Input Gate



$$12 = \overline{1 \cdot 2 \cdot 3 \cdot 5 \cdot 6 \cdot 7 \cdot 9 \cdot 13}$$



ELECTRICAL CHARACTERISTICS

* DRAIN PER GATE

CHARACTERISTIC		TEST SYMBOL	FORCING CONDITIONS INPUTS SINGLE	INPUTS OTHER	OUTPUTS	SUPPLY	NOTE	FULL TEMP RANGE −55°C MIN	−55°C MAX	+25°C MIN	+25°C MAX	+125°C MIN	+125°C MAX	UNIT	LIMITED TEMP RANGE 0°C MIN	0°C MAX	+25°C MIN	+25°C MAX	+75°C MIN	+75°C MAX
INPUT LOAD CURRENT		I_{IN}	$V_{I\ MIN}$	$V_{I\ MAX}$	$I_{O\ MIN}$	V_{CC}	1	—	2.0	—	2.0	—	2.0	mA	—	2.5	—	2.5	—	2.5
INPUT LEAKAGE CURRENT		I_{IN}	$V_{I\ MAX}$	$V_{I\ MIN}$	$I_{O\ MIN}$	V_{CC}	1	—	0.1	—	0.1	—	0.1	mA	—	0.1	—	0.1	—	0.1
INVERSE BETA CURRENT		I_{IN}	$V_{I\ MAX}$	Open	$I_{O\ MIN}$	V_{CC}	1	—	0.1	—	0.1	—	0.1	mA	—	0.1	—	0.1	—	0.1
INPUT (OFF LEVEL) BREAKDOWN VOLTAGE		BV_{IN} "I"	$I_{I\ MIN}$	$V_{I\ MIN}$	$I_{O\ MIN}$	V_{CC}	1	5.5	—	5.5	—	5.5	—	Vdc	5.5	—	5.5	—	5.5	—
INPUT (ON LEVEL) BREAKDOWN VOLTAGE		BV_{IN} "O"	$I_{I\ MIN}$	Open	$I_{O\ MIN}$	V_{CC}	1	5.5	—	5.5	—	5.5	—	Vdc	5.5	—	5.5	—	5.5	—
LOGIC "I" THRESHOLD VOLTAGE		V_{MIN} "I"	—		V_{OL}, I_{OL}	V_{CC}	1	—	2.0	—	1.7	—	1.4	Vdc	—	1.9	—	1.8	—	1.7
LOGIC "O" THRESHOLD VOLTAGE		V_{MAX} "O"	—		V_{OH}, I_{OH}	V_{CC}	1	0.9	—	1.1	—	0.9	—	Vdc	1.0	—	1.1	—	1.0	—
OUTPUT LEAKAGE CURRENT		I_{OUT}	$V_{I\ MIN}$		$V_{O\ MAX}$	V_{CC}	1	—	0.25	—	0.25	—	0.25	mA	—	0.25	—	0.25	—	0.25
OUTPUT SHORT CIRCUIT CURRENT		I_{OUT}	$V_{I\ MIN}$		$V_{O\ MIN}$	V_{CC}	1, 2	25	100	25	100	25	100	mA	25	100	25	100	25	100
LOGIC "O" LEVEL		V_{OUT} "O"	$V_{I\ ON}$		I_{OL}	V_{CC}	1	—	0.40	—	0.40	—	0.45	Vdc	—	0.40	—	0.40	—	0.45
LOGIC "I" LEVEL		V_{OUT} "I"	$V_{I\ OFF}$		I_{OH}	V_{CC}	1	2.7	—	3.1	—	3.15	—	Vdc	2.9	—	3.0	—	3.0	—
BREAKDOWN CURRENT (PER GATE)		$I_{CC\ MAX}$	$V_{I\ MIN}$		$I_{O\ MIN}$	$V_{CC\ MAX}$	1	—	—	—	6.5	—	—	mA	—	—	—	6.75	—	—
* "ON" STATE CURRENT DRAIN		I_{CC} "O"	Open		$I_{O\ MIN}$	V_{CC}	1	—	7.5	—	7.5	—	7.5	mA	—	10	—	10	—	10
* "OFF" STATE CURRENT DRAIN		I_{CC} "I"	$V_{I\ MIN}$		$I_{O\ MIN}$	V_{CC}	1	—	3.75	—	3.75	—	3.75	mA	—	5.0	—	5.0	—	5.0
TURN ON DELAY	9620, 21 & 22	t_{ON}	—		—	V_{CC}	3	—	—	—	10	—	—	nsec	—	—	—	10	—	—
	9625							—	—	—	12	—	—		—	—	—	12	—	—
	9634							—	—	—	15	—	—		—	—	—	15	—	—
TURN OFF DELAY	9620, 21 & 22	t_{OFF}	—		—	V_{CC}	3	—	—	—	10	—	—	nsec	—	—	—	10	—	—
	9625							—	—	—	10	—	—		—	—	—	10	—	—
	9634							—	—	—	10	—	—		—	—	—	10	—	—
RISE TIME	9620, 21 & 22	t_r	—		—	V_{CC}	3	—	—	—	2.5	—	—	nsec	—	—	—	2.5	—	—
	9625							—	—	—	3.0	—	—		—	—	—	3.0	—	—
	9634							—	—	—	3.0	—	—		—	—	—	3.0	—	—
FALL TIME	9620, 21 & 22	t_f	—		—	V_{CC}	3	—	—	—	4.0	—	—	nsec	—	—	—	4.0	—	—
	9625							—	—	—	4.0	—	—		—	—	—	4.0	—	—
	9634							—	—	—	4.5	—	—		—	—	—	4.5	—	—

FORCING CONDITIONS

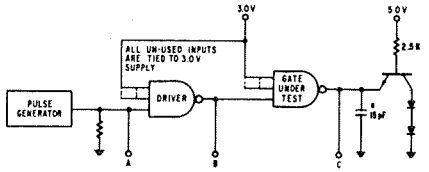
TEMPERATURE RANGE	TEST TEMPERATURE	$V_{I\ MIN}$ Vdc	$V_{I\ MAX}$ Vdc	$V_{I\ OFF}$ Vdc	$V_{I\ ON}$ Vdc	V_{OL} Vdc	V_{OH} Vdc	$V_{O\ MAX}$ Vdc	$V_{O\ MIN}$ Vdc	V_{CC} Vdc	$V_{CC\ MAX}$ Vdc	$I_{I\ MIN}$ mA	$I_{O\ MIN}$ mA	I_{OL}(P) mA	I_{OL}(S) mA	I_{OH}(P) mA	I_{OH}(S) mA
Full	−55°C	0	4.5	0.45	2.7	0.45	2.5	5.5	0	5.0	—	1.0	0	22	12	2.2	1.2
	+25°C	0	4.5	0.45	2.7	0.45	2.4	5.5	0	5.0	8.0	1.0	0	22	12	2.2	1.2
	+125°C	0	4.5	0.45	2.7	0.45	2.5	5.5	0	5.0	—	1.0	0	22	12	2.2	1.2
Limited	0°C	0	4.5	0.45	2.9	0.45	2.5	5.5	0	5.0	—	1.0	0	22.5	12.5	1.8	1.0
	+25°C	0	4.5	0.45	2.9	0.45	2.4	5.5	0	5.0	7.0	1.0	0	22.5	12.5	1.8	1.0
	+75°C	0	4.5	0.45	2.9	0.45	2.5	5.5	0	5.0	—	1.0	0	22.5	12.5	1.8	1.0

(P) = Prime Fan Out (S) = Standard Fan Out

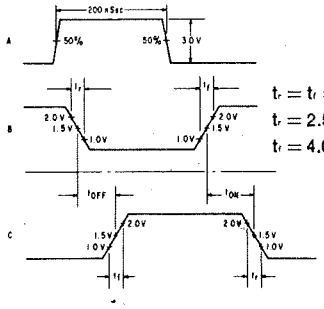
NOTES:

1. Input conditions are for one gate only. All other inputs are to be grounded.
2. Only one output at a time is to be grounded.
3. See switching time test circuit.

SWITCHING TIME TEST CIRCUIT



* 15 pF capacitance includes stray wiring, probes and load.



$t_{on} = t_r = 5.0$ nsec max
$t_{on} = 2.5$ nsec max
$t_f = 4.0$ nsec max

5.1.3 Transistor Transistor Logic (TTL)

a. The PD9624 is a J-K flip-flop which operates up to a guaranteed toggling rate of 30MHz/50MHz over the full military temperature range. Information is fed into the J and/or K inputs while the clock is low. This information is ANDed with the present state of the flip flop and stored when the clock goes high. When the clock again goes low the stored information is ANDed with the inverted clock causing the cross coupled NAND gates to be set accordingly. The 9624 has three J and three K data inputs which can be utilized to provide the AND function right in the flip flop, thus reducing the number of external NAND gates required for system operation. High toggling rates are achieved through the use of charge control devices coupled with discharge networks which allow removal of any excess stored charge at high frequency. The technical specification is given in Fig. 5.7.

b. The PD9625 is a single eight input NAND/NOR gate consisting of an eight emitter input AND gate followed by an inverting amplifier and a push-pull output stage. This gate performs a positive NAND function or negative NOR function. The push-pull output increases noise immunity and permits driving of high capacity loads with a minimum of loss in speed. The technical specification is given in Fig. 5.8.

5.2 Design Appraisals

The following design appraisals describe the construction of the particular family of devices from the final die passivation or oxidation growth through final sealing. Also included are materials used for package construction and final assembly.

5.2.1 DTL - CERPAC

5.2.1.1 Final Assembly - Components

The following are the materials required for final assembly of the DTL-CERPAC as shown in figure 5.9. The component numbers serve as the legend for this figure which also includes an outline drawing of the finished device.

1. Package lid	-	Alumina press formed in die and fired in furnace. Glazed and fired.
2. Lead wire	-	.001" Dia. Aluminum with 1% Silicon in continuous length - cut at assembly.

3. Final Wafer and
Die Processing - OUTLINE (Post Metalization)

These Wafers are passivated following the metallization procedure.

(a) Glass deposition 10,000 $\overset{o}{A}$
(b) Apply resist and bake
(c) Etch contact lands for bonding
(d) Remove resist
(e) Wafer mapping and cleaning
(f) Electrical die sort
(g) Wafer scribing
(h) Visual die sort

4. Lead frame - Partially aluminized Kovar sheet stock stamped into lead frames in a continuous pattern.

5. Package Base - Alumina press formed in die and fired in furnace. Glazed and fired.

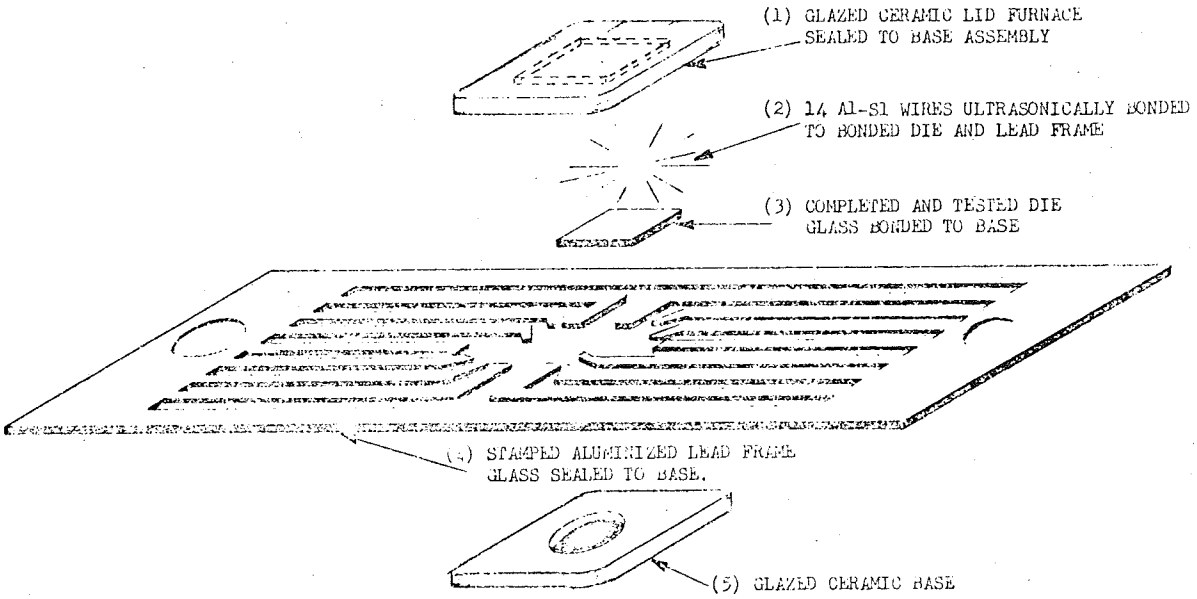
5.2.1.2 Final Assembly - Device

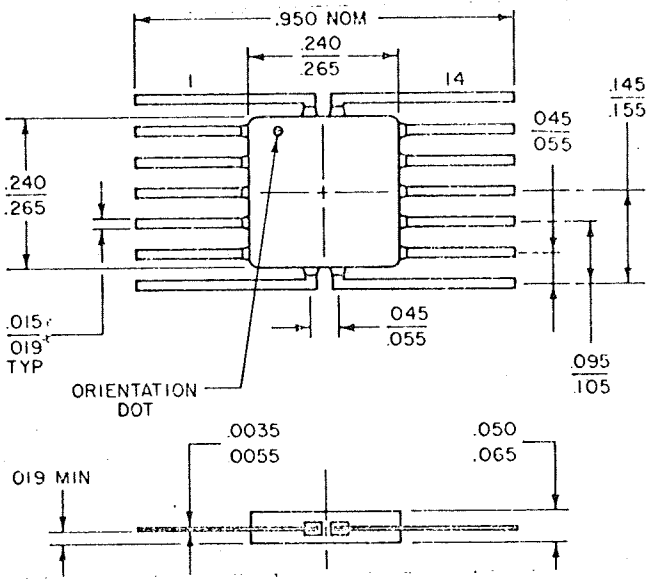
The following is the procedure for final assembly of the DTL-CERPAC as shown in Fig. 5.9. Components are numerically identified to correspond to the legend on the figure.

1. Package - die assembly - Kovar lead frame[4] pre-heated in air to oxidize. Glazed ceramic base[5] heated in fixture in air to soften glass. Pre-heated lead frame[4] placed over base and embedded in softened glass. Back of completed die[3] placed into softened glass in "well" in base[5]. Completed die-package assembly removed to cool.

2. Ultrasonic bonding of lead wires from die to leads - Al-Si[2] wires are ultrasonically "wedge" bonded to complete path between the package leads and the die lands. This method involves the application of ultrasonic energy and pressure to the lead wires and die and lead wires and lands.

Figure 5.9 - DTL CERPAC FINAL ASSEMBLY





3. Device sealing - Package is hermetically sealed after internal visual inspection to provide protection to the die and lead wires. The method involves the fixturing of the die-package assembly and the lid[1] and furnace sealing in a controlled atmosphere.

4. Lead finishing - Sealed device is cleaned and leads are plated with gold.

5. Lead trim - The sealed and finished device leads are trimmed to size in a shearing fixture which also removes the frame end on the leads.

5.2.2 mW RTL - TO-5

5.2.2.1 Final Assembly - Components

The following are the materials required for the final assembly of the mW RTL TO-5. The component numbers serve as the legend for Figure 5.10 which shows the assembly components.

A. Header Processing

1. Package eyelet - Kovar sheet stock stamped and formed into eyelets.

2. Glass Frit - Powdered Kovar sealing glass

3. Package leads - .018" D Kovar wire cut to length.

4. Pre-oxidize eyelet and leads - Eyelet and leads furnace-fired to form uniform oxide coating.

5. Fixture parts - Oxidized eyelet and leads and glass frit are placed into fixture and furnace-fired to form glass to metal seals.

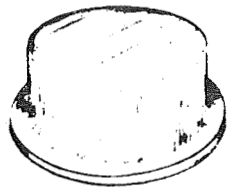
6. Lead trim - Leads are trimmed to length at both ends

7. Finish Header - Glass sealed header cleaned and plated with gold.

B. Top Shield Processing

1. Top shield - Nickel sheet stamped and formed into top shields

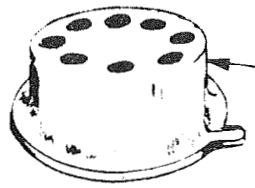
Figure 5.10 - TO-5 PACKAGE CONSTRUCTION SEQUENCE



(1) STAMPED NICKEL TOP SHIELD

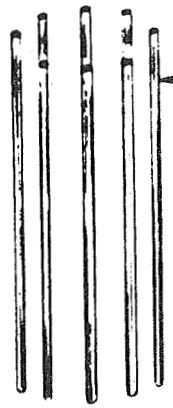
(2) CLEAN AND FIRE IN FURNACE TO ANNEX

PART A - TOP SHIELD



(1) STAMPED KOVAR EYELET

(2) GLASS FRIT



(3) EIGHT KOVAR LEADS

(4) CLEAN AND FIRE (OXIDIZE) EYELET AND LEADS

(5) FIXTURE AND FORM GLASS TO MELT SEALS IN FURNACE

(6) TRIM LEADS TO LENGTH

(7) CLEAN AND GOLD PLATE

2. Finished top shield - Top shield cleaned and annealed in furnace

C. Final Wafer and Die Processing - Outline (From final passivation step)

1. Wafers are final oxidized during the emitter drive-in process.

2. Oxide thickness measurement

3. Apply resist and bake

4. Contact mask align and expose

5. Bake and develop resist

6. Etch

7. Remove resist

8. Wafer mapping and cleaning

9. Metal deposition, delineation, and alloying

10. Wafer mapping and electrical die sort

11. Wafer scribing

12. Visual die sort

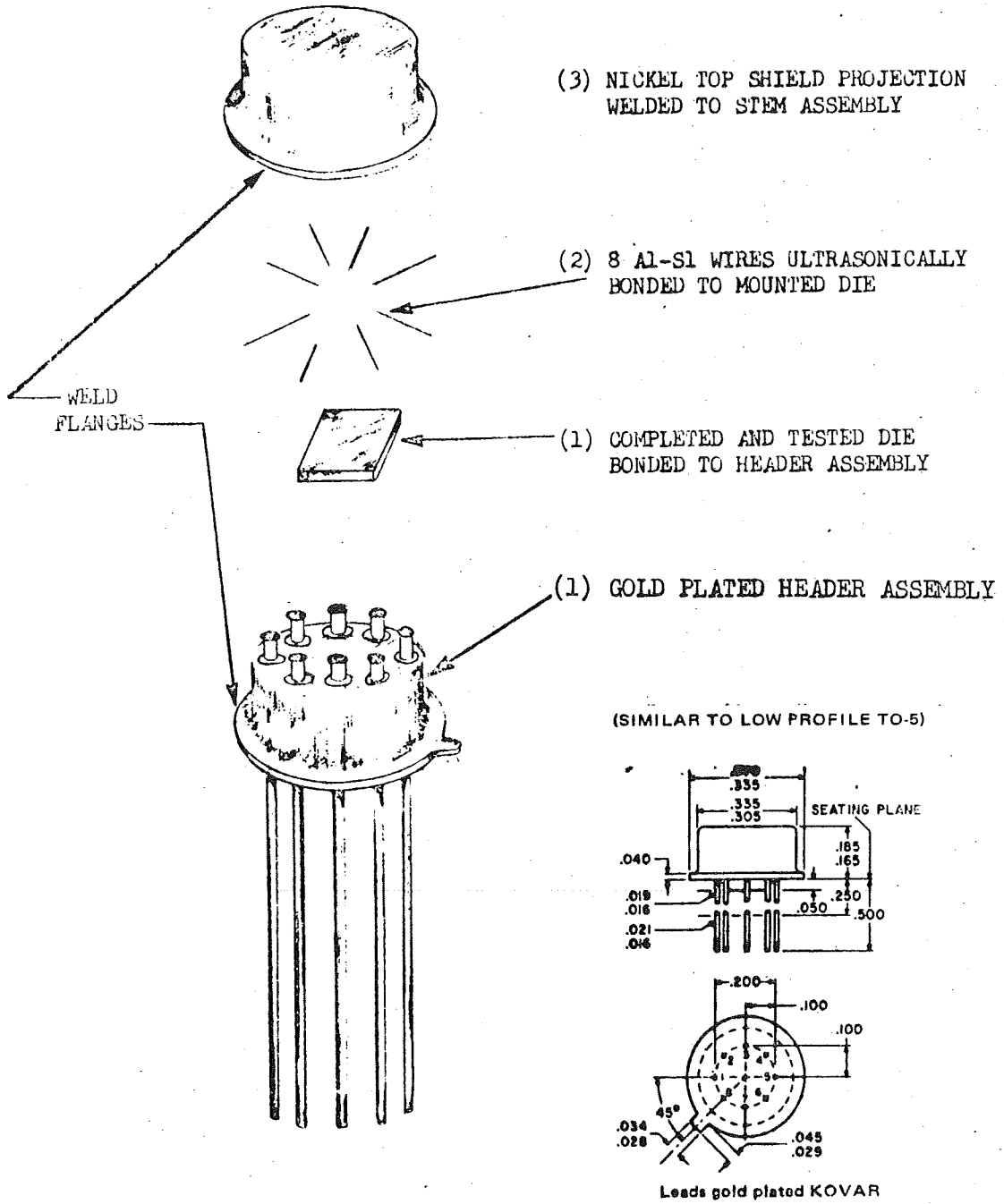
5.2.2.2 Final Assembly - Device

The following is the procedure for final assembly of the mW RTL TO-5 as shown in Fig. 5.11. The procedure numbers serve as legend for this figure which also includes an outline drawing for the finished device.

1. Die mounting on header - Finished TO-5 header is heated in fixture under nitrogen blanket. Die is orientated on header and bonded by scrubbing into place and cooling

2. Ultrasonic bonding of lead wires from die to leads - .001" Dia. Al-Si wires are ultrasonically "wedge" bonded to complete path between the package leads and die lands. This method involves the application of ultrasonic energy and pressure to the lead wires and die, and lead wires and post ends.

Figure 5.11 - RTL TO-5 FINAL ASSEMBLY



3. Top shield welding - Package is hermetically sealed after internal visual inspection and vacuum bake to provide protection to the die and lead wires. The method involves projection welding of the top shield to the finished die-header assembly in a controlled atmosphere (dry) box.

5.2.3 T^2L - CERDIP

5.2.3.1 Final Assembly-Components

The following are the materials required for the assembly of the T^2L-CERDIP, as shown in figure 5.12. The component numbers serve as legend for this figure which also includes an outline drawing of the finished device.

1. Package Lid - Alumina press formed in die and fired in furnace. Glazed and fired.

2. Lead Wire - Aluminum with 1% Silicon in continuous length - cut at assembly.

3. Final wafer and die processing - outline (from final passivation step).

   (a) Wafers are final oxidized during the emitter drive-in process.
   (b) Oxide thickness measurement
   (c) Apply resist and bake
   (d) Contact mask align and expose
   (e) Bake and develop resist
   (f) Etch
   (g) Remove resist
   (h) Wafer mapping and cleaning
   (i) Metal deposition, delineation and alloying
   (j) Wafer mapping
   (k) Electrical die sort
   (l) Wafer scribing
   (m) Visual die sort

4. Lead Frame - Aluminized Kovar sheet stock stamped and bent into lead frames in a continuous pattern by high speed press.

5. Package base - Alumina press formed in die and fired in furnace. Glazed and fired.

5.2.3.2 Final Assembly - Device

The following is the procedure for final assembly of the T^2L CERDIP as shown in Fig. 5.12. Components listed in the text are numerically identified to correspond to the legend on the figure.

A. Package - die assembly - Kovar lead frame[4] pre-heated in air to oxidize. Glazed ceramic base[5] heated in fixture in air to soften glass. Pre-heated lead frame[4] placed over base and embedded in softened glass. Back of completed die[3] placed into softened glass in "well" in base[5]. Completed die-package assembly removed to cool.

B. Ultrasonic bonding of lead wires from die to leads. - .001" Dia. Al+Si wires[2] are ultrasonically "wedge" bonded to complete path between the package leads and the die lands. This method involves the application of ultrasonic energy and pressure to the lead wires and die and lead wires and lands.

C. Lead sealing - Package is hermetically sealed after internal visual inspection to provide protection to the die and lead wires. The method involves the fixturing of the die-package assembly and the lid[1] and furnace sealing in a controlled atmosphere.

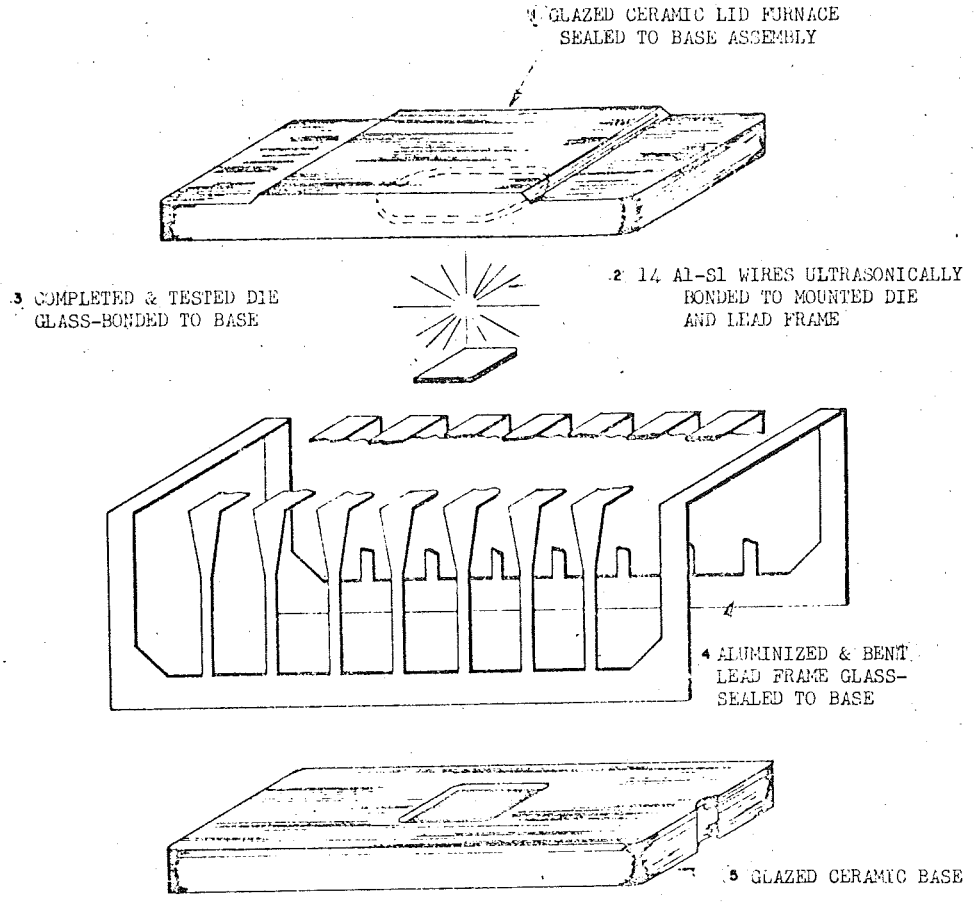
D. Lead finishing - Sealed device is cleaned and leads tinned.

E. Lead trim - The sealed and finished device leads are trimmed to size in a shearing fixture which also removes the frame end on the leads.

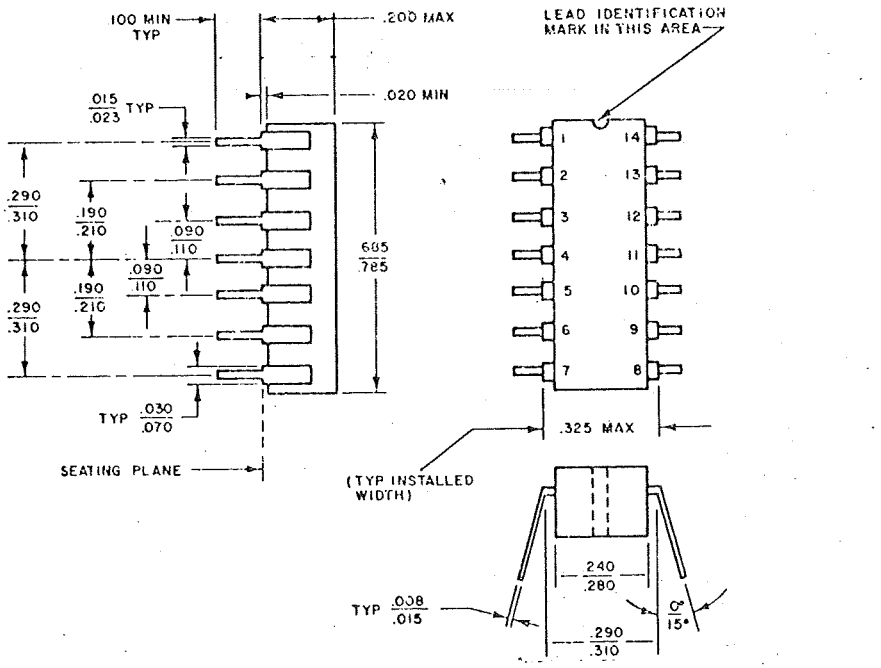
5.2.4 Post Seal Processing

The post seal processing for the selected devices consisted of device finishing, such as plating or tinning leads, gross and helium fine leak test, electrical test and branding. This was the minimum amount of testing necessary to insure that electrically acceptable devices were placed in each stress test and to eliminate

Figure 5.12 - T^2L CERDIP FINAL ASSEMBLY



Cerdip Package (TO-116)



any variables that may be introduced by non-hermetic packages.

The normal pre-conditioning procedure was omitted for these devices in order to present 'raw' devices to each stress test. This procedure normally involves high temperature stabilization bake, temperature cycling and constant acceleration, in addition to the gross and fine leak tests.

SECTION VI

DEVICE FAILURE DEFINITIONS AND FAILURE ANALYSIS

6.1. DEFINITION OF FAILURE CATEGORIES

The failure determination criteria was established as required by the program and in addition, criteria normally used by Philco-Ford for device testing was also applied. Four (4) failure categories were established - two electrical and one each physical and mechanical.

6.1.1. Catastrophic Electrical Failure:

The program requirements included that of continuing all devices on stress test unless a device developed a short or an open, or any leakage current exceeded 100 times the initial limit (except for constant acceleration test), or if reasoned that further stress testing would produce less information than an analysis, at that stress step, would provide. Any device falling within any of the above criteria would be classified a catastrophic or non-functional failure.

6.1.2. Degradation Electrical Failure:

Although not a program requirement, devices that deviated outside the Philco-Ford specified minimum and/or maximum limit for any parameter, were classified as 'deviates' or degradation failures. These devices were not removed from subsequent testing unless they further degraded into the catastrophic category.

6.1.3. Seal Failure:

A third type of failure was a hermetic seal reject. Devices from the thermal shock and lead fatigue test procedures were helium fine and fluorocarbon gross leak tested. Devices with leak rates $>1 \times 10^{-8}$ ATM cm^3/sec or that emanated one or more bubbles were classified as failures for fine or gross leak tests respectively.

6.1.4. Mechanical Failure:

This category was primarily for the lead integrity or fatigue stress test. A particular device was retired from test when all leads were mechanically separated due to the bending stress and strain.

A second type of failure that is considered within this category is package breakage and/or deformation due to accident or inadequate protection by the fixture used to retain the device during acceleration stress tests.

TABLE 6.1 - SUMMARY OF FAILURE CRITERIA

Type Failure	Test	Failure Criteria	Device Disposition
Electrical Catastrophic	Const.Accel.	Short or open	Remove
	All others	Leakage 100 x Initial limit or Short or open	Remove
Electrical Degradation	All	Any Parameter Outside Initial limit	Continue
Seal	Thermal Shock Lead Fatigue	Helium leak rate $>1 \times 10^{-8}$ atm cm^3/sec.-Fluorocarbon Gross Leak Rate-one bubble	Continue
Lead Integrity	Lead Fatigue	All leads off	Remove

6.2 TYPES OF FAILURES ANALYZED

The catastrophic electrical failures were the only devices analyzed. Also a selected portion of the detected leakers were subjected to the penetrant dye test for verification. All analyses were conducted in accordance with Philco-Ford established failure analysis procedure.

6.2.1. Failure Analysis Procedure:

The first step in failure analysis is to study the electrical test data of the device. This usually suggests one or more probable failure modes. The analyst then performs sufficient further electrical tests to verify conclusively that the failure exists and what the probable modes are.

The device is next subjected to helium leak testing and radiographic inspection to determine if leaks, inclusion of foreign particles in the package, or open or shorted internal lead wires are contributing factors. Negative test results do not indicate non-existence of the above factors; however, such results do indicate that if the factors exist, they are beyond the resolution of the best available test equipment.

A gross package leak, which is not detectable by the helium method, can contribute to a device failure. The bubble test may be used if a leak of this magnitude is suspected.

A final check is the use of a highly penetrant dye.

Shorted or open internal leads may not be detected during radiographic inspection because they may be hidden behind other elements, or the separation of an open lead may not be sufficient to be resolved on the radiograph. A large thin foreign particle which could short a device may escape detection because of its transparency to the impinging radiation. The use of aluminum internal lead wires also limits the usefulness of radiographic inspection on certain device families.

Each failed device is then opened and subjected to microscopic examination and electrical measurement using probe techniques to determine the cause or causes for failure. When necessary, interconnecting metalizations are scratched open and component measurements made with probes. Furthermore sophisticated techniques such as preferential etching and staining are used as needed.

A complete failure analysis report (FAR) is issued for each device analyzed. This report includes the device history, the cause of failure, the procedure used in determining the cause of failure, the manufacturing process believed responsible for the failure, photographs and, where possible, the mechanism responsible for the failure.

SECTION VII

7.0. DESCRIPTION OF ELECTRICAL TEST CHARACTERISTICS AND DATA LOGGING FORMAT

7.1. SYMBOL DESCRIPTION

7.1.1. Functional Symbols:

V_{CH} high Vcc used for forward input diode current tests

V_{CL} low Vcc for saturation and high output level tests

V_{IH} input high threshold voltage (enable)

V_{IL} input low threshold voltage (disable)

V_F low voltage for forward input current tests

V_x threshold voltage for extender input current tests

V_{CPTH} clock threshold voltage for transfer (enable)

V_{ILS} direct set and clear low threshold voltage

V_{OL} output low voltage (at I_{OL})

V_{OH} output high voltage (at I_{OH})

V_{FD} forward diode drop for extender tests

I_{OH} output high current (to loads)

I_{OL} output low current (from loads)

I_{FD} forward diode current for extender

I_F forward input diode current (1 unit load)

I_{FCP} forward clock input diode current (2 unit loads)

I_{FS} forward set and clear input diode current (3/4 unit load)

I_{CEX} output transistor collector leakage current (at V_{CEX})

I_{SC} short circuit output current to ground, with inputs low

C_{Pn} clock pin pulsed from V_{OH} to specific level

I_{FSI} forward set and clear input diode current (2 unit loads)

V_{cc} supply voltage

V_{LL} a d-c voltage low enough that only leakage currents flow from the supply terminal. It is used for leakage test on Gates, Type D Flip Flops, Adders, and Half-Adders.

V_{BOT} the maximum input voltage encountered in a milliwatt system.

V_{IN} minimum high level encountered in a milliwatt system

V_{ON} maximum voltage required to turn on a transistor

V_{OFF} the maximum voltage which may be applied to an input terminal without turning on the transistor.

V_{OUT} the output voltage when V_{on} is applied to the input pin

V_{CE} the output voltage when V_{in} is applied to the input pin

I_{A4} current available from an output terminal with a fan-out of 4

I_{A3} current available from an output terminal with a fan-out of 3

I_{AB} current available from the output terminal of a buffer

I_{AM} maximum current available from the output terminal of a Gate or a Dual Gate

I_{IN} the current drawn from the V_{IN} supply by one input of a gate with a fan-in of two or more

$.8I_{IN}$ the current drawn from the V_{IN} supply by the input of a simple milliwatt inverter (FAN-IN = 1)

$1.8I_{IN}$ the current drawn from the V_{IN} supply by a Type D Flip-Flop clock pulse input terminal, Pin 1

$2I_{IN}$ the current drawn from the V_{IN} supply by a buffer element input terminal

I_{CEX} collector current of Gate Expander when V_{OFF} is applied to the input pins and V_{IN} applied to the output pin

I_L leakage current

V_{RL} voltage obtained when the specified resistor is connected to V_{CC}. This resistor represents the lowest node resistor of milliwatt circuit

V_{RH} voltage obtained when the specified resistor is connected to Vcc. This resistor represents the highest node resistor of milliwatt circuit.

7.1.2. Non-Functional Symbols:

V_{MAX} maximum rated Vcc voltage

I_{MAX} maximum rated Vcc current (at V_{MAX})

V_{PD} Vcc voltage for power dissipation test

I_{PD} Vcc current (at V_{PD})

V_R input diode reverse voltage for leakage test

I_R input diode reverse leakage (at V_R)

V_{CEX} output transistor V_{CE} for leakage test

I_{CE} output transistor I_{CE} for LV_{CE} test

LV_{CE} output transistor latch voltage

7.1.3. Subscripts:

O	output
I	input
R	Reverse
F	forward
L	low logic level or supply
H	high logic level or supply

7.2 DATA LOGGING FORMAT

An example of the data logging format is given in Table 7.1. The collated listing has each device's readings arranged such that the initial reading is at the top followed by each subsequent stress step's reading. Table 7.2 gives an example of the header and data cards.

7.2.1. Characteristic Values:

All voltage measurements are recorded in volts times 10^X, where x is a negative integer. All current measurements are recorded in amperes times 10^X, where x is a negative integer. The first four digits of each parameter measurement indicates the numerical value of the measurement and the fifth digit indicates the absolute value of the negative exponent. The power 10 and the negative sign of the exponent are not punched. The decimal of the numerical value, as punched, is always immediately after the fourth digit; hence, the voltage measurement:

25453 indicates 2545. x 10^{-3} volts, or 2.545 volts.

The current measurement: 54235 indicates 5423. x 10^{-5} amperes, or .05423 amperes, or 54.23 ma.

In the event that a device parameter does not meet the imposed specification, this will be indicated on the punch card by a special character punch in the column immediately preceding the exponent for that particular parameter.

7.2.2. Column 80 Pass Reject Punch:

If any parameter on any card is rejected to the imposed specification limits, an '&' symbol will be punched in column 80 of the card containing the rejected parameter. If no rejects occur on the card, column 80 will be punched '0'.

7.2.3. Other Symbols:

If any parameter does not meet the imposed specification limit it is indicated by a symbol that replaces the fourth digit in the data column which reduces the number of significant figures to three. These symbols are given in Table 7.3.

TABLE 7.3 - PARAMETER REJECT SYMBOLS

Parameter Reject	Symbol
High Reject	'&'
Low Reject	'-'
Over Range Reject	'#' or '$'
Polarity Reject	'@' or '*'

Device Type	Spec. Rev. No.	Test Date Code: Month	Day	Year	Test No. or Lot No.	Parameter Test Temp °C	Test Duration Hour Code	Test Code
U7T25	0	NOV 10 78	17	78	E3012	025	000 13C 40C 10K	R1

			IB2	IB3	IB4	IB6	IB7	IB8	VOA2	VOA3	VOA4	VOB6	
	1	A											← (Parameter Name)*
MIN	1	B	--	--	--	--	--	--	--	--	--	--	← (Min. Spec. Limit)*
MAX	1	C	15207	15207	15207	15207	15207	15207	30004	30004	30004	30004	← (Max. Spec. Limit)*
	1	D	AMP	AMP	AMP	AMP	AMP	AMP	VOLT	VOLT	VOLT	VOLT	← (Unit of Measurement)*
000	R1	1	015	13107	12967	12567	12677	13077	13097	20364	19444	20594	22394	0
13C	R1	1	015	12897	12757	12357	12467	12867	12877	20834	19964	21104	22714	0
40C	R1	1	015	12967	12827	12427	12537	12937	12947	20614	19764	20944	22574	0
10K	RC	1	015	12957	12817	12417	12527	12927	12937	20534	19694	20874	22524	0
000	R1	1	016	11367	11347	11037	11077	11067	11437	18924	18014	19324	19614	0
13C	R1	1	016	11197	11187	10887	10927	10917	11287	19184	18234	19554	19874	0
40C	R1	1	016	11257	11237	10937	10977	10967	11327	19054	18154	19464	19784	0
10K	RC	1	016	11247	11227	10927	10967	10947	11317	19014	18104	19394	19694	0
000	R1	1	018	13727	13607	13367	13577	13777	13857	19424	18514	19914	20774	0
13C	R1	1	018	13527	13417	13177	13407	13587	13667	19594	18734	20154	20974	0
40C	R1	1	018	13617	13497	13257	13477	13657	13747	19494	18604	20044	20834	0
10K	RC	1	018	13587	13467	13237	13447	13637	13717	19464	18574	20004	20864	0

*Information from Header Cards - See Figure 7.2

- Duration of Test (Hour Code)
- Test Code
- Data Card No.(10 parameters/card)
- Device Serial No.
- Last col. of every parameter reading is exponent multiplier Ex: $11595 = 1159.x10^{-5} = 0.01159$
- Next to last col. of every parameter reading is individual parameter reject col. If the parameter fails the spec, this. col. is punched with an alphabetic character
- Reject Indication Col. (& indicate Reject, 0 indicates all parameters meet specs.

Figure 7.1

EXAMPLE OF COLLATED TEST DATA

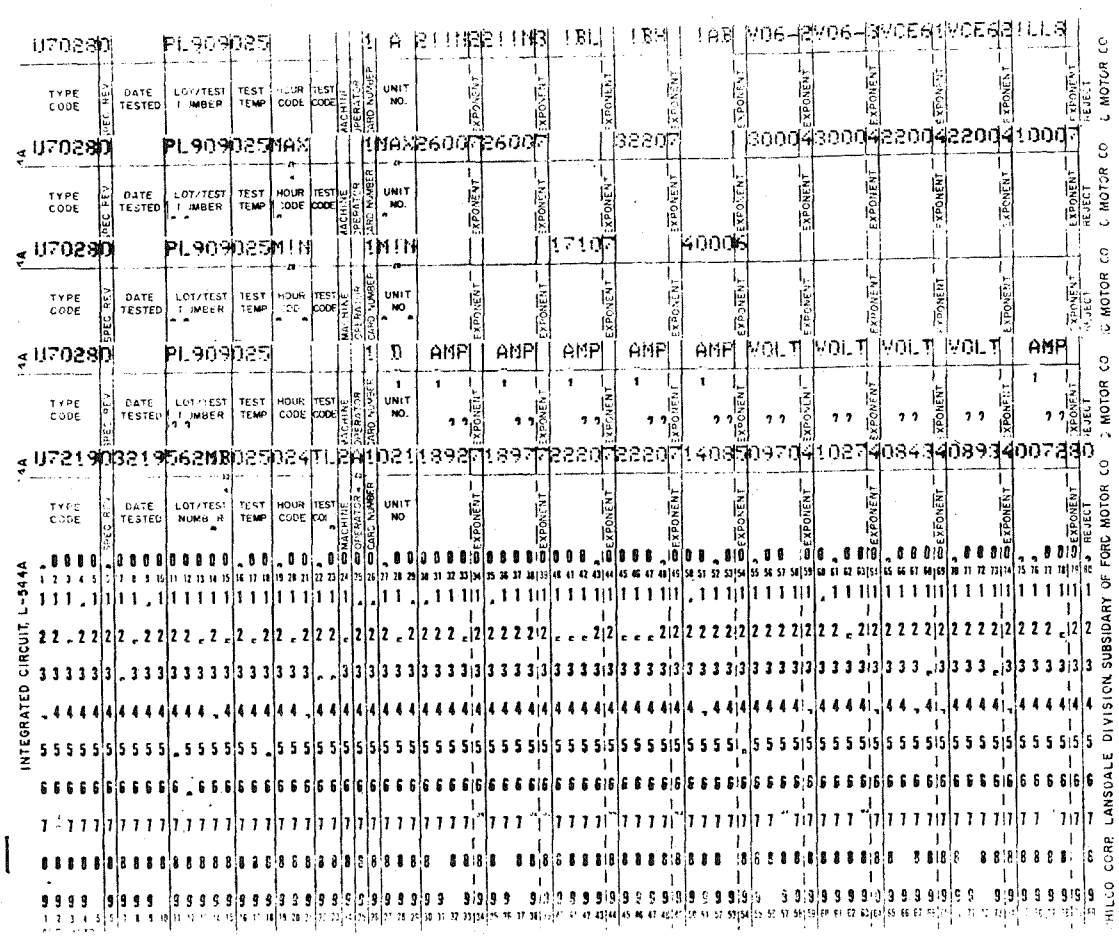


Figure 7.2 Examples of Header and Data Cards.

SECTION VIII

TEST EQUIPMENT & PROCEDURE

8.0. The following paragraphs describe the equipment and procedure used for the step stress testing and the hermeticity and electrical characterization tests.

8.1. HERMETICITY TESTING

8.1.1. Purpose:

The purpose of this test is to determine the seal hermeticity of microelectronic packages with cavities that are either evacuated or contain a gas. It is used to assess the reliability of the seal in preventing the admission of contaminants to the cavity that would degrade device performance.

8.1.2. Equipment:

The equipment required is as follows:

a. Helium fine leak requires a suitable vacuum-pressure bomb chamber and pumps, source of helium, device holding leak-test chambers, and a mass spectrometer type leak detector with a minimum He leak rate sensitivity of 10^{-9} atm cm^3/sec.

b. Fluorocarbon (Freon) gross leak, Part B, requires a vacuum-pressure bombing chamber and pumps, pyrex glass dish, stainless steel mesh, hot plate, temperature controller, magnifier (3X min), and sources of Freon 113 and FC 43 fluorocarbons.

c. Fluorocarbon (Freon) gross leak, Part A, requires all of the above equipment except the bombing chamber and pumps.

The 'A' test is used to detect severe package leaks ($>10^{-3}$atm cm^3/sec) such as cracks and seal fractures that were missed by visual inspection.

The 'B' test overlaps the 'A' test as well as the upper limit of the helium leak test (10^{-5} atm cm^3/sec).

d. Penetrant dye gross leak requires a vacuum-pressure bomb chamber and pumps, Spotcheck* penetrant dye, and dye detector. This test is used to verify questionable leakers.

* Trademark Magaflux Corporation

8.1.3. Procedure:

a. Helium leak test

1. Place devices in bomb chamber and close cover.

2. Turn on vacuum pump to evacuate air.

3. Turn off vacuum pump.

4. Open Helium valve and set pressure to 90 psig for 3 hours.

5. Turn off helium valve and bleed chamber to atmosphere pressure.

6. Open cover and remove devices.

7. "Air wash" devices to remove surface occluded helium.

8. Within 30 minutes after completion of step 4, place one device in each leak test chamber.

9. Test each device individually for traces of helium as determined by the mass spectrometer type leak detector.

10. Record measured leak rates greater than 1×10^{-8} atm cm^3/sec.

11. Repeat steps 8 - 10 for balance of devices.

b. Fluorocarbon gross leak (Part A).

1. Check that stainless steel mesh is 1/4 inch from dish bottom.

2. Check that FC-43 in pyrex dish is at 100°C and that its level is 2-1/2" min.

3. Place devices with lid down individually into FC-43 and on stainless steel mesh.

4. Using 10X microscope, observe whether or not a bubble or bubbles emanate from the device.

5. Record whether or not bubbles emanate and location of emanation.

6. Repeat steps 2 - 5 for each device.

c. Fluorocarbon Gross Leak (Part B).

1. Place devices in beaker and into vacuum-pressure chamber.

2. Evacuate to 1 mm Hg maximum and maintain this vacuum for one hour.

3. Without breaking vacuum, draw Freon 113 into the chamber to cover the devices.

4. Pressurize vessel to 90 psig with nitrogen and maintain pressure for 3 hours.

5. Bleed chamber to atmosphere pressure and remove cover.

6. Remove beaker with Freon 113 covered devices.

7. Check that stainless steel mesh is 1/4 inch from dish bottom.

8. Check that FC-43 in pyrex dish is at 100°C and that its level is 2-1/2" min.

9. Remove one device from beaker and allow to dry 3 minutes.

10. Place devices with lid down individually into FC-43 and on stainless steel mesh.

11. Using 10X microscope observe whether or not a bubble or bubbles emanate from the device.

12. Record whether or not bubbles emanated and location of emanation.

13. Repeat steps 8 - 12 for each device.

d. Penetrant Dye Gross Leak (Used to verify questionable leakers)

1. Place devices in beaker.

2. Evacuate to 1 mm Hg maximum and maintain this vacuum for one hour.

3. Without breaking vacuum, draw penetrant dye into the chamber to cover the devices.

4. Pressurize vessel to 90 psig with nitrogen and maintain pressure for 12 hours minimum.

5. Bleed chamber to atmosphere pressure and remove cover.

6. Remove beaker containing devices, and decant excess penetrant dye into storage vessel.

7. Wash penetrant dye from devices with acetone and dry.

8. Open each device and examine for traces of dye using 10X microscope.

9. Spray each device with penetrant dye detector.

10. Reinspect each device for traces of dye.

11. Record whether or not dye is present in the internal cavity of each device.

8.2. ELECTRICAL TEST

8.2.1. Purpose:

The purpose of the electrical test after stress is to provide a means to determine whether or not an applied environmental stress caused changes in device characteristics that would either impair its performance or cause it to become non-functional.

8.2.2. Equipment:

The equipment used to electrically test all the device types is called the "Philco Evaluation and Logging Tester" or "PELT".

This Quality and Reliability Microcircuit tester is a paper tape programmed unit providing test results onto cards or typewriter and tape.

It performs D.C. tests on microcircuit devices having up to sixteen leads and also provides pulse levels for clocking or setting the device under test to its required level prior to making the test measurement.

A perforated tape block reader is used to program the tests. Microcircuit elements decode the tape information which set up the test circuit.

Automatic, semi-automatic, and manual modes of operation are provided for all phases of engineering studies. An engineering panel, made available for experimental testing, is presented as a matrix with the module pins as the abscissa and the input-output conditions as the ordinate. In this mode, one may monitor and adjust bias levels or monitor the input-output pins of a device under test. A special operating mode is provided to inhibit further testing when a test reject occurs. When this occurs, the operator may choose to examine the test result or command the tester to proceed on.

Eighteen pre-set voltage levels and eight pre-set current levels are available for biasing. Two current readout circuits are provided to measure the device current when forcing a voltage.

8.2.3. Procedure:

a. Obtain programming tape for particular type to be tested and install on Tape Reader.

b. Obtain standards of the same type to be tested to check machine calibration.

c. Read one standard by inserting into test socket on PELT and depressing start pedal.

d. After PELT completes testing and recording, proceed to test other standards.

e. Compare standard readings to original data for these devices and, if within tolerance, proceed to test devices or, if not within tolerance, notify technician.

f. Read and record on 80 column data punch cards, all required parameters for each device.

g. Submit completed test cards to be collated and have data printed out.

h. From print-outs, earmark all readings of devices that were indicated by machine to be outside of one or more initial limits.

i. Verify all leakage tests.

j. Check other device readings to determine if any are unreasonable and need verification.

k. After completion of verification procedure, date and stamp data runoff as "verified".

8.3. HIGH TEMPERATURE STORAGE

8.3.1. Purpose:

The high temperature storage test is used to determine the effect of elevated temperatures, without electrical stress applied, on microelectronic devices. It also can be used as a preconditioning treatment during final processing of devices.

8.3.2. Equipment:

The equipment consists of a controlled temperature chamber capable of attaining and maintaining the specified temperature within $\pm$1%. Containers or trays are provided to hold the devices.

8.3.3. Temperature Control:

The temperature chamber is provided with a thermocouple, and associated circuits, that controls the chamber temperature by switching the input power to the resistance heaters. In addition, a limit switch is provided that prevents the temperature from exceeding a limit 5% above the required chamber temperature. This limit switch sounds an alarm and, if unheeded, cuts all power to the heaters. Manual reset is necessary. The temperature is also monitored by another thermocouple which drives a recording potentiometer. Readings are recorded every two (2) minutes.

Test temperatures of 75, 125, 175, 225, 250, 275, 300, 325, 350, 375, 400, 425, 450 and 475°C were used for the program.

8.3.4. Test Procedure:

a. Read and record specified electrical parameter for each device.

b. Check chamber temperature and adjust and calibrate if necessary.

c. Place devices into holding trays or containers capable of withstanding the chamber temperature.

d. Place tray or container into chamber and record date and time.

e. After the required time of 24 hours, remove tray or container containing devices and let cool to room temperature.

f. Read and record specified electrical parameters for each device.

g. Repeat steps 'b' through 'f' for each test temperature required.

8.4. STEP STRESS OPERATING LIFE

8.4.1. Purpose:

The purpose of the Step Stress Operating Life test is to determine a representative failure rate or demonstrate the reliability of a device when subjected to a specified level of power at a given temperature.

8.4.2. Equipment:

The equipment consists of suitable test boards for the particular device, a controlled temperature chamber and required power supplies.

8.4.3. Circuits and Conditions:

The actual operating life circuits are given in Figures 8.1 to 8.8. Note that series resistances should be sufficiently greater than the impedance of the device to make it possible to control and maintain constant device current, regardless of fluctuations in device impedance.

All device types were subject to stress levels of from 200 mW to 1000 mW at 125°C in 100 mW steps. The dissipation is determined from $P = I_{RL}V_1$ for all types except the PL9909, PL9910 and PL9913. For the PL9909 and PL9910 circuits it can be shown that the device dissipation is approximately:

$$P_D = I_E V_{CE} + I_{RL} (V_{CC}-V_{EE}-I_E R_E-V_{CE})$$

For the PL9913 the dissipation is:

$$P_D = V_1 I_{RL} + V_2 I_2$$

Figure 8.1 - OPERATING LIFE TEST CIRCUIT - PL9932 (u7330)

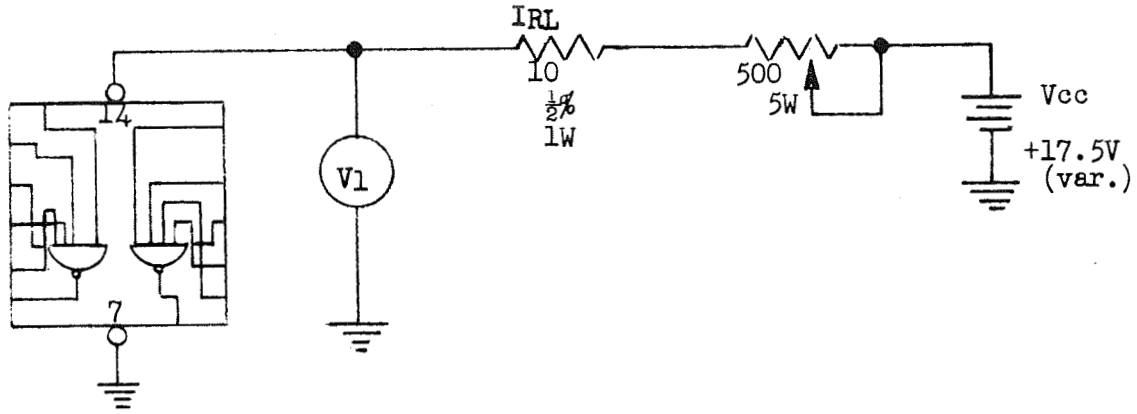


Figure 8.2 - OPERATING LIFE TEST CIRCUIT - PL9945 (u7332)

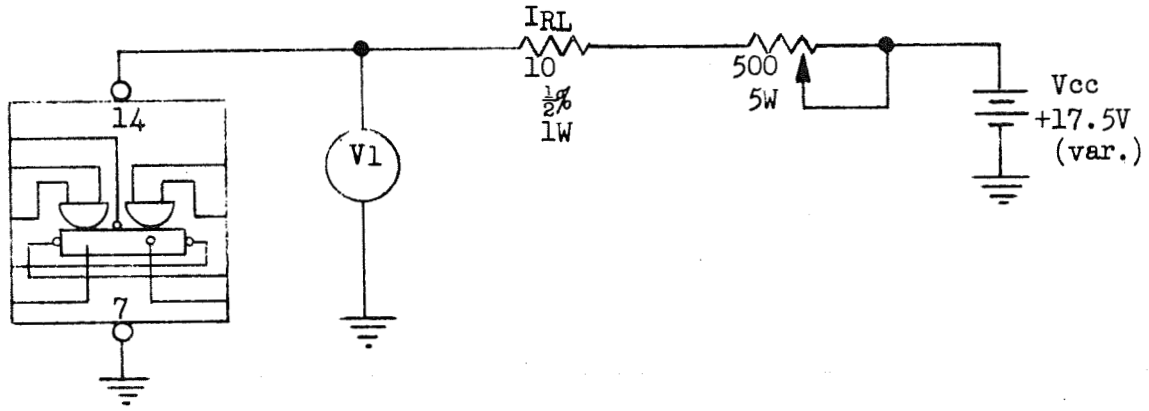


Figure 8.3 - OPERATING LIFE TEST CIRCUIT - PL9962 (u7374)

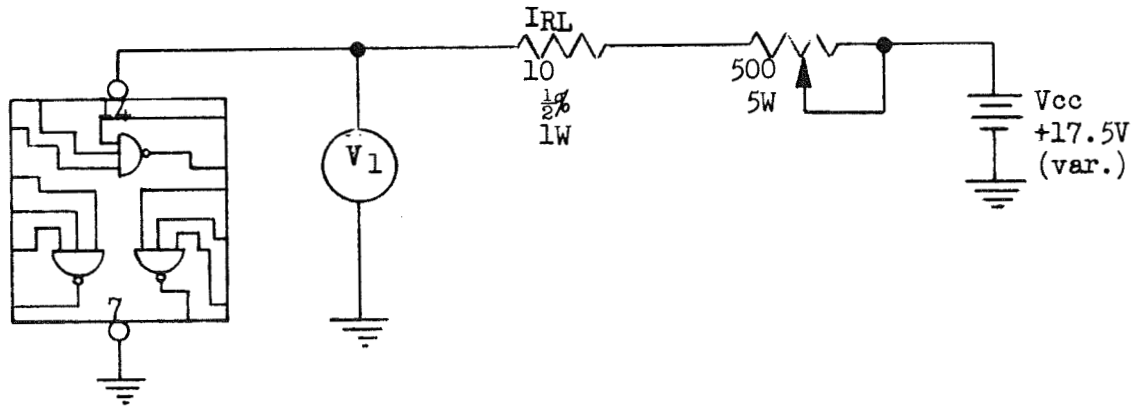


Figure 8.4 - OPERATING LIFE TEST CIRCUIT - PL9909 (μ7219)

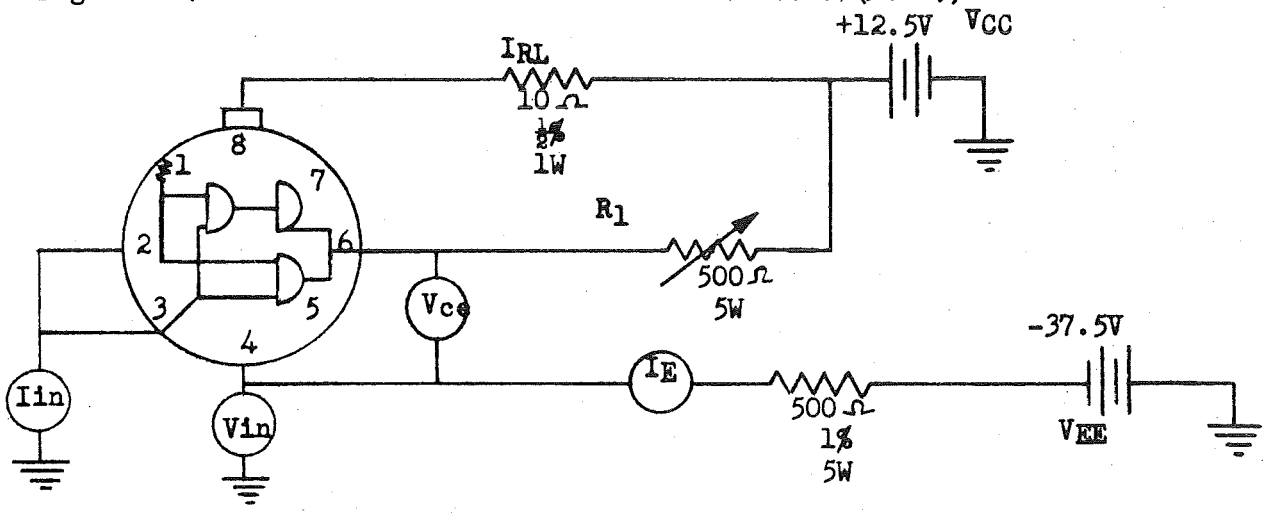


Figure 8.5 - OPERATING LIFE TEST CIRCUIT - PL9910 (μ7220)

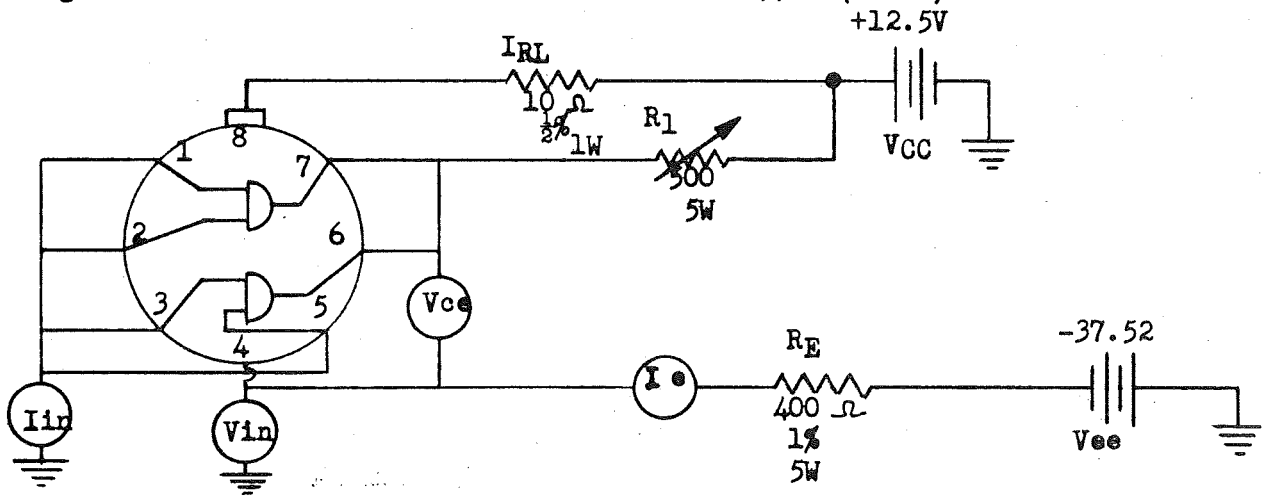


Figure 8.6 - OPERATING LIFE TEST CIRCUIT - PL9913 (μ7032)

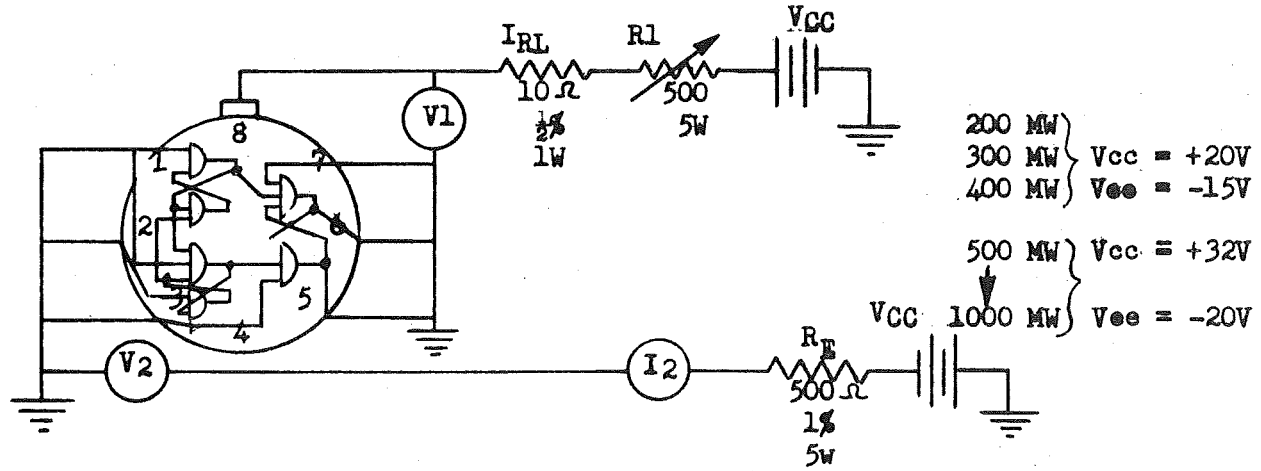


Figure 8.7 - OPERATING LIFE TEST CIRCUIT - PD9624 (u7938)

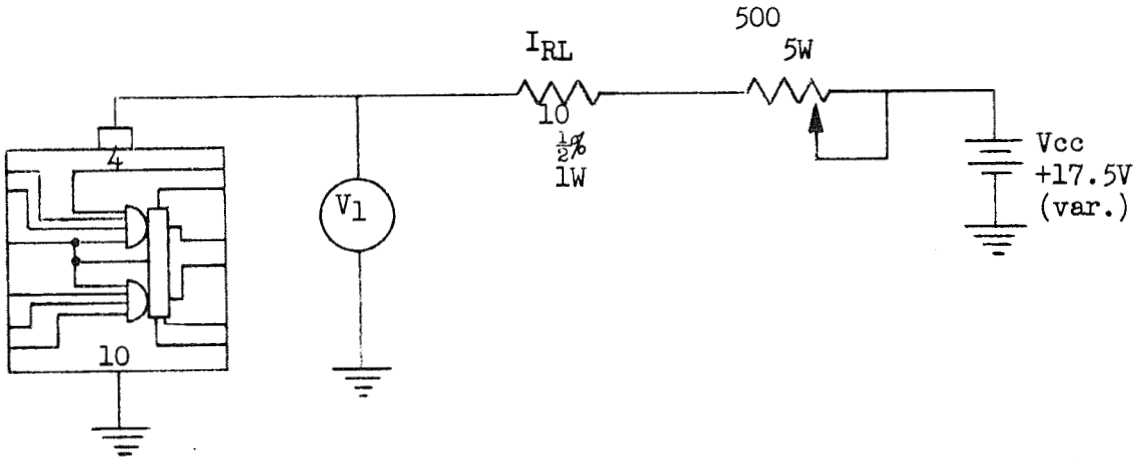
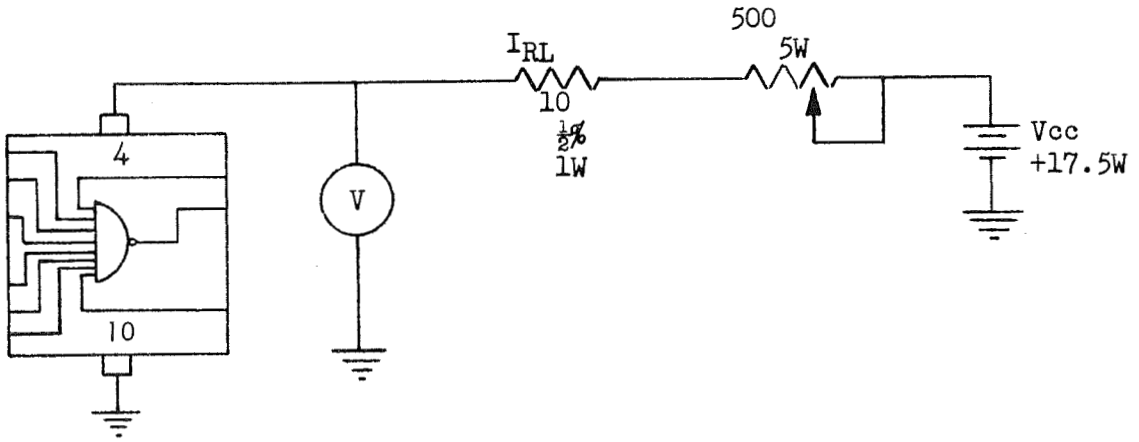


Figure 8.8 - OPERATING LIFE TEST CIRCUIT - PD9625 (u7942)



8.4.4. Procedure:

a. Read and record specified electrical parameters.

b. Load devices into circuit test boards.

c. Check that power supplies are at required supply voltages (V_{cc} and V_{ee})

d. Place test boards containing devices in 125°C test chamber and seat into power sockets.

e. Allow devices to stabilize at 125°C prior to applying power.

f. Adjust V_{ce} and/or V_I and I_E and/or I_{RL} to give required power level.

g. Maintain power level for 24 hours.

h. Turn off power, remove test boards containing devices from chamber and allow to cool.

i. Read and record specified electrical parameters.

j. Repeat steps 'b' through 'i' for each power level.

8.5 REVERSE BIAS

8.5.1. Purpose:

The purpose of the reverse or back bias test is to determine the devices' capability of withstanding its maximum rated voltage at elevated temperature. This electrical stressing serves as an indication of the stability of the devices' surface and bulk characteristics including the surface problems of inversion and channeling.

8.5.2. Equipment:

The equipment consists of suitable test boards for the particular device, a controlled temperature chamber and required power supply.

8.5.3. Circuits and Conditions:

The actual back bias circuits are given in figures 8.9 - 8.16. The bias is applied such that the maximum number of junctions are reverse biased. A 10 Kilohm resistor is placed in series with the

Figure 8.9 - REVERSE BIAS LIFE TEST CIRCUIT - PL 9932 (μ7330)

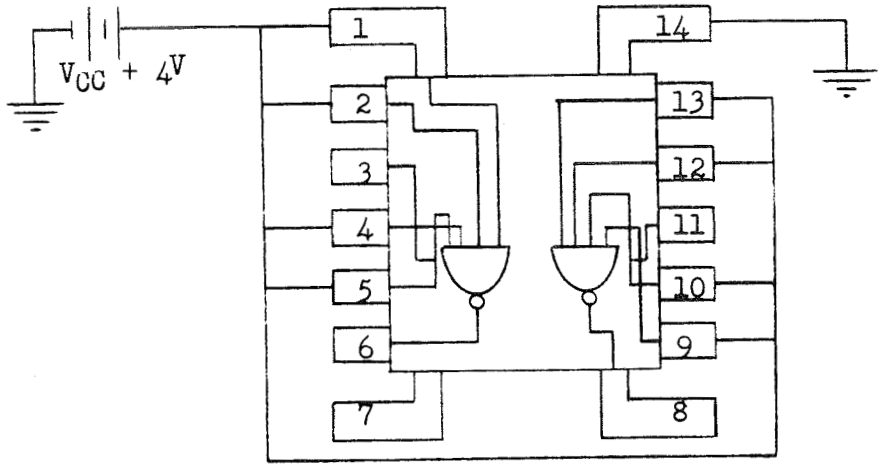


Figure 8.10 - REVERSE BIAS LIFE TEST CIRCUIT - PL9945 (μ7332)

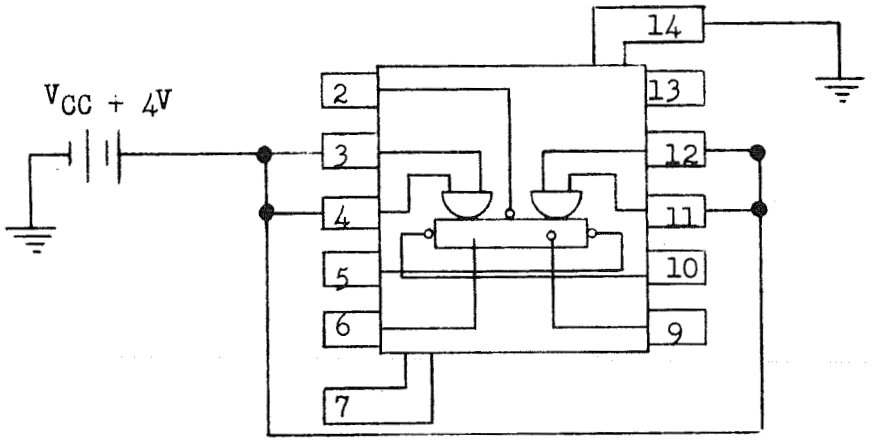


Figure 8.11 - REVERSE BIAS LIFE TEST CIRCUIT - PL9962 (μ7334)

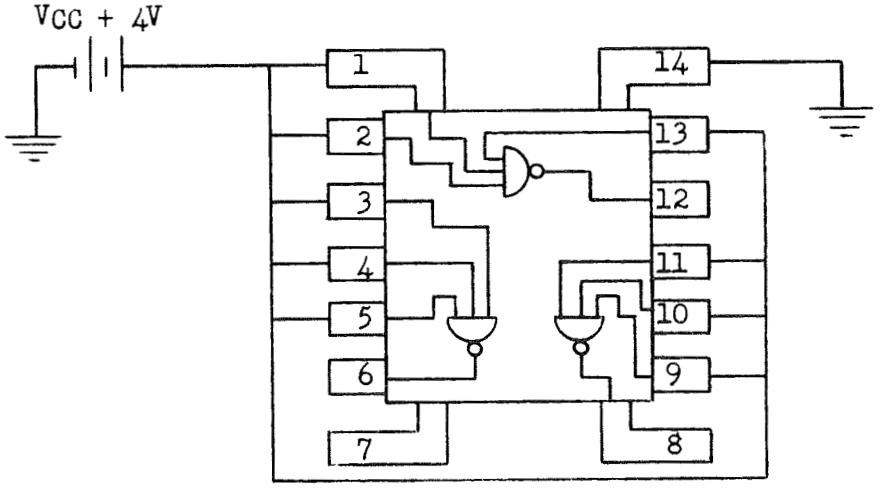


Figure 8.12 - REVERSE BIAS LIFE TEST CIRCUIT - PL909 (μ7219)

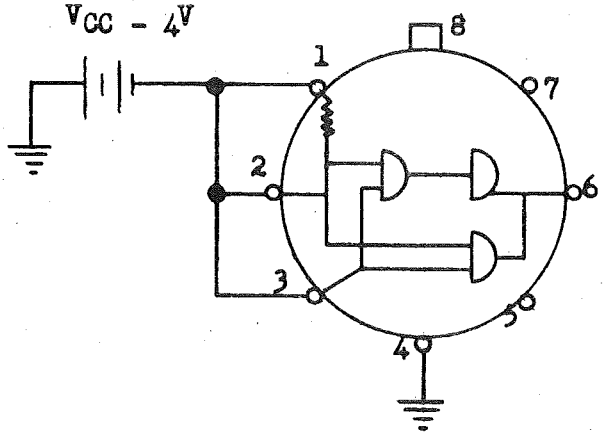


Figure 8.13 - REVERSE BIAS LIFE TEST CIRCUIT - PL9910 (μ7220)

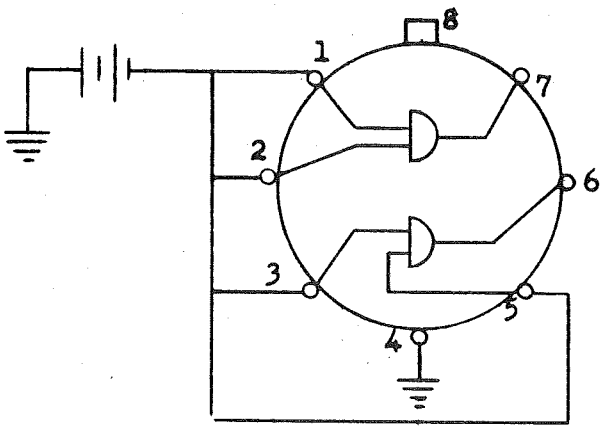


Figure 8.14 - REVERSE BIAS LIFE TEST CIRCUIT - PL9913 (μ7032)

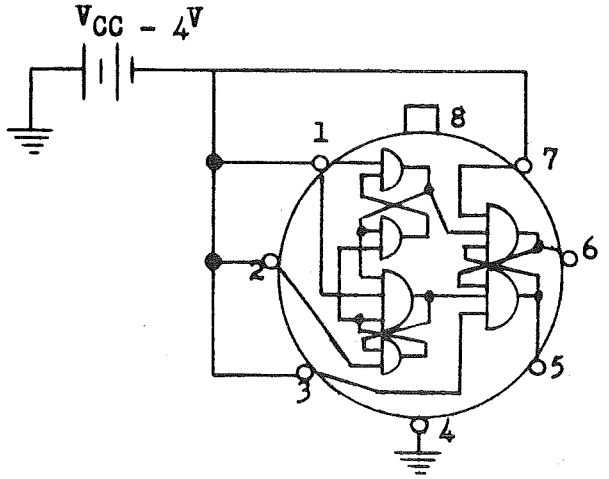


Figure 8.15 - REVERSE BIAS LIFE TEST CIRCUIT - PD9624 (μ7938)

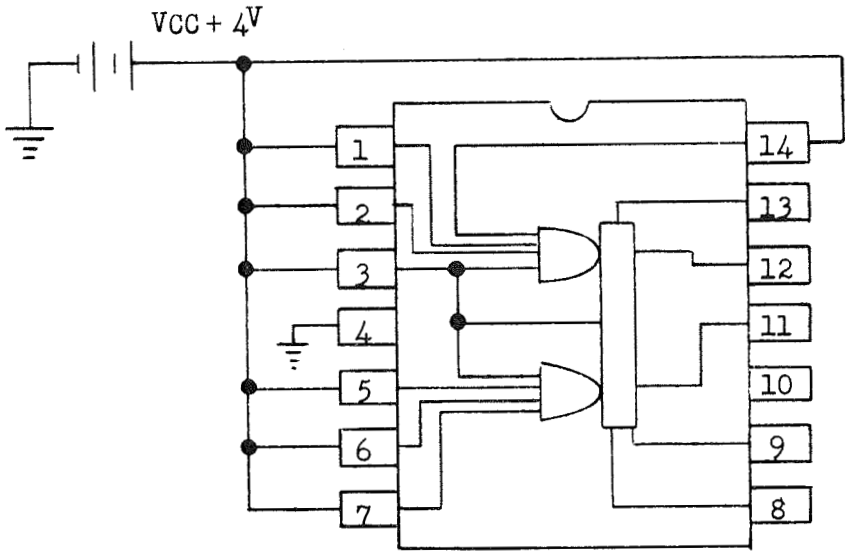
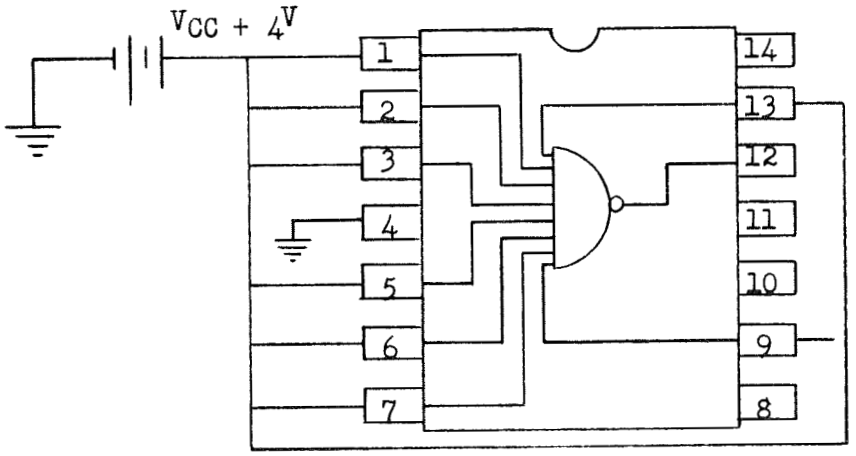


Figure 8.16 - REVERSE BIAS LIFE TEST CIRCUIT - PD9625 (μ7942)



power supply to limit the current in the event that a junction breakdown or other short develops. The amount of power that is dissipated in the normal device is negligible but can increase rapidly should a defect appear. The series resistor prevents this increase and avoids other circuit damage, such as effects of the power dissipation type of test, that can mask the actual reverse bias failure mode.

All devices were tested at the same reverse bias conditions at temperatures of 75, 100, 125, 150°C for a total of 800 hours (200 hrs. per step).

8.5.4. Procedure:

a. Read and record specified electrical parameters.

b. Load devices into circuit test boards.

c. Check that power supply is set at required supply voltage.

d. Set and stabilize chamber temperature.

e. Place test boards containing devices in test chamber and seat into power socket.

f. Allow device temperature to stabilize prior to applying bias.

g. Adjust bias voltage, if necessary.

h. Maintain conditions for 200 hours.

i. Cool devices and turn off power.

j. Remove test boards from chamber.

k. Read and record specified electrical parameter.

l. Repeat steps 'b' through 'k' for each temperature.

8.6. CONSTANT ACCELERATION

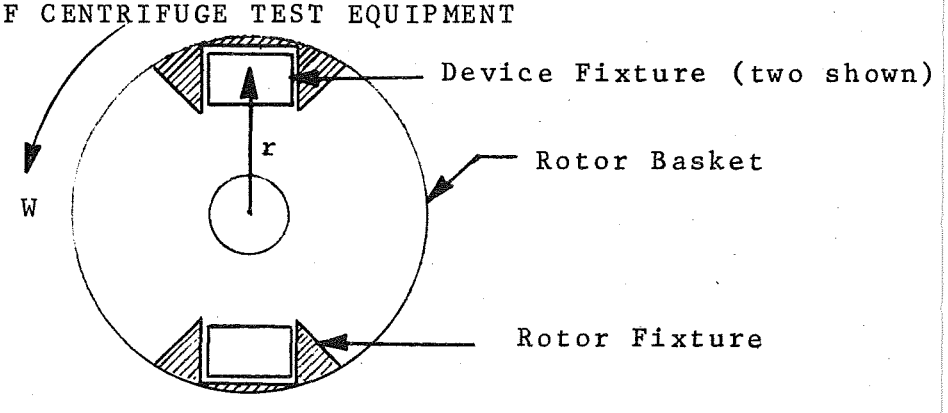
8.6.1. Purpose:

The constant acceleration test is used to determine the effects of centrifugal forces on microelectronic devices. It is used to detect structural and mechanical weaknesses such as those that occur in die bond, wire bonds and cover seals that are not easily discernable by other means. It is also used as a high stress test to determine mechanical limits of packages and device construction methods and interconnections.

8.6.2. Equipment:

The equipment consists of a centrifuge capable of applying the specified centrifugal force to the device in a suitable restraining fixture and rotor. A sketch of the equipment's pertinent details is given in Figure 8.17.

Fig.8.17 - OUTLINE OF CENTRIFUGE TEST EQUIPMENT



8.6.3. G - Level

The acceleration is directly proportional to the square of the angular velocity and the radius of the circular path traversed by the device under stress. This is expressed as:

$$a = w^2 r$$

Where: a = Acceleration in ft/sec^2
w = Angular velocity in radians/sec
r = Radius of circular path in feet.

Since centrifuge speeds are normally specified in the number of revolutions in a given time, such as revolution/min., it can be readily shown that the expression (1) becomes:

$$a = 9.138 \times 10^{-4} w^2 r$$

Where: w = Angular velocity in rpm
r = Radius in inches

Using 'g', the acceleration of gravity as 32.174 ft/sec^2 it is convenient to write the number of 'G's' as:

$$G = 2.841 \times 10^{-5} w^2 r$$

Since the radius is fixed by the rotor diameter and device fixtures, the angular velocity is the variable used to set the

required G level. Thus finally:

$$w = 10^2 \left[\frac{3.520G}{r}\right]^{1/2}$$

Where: w is in rev/min and
r is in inches

or:

$$w = 10^2 \left[\frac{8.941G}{r}\right]^{1/2}$$

Where: r is in cm

For the program, the rpm given in table 8.18 were used to achieve the specified G level at the center of the device in the YI plane

TABLE 8.18 - r.p.m. Required for Given "G" Level

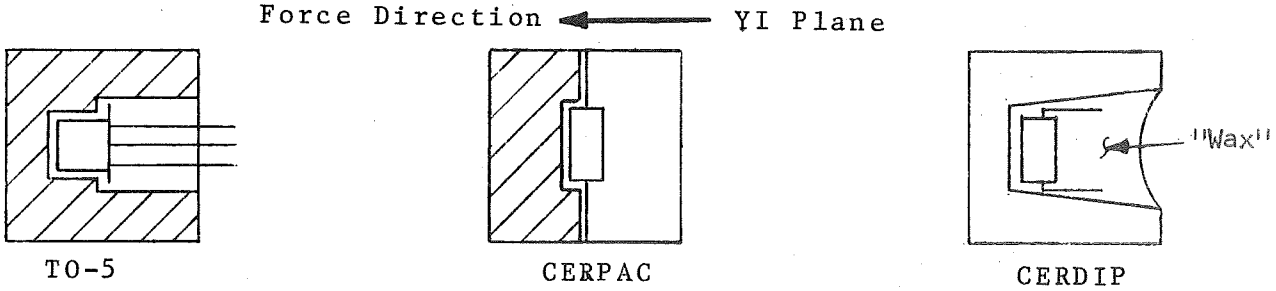
Level	Cerpac r = 3.25"	TO-5 r = 3"	Cerdip r = 2.83"
20,000 G's	14,750	15,250	15,750
40,000 G's	20,750	21,750	22,250
60,000 G's	25,550	26,500	27,500
80,000 G's	29,500	30,500	31,500
100,000 G's	31,750	34,250	35,250

8.6.4. Test Procedure:

a. Read and record specified electrical parameters for each device.

b. Load devices into holding fixtures for the particular type package as given in Figure 8.19.

Figure 8.19 - OUTLINES OF CENTRIFUGE DEVICE HOLDING FIXTURES



The Cerdip is 'waxed' into its fixture for the high 'G' levels to prevent package breakage. This is necessary due to the flat projection in the center of the package top that prevents both top end areas of the package from resting against the fixture bottom. Thus, the device is subjected to bending stresses and at higher acceleration this stress causes breakage at the projection end, or of the package at the end leads.

c. Orientate and load fixtures into centrifuge rotor for acceleration in Y1 plane.

d. Close centrifuge cover.

e. Set centrifuge control at rpm required for particular G level.

f. Start centrifuge and allow to reach the required rpm as indicated by calibrated gage.

g. Hold devices at required rpm for one (1) minute.

h. Turn off centrifuge and allow to coast to stop.

i. Open cover and unload fixtures from rotor.

j. Unload devices from fixtures.

k. Read and record specified electrical parameters for each device.

l. Repeat steps 'b' through 'k' for each 'G' level.

8.7. PNEUPACTOR MECHANICAL SHOCK

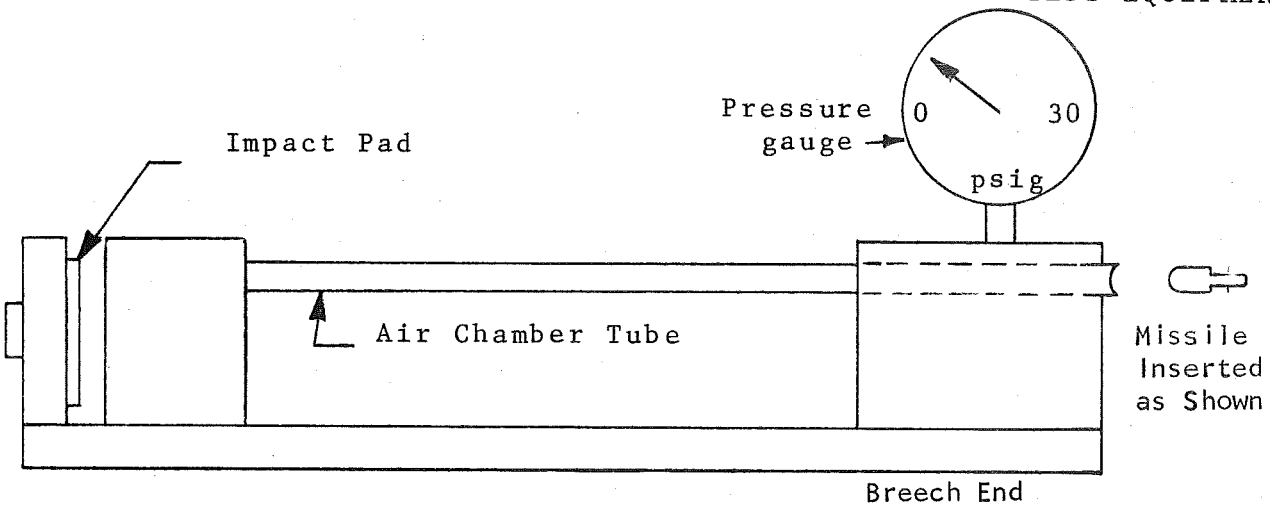
8.7.1. Purpose:

The mechanical shock test is used to determine the effects of short duration acceleration forces on the devices. These forces are similar to those experienced due to abrupt changes in motion or suddenly applied forces in field operation and transportation. The force is normally applied in the Y1 plane.

8.7.2. Equipment:

The equipment consists of a pneumatically accelerated missile (fixture), a guide tube, and an impact pad capable of transmitting high 'G' peak pulses of short duration to the body of the device without damage. A sketch, giving pertinent details of this equipment is given in Figure 8.20.

Figure 8.20 - OUTLINE OF PNEUPACTOR MECHANICAL SHOCK TEST EQUIPMENT



8.7.3. G Level:

The deceleration force applied to the device in the missile being accelerated varies directly as the final velocity of the missile just before impact and the impact pad resiliency, and inversely as the missile's weight. The duration of the force is an inverse function of the impact resiliency. Although the 'G' level and duration can be calculated from the known quantities described above, it is not commonly done since equipment is available that can easily determine the force and duration by actual measurement.

In order to perform the measurement, a force-measuring transducer with the same impact pad material is substituted for the impact pad at the same distance from the breech end. A charge amplifier is used to convert the transducer or accelerometer output of pCb/lb to lbs/volt. The peak voltage is then recorded on a peak reading voltmeter and the number of G's is calculated from F = ma as follows:

$$G = \frac{a}{g} = \frac{F}{m} \cdot \frac{1}{g} = F \cdot \frac{1}{W/g} \cdot \frac{1}{g} = \frac{F}{W}$$

Where: a = acceleration in ft/sec^2
g = acceleration due to gravity, 32.17 ft/sec^2
F = force in lbs.
m = mass in $lbs\text{-}sec^2/ft$
W = missle weight in lbs.

or: $G = \frac{F}{W \times .0022}$

Where: W = Missile weight in grams.

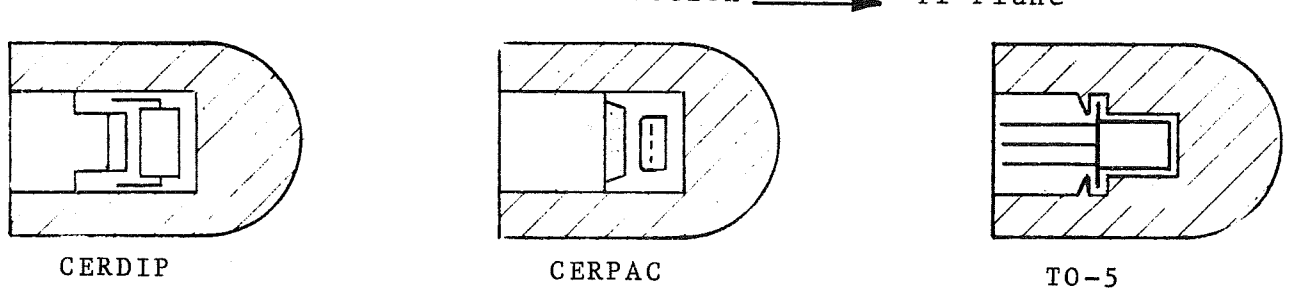
An oscilloscope is used instead of the voltmeter when the pulse duration must be known in addition to the peak acceleration.

8.7.4. Test Procedure:

a. Read and record specified electrical parameters for each device.

b. Load devices into holding fixtures (missiles) for the particular type package as given in Figure 8.21.

Figure 8.21 - Pneupactor Shock Test Fixtures



NOTE: Devices normally 'clamped' in fixture - shown suspended for clarity.

c. Calibrate equipment by using a "dummy" device in a missile.

d. Install accelerometer in place of the impact pad.

e. Place same type of impact pad material on accelerometer.

f. Weigh missile containing device and record in grams.

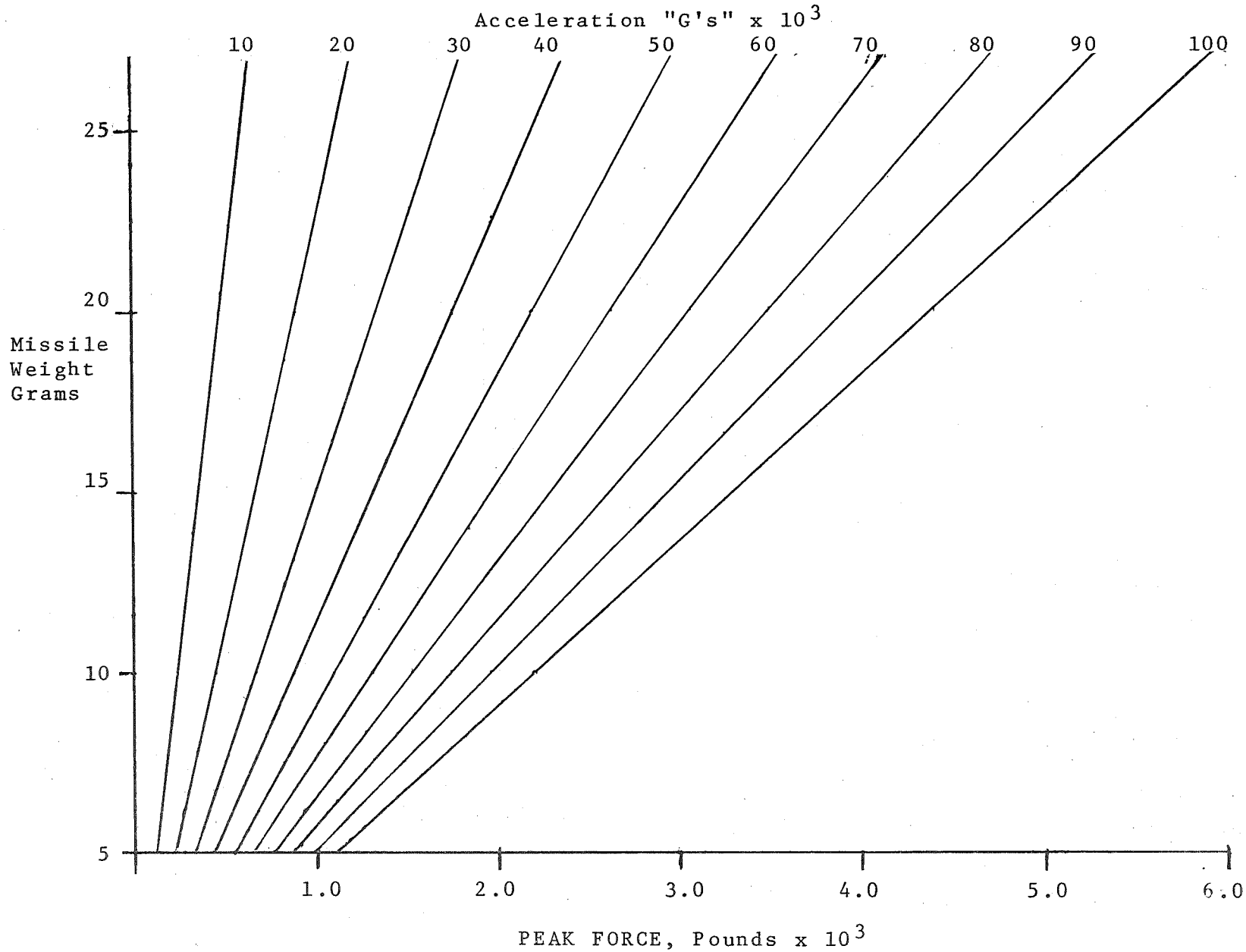
g. From chart, Figure 8.22, determine peak force required to give required acceleration for the missile weight.

h. Set peak reading voltmeter to proper scale, (10, 20, 50, 100, 200, 500, 1000, 2000, or 5000 lbs/volt) to allow peak force to fall approximately mid-scale.

i. Test fire missile with dummy device by placing it in pneupactor breech end and depressing firing pedal.

j. Adjust air pressure to obtain the peak voltage reading required and refire.

Figure 8.22 - REQUIRED FORCE FOR GIVEN MISSILE WEIGHT AT VARIOUS "G" LEVELS



k. Continue test firing until three consecutive readings are within ± 10% of the required value.

l. Fire each test device missile five (5) times.

m. Unload devices from missiles.

n. Read and record specified electrical parameter for each device.

o. Repeat steps "b" through "n" for each 'G' level.

8.8. THERMAL SHOCK

8.8.1. Purpose:

The purpose of this test is to determine the capability of a device to withstand sudden extreme changes in temperature. These temperature changes cause variation in physical characteristics that in turn can cause changes in electrical characteristics and physical damage.

8.8.2. Equipment:

The equipment consists of two temperature controlled baths containing suitable liquids chosen to obtain the temperature extremes. It also includes a device holding basket and a transfer mechanism to alternately immerse the devices in each temperature extreme bath for the specified time.

8.8.3. Temperature Extremes:

The program devices were subjected to the temperature extremes of $+200 \begin{smallmatrix} +0 \\ -5 \end{smallmatrix}$ °C and $-65 \begin{smallmatrix} +5 \\ -0 \end{smallmatrix}$ °C for a total of 200 cycles. Electrical test and hermeticity checks were performed at each 20 cycle interval. Immersion time was 5 minutes and transfer time 3 seconds.

Each bath contains silicon oil which is capable of maintaining proper viscosity at the required extremes.

Temperature control is achieved by means of a thermocouple controlled resistance heater for the high temperature bath and a dry ice cooled bath for the low temperature. Thermometers are also provided for each bath as an additional temperature monitor.

8.8.4. Procedure:

a. Read and record specified electrical parameters for each device.

b. Helium leak test each device. Record readings over 1×10^{-8} atm cm^3/sec.

c. Fluorocarbon gross leak test each device and record whether or not bubbles emanate from each device.

d. Place devices in holding basket and suspend basket on transfer mechanism in thermal shock chamber.

e. Set bath timers and transfer timer to 5 minutes and three (3) seconds respectively.

f. Check bath temperatures and adjust if necessary.

g. Close chamber door and start transfer motor.

h. Allow devices to transfer from 20 complete cycles as determined by mechanical counters.

i. Remove basket with devices and degrease.

j. Repeat steps a, b, and c.

k. Repeat steps 'd' through 'j' for each 20 cycles.

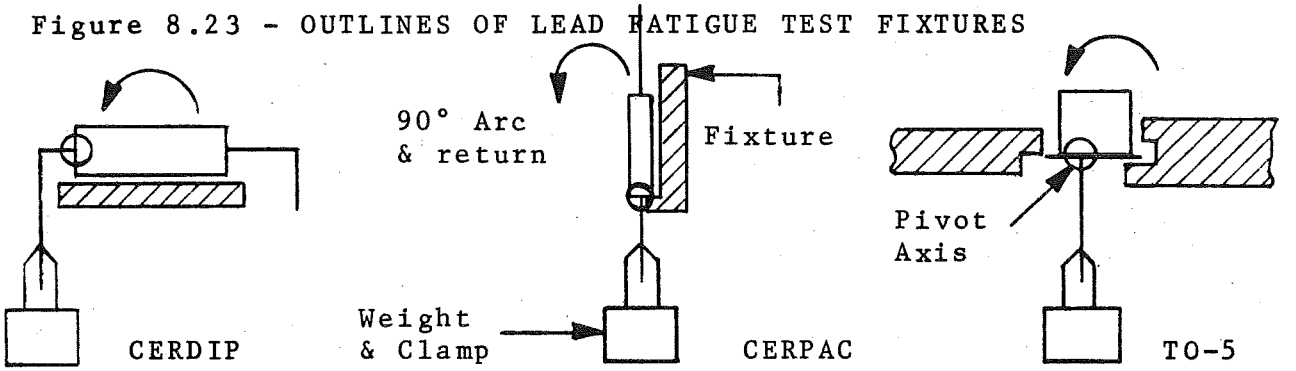
8.9. LEAD FATIGUE (LEAD INTEGRITY)

The purpose of this test is primarily to determine the resistance of the device leads to metal fatigue due to repeated bendings. It is also used to test the capability of the lead seals to maintain hermeticity after repeated bending.

8.9.1. Equipment:

The equipment consists of a fixture capable of holding the device by its body and rotating the body 90°. A weight of 4 ± 0.2 oz. with a clamp for attachment to a device lead is also required. Sketches of the equipment for each type package are shown in Figure 8.23 in the starting position.

Figure 8.23 - OUTLINES OF LEAD FATIGUE TEST FIXTURES



8.9.2. Number of Arcs and Seal Integrity:

The program required subjecting all device leads individually to bending cycles until each lead fatigued or to 200 cycles, whichever occurred first. Helium fine leak and fluorocarbon gross leak tests were performed at selected increments of bending cycles as determined by using other than program devices, such that a minimum of three seal tests were performed.

8.9.3. Procedure:

a. Load device into holding fixture and clamp.

b. Attach weight to device lead number one. Rotate device in fixture 90° and return to starting position for the specified number of bending cycles (arcs).

c. If lead breaks before required number of cycles is completed, record the number of completed bending cycles.

d. Repeat 'b' and 'c' for each lead.

e. Helium fine leak test devices and record leaks $>1 \times 10^{-8}$ atm cm^3/sec.

f. Fluorocarbon gross leak test devices. Record whether or not bubbles are observed emanating from device.

g. Repeat steps 'a' to 'f' for each increment of bending cycles.