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PROJECT TECHNICAL REPORT

TASK ASPO-59

MSFTP-2 BIT SYNCHRONIZER PERFORMANCE ANALYSIS

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MANNED SPACECRAFT CENTER
HOUSTON, TEXAS

Prepared by

Communication and Sensor Systems Department
Electronic Systems Laboratory

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APOLLO COMMUNICATIONS SYSTEM
TASK E-59B
TECHNICAL REPORT

MSFTP-2 BIT SYNCHRONIZER
PERFORMANCE ANALYSIS

27 May 1969

Prepared for
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
MANNED SPACECRAFT CENTER
HOUSTON, TEXAS

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69:7251-HDF-333
24 November 1969
Re: Task E-59C

National Aeronautics and Space Administration
Manned Spacecraft Center
Houston, Texas 77058

Attention: T. E. Ohnesorge, EE7
Tele/Communications Systems Division
Building 440, Room 216

Subject: Update of TRW Project Technical Report #11176-H236-R0-00 "MSFTP-2
Bit Synchronizer Performance Analysis", 27 May 1968.

Gentlemen:

The information contained in this memo will allow the MSFTP-2
BIT SYNCHRONIZER REPORT, TRW Document #11176-H236-R0-00 to be updated.

On page 4-2 there is an error in the definition of λ^2 . The
corrected page 4-3 should be inserted.

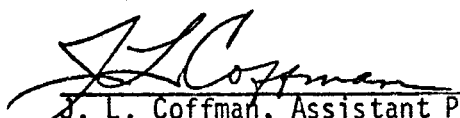
Pages 4-3 and 4-4 attached should replace pages 4-3 and 4-4 in
the document. These pages contain additional information to aid the reader.

The assumption of a constant output for waveform 4 of page 4-11,
Figure 4.3.2.2, while being an excellent engineering assumption (within 1%)
results in an apparent improvement in the matched filter detector from pre-
filtering for low transition densities, i.e. $\approx 10\%$. (Section 4.5.2.2, Perfor-
mance Degradation Curves of I&D Filter Due to Prefiltering, Figures 4.5.5
through 4.5.16). In reality no net improvement can be obtained by pre-
filtering before matched filter detection.

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ABSTRACT

A detailed performance analysis of the MSFTP-2 bit synchronizer based on technical information and drawings supplied by NASA/MSC Information Systems Division has been accomplished. The scope of the analysis includes derivation of a mathematical model describing the bit synchronizer performance as applied in the MSFN network, hardware error analysis of the bit synchronizer to predict and bound its circuit error contributions, and laboratory testing of the bit synchronizer for comparison with predicted results. From the mathematical model, parametric curves are generated showing performance degradation as a function of signal-to-noise ratio, transition density, DC offset, timing error, and prefiltering characteristics. The hardware error analysis, along with the parametric curves, are used to predict the actual performance of the operational hardware. Test results from the bit synchronizer are compared with the predicted results.

The nominal predicted performance degradation for normal operating conditions is 2.5 db from theoretical. This includes approximately 0.7 db degradation attributed to prefiltering in the communications link. The worst case predicted performance, including measurement errors, is 2.9 db.

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1.0 SUMMARY OF CONCLUSIONS AND RECOMMENDATIONS

This section contains a summary of pertinent conclusions regarding performance of the MSFTP-2 bit synchronizer as used in the MSFN system. The conclusions are based on the results of the analysis and test data presented in this report. Recommendations resulting from the analysis are also included.

1.1 INTEGRATE AND DUMP BIT DETECTOR

Three major sources of performance degradation exist in the MSFTP-2 bit synchronizer as follows:

- 1) Degradation due to DC offsets
- 2) Degradation due to timing error
- 3) Degradation due to prefiltering (detector mismatch)

Degradation due to DC offsets exhibits the following characteristics:

- 1) Degradation increases rapidly with increased DC offsets.
- 2) Degradation increases slightly with increase in SNR, i.e., the degradation due to a fixed offset is slightly greater with system operating at an error rate of 10^{-6} than at an error rate of 10^{-3} .
- 3) Degradation depends on the relative likelihood of transmitted "ones" and "zeros".
- 4) DC offsets which occur prior to the split phase chopper (when using split phase code formats) are chopped and integrated to zero yielding no degradation.

Error analysis of the MSFTP-2 bit synchronizer, integrate and dump detector yields a total DC offset error of eight percent (8%) of peak signal amplitude. With ones and zeros equally likely, this offset results in predicted performance degradation as follows:

<u>SNR (db)</u>	<u>Performance Degradation (db)</u>
9.8	0.23
11.4	0.32
13.5	0.40

Degradation of the I&D detector due to timing error exhibits the following characteristics:

- 1) Degradation increases rapidly with increase in timing error.
- 2) Degradation due to timing error decreases with an increase in prefiltering, i.e., the degradation caused by a fixed amount of timing error when operating with unfiltered data is greater than when operating with prefiltered data.
- 3) Degradation due to timing error decreases with a decrease in transition density (less transitions in input data). Since the clock is extracted from the PCM data, the magnitude of the timing error increases with decrease in transition density.

Degradation of the I&D detector due to prefiltering exhibits the following characteristics:

- 1) Degradation increases sharply with decrease in prefilter cut off frequency below twice the bit rate.
- 2) Degradation, with fixed conditions of prefiltering increases with increase in transition density.
- 3) Degradation depends on the filter response characteristics and generally decreases with increase in the order of the filter, i.e., a six pole butterworth low pass filter yields slightly less degradation than does a one pole low pass filter of equivalent cut off frequency.
- 4) Error analysis of the MSFTP-2 bit synchronizer yields a total timing error of nine percent (9%) and ten percent (10%) of a bit period for transition densities of 100 percent and 50 percent respectively.

Predicted performance degradation of the MSFTP-2 bit synchronizer I&D detector due to timing error and prefiltering is approximately 1.5 db for the following set of conditions:

Transition density = 50%

Signal-to-noise ratio = 13.5 db (10^{-6} error rate)

Six pole butterworth low pass prefilter with cut off frequency of 1.5 times the bit rate

Timing error = 10% of a bit period.

For the set of conditions listed above, the total predicted performance is as follows:

DC offset degradation	0.4 (db)
Timing error and prefiltering degradation	<u>1.5</u>
	1.9
Allowance for cumulation of degradations contributing less than 0.1 db degradation each	<u>0.5</u>
<u>Nominal predicted degradation</u>	2.4
Allowance for measurement accuracy	<u>0.5</u>
<u>Worst case predicted degradation</u>	2.9 (db)

1.2 FILTER AND SAMPLE BIT DETECTOR

Error analysis of the MSFTP-2 bit synchronizer, filter and sample detector yields a total DC offset error of six percent (6%) of peak signal amplitude. This offset results in the following predicted performance degradation.

<u>SNR (db)</u>	<u>Performance Degradation (db)</u>
9.8	0.13
11.4	0.19
13.5	0.24

Degradation of the F&S detector due to timing error exhibits the following characteristics:

- 1) Degradation increases with increase in timing error, but less rapidly than for the I&D detector. This is due to the relative "flatness" of the F&S detector output waveform at sampling.
- 2) Degradation due to timing error decreases with decreased transition density. Since the clock is extracted from the PCM data, however, the magnitude of timing error increases with decrease in transition density.
- 3) Error analysis of the MSFTP-2 bit synchronizer yields a total timing error of nine percent (9%) and ten percent (10%) of a bit period for transition densities of 100 percent and 50 percent respectively.

Performance of the F&S detector is degraded, compared to the I&D theoretical, due to the sub-optimum nature of the F&S detector. The predicted performance degradation of the MSFTP-2 F&S detector with unfiltered input data is 2.2 db for the following set of conditions:

Transition density = 50%

Signal-to-noise ratio = 13.5 db (error rate of 10^{-6})

Following is a summary of predicted performance for the F&S detector

DC offset degradation	0.24 (db)
F&S degradation	<u>2.20</u>
	2.44
Allowance for cumulation of degradations contributing less than 0.1 db degradation each	<u>0.50</u>
<u>Nominal predicted degradation</u>	2.94
Allowance for measurement errors	<u>0.50</u>
<u>Worst case predicted degradation</u>	3.44 (db)

The following input conditions pertain to the above listed predicted performance

Transition density = 50%

SNR = 13.5 db (error rate of 10^{-6})

Timing error = 10% of a bit period

1.3 RECOMMENDATIONS

A slight improvement in performance of the MSFTP-2 I&D detector (0.3 db to 0.5 db) can be obtained by prefiltering the input signal at 1.5 to 2.5 times the bit rate. This is because the timing error degradation is slightly reduced by prefiltering.

It is recommended that particular attention be paid, during calibration and maintenance, to the adjustments of the tunable low pass filter, Schmitt triggers, and integrator phasing. These circuits, if not properly aligned, contribute large errors.

It is recommended that the degradation due to input AC baseline variations be measured. Analysis contained in this report shows that the bit synchronizer will be degraded by approximately 2.8 db in the presence of sinusoidal AC baseline variation of frequency equal to one percent of the bit rate and peak-to-peak amplitude equal to the peak-to-peak signal amplitude.

2.0 INTRODUCTION

This report presents the results of the MSFTP-2 Bit Synchronizer performance analysis performed on subtask EB 35-01. The work was performed by TRW Systems for NASA/MSC under Task E-59B. The contents of this report present mathematical modeling, hardware error analysis, performance prediction, and test results for the MSFTP-2 bit synchronizer.

Background, scope, and objectives are given in Section 3.0. This section describes the purpose and direction of the analyses.

Sections 4.0 and 5.0 give the performance analysis and theoretical considerations of the bit synchronizer. Parametric curves are presented showing performance degradation due to DC offsets, timing errors, and prefiltering of the PCM data as a function of transition density, signal-to-noise ratio, and prefilter bandwidth and response characteristics. Curves showing predicted performance, based on the hardware error analysis, are given. Additionally, test data taken on the bit synchronizer are presented and compared with predicted performance.

Appendices A through H give detailed description and analysis in support of the report. Included is the description of operation, DC error analysis, prefiltering performance analysis, timing error analysis, analysis of the bit synchronizer tunable filter and phase lock loop, AC analysis of the baseline correction circuitry, and a description of computer programs used in the numerical computations.

Notable conclusions and recommendations are included in Section 1.0.

3.0 TECHNICAL APPROACH

3.1 BACKGROUND

3.1.1 General

The purpose of the bit synchronizer is to coherently detect noise contaminated PCM data and to do so as efficiently as possible. The bit synchronizer must make the best possible estimate as to which symbol ("one" or "zero") was transmitted.

To accomplish this function the bit synchronizer must perform the following three operations.

Lock onto the incoming signal (or a separately transmitted sync signal) and estimate the location of the bit position.

Provide a bit detector which is matched to the incoming waveform such that the signal-to-noise ratio out of the detector at the time of sampling is maximized.

Compare the detector output, at the sampling time, with a reference voltage which weighs the binary "one" and "zero" symbols equally. The reference voltage is usually zero volts, with a binary "one" being, for example, A volts positive and a binary "zero" being A volts negative. If the detector output exceeds zero volts a binary "one" is outputted, a binary "zero" is outputted otherwise.

The function of the bit detector or matched filter is to maximize the signal-to-noise ratio, over a bit period, at its output. When sampled, this will provide the best estimate as to which symbol was transmitted. Only a decision as to the polarity of the signal and of the detector is required, therefore, preservation of the signal waveform at the detector output is unimportant. The signal waveform into the detector is important, however, because the transfer function of the matched filter (and whether or not a realizable matched filter exists) depends on the signal waveform.

The matched filter [1,2] in the presence of additive Gaussian noise has the transfer function $H(j\omega)$ given by

$$H(j\omega) = \frac{F^*(j\omega)e^{-j\omega t_0}}{|G_n(F)|^{1/2}}$$

where

$F^*(j\omega)$ = Fourier transform of the conjugate of the bit waveform to be detected

$G_n(F)$ = power spectral density of the additive Gaussian noise

Signal and noise voltages are independent.

For the important case where the noise spectrum is flat (white Gaussian noise), $G_n(F) = N_0$, (one sided noise spectral density)

$$H(j\omega) = K F^*(j\omega)e^{-j\omega t_0}$$

and the filter impulse response $h(t)$ is the time inverted replica of the bit waveform.

For the case of square wave PCM data, the bit symbol over a bit period (T) is a constant value (A). The filter with impulse response $h(t)$ which is a time inverted replica of the bit waveform is the familiar integrate and dump (I&D) filter which is dumped or reset at time T .

For the I&D filter:

$$H(S) = \frac{A(1 - e^{-ST})}{S}$$

$$h(t) = A \quad 0 < t < T$$

Thus the I&D filter is a matched filter to a square wave PCM pulse provided that the dump signal is supplied at exactly the right time and that the magnitude of the amplitudes of the binary ones and zeros are symmetrical with respect to the comparison reference voltage. The I&D filter, along with pertinent waveforms, is shown in Figure 3.1.1.

In the figure the reference voltage (E_{ref}) is zero volts which requires the input binary one-zero symbols to be of amplitudes A and $-A$ respectively. Any DC offset in the PCM data must be corrected prior to input to the bit detector or the reference voltage must be shifted with the DC offset to maintain the symmetry.

As stated earlier, the I&D filter is matched only for square wave inputs. Prefiltering of the data prior to input to the I&D mismatches the filter with resulting loss in detection efficiency.

From the preceeding discussion it is seen that there are three (3) major sources of performance degradation in the bit synchronizer identified as follows:

1. DC Offset
2. Timing Error
3. Prefiltering Mismatch

Each error is composed of a number of error contributions. DC offset error is the sum of DC circuit offsets and equivalent AC offsets which occur in a given bit period. The timing error is the sum of filter delays, phase lock loop output jitter, static phase error, etc. The prefiltering mismatch is a function of bandwidth and phase/magnitude characteristics of the link preceeding the bit synchronizer. It is recognized that performance improvement may result from prefiltering with some forms of bit detectors, i.e., the prefiltering serves to better "match" the detector. This is generally true of the filter and sample detector which will also be discussed.

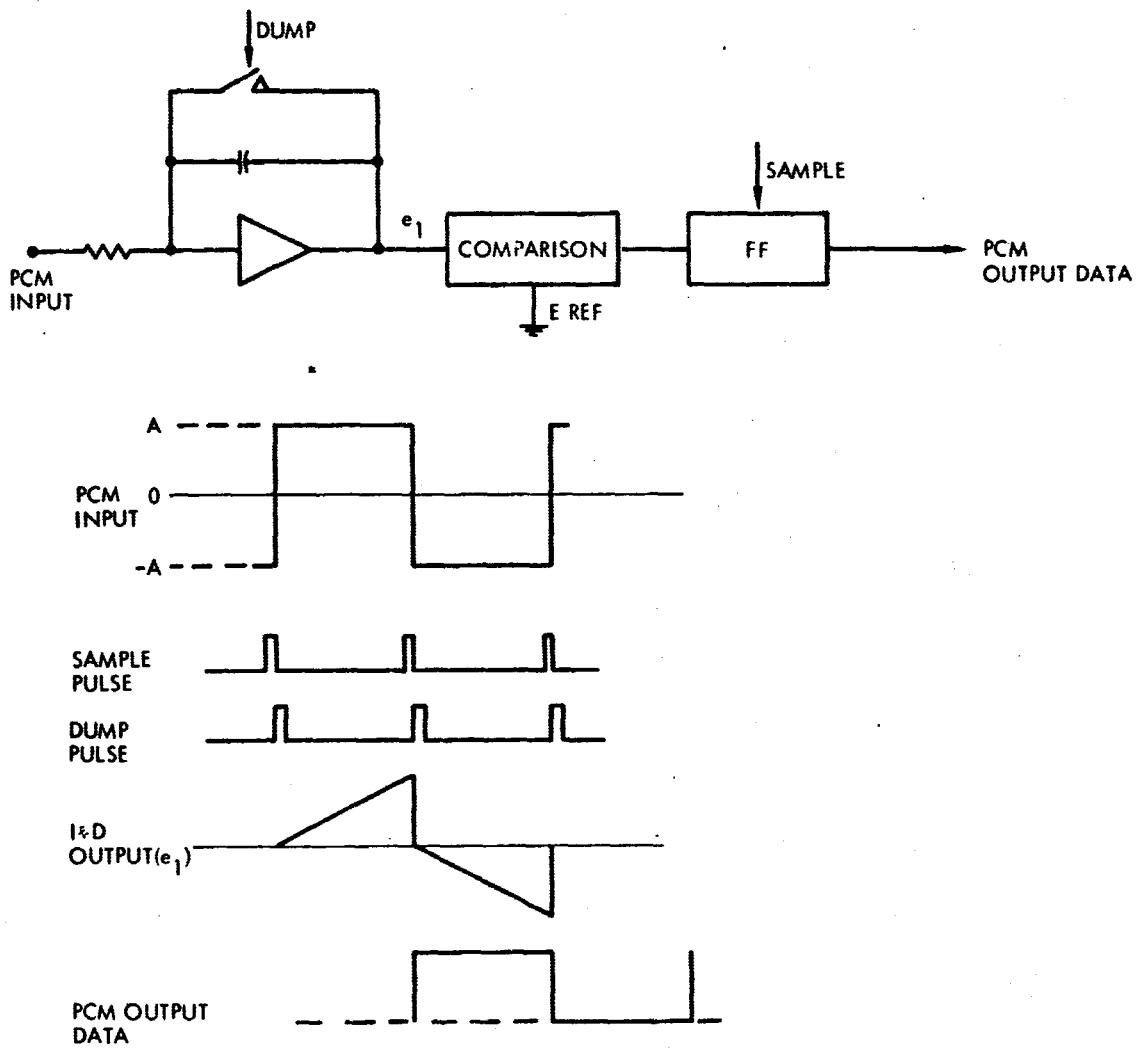


Figure 3.1.1 Integrate and Dump Detector and Pertinent Waveforms

3.1.2 MSFTP-2 Bit Synchronizer Simplified Block Diagram and Description

The MSFTP-2 bit synchronizer is shown in simplified block diagram form in Figure 3.1.2. The bit synchronizer utilizes two bit detectors, the integrate and dump (I&D) and the filter and sample (F&S). Either of the two detectors can be used to reconstruct NRZ or RZ data and the I&D detector can be used to reconstruct split phase (manchester code) data as well.

Provision is made within the synchronizer to extract the clock or timing information directly from the PCM data. This is done via the clock extraction loop. The clock extraction loop provides the necessary timing signal to the bit detectors. In the case of the I&D, the detector is sampled just prior to dump, and dumped or reset at the end of each bit period. The F&S detector is sampled at the middle of each bit period.

Also included in the bit synchronizer is an automatic gain control (AGC) and a baseline correction loop. The baseline correction loop compensates for AC and DC baseline offset of the PCM data at the input. The comparison reference voltage is zero volts. A detailed description of operation and block diagram of the MSFTP-2 bit synchronizer is included in Appendix A.

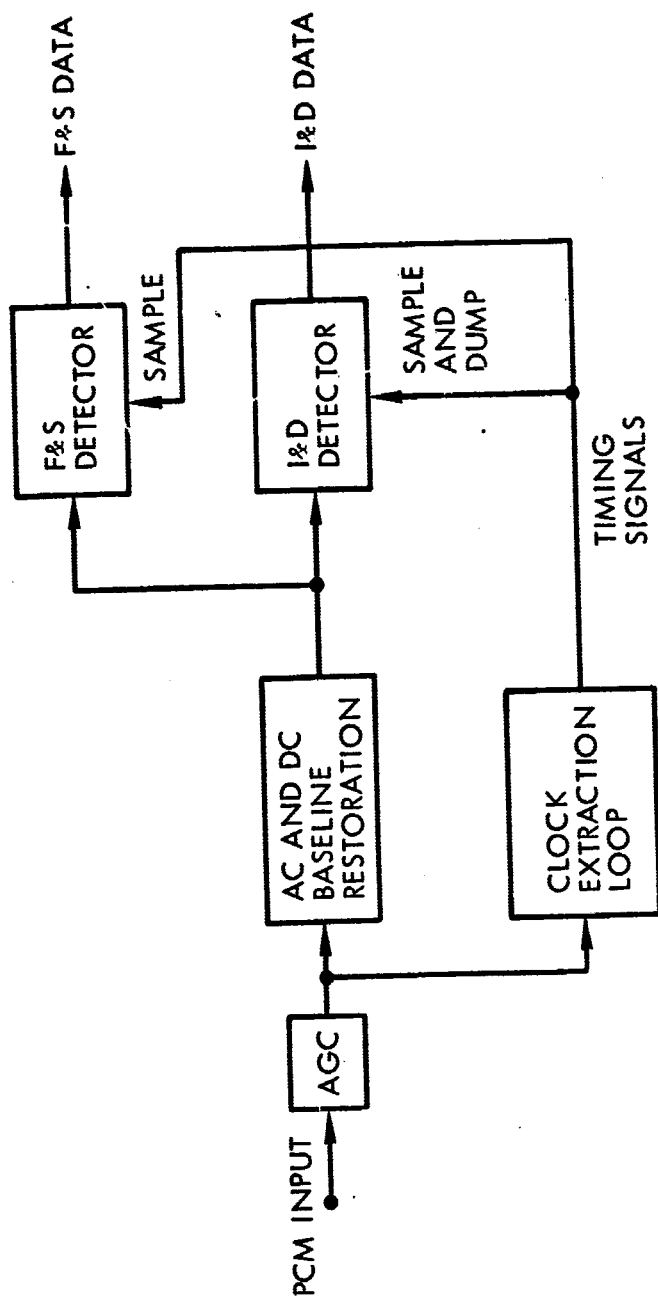


Figure 3.1.2 Simplified Block Diagram of MSFTP-2 Bit Synchronizer

3.2 SCOPE AND OBJECTIVES

The scope of the performance analysis of the MSFTP-2 bit synchronizer, carried out in this report, includes derivation of a mathematical model describing the unit performance with respect to DC offset, timing error, and prefiltering as well as error analysis of the hardware. The error analysis was conducted in an attempt to bound and predict the overall performance of the operational hardware. In some cases where detailed information of circuit characteristics or mechanization techniques is not available, engineering estimates of error contributions are utilized.

The mathematical modeling approach is shown pictorially in Figure 3.2.1. The I&D and F&S bit detectors, which are assumed ideal, have noise contaminated square wave inputs applied through a low pass filter $H(j\omega)$ which represents the data link. Summed with the PCM data, at the detector inputs, is a DC offset (r) normalized to nominal peak signal amplitude. Finally, a timing error (θ), normalized to the bit period (T), is injected into the detector timing signals.

Performance degradation is calculated as a function of signal-to-noise ratio, bit transition density, DC offset, timing error, and filter bandwidth and characteristics. The performance degradation is arrived at by calculating the bit error rate (BER) which results from the combination of errors and comparing this BER with its theoretical BER which would result with square wave data and no timing or offset errors. The performance degradation (in db) is the increase in input SNR which would be required with a given combination of errors and prefiltering to achieve the BER which would result were the errors and prefiltering not present. Calculation of the performance degradation involves expressions which cannot be shown in closed form, therefore the computations were run on the computer and are included in the form of parametric curves from which the degradation can be read as a function of the error combinations.

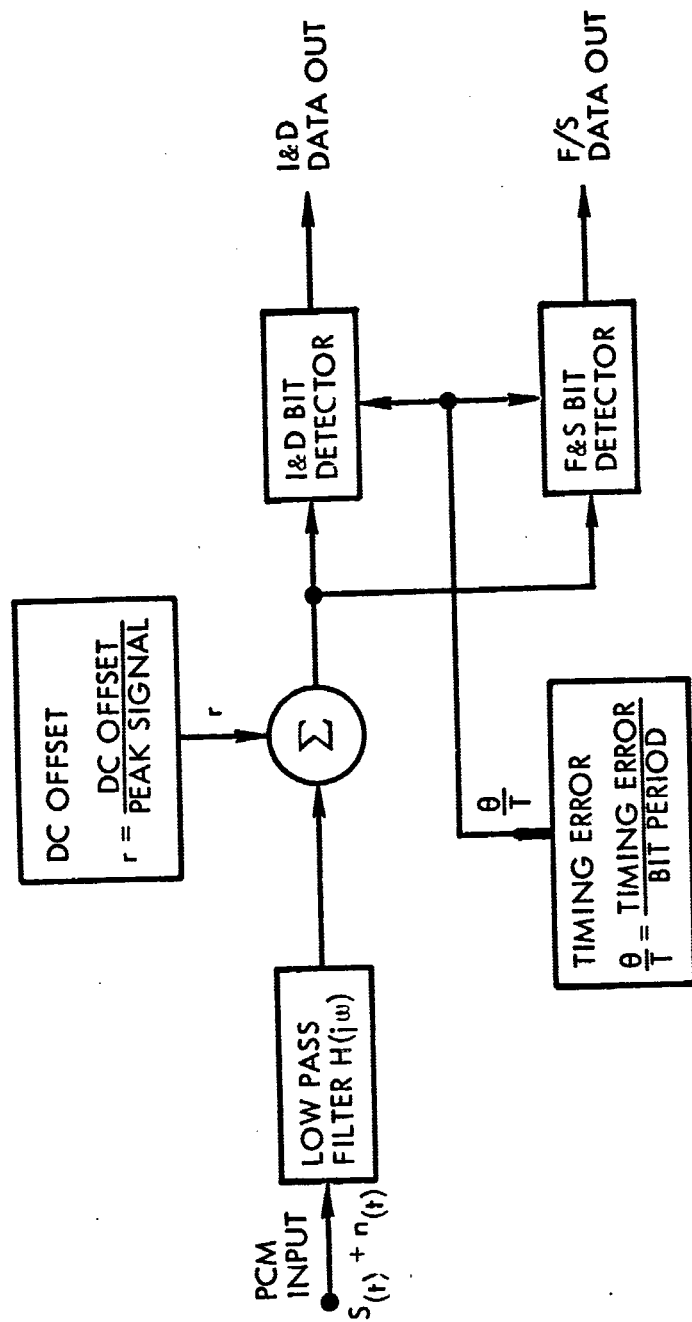


Figure 3.2.1 Block Diagram Illustrating Math Model of MSFTP-2 Bit Synchronizer

4.0 PERFORMANCE ANALYSIS UTILIZING INTEGRATE AND DUMP BIT DETECTOR

4.1 THEORETICAL PERFORMANCE OF I&D DETECTOR

The probability of occurrence of a bit error in a PCM system is the probability that the noise will exceed the signal voltage in amplitude and be of the opposite polarity, causing the detector to decide on the wrong symbol. For the case of Gaussian noise the probability of error is determined using the Gaussian probability density function, $P(X)$.

$$P(X) = \frac{1}{\sqrt{2\pi} \sigma} e^{-\frac{x^2}{2\sigma^2}} \quad (4.1.1)$$

The probability that the instantaneous noise voltage is less than the peak signal voltage, A , is:

$$\text{Prob}(X < A) = \int_{-\infty}^A P(X) dx = \int_{-\infty}^A \frac{1}{\sqrt{2\pi} \sigma} e^{-\frac{x^2}{2\sigma^2}} dx \quad (4.1.2)$$

letting $y = \frac{x}{\sigma}$

$$\text{Prob}(X < A) = \int_{-\infty}^{\frac{A}{\sigma}} \frac{1}{\sqrt{2\pi}} e^{-\frac{y^2}{2}} dy \quad (4.1.3)$$

but: $\frac{A}{\sigma} = \lambda = \frac{\text{Peak signal voltage out of the detector}}{\text{RMS noise voltage out of the detector}}$

The probability of error as a function of signal-to-noise ratio, $P_E(\lambda)$, is:

$$P_E(\lambda) = 1 - \int_{-\infty}^{\lambda} \frac{1}{\sqrt{2\pi}} e^{-\frac{y^2}{2}} dy = 1 - \phi(\lambda) \quad (4.1.4)$$

$$P_E(\lambda) = 0.5 - \int_0^{\lambda} \frac{1}{\sqrt{2\pi}} e^{-\frac{y^2}{2}} dy \quad (4.1.5)$$

$$\lambda^2 = \frac{\text{Signal energy per bit out of the detector}}{\text{RMS noise out of the detector}}$$

$$\lambda^2 = \frac{E}{N_0 B} = \text{Detector output signal-to-noise ratio}$$

E = signal energy

N_0 = noise spectral density (one sided)

B = detector bandwidth

Therefore the probability of error, $P_E(\lambda)$, is a function of the voltage signal-to-noise ratio out of the detector and is therefore referred to the detector noise bandwidth. The noise bandwidth of an integrate and dump detector with NRZ data is one half the bit rate as shown in the following.

The noise bandwidth (B_N) of a linear network [6] is defined as:

$$B_N = \frac{\int_{-\infty}^{\infty} |H(j\omega)|^2 df}{|H(j\omega)|_{MAX}^2}$$

$H(j\omega)$ = magnitude of network transfer function

The transfer function of the I&D filter is:

$$H(S) = \frac{A(1 - e^{-ST})}{S} \quad (4.1.6)$$

$$H(j\omega) = \frac{A}{j\omega} (1 - e^{-j\omega T}) = \frac{A}{j\omega} \left(e^{j\frac{\omega T}{2}} - e^{-j\frac{\omega T}{2}} \right) e^{-j\frac{\omega T}{2}} \quad (4.1.7)$$

$$\sin X = \frac{1}{2j} (e^{jX} - e^{-jX})$$

$$H(j\omega) = AT e^{-j\frac{\omega T}{2}} \left[\frac{\sin \frac{\omega T}{2}}{\frac{\omega T}{2}} \right] \quad (4.1.8)$$

$$|H(j\omega)|^2 = A^2 T^2 \left[\frac{\sin \frac{\omega T}{2}}{\frac{\omega T}{2}} \right]^2 = A^2 T^2 \left[\frac{\sin \pi T f}{\pi T f} \right]^2 \quad (4.1.9)$$

$$B_N = \frac{A^2 T^2 \int_0^{\infty} \left[\frac{\sin \pi T f}{\pi T f} \right]^2 df}{A^2 T^2}$$

Let

$$X = \pi T f$$

$$B_N = \frac{1}{\pi T} \int_0^{\infty} \left[\frac{\sin X}{X} \right]^2 dX$$

$$\int_0^{\infty} \left[\frac{\sin X}{X} \right]^2 dX = \frac{\pi}{2}$$

$$B_N = \frac{1}{2T}$$

$$\frac{1}{T} = f_B = \text{bit rate}$$

Therefore

$$B_N = \frac{f_B}{2} = \frac{1}{2} \text{ bit rate}$$

Sample calculation of theoretical performance for the I&D filter, using Equation 4.1.4, are shown tabulated in Table 4.1.1 and plotted in Figure 4.1.1.

The results of the preceding discussion are adhered to throughout the MSFTP-2 bit synchronizer analysis. Performance degradation is always calculated as degradation from theoretical as shown in the figure. Signal-to-noise ratio is always referred to the I&D detector noise bandwidth of one-half the bit rate.

TABLE 4.1.1

SAMPLE CALCULATIONS OF THEORETICAL PERFORMANCE OF I&D FILTER

SNR (db)	λ	$\phi(\lambda)$	$P_E = 1 - \phi(\lambda)$
2.0	1.26	0.8961653188	1.0383468×10^{-1}
4.0	1.585	0.9429465667	$5.70534333 \times 10^{-2}$
5.92	1.98	0.9761482356	$2.38517644 \times 10^{-2}$
7.96	2.50	0.9937903346	6.2096654×10^{-3}
9.8	3.09	0.99900000	1.0000×10^{-3}
9.96	3.15	0.9991836477	8.163523×10^{-4}
11.92	3.95	0.9999609244	3.90756×10^{-5}
14.0	5.0	0.9999997133	2.867×10^{-7}

$$\text{SNR}(\text{db}) = 20 \log \lambda$$

$$\phi(\lambda) = \int_{-\infty}^{\lambda} \frac{1}{\sqrt{2\pi}} e^{-\frac{y^2}{2}} dy$$

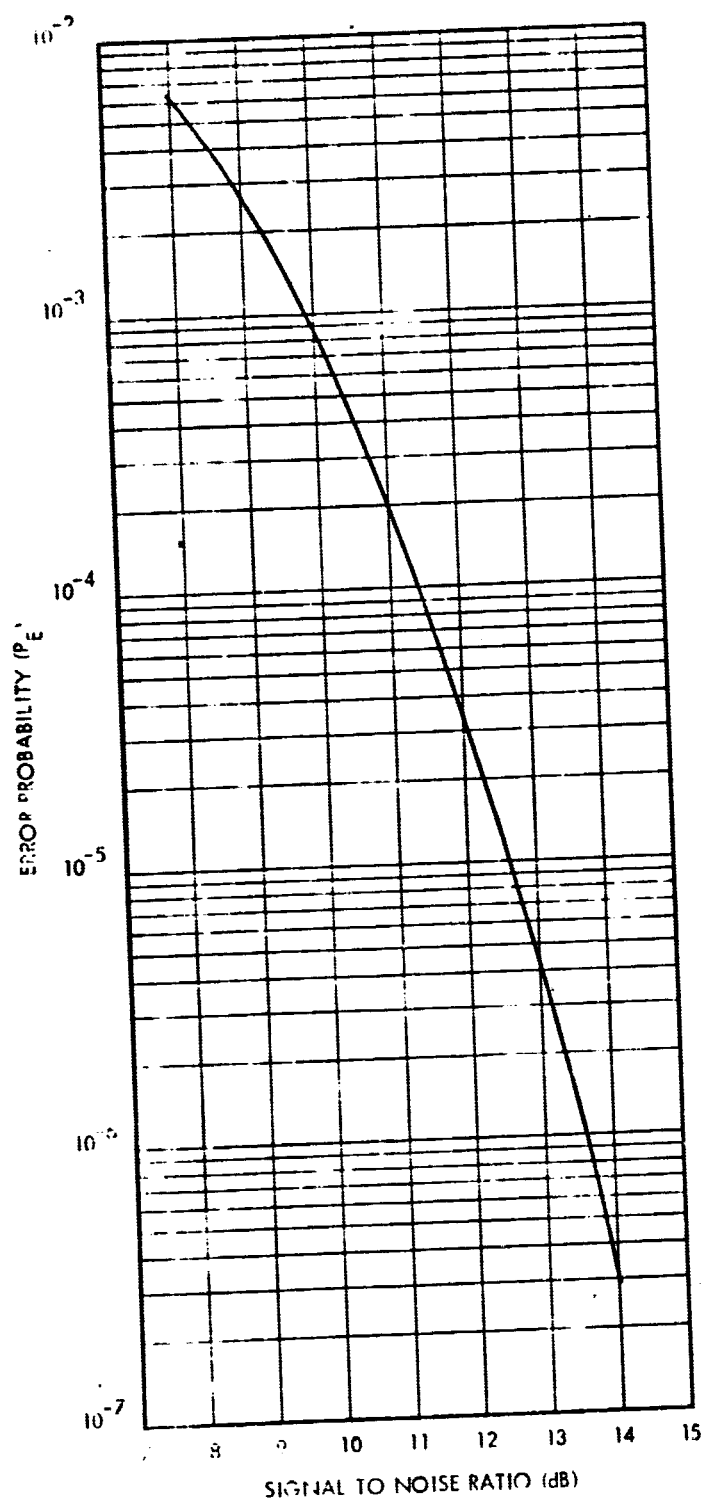


Figure 4.1.1 Theoretical Error Probability Versus Signal-to-Noise Ratio

4.2 PERFORMANCE DEGRADATION DUE TO DC OFFSETS

DC offsets at the detector input, regardless of the source of the offsets, add to the signal level of one binary symbol and subtract for the other, i.e., for an NRZ-L code format where binary ones are represented by a positive voltage level and zeros by a negative level, a positive DC offset adds to the ones level and subtracts from the zeros. Thus the DC offset is an apparent increase in SNR to the ones and an apparent decrease to the zeros in the bit stream. The resulting error probability is the sum of the fractional error probabilities for the ones and zeros.

$$P_{E(r)} = B P_{E1} + (1 - B) P_{E0} \quad (4.2.1)$$

P_{E1} = probability of error given a one was transmitted = $1 - \phi[\lambda(1+r)]$

P_{E0} = probability of error given a zero was transmitted = $1 - \phi[\lambda(1-r)]$

B = fraction of transmitted bits which are ones

r = DC offset normalized to peak signal level

$$P_{E(r)} = 1 - B \phi[\lambda(1+r)] - (1 - B) \phi[\lambda(1-r)] \quad (4.2.2)$$

$$\phi[\lambda(1+r)] = \int_{-\infty}^{\lambda(1+r)} \frac{1}{\sqrt{2\pi}} e^{-\frac{y^2}{2}} dy$$

For the usual case where ones and zeros are equally likely:

$$P_{E(r)} = 1 - 0.5 \phi[\lambda(1+r)] - 0.5 \phi[\lambda(1-r)] \quad (4.2.3)$$

The degradation due to DC offsets has been calculated, using Equation 4.2.2, for a range of DC offsets up to 50% of peak signal amplitude (this range of DC offset allows the general shape of the curve of degradation to be seen). The calculations were made for SNR from 9.8 db to 13.5 db, and likelihood of transmission of ones from 25% to 75% (normal operating ranges). The data is presented and explained in Section 4.5, Figures 4.5.1 through 4.5.4.

4.3 PERFORMANCE DEGRADATION OF THE I&D FILTER DUE TO PREFILTERING

4.3.1 General

The theoretical performance of the I&D filter is based on infinite bandwidth preceeding the bit synchronizer (unfiltered PCM data). Addition of prefiltering ahead of the bit synchronizer causes a loss in I&D performance. The inability of the prefilter output to respond, in zero time, to the data transitions "mismatches" the input waveform to the I&D. As will be shown, the loss depends on the filter bandwidth and transfer function.

The prefiltering also serves to reduce the noise out of the I&D filter. The resulting performance loss is the combined effects of signal degradation and noise improvement in the prefilter. In general, the probability of error as a function of prefiltering, $P_E(f)$, is:

$$P_E(f) = 1 - \phi\left[\lambda\left(\frac{a}{b}\right)\right] \quad (4.3.1)$$

where:

- a = $\frac{\text{Detector output signal voltage with prefilter}}{\text{Detector output signal voltage without prefilter}}$
- b = $\frac{\text{Detector output noise voltage with prefilter}}{\text{Detector output noise voltage without prefilter}}$

The factor (a) represents a reduction in signal at the detector output due to prefiltering and (b) represents a reduction in noise at the detector output.

4.3.2 Signal Loss Due to Prefilter

The response, $f(t)$, of a prefilter to square wave PCM data is shown pictorially in Figure 4.3.2.1. The output is delayed from the input and the waveform is corrupted. The degree to which the waveform is corrupted depends on the occurrence of transitions in the data.

Inspection of Figure 4.3.2.1 reveals that there are four possible waveforms, over a bit period, which result from the prefiltering. The four waveforms are sketched in Figure 4.3.2.2. The conditions for each waveform are as follows:

Waveform (1) - two adjacent transitions

Waveform (2) - lack of transition followed by transition

Waveform (3) - transition followed by lack of transition

Waveform (4) - lack of transitions in adjacent bits

That there are only four waveforms, assumes that the prefilter characteristics are such that the filter output reaches the final value (A) in a time equal to one bit period, i.e., the prefilter intersymbol interference extends only over adjacent bits. For prefiltering cut off frequencies of the order of 1.5 times the bit rate, as occurs in the MSFTP-2 this assumption is valid. For heavily prefiltered data (cut off frequency less than the bit rate), the assumption will yield slightly optimistic results but will serve as a good approximation.

There are four signal loss factors (a_i of Equation 4.3.1), one for each of the four waveforms. Assuming that the filter delay is exactly known by the bit synchronizer (no timing error), the I&D filter output, at sampling, for each waveform, $f(t)$, is the integral of the waveform over the bit period.

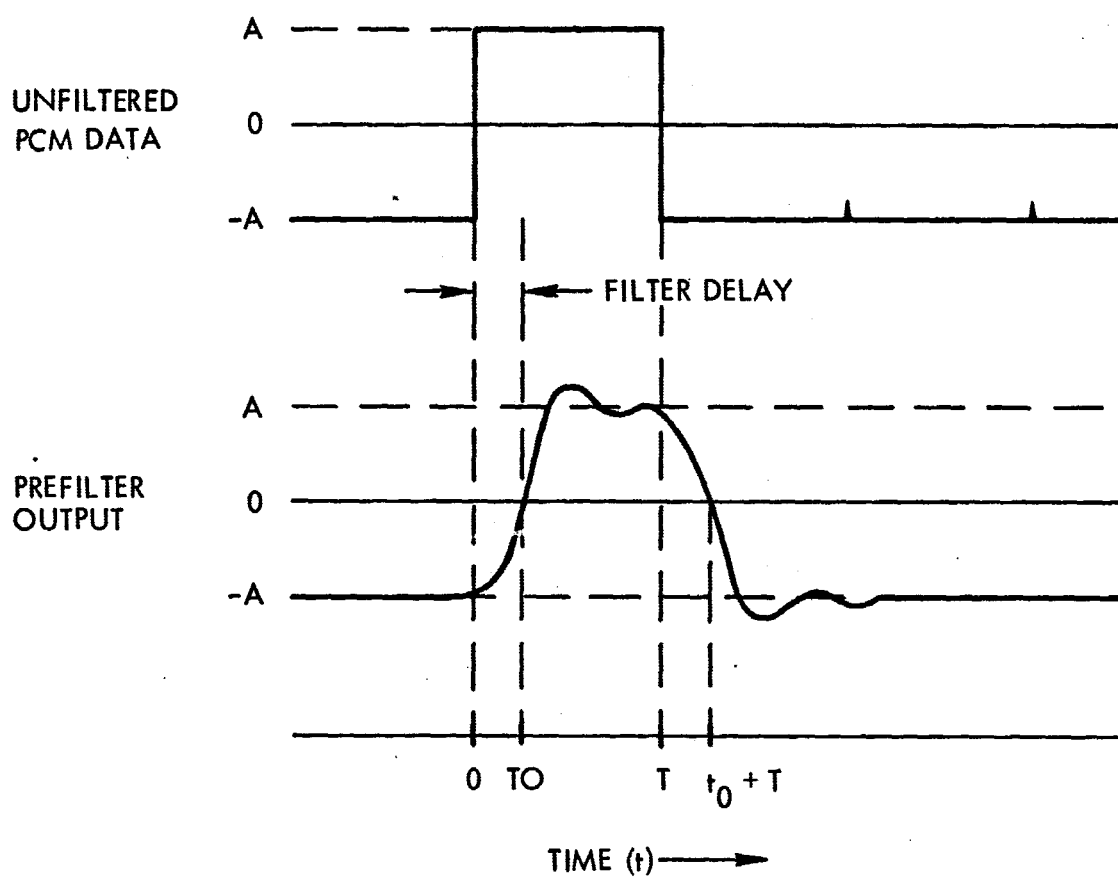


Figure 4.3.2.1 Output Waveform of Prefilter with Unfiltered PCM Input Data

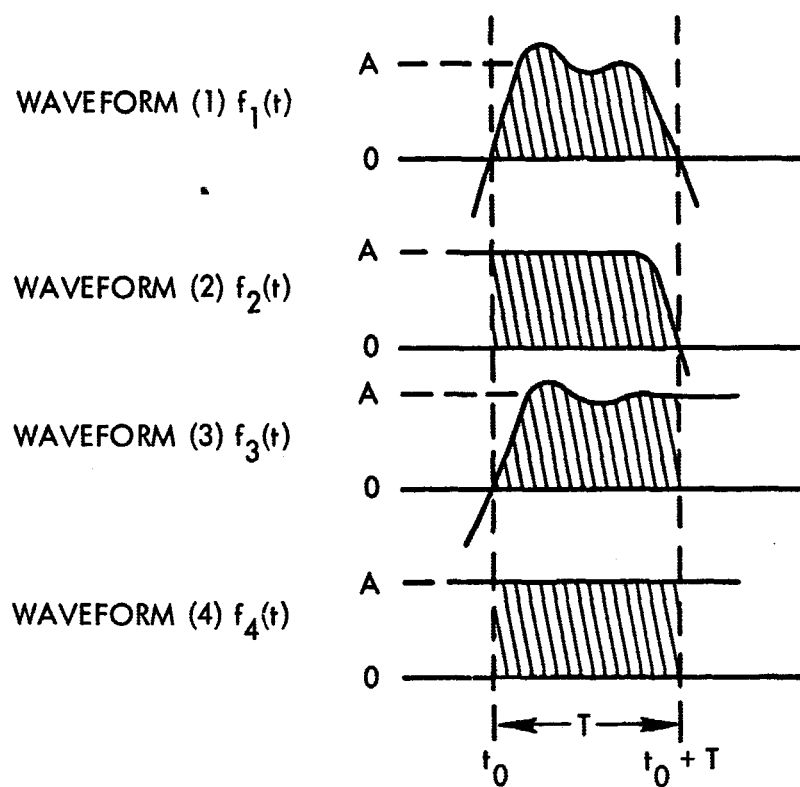


Figure 4.3.2.2 Four Possible Waveforms, over a Bit Period, of Prefiltered PCM Data

Thus, the signal loss factors are:

$$a_1 = \frac{\frac{1}{T} \int_{t_0}^{t_0+T} f_1(t) dt}{\frac{1}{T} \int_{t_0}^{t_0+T} A dt}$$

$$a_1 = \frac{1}{AT} \int_{t_0}^{t_0+T} f_1(t) dt$$

$$a_2 = \frac{1}{AT} \int_{t_0}^{t_0+T} f_2(t) dt$$

$$a_3 = \frac{1}{AT} \int_{t_0}^{t_0+T} f_3(t) dt$$

$$a_4 = \frac{1}{AT} \int_{t_0}^{t_0+T} f_4(t) dt = 1$$

These signal loss factors have been calculated for the following of prefilters for a range of filter cut off frequencies:

- 1) One pole low pass filter (RC section)
- 2) Six pole Butterworth low pass filter
- 3) "Ideal" low pass filter (this filter, which has a "square" passband as shown in Figure C-4, is not physically realizable)

The one pole filter represents a "minimum" type of filtering which might precede the bit synchronizer while the ideal filter represents a maximally flat, infinite slope type of filtering. The six pole Butterworth filter is a good approximation of the actual predetection filtering (Reference No. 7, Appendix B, page B-7). All three filters were used in an attempt to bound the performance of the MSFTP-2 bit synchronizer as a function of prefiltered data.

The loss factors as a function of filter type and cut off frequency are tabulated in Table 4.3.2.1. The calculation of the prefilter loss factors is included in Appendix C of this report.

4.3.3 Noise Improvement at the I&D Detector Output due to Prefiltering

The noise improvement (b) due to prefiltering is the ratio of noise voltages out of the detector with and without prefiltering.

$$b^2 = \frac{P_{02}}{P_{01}} = \frac{\text{Noise Power out of Detector with Prefilter}}{\text{Noise Power out of Detector without Prefilter}}$$

Assuming a constant noise spectral density, (N_0) (White noise):

$$P_{01} = \int_{-\infty}^{\infty} N_0 |H(j\omega)|^2 df$$

Letting N_0 be normalized to one

$$P_{01} = \int_{-\infty}^{\infty} |H(j\omega)|^2 df$$

$H(j\omega)$ = Detector transfer function

TABLE 4.3.2.1

SIGNAL LOSS FACTORS AT I&D OUTPUT DUE TO PREFILTERING

FIL TYPE	R	a ₁	a ₂	a ₃	a ₄	b
One Pole Low Pass Filter	0.5	0.585	0.875	0.709	1.0	0.945
	1.0	0.779	0.937	0.841	1.0	0.968
	1.3	0.821	0.952	0.877	1.0	0.974
	1.5	0.852	0.958	0.893	1.0	0.977
	1.7	0.869	0.963	0.906	1.0	0.981
	2.0	0.889	0.968	0.920	1.0	0.983
	3.0	0.926	0.979	0.946	1.0	0.989
	4.0	0.944	0.984	0.960	1.0	0.995
	5.0	0.955	0.987	0.968	1.0	~1.0
	6.0	0.963	0.989	0.973	1.0	~1.0
	8.0	0.972	0.992	0.980	1.0	~1.0
Six Pole Butterworth Filter	0.5	0.577	0.875	0.704	1.0	0.882
	1.0	0.81	0.958	0.852	1.0	0.950
	1.3	0.841	0.955	0.885	1.0	0.956
	1.5	0.866	0.965	0.902	1.0	0.965
	1.7	0.888	0.974	0.914	1.0	0.972
	2.0	0.902	0.977	0.926	1.0	0.974
	3.0	0.933	0.983	0.950	1.0	0.983
	4.0	0.956	0.987	0.963	1.0	0.987
	5.0	0.960	0.988	0.970	1.0	0.991
	6.0	0.967	0.991	0.975	1.0	1.0
	8.0	0.975	0.994	0.981	1.0	1.0
"Ideal" Square Low Pass Filter	1.0	0.814	0.907	0.907	1.0	0.95
	1.3	0.834	0.918	0.918	1.0	0.955
	1.5	0.870	0.934	0.934	1.0	0.964
	1.7	0.892	0.949	0.949	1.0	0.972
	2.0	0.904	0.952	0.952	1.0	0.974

$$R = \frac{f_c}{f_B} = \frac{\text{filter cut off frequency}}{\text{bit rate}}$$

Assuming the prefilter to pass flat noise in equivalent noise bandwidth, (f_0):

$$P_{02} = \int_{-\infty}^{f_0} |H(j\omega)|^2 df \quad (4.3.3.2)$$

$$b^2 = \frac{\int_{-\infty}^{f_0} |H(j\omega)|^2 df}{\int_{-\infty}^{\infty} |H(j\omega)|^2 df} \quad (4.3.3.3)$$

It was shown in Section 4.1 (Equation 4.1.8) that the transfer function, $H(j\omega)$, of the I&D filter is:

$$H(j\omega) = AT \left[\frac{\sin \frac{\omega T}{2}}{\frac{\omega T}{2}} \right] e^{-\frac{j\omega T}{2}} \quad (4.3.3.4)$$

$$|H(j\omega)|^2 = A^2 T^2 \left[\frac{\sin \frac{\omega T}{2}}{\frac{\omega T}{2}} \right]^2 \quad (4.3.3.5)$$

$$\text{Let } x = \frac{\omega T}{2} = \pi f_0 T$$

$$T = \frac{1}{f_B} \quad f_B = \text{bit rate}$$

$$x = \pi \frac{f_0}{f_B}$$

$$|H(j\omega)|^2 = A^2 T^2 \left[\frac{\sin X}{X} \right]^2$$

$$b^2 = \frac{\frac{A^2 T^2}{\pi T} \int_0^X \left[\frac{\sin X}{X} \right]^2 dX}{\frac{A^2 T^2}{\pi T} \int_0^\infty \left[\frac{\sin X}{X} \right]^2 dX} \quad (4.3.3.6)$$

$$b^2 = \frac{\int_0^X \left[\frac{\sin X}{X} \right]^2 dX}{\int_0^\infty \left[\frac{\sin X}{X} \right]^2 dX} \quad (4.3.3.7)$$

$$b^2 = \frac{\text{Si } 2X - \frac{\sin^2 X}{X}}{\frac{\pi}{2}} \quad (4.3.3.8)$$

where $\text{Si } \bar{X} = \int_0^{\bar{X}} \frac{\sin X}{X} dX$

$$b^2 = \frac{2}{\pi} \left(\text{Si } 2\pi \frac{f_o}{f_B} - \frac{\sin^2 \pi \frac{f_o}{f_B}}{\frac{\pi f_o}{f_B}} \right) \quad (4.3.3.9)$$

$$b = \left[\frac{2}{\pi} \left(\text{Si } 2\pi \frac{f_o}{f_B} - \frac{\sin^2 \pi \frac{f_o}{f_B}}{\frac{\pi f_o}{f_B}} \right) \right]^{1/2} \quad (4.3.3.10)$$

The noise improvement factor squared (b^2) is tabulated in Table 4.3.3.1 and plotted in Figure 4.3.3.1. The noise improvement factor can be read from the figure if the filter effective noise bandwidth is known.

Prefilter Effective Noise Bandwidth

The effective noise bandwidth (f_0) of the one pole, ideal, and six pole Butterworth filters are calculated using the definition of effective square noise bandwidth.

$$f_0 = \frac{\int_{-\infty}^{\infty} |H(j\omega)|^2 df}{|H(j\omega)|_{MAX}^2} \quad (4.3.3.11)$$

$H(j\omega)$ = filter transfer function

For the one pole low pass filter:

$$H(j\omega) = \frac{1}{1 + j\omega T} \quad (4.3.3.12)$$

$$|H(j\omega)|^2 = \frac{1}{1 + \omega^2 T^2} \quad (\text{Magnitude squared})$$

$$|H(j\omega)|_{MAX}^2 = 1$$

$$f_0 = \int_0^{\infty} \frac{df}{1 + (2\pi T)^2 f^2} \quad (4.3.3.13)$$

TABLE 4.3.3.1

SAMPLE CALCULATIONS OF PREFILTER NOISE IMPROVEMENT FACTOR

$\frac{f_o}{f_B}$	$2\pi \frac{f_o}{f_B}$	$\pi \frac{f_o}{f_B}$	$\text{Si } 2\pi \frac{f_o}{f_B}$	$\sin^2 \pi \frac{f_o}{f_B}$	b^2
0	0	0	0	0	0
.25	1.57	.785	1.36	.5	.46
.50	3.14	1.57	1.851	1.0	.775
.75	4.71	2.35	1.61	.5	.888
1.0	2π	π	1.418	0	.903
1.25	7.85	3.92	1.55	.5	.904
1.5	9.42	4.71	1.674	1.0	.932
1.75	11.0	5.5	1.578	.5	.946
2.0	12.56	6.28	1.495	0	.953
2.25	14.12	7.06	1.56	.5	.954
2.5	15.7	7.85	1.632	1.0	.956
2.75	17.28	8.64	1.572	.5	.964
3.0	18.84	9.42	1.5312	0	.976

$$b^2 = \frac{2}{\pi} \text{Si } 2\pi \frac{f_o}{f_B} - \frac{\sin^2 \pi \frac{f_o}{f_B}}{\pi \frac{f_o}{f_B}}$$

$$\text{Si } \bar{X} = \int_0^{\bar{X}} \frac{\sin x}{x} dx$$

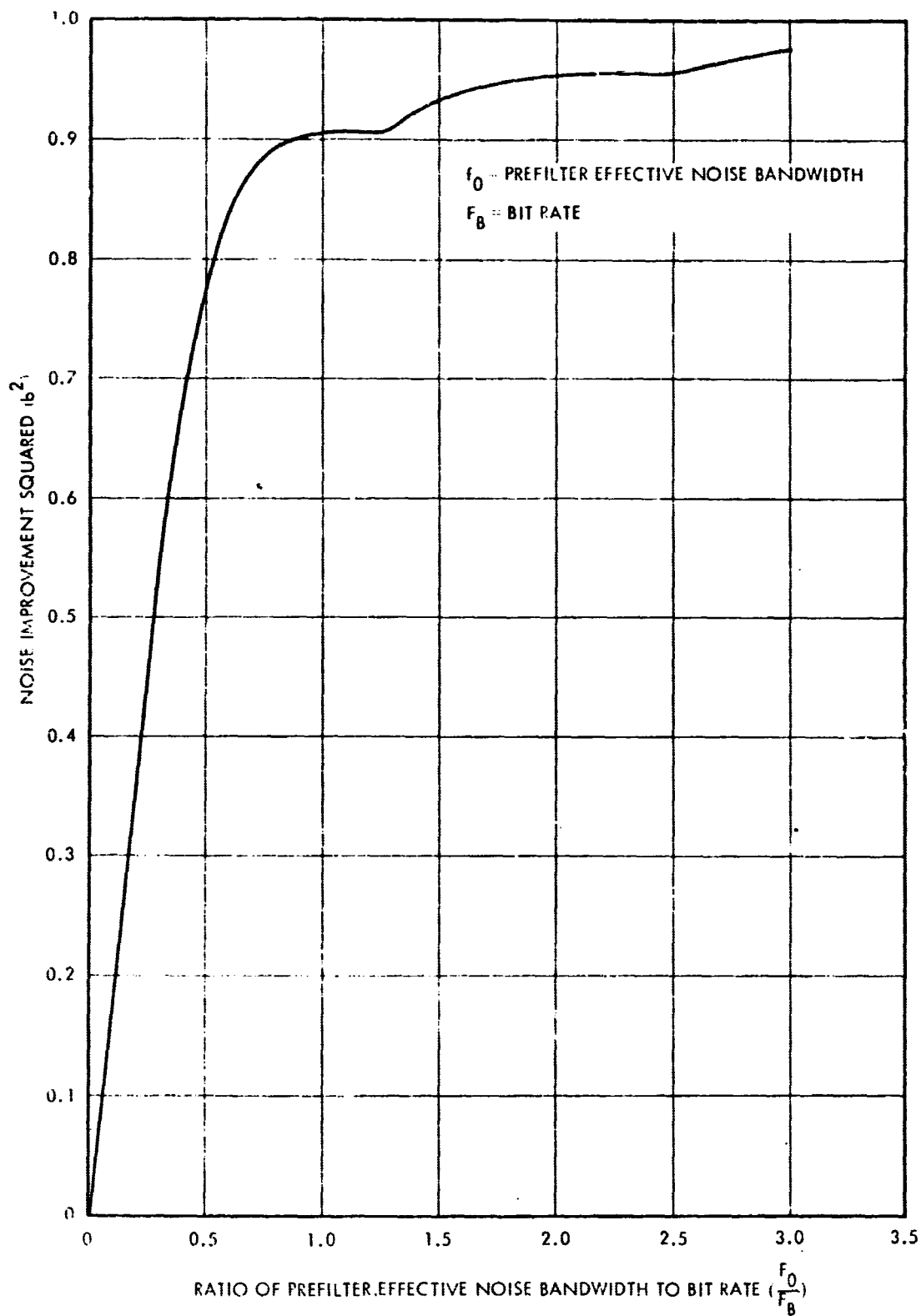


Figure 4.3.3.1 Prefilter Noise Improvement Factor Versus Prefilter Effective Noise Bandwidth

$$f_{01} = \frac{1}{2\pi T} \tan^{-1} T f \Big|_0^\infty$$

$$f_{01} = \frac{1}{2\pi T} \frac{\pi}{2} = \frac{1}{4T}$$

$$T = RC = \frac{1}{2\pi f_c}$$

$f_c = 3$ db cut off frequency of one pole filter

$$f_o = \frac{\pi}{2} f_c = 1.57 f_c \quad (4.3.3.14)$$

For the ideal low pass filter the effective noise bandwidth is equal to the cut off frequency.

$f_o = f_c =$ cut off frequency of ideal filter.

For the six pole Butterworth filter, the magnitude is of the form:

$$|H(j\omega)| = \frac{1}{\left[1 + \left(\frac{f}{f_c}\right)^{12}\right]^{1/2}} \quad (4.3.3.15)$$

$f_c = 3$ db cut off frequency

$$|H(j\omega)|^2 = \frac{1}{1 + \left(\frac{f}{f_c}\right)^2}$$

$$|H(j\omega)|_{MAX}^2 = 1$$

$$f_o = \int_0^{\infty} \frac{df}{1 + \left(\frac{f}{f_c}\right)^2}$$

Integrating numerically, the effective noise bandwidth was found to be.

$$f_o = 1.011 f_c \quad (4.3.3.16)$$

The equations for noise improvement factor for each of the three filters Equation (4.3.3.9) are written below:

One Pole Filter

$$b^2 = \frac{2}{\pi} \left(\text{Si } \pi^2 R - \frac{\text{Sin}^2 \frac{1}{2} \pi^2 R}{\frac{1}{2} \pi^2 R} \right)$$

Ideal Filter

$$b^2 = \frac{2}{\pi} \left(\text{Si } 2\pi R - \frac{\text{Sin}^2 \pi R}{\pi R} \right)$$

Six Pole Butterworth Filter

$$b^2 = \frac{2}{\pi} \left(\text{Si } 2.022\pi R - \frac{\text{Sin}^2 1.011\pi R}{1.011\pi R} \right)$$

where:

$$R = \frac{f_c}{f_B} = \text{the ratio of filter 3 db cut off frequency to bit rate}$$

Values of noise improvement factor (b) for each of the filter types, as a function of filter cut off frequency, are tabulated in Table 4.3.2.1. The calculations were run using a computer program for the above equations.

4.3.4 Probability of Error of Prefiltered Data

The error probability as a function of prefiltering, $P_E(f)$, is calculated by calculating the error rate for each of the four waveforms and summing the error rates in proportion to the likelihood of occurrence of each waveform.

$$P_{E(f)} = \alpha_1 P_{E1} + \alpha_2 P_{E2} + \alpha_3 P_{E3} + \alpha_4 P_{E4} \quad (4.3.4.1)$$

P_{E1} through P_{E4} are the probabilities of error resulting from waveforms 1 through 4 respectively.

α_1 through α_4 are the probabilities of occurrence of waveforms 1 through 4 respectively of Figure 4.3.2.2.

$$\alpha_1 + \alpha_2 + \alpha_3 + \alpha_4 = 1$$

The weighting functions (α_1 through α_4) depend on the transition density and the relative spacing of transitions. Waveform (1) can occur only if two adjacent transitions occur and waveform (4) can occur only if there is a lack of transitions in two adjacent bits. For an assumed 100% transition density for NRZ data the only waveform present at the prefilter output is waveform (1).

In this case:

$$\alpha_1 = 1$$

$$\alpha_2 = \alpha_3 = \alpha_4 = 0$$

If no transitions occur in the data (transition density = 0), then

$$\alpha_4 = 1$$

$$\alpha_1 = \alpha_2 = \alpha_3 = 0$$

A good representation of an actual system is to assume that the occurrence of transitions are "random" such that the likelihood of occurrence of a transition in any bit is equal, and is equal to the transition density (M). The likelihood of the lack of a transition, in any bit, is then one minus the transition density (1 - M). Utilizing the above assumption, the likelihood of each waveform is:

$$\alpha_1 = (M) (M) = M^2 \quad (4.3.4.2)$$

$$\alpha_2 = (1-M) (M) = -M^2 + M \quad (4.3.4.3)$$

$$\alpha_3 = (M) (1-M) = -M^2 + M \quad (4.3.4.4)$$

$$\alpha_4 = (1-M) (1-M) = M^2 - 2M + 1 \quad (4.3.4.5)$$

$$\alpha_1 + \alpha_2 + \alpha_3 + \alpha_4 = 1$$

$$0 \leq M \leq 1$$

The weighting functions (α_1 through α_4) are sketched in Figure 4.3.4.1.

Equation 4.3.4.1, describing error probability due to prefiltering, can now be written in terms of transition density and signal loss and noise improvement due to prefiltering.

$$\begin{aligned} P_{E(f)} = & M^2 [1 - \phi(\lambda \frac{a_1}{b})] + M(1-M) [1 - \phi(\lambda \frac{a_2}{b})] + M(1-M) [1 - \phi(\lambda \frac{a_3}{b})] \\ & + (1-M)^2 [1 - \phi(\lambda \frac{1}{b})] \end{aligned} \quad (4.3.4.6)$$

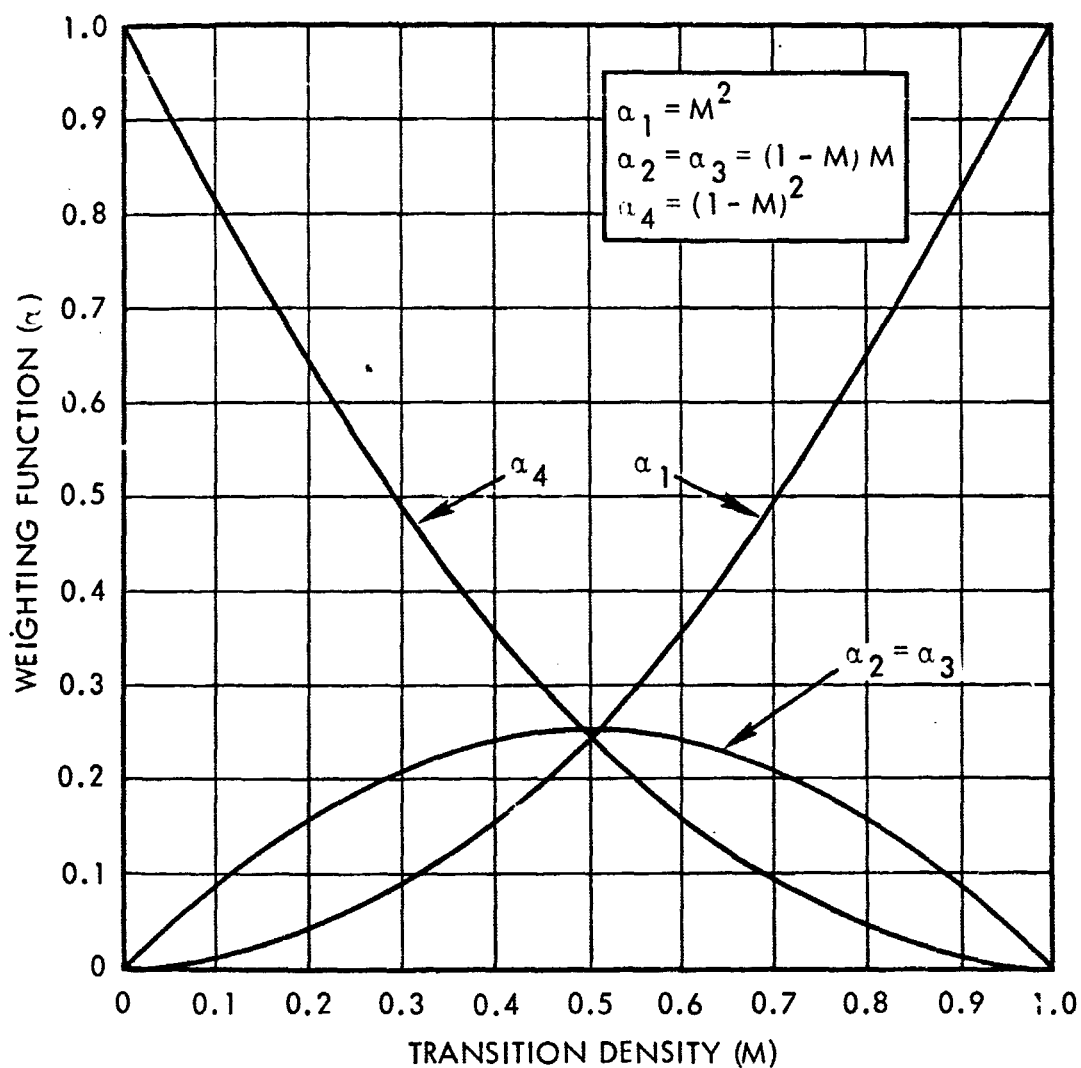


Figure 4.3.4.1 Prefiltered Waveform Weighting Functions Versus Transition Density

The error probability, $P_E(f)$, due to prefiltering has been calculated (using Equation 4.3.4.6) for all three prefilter types. The calculations were made for filter cut off frequencies ranging from one-half the bit rate to eight times the bit rate, for transition densities ranging from 10% to 100%, and signal-to-noise ratios ranging from 9.8 db to 13.5 db which theoretically correspond to error probabilities ranging from 10^{-3} to 10^{-6} . The performance degradation, in db, was calculated for each calculated error probability, $P_E(f)$, by calculating the SNR at which a theoretical I&D filter, with no prefiltering, would yield the same error probability as $P_E(f)$. The degradation was calculated using a successive approximation computer routine and Equation 4.1.4. The computer routine and flow diagram used in the calculations is described in Appendix H of this report. The ranges of cut off frequency, transition density, and SNR were chosen to show the general "shape" of degradation versus these parameters.

Parametric curves showing performance degradation as a function of prefiltering are shown in Figures 4.5.5 through 4.5.16 of Section 4.5.

4.4 PERFORMANCE DEGRADATION OF I&D FILTER DUE TO TIMING ERROR

4.4.1 General

As shown in Section 3.1, the I&D filter is matched to the incoming PCM waveform only if it is sampled and reset at exactly the right time (at the end of the bit period). If timing error exists which displaces the sample and reset point in time, a signal loss occurs at the I&D output with resulting performance degradation. The amount of degradation, with a given timing error, depends on the waveshape at the I&D input and therefore on the characteristics of prefiltering. In general, the degradation due to small timing error decreases with increased prefiltering, i.e., decrease in prefiltering bandwidth. This results from the decreased slope of the input PCM waveform at the data transitions.

The general equation for calculating error probability with timing error (θ) is:

$$P_{E(\theta)} = 1 - \phi[\lambda(\bar{a}_\theta)] \quad (4.4.1.1)$$

$$\bar{a}_\theta = \frac{\text{Detector output signal voltage with timing error}}{\text{Detector output signal voltage without timing error}}$$

The factor ($\bar{a}_\theta$) represents the reduction in signal voltage, due to timing error, at the I&D detector output.

For the case of prefiltered data and timing error, the error probability is:

$$P_{E(f,\theta)} = 1 - \phi[\lambda(\frac{a_\theta}{b})] \quad (4.4.1.2)$$

The factor, a_θ , is now the signal voltage loss at the output of the I&D with prefiltered data and timing error.

The factor b is the same as shown in Equation 4.3.1 and represents the noise improvement due to the prefiltering. Use of Equation 4.4.1.2, $P_{E(f,\theta)}$, yields the error probability due to both prefiltering and timing error.

The four prefilter output waveforms, described in Section 4.3, apply to the timing error loss as well, such that there are four values of a_θ , one for each waveform. The final equation for error rate as a function of timing error and prefiltering is:

$$\begin{aligned} P_{E(f,\theta)} = & M^2[1 - \phi(\lambda\frac{a_{1\theta}}{b})] + M(1-M)[1 - \phi(\lambda\frac{a_{2\theta}}{b})] \\ & + M(1-M)[1 - \phi(\lambda\frac{a_{3\theta}}{b})] + (1-M)^2[1 - \phi(\lambda\frac{a_{4\theta}}{b})] \quad (4.4.1.3) \end{aligned}$$

where:

a_{10} through a_{40} represent the signal losses for waveforms 1 through 4, respectively, as a function of timing error and prefiltering.

b represents prefilter noise improvement

M = transition density

4.4.2 Signal Loss Due to Timing Error

The signal loss at the output of the I&D filter, caused by timing error, results from the integration period of the filter "straddling" data transitions. The filter integrates part of the signal voltage of adjacent bits. If a transition occurs, the voltage polarity of adjacent bits is reversed resulting in reduced I&D output. This is shown pictorially in Figure 4.4.2.1. The figure shows four bits of a PCM waveform. Each bit waveform is one of the four possible and is so marked, i.e., waveform (1) is between adjacent transitions, waveform (4) has no transition on either side. For simplicity the waveforms are drawn for the unfiltered case (square wave data).

A timing error (θ) is present such that the I&D integration period (I) is displaced θ seconds in time from the transitions. The resulting signal loss factors as a function of timing error, for no prefiltering, are:

$$a_{\theta} = \frac{\text{Detector output with timing error}}{\text{Detector output without timing error}}$$

$$a_{10} = \frac{\frac{1}{T} \int_{\theta}^T A dt + \frac{1}{T} \int_T^{T+\theta} A dt}{\frac{1}{T} \int_0^T A dt}$$

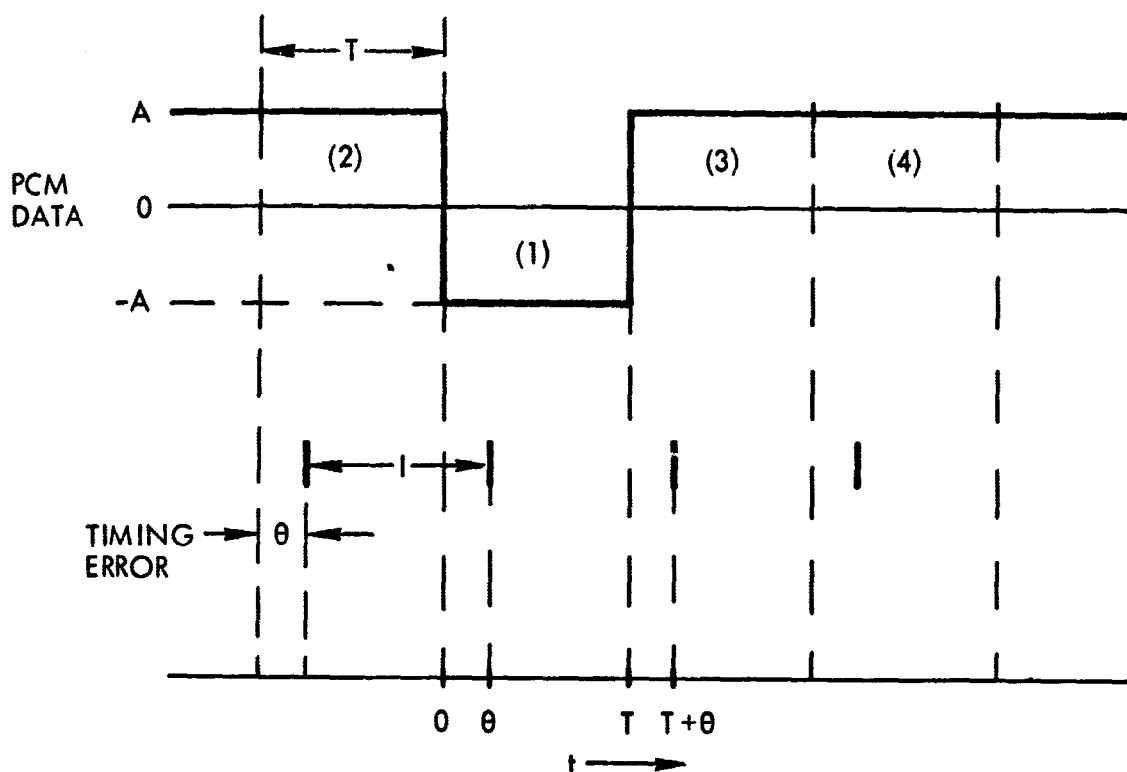


Figure 4.4.2.1 Timing Diagram Illustrating Timing Error in the Bit Synchronizer

$$a_{10} = 1 - 2\frac{\theta}{T}$$

Similarly

$$a_{20} = 1 - 2\frac{\theta}{T}$$

$$a_{30} = 1$$

$$a_{40} = 1$$

Thus, for no prefiltering, the signal loss is proportional to twice the normalized timing error, at the occurrence of data transitions, where the timing error is normalized to the bit period T .

For the case of prefiltering, the loss factors are determined as shown above except the output time response of the filter to the PCM waveform is used. This is shown in Appendix C. The signal loss factors resulting from the six pole Butterworth prefilter are shown in Table 4.4.2.1 for filter cut off frequencies ranging from one-half the bit rate to eight times the bit rate and for timing error ($\frac{\theta}{T}$) from up to 20% of the bit period. The signal loss factors as a function of timing error, for no prefiltering, ($R = \infty$) are also shown in the table.

4.4.3 Probability of Error with Timing Error

The probability of error and performance degradation in db as a function of timing error (using Equation 4.4.1.3) has been calculated using the computer routine described in Appendix H. The calculations were run for each set of loss factors shown in Table 4.4.2.1 with transition densities ranging from 10% to 100% and SNR ranging from 9.8 db to 13.5 db (normal operating ranges).

The calculated data are plotted and described in the curves of Figures 4.5.17 through 4.5.57 of Section 4.5.

TABLE 4.4.2.1

Signal Loss Due to Timing Error and Six Pole Butterworth
Low Pass Filter

R	$\frac{\theta}{T}$	$a_{1\theta}$	$a_{2\theta}$	$a_{3\theta}$	$a_{4\theta}$	b
0.5	0	0.577	0.875	0.704	1	0.882
	0.05	0.571	0.922	0.651	1	0.882
	0.10	0.553	0.963	0.592	1	0.882
	0.15	0.520	0.997	0.526	1	0.882
	0.20	0.485	1.029	0.458	1	0.882
1.0	0	0.810	0.958	0.852	1	0.950
	0.05	0.798	1.002	0.796	1	0.950
	0.10	0.764	1.035	0.729	1	0.950
	0.15	0.708	1.057	0.651	1	0.950
	0.20	0.633	1.069	0.563	1	0.950
1.5	0	0.866	0.965	0.902	1	0.965
	0.05	0.847	1.006	0.843	1	0.965
	0.10	0.799	1.031	0.768	1	0.965
	0.15	0.719	1.042	0.679	1	0.965
	0.20	0.617	1.040	0.577	1	0.965
2.0	0	0.902	0.977	0.926	1	0.974
	0.05	0.864	1.008	0.857	1	0.974
	0.10	0.813	1.033	0.782	1	0.974
	0.15	0.714	1.033	0.682	1	0.974
	0.20	0.593	1.022	0.571	1	0.974
3.0	0	0.933	0.983	0.950	1	0.983
	0.05	0.900	1.017	0.884	1	0.983
	0.10	0.811	1.022	0.789	1	0.983
	0.15	0.690	1.011	0.678	1	0.983
	0.20	0.567	1.000	0.567	1	0.983

TABLE 4.4.2.1 (Continued)

R	$\frac{O}{T}$	a_{10}	a_{20}	a_{30}	a_{40}	b
4.0	0	0.956	0.987	0.963	1	0.987
	0.05	0.912	1.015	0.891	1	0.987
	0.10	0.802	1.010	0.786	1	0.987
	0.15	0.675	0.997	0.673	1	0.987
	0.20	0.538	0.993	0.569	1	0.987
5.0	0	0.960	0.988	0.970	1	0.991
	0.05	0.906	1.011	0.893	1	0.991
	0.10	0.785	1.000	0.784	1	0.991
	0.15	0.669	0.993	0.675	1	0.991
	0.20	0.576	0.996	0.578	1	0.991
6.0	0	0.967	0.991	0.975	1	1.0
	0.05	0.906	1.010	0.894	1	1.0
	0.10	0.784	1.000	0.783	1	1.0
	0.15	0.683	0.999	0.683	1	1.0
	0.20	0.594	1.004	0.588	1	1.0
8.0	0	0.975	0.994	0.981	1	1.0
	0.05	0.898	1.005	0.892	1	1.0
	0.10	0.781	0.997	0.784	1	1.0
	0.15	0.689	1.001	0.688	1	1.0
	0.20	0.587	1.000	0.587	1	1.0
∞	0	1.0	1.0	1.0	1.0	1.0
	0.05	0.9	1.0	0.9	1.0	1.0
	0.10	0.8	1.0	0.8	1.0	1.0
	0.15	0.7	1.0	0.7	1.0	1.0
	0.20	0.6	1.0	0.6	1.0	1.0

4.5 SUMMARY DESCRIPTION OF CALCULATED DATA, PREDICTED PERFORMANCE OF THE MSFTP-2 BIT SYNCHRONIZER, AND TEST DATA FOR THE INTEGRATE AND DUMP DETECTOR

4.5.1 General

In this section, the following is presented:

Calculated Data - The degradation which results from DC offsets, pre-filtering (or system bandlimiting), and timing error are shown in a set of parametric curves. From the curves, the degradation can be determined for variable SNR, transition density, and prefiltering bandwidth.

Predicted Performance - Curves are presented which show the predicted performance of the MSFTP-2 bit synchronizer. The curves were drawn by using the calculated curves and the hardware error analyses given in the Appendices. Using the calculated/estimated errors, the degradation is read from the calculated curves.

Test Data - Test data from the MSFTP-2 bit synchronizer is presented for comparison with predicted results.

4.5.2 Calculated Data

4.5.2.1 Performance Degradation Curves of I&D Filter Due to DC Offsets

Figure 4.5.1 shows performance degradation versus DC offset for four signal-to-noise ratios from 9.8 db to 13.5 db (normal operating range). These SNR's correspond to theoretical bit error rates of 10^{-3} and 10^{-6} respectively. In this figure ones and zeros are equally likely.

Figure 4.5.2 shows performance degradation versus SNR for four values of DC offset from 5% to 20% of peak signal amplitude. Again ones and zeros are equally likely.

Figure 4.5.3 shows performance degradation versus likelihood of transmission of ones, for values of DC offset from 5% to 20% of peak signal amplitude. The SNR is 9.8 db.

The following conclusions are drawn regarding the degradation due to DC offset:

- 1) The degradation increases very rapidly as a function of offset for offsets of greater than 5% of peak signal amplitude.
- 2) The degradation increases slightly, at a given DC offset, with increase in SNR, i.e., the degradation with a fixed DC offset is more severe in systems operating at a lower error rate.

4.5.2.2 Performance Degradation Curves of I&D Filter Due to Prefiltering

Figures 4.5.5 through 4.5.16 show the I&D performance degradation due to prefiltering. The degradation increases sharply with decrease in bandwidth. The absolute values of degradation for each filter are close, with the six pole Butterworth and the ideal filter being almost identical. From this it is concluded that degradation due to filtering in the MSFTP-2 system, whatever the equivalent transfer function of the filtering, should closely agree with calculated results so long as the bandwidth is specified.

4.5.2.3 Performance Degradation Curves of I&D Filter Due to Timing Error

The curves of Figures 4.5.17 through 4.5.56 show performance degradation due to timing error. Figure 4.5.17 through 4.5.52 include a six pole Butterworth prefilter and thus show the composite losses due to prefiltering and timing error. Timing error losses, with the prefilter, can be arrived at singly by subtracting the prefiltering loss or the loss with zero timing error from the composite loss with timing error. Figures 4.5.53 through 4.5.56 show the loss due to timing error with no prefiltering.

It will be noted in the curves that degradation due to timing error increases more rapidly as the filter bandwidth is increased. For example, Figure 4.5.25 shows that with filter cut off frequency of 1.5 times the bit rate, 50% transition density, and zero timing error, the prefilter loss is approximately 0.4 db. Addition of timing error of 10% of a bit period increases the degradation to approximately 1.1 db, thus the timing error loss is 0.7 db. Figure 4.5.53 shows that for identical conditions,

except that the prefilter has infinite bandwidth, the loss with timing error of 10% of a bit period is approximately 1.3 db. Thus, with 10% timing error, the prefilter improves the overall performance by approximately 0.2 db. This is shown in Figure 4.5.57 which shows degradation versus filter cut off frequency for several values of timing error. So long as the timing error is small, the best performance is obtained with square wave data (large cut off frequency). For large timing error, however, slight improvement results from some values of prefiltering.

4.5.3 Predicted Performance Results of MSFN Bit Synchronizer, 1&D Filter

Figures 4.5.58 through 4.5.67 show predicted performance losses for the MSFTP-2 bit synchronizer for transition densities of 50% and 100%, for prefilter cut off frequencies of 0.5, 1.0, 1.5, and 2.0 times the bit rate, and for infinite bandwidth ($R = \infty$). The transition densities and cut off frequencies listed above were also used in the test measurements.

The curves show the following:

- 1) Theoretical performance
- 2) Loss due to composite DC offset
- 3) Loss due to prefiltering and timing error
- 4) Total loss due to DC offset, prefiltering, and timing error
[sum of (2) and (3)]
- 5) Nominal predicted performance
- 6) Worst case predicted performance

Curves 2 and 3 above were drawn by applying the results of the hardware error analyses to the general curves of degradation for DC offset and prefiltering and timing error. The DC error analysis of Appendix B yields an estimated composite DC offset of 8% of peak signal amplitude. The timing error analysis of Appendix D yields an estimated timing error of 9% and 10% of a bit period for transition densities of 100% and 50% respectively. The final nominal and worst case curves, (5) and (6) above, were drawn by adding 0.5 db to the predicted curves to account for omissions and errors in assumptions and adding an additional 0.5 db to account for measurement accuracies.

4.5.4 Test Data from MSFTP-2 Bit Synchronizer

Figures 4.5.68 through 4.5.73 show measured performance of the MSFTP-2 bit synchronizer. The curves are plotted from test data taken by NASA/MS.

Figures 4.5.68 through 4.5.72 show measured error rate versus SNR. Also shown is the nominal and worst case calculated performance. The data for these curves were taken by applying unfiltered PCM data to the MSFTP-2 bit synchronizer through a variable bandwidth filter and measuring error rate versus SNR for various filter bandwidths.

Figure 4.5.73 shows measured performance degradation with incremental DC offset applied to the input PCM data with the baseline offset correction circuitry disabled. No prefiltering was used in this test.

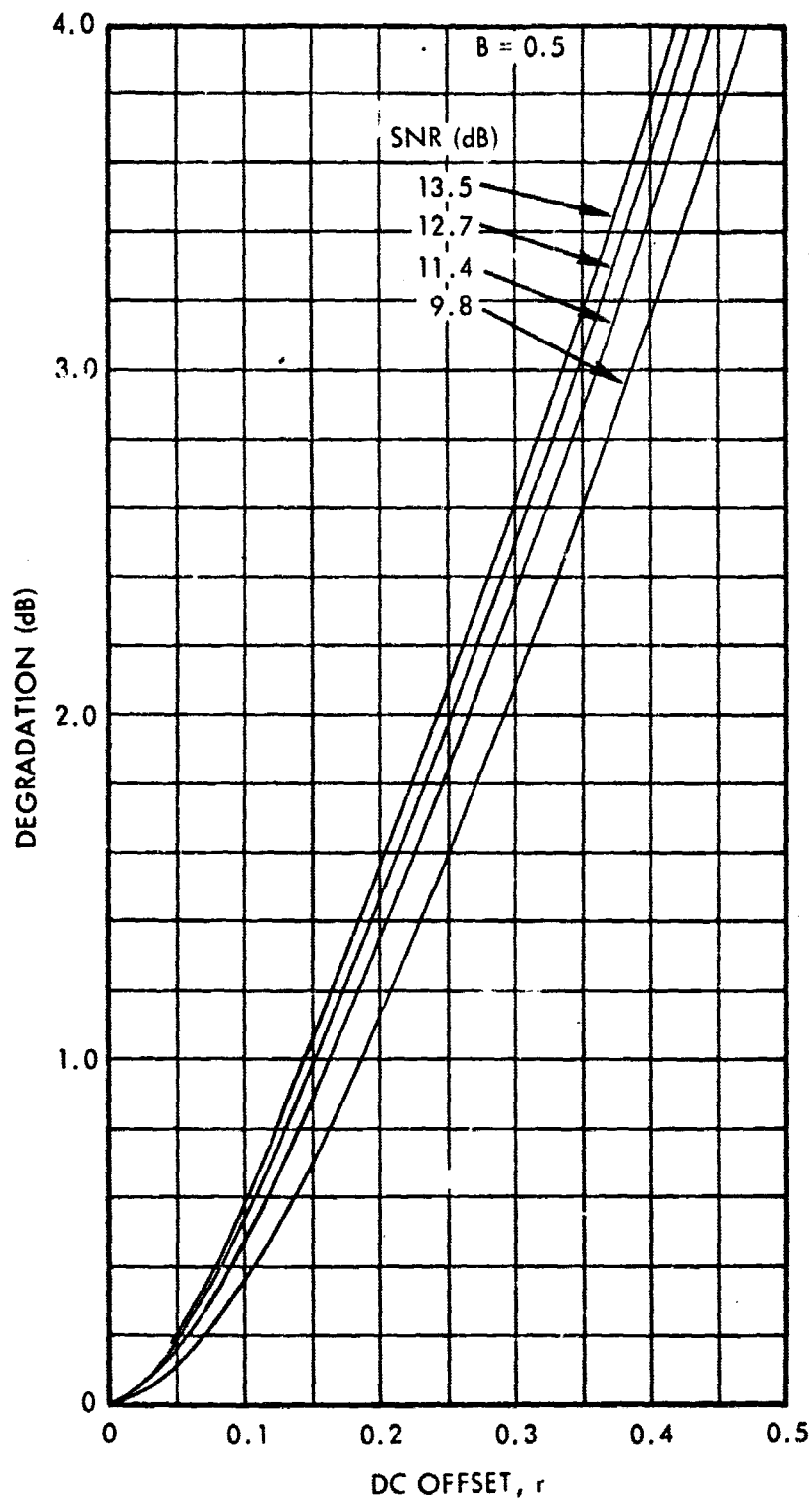


Figure 4.5.1a Performance Degradation Versus DC Offset

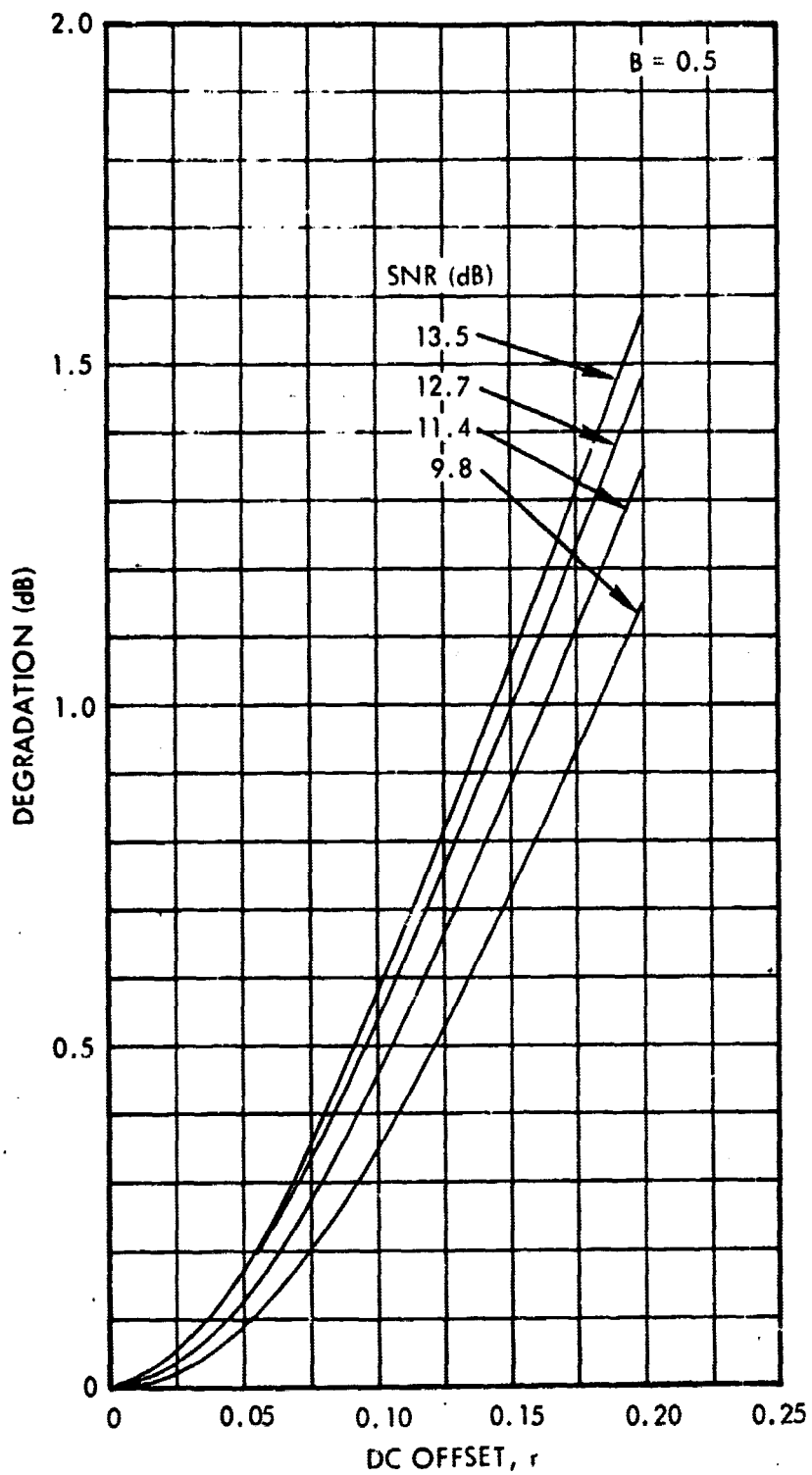


Figure 4.5.1b Performance Degradation versus DC Offset

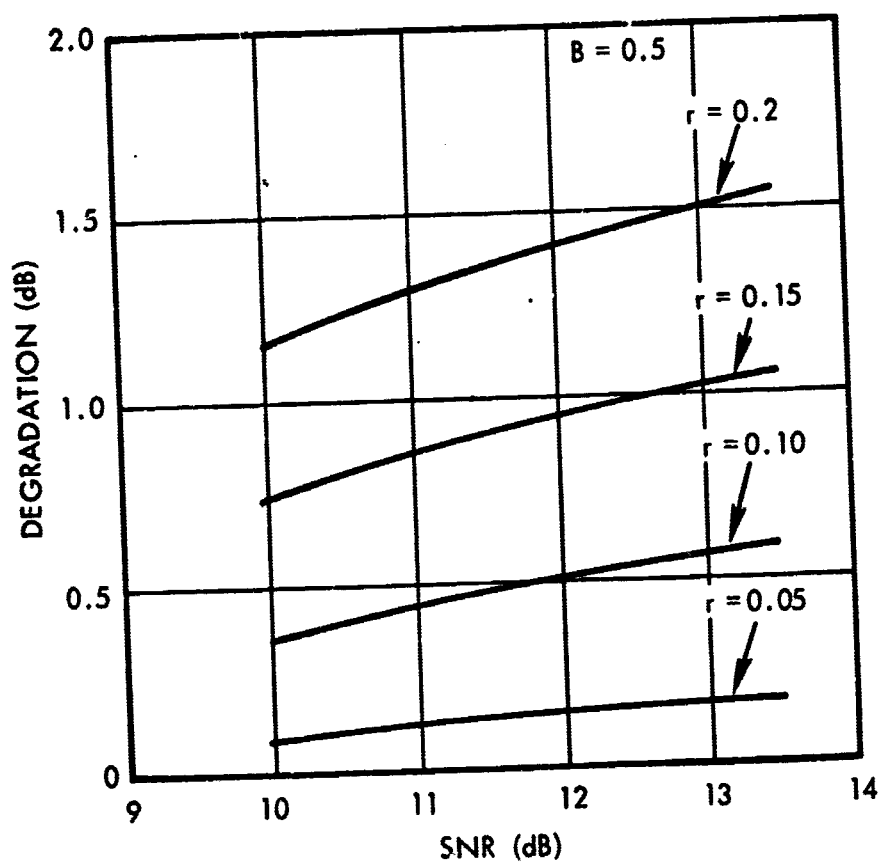


Figure 4.5.2 Performance Degradation due to DC Offsets Versus Signal-to-Noise Ratio

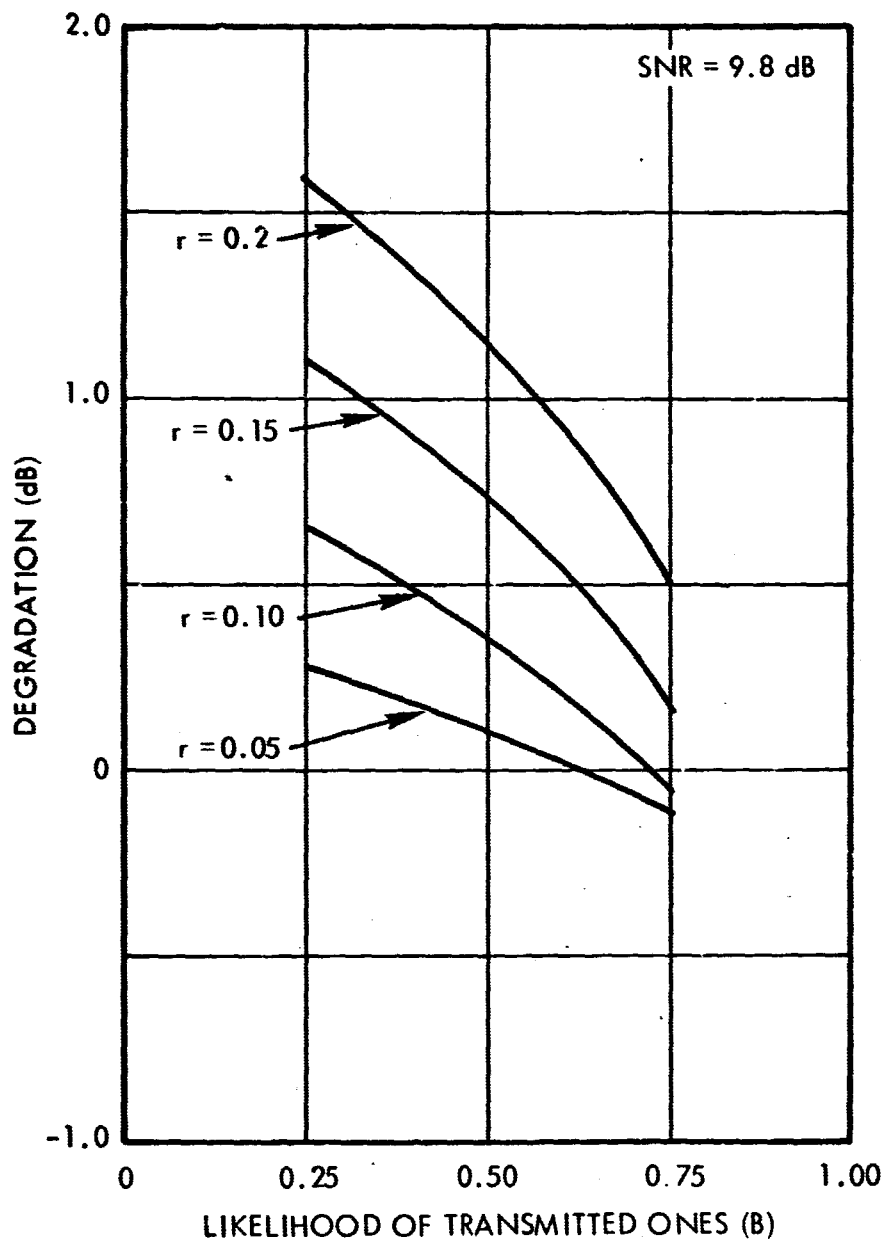


Figure 4.5.3 Performance Degradation due to DC Offsets Versus Likelihood of Transmitted Ones

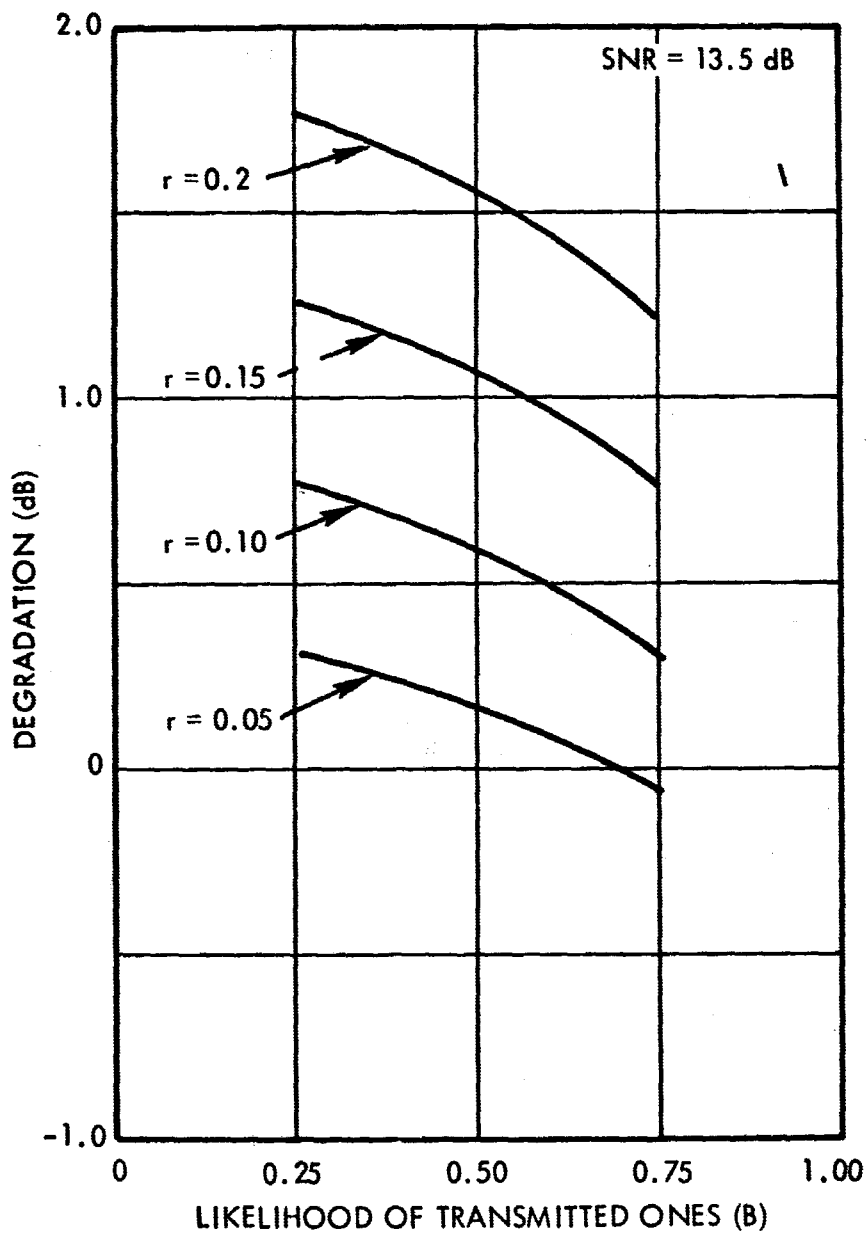


Figure 4.5.4 Performance Degradation due to DC Offsets Versus Likelihood of Transmitted Ones

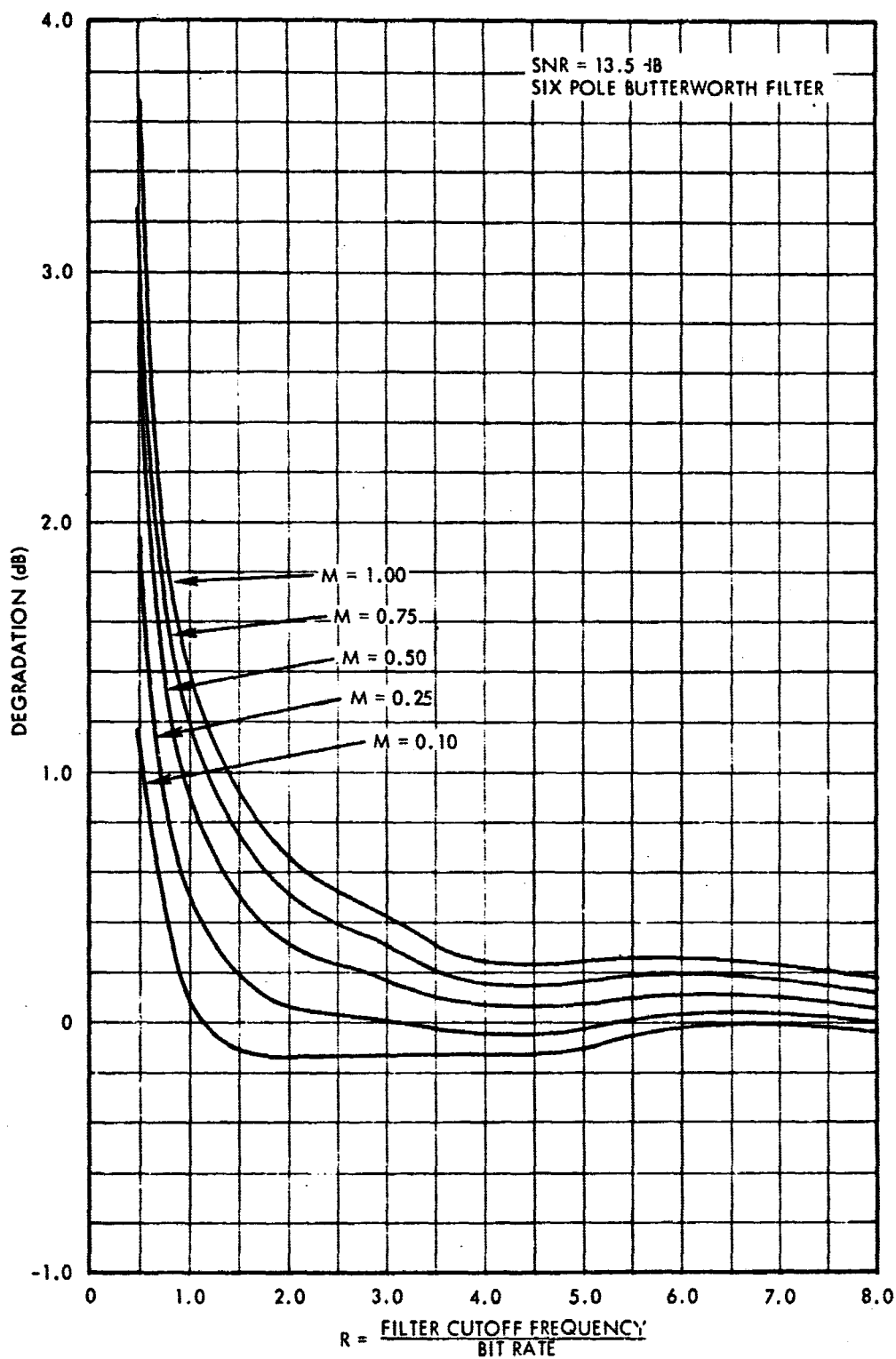


Figure 4.5.5 Performance Degradation due to Prefiltering Versus Prefilter Bandwidth, Integrate and Dump Bit Detector

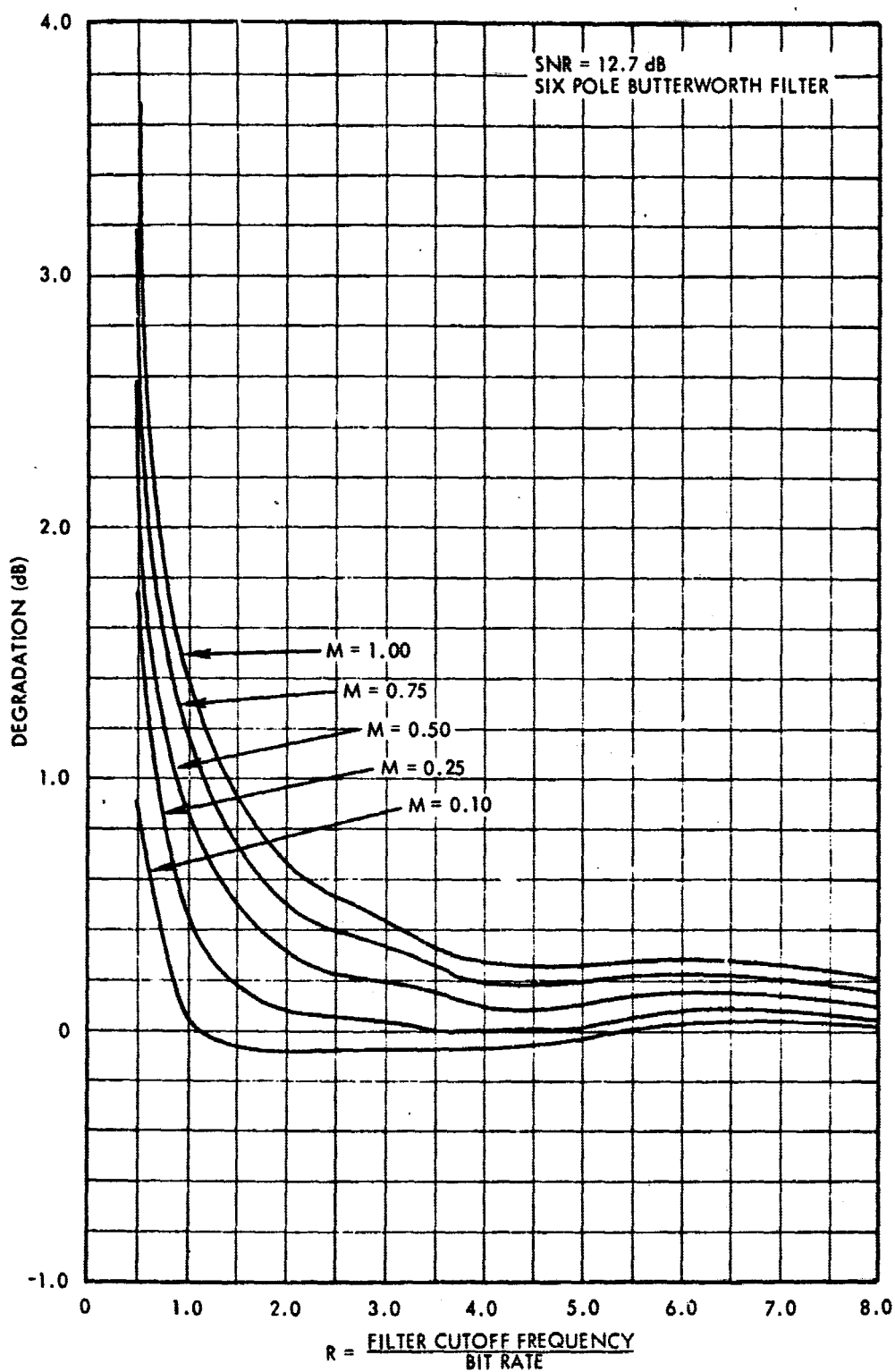


Figure 4.5.6 Performance Degradation due to Prefiltering Versus Prefilter Bandwidth, Integrate and Dump Bit Detector

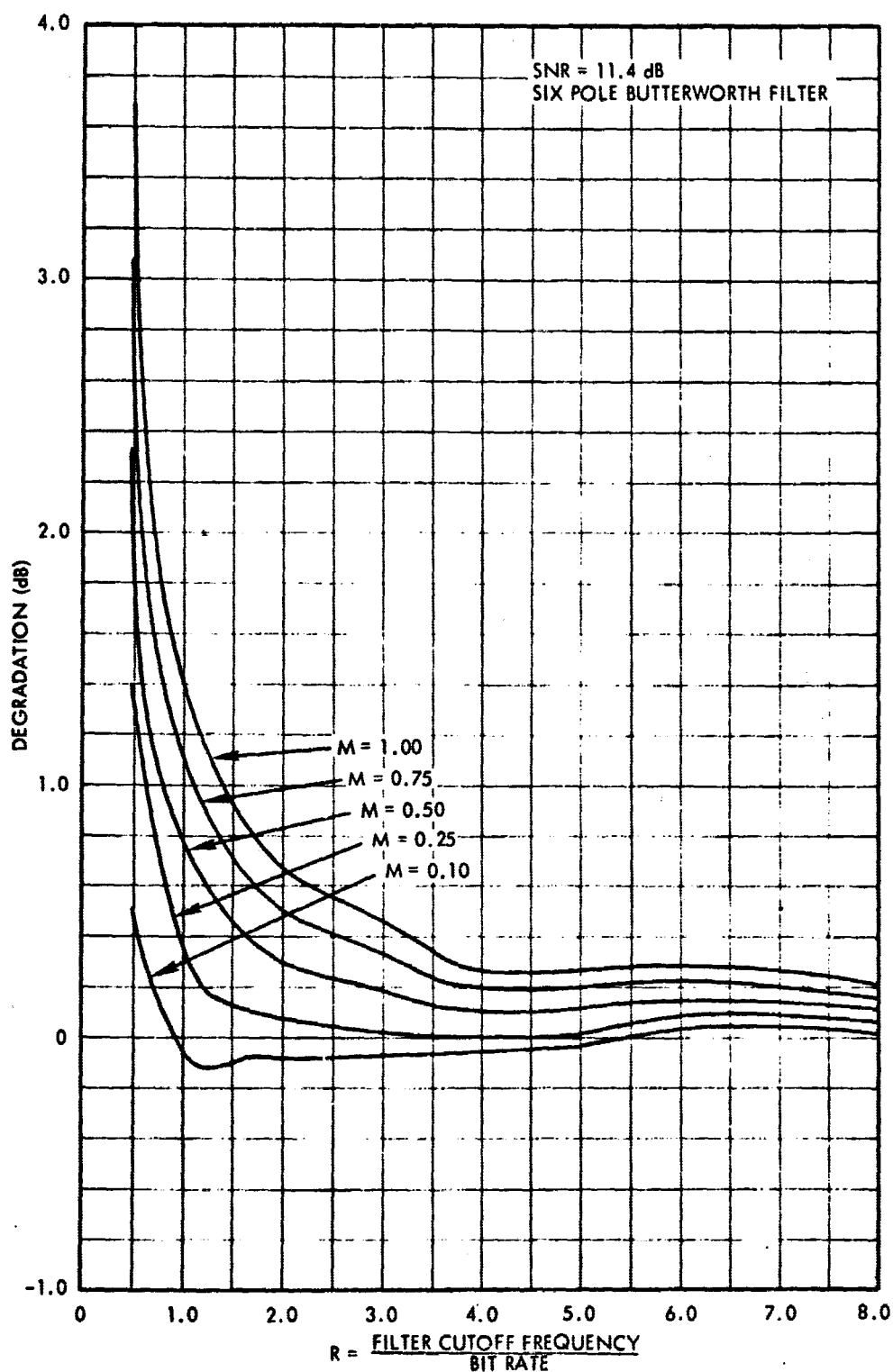


Figure 4.5.7 Performance Degradation due to Prefiltering Versus Prefilter Bandwidth, Integrate and Dump Bit Detector

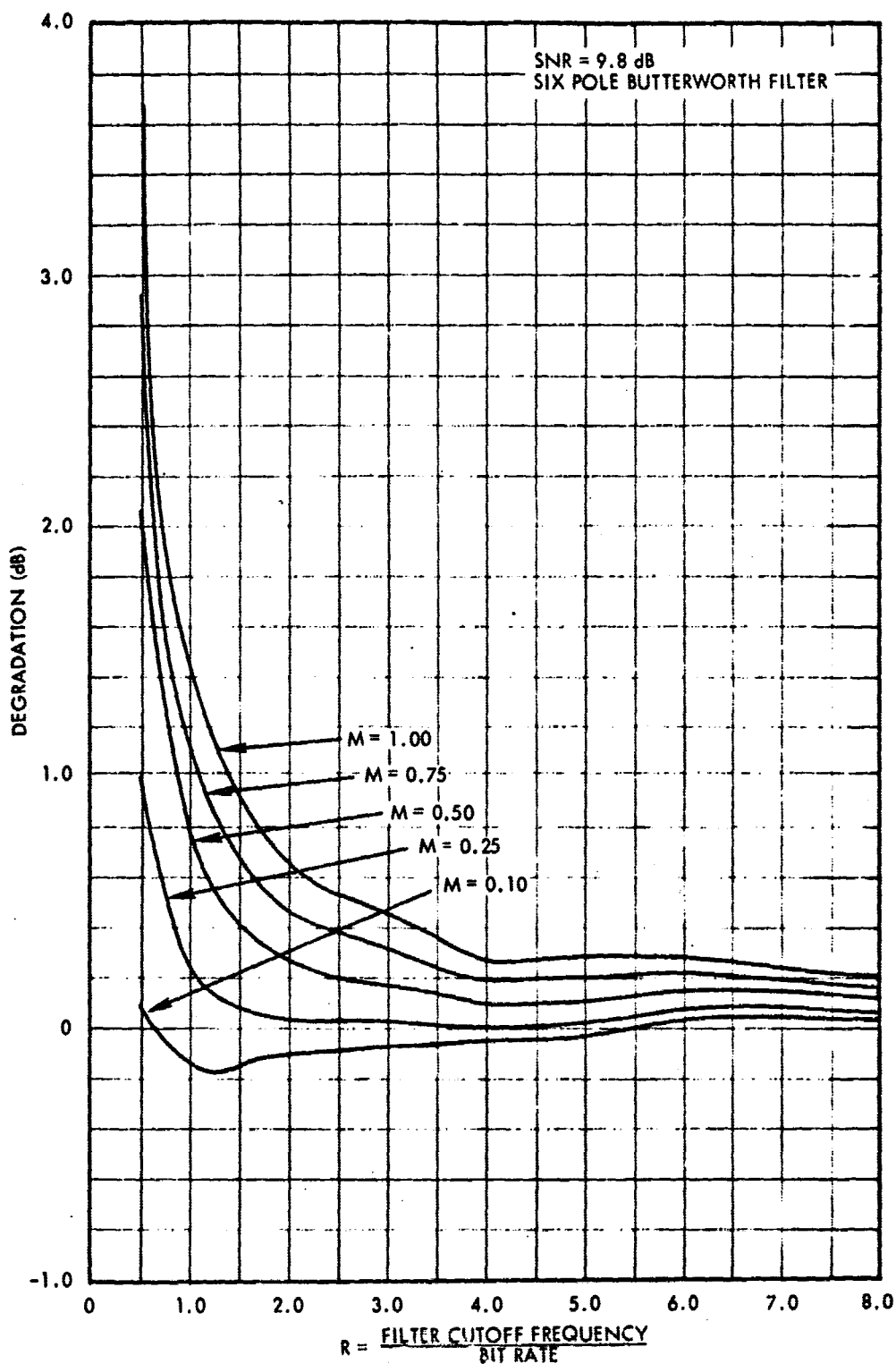


Figure 4.5.8 Performance Degradation due to Prefiltering Versus Prefilter Bandwidth, Integrate and Dump Bit Detector

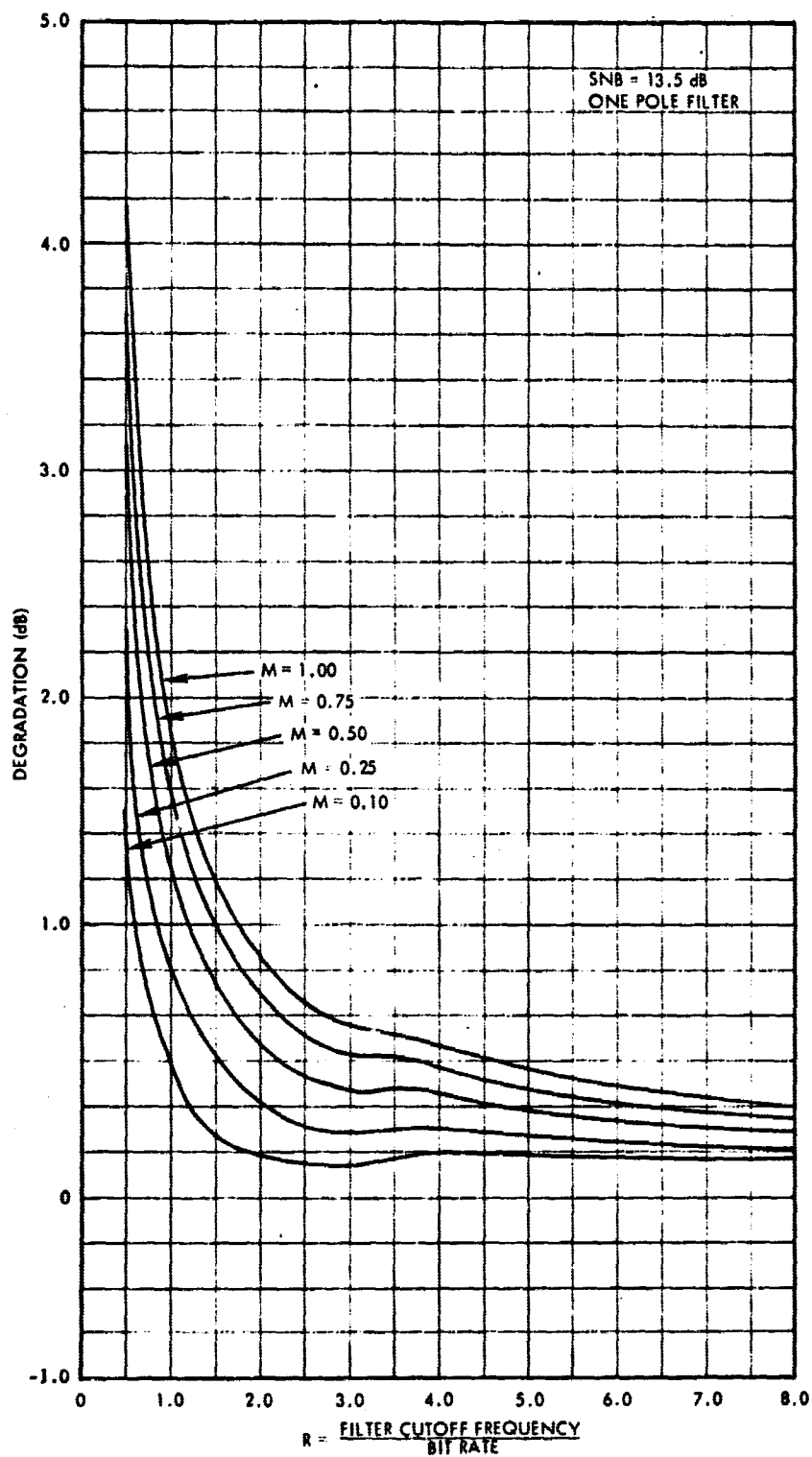


Figure 4.5.9 Performance Degradation due to Prefiltering Versus Prefilter Bandwidth, Integrate and Dump Bit Detector

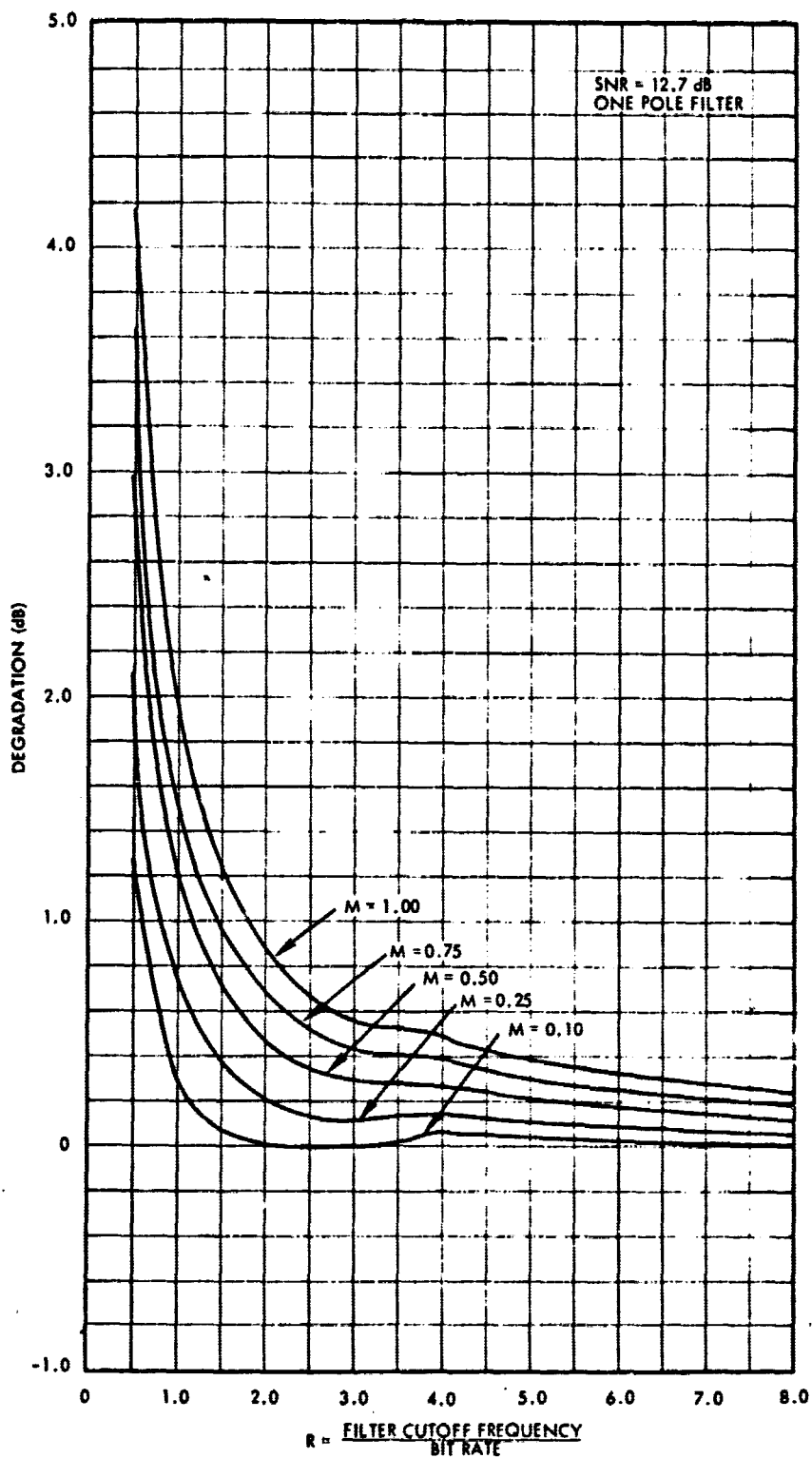


Figure 4.5.10 Performance Degradation due to Prefiltering Versus Prefilter Bandwidth, Integrate and Dump Bit Detector

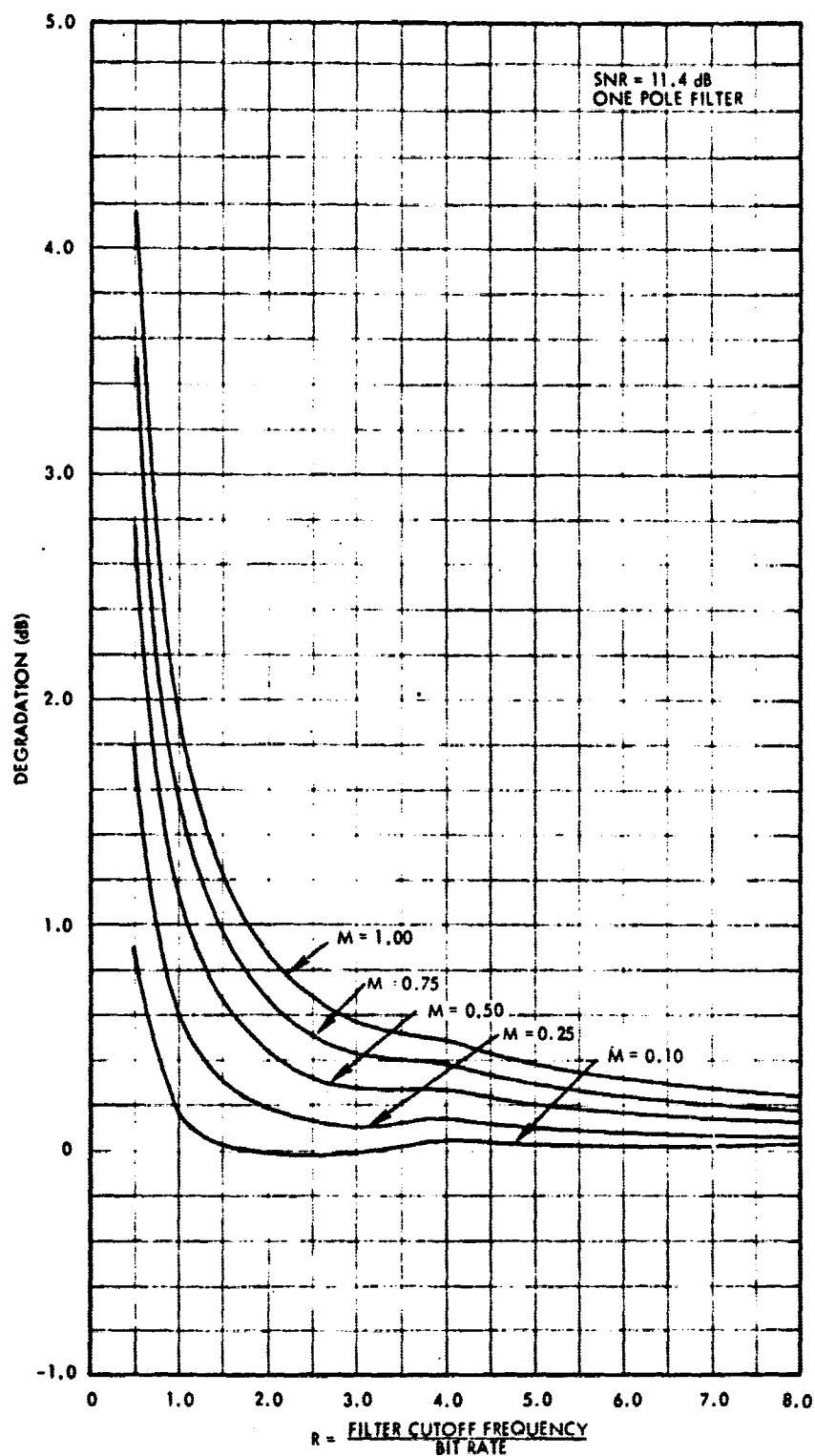


Figure 4.5.11 Performance Degradation due to Prefiltering Versus Prefilter Bandwidth, Integrate and Dump Bit Detector

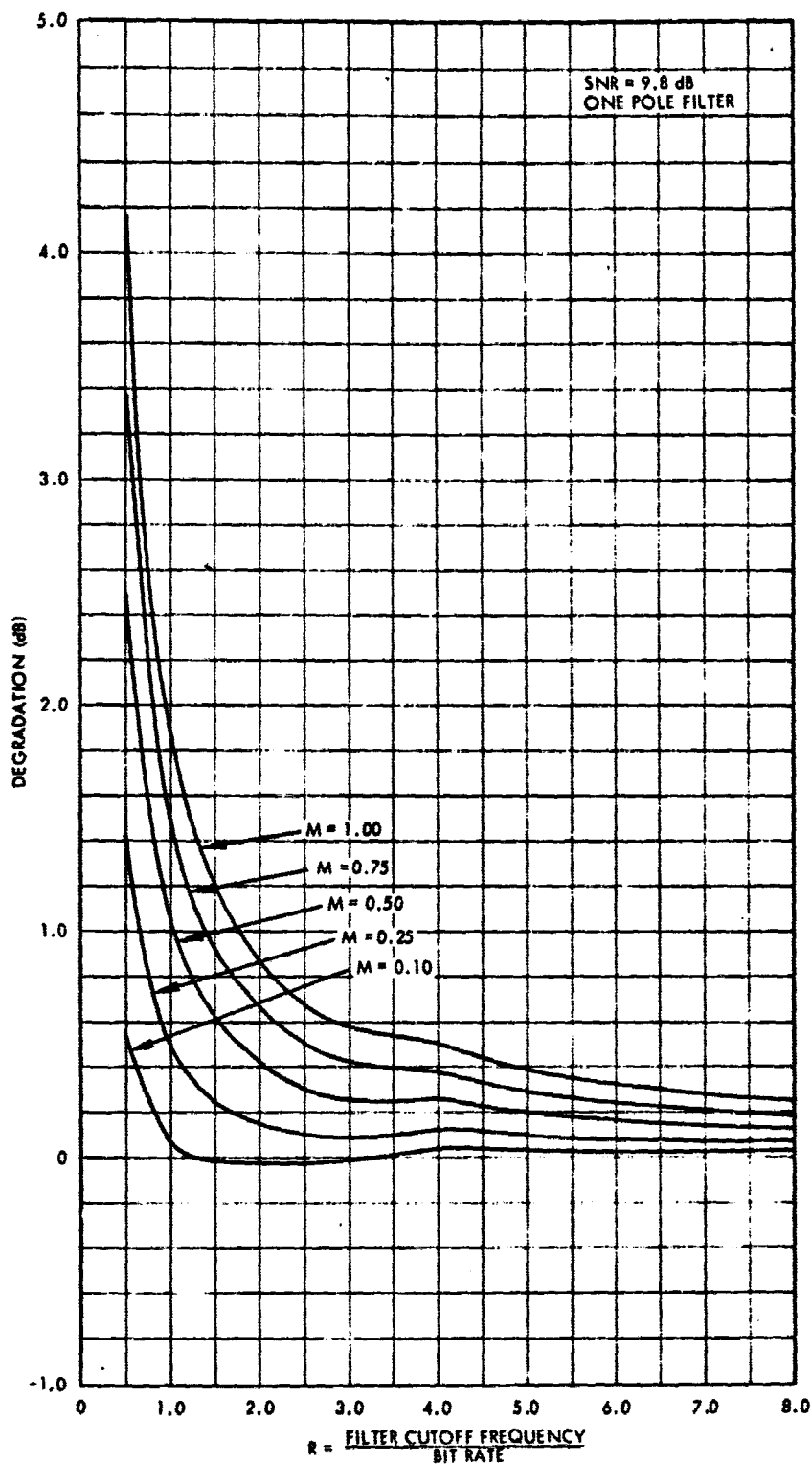


Figure 4.5.12 Performance Degradation due to Prefiltering Versus Prefilter Bandwidth, Integrate and Dump Bit Detector

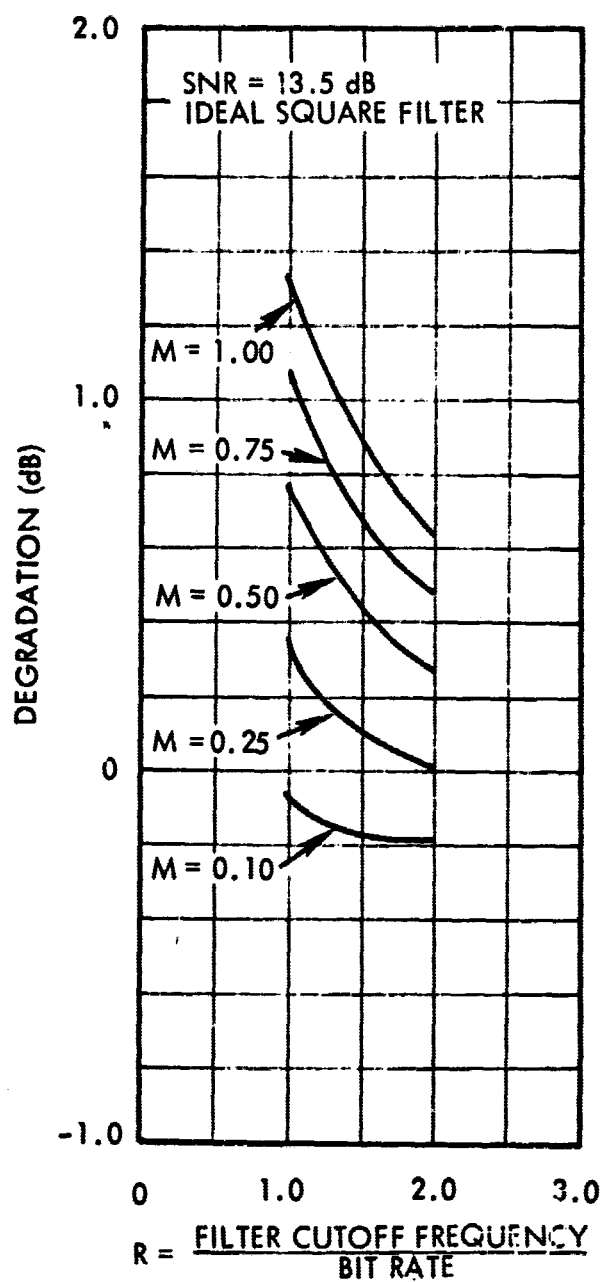


Figure 4.5.13 Performance Degradation Versus Prefilter Cut off Frequency

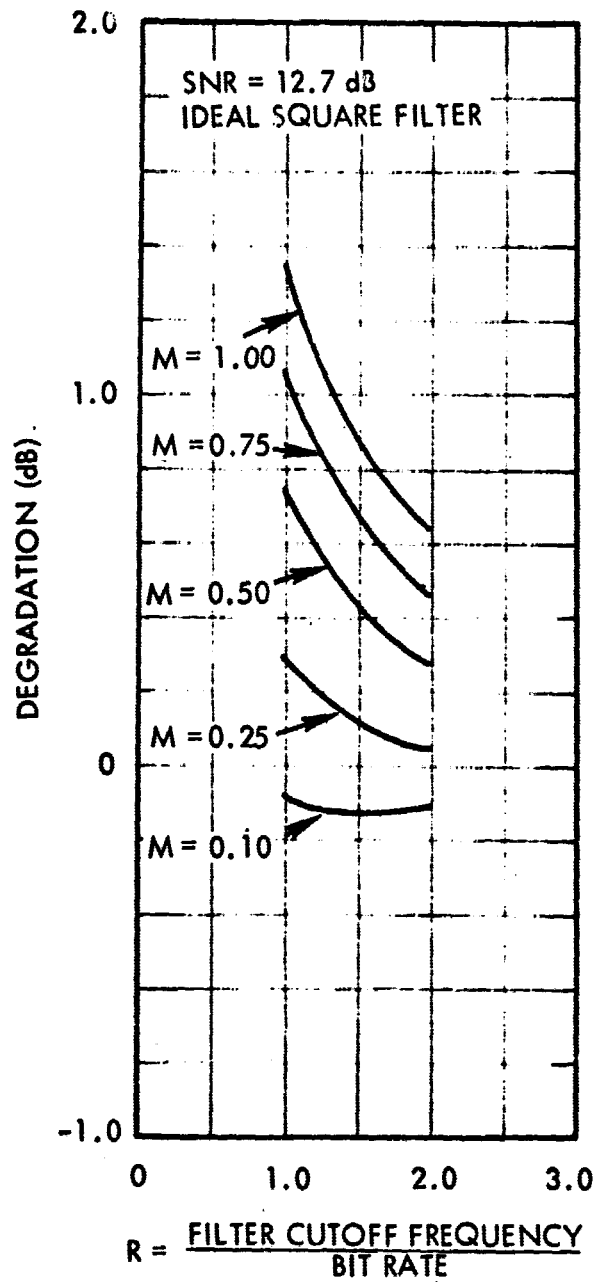


Figure 4.5.14 Performance Degradation Versus Prefilter Cut Off Frequency

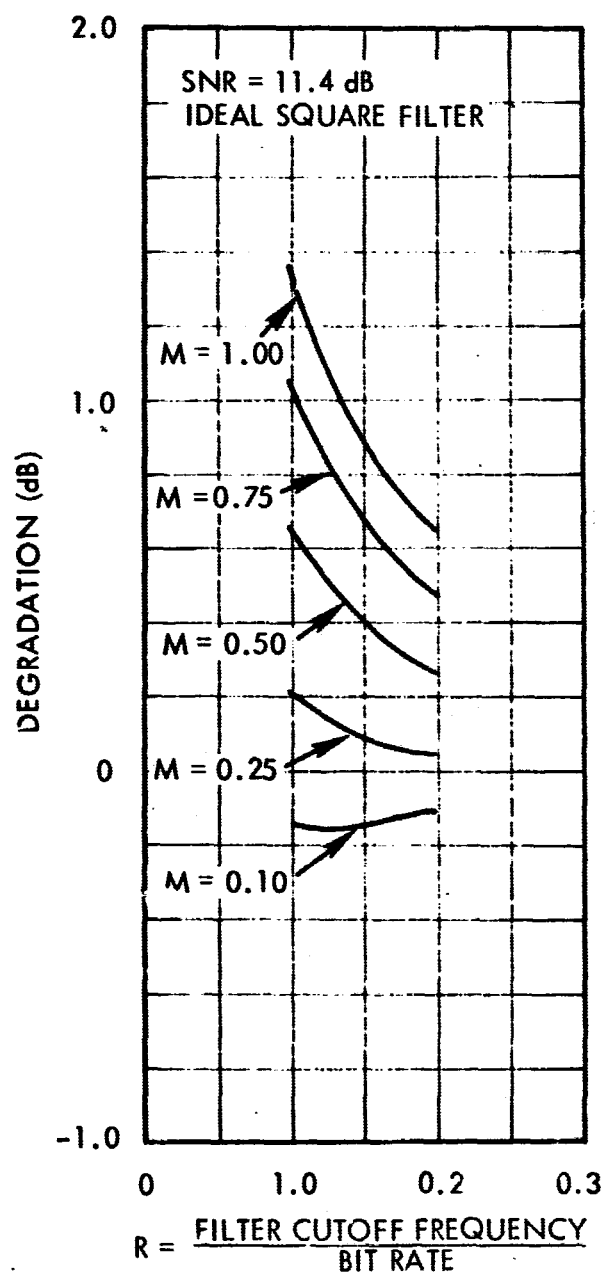


Figure 4.5.15 Performance Degradation Versus Prefilter Cut Off Frequency

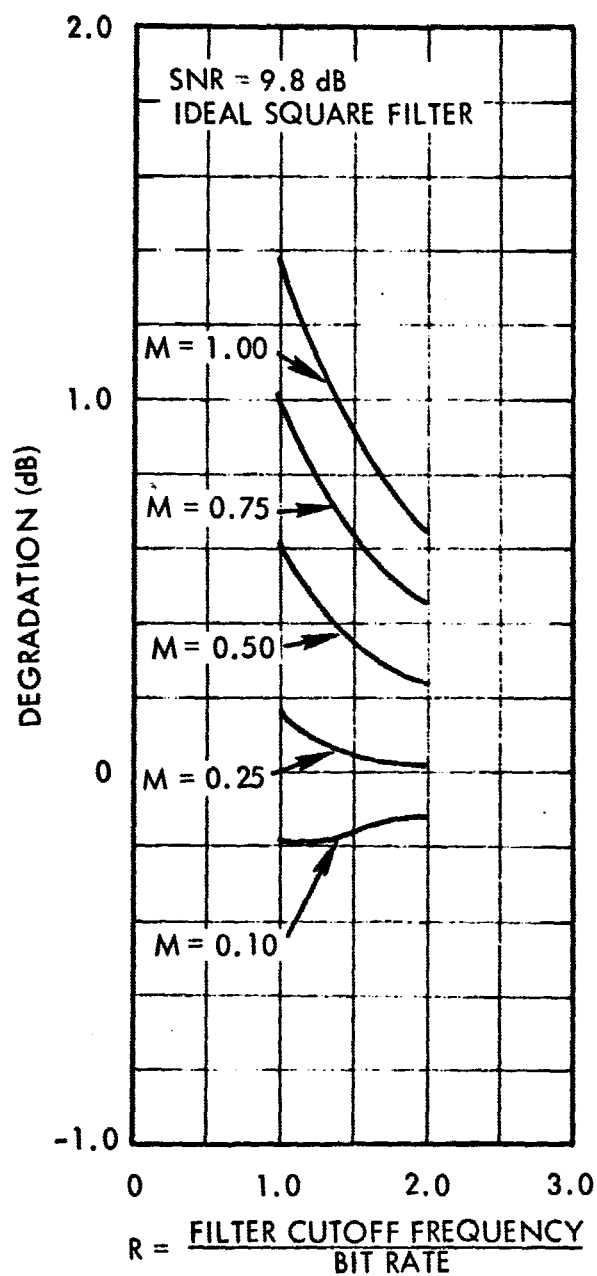


Figure 4.5.16 Performance Degradation Versus Prefilter Cut Off Frequency

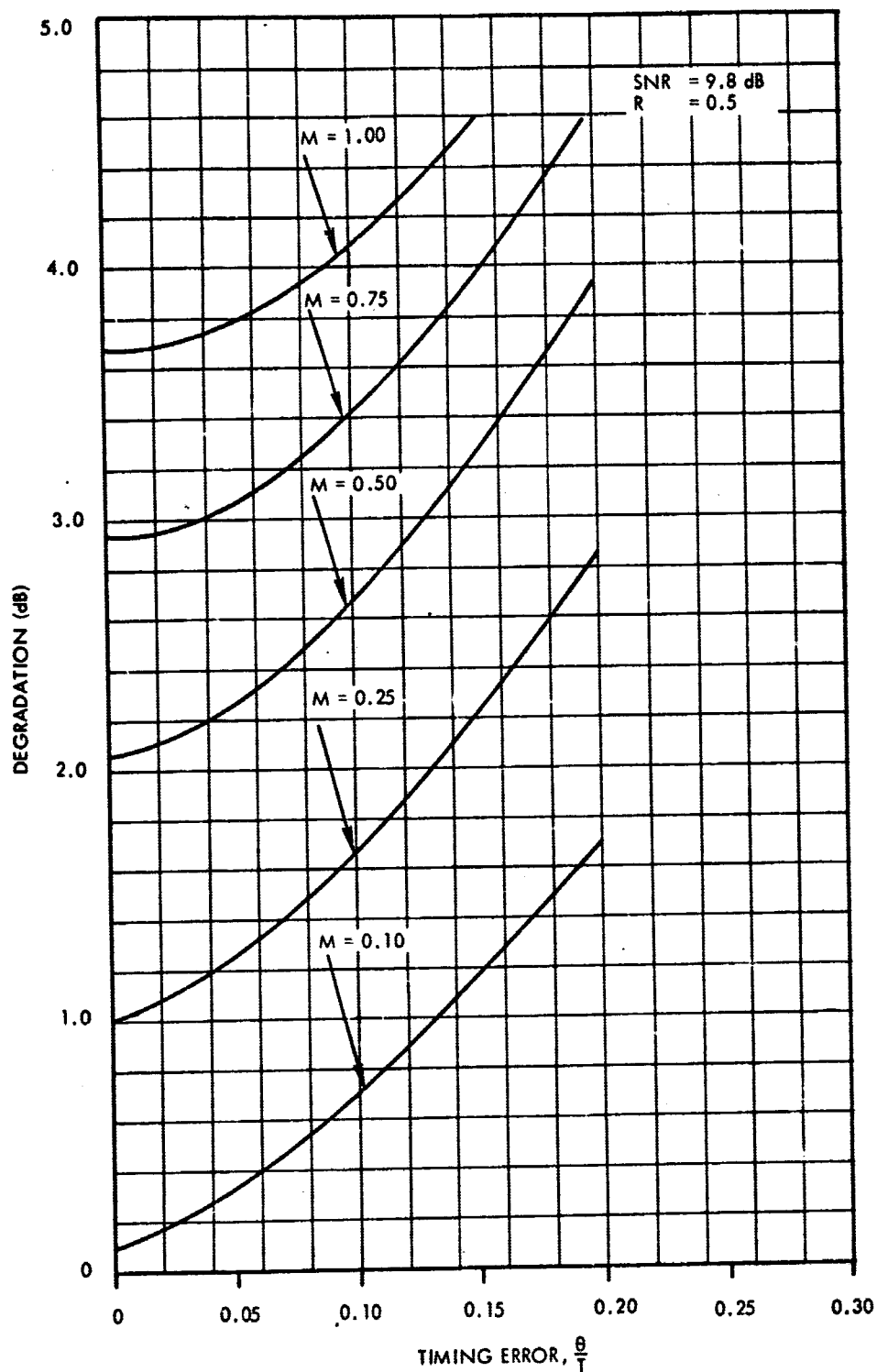


Figure 4.5.17 Performance Degradation Versus Timing Error, Integrate and Dump Bit Detector

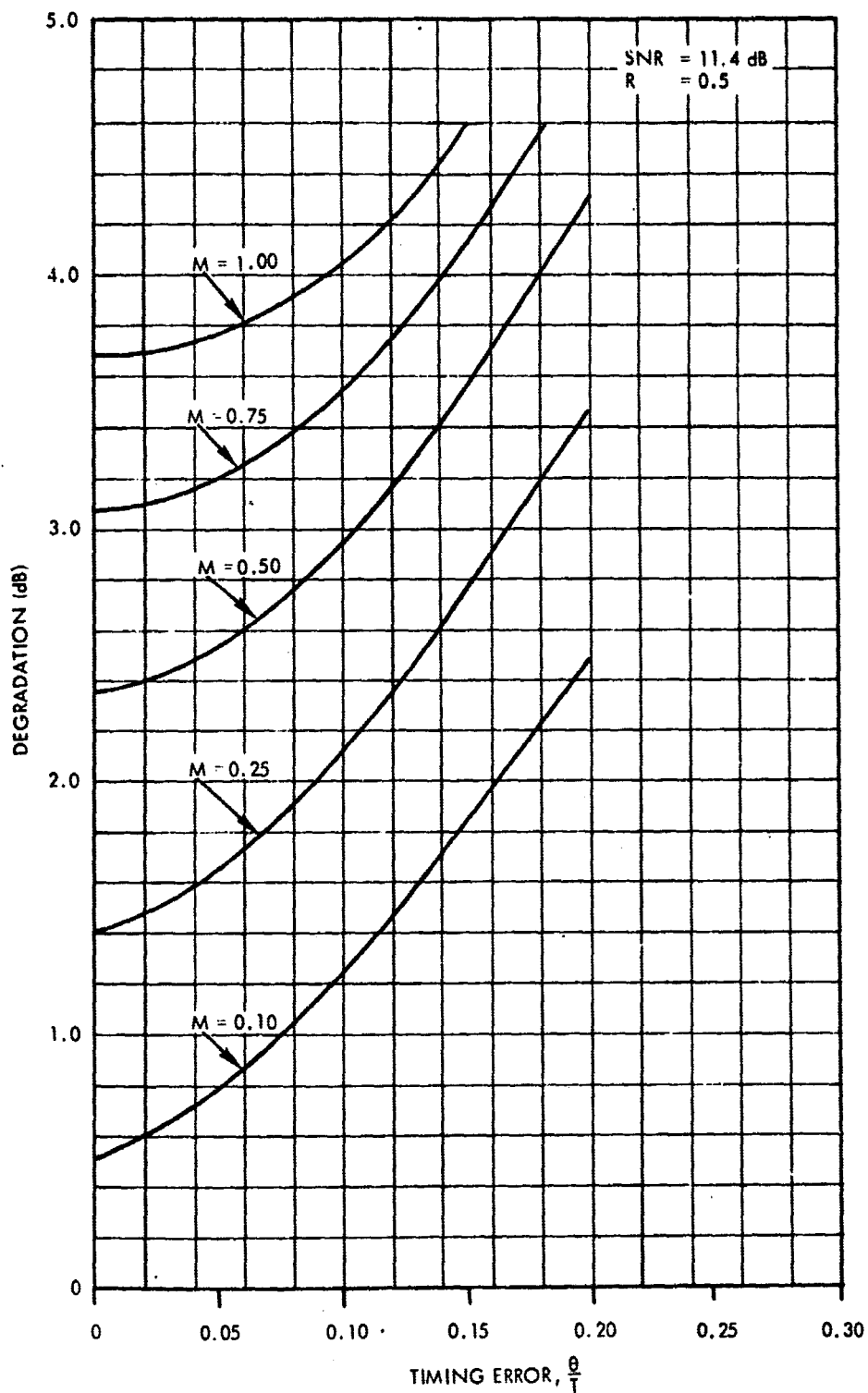


Figure 4.5.18 Performance Degradation Versus Timing Error, Integrate and Dump Bit Detector

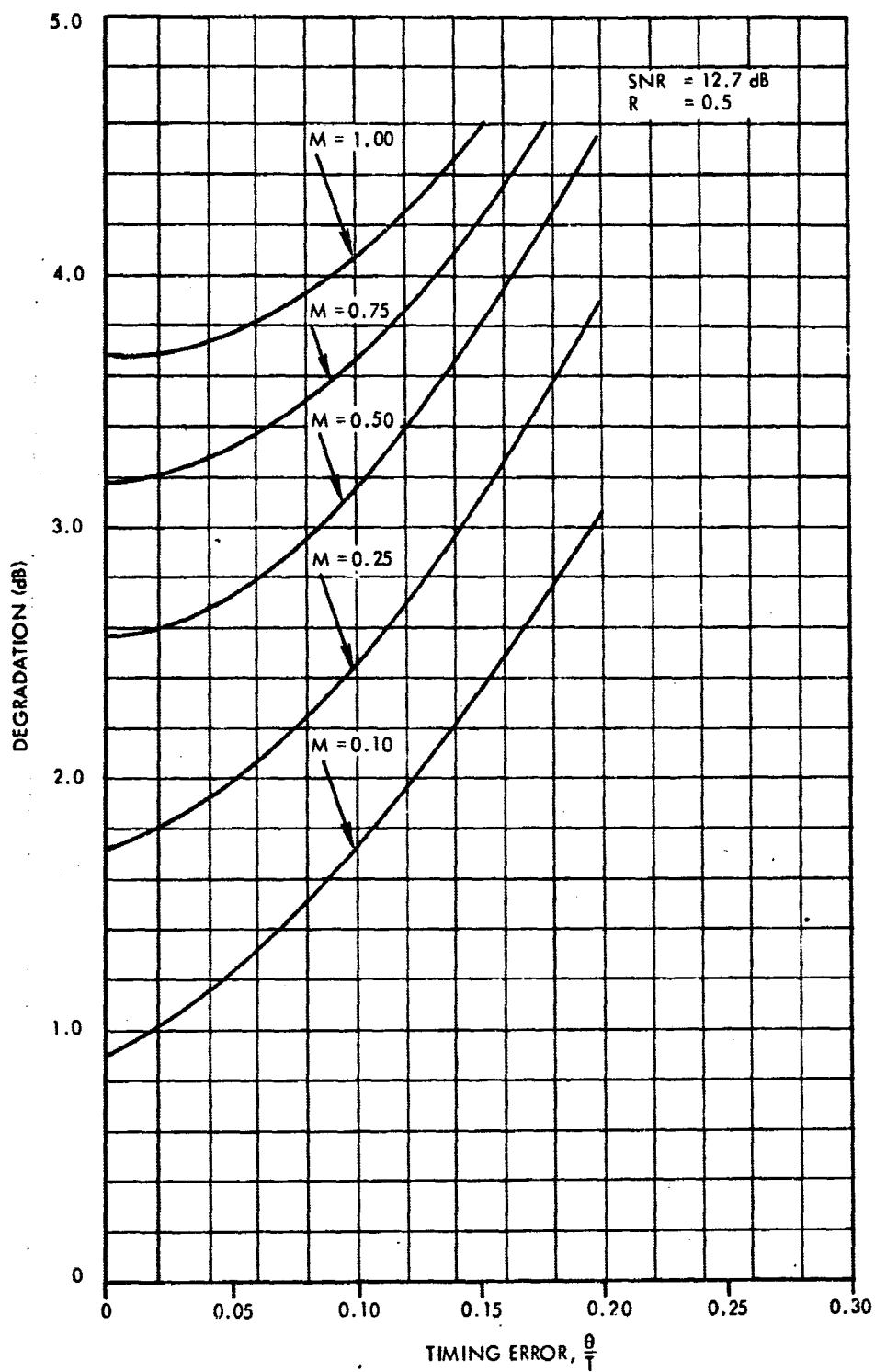


Figure 4.5.19 Performance Degradation Versus Timing Error, Integrate and Dump Bit Detector

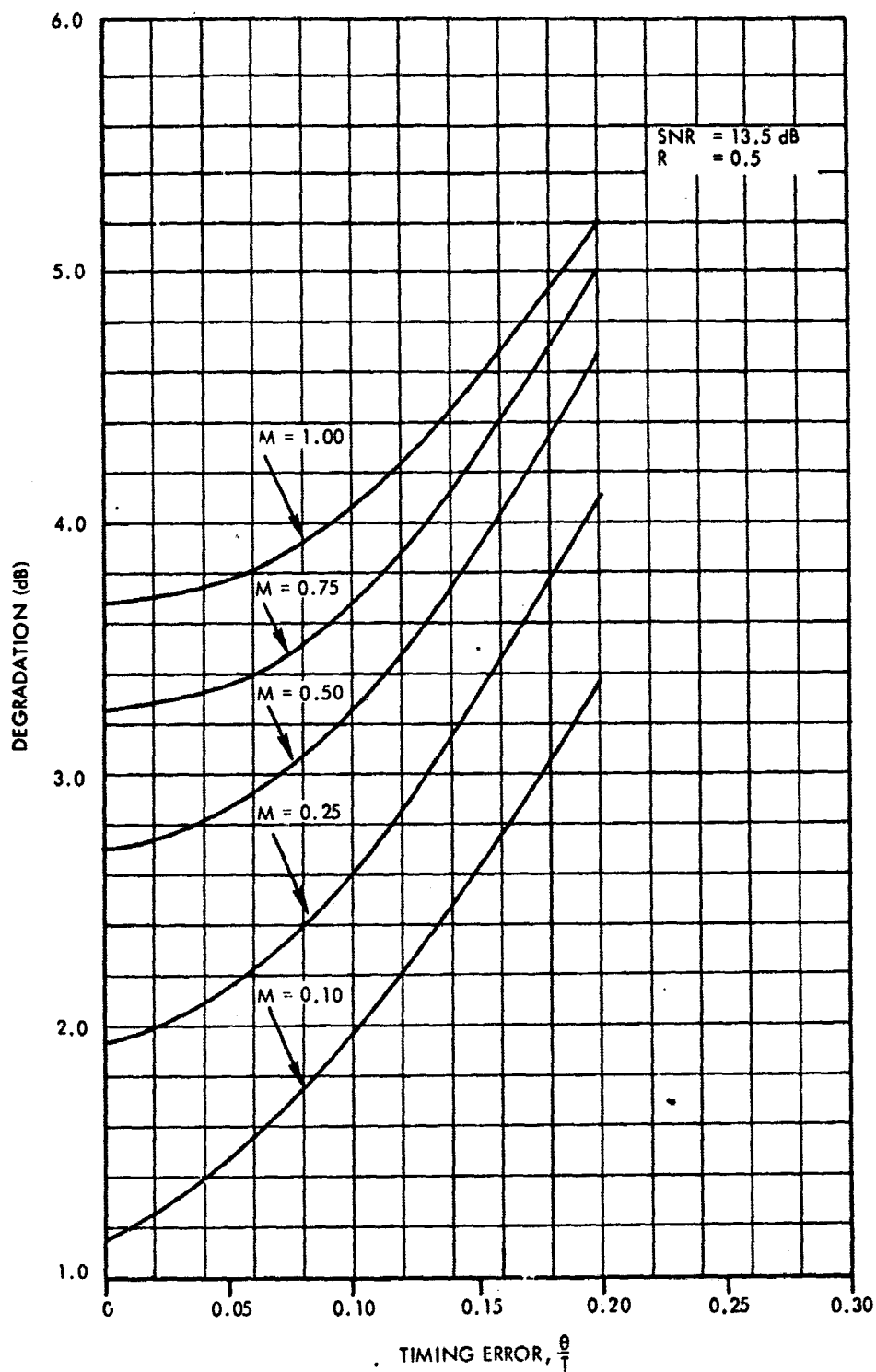


Figure 4.5.20 Performance Degradation Versus Timing Error, Integrate and Dump Bit Detector

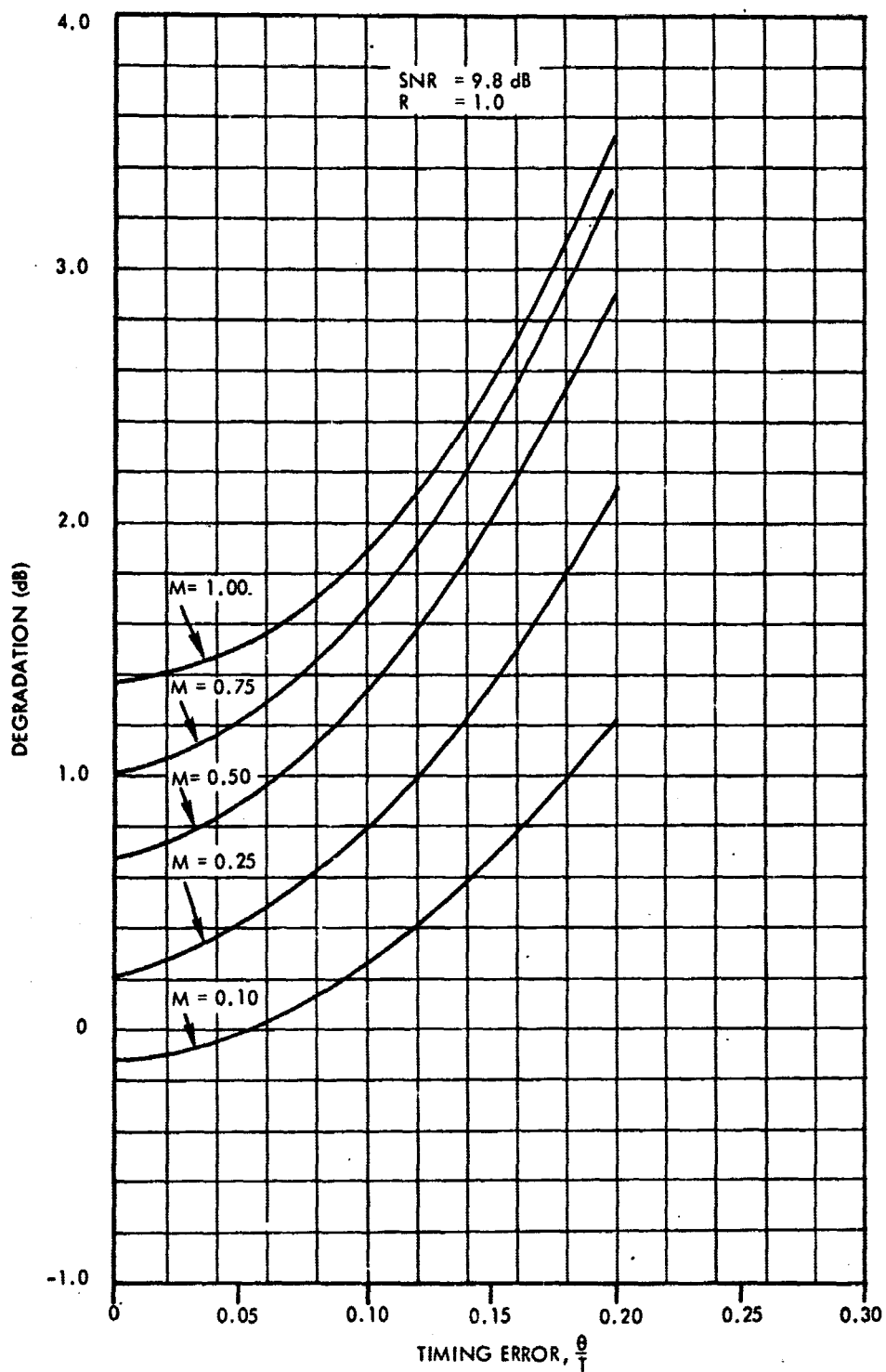


Figure 4.5.21 Performance Degradation Versus Timing Error, Integrate and Dump Bit Detector

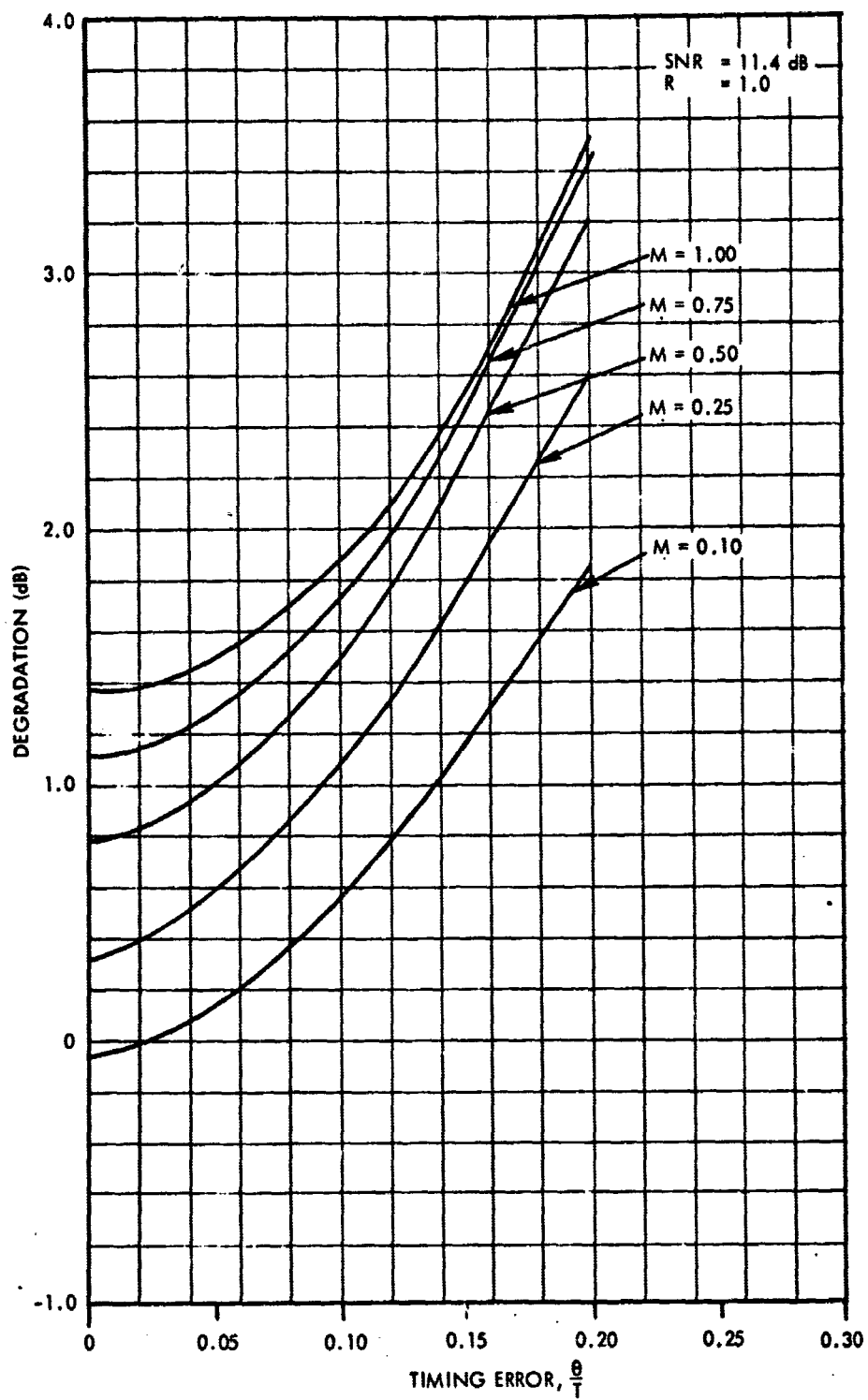


Figure 4.5.22 Performance Degradation Versus Timing Error, Integrate and Dump Bit Detector

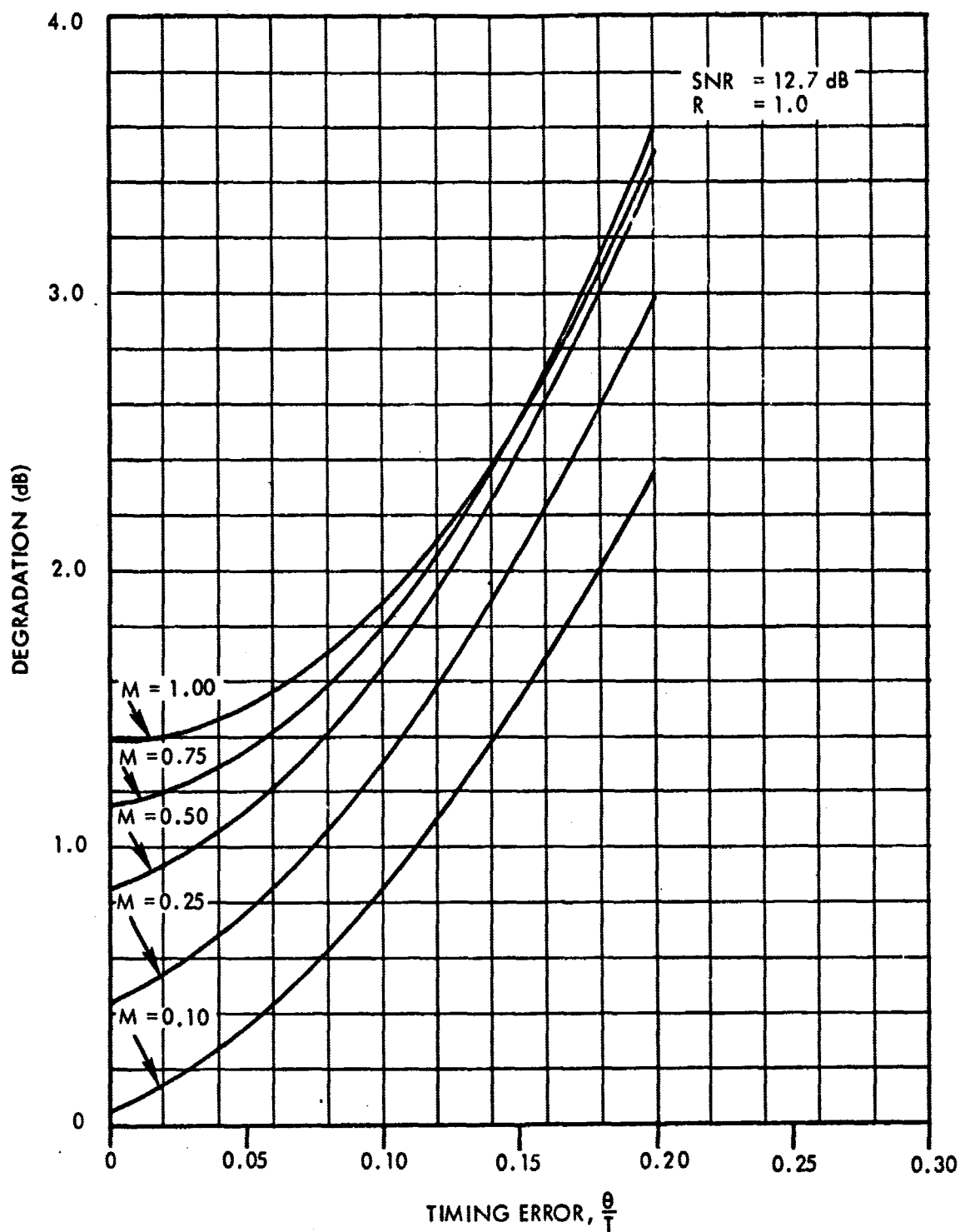


Figure 4.5.23 Performance Degradation Versus Timing Error, Integrate and Dump Bit Detector

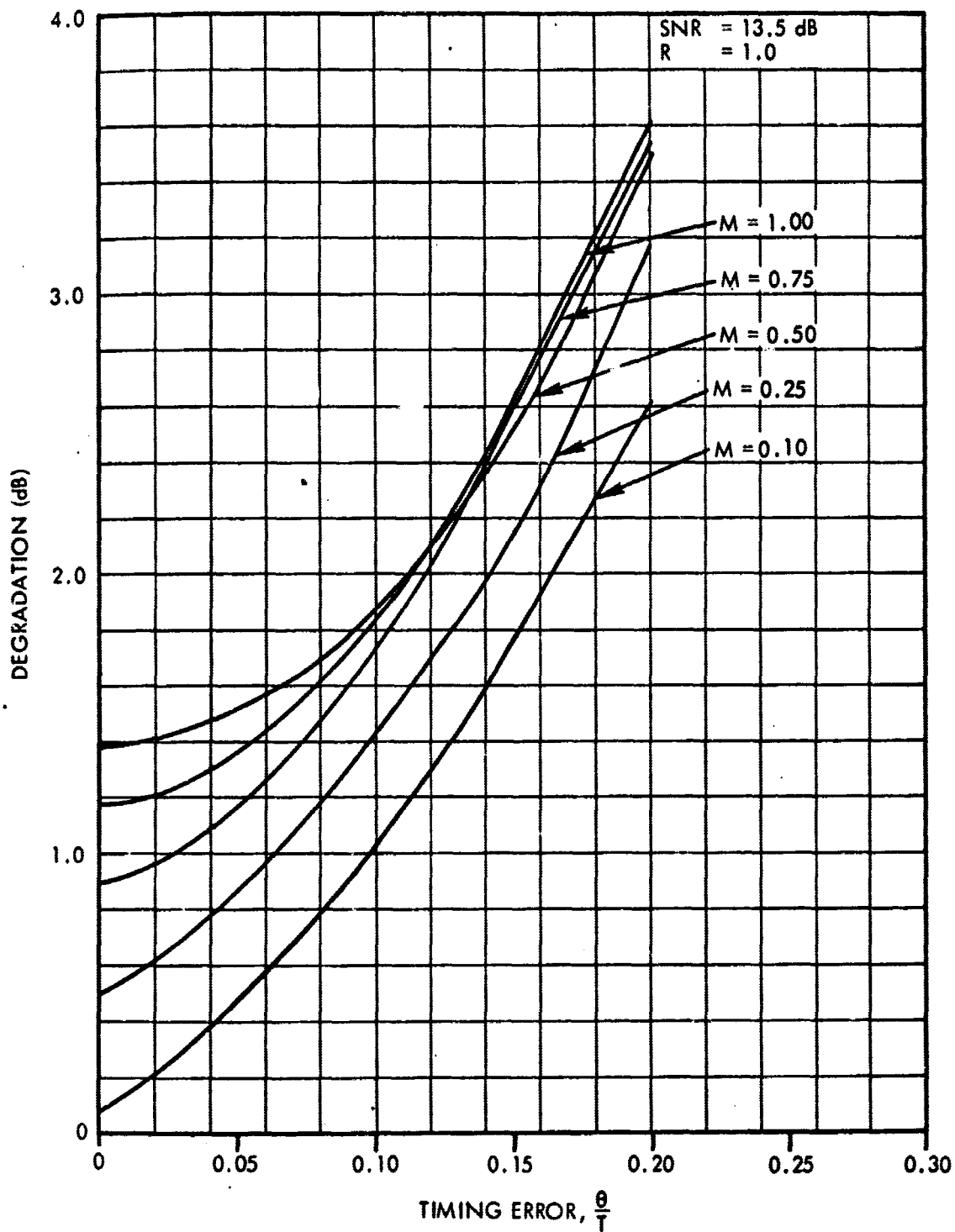


Figure 4.5.24 Performance Degradation Versus Timing Error; Integrate and Dump Bit Detector

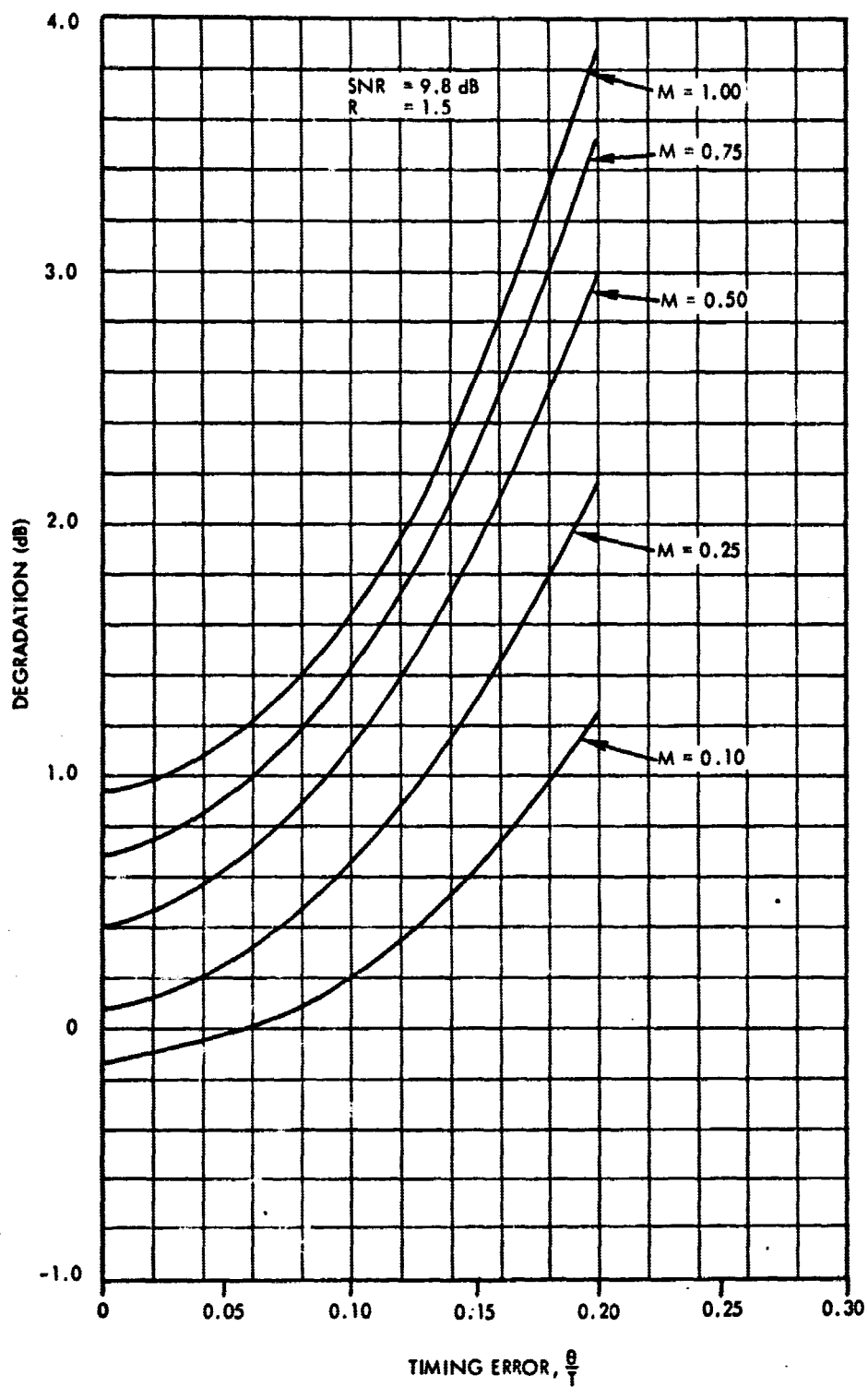


Figure 4.5.25 Performance Degradation Versus Timing Error, Integrate and Dump Bit Detector

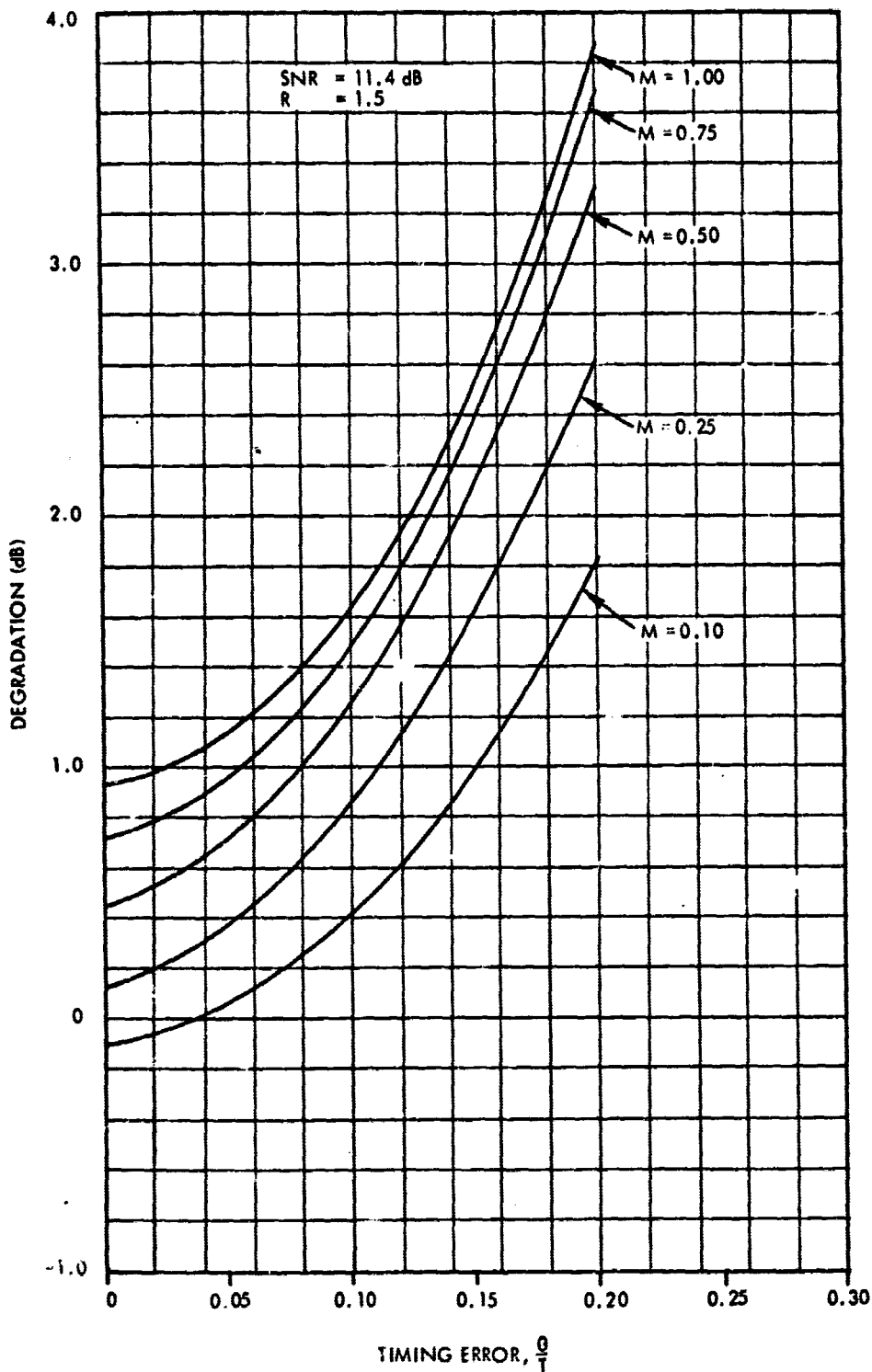


Figure 4.5.26 Performance Degradation Versus Timing Error, Integrate and Dump Bit Detector

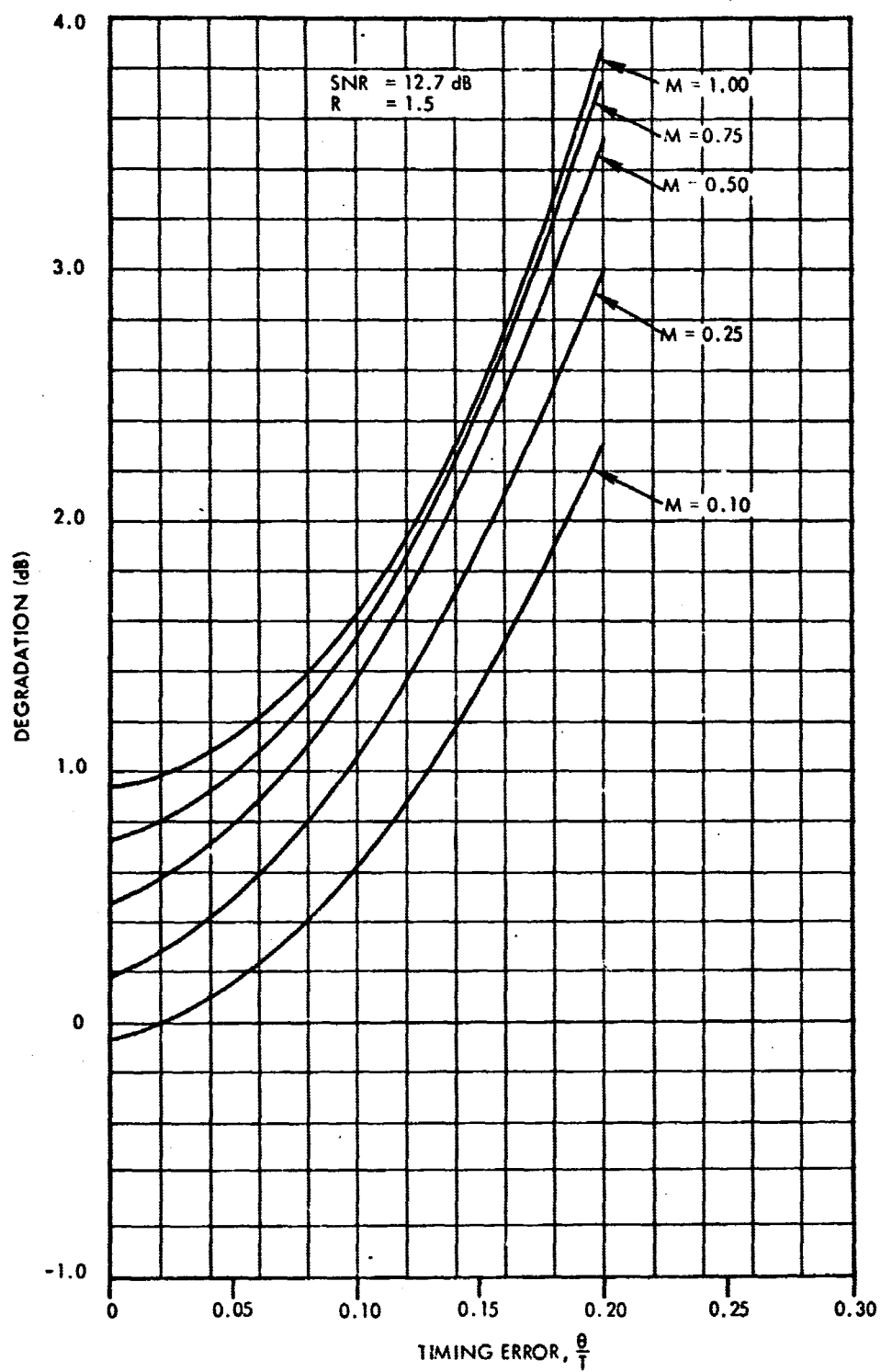


Figure 4.5.27 Performance Degradation Versus Timing Error, Integrate and Dump Bit Detector

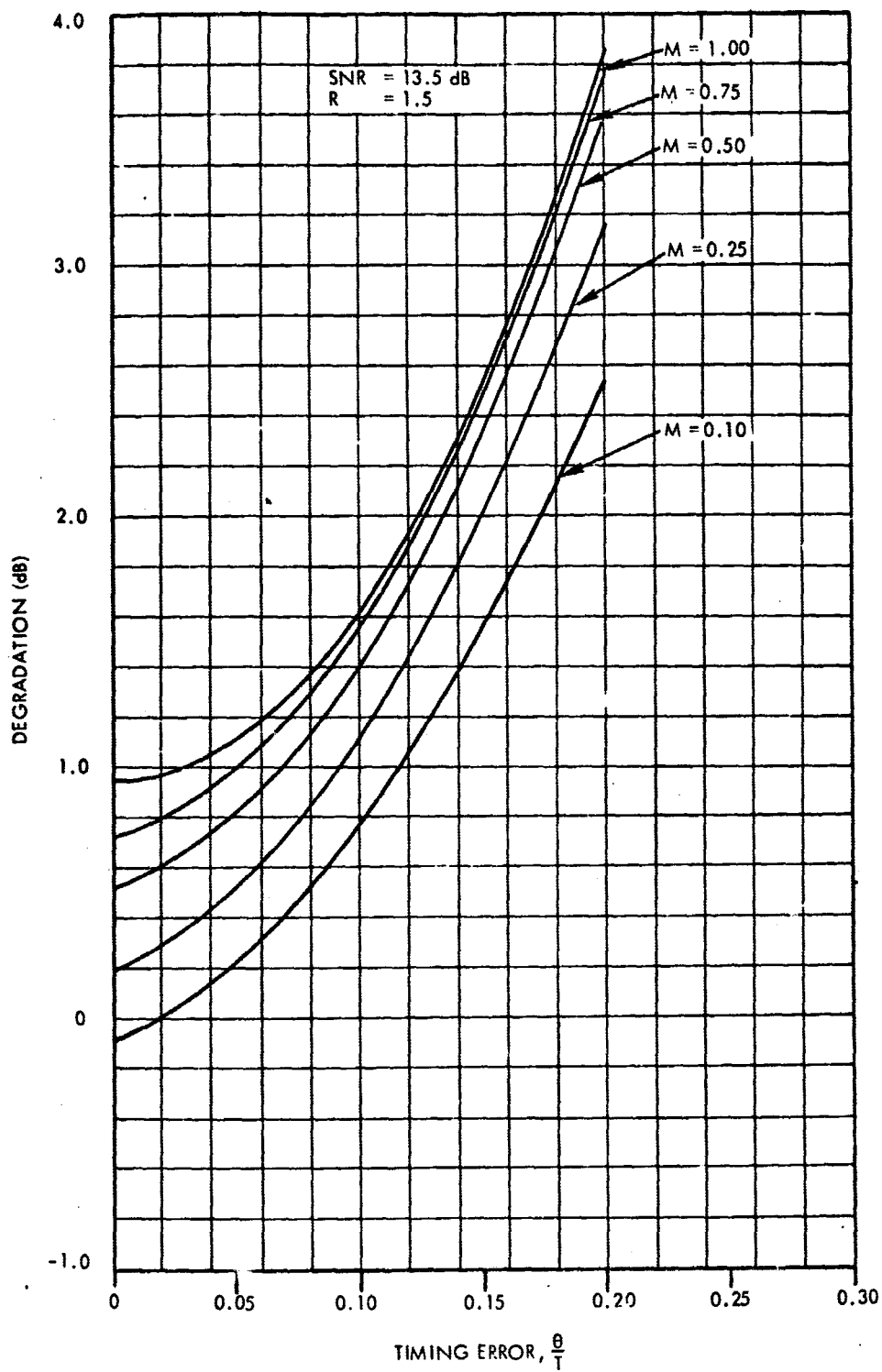


Figure 4.5.28 Performance Degradation Versus Timing Error, Integrate and Dump Bit Detector

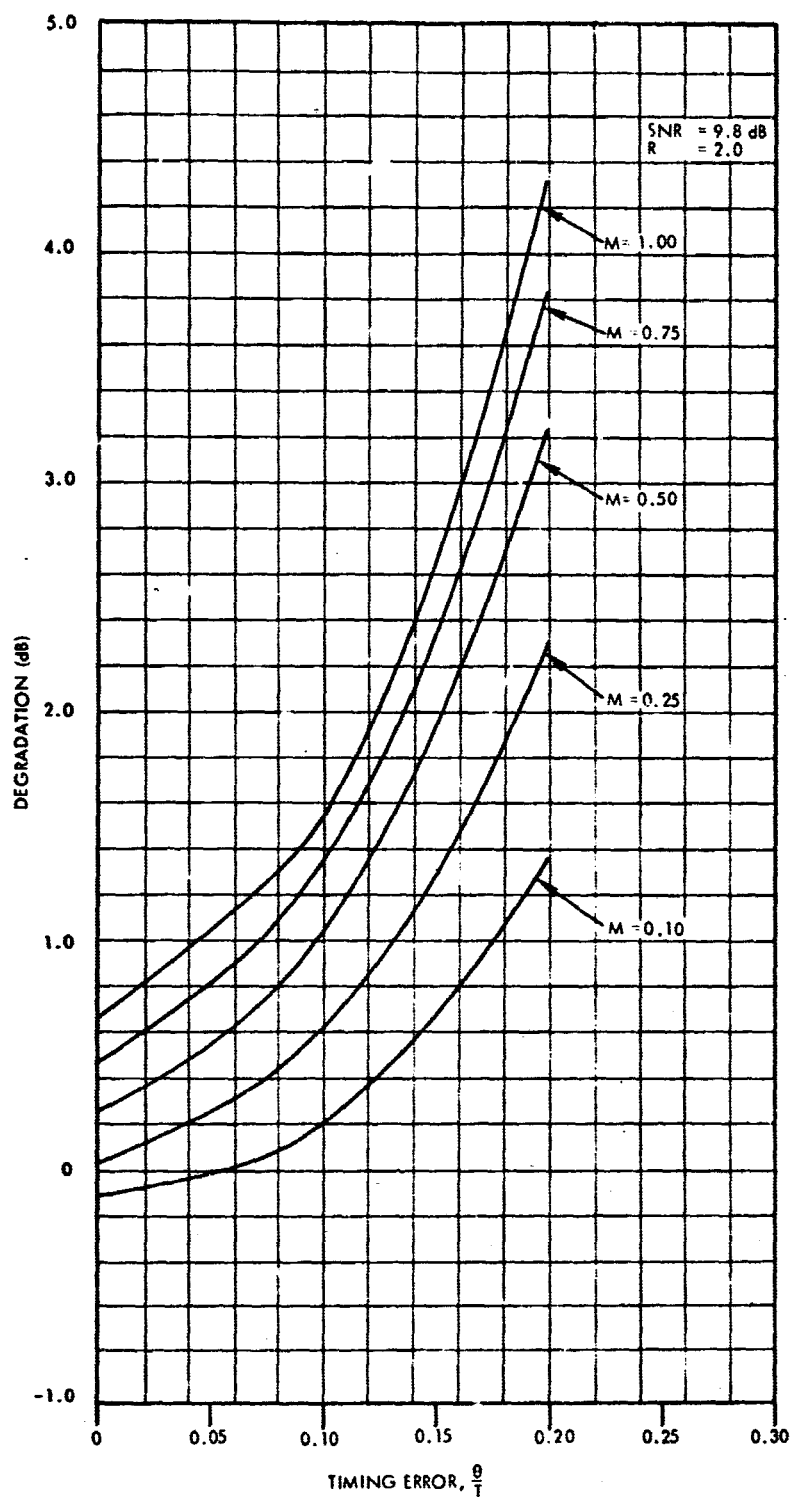


Figure 4.5.29 Performance Degradation Versus Timing Error, Integrate and Dump Bit Detector

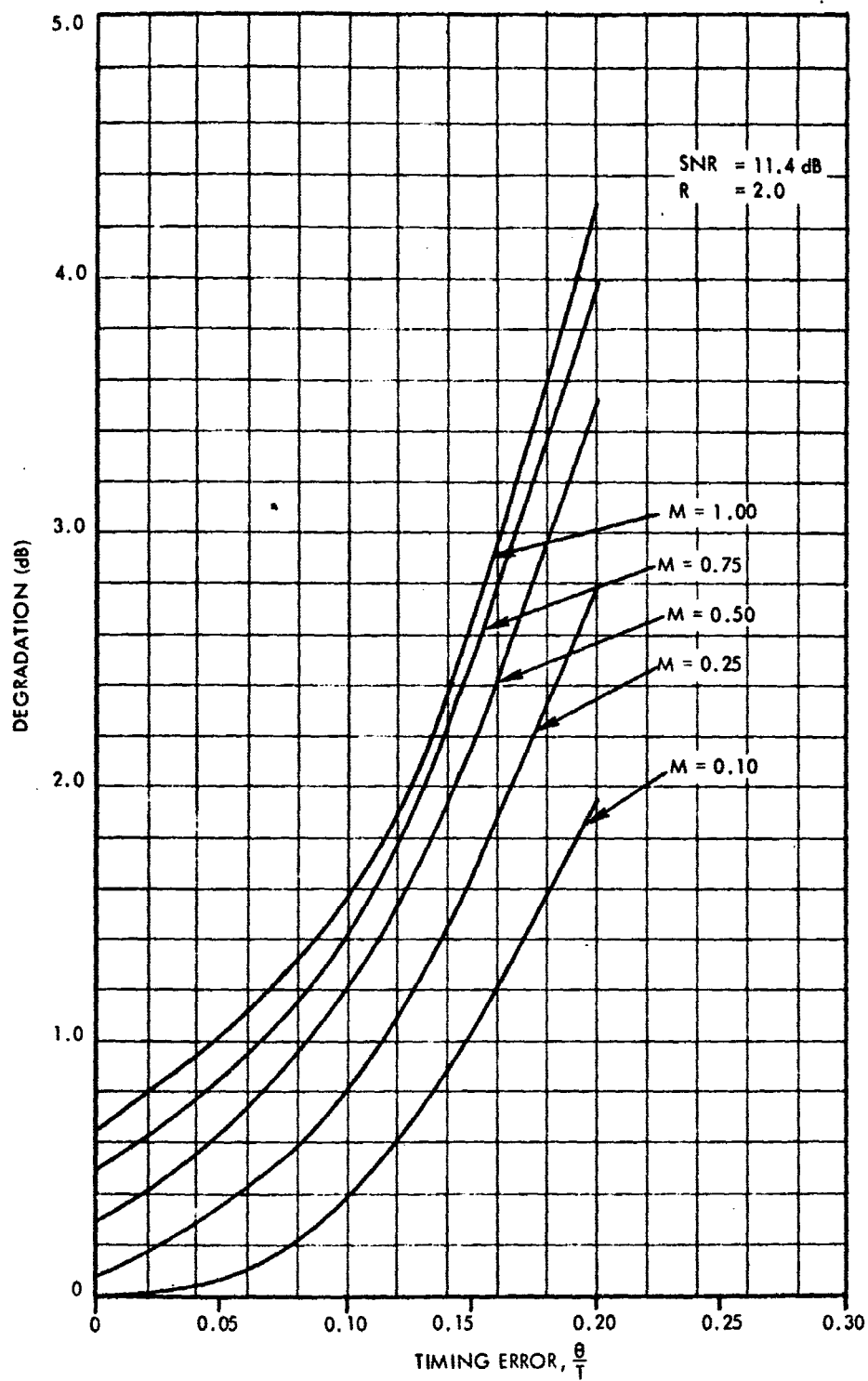


Figure 4.5.30 Performance Degradation Versus Timing Error, Integrate and Dump Bit Detector

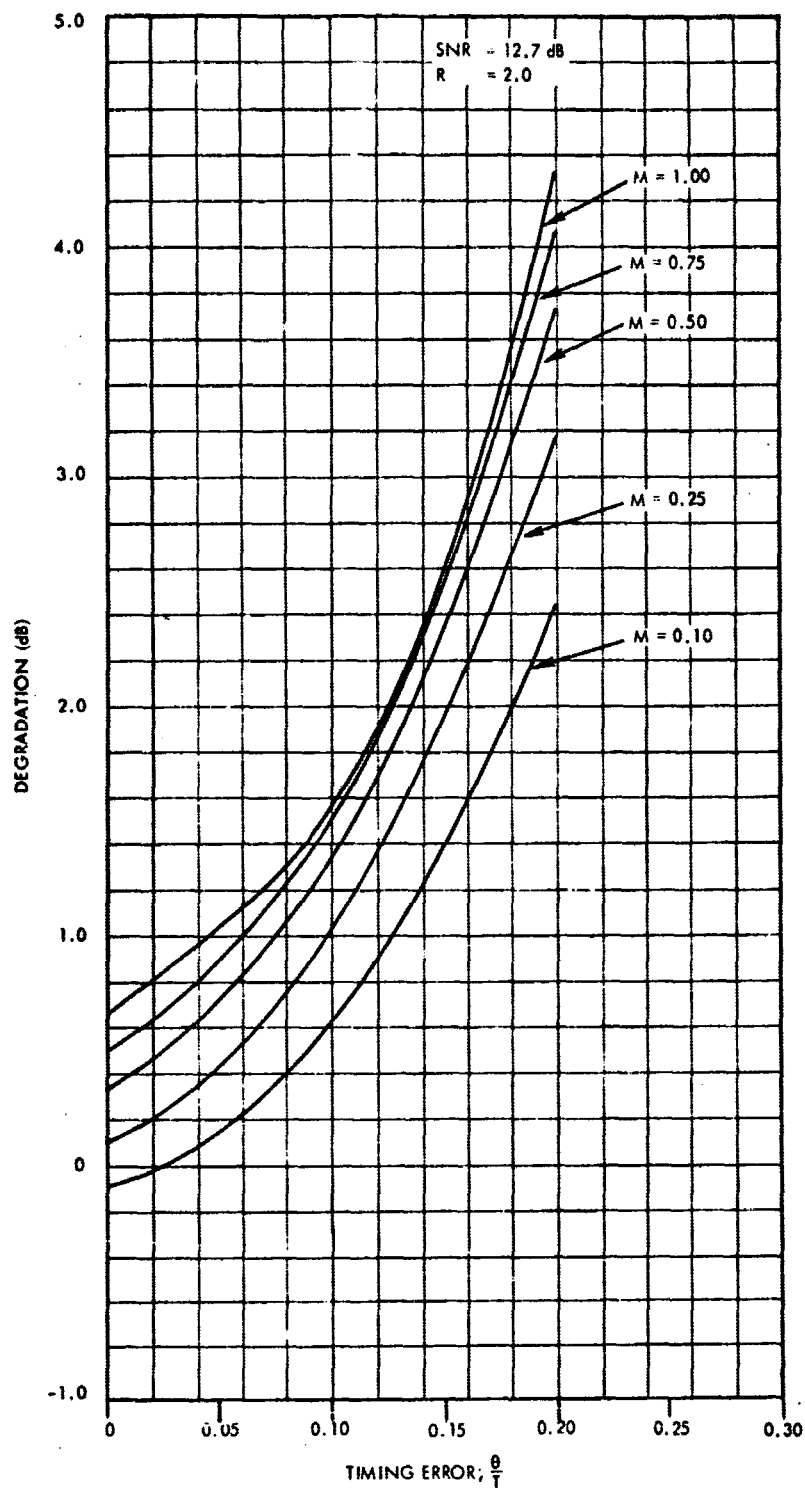


Figure 4.5.31 Performance Degradation Versus Timing Error, Integrate and Dump Bit Detector

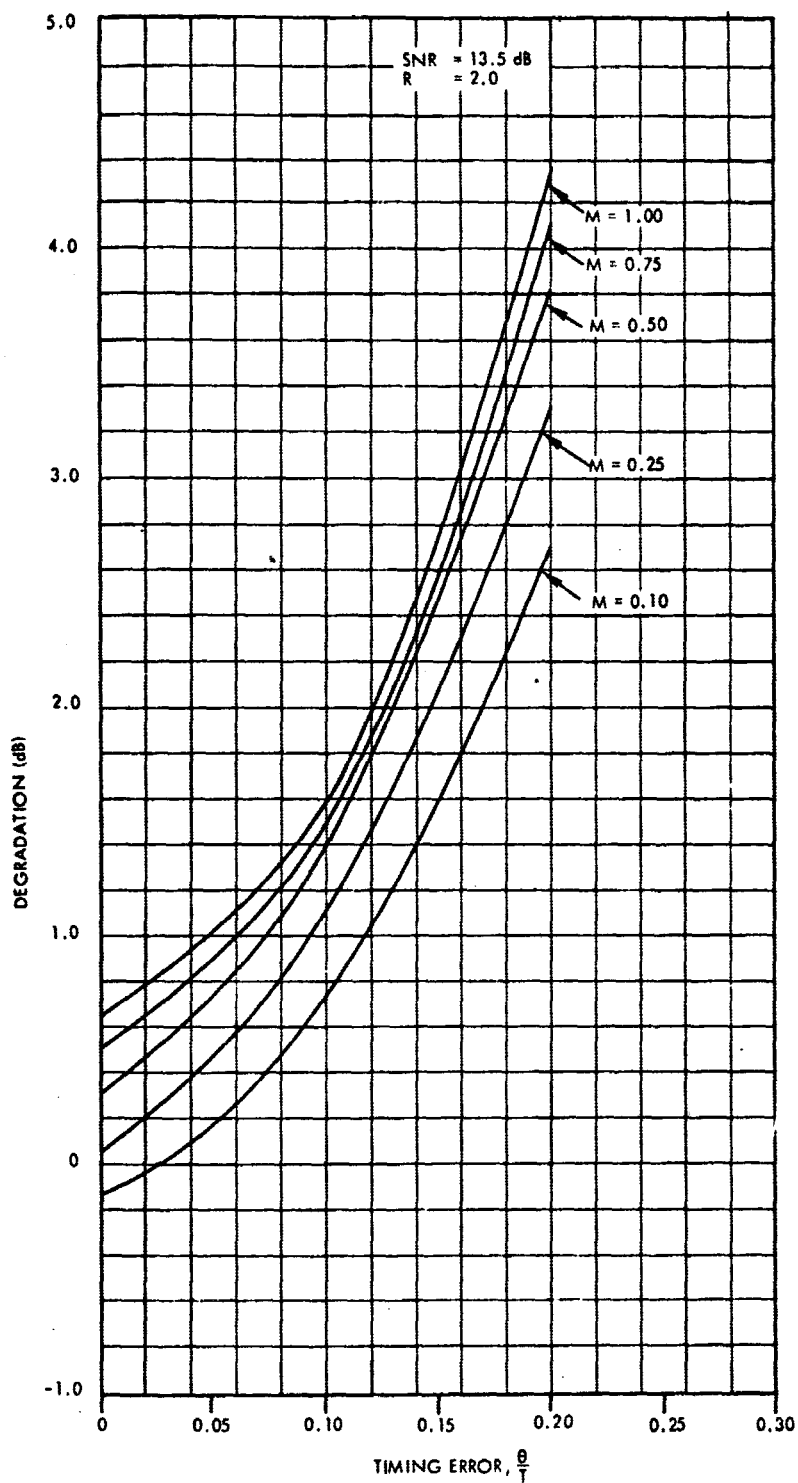


Figure 4.5.32 Performance Degradation Versus Timing Error, Integrate and Dump Bit Detector

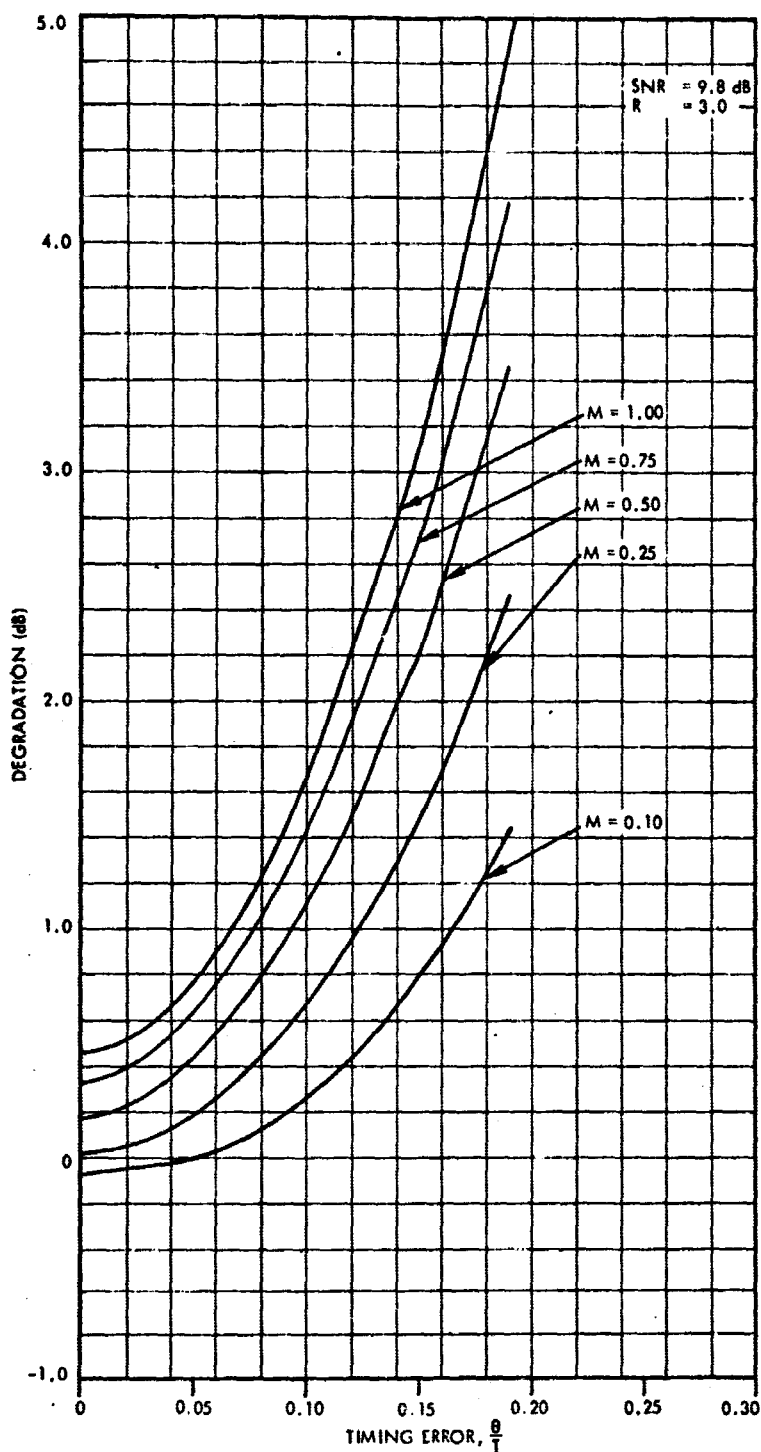


Figure 4.5.33 Performance Degradation Versus Timing Error, Integrate and Dump Bit Detector

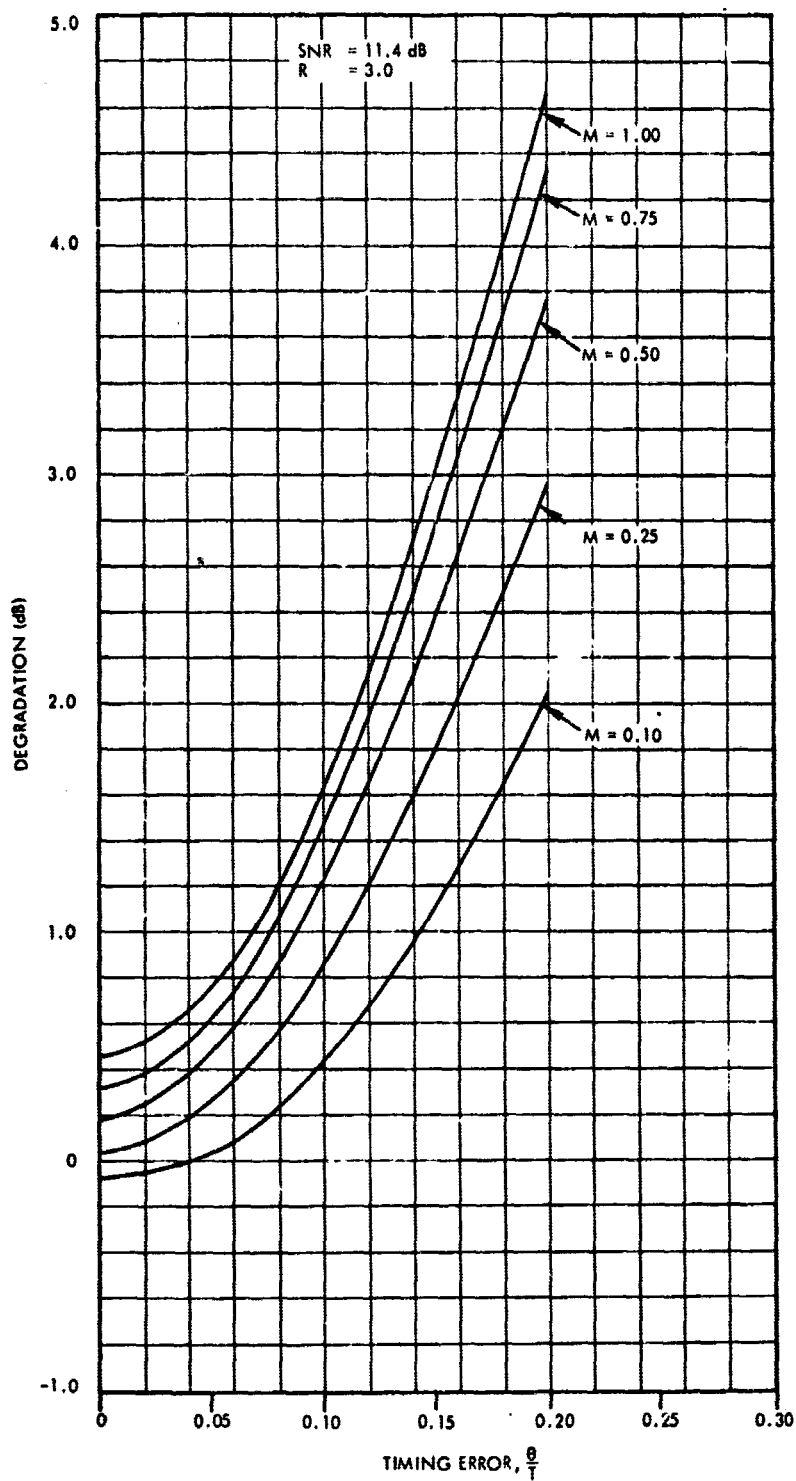


Figure 4.5.34 Performance Degradation Versus Timing Error, Integrate and Dump Bit Detector

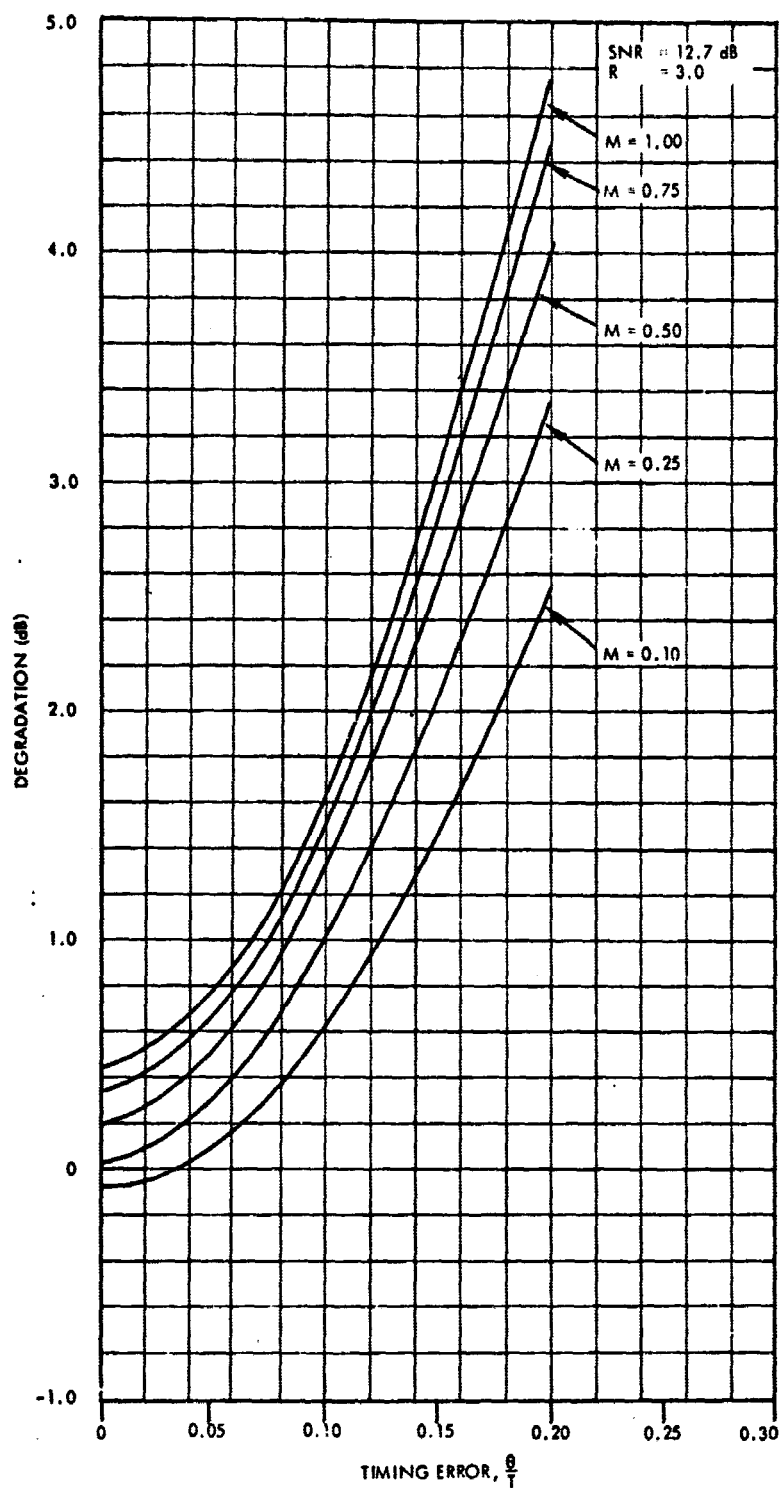


Figure 4.5.35 Performance Degradation Versus Timing Error, Integrate and Dump Bit Detector

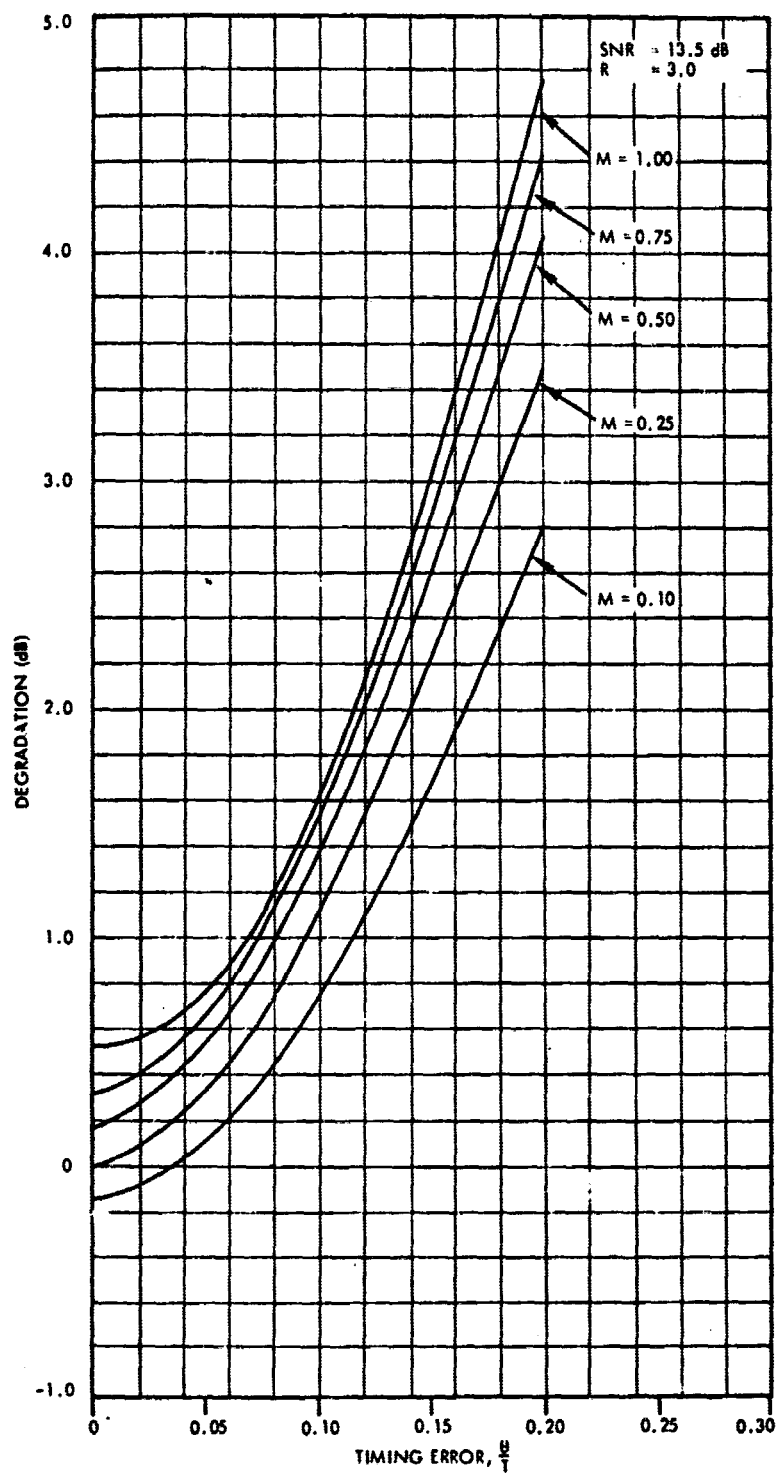


Figure 4.5.36 Performance Degradation Versus Timing Error, Integrate and Dump Bit Detector

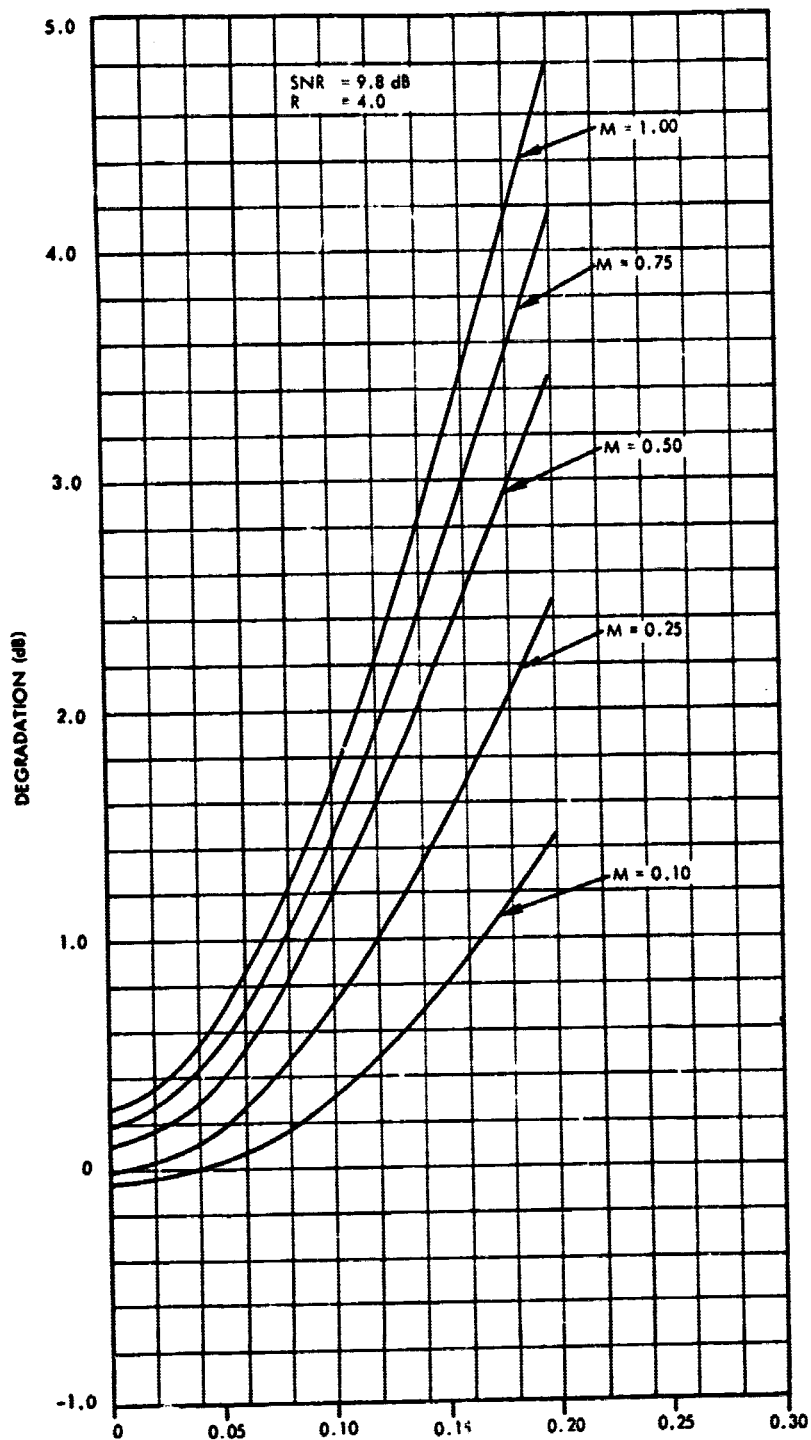


Figure 4.5.37 Performance Degradation Versus Timing Error, Integrate and Dump Bit Detector

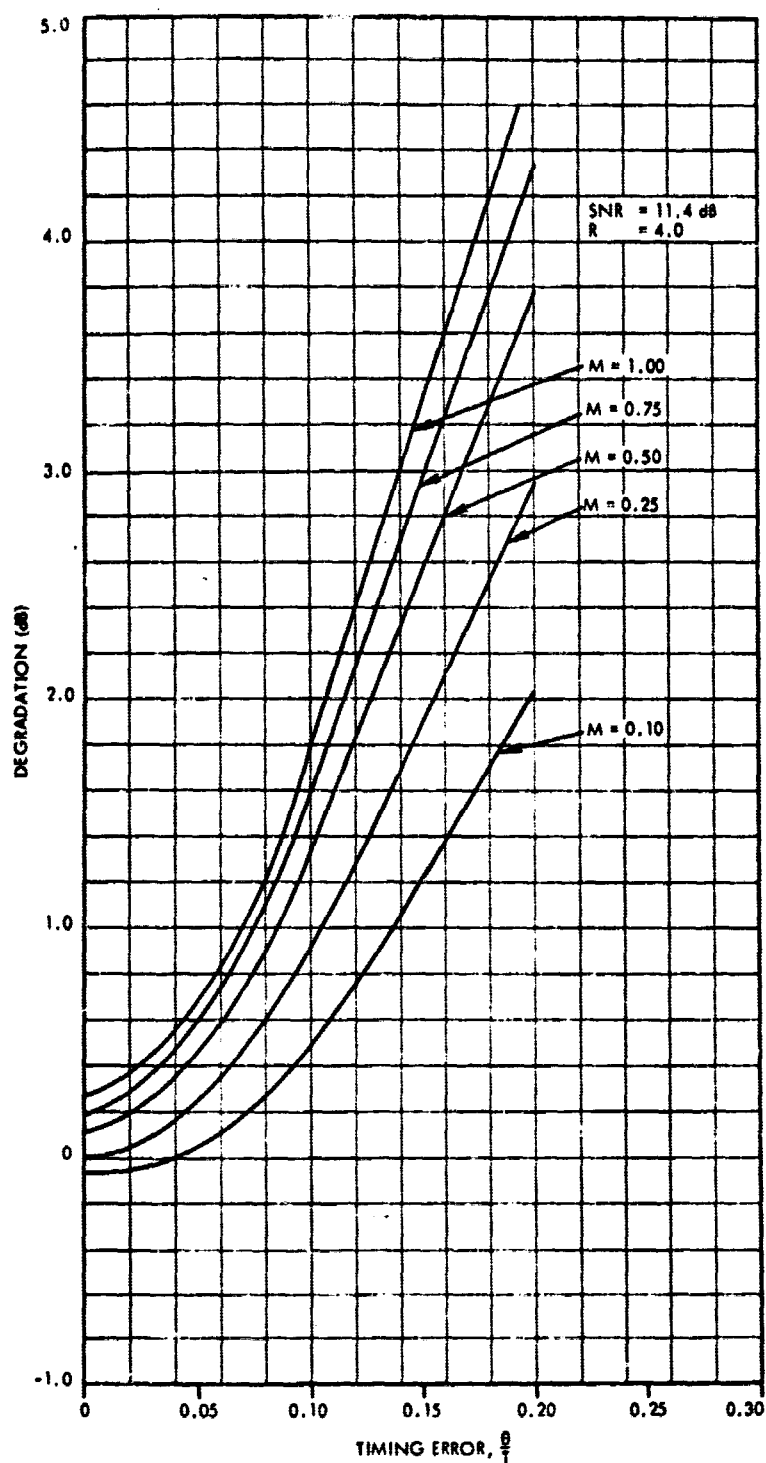


Figure 4.5.38 Performance Degradation Versus Timing Error, Integrate and Dump Bit Detector

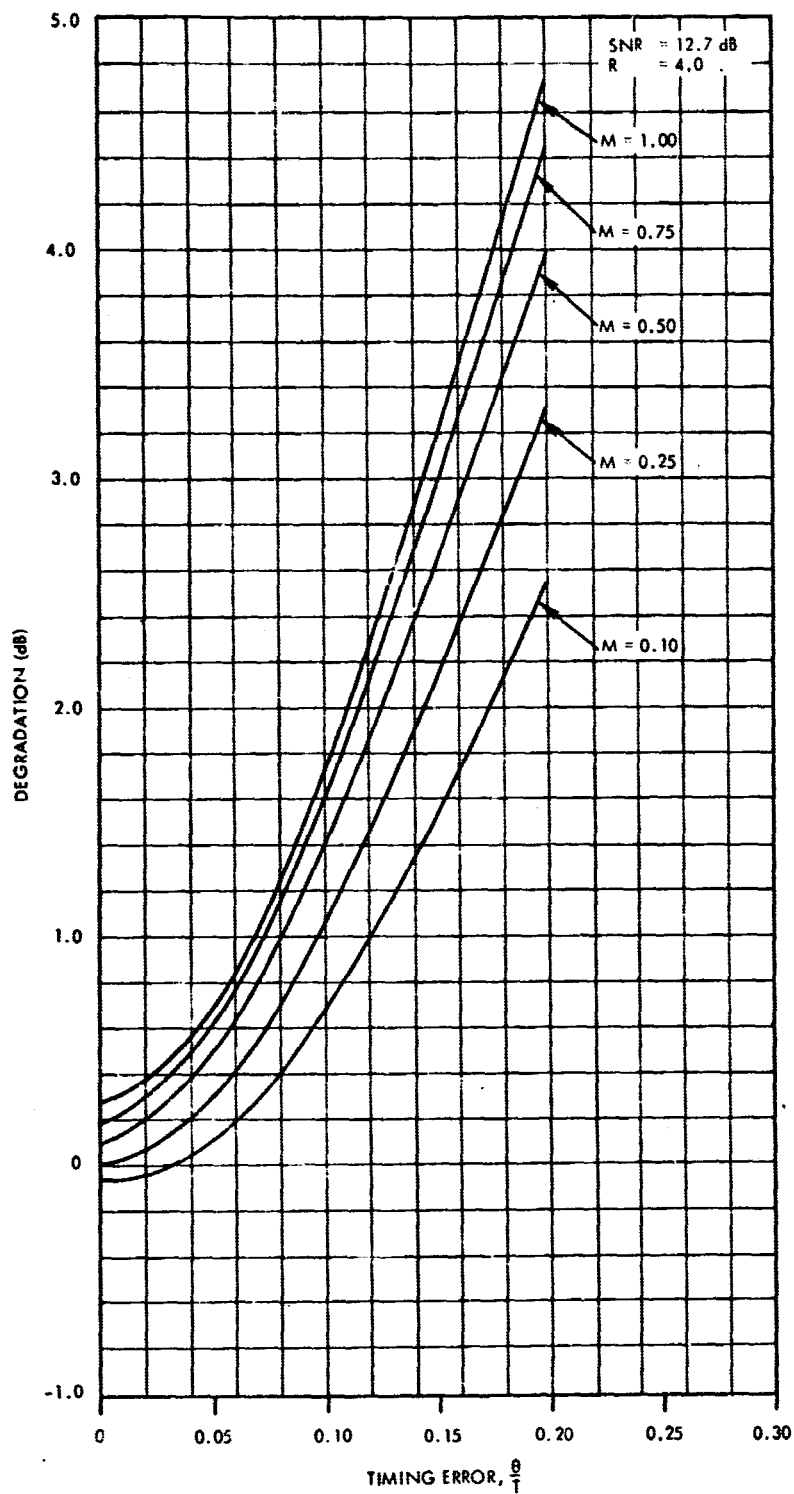


Figure 4.5.39 Performance Degradation Versus Timing Error, Integrate and Dump Bit Detector

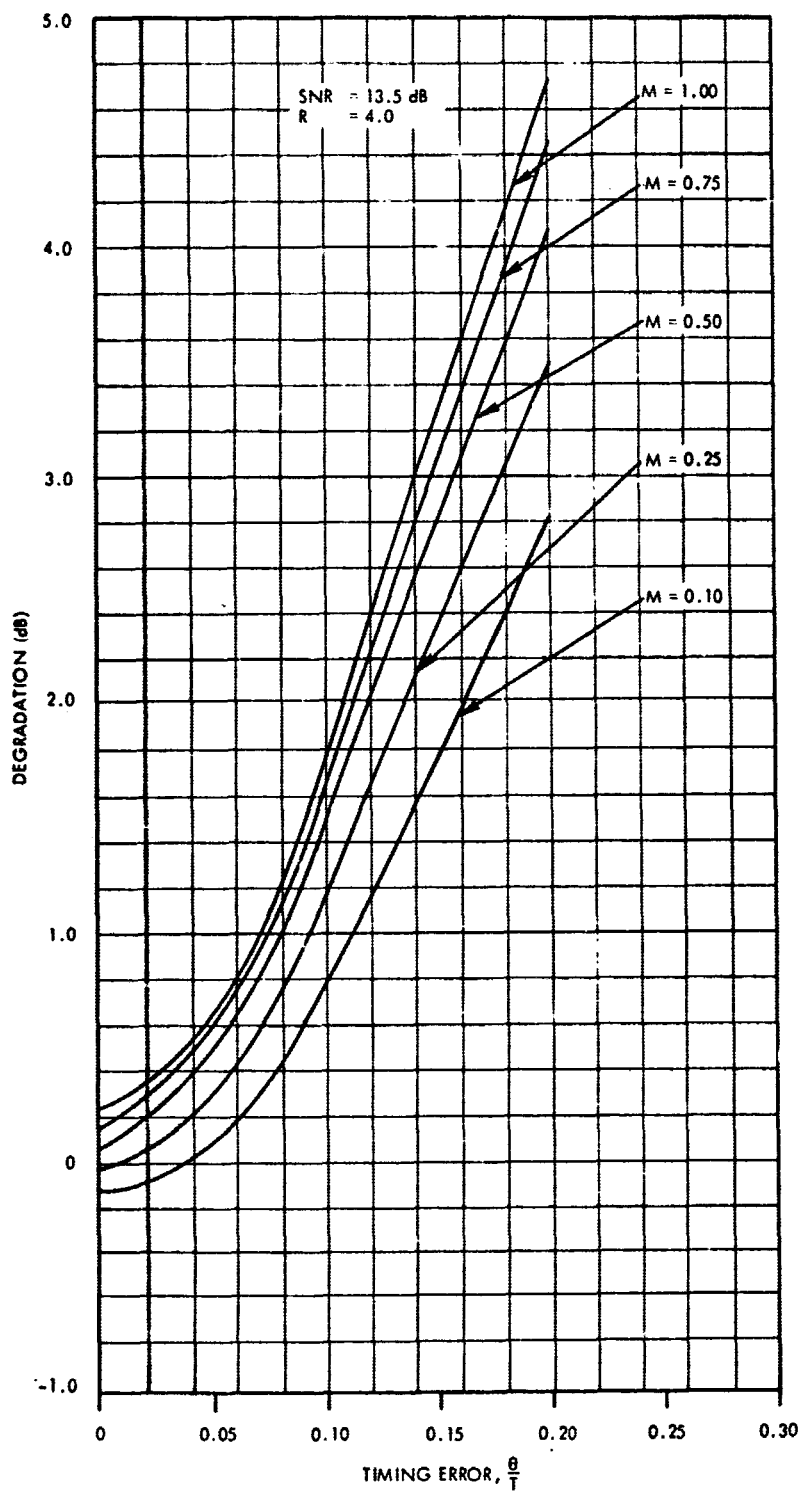


Figure 4.5.40 Performance Degradation Versus Timing Error, Integrate and Dump Bit Detector

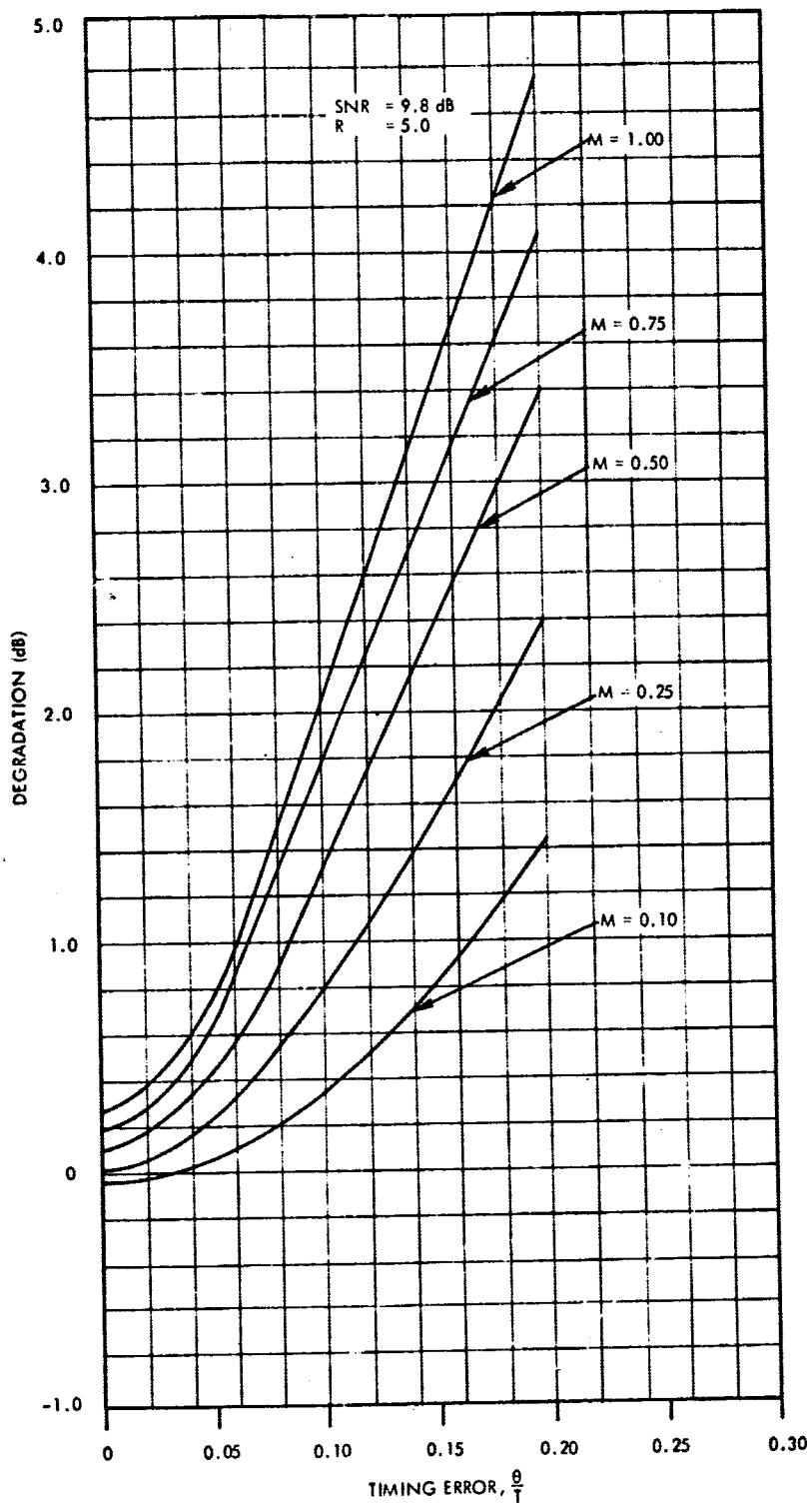


Figure 4.5.41 Performance Degradation Versus Timing Error, Integrate and Dump Bit Detector

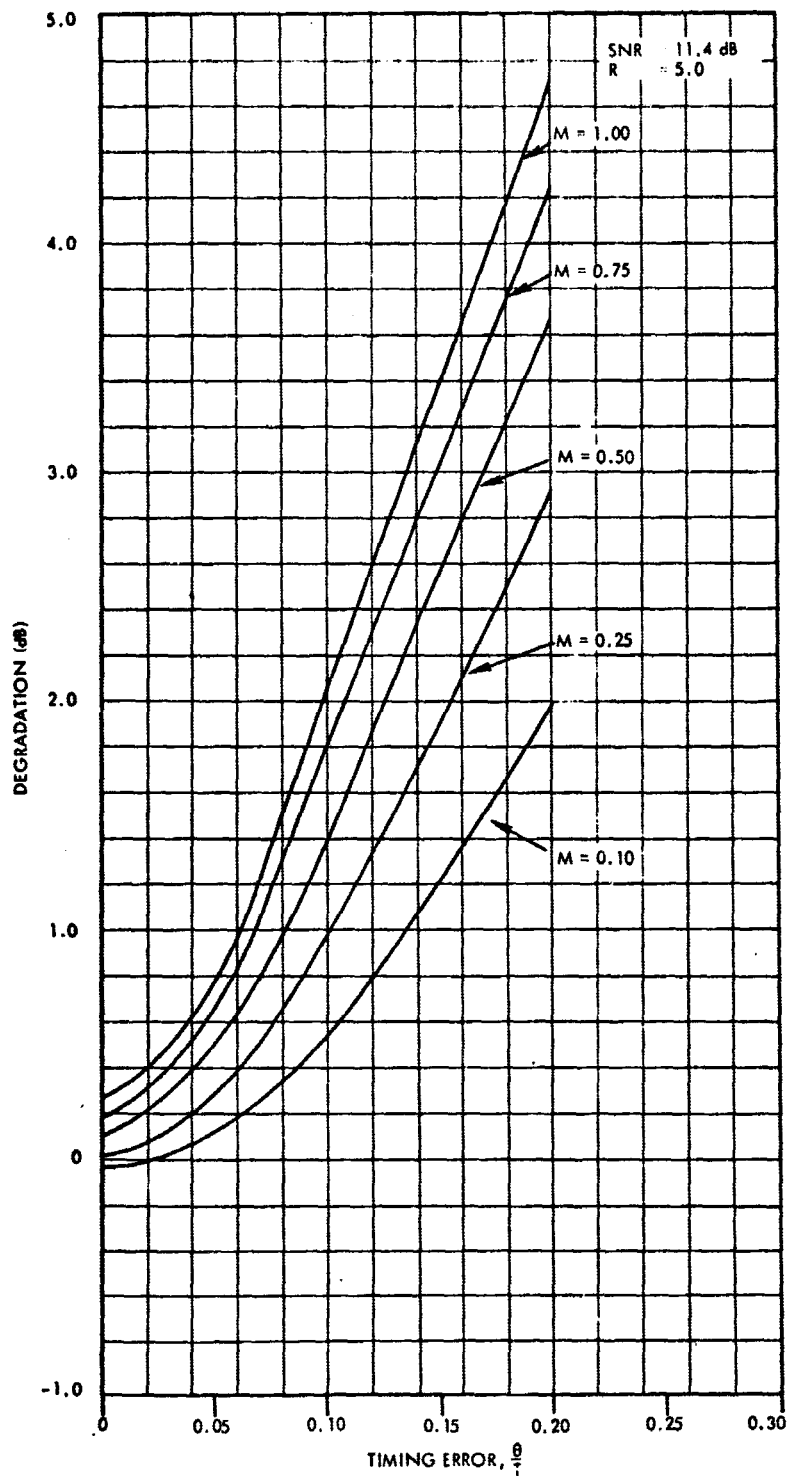


Figure 4.5.42 Performance Degradation Versus Timing Error, Integrate and Dump Bit Detector

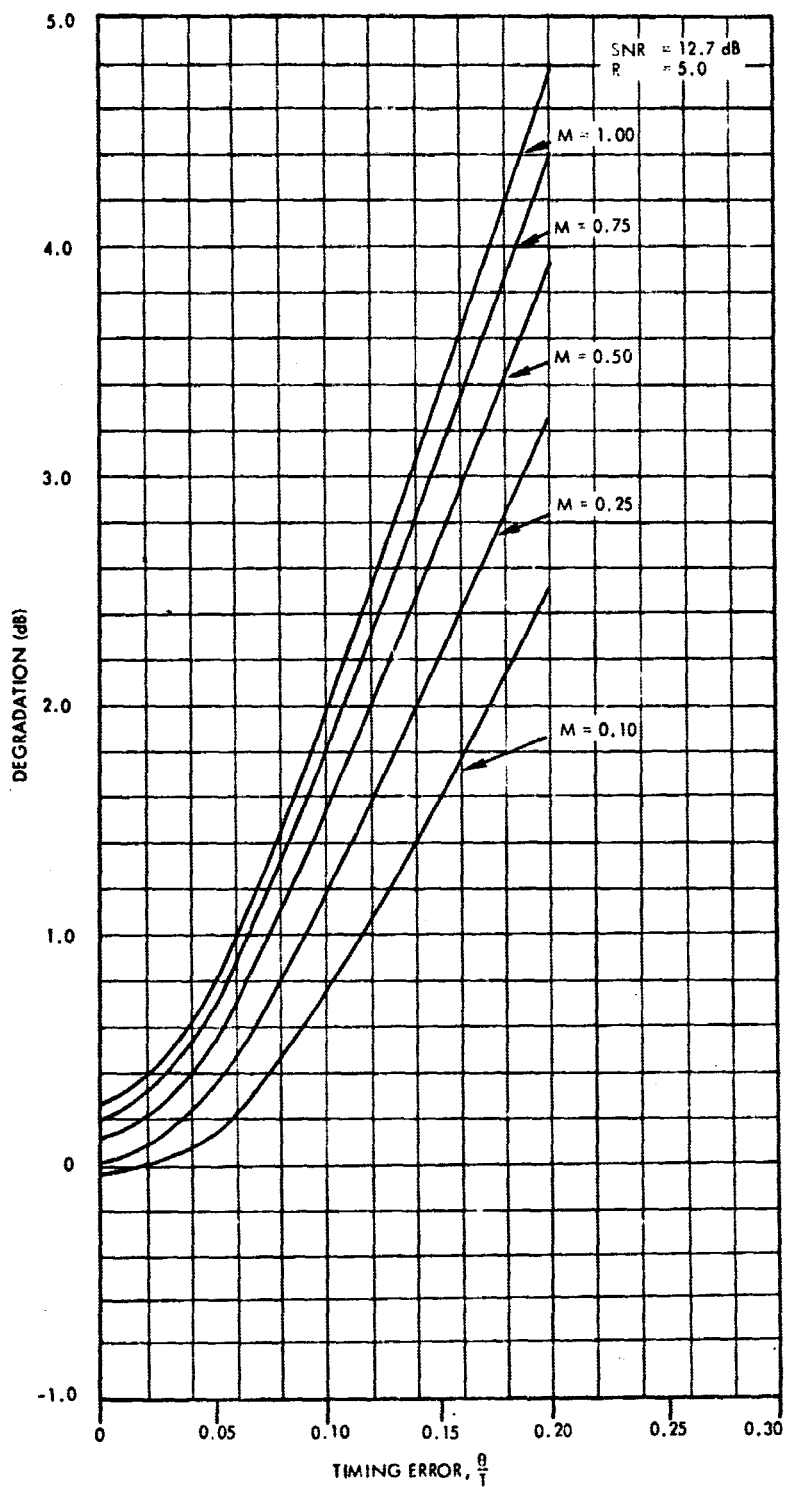


Figure 4.5.43 Performance Degradation Versus Timing Error, Integrate and Dump Bit Detector

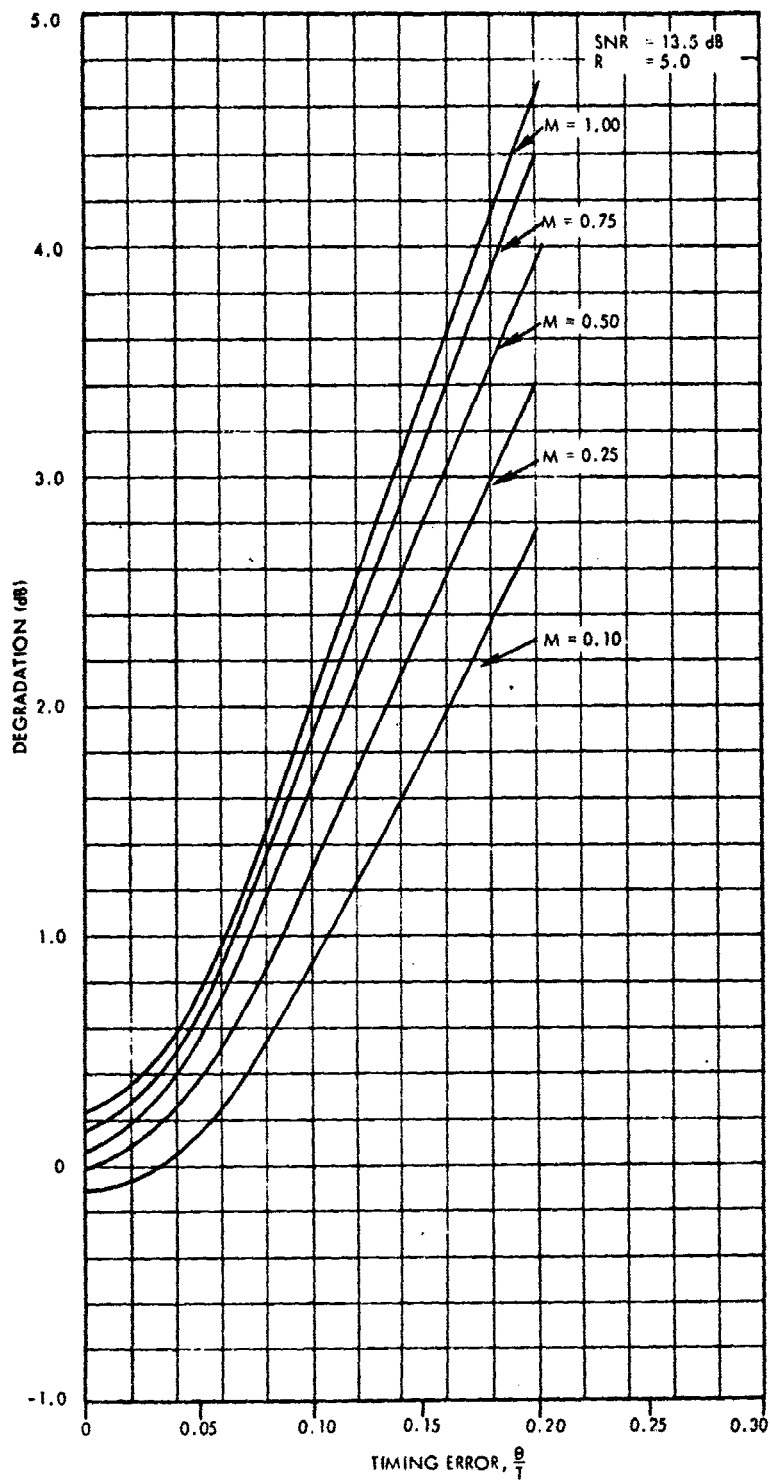


Figure 4.5.44 Performance Degradation Versus Timing Error, Integrate and Dump Bit Detector

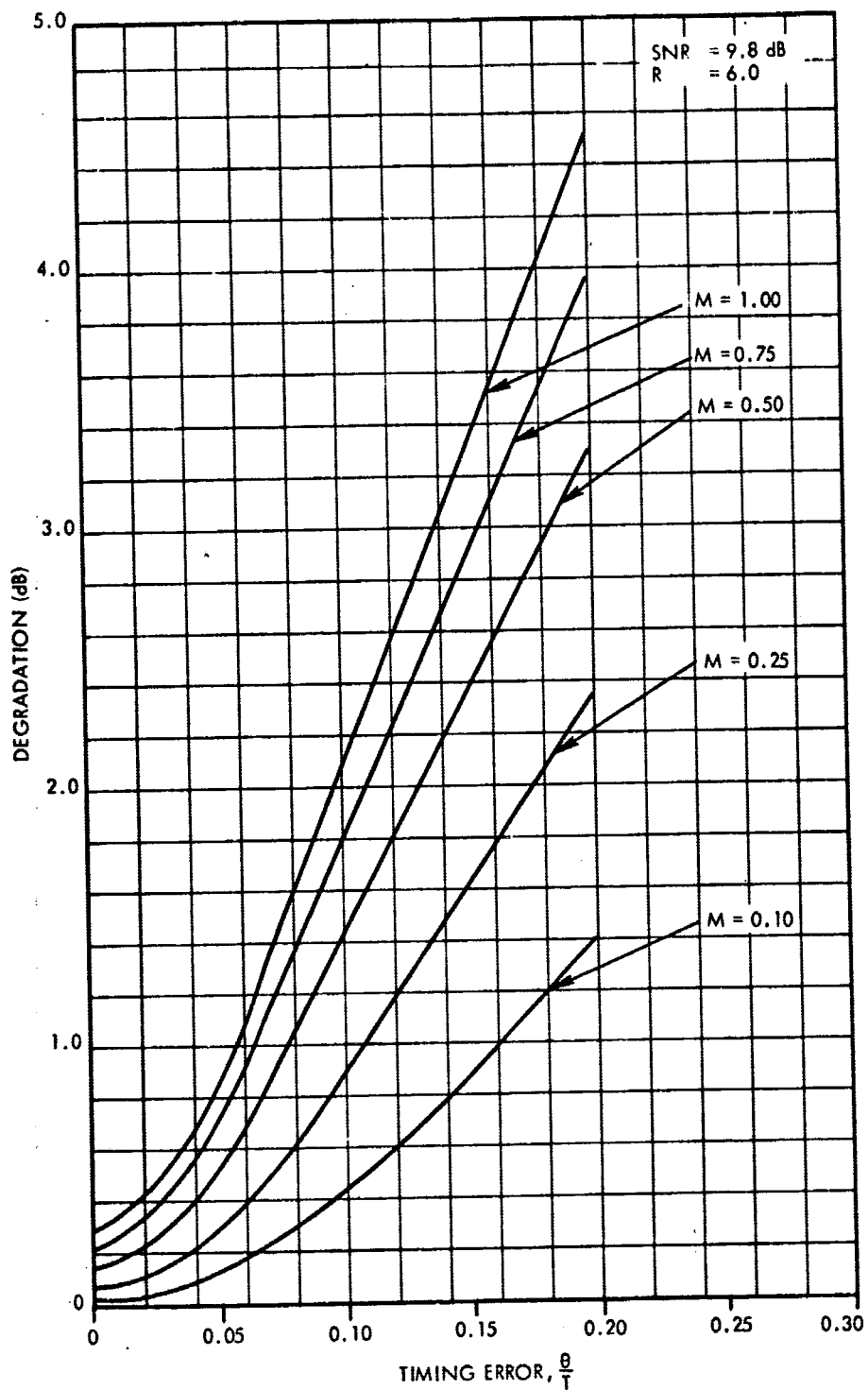


Figure 4.5.45 Performance Degradation Versus Timing Error, Integrate and Dump Bit Detector

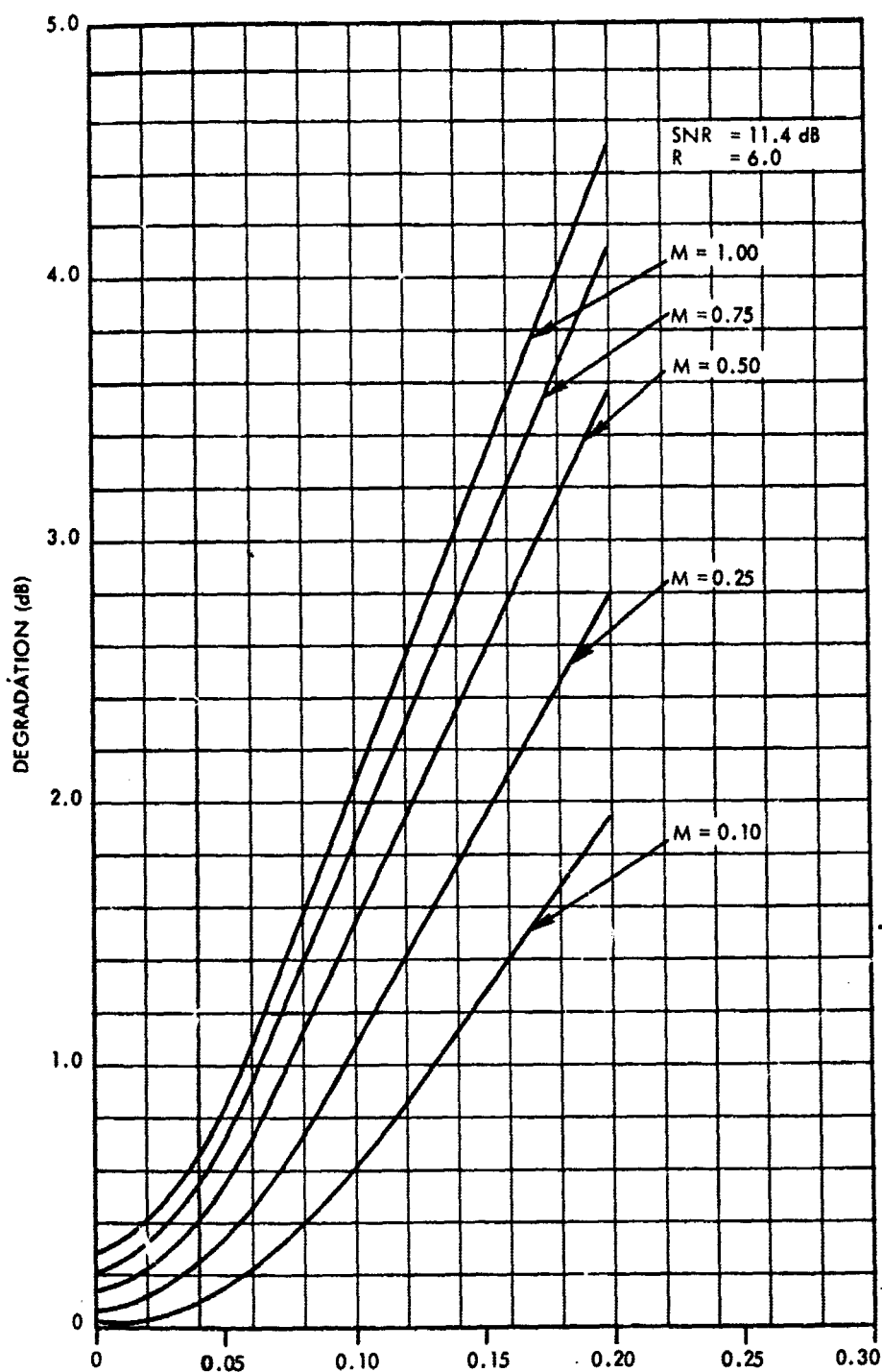


Figure 4.5.46 Performance Degradation Versus Timing Error, Integrate and Dump Bit Detector

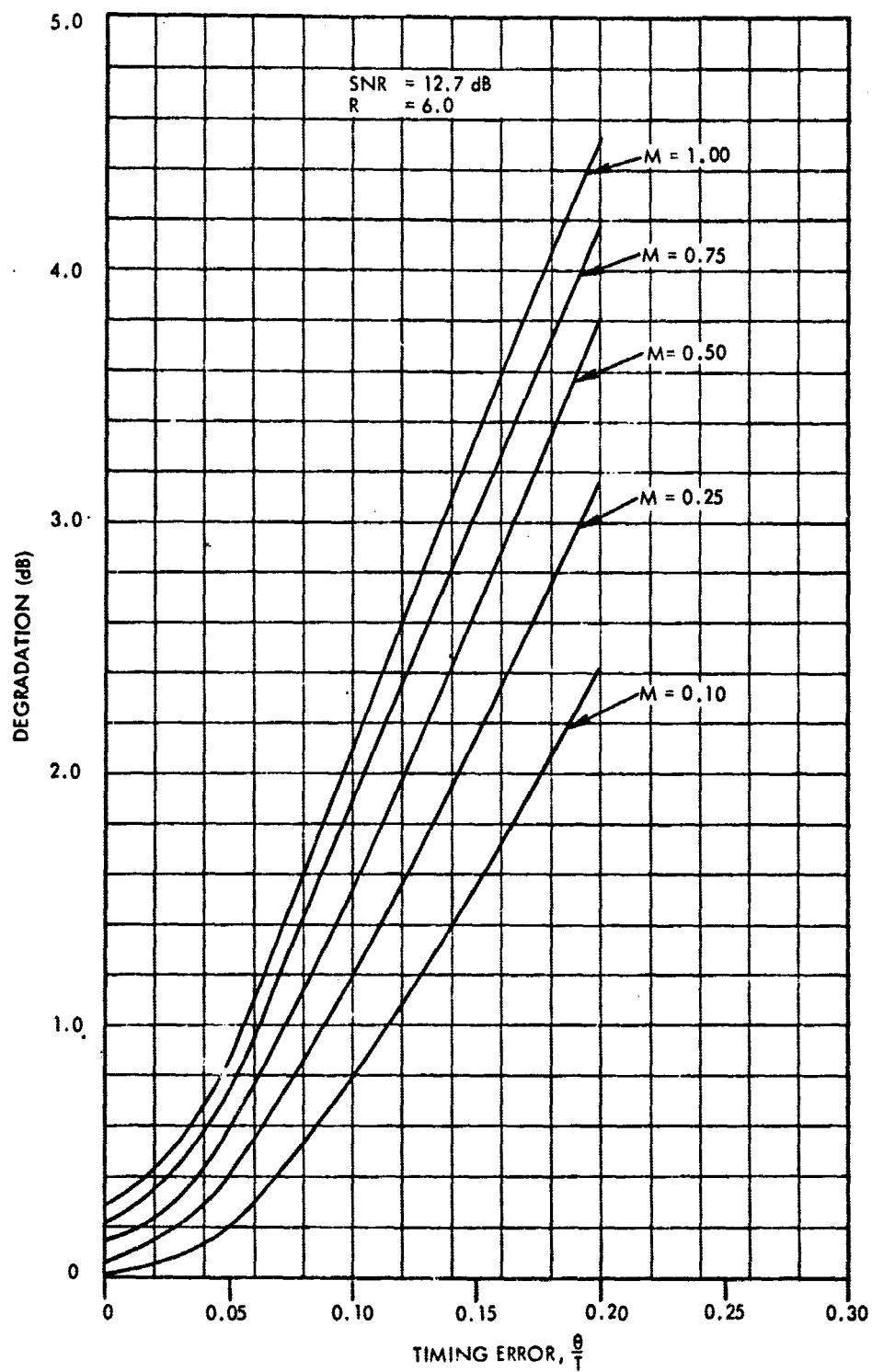


Figure 4.5.47 Performance Degradation Versus Timing Error, Integrate and Dump Bit Detector

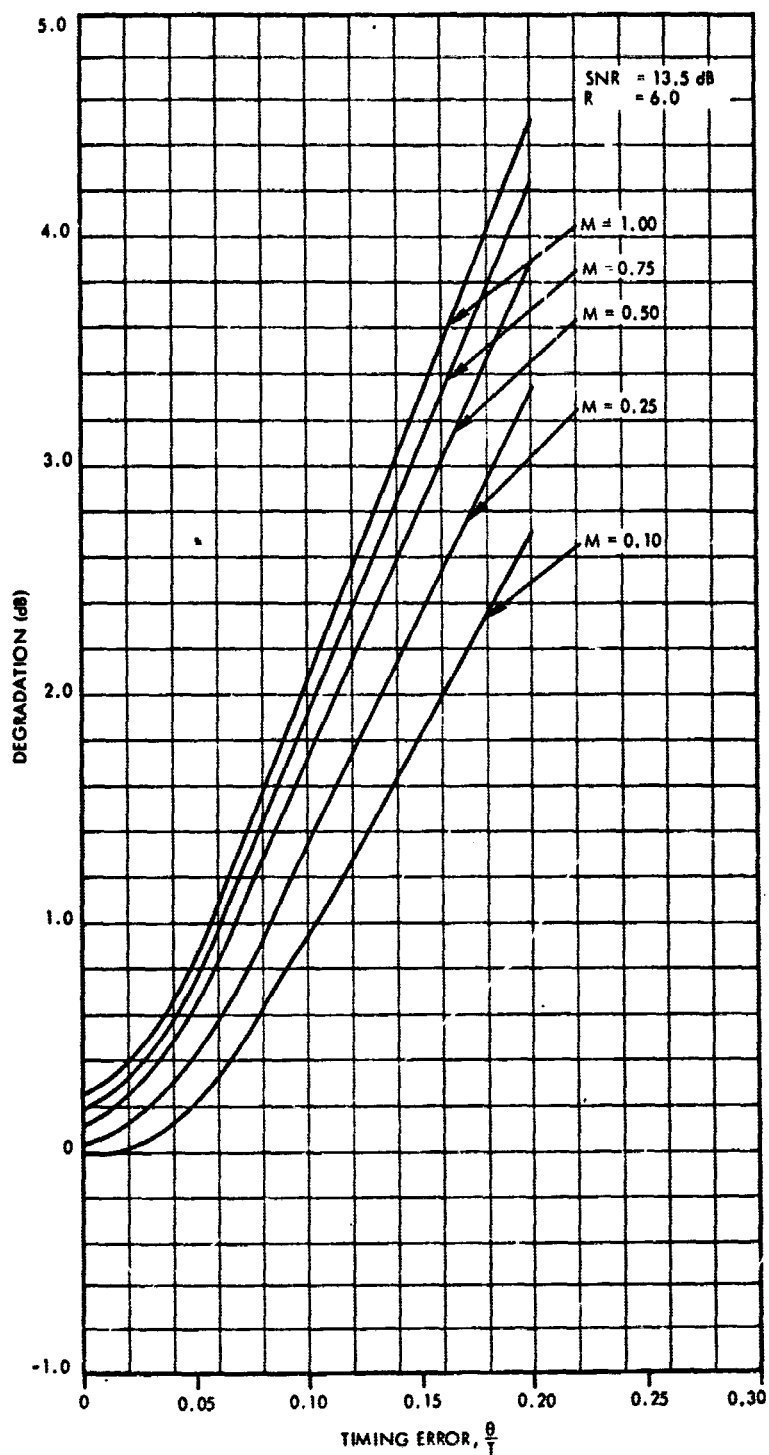


Figure 4.5.48 Performance Degradation Versus Timing Error, Integrate and Dump Bit Detector

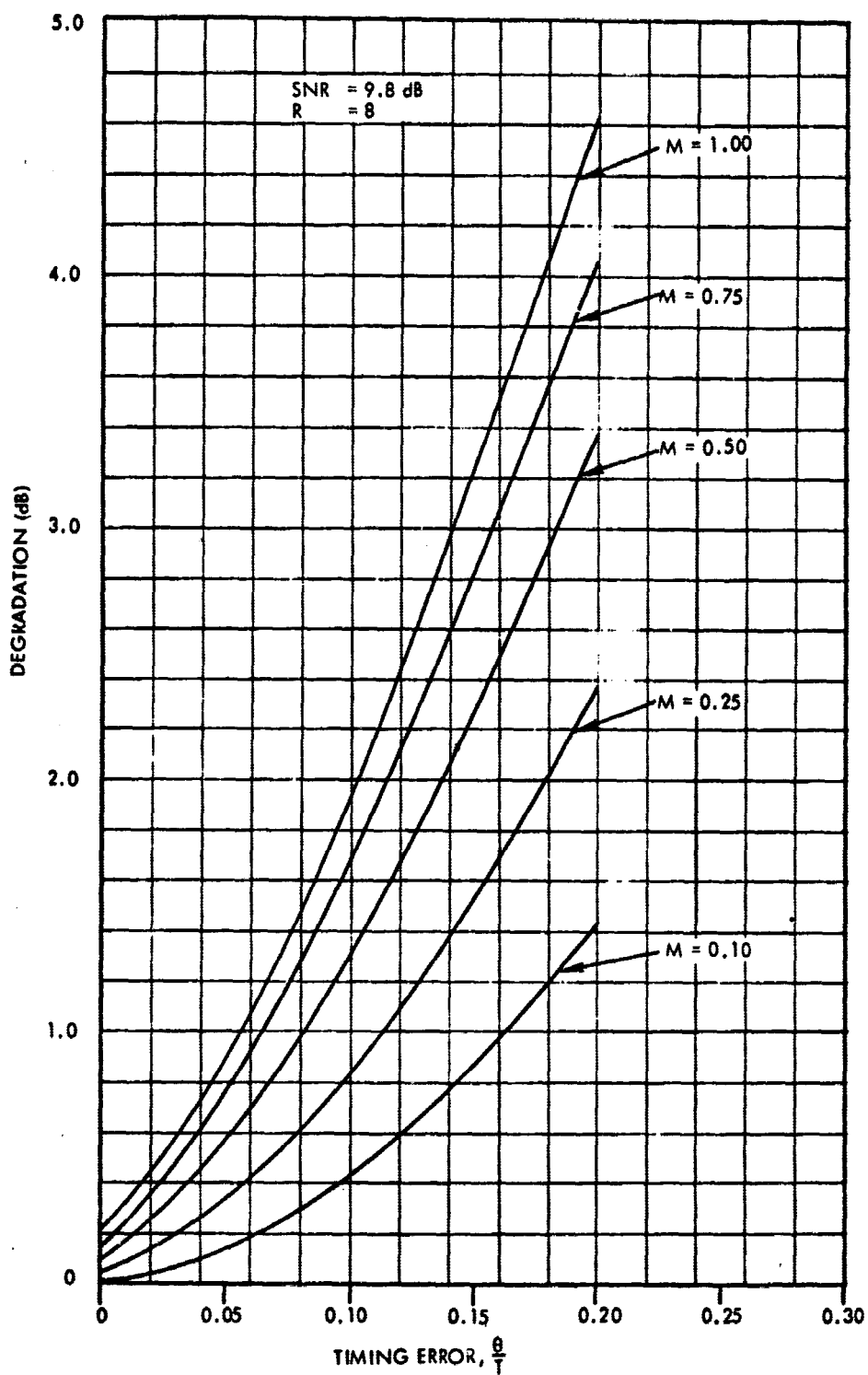


Figure 4.5.49 Performance Degradation Versus Timing Error, Integrate and Dump Bit Detector

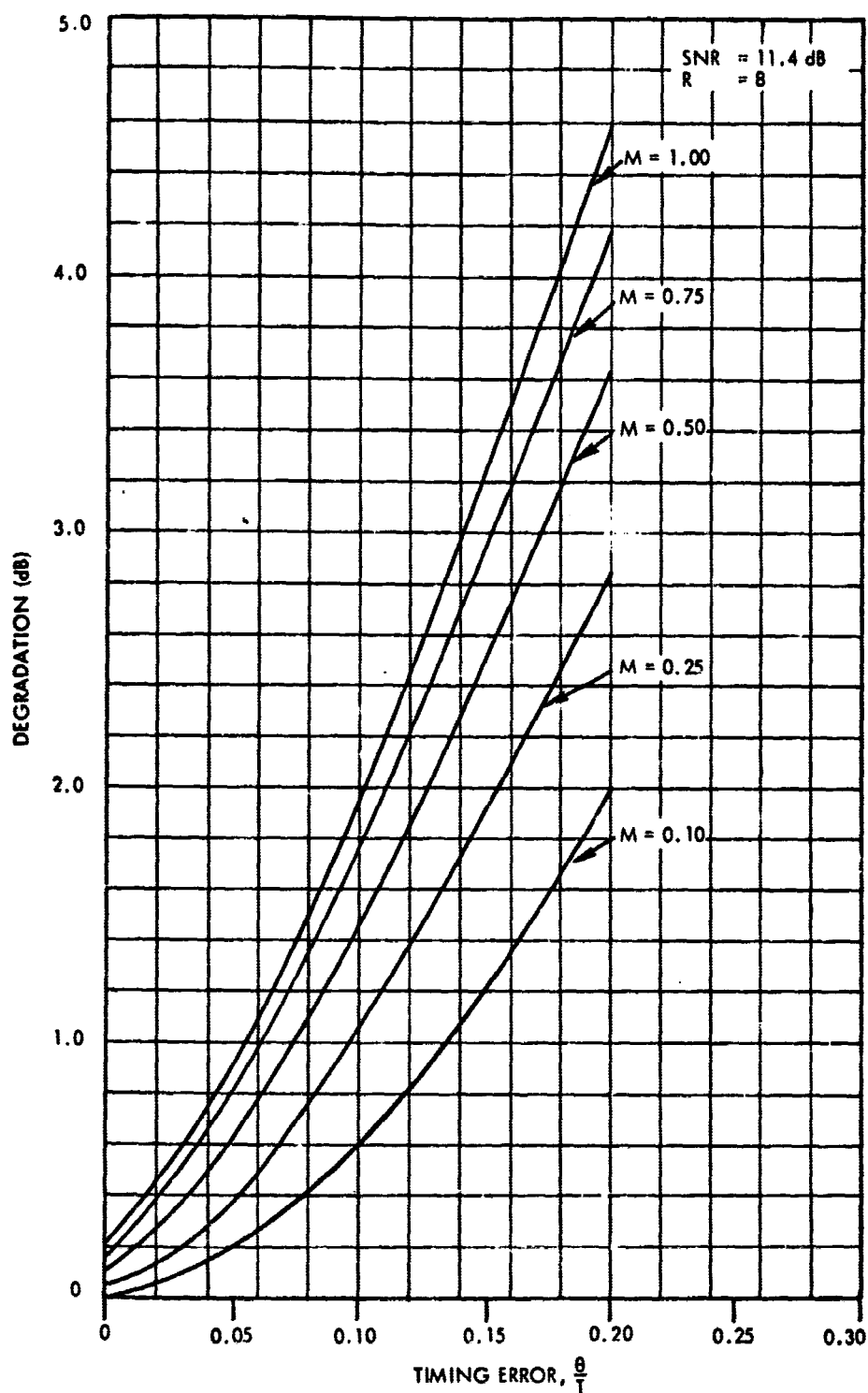


Figure 4.5.50 Performance Degradation Versus Timing Error, Integrate and Dump Bit Detector

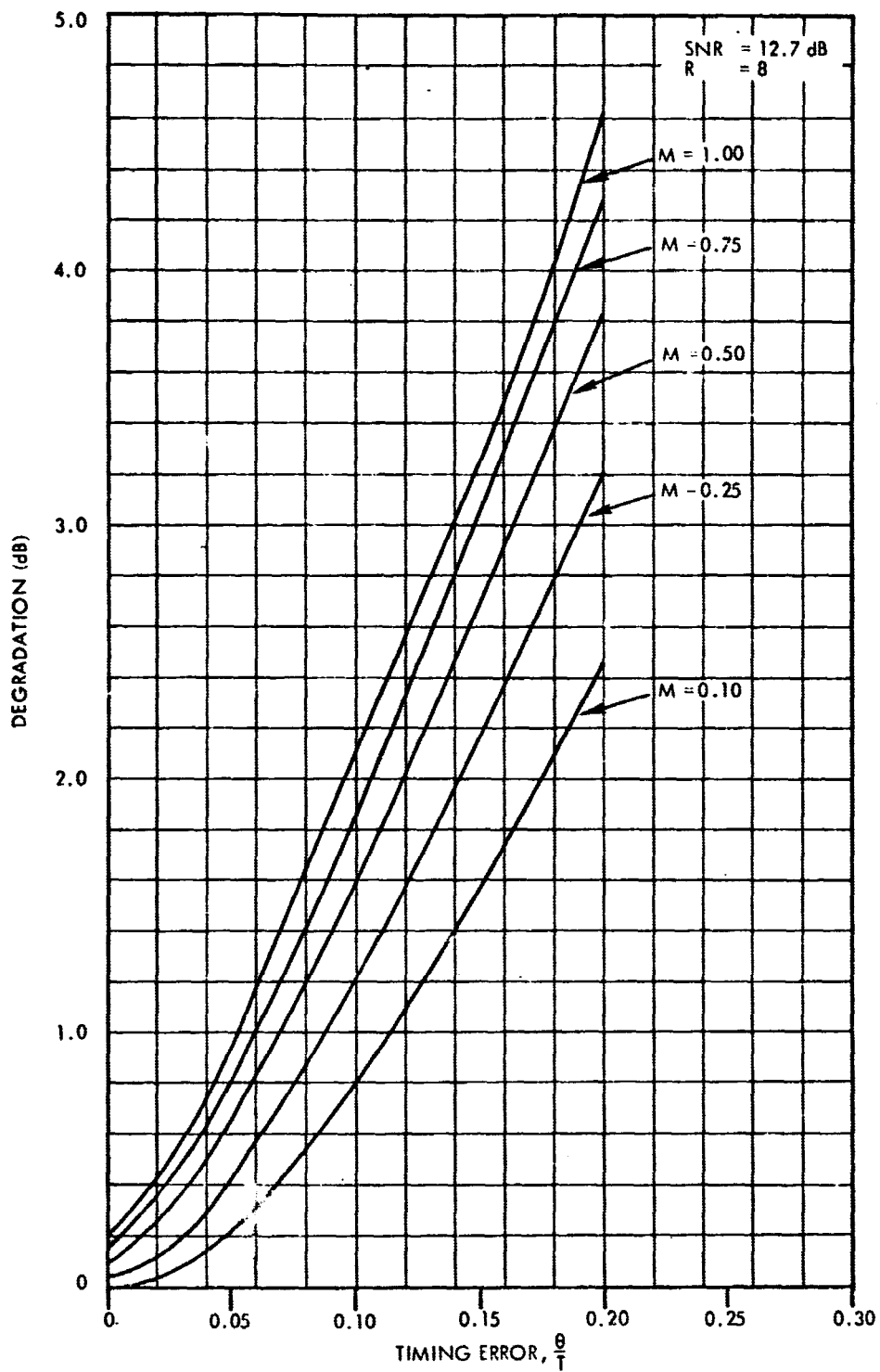


Figure 4.5.51 Performance Degradation Versus Timing Error, Integrate and Dump Bit Detector

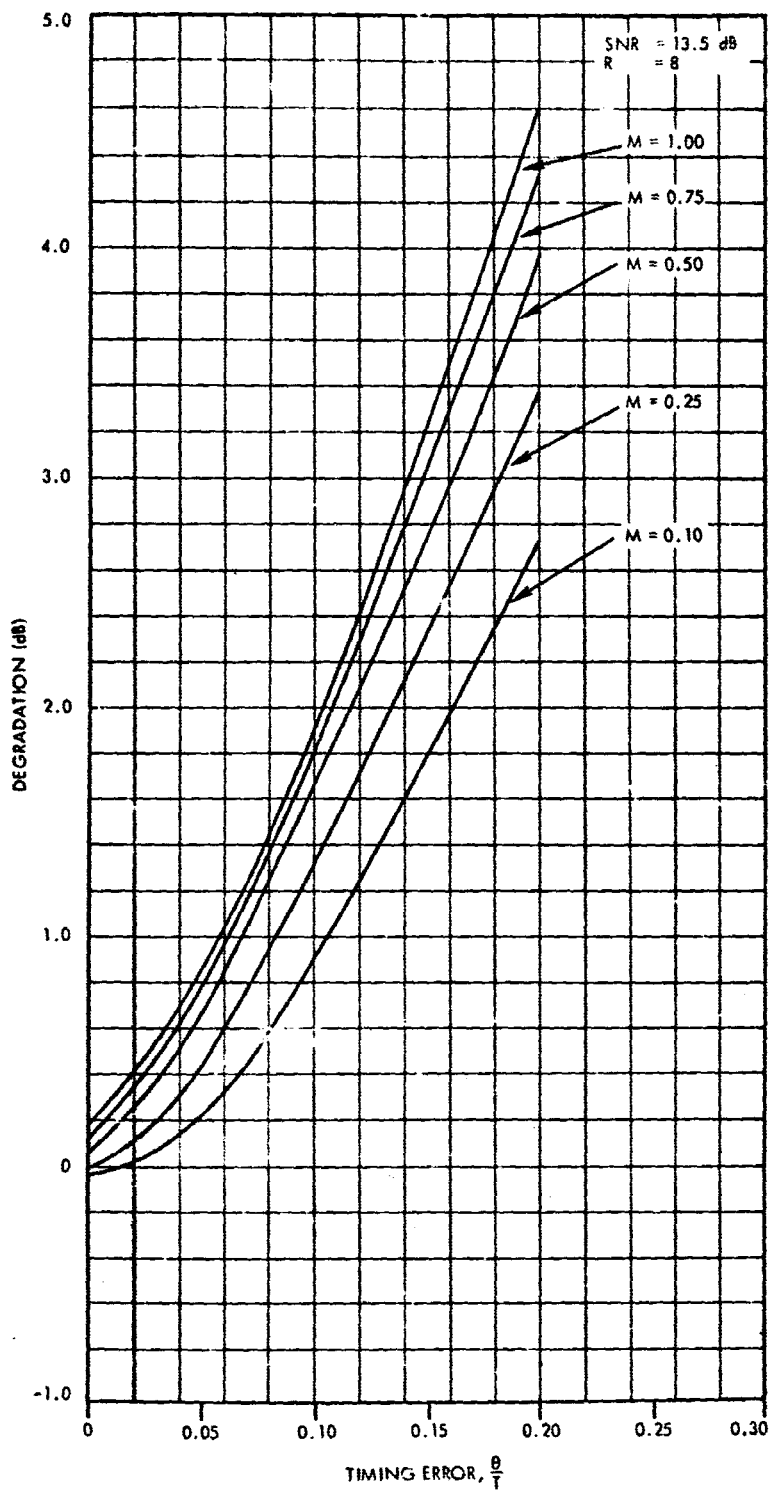


Figure 4.5.52 Performance Degradation Versus Timing Error, Integrate and Dump Bit Detector

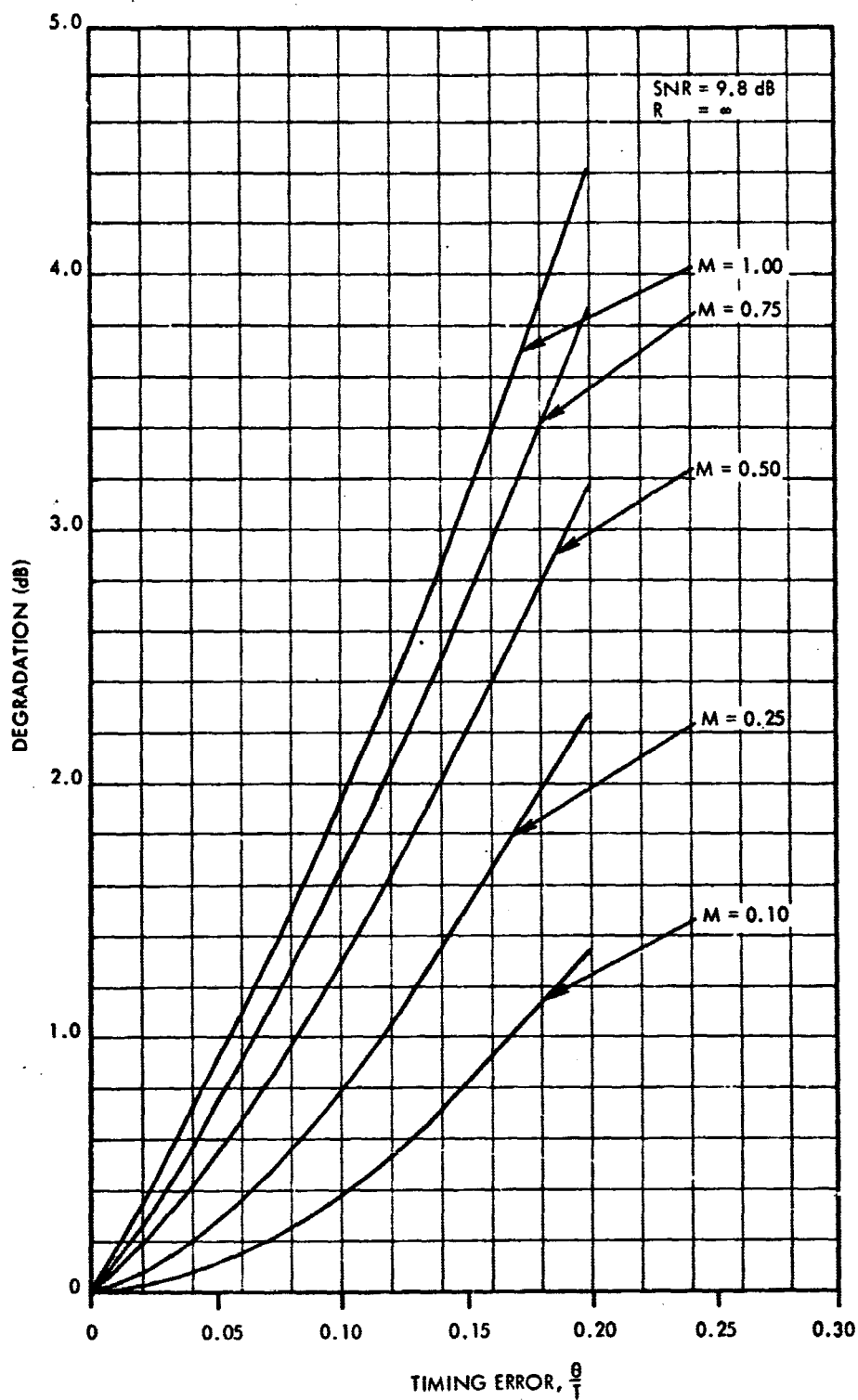


Figure 4.5.53 Performance Degradation Versus Timing Error, Integrate and Dump Bit Detector

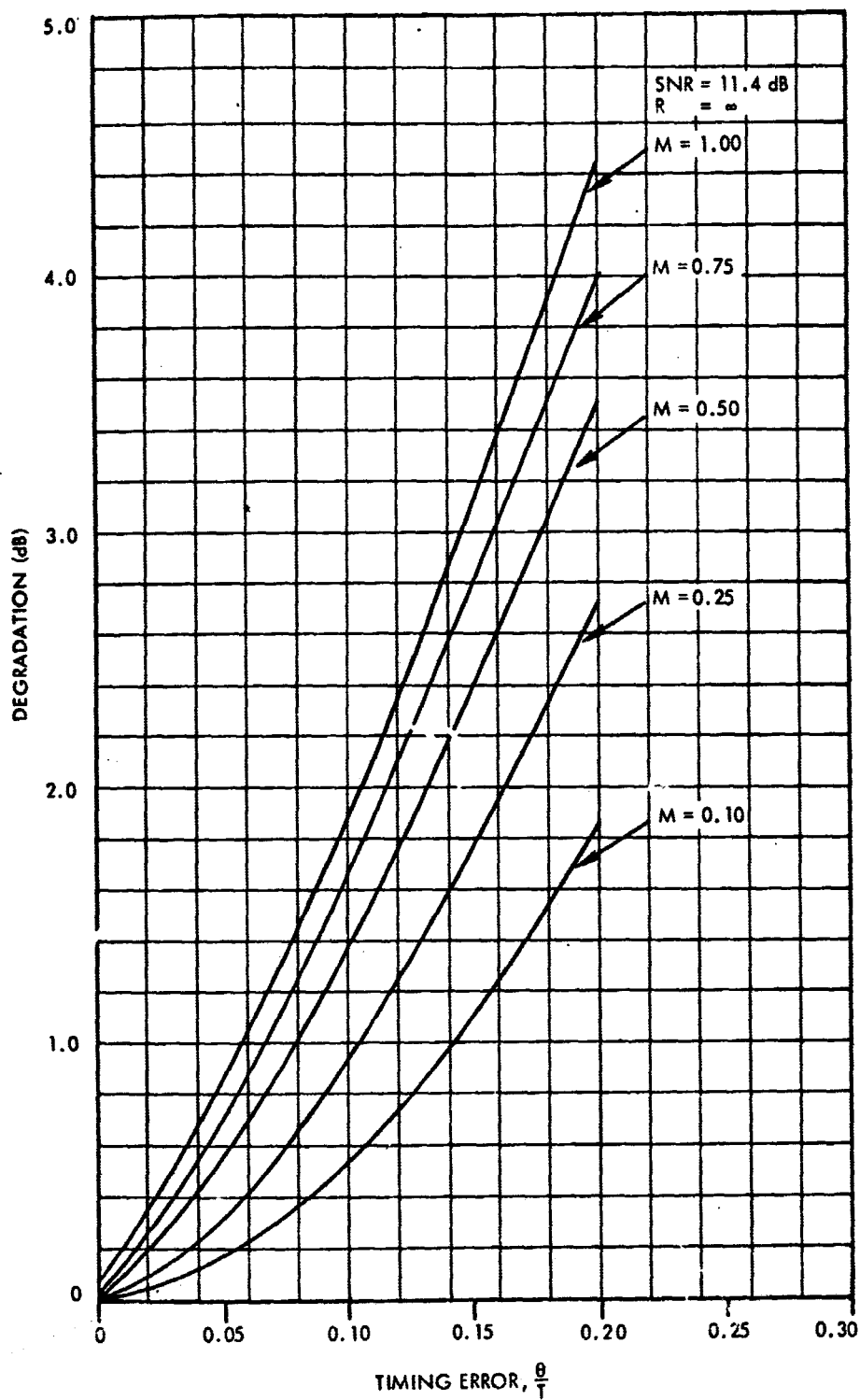


Figure 4.5.54 Performance Degradation Versus Timing Error, Integrate and Dump Bit Detector

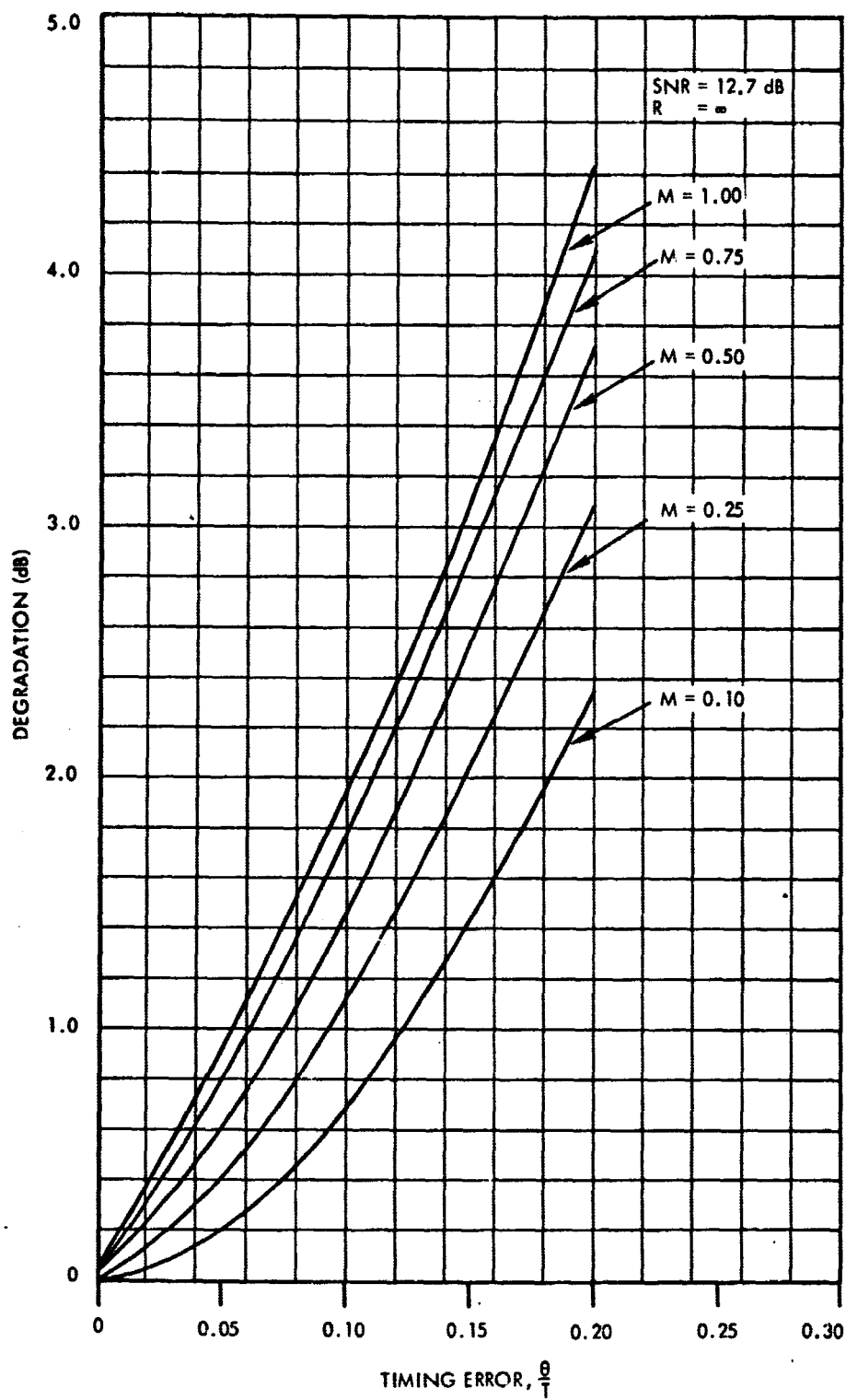


Figure 4.5.55 Performance Degradation Versus Timing Error, Integrate and Dump Bit Detector

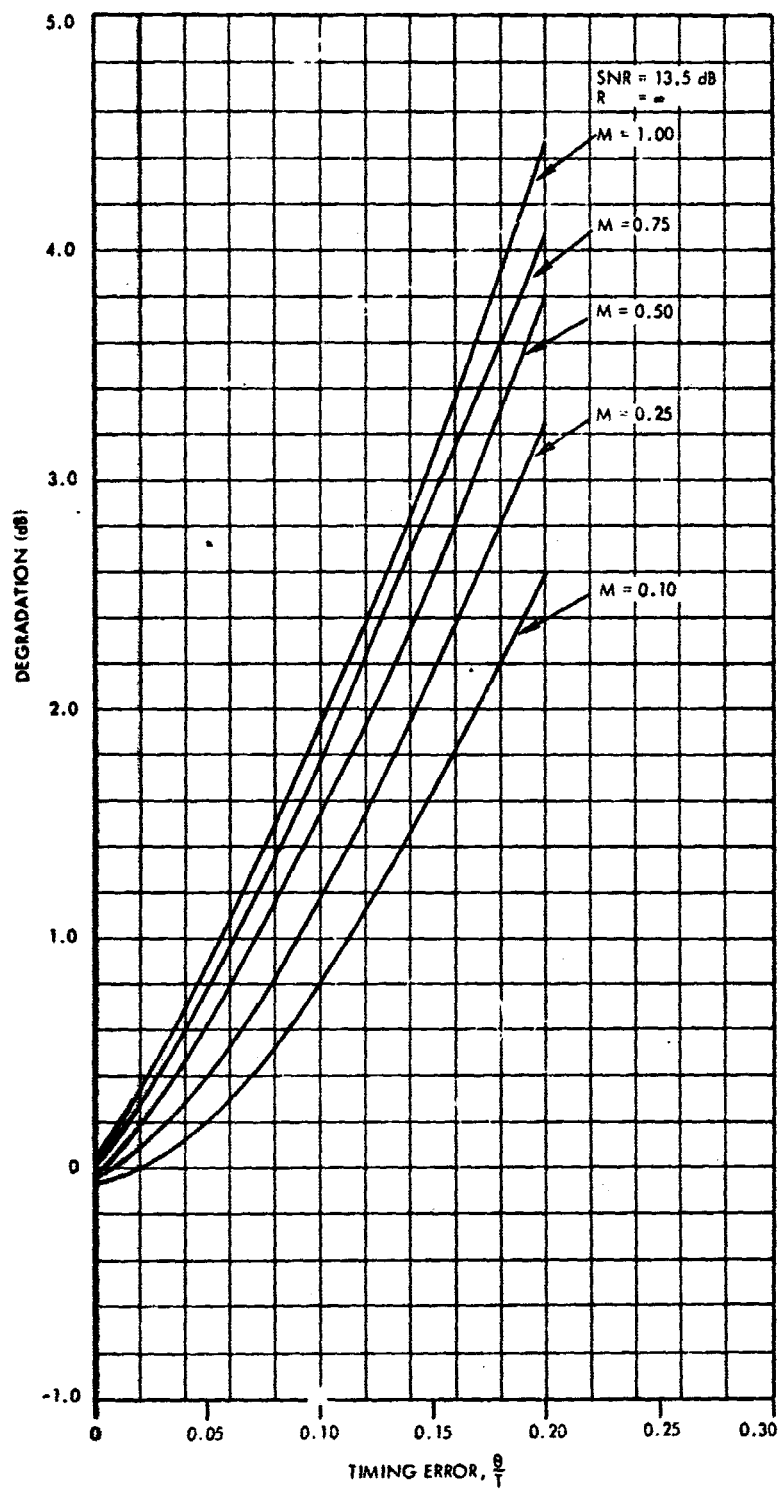


Figure 4.5.56 Performance Degradation Versus Timing Error
Integrate and Dump Bit Detector

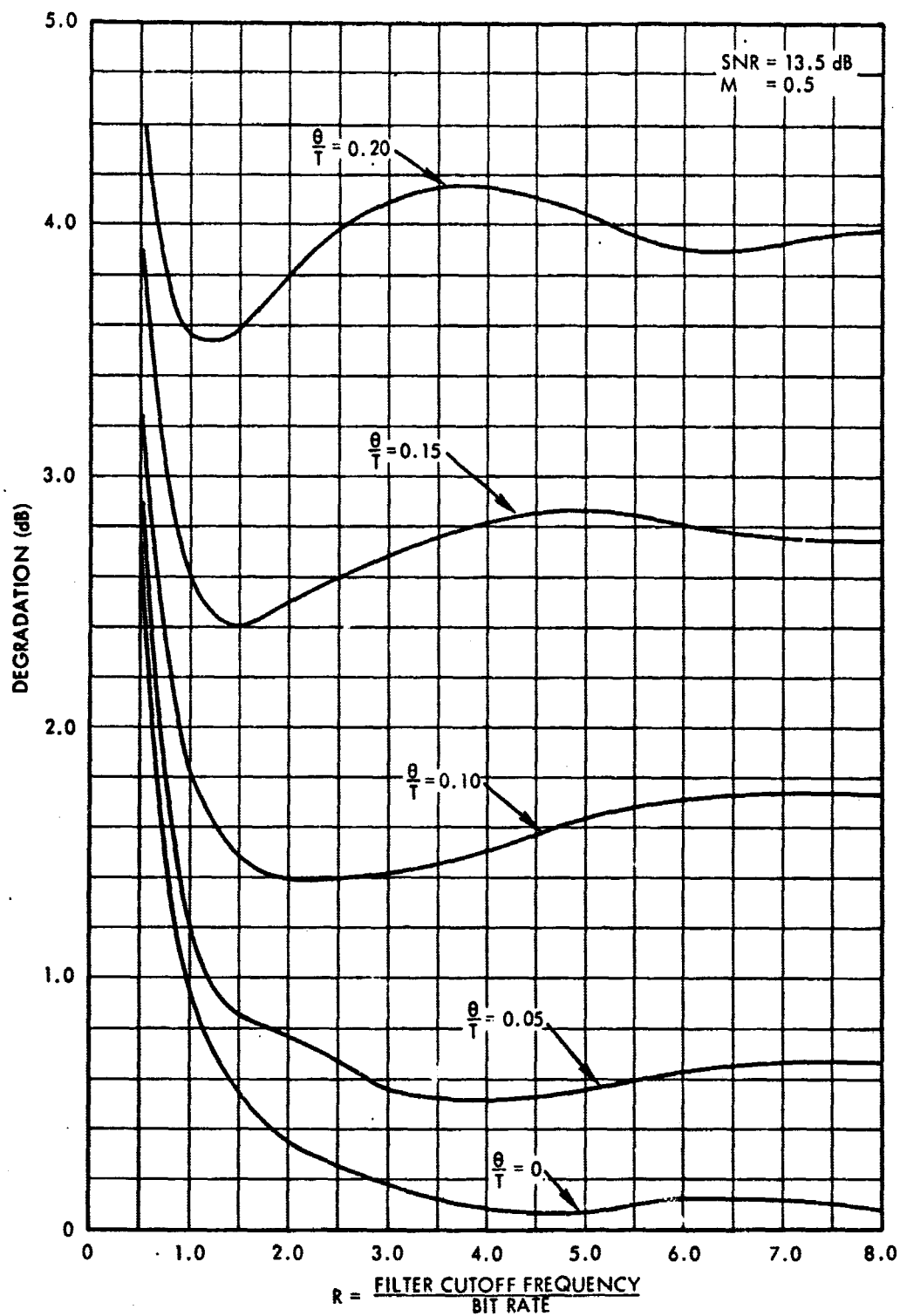


Figure 4.5.57 Performance Degradation due to Timing Error Versus Prefilter Bandwidth; Integrate and Dump Bit Detector Preceded by a Six Pole Butterworth Low Pass Filter

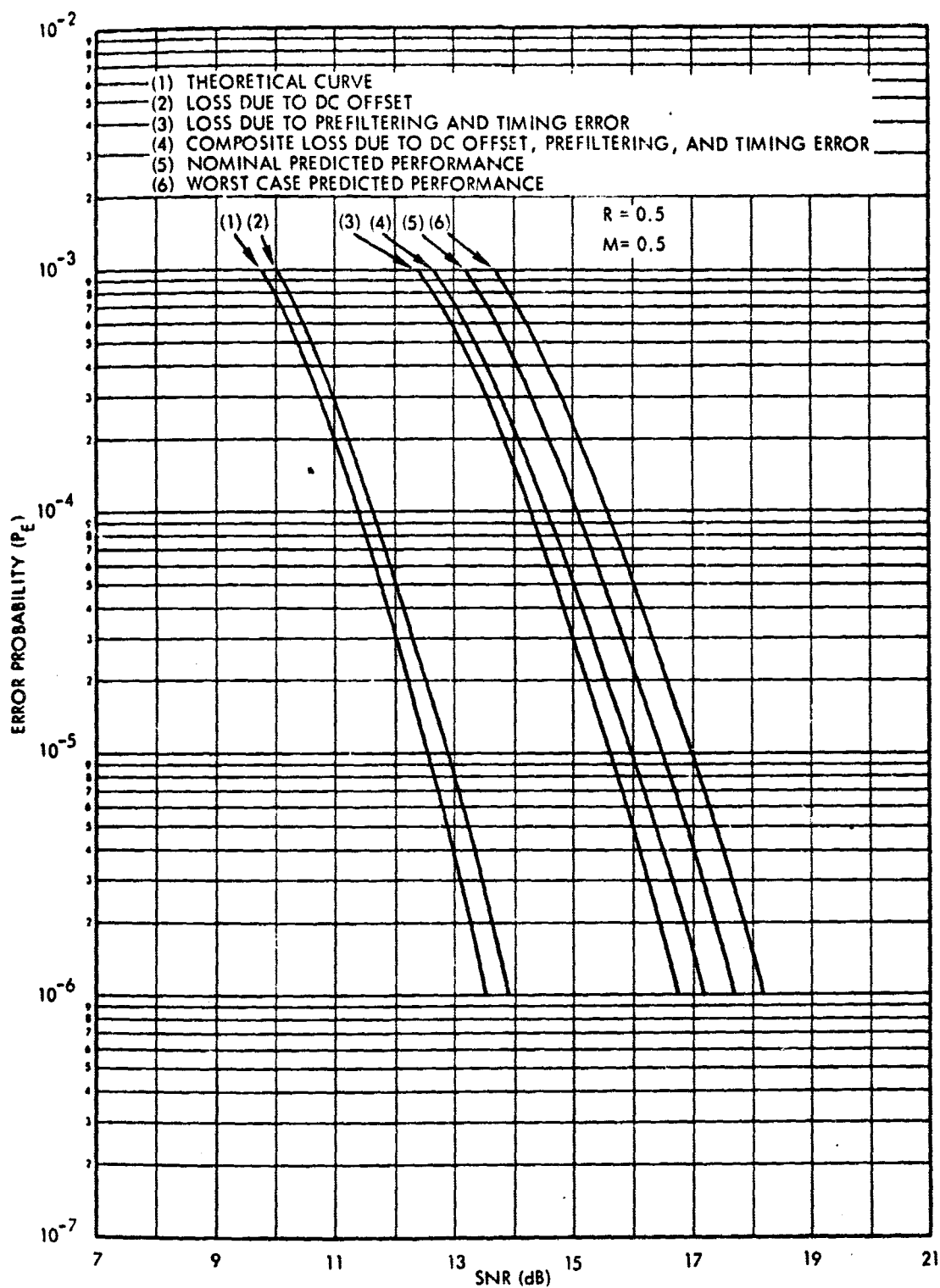


Figure 4.5.58 Predicted Error Probability Versus Signal-to-Noise Ratio, MSFTP-2 Bit Synchronizer, Integrate and Dump Bit Detector

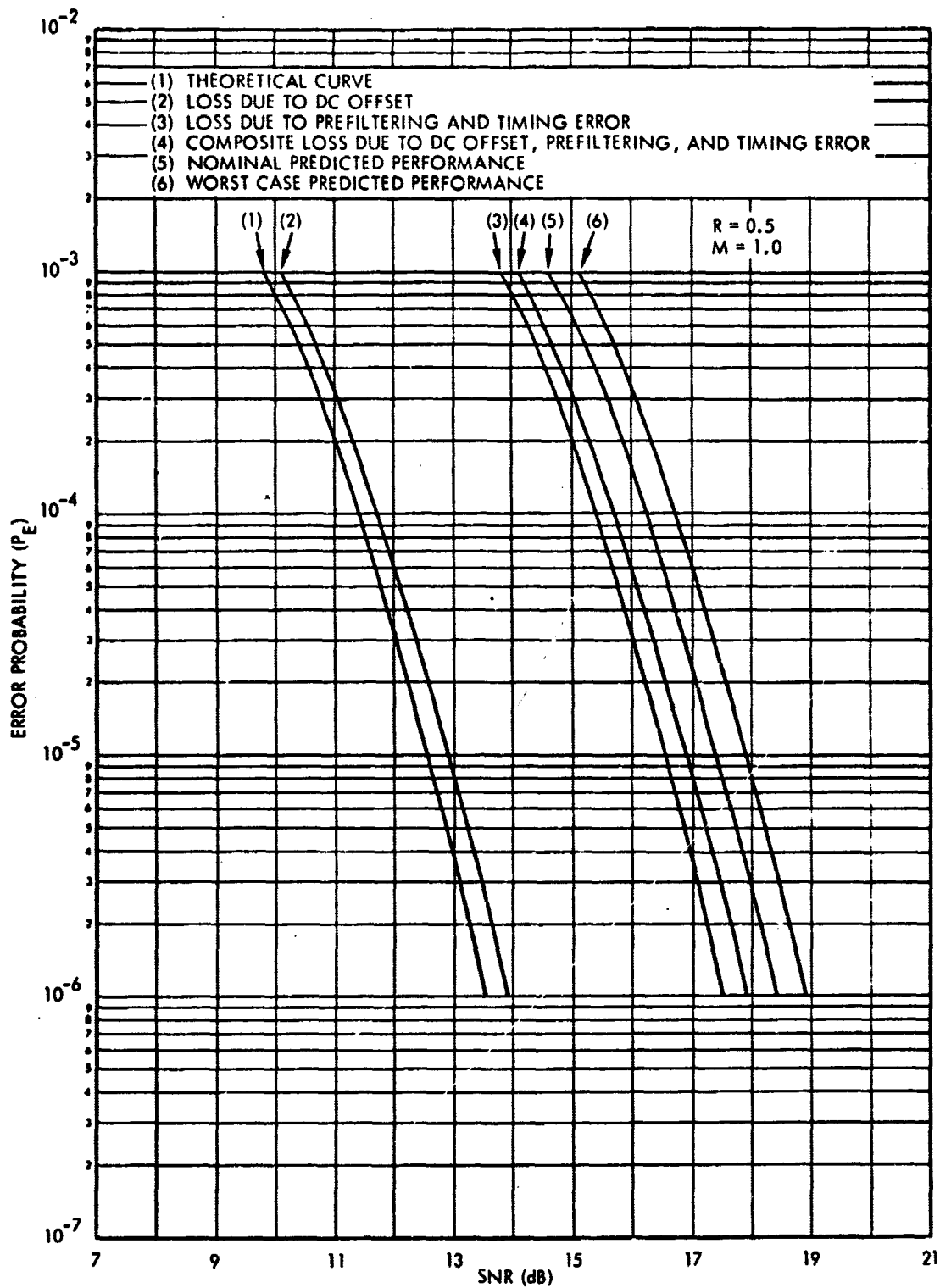


Figure 4.5.59 Predicted Error Probability Versus Signal-to-Noise Ratio, MSFTP-2 Bit Synchronizer, Integrate and Dump Bit Detector

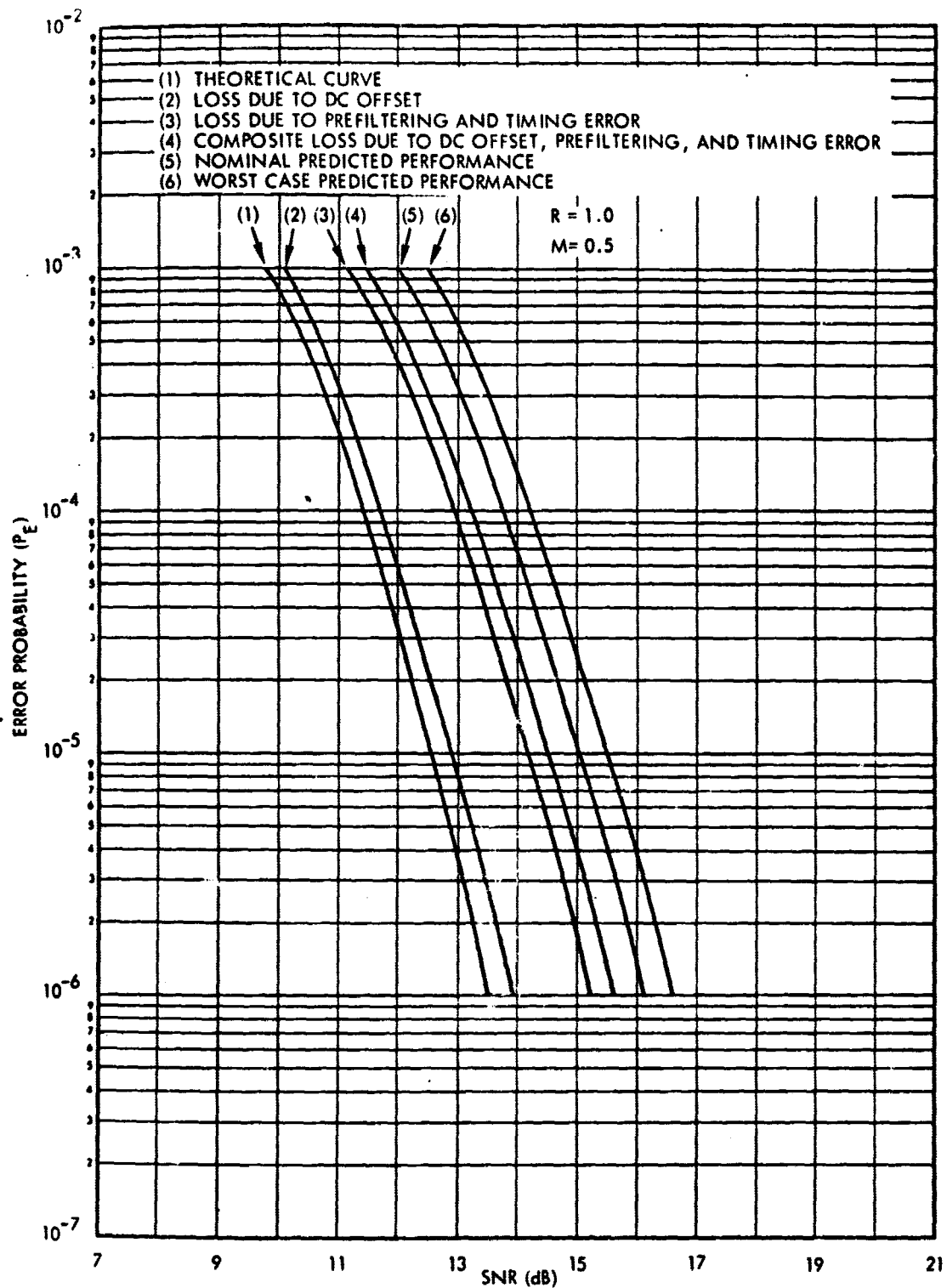


Figure 4.5.60 Predicted Error Probability Versus Signal-to-Noise Ratio, MSFTP-2 Bit Synchronizer, Integrate and Dump Bit Detector

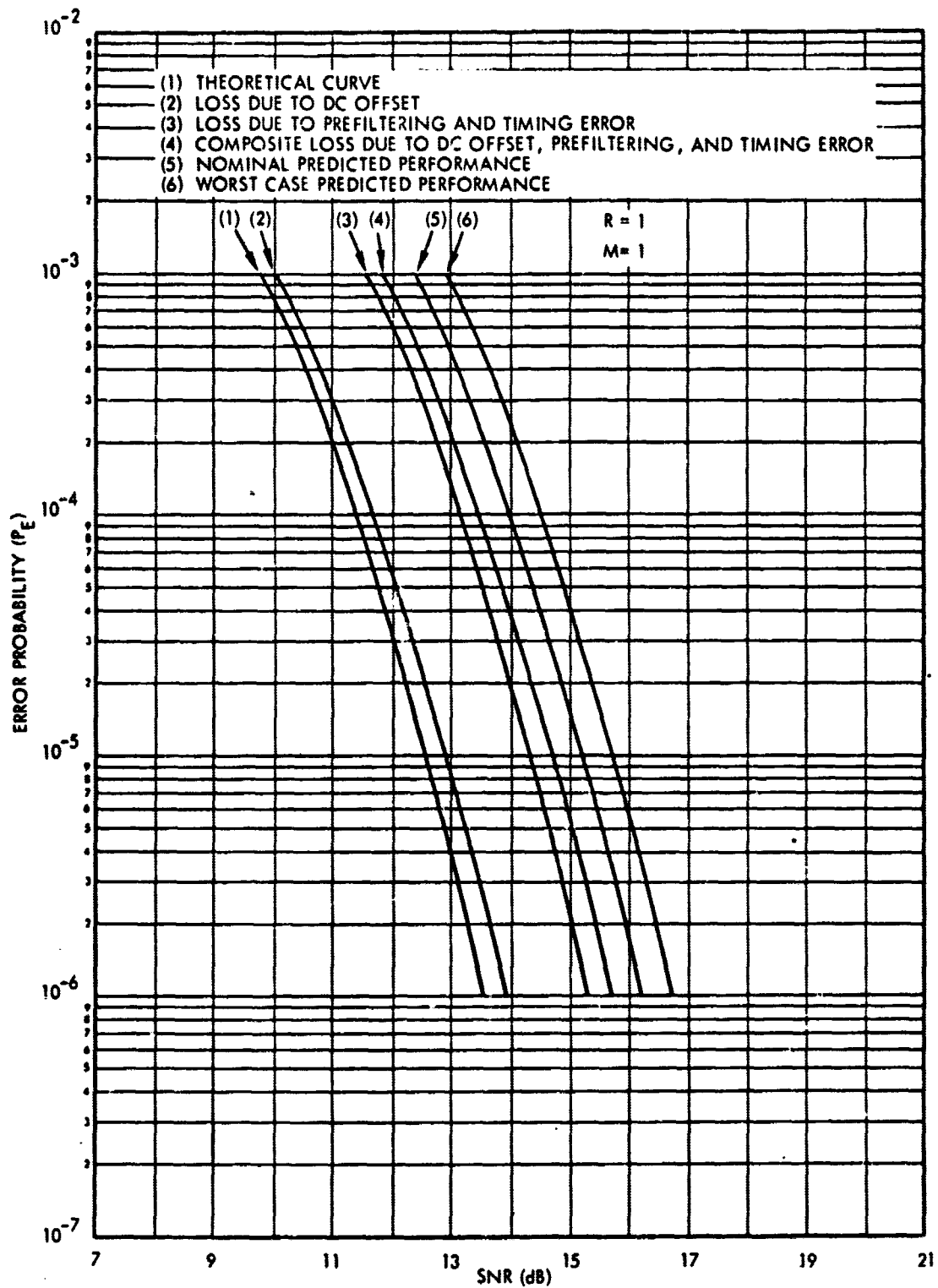


Figure 4.5.61 Predicted Error Probability Versus Signal-to-Noise Ratio, MSFTP-2 Bit Synchronizer, Integrate and Dump Bit Detector

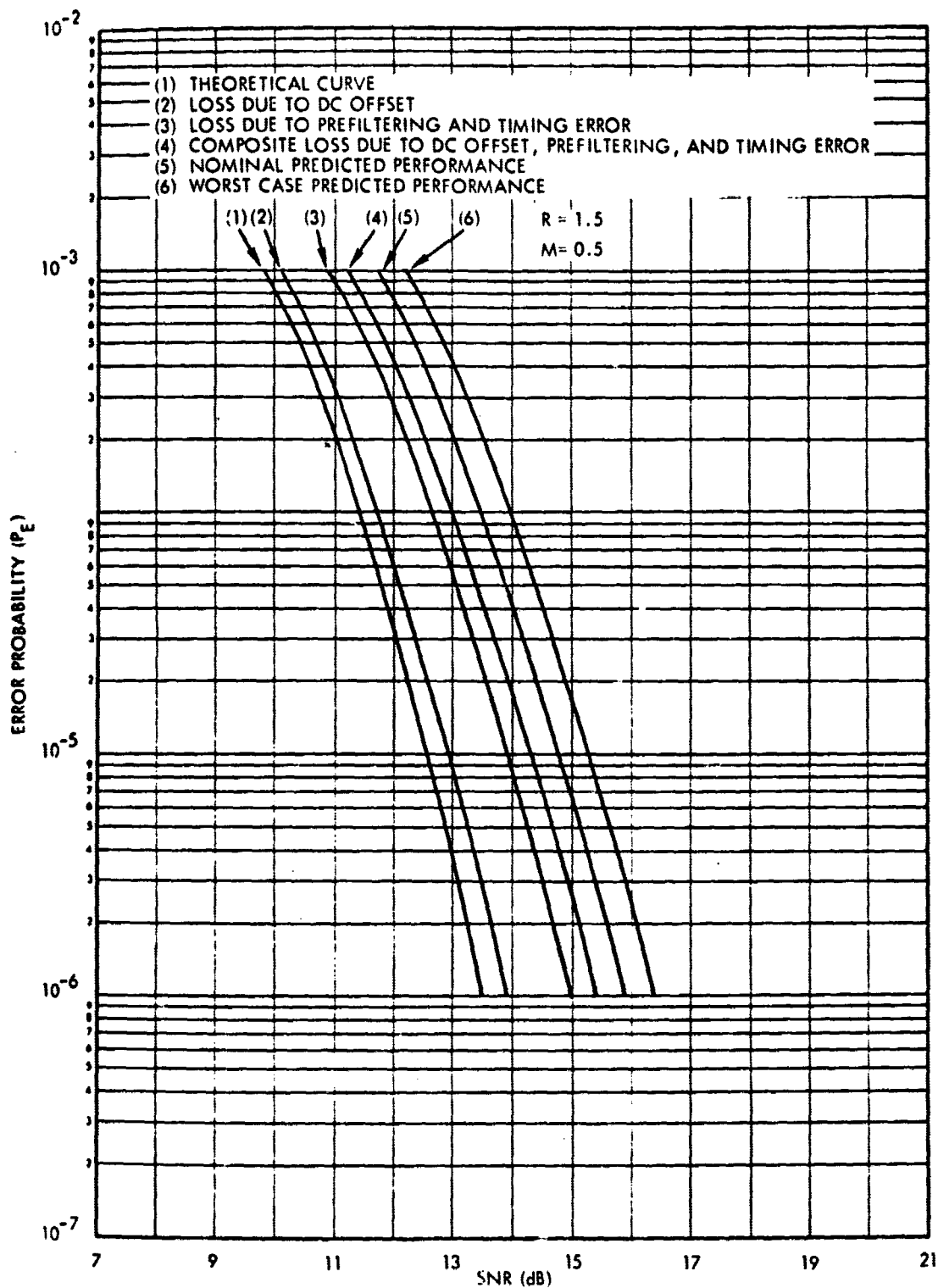


Figure 4.5.62 Predicted Error Probability Versus Signal-to-Noise Ratio, MSFTP-2 Bit Synchronizer, Integrate and Dump Bit Detector

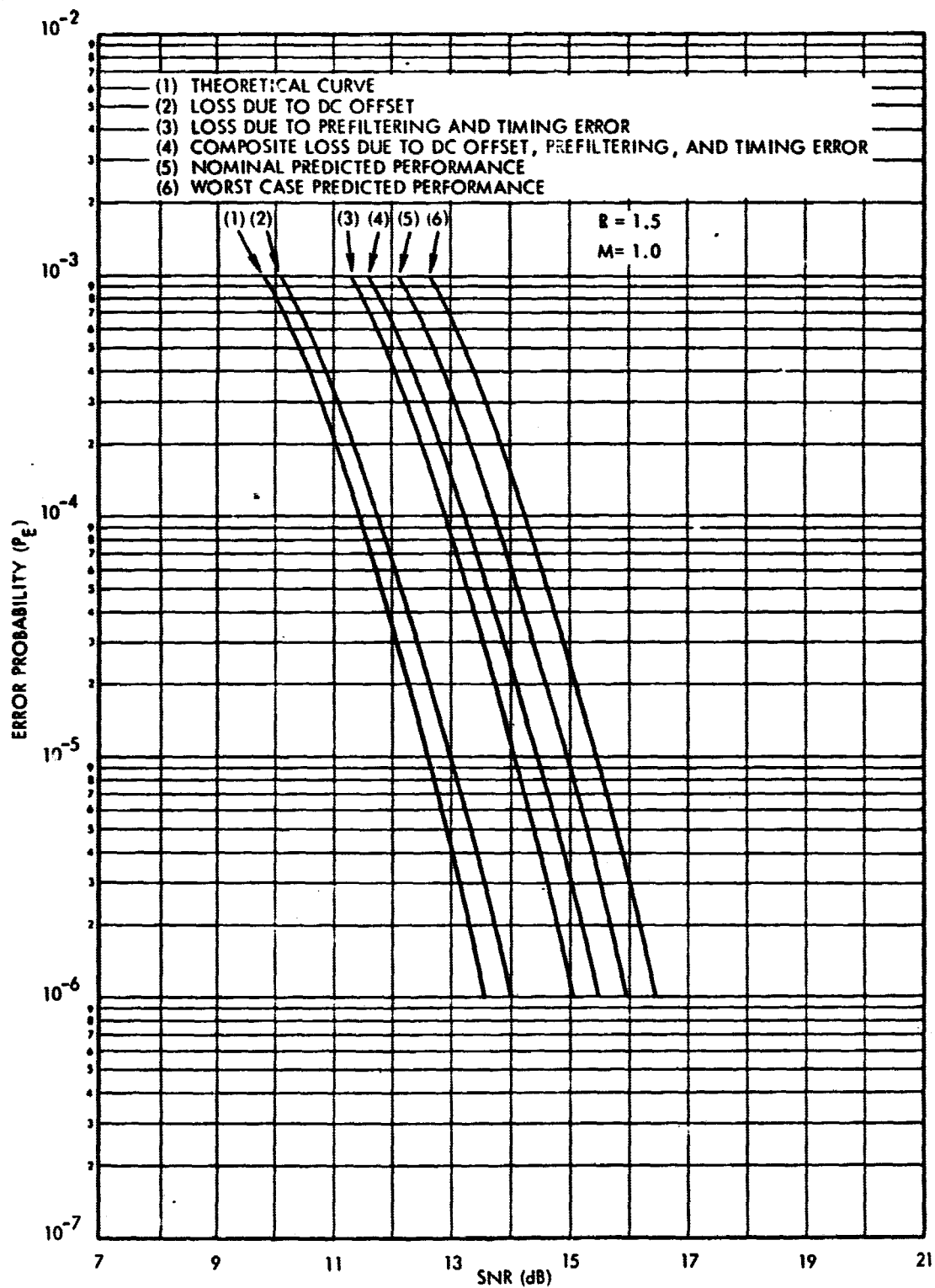


Figure 4.5.63 Predicted Error Probability Versus Signal-to-Noise Ratio, MSFTP-2 Bit Synchronizer, Integrate and Dump Bit Detector

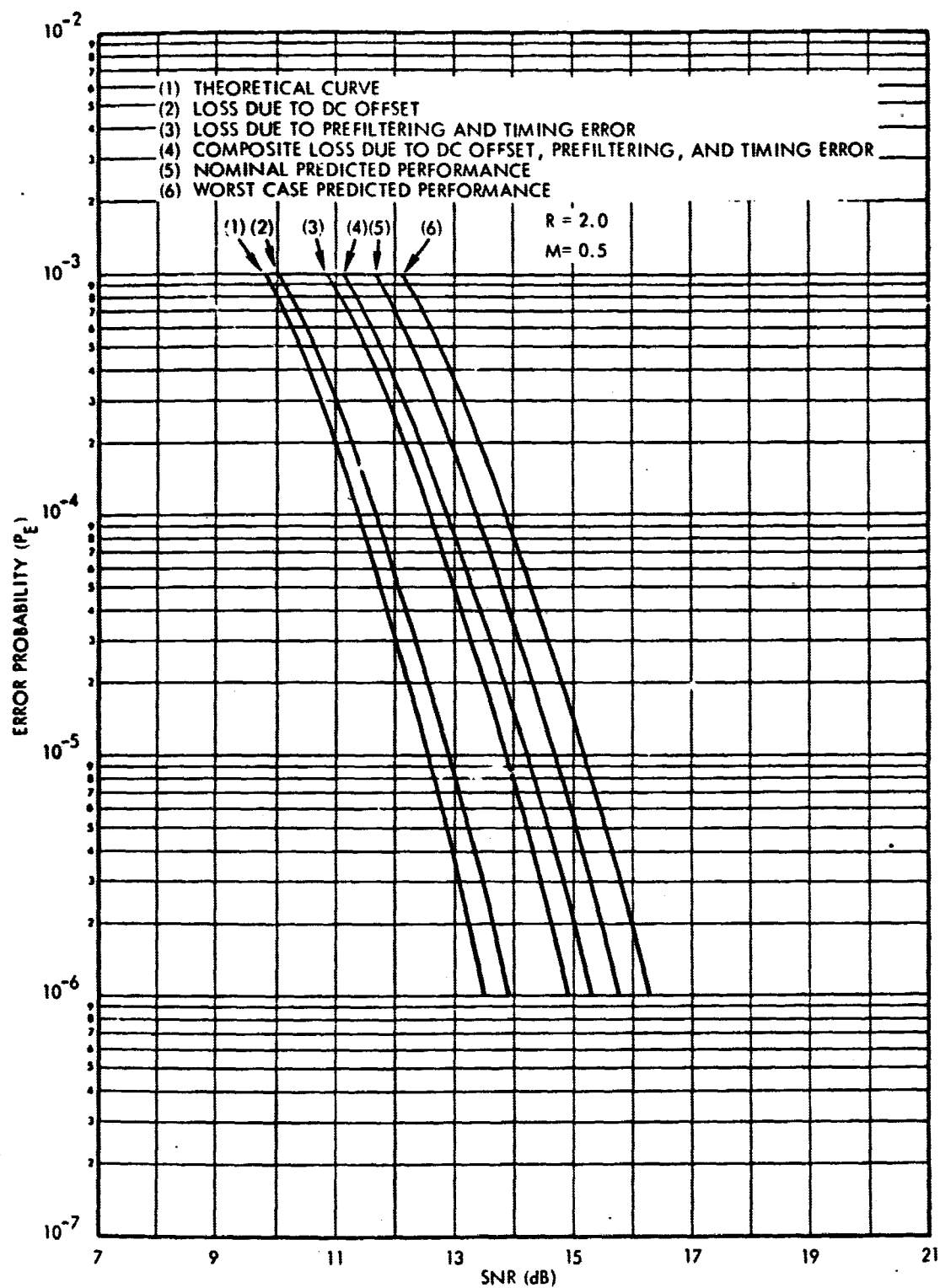


Figure 4.5.64 Predicted Error Probability Versus Signal-to-Noise Ratio, MSFTP-2 Bit Synchronizer, Integrate and Dump Bit Detector

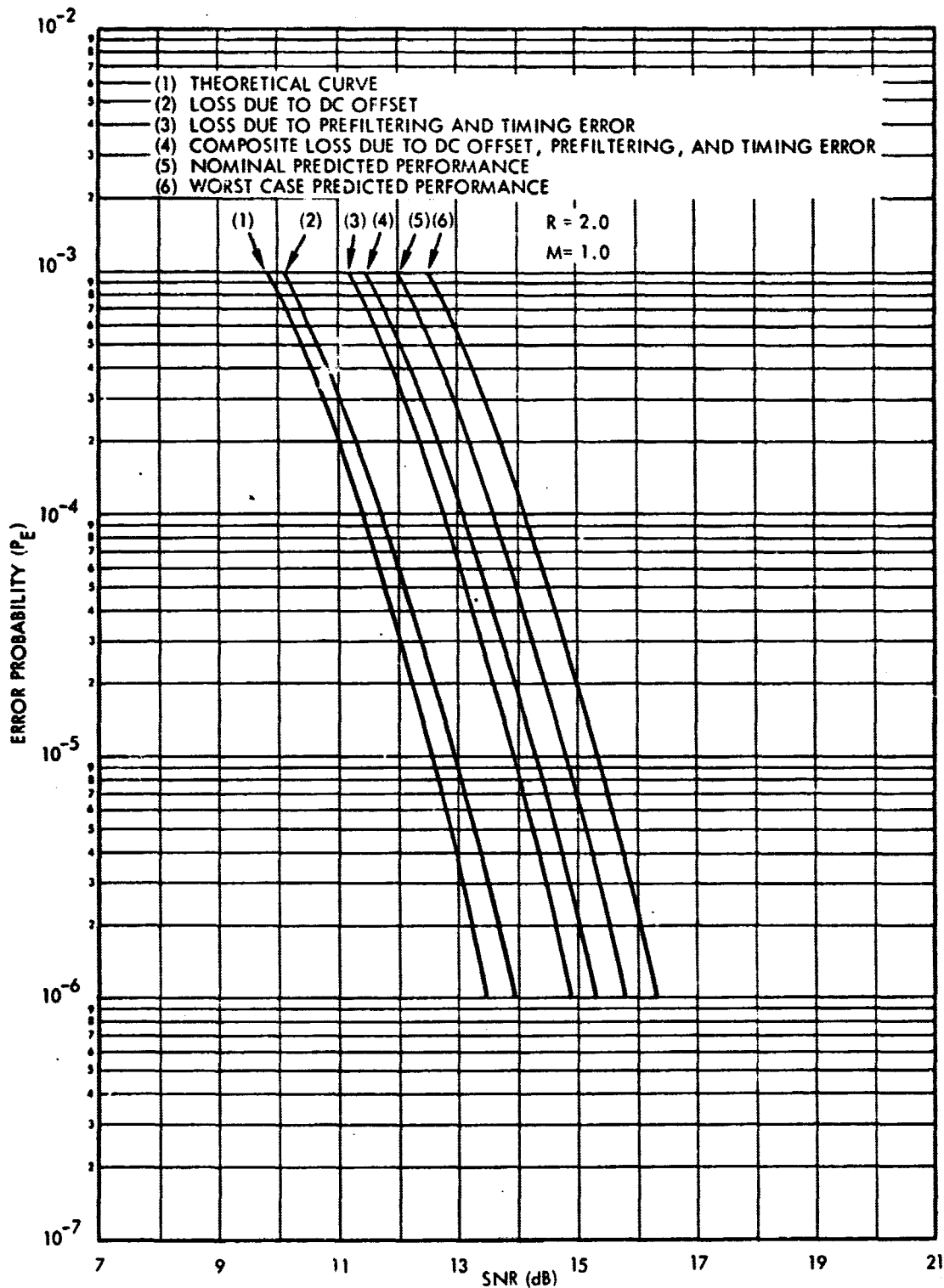


Figure 4.5.65 Predicted Error Probability Versus Signal-to-Noise Ratio, MSFTP-2 Bit Synchronizer, Integrate and Dump Bit Detector.

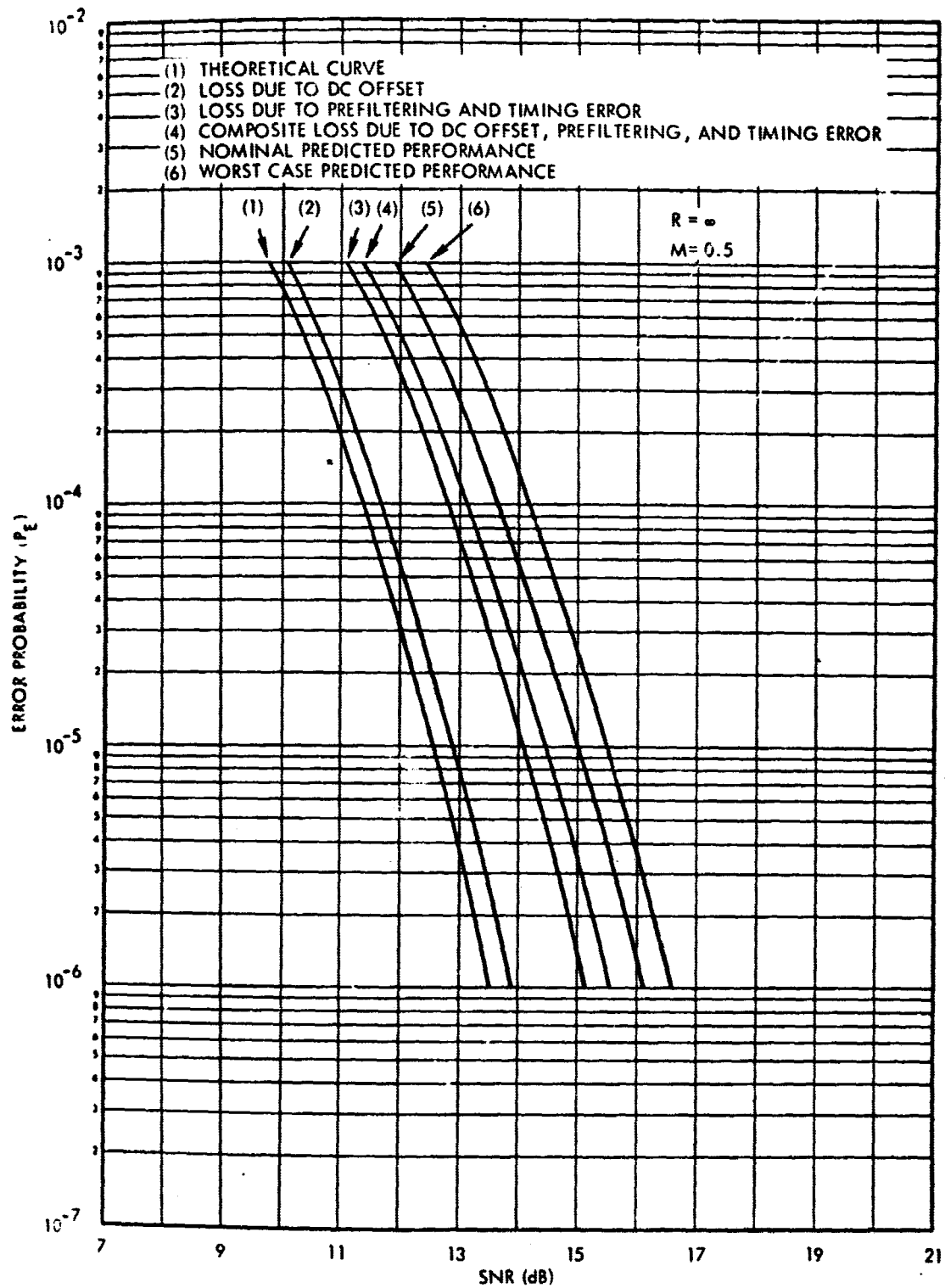


Figure 4.5.66 Predicted Error Probability Versus Signal-to-Noise Ratio, MSFTP-2 Bit Synchronizer, Integrate and Dump Bit Detector

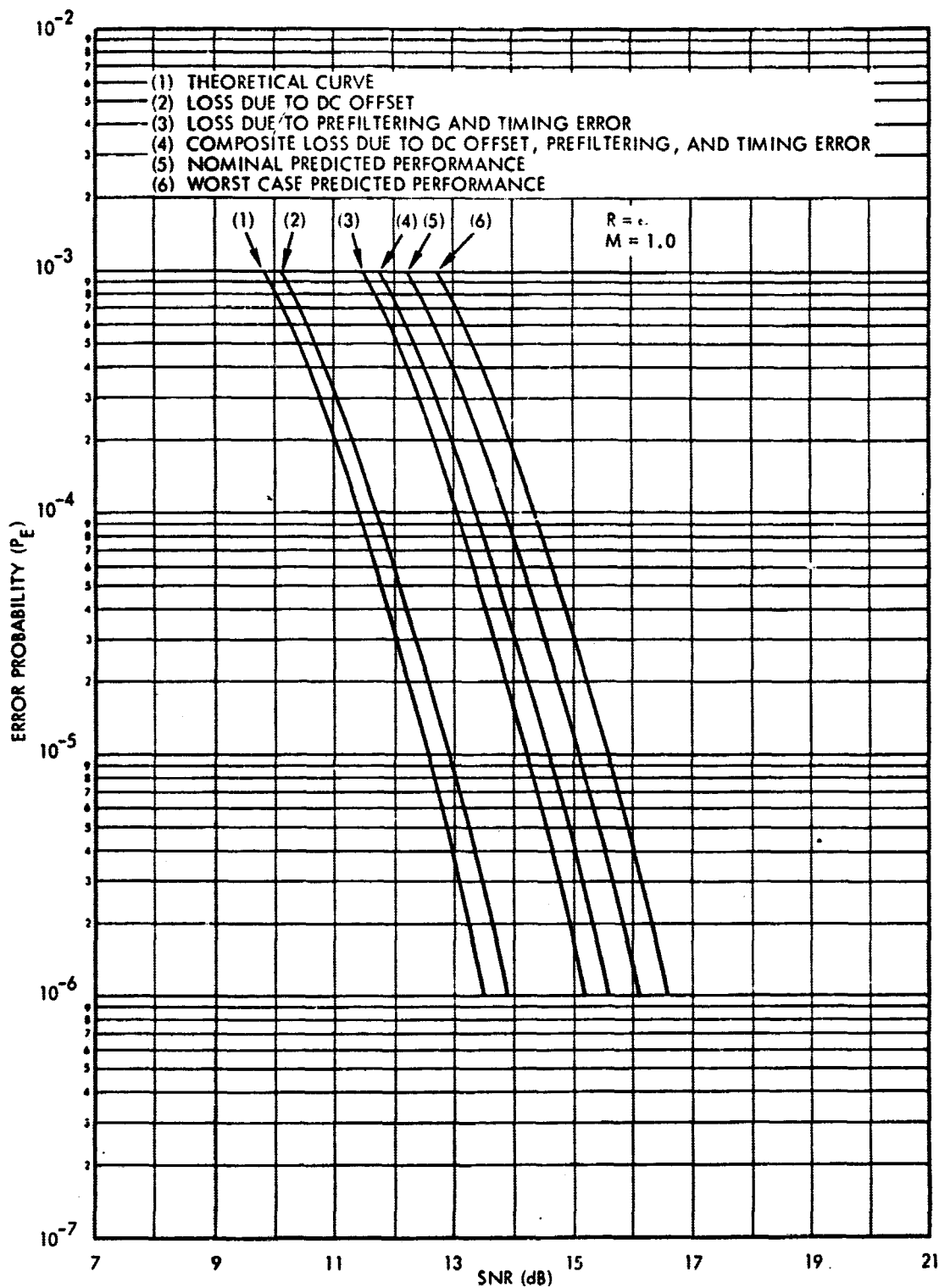


Figure 4.5.67 Predicted Error Probability Versus Signal-to-Noise Ratio, MSFTP-2 Bit Synchronizer, Integrate and Dump Bit Detector

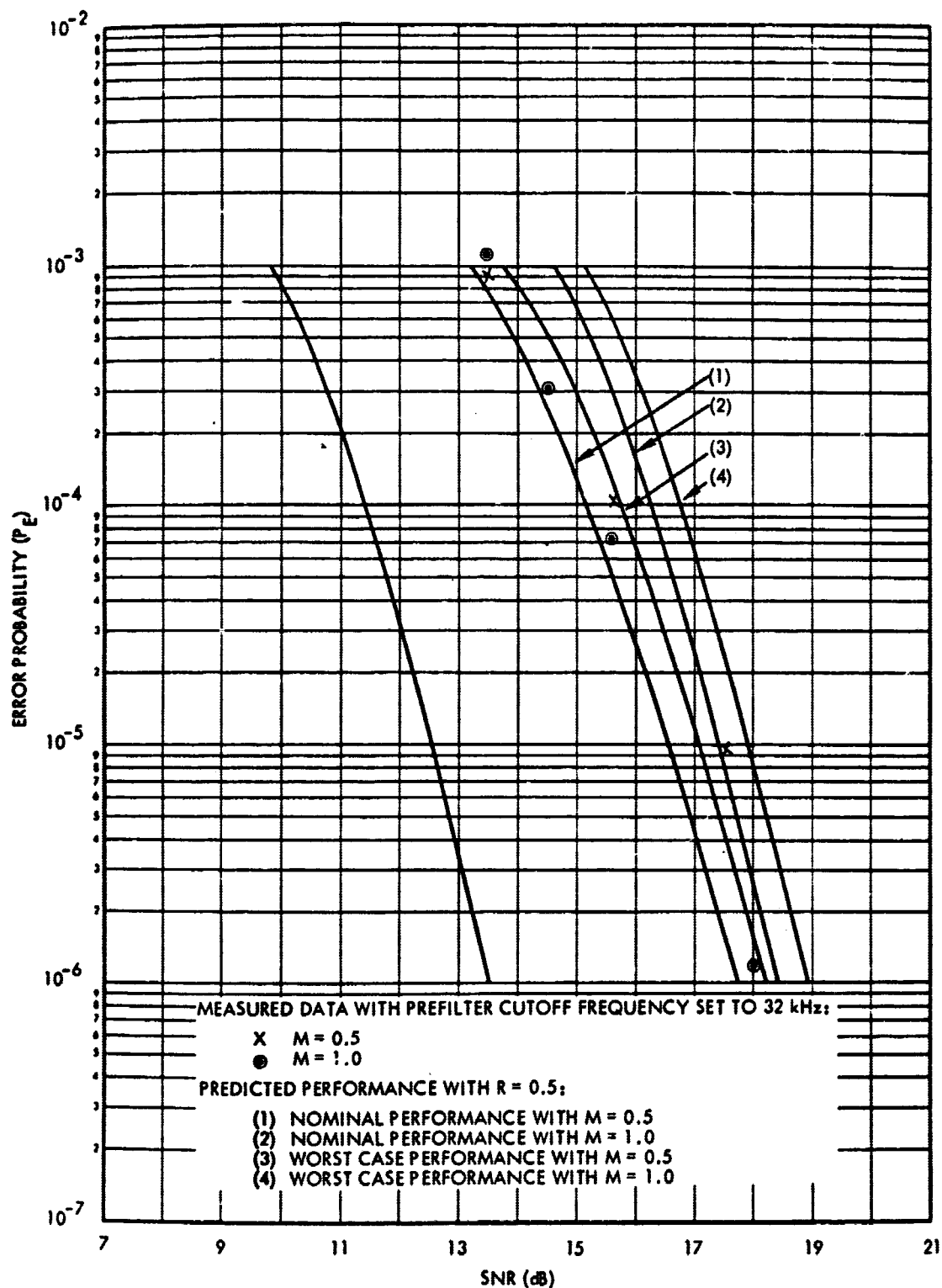


Figure 4.5.68 Measured Data Compared with Predicted Performance, MSFTP-2 Bit Synchronizer, Integrate and Dump Bit Detector

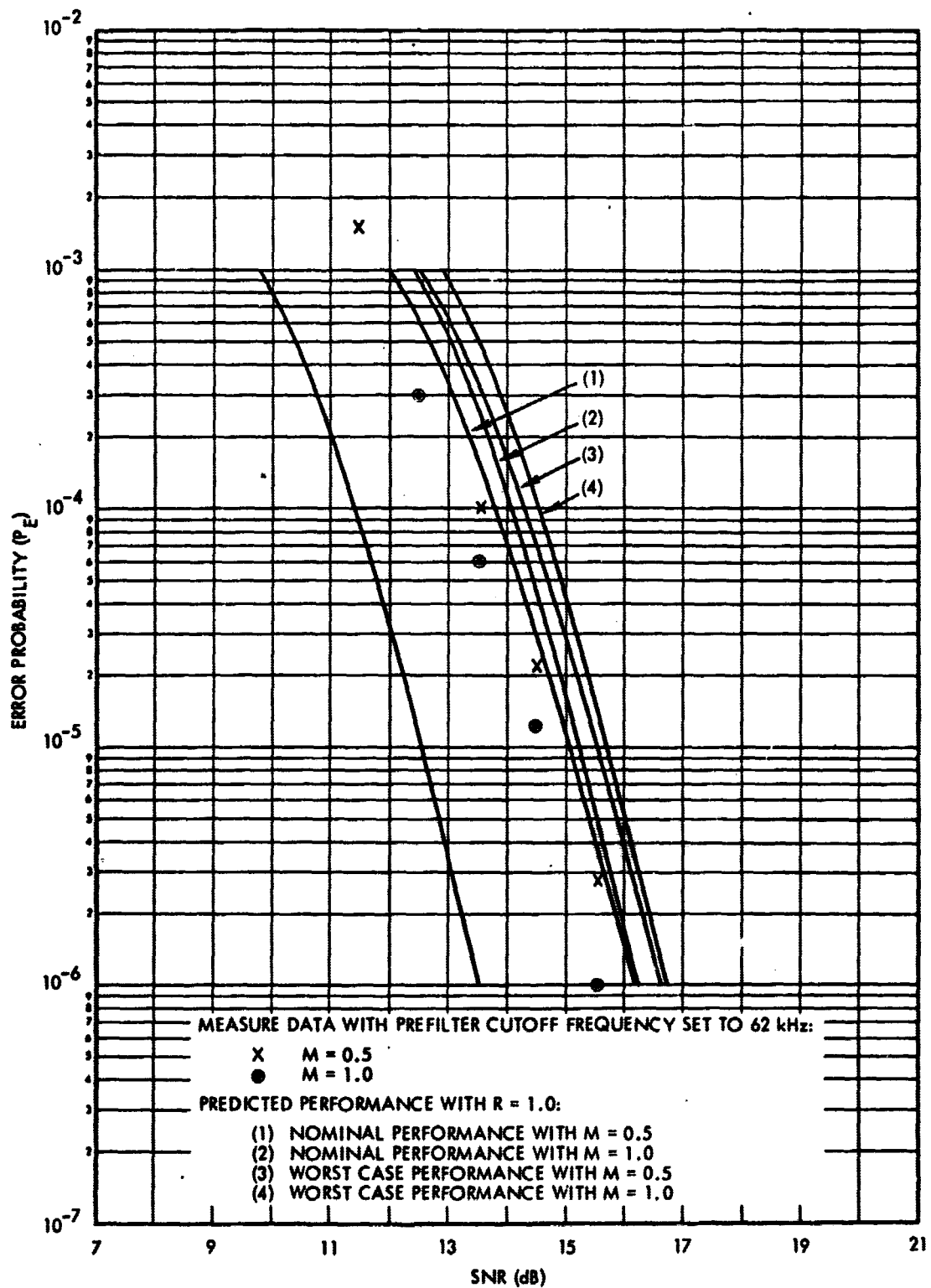


Figure 4.5.69 Measured Data Compared with Predicted Performance, MSFTP-2 Bit Synchronizer, Integrate and Dump Bit Detector

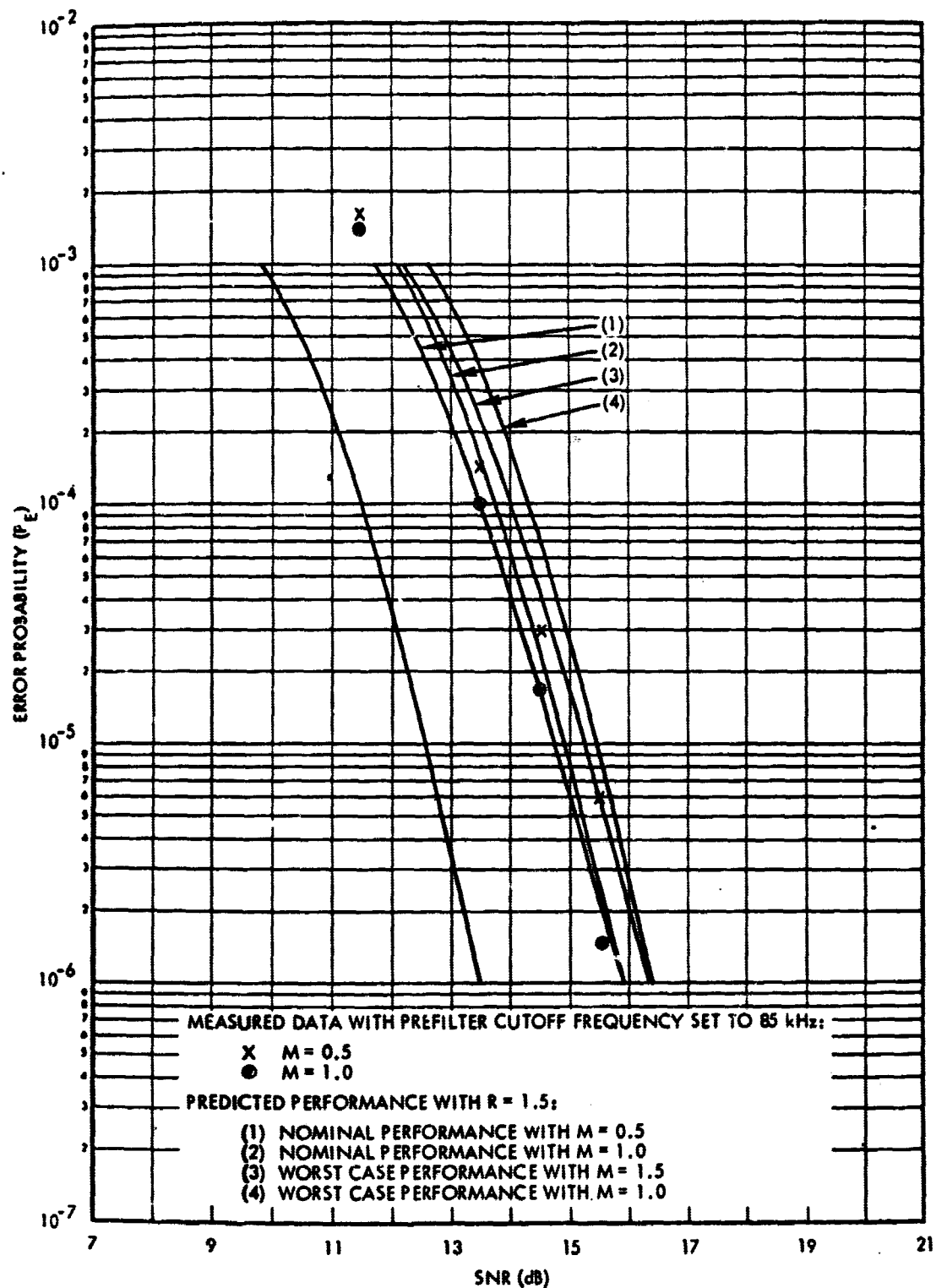


Figure 4.5.70 Measured Data Compared with Predicted Performance, MSFTP-2 Bit Synchronizer, Integrate and Dump Bit Detector

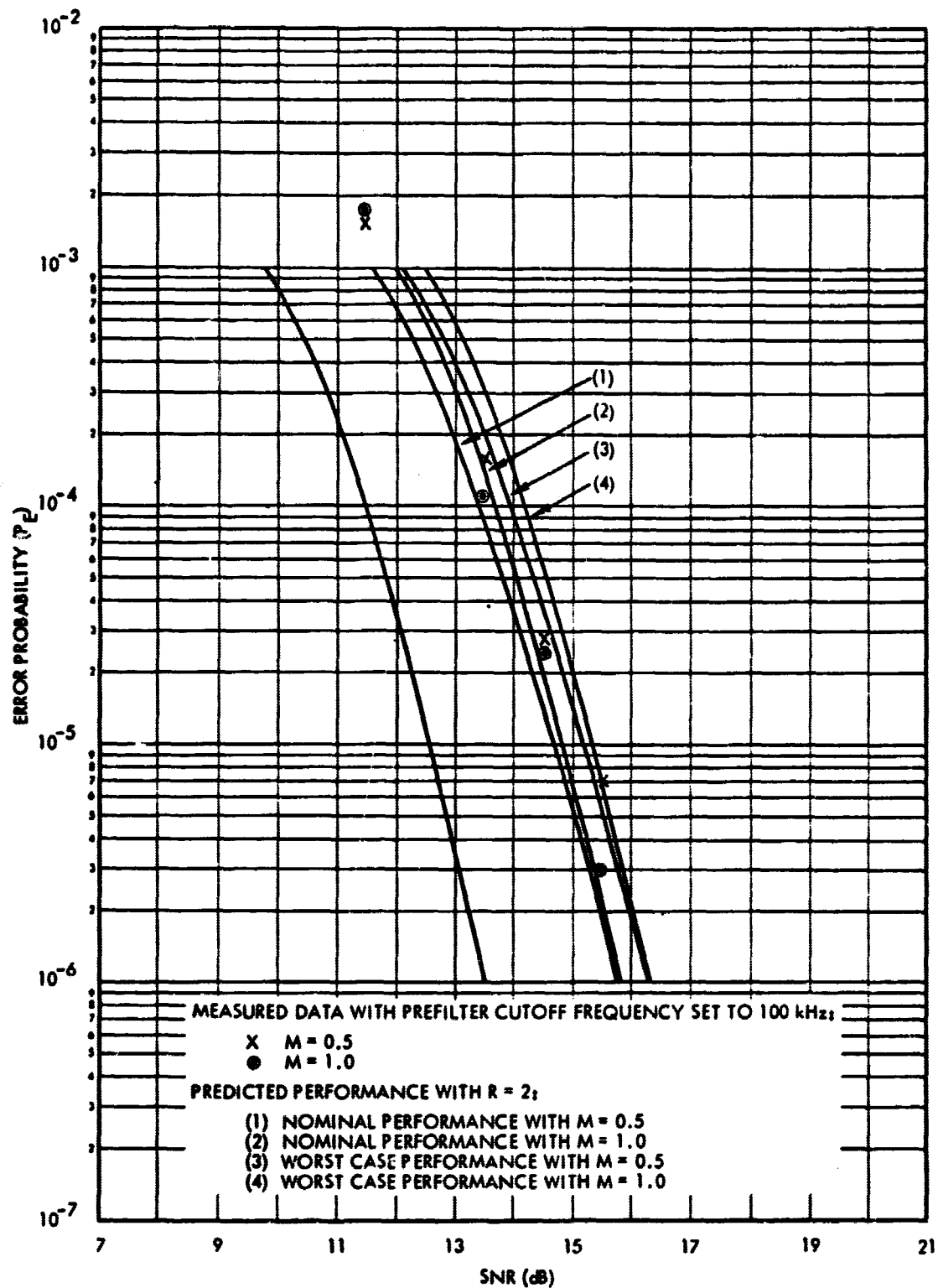


Figure 4.5.71 Measured Data Compared with Predicted Performance, MSFTP-2 Bit Synchronizer, Integrate and Dump Bit Detector

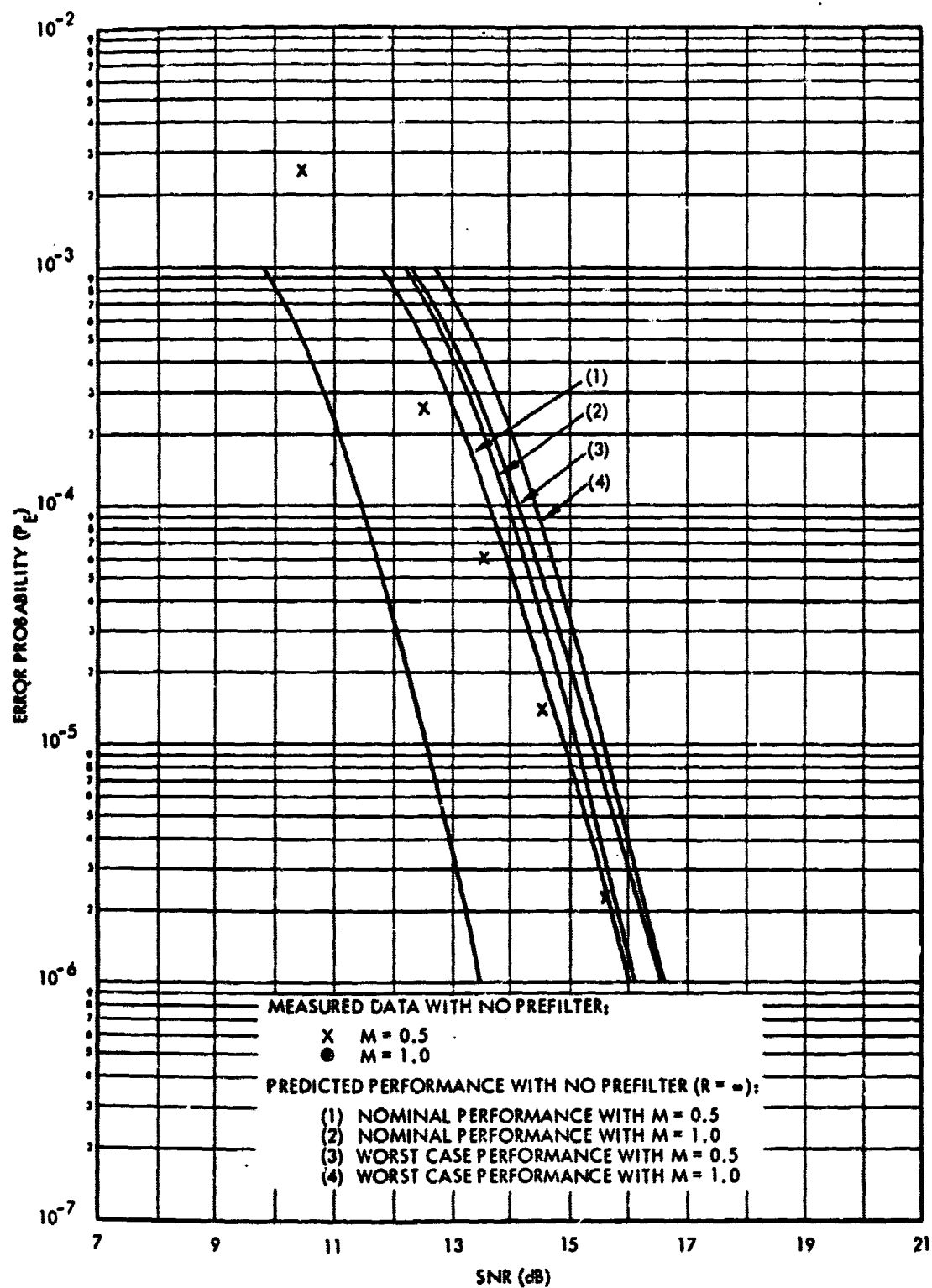


Figure 4.5.72 Measured Data Compared with Predicted Performance, MSFTP-2 Bit Synchronizer, Integrate and Dump Bit Detector

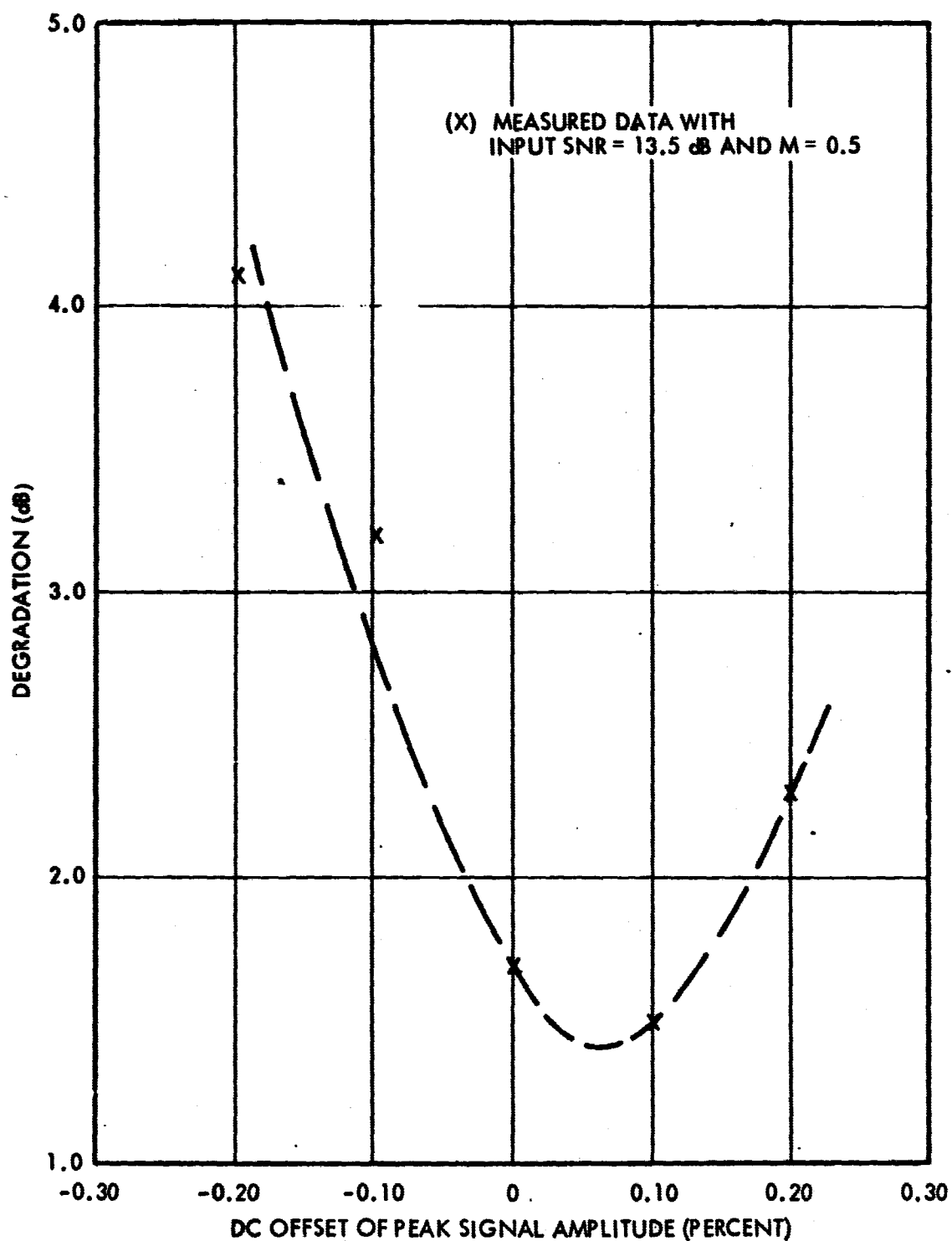


Figure 4.5.73 Measured Performance Degradation Versus DC Offset with Baseline Correction Circuitry Disabled, MSFTP-2 Bit Synchronizer

5.0 PERFORMANCE ANALYSIS UTILIZING FILTER AND SAMPLE BIT DETECTOR

5.1 GENERAL

The MSFTP-2 bit synchronizer filter and sample (F&S) detector is shown in the block diagram of Figure 5.1.1. It consists of the following:

- 1) Tunable Low Pass Filter (TLPF)
- 2) Schmitt Trigger (ST)
- 3) Sample Flip Flop (SF)

The incoming noise contaminated PCM data is applied to the input of the TLPF which, ideally, is tuned to a frequency of one-half the bit rate. The filtered TLPF output is applied to the ST which continuously decides as to the polarity of the TLPF output (positive or negative). The SF, when sampled, assumes the polarity of the ST yielding the detected PCM data.

The sampling signal to the SF is supplied via the clock extraction circuitry and, under idealized conditions, occurs coincident with transitions in the incoming data. The TLPF delay, under ideal conditions, is one-half the bit period such that F&S sampling occurs at the mid bit point of the TLPF output where the signal amplitude is maximum.

Like the I&D detector, discussed in Section 4, the F&S detector performance depends on the following:

- 1) Timing error
- 2) DC offset (including AC offset as equivalent DC offset)
- 3) Prefiltering

Timing error displaces the sample point away from mid bit resulting in increased bit error rates.

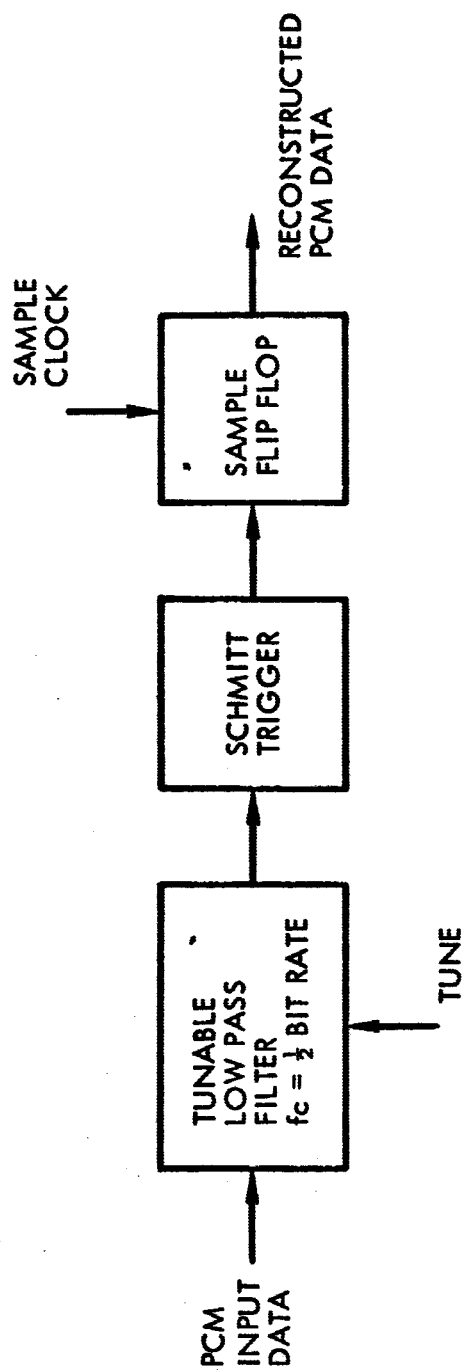


Figure 5.1.1 MSFTP-2 Bit Synchronizer Filter and Sample Bit Detector

DC offset is an increase in signal level to one transmitted symbol and a decrease in signal level to the other. Thus there is an apparent increase in SNR for transmitted "ones" and an apparent decrease in SNR for transmitted "zeros". The resulting performance degradation is discussed in Section 4.2.

It was shown in Section 4.3 that prefiltering of the input PCM data degrades the performance of the I&D detector because it "mismatches" the PCM waveform to the I&D detector. Prefiltering of the PCM data prior to input to the F&S detector has somewhat the opposite effect. Since the F&S detector is not matched to square wave data, prefiltering may improve the F&S performance, or have little effect on it, while it degrades the I&D. Thus prefiltering tends to improve the F&S performance compared to the I&D performance. With heavily filtered input data the F&S may outperform the I&D.

Analysis of the MSFTP-2 F&S detector with prefiltered data is not undertaken in this report because the MSFTP-2 predetection bandwidths are assumed to be considerably wider than the F&S detector bandwidth. The F&S detector cut off frequency is one-half the bit rate while the nominal predetection cut off frequency is of the order of 1.5 times the bit rate. The F&S detector is analyzed for square wave data which is considered to be the "worst case". The idealized performance of the F&S detector with square wave inputs is calculated and compared to the I&D performance. Additionally, the F&S degradation due to DC offsets and timing error are calculated.

5.2 IDEALIZED PERFORMANCE OF THE MSFTP-2 BIT SYNCHRONIZER FILTER AND SAMPLE DETECTOR WITH SQUARE WAVE INPUT DATA

In this section the performance of the MSFTP-2 F&S detector with square wave input data is calculated for no timing errors or DC offset. The results are compared with the theoretical performance of the I&D detector.

It was shown in Section 4.1 that the probability of error for the I&D detector is given by:

$$P_E(\lambda) = 1 - \phi(\lambda) = 1 - \int_{-\infty}^{\lambda} \frac{1}{\sqrt{2\pi}} e^{-\frac{y^2}{2}} dy \quad (4.1.4)$$

where (λ) is the voltage signal-to-noise ratio out of the I&D detector.

$$\lambda = \frac{\text{Peak signal voltage out of detector}}{\text{RMS noise voltage out of detector}}$$

The probability of error of the filter and sample detector, referred to the I&D detector, is:

$$P_E(\lambda) = 1 - \phi\left[\lambda\left(\frac{a}{b}\right)\right] \quad (5.2.1)$$

$$P_E(\lambda) = 1 - \int_{-\infty}^{\lambda \frac{a}{b}} \frac{1}{\sqrt{2\pi}} e^{-\frac{y^2}{2}} dy \quad (5.2.2)$$

where:

"a" (the signal loss factor) is the ratio of signal voltage out of the F&S detector at sampling to the signal voltage out of the I&D detector at sampling.

$$a = \frac{\text{Sampled signal voltage out of F\&S}}{\text{Sampled signal voltage out of I\&D}}$$

"b" (the noise improvement factor) is the square root of the ratio of the F&S and I&D detector noise bandwidth.

$$b = \left[\frac{\text{F\&S noise bandwidth}}{\text{I\&D noise bandwidth}} \right]^{1/2}$$

The factors (a) and (b) are determined from Appendix E, the analysis of the tunable low pass filter.

Figure E-6 shows the response of the filter to a step and to a pulse one bit period wide. Assuming that the F&S detector input is unfiltered PCM data of variable transition density, the response of the F&S filter can be approximated by the step and pulse responses of Figure E-6. Four possible waveforms, over a bit time, appear at the F&S filter output and are sampled at time (T). The four waveforms are illustrated in Figure 5.2.1. The conditions for each waveform are as follows:

Waveform (1) Adjacent transitions (pulse)

Waveform (2) Lack of transition followed by transition

Waveform (3) Transition followed by lack of transition

Waveform (4) Lack of adjacent transitions

The (a) factors of Equation 5.2.1 are then the ratio of the value of each of the waveforms at sampling to the voltage output of the I&D with unity square wave inputs. Since the I&D voltage output with unity square wave inputs is unity, the (a) factors are simply the values of the waveforms at sampling and are read from Figure E-6 as follows:

$$a_1 = 1.11 \text{ (value of pulse response at } \frac{t}{T} = 1)$$

$$a_2 = 1 \text{ (value of step response at } \frac{t}{T} = 0)$$

$$a_3 = 1.11 \text{ (value of step response at } \frac{t}{T} = 1)$$

$$a_4 = 1$$

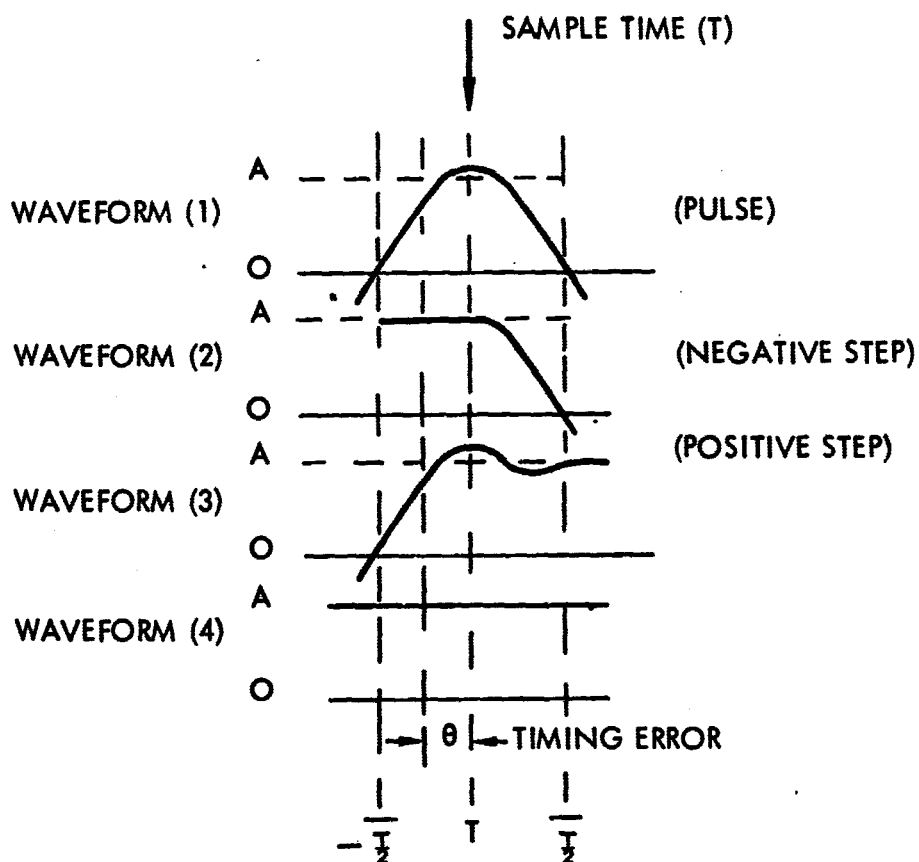


Figure 5.2.1 Illustrating Output Waveforms of Tunable Low Pass Filter with Unfiltered PCM Input

The effective noise bandwidth is shown in Section 3.0 of Appendix E to be 0.785 times the bit rate. Since the I&D detector noise bandwidth is one-half the bit rate the (b) factor of equation 5.2.1 is:

$$b = \left[\frac{0.758}{0.5} \right]^{1/2} = [1.57]^{1/2} = 1.26$$

Equation 5.2.1, for the four possible waveforms, becomes:

$$P_E(\lambda) = 1 - \alpha_1 \phi \left[\lambda \left(\frac{a_1}{b} \right) \right] - \alpha_2 \phi \left[\lambda \left(\frac{a_2}{b} \right) \right] - \alpha_3 \phi \left[\lambda \left(\frac{a_3}{b} \right) \right] \\ - \alpha_4 \phi \left[\lambda \left(\frac{a_4}{b} \right) \right] \quad (5.2.3)$$

where α_1 through α_4 are the probabilities of occurrence of waveforms (1) through (4) respectively and (from Section 4.3.4) are:

$$\alpha_1 = M^2$$

$$\alpha_2 = \alpha_3 = (M)(1 - M)$$

$$\alpha_4 = (1 - M)^2$$

where M = transition density.

The final equation for probability of error for the MSFTP-2 bit synchronizer with unfiltered input data is:

$$P_E = 1 - M^2 \phi \left[\lambda \left(\frac{1.11}{1.26} \right) \right] - M(1 - M) \phi \left[\lambda \left(\frac{1}{1.26} \right) \right] \\ - M(1 - M) \phi \left[\lambda \left(\frac{1.11}{1.26} \right) \right] - (1 - M)^2 \phi \left[\lambda \left(\frac{1}{1.26} \right) \right] \quad (5.2.4)$$

The error probability and the degradation in db, versus SNR, for various transition densities, were calculated from Equation 5.2.4 using the computer routine of Appendix H. The results are shown in Figure 5.2.2 and 5.2.3. Figure 5.2.2 shows calculated error probability versus SNR and Figure 5.2.3 shows the degradation in (db) (referred to the I&D theoretical) versus SNR.

From the curves it is seen that the calculated performance of the MSFTP-2 bit synchronizer F&S detector, with square wave inputs and 50% transition density, is approximately 2 db worse than the theoretical for the I&D detector.

5.3 PERFORMANCE DEGRADATION OF FILTER AND SAMPLE DETECTOR DUE TO DC OFFSETS

The performance degradation of the F&S detector due to DC offsets is determined from the analysis of performance degradation due to DC offset of Section 4.2 and from the DC analysis and error budget of Appendix B.

In Appendix B it is shown that the worst case expected DC offset error (r) in the F&S detector is 6% of peak signal amplitude. Using this value, the degradation is read from Figure 4.5.1b and is as follows:

<u>SNR (db)</u>	<u>Degradation (db)</u>
9.8	0.13
11.4	0.19
13.5	0.24

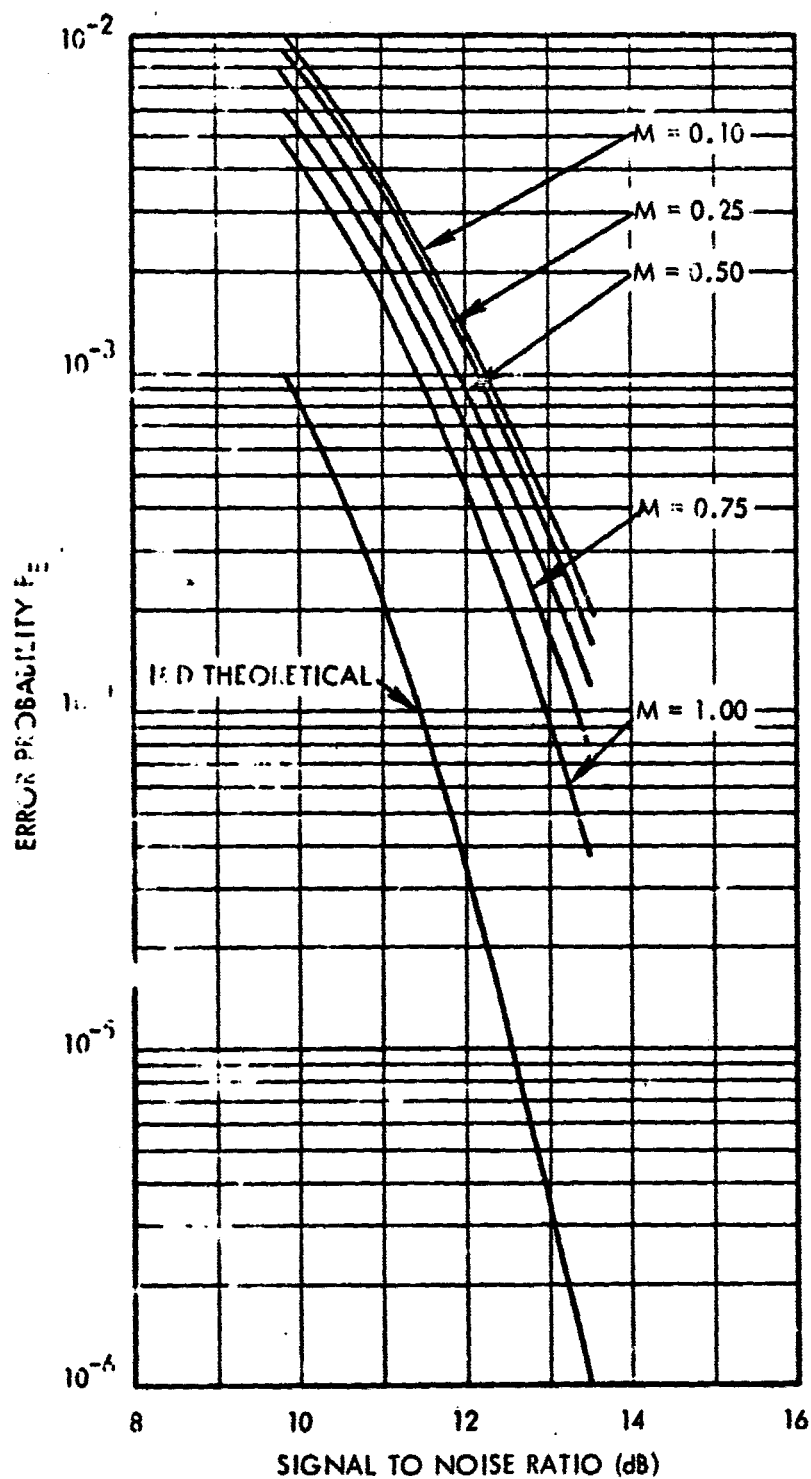


Figure 5.2.2 Probability of Error Versus SNR; MSFTP-2 Bit Synchronizer Filter and Sample Detector with Unfiltered Data

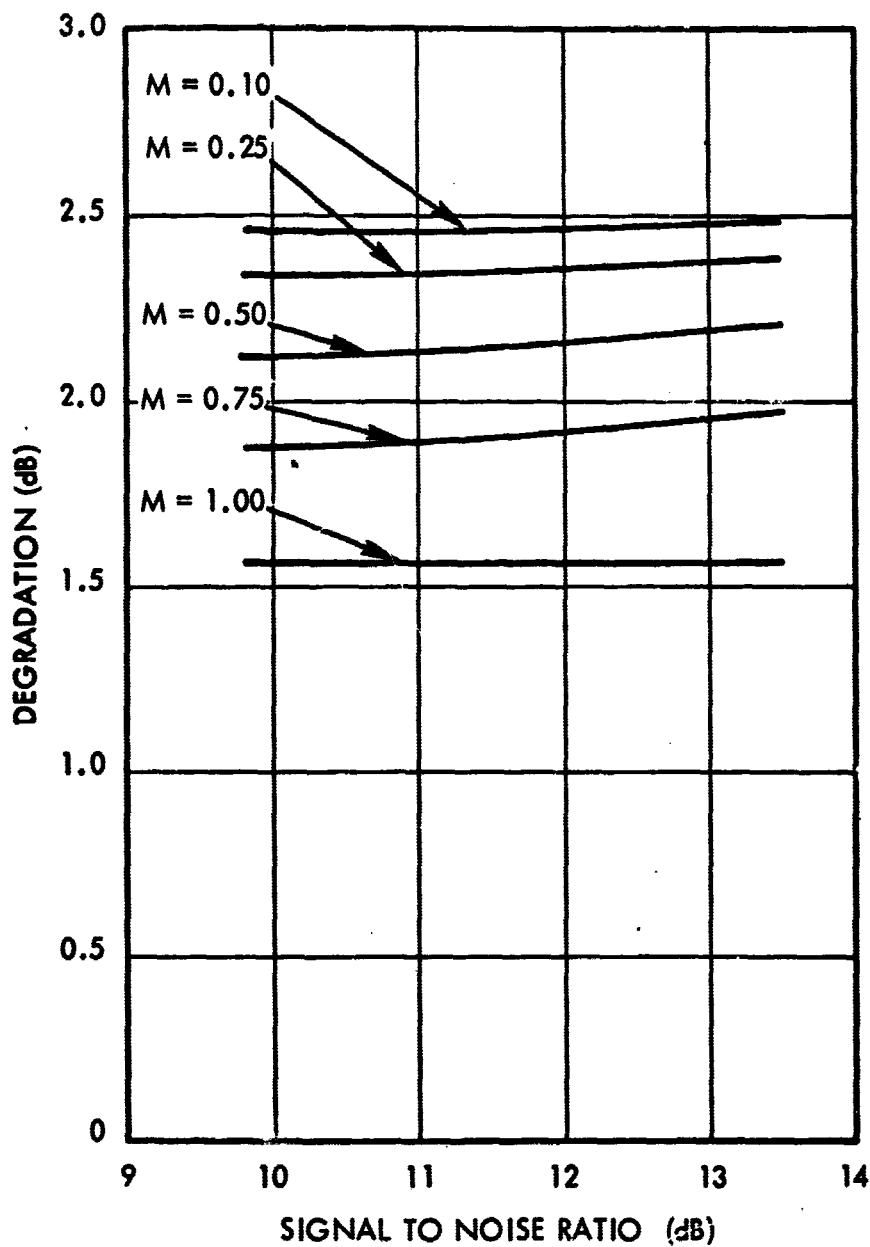


Figure 5.2.3 Performance Degradation Versus SNR MSFTP-2 Bit Synchronizer F&S Detector with Unfiltered Data

The degradation due to DC offsets is shown plotted on Figures 5.5.1 and 5.5.2.

5.4 PERFORMANCE DEGRADATION OF FILTER AND SAMPLE DETECTOR DUE TO TIMING ERROR

The F&S detector, ideally, is sampled at time T (see Figure 5.2.1) where the filter output voltage is very near its maximum. This point corresponds to maximum SNR for the F&S detector. Timing error (θ) displaces the sample point away from the maximum, resulting in a reduction in SNR at the F&S output and consequent increased error rate.

The filter output voltages (the "a" factors of Equation 5.2.3) as a function of timing error are read from the time response of Figure E6 and are as follows:

Timing Error $\frac{\theta}{T}$ (Fraction of a bit period)	$a_{1\theta}$	$a_{2\theta}$	$a_{3\theta}$	$a_{4\theta}$
0	1.11	1	1.11	1
0.10	1.08	1	1.08	1
0.20	1.02	1	1.02	1

The degradation with the above listed values of timing error for transition densities of from 10% to 100% was calculated using equation 5.2.3 and the computer routine of Appendix H. The results are plotted in Figures 5.4.1 through 5.4.4. These Figures show the loss with square wave data in the MSFTP-2 bit synchronizer F&S detector (referred to the I&D theoretical) plus the loss due to timing error.

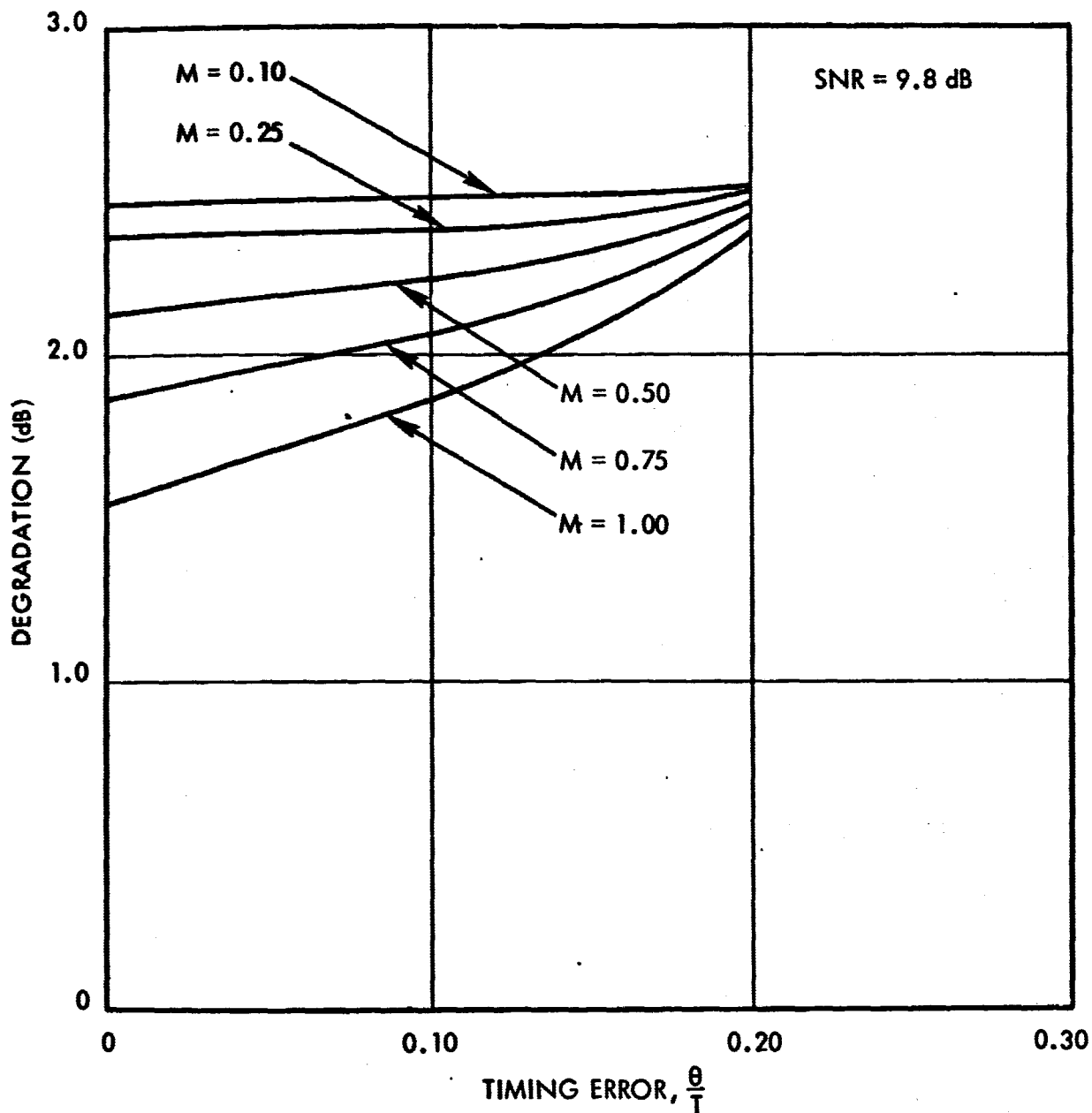


Figure 5.4.1 Performance Degradation Referred to the I&D Theoretical, Versus Timing Error, MSFTP-2 Filter and Sample Bit Detector

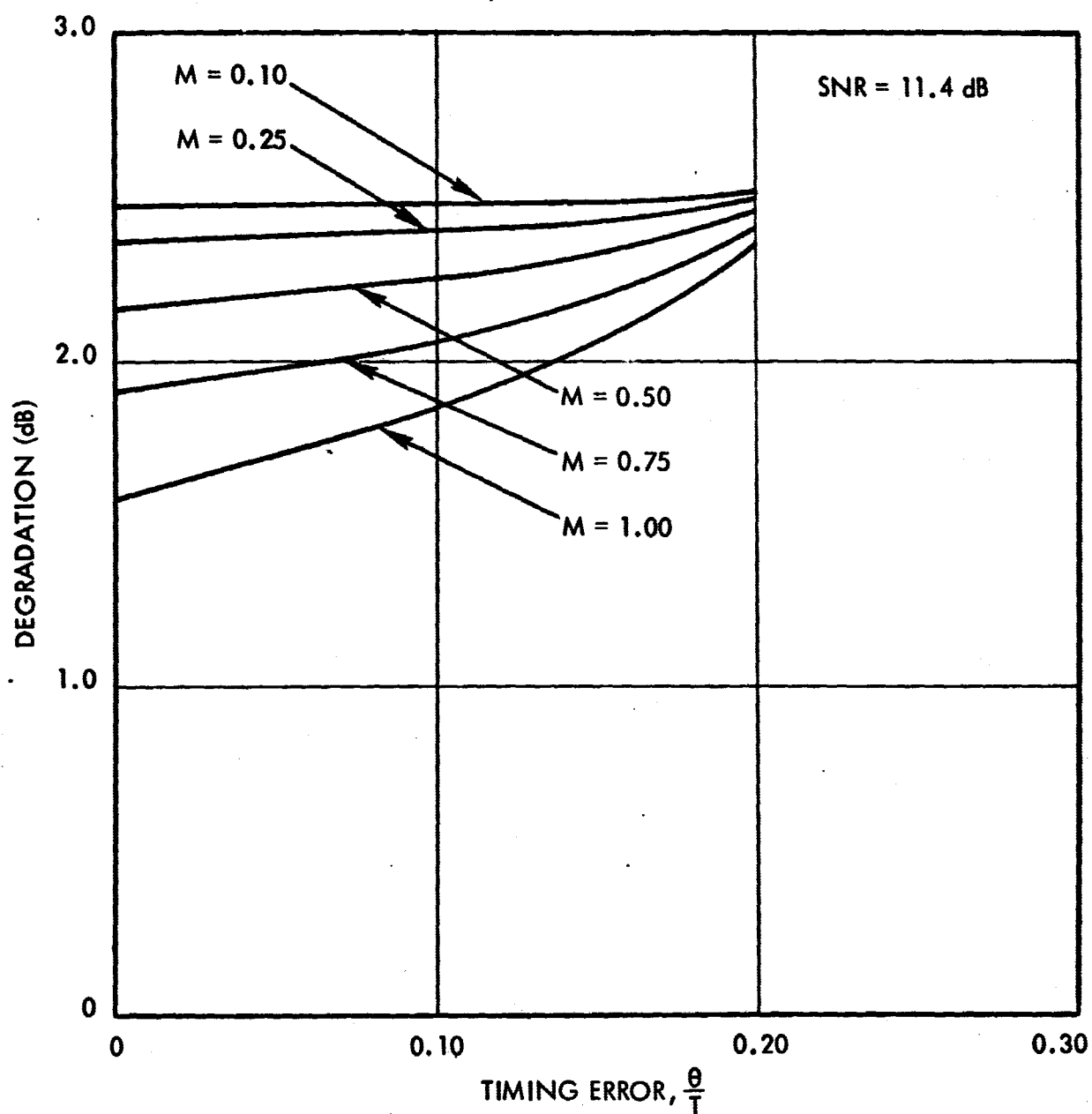


Figure 5.4.2 Performance Degradation Referred to the I&D Theoretical, Versus Timing Error, MSFTP-2 Filter and Sample Bit Detector

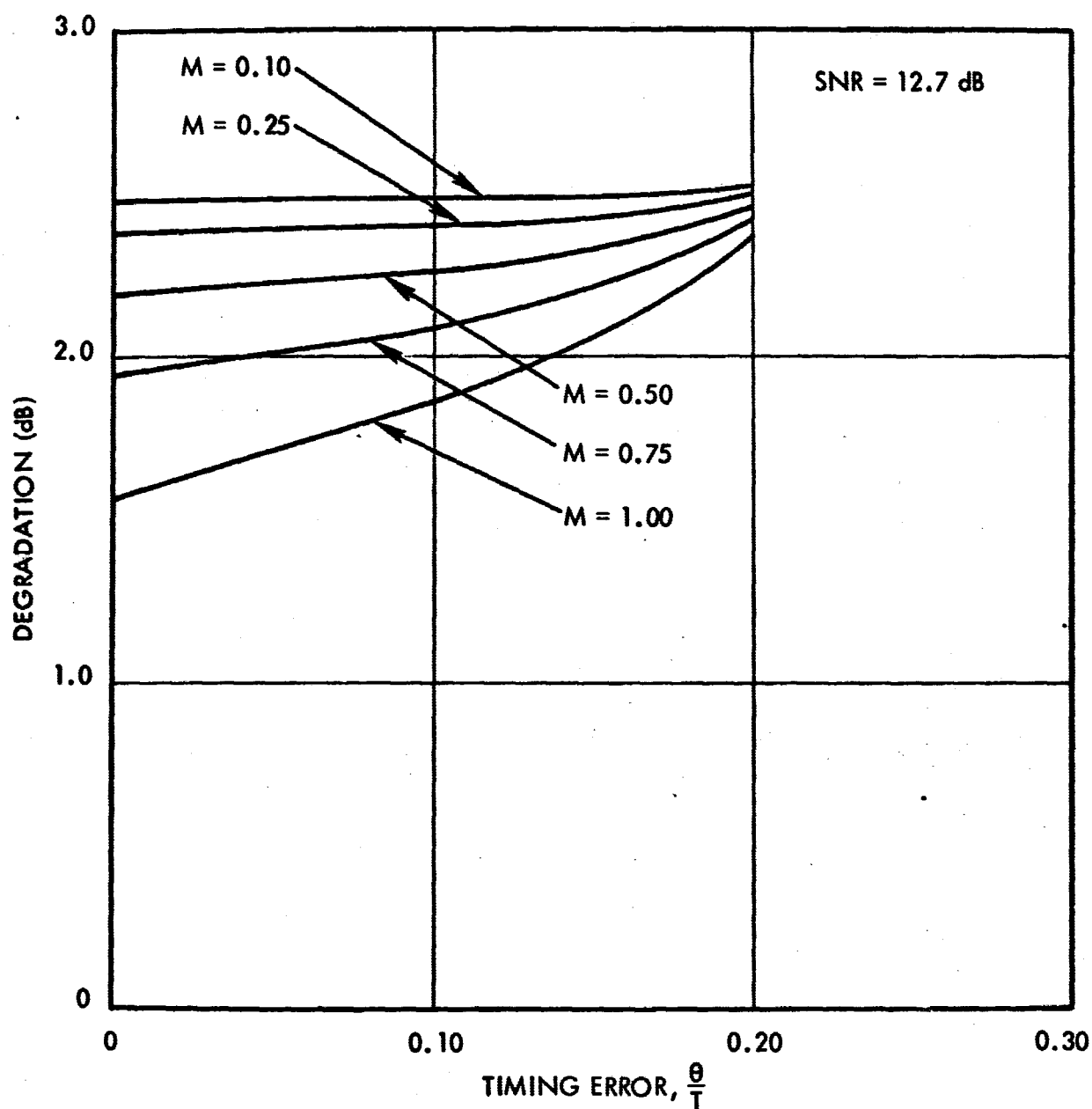


Figure 5.4.3 Performance Degradation Referred to the I&D Theoretical, Versus Timing Error, MSFTP-2 Filter and Sample Bit Detector

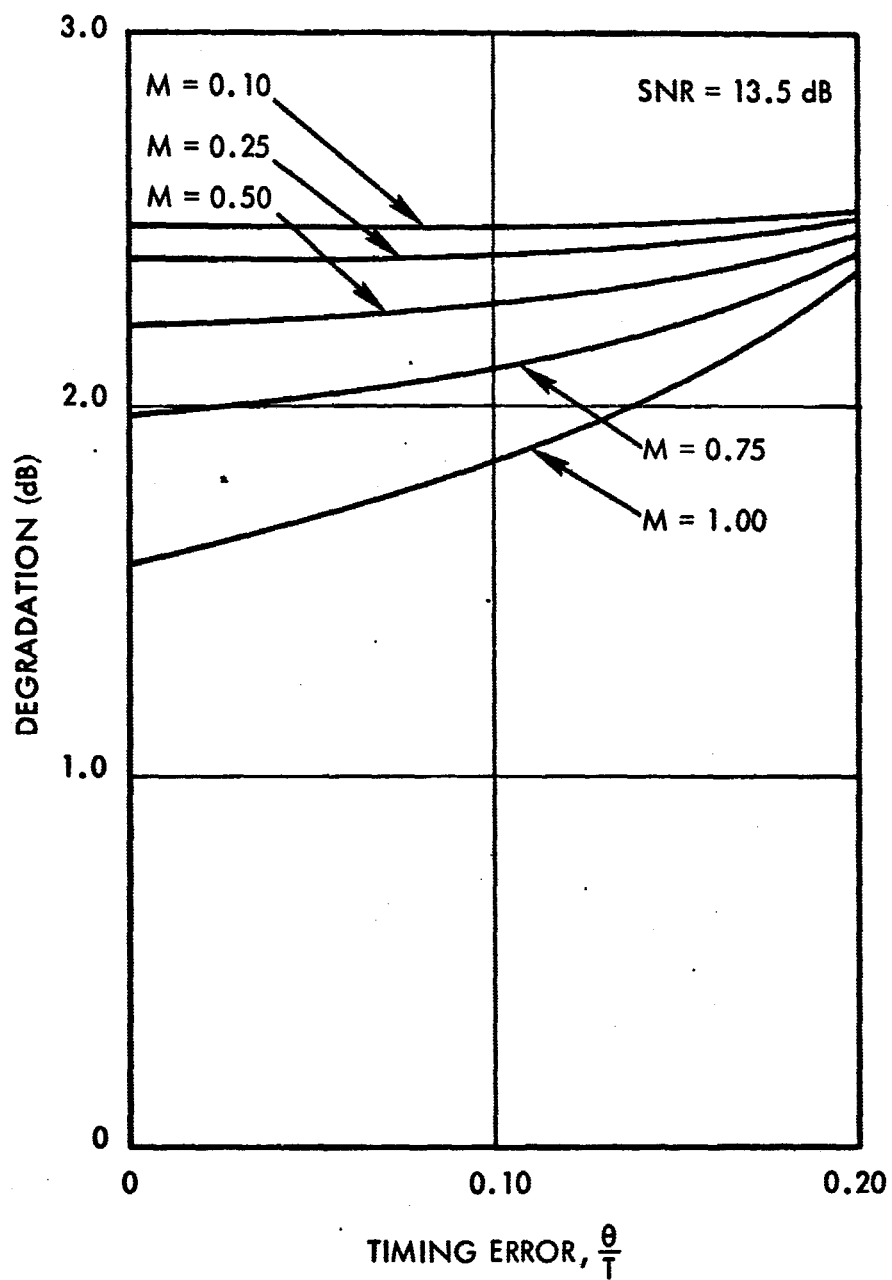


Figure 5.4.4 Performance Degradation Referred to the I&D Theoretical, Versus Timing Error, MSFTP-2 Filter and Sample Bit Detector

5.5 PREDICTED PERFORMANCE AND TEST RESULTS OF FILTER AND SAMPLE DETECTOR

Figures 5.5.1 and 5.5.2 show the predicted performance and measured data for transition densities of 100% and 50% respectively.

The curves of each figure are as follows:

- 1) Theoretical curve - I&D detector with unfiltered input data.
- 2) Predicted performance degradation (with unfiltered data) due to DC offsets - F&S detector.
- 3) F&S Performance with unfiltered data and timing error - This curve is drawn using Figures 5.4.1 through 5.4.4 and the estimated timing errors of Appendix D. The estimated timing error is 9% and 10% of a bit period for transition densities of 100% and 50% respectively.
- 4) Composite calculated losses - The sum of curves (2) and (3).
- 5) Nominal predicted performance - This curve is drawn by adding 0.5 db to curve (4) to allow for cumulation of degradations contributing less than 0.1 db degradation each.
- 6) Worst case predicted performance - This curve is drawn by adding 0.5 db to curve (5) to account for measurement errors.

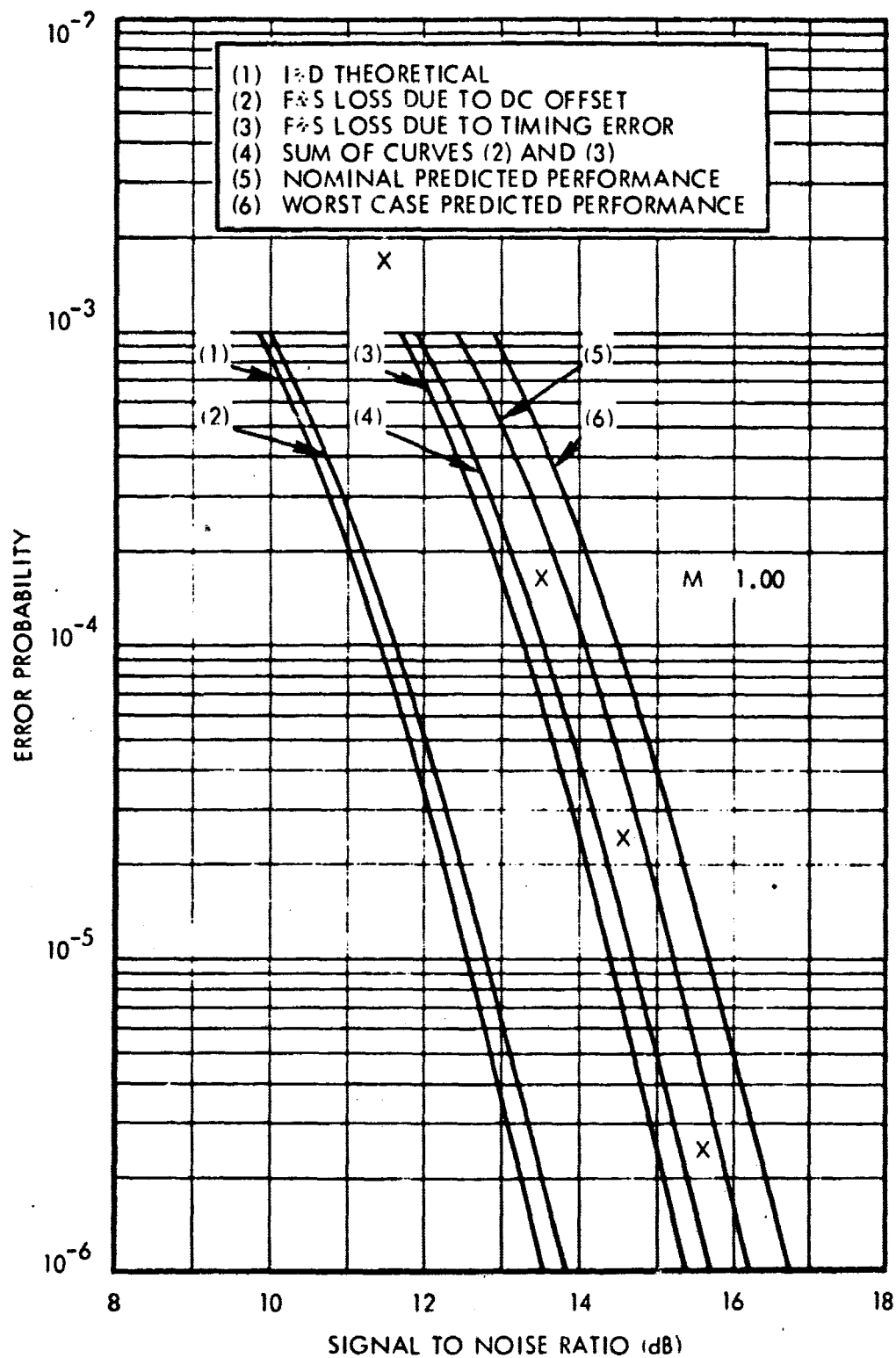


Figure 5.5.1 Measured Error Probability Versus SNR Compared With Predicted Performance; MSFTP-2 Filter and Sample Bit Detector with Unfiltered Input Data

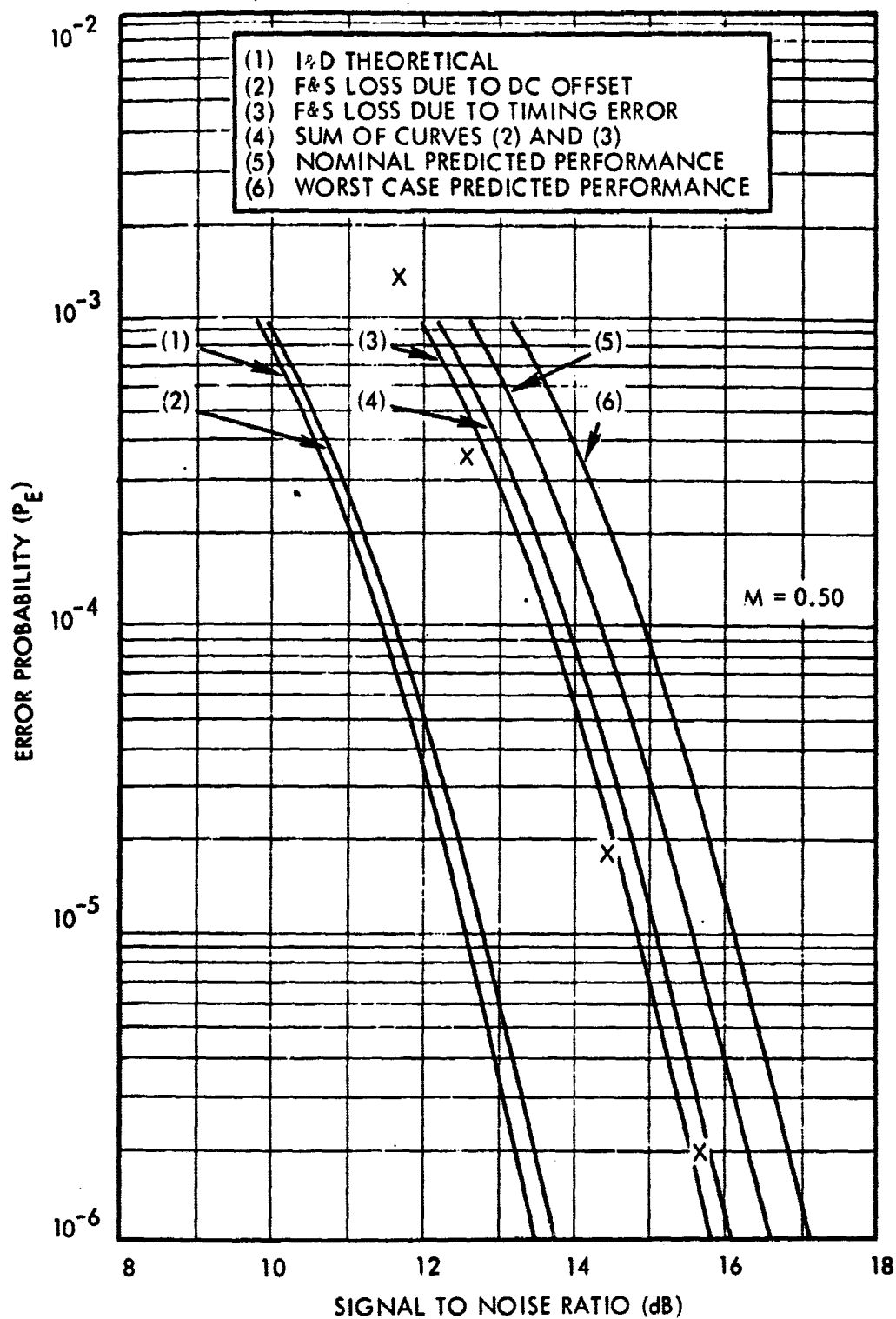


Figure 5.5.2 Measured Error Probability Versus SNR Compared With Predicted Performance; MSFTP-2 Filter and Sample Bit Detector with Unfiltered Input Data

APPENDIX A

BLOCK DIAGRAM AND DESCRIPTION OF OPERATION OF MSFTP-2 BIT SYNCHRONIZER

1.0 GENERAL

This appendix contains a block diagram and description of operation of the MSFTP-2 bit synchronizer. The material included was extracted from the MSFTP-2 technical information* supplied by NASA.

The overall block diagram of the MSFTP-2 bit synchronizer is shown in Figure A-1. The bit synchronizer contains five functional sections as follows:

- 1) Automatic Gain Control
- 2) Integrate and Dump Bit Detector
- 3) Filter and Sample Bit Detector
- 4) Baseline Correction Circuitry

Code Averaging Circuit

Baseline Correction Loop

- 5) Clock Extraction Circuitry
- Zero Crossing Detector
- Phase Lock Loop

2.0 AUTOMATIC GAIN CONTROL (AGC)

The AGC consists of the Gain Control Amplifier and AGC loop. The AGC loop consists of the 1) tunable low pass filter, 2) full wave rectifier, and 3) integrator. The filtered PCM data out of the low pass filter is rectified and applied to the integrator. The integrator reference voltage

*Dynatronics Inc. Technical Manual, Model 200 PCM Decommutator, MH-1042
Volumes 1, 2 and 4.

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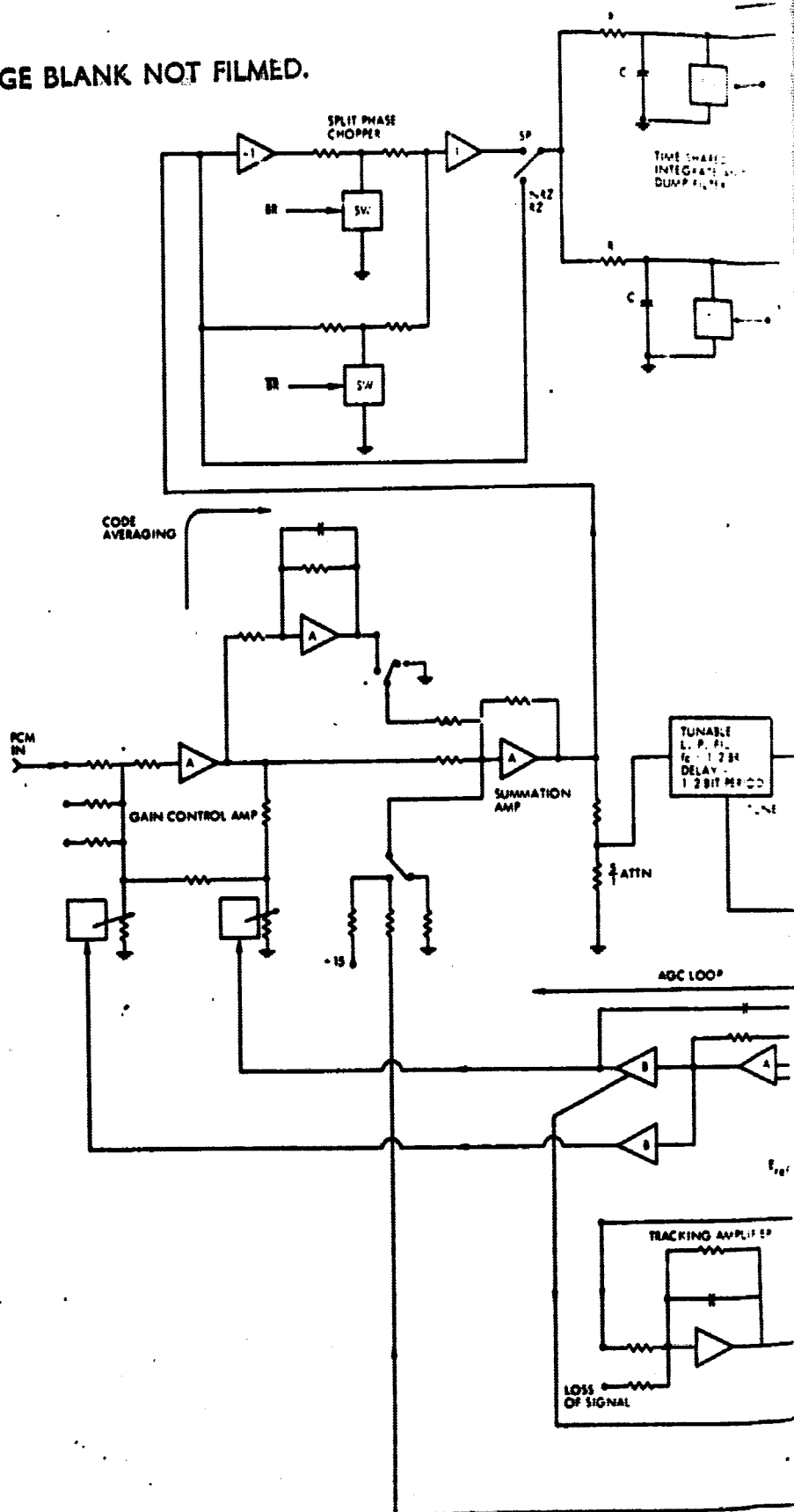
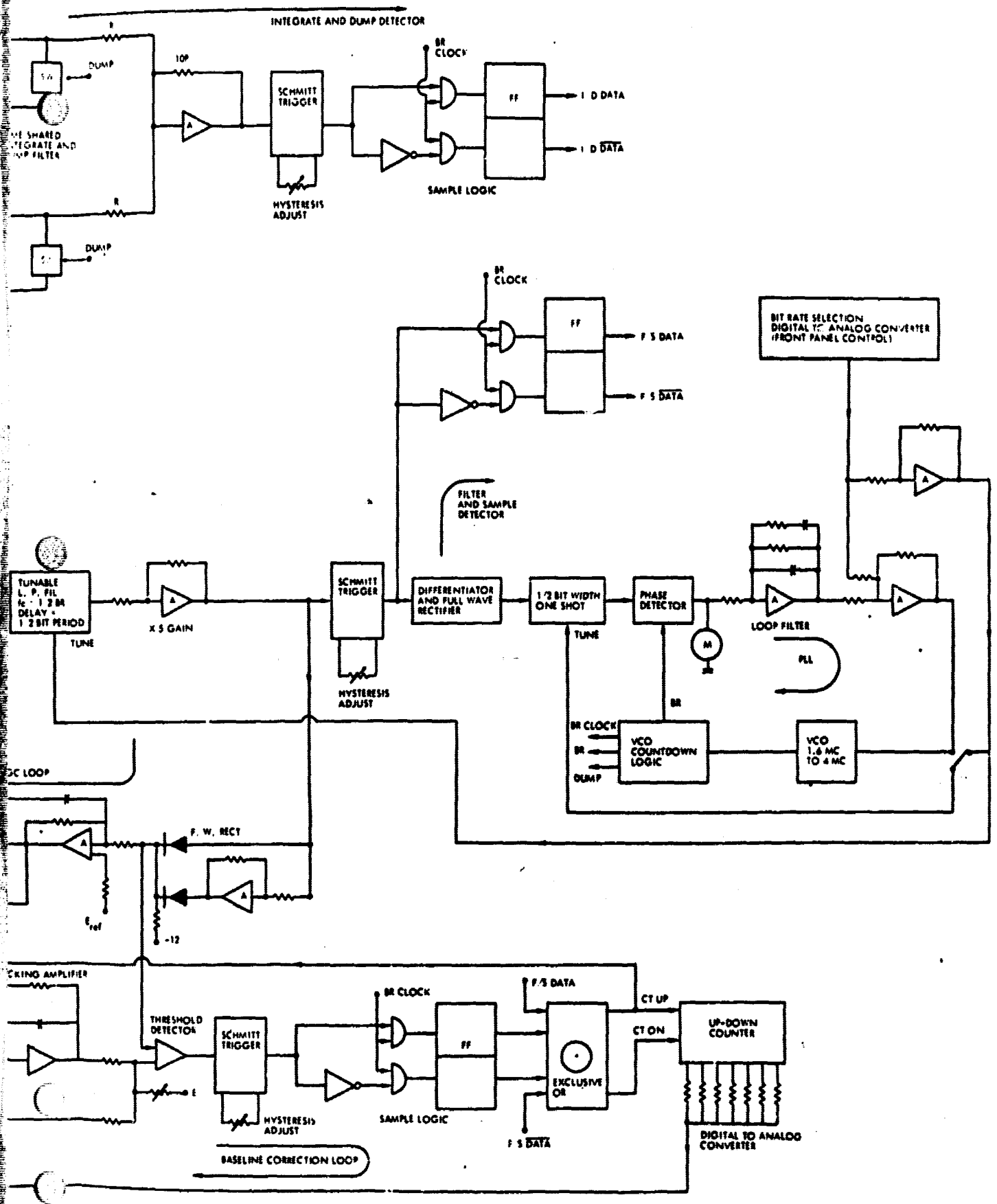


Figure A-1 Detailed Block Diagram of the MSFTP-2 Bit Synchronizer



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(E_{ref}) is preset to correspond to the desired signal level out of the AGC. The integrator output drives the gain control elements of the gain control amplifier. The gain control elements are photo sensitive resistors (Raysistors) with built-in voltage controlled light sources and form part of a resistor network around an operational amplifier.

The nominal AGC voltage output is specified as 2 volts peak with input voltages of from 0.5 to 30 volts peak to peak. The input voltage is broken into three ranges, depending on the gain control amplifier input attenuator, as follows:

<u>Position</u>	<u>Input Voltage Range</u>
1	0.5 to 7.0 volts peak to peak
2	1.0 to 15.0 volts peak to peak
3	2.0 to 30.0 volts peak to peak

3.0 INTEGRATE AND DUMP BIT DETECTOR

The I&D detector consists of, integrate and dump filter, schmitt trigger, and sampling logic. Also included is a split phase chopper which is used when operating with split phase code formats.

The split phase chopper switching inputs (BR) are square waves at the bit rate frequency. These signals are supplied from the clock extraction circuits such that when synchronism is obtained the split phase chopper demodulates the split phase coded data providing NRZ data at its output. The overall gain of the split phase chopper is approximately unity.

The integrate and dump filter consists of two time shared RC integrate and dump networks. Each network integrates and is dumped (the capacitor shorted and discharged) over alternate bit periods. One network is integrating while the other is being dumped. The outputs of the two networks are combined via an operational amplifier and applied to the schmitt trigger.

The schmitt trigger serves as a comparator to decide whether the operational amplifier output is positive or negative. The schmitt trigger output is sampled and stored, at the end of each bit period, via the sampling logic. The sampling flip flop output is the reconstructed PCM data from the I&D bit detector.

4.0 FILTER AND SAMPLE BIT DETECTOR

The filter and sample (F&S) bit detector consists of the tunable low pass filter, schmitt trigger, and sampling logic. The filtered PCM data out of the tunable low pass filter is applied to the schmitt trigger which serves as a comparator to decide the polarity of the filter output. The schmitt trigger output is sampled and stored via the sampling logic. The sampling flip flop output is the reconstructed PCM data from the F&S detector.

The tunable low pass filter has variable bandwidth, controlled from the front panel. Ideally, the filter cut off frequency is set to one-half the bit rate frequency and the filter phase delay is one-half the bit period. The sampling logic clock is coincident with zero crossings of the input data such that (including the filter delay) sampling occurs at the mid bit point of the filter output.

5.0 BASELINE CORRECTION CIRCUITRY

The baseline correction circuitry consists of the code averaging circuit and baseline correction loop of Figure A-1. The baseline correction circuitry is shown in simplified form in Figure A-2.

5.1 CODE AVERAGING

The code averaging (CA) circuit consists of an active low pass filter and summation amplifier. The input PCM data (and any DC offset on the data) is applied to the low pass filter and to one input of the summation amplifier. The low pass filter output is applied to a second input of the summation

amplifier. Since the active filter inverts the polarity of its input (180° phase reversal), the low pass filter output is subtracted from its input signal via the summation amplifier. Assuming that the input to the low pass filter is a periodic AC signal with a DC offset and the AC component is much higher than the filter cut off frequency, then the filter output will be the DC offset of the input.. The DC offset is then subtracted from the input in the summation amplifier yielding, at the summation amplifier output, the AC component.

The actual input to the code averaging circuit, which is PCM data, is not usually periodic and will contain a DC component depending on the relative number of transmitted ones and zeros. There will be no DC component only if ones and zeros are equally likely. The code averaging circuit cannot differentiate between DC offset and a DC component in the PCM data and will tend to eliminate both thereby corrupting the PCM waveform. The tendency of the code averaging circuit to eliminate DC components of the PCM data is compensated for by the baseline correction loop, as will be shown. Thus the code averaging circuit makes a "coarse" correction for DC offset and the baseline correction loop makes the "fine" correction.

The transfer function of the code averaging circuit is given in Appendix G of this report.

5.2 BASELINE CORRECTION LOOP

Figures A-2 and A-3 show a simplified block diagram and pertinent waveforms, respectively, for the baseline correction loop. Figure A-3 shows waveforms out of the tunable low pass filter and out of the full wave rectifier for conditions of no DC offset and positive and negative DC offset. For convenience the waveforms are drawn for an alternate 1, 0 data pattern. When no DC offset is present in the input, the peaks of the rectifier output are of equal amplitude. When a positive DC offset is present, the peaks which correspond to "ones" are increased and those corresponding to "zeros" decreased. With negative DC offset the peaks which correspond to "zeros" are increased and those corresponding to "ones" are decreased.

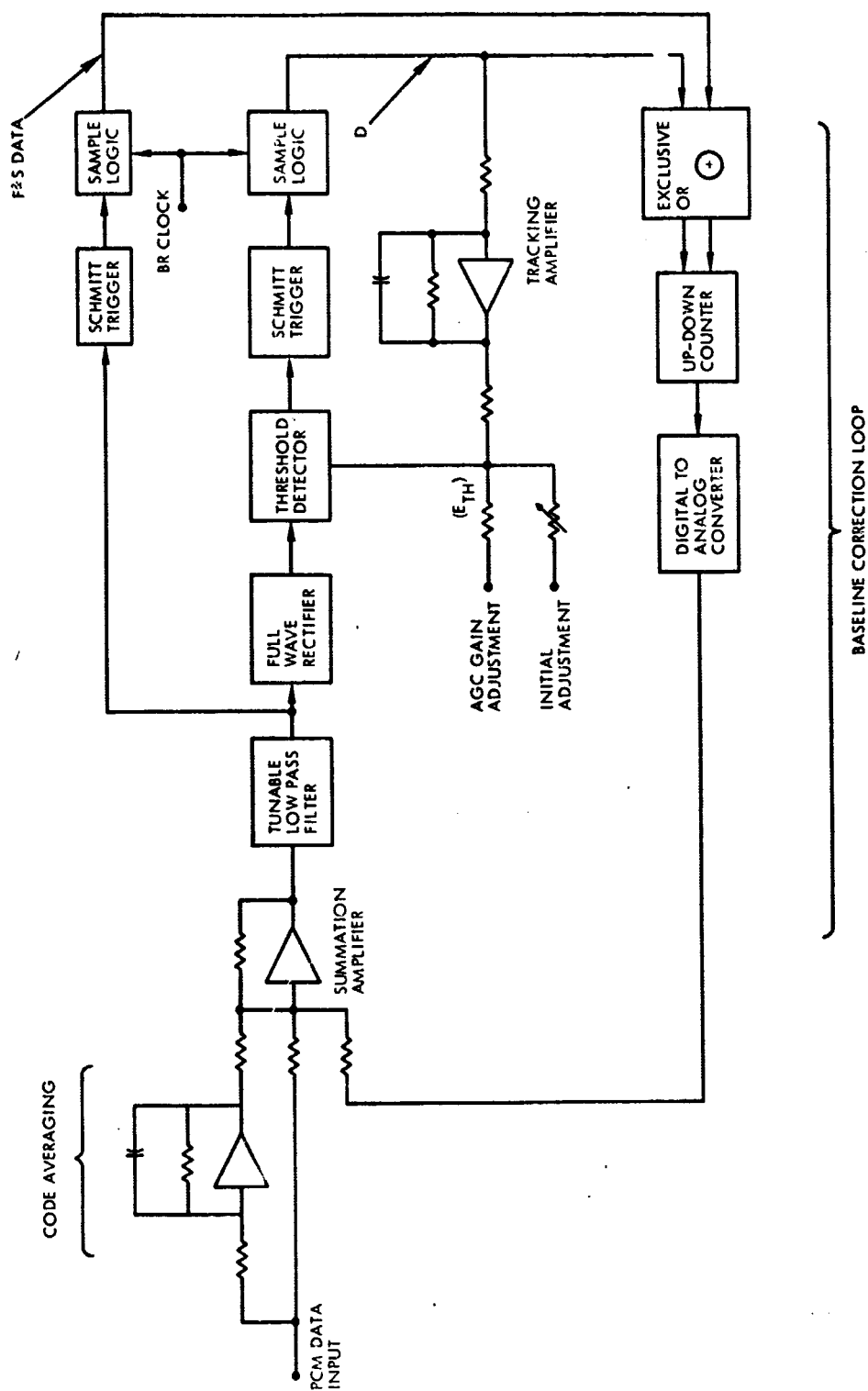


Figure A-2 Block Diagram of Baseline Correction Circuitry

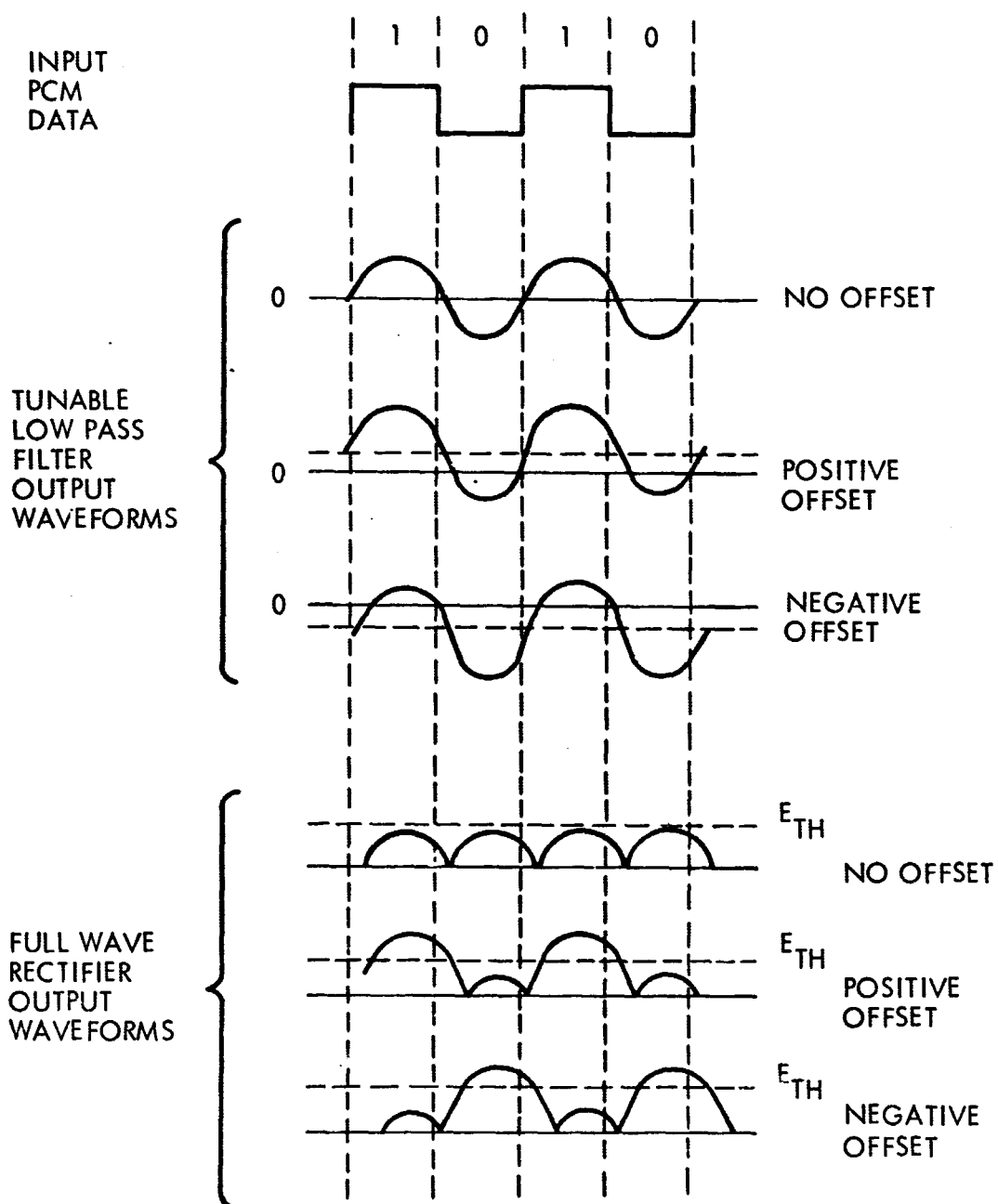


Figure A-3 Baseline Correction Loop Waveforms

The rectifier output is applied to a threshold detector whose reference voltage (E_{TH}) is ideally set equal to the amplitude of the rectifier output peaks when no DC offset is present. When positive DC offset is present the threshold is exceeded when "ones" occur in the data and when negative DC offset is present the threshold is exceeded in "zeros" are present in the data. The threshold detector output is sampled and stored in a flip flop. The flip flop output (D) is true or false depending on whether or not the threshold was exceeded. Simultaneously, the filter and sample bit detector determines if the transmitted bit was a "one" or "zero" (F&S Data). The two outputs (D) and (F&S Data) are combined in an exclusive OR gate and a decision made as to whether the DC offset is positive or negative. The exclusive OR logic is as follows:

$$(F\&S\ Data)(D) + (\overline{F\&S\ Data})(\overline{D}) = \text{positive offset}$$

$$(F\&S\ Data)(\overline{D}) + (\overline{F\&S\ Data})(D) = \text{negative offset}$$

The exclusive OR gate drives an up-down counter and digital to analog converter (DAC). The DAC output is applied to an input of the summation amplifier. If positive offset is detected via the exclusive OR, the up-down counter is incremented down producing a negative voltage out of the DAC which subtracts the positive offset out in the summation amplifier.

Operation of the baseline correction loop depends on the threshold voltage (E_{TH}) being set very nearly equal to the rectifier output peaks when no DC or AC offset is present. The peak output of the rectifier is subject to change with change in input signal level or AGC gain. The threshold (E_{TH}) must "track" any change in the threshold and maintain its level equal to the rectifier output peaks. To maintain this level, three adjustments of E_{TH} are provided as shown in Figure A-2. They are:

- 1) AGC gain adjustment - This adjustment is feedback from the AGC loop which changes E_{TH} in accordance with changes in AGC gain.
- 2) Initial adjustment - This is an adjustment potentiometer which is set manually at calibration.

- 3) Tracking amplifier - The tracking amplifier is an (impure) integrator the input of which is the switched logic level of the threshold detector sampling logic. The output of the tracking amplifier adjusts E_{TH} in accordance with the duty cycle of the logic level at its input. The tracking amplifier will tend to adjust E_{TH} to a value so the duty cycle of its input is 50%. This duty cycle corresponds to E_{TH} equal to the rectifier output peaks.

6.0 CLOCK EXTRACTION CIRCUITRY

6.1 ZERO CROSSING DETECTOR

The zero crossing detector of Figure A-1 consists of the tunable low pass filter, schmitt trigger, differentiator and full wave rectifier, and one-half bit width one shot.

The filtered PCM data out of the low pass filter is "squared up" in the schmitt trigger producing at its output a square wave signal with transitions coincident with zero crossings of the low pass filter output. The differentiator and full wave rectifier produces unipolar pulses coincident with the transitions of the schmitt trigger output. The pulses fire the one-half bit width one shot which produces pulses of width equal to one-half the bit period the leading edges of which are coincident with zero crossings of the low pass filter output.

6.2 PHASE LOCK LOOP

The phase lock loop (PLL) consists of the phase detector, loop filter, VCO drive amplifier, VCO, and digital divider. It is a conventional phase lock loop which locks onto the bit rate frequency component of the one shot output. The timing signals of the bit synchronizer are supplied from the PLL.

APPENDIX B

DC ANALYSIS AND ERROR BUDGET MSFTP-2 BIT SYNCHRONIZER

1.0 SUMMARY AND CONCLUSIONS

The technical information, supplied by NASA, on the MSFTP-2 bit synchronizer has been utilized to calculate and estimate the worst case expected DC offset errors in the bit synchronizer. The worst case DC offset error resulting from this analysis is used in Section 4.0 to calculate the performance degradation of the MSFTP-2 bit synchronizer due to DC offset errors.

The following worst case calculated DC offsets resulted from this analysis:

8% of peak signal amplitude for I&D detector

6% of peak signal amplitude for F&S detector

2.0 INTRODUCTION

Twelve (12) major sources of DC offset error have been identified, are discussed in Section 3.0 of this Appendix, and are summarized in Table B-1. The normalized error contribution for each error source has been calculated and is tabulated in Table B-1 opposite the error source. The first entry in Table B-1 shows the baseline loop quantization error which is caused by the digital-to-analog converter in the baseline correction loop. This error is constant and is ± 2.35 percent of the nominal peak signal amplitude or is a normalized DC error of 0.0235. The second entry in the table shows the DC error caused by tuning error of the tunable low pass filter. The error contribution is ± 0.21 percent of nominal peak signal amplitude per percent tuning error. The filter is nominally tuned to a frequency of one-half the bit rate. For each one percent error between filter tuning and input bit rate, a normalized DC error of ± 0.0021 is generated. The eighth entry in the table shows the error due to switch offset in the integrate and dump filter. The normalized DC error is ± 0.005 for each millivolt of switch offset.

Tables B-2 and B-3 show the combined DC error contributions for different magnitudes of error. In Table B-2 the contributions are calculated assuming detuning and adjustment errors of 5%, and circuit offsets in each switch and amplifier of 5 mv. In Table B-3 the detuning and adjustment errors are assumed to be 10% and the switch and amplifier offsets 10 mv. The error contributions are listed for NRZ and Split Phase data for the integrate and dump detector and for NRZ data with the filter and sample detector. When using Split Phase data the error contributions due to the baseline loop and the low pass filter do not apply. This is because these DC errors are chopped at the bit rate in the split phase chopper and integrated to zero in the integrate and dump filter. When using the filter and sample detector the contributions due to the split phase chopper, integrate and dump filter, and low pass filter do not apply. Any offset in the low pass filter is compensated by the baseline loop as seen by the filter and sample detector.

Tables B-2 and B-3 show both the worst case total offset and the root sum squared offset. Because of the number of contributions (which may assume either polarity) the RSS total is most realistic.

The RSS errors of Table B-3 are taken as worst case for the MSFN bit synchronizer. For the I&D detector, the calculated errors are 8.3% and 5.13% for NRZ and split phase data respectively, therefore, worst case value of 8% is taken for the I&D detector. For the F&S detector (calculated 5.97%) a worst case value of 6% is taken.

Not shown in Tables B-2 and B-3, is the schmitt trigger hysteresis error of Table B-1. The hysteresis error, which depends on transition density, cannot be added to the other contributions and must be calculated separately. The calculated performance degradation due to schmitt trigger hysteresis error is shown in Figure B-10 and is seen to be approximately 0.1 db with hysteresis of 100 mv. The hysteresis error increases rapidly for hysteresis voltage greater than 100 mv. The hysteresis is not expected to be as great as 100 mv, however, and is neglected in the performance predictions of Section 4.0.

TABLE B-1

DC ERROR SOURCES AND CONTRIBUTIONS

Error Sources		Normalized Error Contribution	
Baseline Loop Quantization Error (ΔQ)		$\pm 2.35\%$ of Peak Signal Amplitude	
Baseline Loop Threshold Error (ΔT)	Fil Detuning Error	± 0.21	$\frac{\% \text{ Peak Signal Amplitude}}{\% \text{ Detuning}}$
	Initial Adjustment Error	± 0.36	$\frac{\% \text{ P.S.A.}}{\% \text{ Adjustment Error}}$
	AGC Adjustment Error	± 0.36	$\frac{\% \text{ P.S.A.}}{\% \text{ Adjustment Error}}$
Split Phase Chopper Circuit Error (ΔC)	Switch Offset	± 0.104	$\frac{\% \text{ P.S.A.}}{\text{MV Offset}}$
	Input Amp Offset	± 0.025	$\frac{\% \text{ P.S.A.}}{\text{MV}}$
	Output Amp Offset	± 0.05	$\frac{\% \text{ P.S.A.}}{\text{MV}}$
I&D Filter Circuit Error (ΔI)	Switch Offset	± 0.5	$\frac{\% \text{ P.S.A.}}{\text{MV}}$
	Output Amp Offset	± 0.05	$\frac{\% \text{ P.S.A.}}{\text{MV}}$
Tunable Low Pass Filter Offset Error (ΔF)	Active Fil Offset	± 0.25	$\frac{\% \text{ P.S.A.}}{\text{MV}}$
	Output Amp Offset	± 0.05	$\frac{\% \text{ P.S.A.}}{\text{MV}}$
Schmitt Trigger Hysteresis Error (ΔST)		± 0.05	$\frac{\% \text{ P.S.A.}}{\text{MV Offset}}$

TABLE B-2
DC ERROR SOURCES, ERROR MAGNITUDES, AND RESULTANT ERROR CONTRIBUTIONS

Error Source	Estimated Error Magnitude	Resultant Error Contribution		
		I&D Detector	Split Phase	F&S Detector
ΔQ	Constant	NRZ		NRZ
		+0.024		+0.024
Fil Detuning	5%	+0.010		+0.010
Initial Adj.	5%	+0.018		+0.018
AGC Adj.	5%	+0.018		+0.018
Switch Offset	5 millivolts		+0.005	
Input Amp	5 millivolts		+0.001	
Output Amp	5 millivolts		+0.002	
Switch Offset	5 millivolts	+0.025	+0.025	
Output Amp	5 millivolts	+0.002	+0.002	
Active Fil	5 millivolts	+0.012		
Output Amp	5 millivolts	+0.002		
Worst Case Total		0.111	0.035	0.070
Root Sum Squared Total (RSS)		0.046	0.0256	0.0364

TABLE B-3
DC ERROR SOURCES, ERROR MAGNITUDES, AND RESULTANT ERROR CONTRIBUTIONS

Error Source	Estimated Error Magnitude	Resultant Error Contributions			
		I&D Detector		F&S Detector	
		NRZ	Split Phase	NRZ	NRZ
ΔQ	Constant	± 0.024		± 0.024	
Fil Detuning	10%	± 0.020		± 0.020	
ΔT Initial Adj.	10%	± 0.036		± 0.036	
AGC Adj.	10%	± 0.036		± 0.036	
Switch Offset	10 millivolts		± 0.010		
ΔC Input Amp	10 millivolts		± 0.002		
Output Amp	10 millivolts		± 0.004		
Switch Offset	10 millivolts	± 0.050	± 0.050		
ΔI Output Amp	10 millivolts	± 0.004	± 0.004		
Active Fil	10 millivolts	± 0.024			
ΔF Output Amp	10 millivolts	± 0.004			
Worst Case Total		0.198	0.070		0.116
Root Sum Squared Total (RSS)		0.083	0.0513		0.0597

3.0 DC ANALYSIS

The portion of the bit synchronizer which contributes DC offset errors to the integrate and dump (I&D) and filter and sample (F&S) detectors is shown in block diagram form in Figure B-1.

In general, DC offset which affects the performance of the I&D detector consists of any offset at the output of the summation amplifier plus circuit offsets in the split phase chopper, I&D filter, and schmitt trigger.

DC offset which affects the F&S detector consists of any offset at the output of the low pass filter plus any offset in the schmitt trigger.

The baseline correction loop corrects for DC offset by sensing the offset at the output of the tunable low pass filter and subtracting it out at the summation amplifier input via the digital to analog converter and up-down counter. The baseline loop senses the "total" DC offset at the summation amplifier output. This includes any offset on the PCM data input, plus the circuit offsets in 1) the gain control amplifier, 2) code averaging amplifier, and 3) summation amplifier. Therefore the baseline loop corrects for circuit errors in the three above mentioned circuits so these can be neglected. The baseline loop also senses any offset in the low pass filter and adds this offset to the output of the summation amplifier. The DC offset at the summation amplifier therefore depends on the accuracy of the baseline loop and the offset in the low pass filter so the block diagram can be simplified to that shown in Figure B-2.

3.1 DC ERROR CONTRIBUTIONS OF THE BASELINE CORRECTION LOOP

Examination of the baseline correction loop yields two major DC error contributions as follows:

1. Quantization error of the Digital to Analog Converter
2. Error in the Threshold Voltage of the Threshold Detector.

These errors are discussed below.

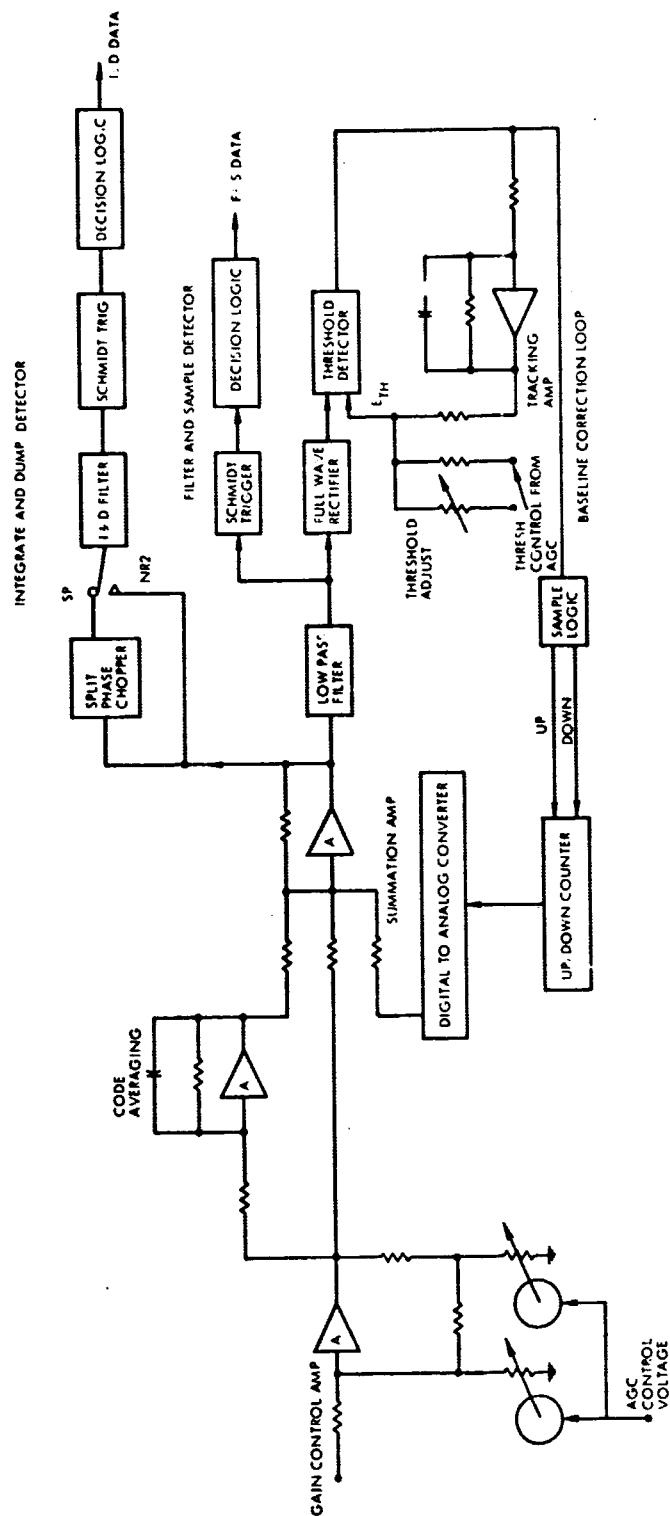


Figure B-1 Portion of MSFTP-2 Bit Synchronizer which Contributes to DC Offset Errors

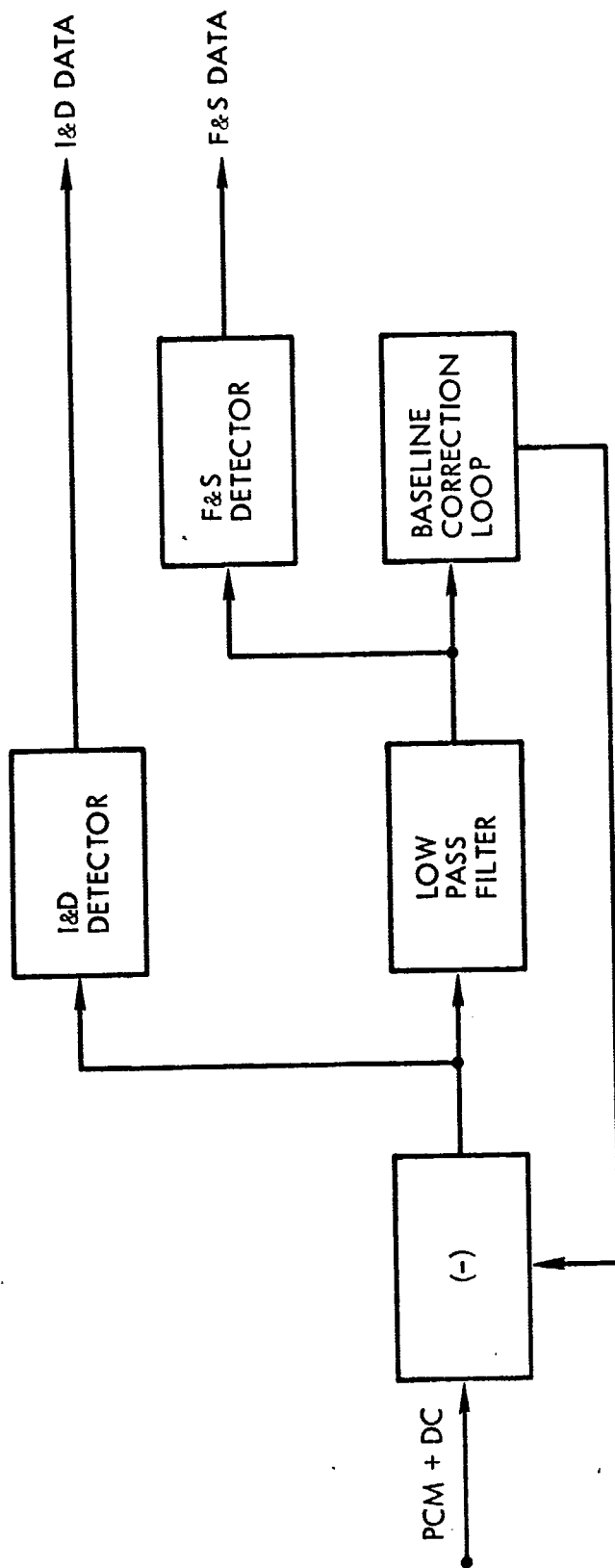


Figure B-2 Simplified Block Diagram of Portion of MSFTP-2 Bit Synchronizer which Contributes to DC Offset Errors

3.1.1 Quantization Error in Baseline Loop

The analog correction voltage at the summation amplifier input is generated via the up/down counter and digital to analog converter. The correction voltage is shown pictorially in Figure B-3. The voltage out of the D/A is $\pm V$ depending on the count in the up/down counter. The D/A is capable of subtracting DC errors of magnitude equal to approximately 6V. The up/down counter is seven (7) bit or 128 position, therefore, the D/A output changes by 12 volts in 128 counts of the up/down counter. The nominal peak signal voltage out of the summation amp is 2V peak.

The peak quantization error as a percentage of peak signal voltage is:

$$\Delta Q_{PK} = \left(\frac{12}{128} \right) \left(\frac{1}{2} \right) = 4.7\% \text{ of peak signal.}$$

The average quantization error is:

$$\Delta Q = \frac{1}{2} (4.7\%) = 2.35\% \text{ of peak signal.}$$

3.1.2 Threshold Error in Baseline Loop

Accurate correction of DC baseline requires the reference threshold (E_{TH}) of the threshold detector to be exactly equal to the peak signal voltage at the output of the low pass filter. Any difference between E_{TH} and the peak signal voltage will cause a DC offset at the output of the summation amplifier equal to the voltage difference. The peak signal voltage at the output of the low pass filter will be constant except for variation in AGC gain and variation in the tuning of the low pass filter. Detuning of the low pass filter causes its attenuation to change.

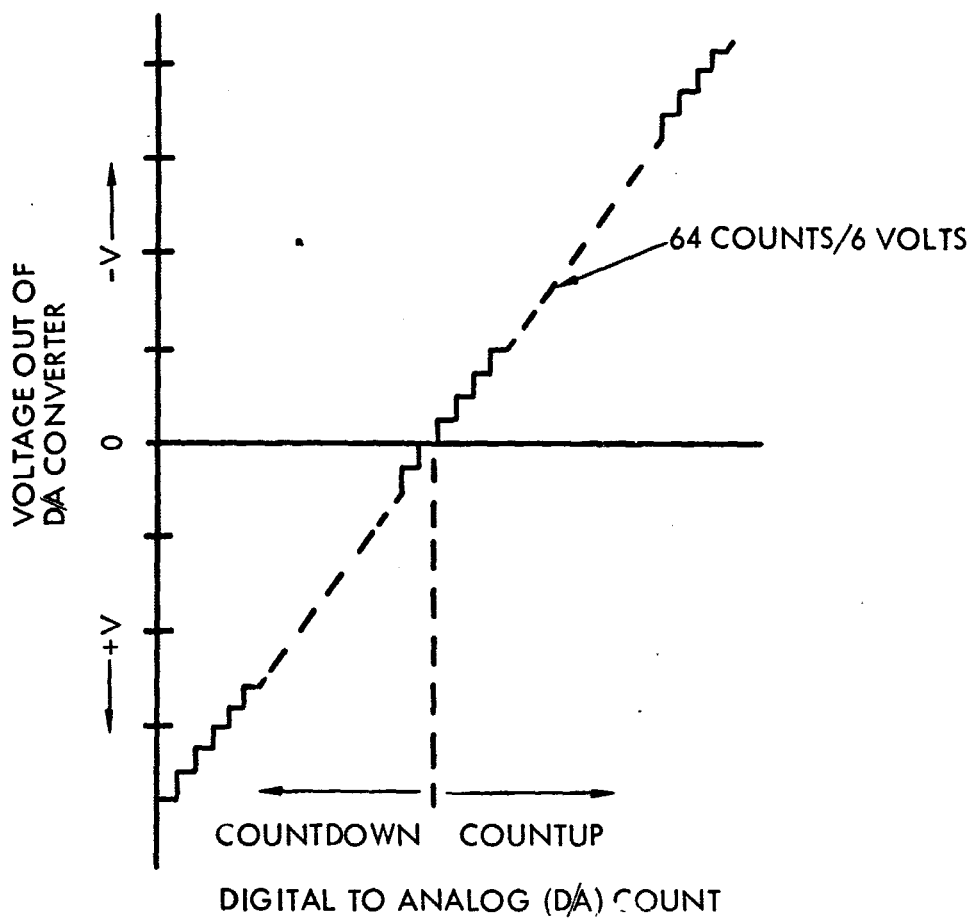


Figure B-3 Digital-to-Analog Converter
Input-Output Characteristics

Three adjustments of E_{TH} are provided to hold it at the correct value as follows:

1. A feedback is provided from the AGC detector to increase or decrease E_{TH} as the AGC gain increases or decreases.
2. An adjustment potentiometer is provided to manually set the threshold initially or on a periodic basis.
3. A "tracking amplifier" is provided to automatically set the threshold. The tracking amplifier senses the duty cycle at the output of the threshold detector and tends to set E_{TH} to a value corresponding to a 50 percent duty cycle. The correct value of E_{TH} will yield a 50% duty cycle at the output of the threshold detector. The tracking amplifier is an imperfect integrator so the error in E_{TH} will be the initial error due to uncorrected AGC gain variations, filter detuning, and error in initial manual adjustment divided by the DC gain of the tracking amplifier. If a pure integral tracking amplifier were used (DC gain very large) the error would tend to be zero.

$$\Delta_T = \text{THRESHOLD ERROR} = \frac{\Delta_i + \Delta_D + \Delta_G}{A_T}$$

Δ_i = initial adjustment error

Δ_D = filter detuning error

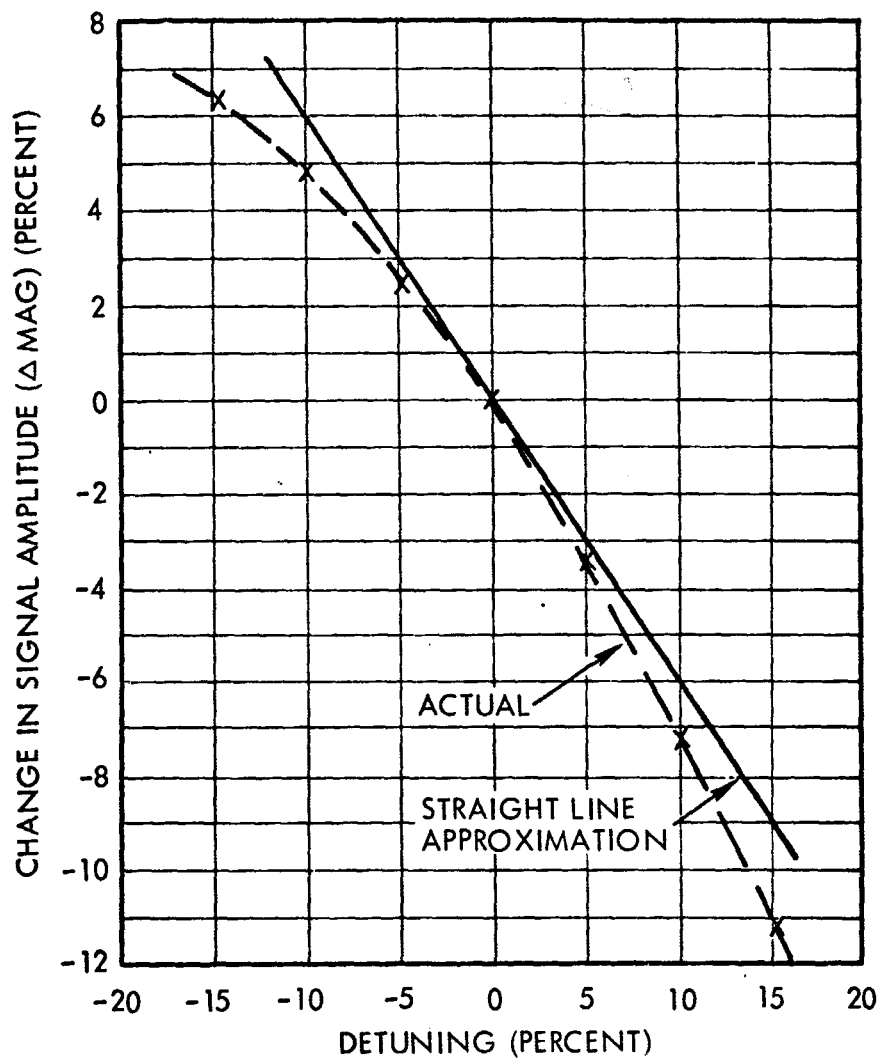
Δ_G = AGC gain error

A_T = tracking amplifier DC gain

$$A_T = \frac{5.6 \text{ MEG}}{2 \text{ MEG}} = 2.8$$

Filter Detuning Error

The filter detuning error is the change in filter gain due to tuning error of the tunable low pass filter. The filter is nominally tuned to a frequency of one-half the bit rate and the filter gain is one (1). Figure B-4 shows the percentage change in signal amplitude out of the filter versus percentage detuning from nominal. The magnitude expression for Figure B-4 is given in Appendix E, Analysis of Tunable Low Pass Filter.



$$\text{MAG} = \frac{1}{\sqrt{(1-\alpha^2)^2 + [1.2\alpha - 0.2\alpha^3]^2}}$$

$$\alpha = \frac{f}{f_0} \quad f_0 = \text{NOMINAL FREQUENCY} = \frac{1}{2} \text{BIT RATE}$$

Figure B-4 Attenuation Versus Detuning Tunable Low Pass Filter

A straight line approximation of the actual curve, also shown in the figure, shows the detuning error to be:

$$\Delta_D = \frac{6 \text{ percent of sig ampl}}{10 \text{ percent detuning}} = 0.6 \frac{\% \text{ sig ampl}}{\% \text{ detuning}}.$$

The threshold error contributed by Δ_D is:

$$\frac{\Delta_D}{A_T} = \frac{0.6}{2.8} = 0.21 \frac{\% \text{ of Signal Ampl}}{\% \text{ of Detuning}}$$

for 5% detuning error

$$\Delta_D = (0.21) (5) = 1.05\% \text{ of Signal Ampl}$$

for 10% detuning error

$$\Delta_D = 2.1\% \text{ of Signal Amplitude}$$

Initial Adjustment Error and AGC Gain Error

The initial adjustment error and AGC gain error depend on how well the operator sets the potentiometer and on the accuracy of the resistors.

$$\frac{\Delta_i}{A_T} = \frac{1\%}{2.8} = 0.357 \frac{\% \text{ of Signal Amplitude}}{\% \text{ of Sig Ampl. Adjust. Error}}$$

$$\frac{\Delta_G}{A_T} = \frac{1\%}{2.8} = 0.357 \frac{\% \text{ of Signal Amplitude}}{\% \text{ of Sig Ampl. Adjust. Error}}$$

for 5% error in adjustment

$$\frac{\Delta_i}{A_T} = \frac{\Delta_G}{A_T} = \frac{5\%}{2.8} = 1.79\% \text{ of Signal Amplitude}$$

for 10% error in adjustment

$$\frac{\Delta_i}{A_T} = \frac{\Delta_G}{A_T} = \frac{10\%}{2.8} = 3.58\% \text{ of Signal Amplitude}$$

3.2 DC ERROR CONTRIBUTIONS OF THE I&D DETECTOR SPLIT PHASE CHOPPER CIRCUIT ERROR

The split phase chopper schematic is shown in Figure B-5a. Figure B-5b is an approximate equivalent circuit of the split phase chopper switch. The switch consists of parallel NPN and PNP common emitter switches. When the switch is OFF both transistors are back biased by approximately 5.5V, keeping the switch off unless the voltage at the collectors exceed ± 5.5 volts. When the switch is ON both transistors are turned on.

Figure B-6 shows the split phase chopper with the switches replaced by ideal switches each with a series offset. Switch S1 has an offset of $\Delta 1$, switch S2 has an offset $\Delta 2$. Amplifier A1 has a gain of -1 and an equivalent offset $\Delta 3$. Amplifier A2 has an equivalent offset $\Delta 4$. The input signal has an offset of ΔS . Switches S1 and S2 close on alternate half bit intervals, S1 is closed the first half of each bit and S2 is closed the second half of each bit. Since the chopper is followed by an integrate and dump filter, any DC offset in the last half bit period which is equal to a DC offset in the first half bit period, but opposite in polarity, will integrate to zero.

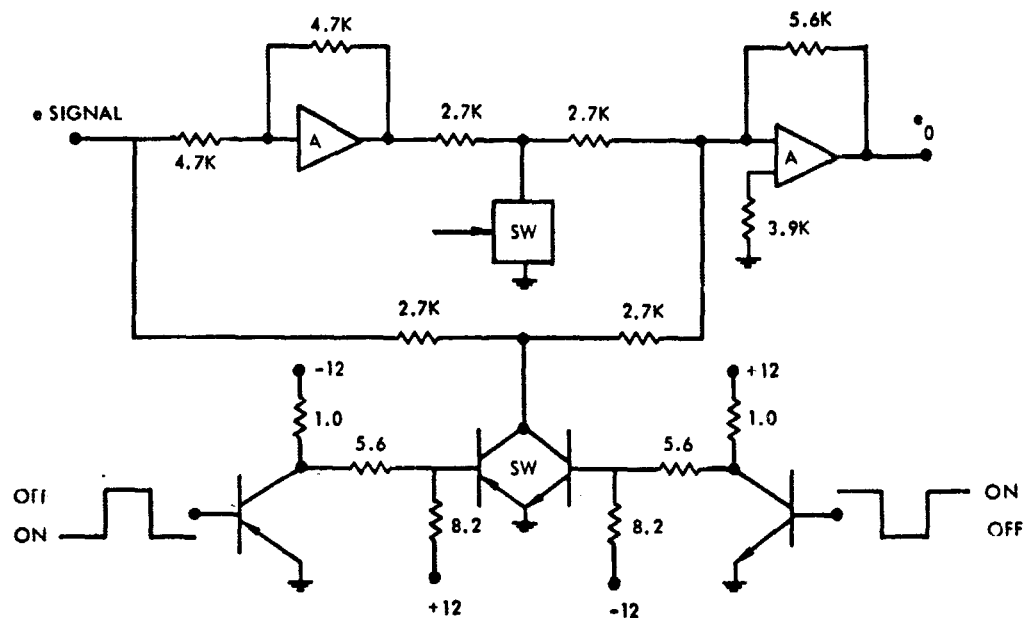
The chopper output for the first half bit period (when S1 is closed) is:

$$E_{01} = (E \text{ sig} + \Delta S) \frac{R_2}{2R_1} \pm \Delta 1 \frac{R_2}{R_1} \pm \Delta 4 .$$

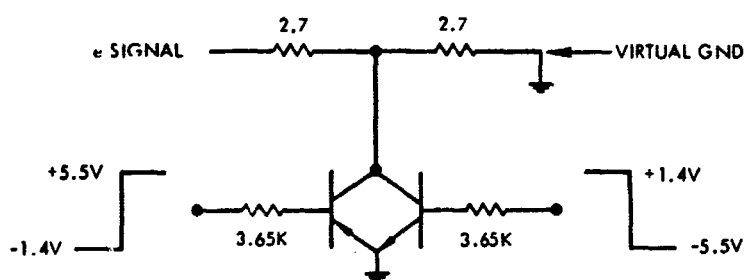
The chopper output for the last half bit period (when S2 is closed) is:

$$E_{02} = -(E \text{ sig} + \Delta S \pm \Delta 3) \frac{R_2}{2R_1} \pm \Delta 2 \left(\frac{R_2}{R_1} \right) \pm \Delta 4 .$$

From the above expressions it is seen that the input signal offset (ΔS) is always equal in magnitude but opposite in polarity over each bit period. Therefore, when using the split phase code, all DC error prior to the SP chopper is integrated out and need not be considered.



(a) Split Phase Chopper Schematic



(b) Approximate Equivalent Circuit of Split Phase Chopper

Figure B-5 Circuit Diagram of Split Phase Chopper

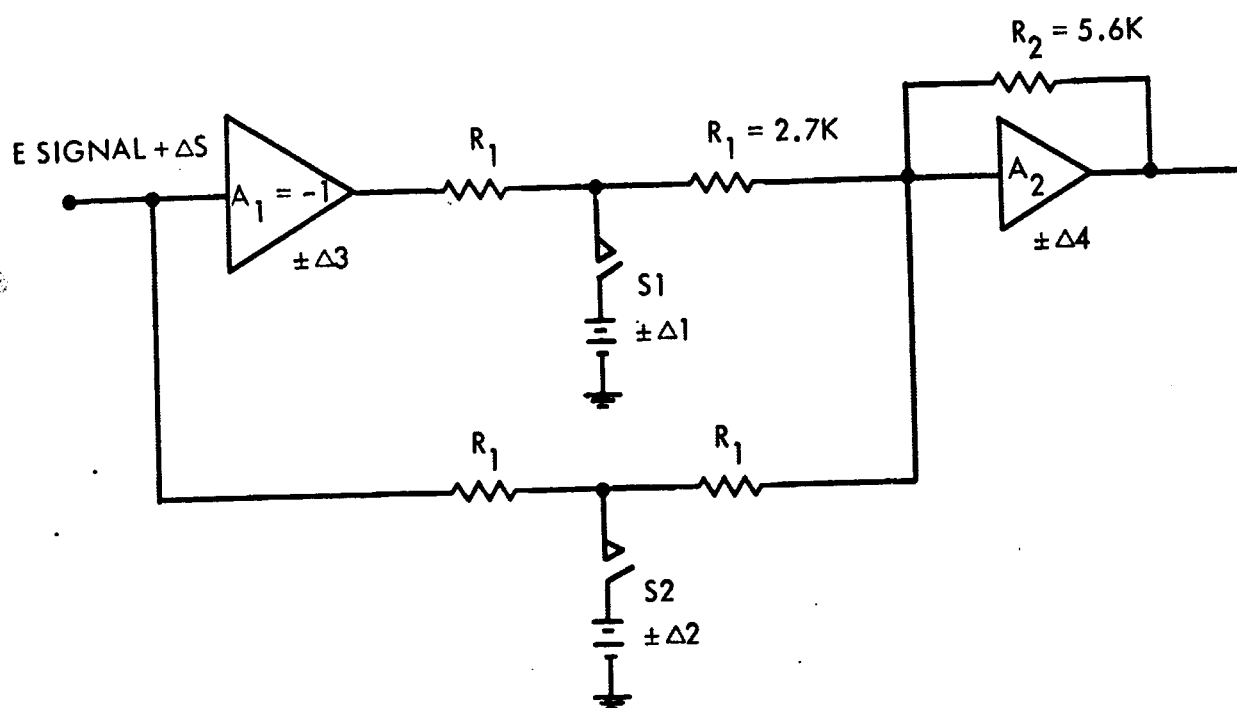


Figure B-6 Equivalent Circuit of Split Phase Chopper

The resulting offset error (ΔC) out of the chopper over each half bit period is:

$$\Delta C_1 = \pm \Delta 1 \left(\frac{R_2}{R_1} \right) \pm \Delta 4$$

$$\Delta C_2 = \pm \Delta 2 \left(\frac{R_2}{R_1} \right) \pm \Delta 3 \frac{R_2}{2R_1} \pm \Delta 4.$$

Assuming the switch offset ($\Delta 1$ & $\Delta 2$) to be equal and of the same polarity, the offset over the bit time is:

$$\Delta C = \pm \Delta 1 \left(\frac{R_2}{R_1} \right) \pm \frac{1}{2} \Delta 3 \left(\frac{R_2}{2R_1} \right) \pm \Delta 4 .$$

Since the nominal signal level is 2.0V, the normalized error per millivolt of offset is:

$$\text{Normalized Error} = \frac{1 \times 10^{-3}}{2} (100) = 0.05 \frac{\text{Percent of Sig Ampl}}{\text{MV Offset}}$$

$$\frac{R_2}{R_1} = \frac{5.6}{2.7} = 2.08$$

$$\frac{R_2}{2R_1} = 1.04$$

$$\Delta C = \pm 0.104 \frac{\% \text{ of Sig Ampl}}{\text{MV Switch Offset}} \pm 0.025 \frac{\% \text{ of Sig Ampl}}{\text{MV Amp Offset}} \pm 0.05 \frac{\% \text{ of Sig Ampl}}{\text{MV Amp Offset}}$$

3.3 INTEGRATE AND DUMP FILTER CIRCUIT ERROR

The I&D filter is shown in simplified form in Figure B-7. The values of R and C are programmed as a function of bit rate to maintain a near ideal integration time constant. This results in a voltage attenuation in the RC network of approximately 10 to 1. The loss is regained in the output amplifier whose gain is maintained at approximately 10. At the sampling time (end of each bit period), assuming the magnitudes of the switch offset are equal, the voltage out of the amplifier is:

$$E_0 = E_c \left(\frac{10R}{R} \right) \pm \Delta 1 \frac{10R}{R} \pm \Delta 3$$

$\Delta 3$ = the total output DC offset of the amplifier

E_c = final voltage on the capacitor

$\Delta 1 = \Delta 2$ = switch offset.

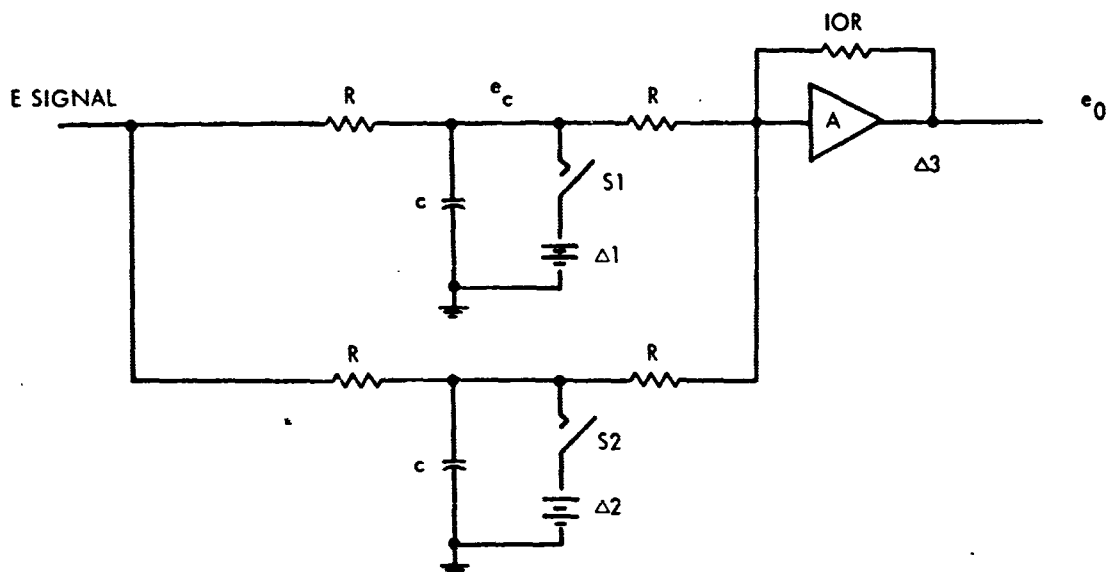
The DC error (ΔI) out of the I&D filter is:

$$\Delta I = \pm 10\Delta 1 \pm \Delta 3$$

Since the nominal signal level out of the amplifier is 2.0V, the normalized error per millivolt offset is:

$$\text{Normalized Error} = \frac{1 \times 10^{-3}}{2} \times 100 = 0.05 \frac{\% \text{ of Sig Ampl}}{\text{MV Offset}}$$

$$\Delta I = \pm 0.5 \frac{\% \text{ of Sig Ampl}}{\text{MV Switch Offset}} \pm 0.05 \frac{\% \text{ of Sig Ampl}}{\text{MV Amp Offset}}$$



INPUT (E SIGNAL)

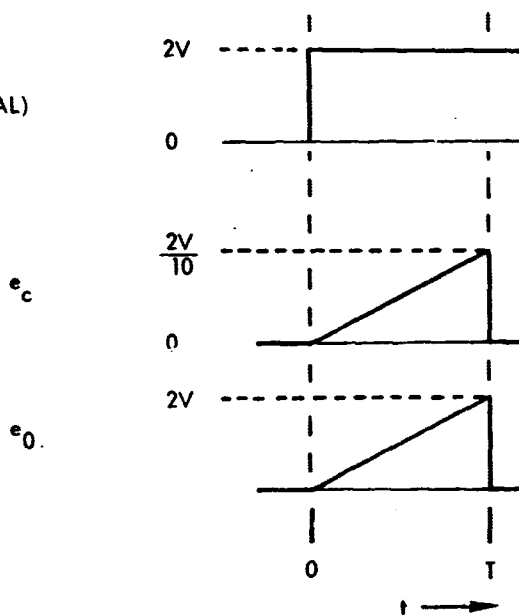


Figure B-7 Simplified Circuit of MSFTP-2 Integrate and Dump Bit Detector

3.4 ERROR DUE TO TUNABLE LOW PASS FILTER OFFSET

The tunable low pass filter is shown in Figure B-8. The filter consists of an active three section low pass filter preceeded by a resistive attenuator with attenuation factor of 5:1 and followed by an amplifier with gain of 5. The attenuation preceeding the filter is required to avoid overdriving the active filter and the amplifier is used to maintain an overall gain of one.

The active filter utilizes junction FET transistors as resistive elements in three (3) RC sections. Fine tuning of the filter is accomplished by varying the resistance of the FET devices by a control voltage. The MSFN technical information states that the FET devices induce DC offsets in the filter which are compensated by an internal DC regulator. The magnitudes of the offset are not specified.

The amplifier output is:

$$E_o = 5(E_F \pm \Delta 1) \pm \Delta 2$$

$\Delta 1$ = filter DC offset

$\Delta 2$ = total output offset of amplifier

The L.P. filter DC error is:

$$\Delta F = \pm 5 \Delta 1 \pm \Delta 2$$

The nominal output signal level is 2.0 volts peak, therefore:

$$\Delta F = \pm 5 \frac{1 \times 10^{-3}}{2} (100) \pm \frac{1 \times 10^{-3}}{2} (100) \frac{\text{percent signal ampl}}{\text{MV offset}}$$

$$\Delta F = \pm 0.25 \frac{\% \text{ Sig Ampl}}{\text{MV Filter Offset}} \pm 0.05 \frac{\% \text{ Sig Ampl}}{\text{MV Amp Offset}}$$

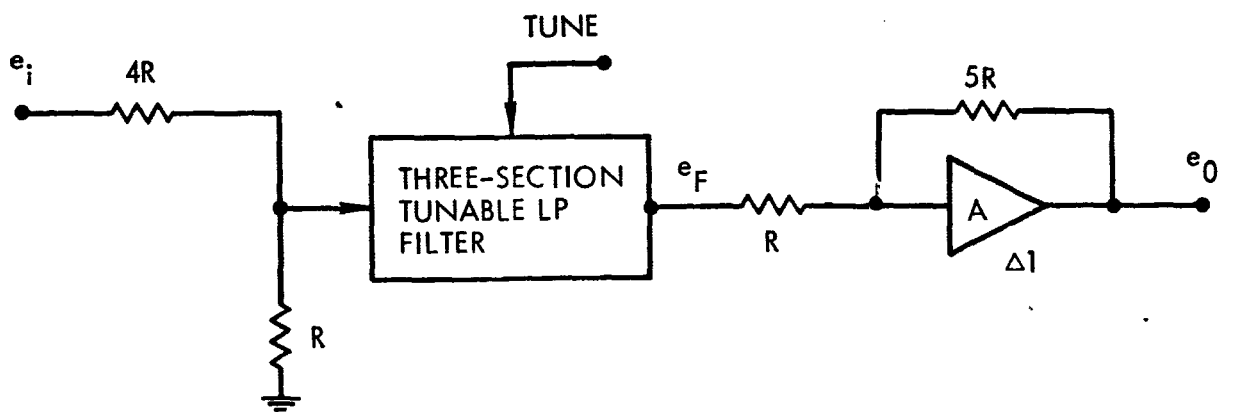


Figure B-8 Simplified Schematic of Tunable Low Pass Filter

3.5 ERROR DUE TO SCHMITT TRIGGER HYSTERESIS

The loss due to hysteresis in the schmitt trigger depends on the transition density. This is illustrated in Figure B-9. The figure shows a schmitt trigger (ST) fed by an I&D filter but the losses due to hysteresis hold for any other filter. The schmitt trigger has hysteresis (X) which determines the upper, and lower trigger points. It is assumed that the hysteresis is symmetrical about zero so the UTP and LTP are equal. Once the input voltage to the ST has crossed above the UTP the output state will not change until the input voltage crosses below the LTP. Likewise if the LTP has been exceeded there will be no change of state until the UTP is exceeded.

If a transmitted symbol (a one, for example) was preceeded by a like symbol (also a one) which caused the UTP to be crossed, then a noise induced error can occur only if the magnitude of the noise voltage on the transmitted symbol is equal to the signal voltage plus the hysteresis.

If the transmitted symbol (again a one) was preceeded by a zero (a transition occurred), then a noise induced error would occur if the magnitude of the noise voltage were equal to the signal voltage minus the hysteresis. Therefore the hysteresis improves the likelihood of making the correct decision if no transition occurs and decreases the likelihood of making the correct decision if a transition occurs. The hysteresis voltage (X) effectively adds to the signal voltage if no transition occurs and subtracts from the signal voltage if a transition does occur.

Since the ST error depends on the transition density, its error contribution cannot be added directly to the DC error budget but must be calculated separately.

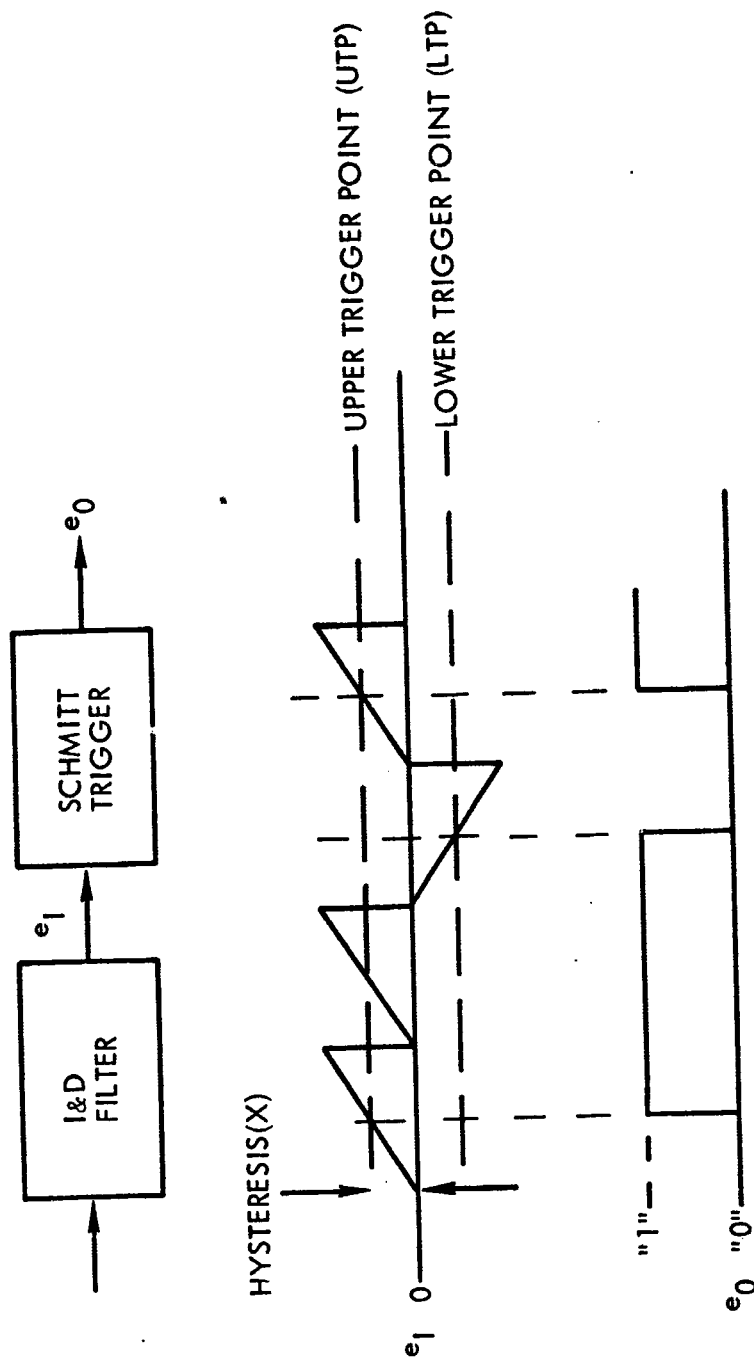


Figure B-9 Illustrating Input/Output Waveforms of Schmitt Trigger
Used in I&D Bit Detector

The probability of error due to ST hysteresis is:

$$P_E = 1 - M \phi[\lambda(1 + X)] - (1 - M) \phi[\lambda(1 - X)]$$

M = transition density

λ = voltage SNR

$\phi(\lambda)$ = cumulative Gaussian dist. function

X = hysteresis normalized to the peak signal level

Since the nominal peak signal level at the ST input is 2.0V, the normalized ST hysteresis is:

$$X = \frac{1 \times 10^{-3}}{2} (100) = \frac{0.05\% \text{ of peak sig ampl}}{\text{MV ST Hyst.}}$$

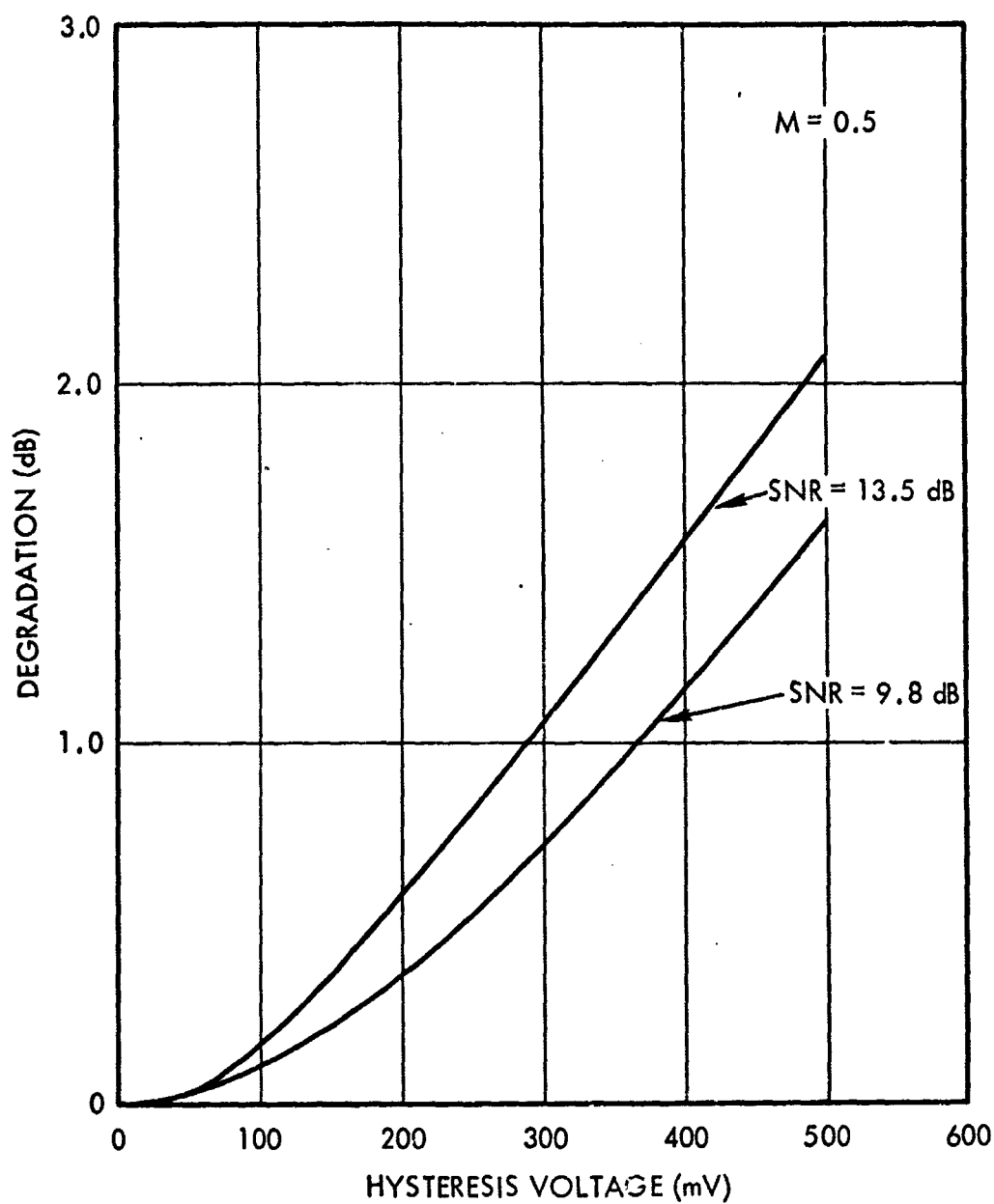


Figure B-10 Performance Degradation Versus Schmitt Trigger Hysteresis Voltage

APPENDIX C

INTEGRATE AND DUMP FILTER SIGNAL LOSS DUE TO PREFILTERING AND TIMING ERROR

1.0 GENERAL

In this appendix the expressions for signal loss (amplitude reduction) at the I&D output with the input PCM data prefiltered by a one pole low pass filter, an ideal square low pass filter, and a six pole Butterworth low pass filter are given. Also given are the expressions for I&D signal loss due to timing error with the input PCM data prefiltered with a six pole Butterworth low pass filter.

2.0 ONE POLE LOW PASS PREFILTER

The one pole low pass filter, shown in Figure C-1 has the transfer function $H(j\omega)$ given by:

$$H(j\omega) = \frac{1}{1 + j\omega RC}$$

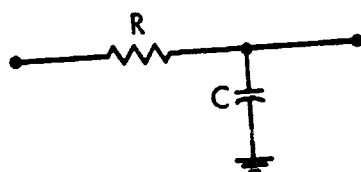
The response to a step input $A(t)$ is:

$$E_o(t) = A \left(1 - e^{-\frac{t}{RC}} \right)$$

The response to a pulse one bit period (T) wide is:

$$E_o(t) = A \left[1 - e^{-\frac{t}{RC}} - u(t-T) e^{-\frac{(t-T)}{RC}} \right]$$

The step and pulse response is shown in Figure C-2.



$$H(j\omega) = \frac{1}{1 + j\omega RC}$$

Figure C-1 One Pole Low Pass Filter

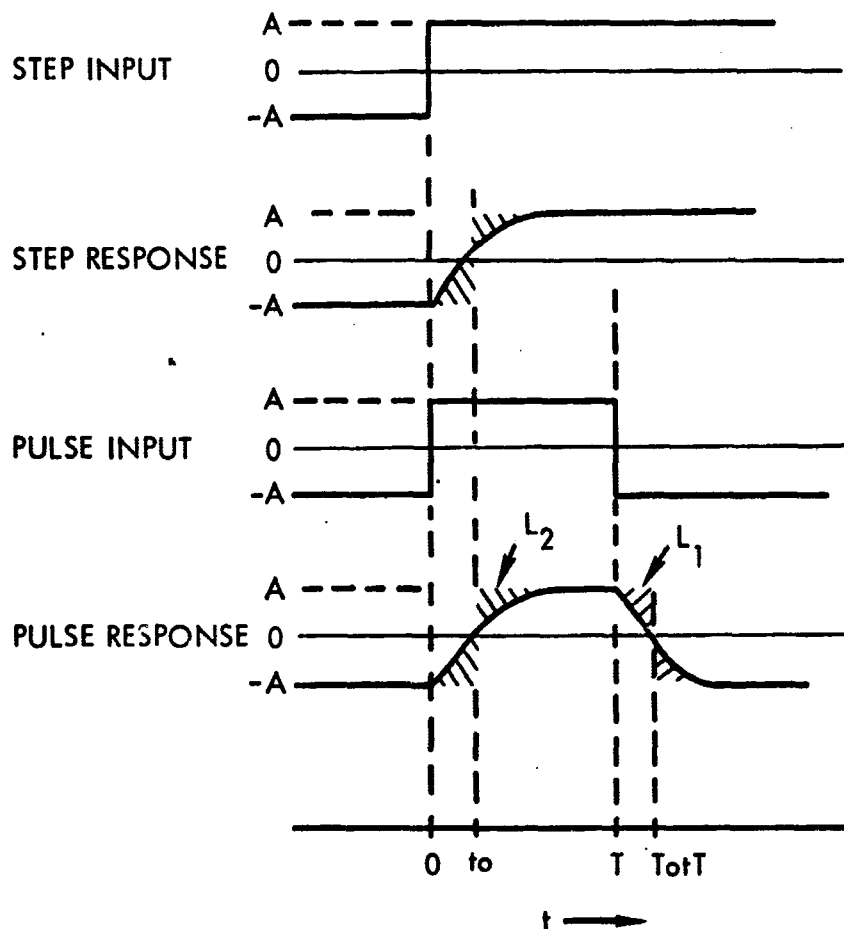


Figure C-2 Response of One Pole Filter to Step and Pulse Inputs

The voltage output of the I&D filter with a one pole filter is the area under a square pulse (0 to T) less the loss (L_1 , L_2) which occurs due to transitions. The losses (L_1 and L_2) are represented by the shaded areas of Figure C-2.

Inspection of Figure C-2 shows that there are four possible waveforms, over a bit time, out of the one pole low pass filter. The four waveforms are shown in Figure C-3.

The loss factors which are the I&D voltage outputs with the filter normalized to the I&D voltage output without the filter for each of the four possible waveforms are:

$$a_1 = \frac{\frac{1}{T} \int_0^T \frac{A}{2} dt - L_1 - L_2}{\frac{1}{T} \int_0^T \frac{A}{2} dt}$$

$$a_1 = \frac{\frac{1}{2} A - L_1 - L_2}{\frac{1}{2} A} = 1 - \frac{2(L_1 + L_2)}{A}$$

Similarly:

$$a_2 = \frac{\frac{1}{2} A - L_1}{\frac{1}{2} A} = 1 - \frac{2L_1}{A}$$

$$a_3 = \frac{\frac{1}{2} A - L_2}{\frac{1}{2} A} = 1 - \frac{2L_2}{A}$$

$$a_4 = \frac{\frac{1}{2} A}{\frac{1}{2} A} = 1$$

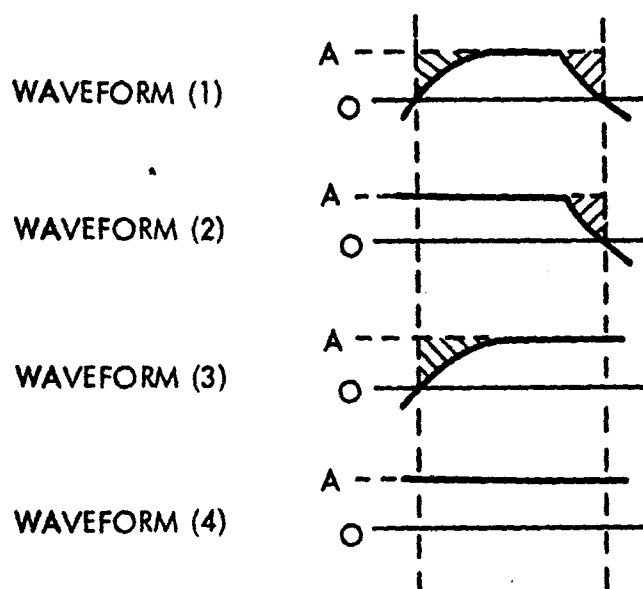


Figure C-3 Four Possible Waveforms, Over a Bit Period,
at the Output of the One Pole Low Pass Filter
with Unfiltered PCM Input

The losses L_1 and L_2 are as follows:

$$L_1 = \frac{1}{T} \int_0^{t_0} A \, dt - \frac{1}{T} \int_0^{t_0} A e^{-\frac{t}{RC}} \, dt$$

$$L_1 = A \frac{t_0}{T} + A \frac{RC}{T} \left(e^{-\frac{t_0}{RC}} - 1 \right)$$

t_0 is the filter delay and is the time at which the waveform crosses $\frac{A}{2}$.

$$A e^{-\frac{t_0}{RC}} = \frac{1}{2} A$$

$$e^{-\frac{t_0}{RC}} = \frac{1}{2}$$

$$t_0 = 0.695 RC$$

$$L_1 = A \left(\frac{0.695 RC}{T} \right) - A \frac{RC}{T} (0.5)$$

$$L_1 = A \frac{RC}{T} (0.195)$$

$$RC = \frac{1}{2\pi f_c}$$

f_c = filter 3 db cut off frequency

$$T = \frac{1}{f_B}$$

f_B = bit rate

$$L_1 = \frac{A}{2\pi} \left(\frac{f_B}{f_c} \right) (0.195)$$

$$L_2 = \frac{1}{T} \int_{t_0}^T A e^{-\frac{t}{RC}}$$

$$L_2 = -A \frac{RC}{T} \left(e^{-\frac{T}{RC}} - e^{-\frac{t_0}{RC}} \right)$$

$$L_2 = -A \frac{RC}{T} \left(e^{-\frac{T}{RC}} - 0.5 \right)$$

$$L_2 = \frac{A}{2\pi} \left(\frac{f_B}{f_c} \right) \left(0.5 - e^{-2\pi \frac{f_c}{f_B}} \right)$$

$$\frac{f_c}{f_B} = R \quad R \geq 0.5$$

$$L_1 = \frac{A}{2\pi} \frac{1}{R} (0.195)$$

$$L_2 = \frac{A}{2\pi} \frac{1}{R} \left(0.5 - e^{-2\pi R} \right)$$

$$L_1 + L_2 = \frac{A}{2\pi R} \left(0.695 - e^{-2\pi R} \right)$$

The signal loss factors are:

$$a_1 = 1 - \frac{1}{\pi R} (0.695 - e^{-2\pi R})$$

$$a_2 = 1 - \frac{1}{\pi R} (0.195)$$

$$a_3 = 1 - \frac{1}{\pi R} (0.5 - e^{-2\pi R})$$

$$a_4 = 1$$

3.0 IDEAL LOW PASS FILTER

The passband characteristic of the "ideal" low pass filter is shown in Figure C-4. This is a non-realizable filter. The response of this filter to a step input $A(t)$ is [1]:

$$E_o(t) = \frac{A}{2} + \frac{A}{\pi} \text{Si}(\omega_c t)$$

$$\text{Si}(x) = \int \frac{\sin x}{x} dx$$

$$\omega_c = 2\pi f_c$$

$$R = \frac{f_c}{f_B} = \frac{\text{filter cut off frequency}}{\text{bit rate}}$$

$$T = \frac{1}{f_B} = \text{bit period}$$

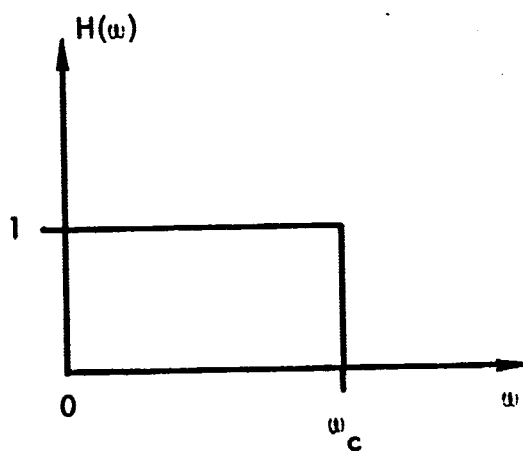


Figure C-4 Passband of Ideal Low Pass Filter

$$\omega_c = 2\pi R \left(\frac{1}{T} \right)$$

$$E_o(t) = \frac{A}{2} + \frac{A}{\pi} \text{Si } 2\pi R \frac{t}{T}$$

The response to an input pulse of amplitude (A) and width (T) is:

$$E_{op}(t) = E_o(t) - E_o(t-T)$$

$$E_{op}(t) = \frac{A}{2} + \frac{A}{\pi} \text{Si } 2\pi R \frac{t}{T} - \left[\frac{A}{2} + \frac{A}{\pi} \text{Si } 2\pi R \left(\frac{t}{T} - 1 \right) \right]$$

$$\text{Si}(-x) = -\text{Si } x$$

$$E_{op}(t) = \frac{A}{\pi} \left[\text{Si } 2\pi R \frac{t}{T} - \text{Si } 2\pi R \left(\frac{t}{T} - 1 \right) \right]$$

Let A = 1

Then:

Step Response is:

$$E_o(t) = \frac{1}{2} + \frac{1}{\pi} \text{Si } 2\pi R \left(\frac{t}{T} \right)$$

Pulse Response is:

$$E_{op}(t) = \frac{1}{\pi} \left[\text{Si } 2\pi R \frac{t}{T} - \text{Si } 2\pi R \left(\frac{t}{T} - 1 \right) \right]$$

The step and pulse response for $R = 1.5$ is plotted in Figure C-5 as a function of time normalized to a bit period $\left(\frac{t}{T}\right)$.

The signal loss factors for the I&D filter are the areas under step and pulse response curves (above the one-half value) over a bit period, normalized to the area under a square pulse one bit period wide. The loss factors are found by integrating the step and pulse responses.

$$\text{Let } \frac{t}{T} = X$$

$$E_o(X) = \frac{1}{2} + \frac{1}{\pi} \text{Si } 2\pi R X$$

$$E_o(X-1) = \frac{1}{2} + \frac{1}{\pi} \text{Si } 2\pi R(X-1)$$

$$E_{op}(X) = \frac{1}{\pi} [\text{Si } 2\pi R X - \text{Si } 2\pi R(X-1)]$$

$$a_1 = \frac{\int_0^{X=1} E_{op}(X) dx - \int_0^{X=1} \frac{1}{2} dx}{\int_0^{X=1} \frac{1}{2} dx}$$

$$a_1 = \frac{\int_0^{X=1} \frac{1}{\pi} [\text{Si } 2\pi R X - \text{Si } 2\pi R(X-1)] dx - \int_0^{X=1} \frac{1}{2} dx}{\int_0^{X=1} \frac{1}{2} dx}$$

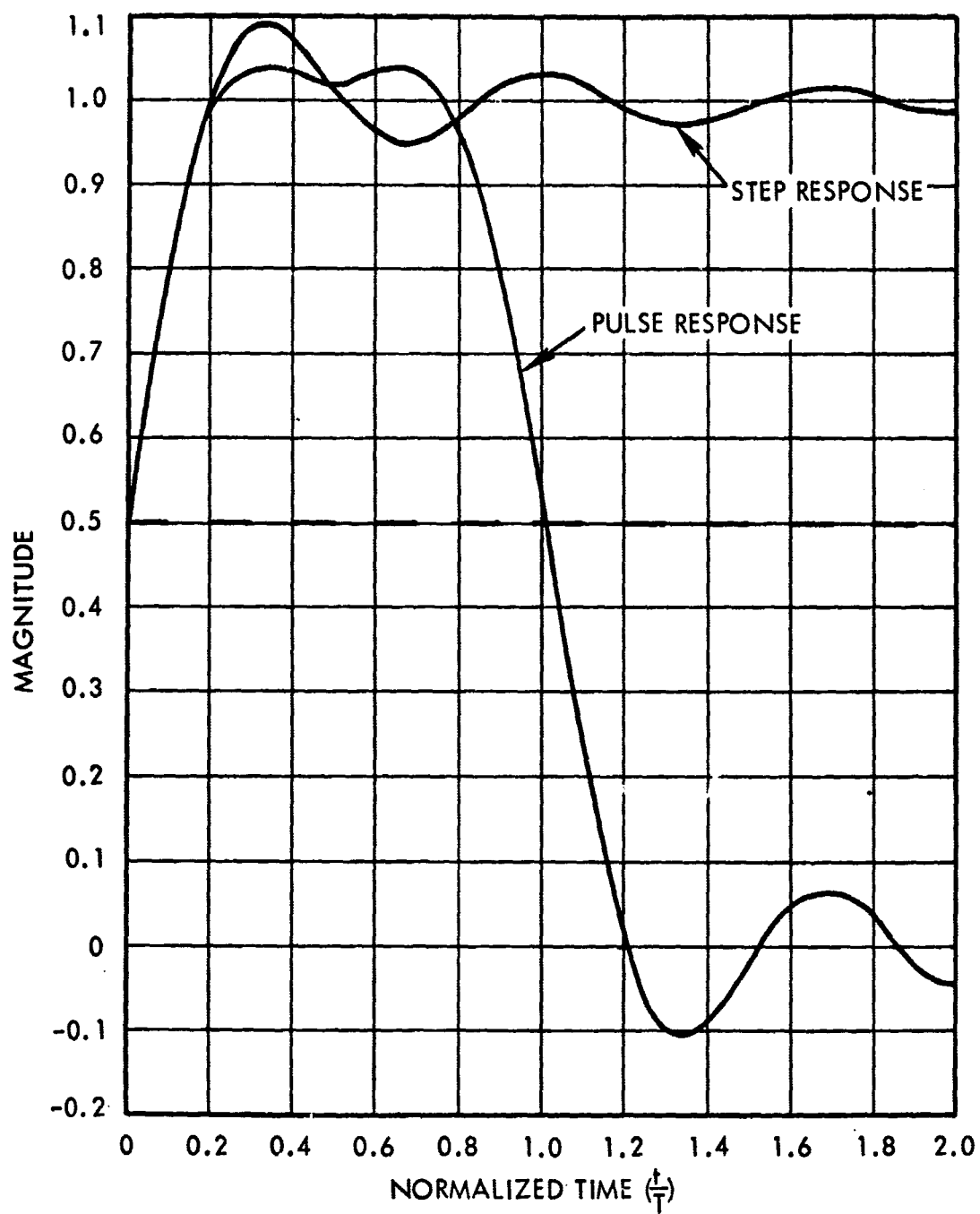


Figure C-5 Ideal Filter Step and Pulse Response

$$a_1 = \frac{\int_0^{X=R} \frac{1}{\pi} \left[\text{Si } 2\pi X \, dx - \text{Si } 2\pi(X-1) \right] dx - \int_0^{X=R} \frac{1}{2} \, dx}{\int_0^{X=R} \frac{1}{2} \, dx}$$

$$a_1 = \frac{2}{R} \int_0^R \frac{1}{\pi} \left[\text{Si } 2\pi X \, dx - \text{Si } 2\pi(X-1) \right] dx - 1$$

$$- \int_0^R \frac{1}{\pi} \text{Si } 2\pi(X-1) \, dx = \int_0^R \text{Si } 2\pi X \, dx$$

$$a_1 = \frac{2}{R} \int_0^R \frac{1}{\pi} \text{Si } 2\pi X \, dx + \frac{2}{R} \int_0^R \text{Si } 2\pi X \, dx - 1$$

$$a_1 = \frac{4}{R} \int_0^R \frac{1}{\pi} \text{Si } 2\pi X \, dx - 1$$

$$a_2 = a_3 = \frac{\int_0^R \left[\frac{1}{2} + \frac{1}{\pi} \text{Si } 2\pi X \right] dx - \frac{1}{2} \int_0^R dx}{\frac{1}{2} \int_0^R dx}$$

$$a_2 = a_3 = \frac{2}{R} \int_0^R \frac{1}{\pi} \text{Si } 2\pi X \, dx$$

$$a_4 = 1$$

The equations for the signal loss factors contain the integral of the Si function which cannot be shown in closed form. The integration was performed numerically, using a computer, as explained below.

The function $(\int_0^X \frac{1}{\pi} \text{Si } 2\pi X \, dx)$ was integrated numerically by evaluating it for incremental (X) and summing the results of each evaluation. A table was printed out $(I|_0^X)$ from which the value of the integral between desired limits (0 to X) could be read. Using the printed table the signal loss factors were read as follows:

$$a_1 = \frac{4}{R} \left(I|_0^{X=R} \right) - 1$$

$$a_2 = a_3 = \frac{2}{R} \left(I|_0^{X=R} \right)$$

The signal loss factors were read for a range of (R) from 0.5 to 8.0 and are included in Table 4.3.2.1.

4.0 SIX POLE BUTTERWORTH FILTER

4.1 TRANSFER FUNCTION AND TIME RESPONSE

The pole locations of the six section Butterworth low pass filter are shown in Figure C-6. They are:

$$S_{1,2} = -B \pm jA$$

$$S_{3,4} = -C \pm jC$$

$$S_{5,6} = -A \pm jB$$

$$A = \cos 15^\circ = \sqrt{\frac{1}{2} + \frac{\sqrt{3}}{4}} = 0.9659$$

$$B = \sin 15^\circ = \sqrt{\frac{1}{2} - \frac{\sqrt{3}}{4}} = 0.2588$$

$$C = \sin 45^\circ = \frac{\sqrt{2}}{2} = 0.7071$$

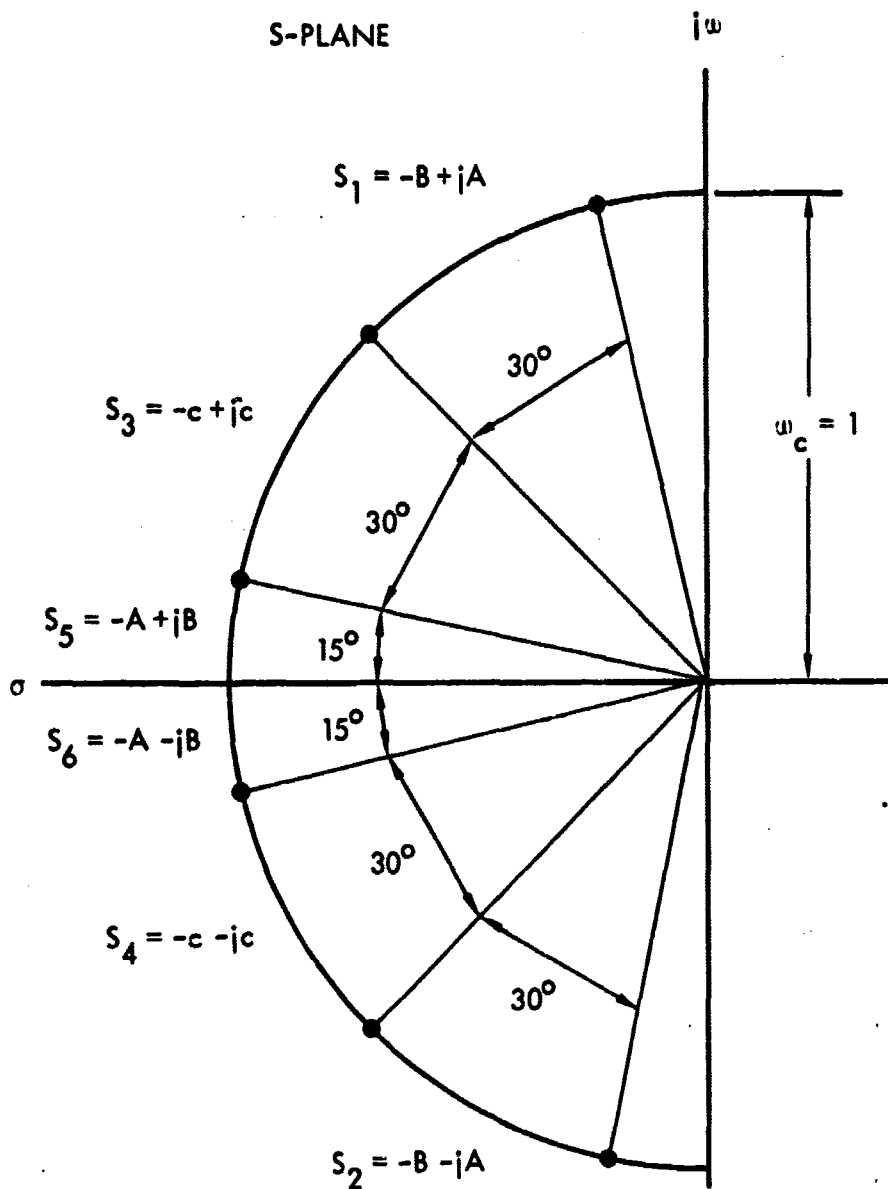


Figure C-6 Pole Locations of Six Pole Butterworth Low Pass Filter

The transfer function is:

$$H(S) = \frac{1}{(S+B-jA)(S+B+jA)(S+C-jC)(S+C+jC)(S+A-jB)(S+A+jB)}$$

$$H(S) = \frac{1}{(S^2+2BS+A^2+B^2)(S^2+2AS+A^2+B^2)(S^2+2CS+2C^2)}$$

The response to a unit step input is:

$$F(S) = H(S)\left(\frac{1}{S}\right) = \frac{1}{S(S^2+2BS+A^2+B^2)(S^2+2AS+A^2+B^2)(S^2+2CS+2C^2)}$$

which is of the form:

$$F(S) = \frac{1}{S(S^2+2\zeta_1\omega_1S+\omega_1^2)(S^2+2\zeta_2\omega_2S+\omega_2^2)(S^2+2\zeta_3\omega_3S+\omega_3^2)}$$

and has time response of the form:

$$\begin{aligned} f(t) = & K_0 + 2K_1e^{-\zeta_1\omega_1t} \sin(\omega_1\sqrt{1-\zeta_1^2}t + \phi_1) \\ & + 2K_2e^{-\zeta_2\omega_2t} \sin(\omega_2\sqrt{1-\zeta_2^2}t + \phi_2) \\ & + 2K_3e^{-\zeta_3\omega_3t} \sin(\omega_3\sqrt{1-\zeta_3^2}t + \phi_3) \end{aligned}$$

$$K_1 = (S_1 - S_1) F(S) \Big|_{S = S_1}$$

$$\phi_1 = \text{Angle of } K_1 + 90^\circ$$

$$\zeta_1 \omega_1 = B$$

$$\omega_1 = \sqrt{A^2 + B^2} = 1 = \omega_c$$

$$\zeta_2 \omega_2 = A$$

$$\omega_2 = \sqrt{A^2 + B^2} = 1 = \omega_c$$

$$\zeta_3 \omega_3 = C$$

$$\omega_3 = \sqrt{2} C = 1 = \omega_c$$

$$\sqrt{1 - \zeta_1^2} = \sqrt{1 - B^2} = A$$

$$\sqrt{1 - \zeta_2^2} = \sqrt{1 - A^2} = B$$

$$\sqrt{1 - \zeta_3^2} = \sqrt{1 - C^2} = C$$

$$f(t) = K_0 + 2K_1 e^{-B\omega_c t} \sin(A\omega_c t + \phi_1)$$

$$+ 2K_2 e^{-A\omega_c t} \sin(B\omega_c t + \phi_2)$$

$$+ 2K_3 e^{-C\omega_c t} \sin(C\omega_c t + \phi_3)$$

$$K_0 = S F(S) \Big|_{S=0}$$

$$K_0 = \frac{1}{(B-jA)(B+jA)(C-jC)(C+jC)(A-jB)(A+jB)} = 1$$

$$K_1 = (S+B-jA) F(S) \Big|_{S=-B+jA}$$

$$K_1 = \frac{1}{(-B+jA)(j2A)[(\dot{C}-B)=j(A-C)][(C-B)+j(A-C)][(A-B)+j(A-B)][(A-B)+j(A+B)]}$$

$$K_1 = \frac{1}{\sqrt{2} \sqrt{3}} \quad \angle -\frac{\pi}{4}$$

$$K_2 = (S+A-jB) F(S) \Big|_{S=-A+jB}$$

$$K_2 = -\frac{1}{\sqrt{2} (2-\sqrt{3})} \quad \angle -\frac{\pi}{4}$$

$$K_3 = (S+C-jC) F(S) \Big|_{S=-C+jC} = \frac{1}{\sqrt{2} (2\sqrt{3}-3)} \quad \angle \frac{\pi}{4}$$

$$\phi_1 = -\frac{\pi}{4} + \frac{\pi}{2} = \frac{\pi}{4}$$

$$\phi_2 = -\frac{\pi}{4} + \frac{\pi}{2} = \frac{\pi}{4}$$

$$\phi_3 = \frac{\pi}{4} + \frac{\pi}{2} = \frac{3\pi}{4}$$

The step time response is then:

$$\begin{aligned}
 f(t) = & 1 + \frac{\sqrt{2}}{\sqrt{3}} e^{-B\omega_c t} \sin\left(A\omega_c t + \frac{\pi}{4}\right) \\
 & - \frac{\sqrt{2}}{2-\sqrt{3}} e^{-A\omega_c t} \sin\left(B\omega_c t + \frac{\pi}{4}\right) \\
 & + \frac{\sqrt{2}}{2\sqrt{3}-3} e^{-C\omega_c t} \sin\left(C\omega_c t + \frac{3\pi}{4}\right)
 \end{aligned}$$

$$\omega_c = 2\pi f_c$$

$$\frac{f_c}{f_B} = R$$

$$\begin{aligned}
 f_c &= 3 \text{ db cut off frequency} \\
 f_B &= \frac{1}{T} = \text{bit rate}
 \end{aligned}$$

$$\omega_c = 2\pi R \frac{1}{T}$$

Therefore the step response is:

$$\begin{aligned}
 f(t) = & 1 + \frac{\sqrt{2}}{\sqrt{3}} e^{-B2\pi R \frac{t}{T}} \sin\left(A2\pi R \frac{t}{T} + \frac{\pi}{4}\right) \\
 & - \frac{\sqrt{2}}{2-\sqrt{3}} e^{-A2\pi R \frac{t}{T}} \sin\left(B2\pi R \frac{t}{T} + \frac{\pi}{4}\right) \\
 & + \frac{\sqrt{2}}{2\sqrt{3}-3} e^{-C2\pi R \frac{t}{T}} \sin\left(C2\pi R \frac{t}{T} + \frac{3\pi}{4}\right)
 \end{aligned}$$

The response to a pulse one bit period wide is:

$$f(t) - f(t - T)$$

$$\begin{aligned}
 f(t-T) = & 1 + \frac{\sqrt{2}}{\sqrt{3}} e^{-B2\pi R \left(\frac{t}{T} - 1\right)} \sin\left[A2\pi R \left(\frac{t}{T} - 1\right) + \frac{\pi}{4}\right] \\
 & - \frac{\sqrt{2}}{2-\sqrt{3}} e^{-A2\pi R \left(\frac{t}{T} - 1\right)} \sin\left[B2\pi R \left(\frac{t}{T} - 1\right) + \frac{\pi}{4}\right] \\
 & + \frac{\sqrt{2}}{2\sqrt{3}-3} e^{-C2\pi R \left(\frac{t}{T} - 1\right)} \sin\left[C2\pi R \left(\frac{t}{T} - 1\right) + \frac{3\pi}{4}\right]
 \end{aligned}$$

The response of the filter to a unit step input and a bit period pulse is shown in Figure C-7. The ratio of filter 3 db frequency and bit rate $\left(\frac{f_c}{f_B}\right)$ of Figure C-7 is 1.5.

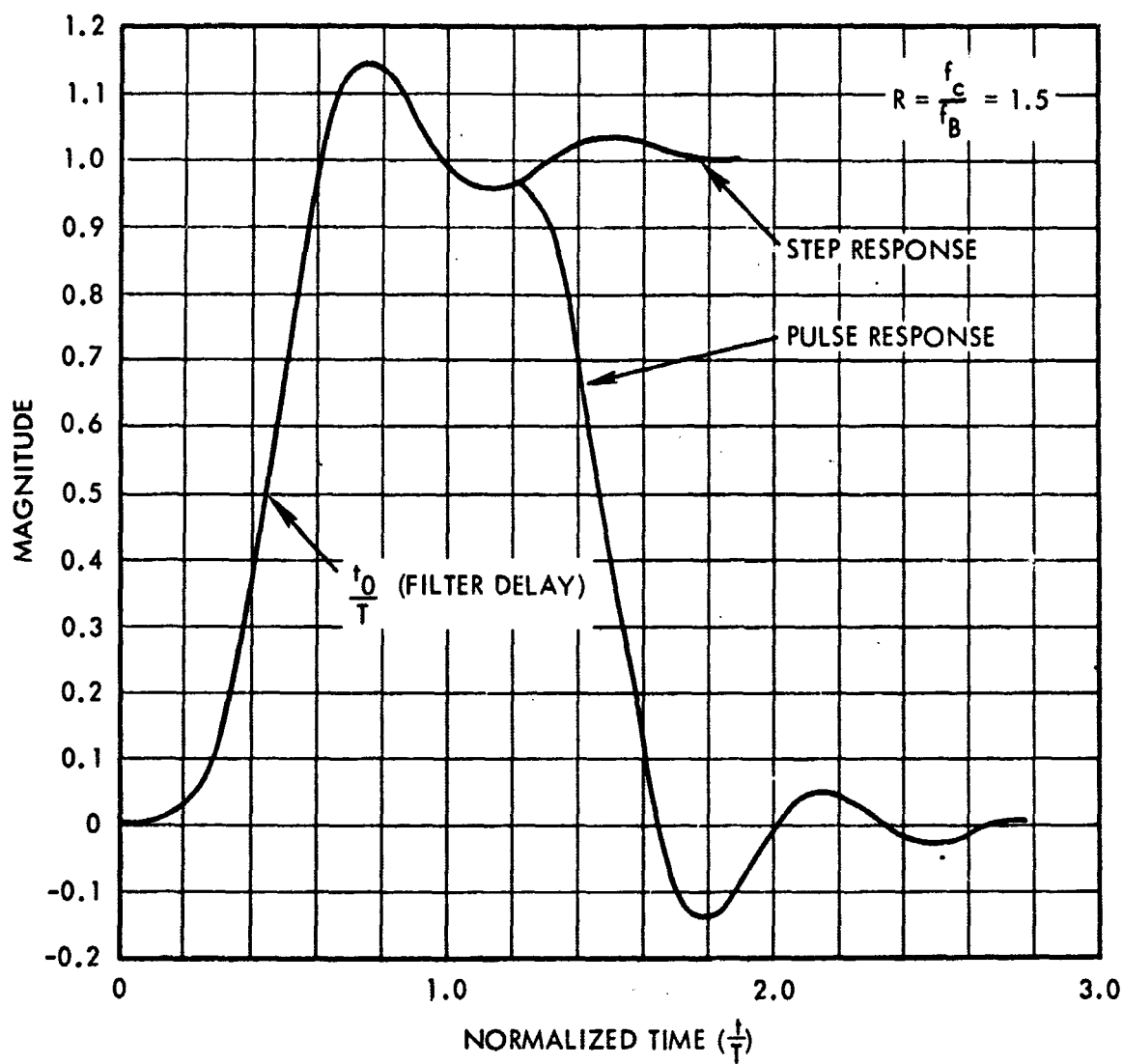


Figure C-7 Six Pole Butterworth Filter Step and Pulse Response

4.2 SIGNAL LOSS FACTORS SIX POLE BUTTERWORTH FILTER

Let $\frac{t}{T} = X$

$\frac{t_0}{T} = X_0$ filter delay (See Figure C-7)

$$F(X) = 1 + \frac{\sqrt{2}}{\sqrt{3}} e^{-B2\pi RX} \sin\left(A2\pi RX + \frac{\pi}{4}\right)$$

$$- \frac{\sqrt{2}}{2-\sqrt{3}} e^{-A2\pi RX} \sin\left(B2\pi RX + \frac{\pi}{4}\right)$$

$$+ \frac{\sqrt{2}}{2\sqrt{3}-3} e^{-C2\pi RX} \sin\left(C2\pi RX + \frac{3\pi}{4}\right)$$

$$F(X-1) = 1 + \frac{\sqrt{2}}{\sqrt{3}} e^{-B2\pi R(X-1)} \sin\left[A2\pi R(X-1) + \frac{\pi}{4}\right]$$

$$- \frac{\sqrt{2}}{2-\sqrt{3}} e^{-A2\pi R(X-1)} \sin\left[B2\pi R(X-1) + \frac{\pi}{4}\right]$$

$$+ \frac{\sqrt{2}}{2\sqrt{3}-3} e^{-C2\pi R(X-1)} \sin\left[C2\pi R(X-1) + \frac{3\pi}{4}\right]$$

$$E_{(X)} = F_{(X)} \text{ with } R = 1$$

$$E_{(X-1)} = F_{(X-1)} \text{ with } R = 1$$

$$E_{(X)} = 1 + \frac{\sqrt{2}}{\sqrt{3}} e^{-2\pi BX} \sin\left(2\pi AX + \frac{\pi}{4}\right)$$

$$- \frac{\sqrt{2}}{2-\sqrt{3}} e^{-2\pi AX} \sin\left(2\pi BX + \frac{\pi}{4}\right)$$

$$+ \frac{\sqrt{2}}{2\sqrt{3}-3} e^{-2\pi CX} \sin\left(2\pi CX + \frac{\pi}{4}\right)$$

$$E_{(X-1)} = 1 + \frac{\sqrt{2}}{\sqrt{3}} e^{-2\pi B(X-1)} \sin\left[2\pi A(X-1) + \frac{\pi}{4}\right]$$

$$- \frac{\sqrt{2}}{2-\sqrt{3}} e^{-2\pi A(X-1)} \sin\left[2\pi B(X-1) + \frac{\pi}{4}\right]$$

$$+ \frac{\sqrt{2}}{2\sqrt{3}-3} e^{-2\pi C(X-1)} \sin\left[2\pi C(X-1) + \frac{3\pi}{4}\right]$$

$$a_1 = \frac{\int_{x=x_0}^{x=x_0+1} [F(x) - F(x-1)] dx - \int_{x_0}^{x_0+1} \frac{1}{2} dx}{\int_{x_0}^{x_0+1} \frac{1}{2} dx}$$

$$\int_{x_0}^{x_0+1} F(x) dx = \int_{x_0}^{x_0+R} E(x) dx$$

$$\int_{x_0}^{x_0+1} F(x-1) dx = \int_0^{x_0} E(x) dx$$

$$\int_{x_0}^{x_0+1} \frac{1}{2} dx = \int_0^R \frac{1}{2} dx = \frac{R}{2}$$

$$a_1 = \frac{\int_{x_0}^{x_0+R} E(x) dx - \int_0^{x_0} E(x) dx - \frac{R}{2}}{\frac{R}{2}}$$

$$a_2 = \frac{\int_{x_0}^{x_0+R} E(x) dx - \frac{R}{2}}{\frac{R}{2}}$$

$$a_3 = \frac{\frac{R}{2} - \int_0^{x_0} E(x) dx}{\frac{R}{2}}$$

$$a_4 = 1$$

The signal loss factors for the six pole Butterworth filter were calculated numerically as follows:

The function $\left(\int_0^x E(x) dx\right)$ was integrated, using a computer, by evaluating it for incremental (X) and summing the results of each evaluation. A table was printed out $(I|_0^x)$ from which the integral between desired limits $(0 \text{ to } X)$ could be read. The value of the filter delay (x_0) was found numerically to be 0.66. Using the printed table the signal loss factors were read as follows:

$$a_1 = \frac{2}{R} \left[I|_{0.66}^{R+0.66} - I|_0^{0.66} \right] - 1$$

$$a_2 = \frac{2}{R} \left[I|_{0.66}^{R+0.66} \right] - 1$$

$$a_3 = 1 - \frac{2}{R} \left[I|_0^{0.66} \right]$$

$$a_4 = 1$$

The loss factors were read for a range of R from 0.5 to 8.0 and are included in table 4.3.2.1.

5.0 SIGNAL LOSS FACTORS WITH TIMING ERROR AND SIX POLE BUTTERWORTH PREFILTER

Figure C-8 shows a sketch of the pulse and step response of the filter, i.e., the response to adjacent transitions and a single transition. A timing error θ is assumed such that the integration period of the I&D filter is displaced from the transition. Inspection of the figure reveals the following:

For adjacent transitions: A voltage loss due to timing error occurs at the I&D output equal to the sum of the shaded areas L_1 and L_2 .

For a single transition: Bit one suffers a voltage loss at the I&D output, due to timing error, equal to the shaded area L_3 and a voltage increase equal to the shaded area L_4 .

Bit two suffers a voltage loss at the I&D output, due to timing error, equal to the sum of the shaded areas L_3 and L_5 .

If no transition occurs no loss occurs due to timing error.

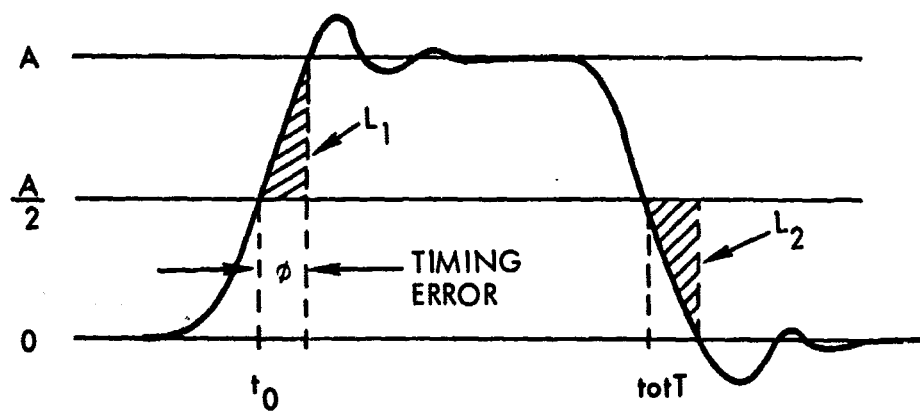
$$L_1 = L_2 = L_3$$

$$L_4 = L_5$$

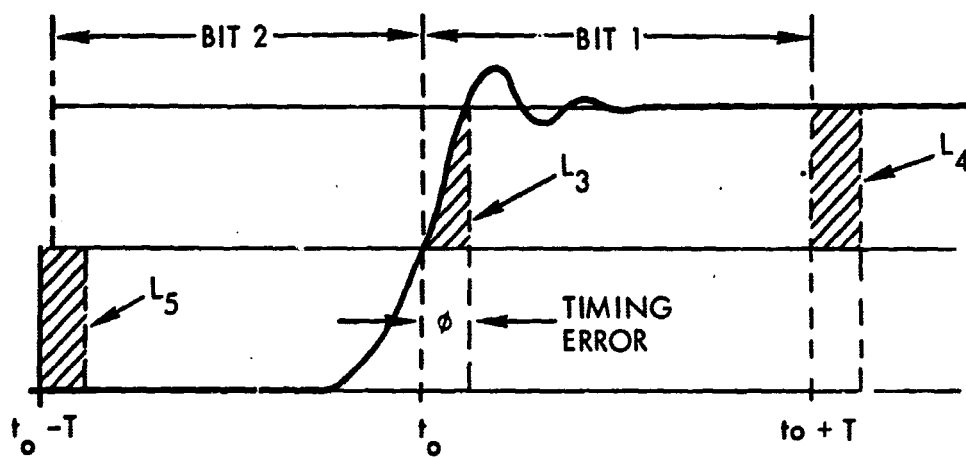
$$L_1 = \int_{X_0}^{X_0+R\theta} E(x) dx - \frac{1}{2} \int_{X_0}^{X_0+R\theta} dx$$

$$L_1 = \int_{X_0}^{X_0+R\theta} E(x) dx - \frac{1}{2} R\theta$$

$$L_4 = \frac{1}{2} \int_0^{R\theta} dx = \frac{1}{2} R\theta$$



(a) ADJACENT TRANSITIONS



(b) SINGLE TRANSITION

Figure C-8 Illustrating Signal Loss due to Timing Error

The losses normalized to the I&D output with no prefiltering are:

$$\overline{L}_1 = \frac{\int_{X_0}^{X_0+R\theta} E(x) dx - \frac{1}{2} R\theta}{\frac{1}{2} R} = \frac{2}{R} \int_{X_0}^{X_0+R\theta} E(x) dx - \theta$$

$$\overline{L}_4 = \frac{\frac{1}{2} R\theta}{\frac{1}{2} R} = \theta$$

Using the printed table of the integral of $E(x)$ as explained in Section 4.0 of this appendix, the loss are read as follows:

$$\overline{L}_1 = \frac{2}{R} \left(I \Big|_{0.66}^{0.66+R\theta} \right) - \theta$$

$$\overline{L}_4 = \theta$$

The signal loss factors due to prefiltering and timing error are the signal loss factors due to the prefilter minus the losses due to timing error. They are as follows:

$$a_1(\theta) = a_1 - 2\overline{L}_1(\theta) = a_1 + 2\theta - \frac{4}{R} \left(I \Big|_{0.66}^{0.66+R\theta} \right)$$

$$a_2(\theta) = a_2 + \overline{L}_4(\theta) - \overline{L}_1(\theta) = a_2 + 2\theta - \frac{2}{R} \left(I \Big|_{0.66}^{0.66+R\theta} \right)$$

$$a_3(\theta) = a_3 - \overline{L}_4(\theta) - \overline{L}_1(\theta) = a_3 - \frac{2}{R} \left(I \Big|_{0.66}^{0.66+R\theta} \right)$$

$$a_4(\theta) = 1$$

The signal loss factors due to timing error with the six pole Butterworth prefilter were read for a range of R from 0.5 to 8.0 and a range of θ from 5% to 20% of a bit period. The loss factors are included in Table 4.4.2.1.

APPENDIX D

ANALYSIS AND BUDGET OF TIMING ERROR FOR THE MSFTP-2 BIT SYNCHRONIZER

1.0 INTRODUCTION AND SUMMARY

The technical information, supplied by NASA, on the MSFTP-2 bit synchronizer has been utilized to calculate and estimate the worst case expected timing errors in the bit synchronizer. The worst case timing errors resulting from this analysis are used in Sections 4 and 5 to calculate the bit synchronizer performance degradation due to timing error.

Six major sources of timing error have been identified. They are listed in Table D-1 along with their corresponding normalized error contributions. An explanation of each error source is given in Paragraph 2 of this appendix.

Table D-2 shows the error contribution of each error source which results from the worst case error magnitudes estimated to exist in the bit synchronizer.

The worst case estimated timing error (shown in Table D-2) is approximately 9% and 10% of a bit period, for transition densities of 100% and 50% respectively.

2.0 TIMING ERROR ANALYSIS

The portion of the MSFTP-2 bit synchronizer which contributes to timing error is shown in Figure D-1. This portion of the bit synchronizer is the clock extraction circuitry which consists of the zero crossing detector and phase lock loop (PLL).

TABLE D-1
TIMING ERROR SOURCES AND ERROR CONTRIBUTIONS

Error Source	Normalized Error Contribution ($\frac{\sigma}{T}$)
Tunable Low Pass Filter	
Static Timing Error	± 0.64 $\frac{\text{Percent of Bit Period}}{\text{Percent Detuning}}$
Dynamic Timing Error	± 5 Percent of Bit Period
Schmitt Trigger	
Hysteresis Delay	-1 Percent of Bit Period
One Half Bit Width One Shot	
Static Timing Error	± 0.5 $\frac{\text{Percent of Bit Period}}{\text{Percent Circuit Timing Error}}$
Dynamic Timing Error	± 0.5 $\frac{\text{Percent of Bit Period}}{\text{Percent Detuning}}$
Phase Lock Loop	
Static Phase Error	
High Loop B.W.	$\frac{0.4}{M}$
Med Loop B.W.	$\frac{1.3}{M}$
Low Loop B.W.	$\frac{3.0}{M}$
	$\left. \begin{array}{l} \frac{0.4}{M} \\ \frac{1.3}{M} \\ \frac{3.0}{M} \end{array} \right\} \begin{array}{l} \text{Percent of Bit Period} \\ \text{Percent Frequency Uncertainty} \end{array}$
	$0 \leq M \leq 1 = \text{Transition Density}$
Jitter Due to Noise	Negligible

TABLE D-2
ERROR SOURCES, ERROR MAGNITUDES, AND TIMING ERROR CONTRIBUTIONS

Error Source	Error Magnitude	Timing Error Contribution $\frac{\theta}{T}$ Percent of Bit Period
Tunable Low Pass Filter		
Static Error	5% Detuning	± 3.2
Dynamic Error	Constant	$+ 5.0$
Schmitt Trigger		
Hysteresis Delay	50 MV Hysteresis	$- 1.0$
One Half Bit Width One Shot		
Static Error	3% RSS Circuit Error	± 1.5
Dynamic Error	1% Detuning	± 0.5
Phase Lock Loop		
Static Phase Error (Medium Loop BW)	1% Frequency } $M = 0.5$ Uncertainty } $M = 1.0$	$+ 2.6$ $+ 1.3$

Worst Case RSS Error $\left(\frac{\theta}{T}\right)$:

$$\frac{\theta}{T} \text{ (for } M = 1) = \left[\sqrt{(3.2)^2 + (1.5)^2 + (0.5)^2} \right] + 5 - 1 + 1.3 = \underline{8.86} \text{ Percent of Bit Period}$$

$$\frac{\theta}{T} \text{ (for } M = 0.5) = \left[\sqrt{(3.2)^2 + (1.5)^2 + (0.5)^2} \right] + 5 - 1 + 2.6 = \underline{10.16} \text{ Percent of Bit Period}$$

Note: The worst case RSS error is the RSS of the contributions which may take either sign plus the contributions which have a fixed sign.

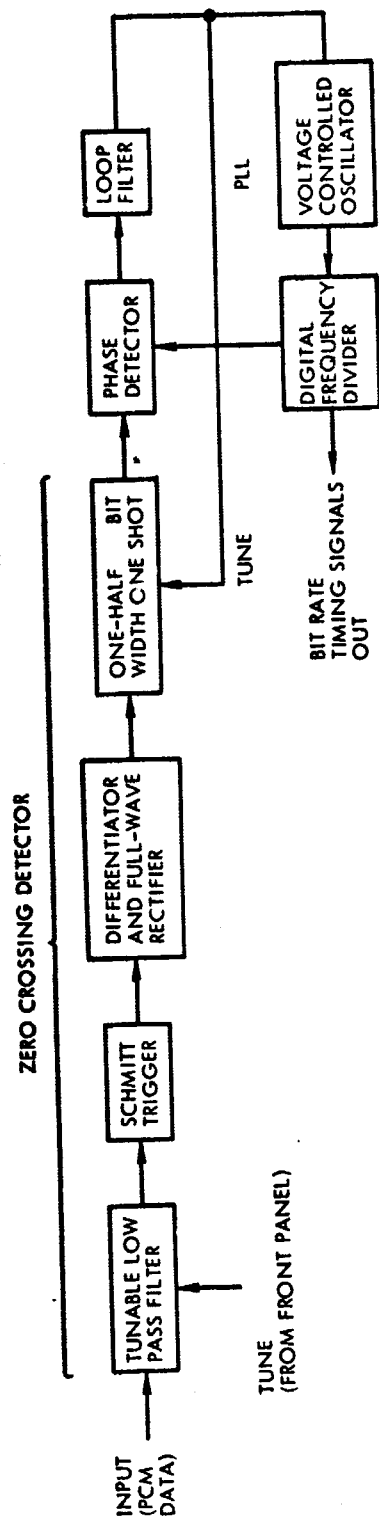


Figure D-1 Clock Extraction Circuitry for the MSFTP-2 Bit Synchronizer

The major timing error contributions are enumerated below by circuit block.

- 1) Tunable low pass filter
 - a) Static timing error
 - b) Dynamic timing error
- 2) Schmitt trigger
 - a) Hysteresis delay
- 3) One half bit width one shot
 - a) Static timing error
 - b) Dynamic timing error
- 4) Phase lock loop
 - a) Static phase error
 - b) Jitter due to noise in the loop

Considering the state-of-the-art in available circuitry, the differentiator and full wave rectifier timing errors are judged to be negligible.

An explanation of each timing error contribution follows.

2.1 TUNABLE LOW PASS FILTER (TLPF)

Static Timing Error - The static timing error due to the TLPF is the phase delay error through the filter due to detuning. If the filter is tuned to exactly one half the bit rate this error contribution is zero.

The static timing error of the TLPF is shown in Appendix E to be:

$$\frac{\theta}{T} = \frac{90^\circ - \tan^{-1} \left[\frac{1.2 \frac{f}{f_0} - 0.2 \left(\frac{f}{f_0} \right)^3}{1 - \left(\frac{f}{f_0} \right)^2} \right]}{180^\circ}$$

For small detuning errors (less than 15%) the static timing is approximately:

$$\frac{\theta}{T} = 0.64 \left(1 - \frac{f}{f_0} \right)$$

Thus the static timing error is 0.64 percent of a bit period per percent frequency detuning or difference between one-half the incoming bit rate and the frequency to which the filter is tuned.

$$\frac{\theta}{T} = \pm 0.64 \frac{\text{Percent of a bit period}}{\text{Percent TLPF detuning}}$$

Dynamic Timing Error - The dynamic timing error due to the TLPF is the phase delay through the filter due to its intersymbol interference and due to the harmonic content of the input PCM data. If the TLPF input is a one-half bit rate sinusoid (heavily perfiltered alternate 1,0 PCM pattern) the dynamic timing error contribution is zero. Harmonics in the PCM data (such as with square wave PCM) and uneven spacing of transitions causes the dynamic timing error.

The dynamic timing error is approximated, using the time response analysis of the TLPF in Appendix E, as follows.

Figure E-6 shows the TLPF output response to a step and to a square pulse one bit period wide. The waveforms are those which would result from a single transition or two adjacent transitions respectively. The point at which the waveforms cross 0.5 amplitude corresponds to the "zero crossing" or the point in time which the zero crossing detector will detect. Ideally the waveform should cross 0.5 amplitude at $\frac{T}{2}$ or one-half bit period.

From the figure it is seen that with a step input the 0.5 amplitude crossing occurs at $0.44T$. The sampling point (T_s) is:

$$T_s = (0.44 + 0.5) T = 0.94T$$

Ideally the sampling point should be (T) thus there is a 6%, of a bit period, timing error.

From the pulse response it is seen that the 0.5 amplitude crossings are $0.44T$ and $1.47T$ yielding errors of 6% and 3% respectively.

The timing errors in the 0.5 amplitude crossings are "averaged" in the phase lock loop such that, assuming 50% pulses and 50% single transitions, the average dynamic timing error is approximated as:

$$\frac{\theta}{T} = \frac{6\% + 6\% + 3\%}{3} = +5\% \text{ of a bit period}$$

Note that these errors "lead" and therefore carry a positive sign.

2.2 SCHMITT TRIGGER (ST)

Hysteresis Delay Timing Error - This error results from failure of the ST to trigger at exactly the zero crossings. Hysteresis in the ST will cause its output to be delayed by the time required for the input to reach the trigger point.

Assuming that the hysteresis is symmetrical, i.e., the upper trigger point is equal to the lower trigger point, and the ST input is 2 volts peak the timing error due to hysteresis is approximately:

$$\frac{\theta}{T} = \frac{1}{\pi} \sin^{-1} \frac{V_{ST(HYST)}}{2}$$

where

$$V_{ST(HYST)} = \text{Hysteresis voltage}$$

The above equation assumes a sinusoidal input to the ST.

For $V_{ST(HYST)} = 10 \text{ MV}$:

$$\frac{\theta}{T} = \frac{1}{\pi} \sin^{-1} \frac{10^{-2}}{2} = 0.16\%$$

For $V_{ST(HYST)} = 100 \text{ MV}$:

$$\frac{\theta}{T} = \frac{1}{\pi} \sin^{-1} \left(\frac{0.1}{2} \right) = -1.6\%$$

Based on the calibration procedure of Reference 3, wherein the hysteresis is set to the minimum value below which noise triggering occurs, it is estimated that the worst case hysteresis voltage is of the order of 50 MV, so that:

$$\frac{\theta}{T} = -1.0\%$$

Note that this error is a delay and therefore carries a negative sign.

2.3 ONE HALF BIT WIDTH ONE SHOT ($\frac{1}{2}$ BWOS)

Static Timing Error - This error is caused by the period of the one shot output not being set to exactly one half the bit period or $\frac{T}{2}$. Ideally the one shot output starts at the zero crossing of the data transition and is $\frac{T}{2}$ wide. The one shot output is compared with the phase lock loop reference frequency in the phase detector and, for the in sync condition, the phase lock loop reference frequency transitions mark the mid point of the one shot output, i.e., the reference frequency transitions (T_R) occur $\frac{T}{4}$ delayed from the data transitions.

$$T_R = \frac{1}{2} \left(\frac{T}{2} \right) = \frac{T}{4}$$

An error (Δ) in the one shot output yields an error in the reference frequency transitions (phase) as follows:

$$\frac{\theta}{T} = \frac{1}{2} [\Delta]$$

Thus the timing error is one-half the one shot static error.

An RSS static one shot error of 3% is assumed to account for component tolerance and calibration accuracy. (The timing capacitors, which are switched as a function of bit rate, are specified as $\pm 10\%$. This tolerance is considered to be the "3 σ " value such that the equivalent component tolerance error is $10\%/3 = 3\%$.) The resulting static timing error is:

$$\frac{\theta}{T} = \frac{1}{2} (0.03) = 0.015 \text{ or } \pm 1.5\%$$

Dynamic Timing Error - This error is caused by imperfect closed loop tuning of the one shot. As seen in Figure D-1, the one shot is tuned by the output of the PLL loop filter. Small changes in input bit rate ($\pm 10\%$) are "tracked" by the PLL and, since the one shot timing capacitors are fixed for small frequency change, the one shot output period is made to "track" the frequency changes via the closed loop tuning. If the closed loop

tuning were not provided, the maximum dynamic timing error would be $\pm 10\%$. Assuming, however, that the closed loop tuning has a worst error of 10%, the resulting tuning error is:

$$\text{tuning error } (0.1)(10\%) = 1\%$$

and the dynamic timing error is:

$$\frac{\phi}{T} = \frac{1}{2} (0.01) = 0.005 = \pm 0.5\%$$

2.4 PHASE LOCK LOOP (PLL)

Static Phase Error - This error arises from the phase error which results in the PLL when the incoming bit rate frequency is not exactly equal to the VCO center frequency. This error is a function of loop gain. Since loop gain of the MSFTP-2 bit synchronizer depends on the transition density and the loop bandwidth setting, the static phase error is a function of transition density and loop bandwidth setting.

The PLL static phase error analysis has been carried out in Appendix F of this report. The error contributions for the three MSFTP-2 loop bandwidth settings (from Page F-27) are:

LOOP BANDWIDTH SETTING	TIMING ERROR $\frac{\phi}{T}$
	$\frac{\text{Percent of a bit period}}{\text{Percent Frequency Uncertainty}}$
High	$\frac{0.4}{M}$
Medium	$\frac{1.3}{M}$
Low	$\frac{3.0}{M}$

where $M = \text{transition density } 0 \leq M \leq 1$

The timing error for the medium loop bandwidth setting (the most commonly used setting) as a function of transition density is tabulated below:

TRANSITION DENSITY (M)	TIMING ERROR $\frac{\sigma}{T}$
	<u>Percent of a Bit Period</u> <u>Percent Frequency Uncertainty</u>
1.0	1.3
0.5	2.6
0.25	5.2
0.10	13

Jitter due to Noise in the PLL - This error contribution results from additive noise at the input to the tunable low pass filter which varies the time of occurrence of the data transitions or zero crossings at the output of the filter.

The error contribution is illustrated pictorially in Figure D-2. Figure D-2a shows the pertinent waveforms of the zero crossing detector and phase lock loop for the noise free case and ideal circuitry. The output of the TLPF is assumed to be sinusoidal (100% transition density). Figure D-2b shows waveforms for the noisy case. It is seen that the zero crossings of the $\frac{1}{2}$ BWOS contain jitter or timing error. A modified amount of this jitter is transferred to the PLL bit rate output depending on the jitter spectrum and the PLL noise bandwidth.

A noise analysis of the zero crossing detector is included in the following paragraphs from which it is seen that the timing error (jitter) contribution due to additive gaussian noise is negligible for SNR in the range of 9.8 db to 13.5 db. It is noted that the major timing error contribution in the tunable low pass filter is its dynamic or intersymbol "jitter" while noise induced jitter is very small.

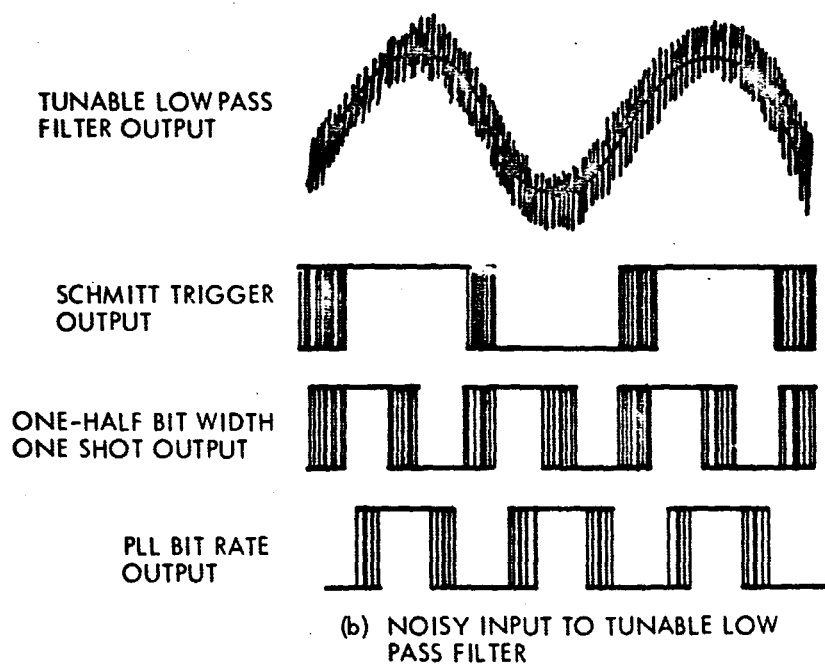
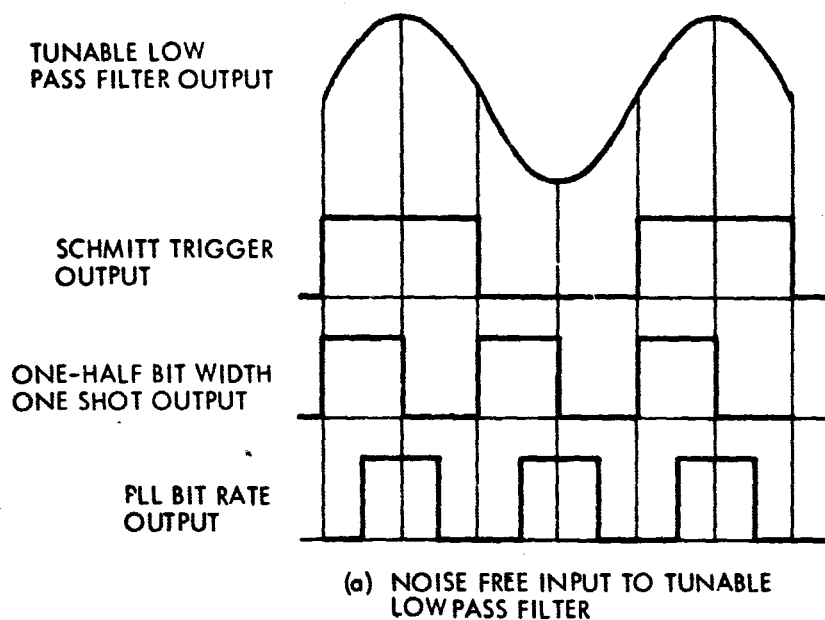


Figure D-2 Illustrating Jitter due to Noise in the Phase Lock Loop

2.5 NOISE ANALYSIS OF ZERO CROSSING DETECTOR

The sinusoidal output of the tunable low pass filter, $e_v(t)$, of Figure D-2 has a slope at the zero crossings as follows:

$$e_v(t) = \sin \omega_c t$$

where:

$$\omega_c = 2\pi f_c$$

$$f_c = \text{cut off frequency of TLPF} = \frac{f_B}{2}$$

$$f_B = \text{bit rate} = \frac{1}{T}$$

$$\omega_c = \frac{\pi}{T}$$

$$\left. \frac{d e_v(t)}{dt} \right|_{t=0} = \omega_c \cos \omega_c t \Big|_{t=0}$$

$$\left. \frac{d e_v(t)}{dt} \right|_{t=0} = \omega_c = \frac{\pi}{T} \text{ slope at zero crossings}$$

The amplitude of noise voltage (e_N) necessary to cause a timing error shift (time shift of zero crossings) of T_1 is:

$$e_N = \frac{\pi}{T} t \Big|_t = T_1$$

$$e_N = \pi \left(\frac{T_1}{T} \right)$$

Assuming white Gaussian noise out of the TLPPF, the probability that the magnitude of the noise is equal to or greater than the value required to cause a timing error shift of (T_1) is determined from the Gaussian probability density function as follows:

$$P \left[|e_N| \geq \frac{\pi T_1}{T} \right] = 2 \int_{\frac{\pi T_1}{T}}^{\infty} \frac{1}{\sqrt{2\pi} \sigma} e^{-\frac{e_N^2}{2\sigma_x^2}} de_N$$

Making a change of variable let

$$x^2 = \frac{e_N^2}{2\sigma_x^2}, \quad x = \frac{e_N}{\sqrt{2}\sigma_x}, \quad dx = \frac{1}{\sqrt{2}\sigma_x} de_N$$

where:

$$e_N = \frac{\pi T_1}{T}, \quad x = \frac{\pi T_1}{T\sqrt{2}\sigma_x}$$

$$e_N = \infty, \quad x = \infty$$

Now:

$$P\left[|e_N| \geq \frac{\pi T_1}{T}\right] = 2 \int_{\frac{\pi T_1}{T\sqrt{2}\sigma_x}}^{\infty} \frac{1}{\sqrt{2\pi}\sigma_x} e^{-\frac{x^2}{2\sigma_x^2}} dx$$

$$P\left[|e_N| \geq \frac{\pi T_1}{T}\right] = \frac{2}{\sqrt{\pi}} \int_{\frac{\pi T_1}{T\sqrt{2}\sigma_x}}^{\infty} e^{-x^2} dx$$

$$P\left[|e_N| \geq \frac{\pi T_1}{T}\right] = 1 - H\left(\frac{\pi T_1}{T\sqrt{2}\sigma_x}\right)$$

where:

$$H(x) = \frac{2}{\sqrt{\pi}} \int_0^x e^{-\alpha^2} d\alpha$$

It is observed that it is necessary to know the standard deviation of the noise σ_x in order to evaluate the probability of having a timing error larger than some certain value. The standard deviation is determined as follows:

The variance of a random variable, x , is defined as

$$\sigma_x^2 = E\left\{\left[x - \bar{x}\right]^2\right\}$$

But the noise is zero mean $E[x] = \bar{x} = 0$ so that

$$\sigma^2 = E[x^2]$$

The autocorrelation of a wide sense stationary random variable, $[R_x(\tau)]$, is defined as:

$$R_x(\tau) = E \left\{ [x(t)] [x(t + \tau)] \right\}$$

and if $\tau = 0$

$$R_x(0) = E[x^2]$$

The autocorrelation $R_x(\tau)$ and spectral density $S_x(f)$ are Fourier transforms of each other,

$$R_x(\tau) = \int_{-\infty}^{\infty} S_x(f) e^{-j\omega\tau} d\tau$$

For white noise

$$S_x(f) = \frac{N_0}{2} \quad (\text{two sided})$$

Therefore

$$R_x(0) = \frac{N_0}{2}$$

so that

$$\sigma_x^2 = E[x^2] = R_x(0) = \frac{N_0}{2}$$

$$\sigma_x = \sqrt{\frac{N_0}{2}}$$

Therefore the standard deviation, σ_x , can be determined from the noise spectral density, $\frac{N_0}{2}$. The noise spectral density is determined as follows:

Assume that the worst case post detection SNR is 9.8 db (which corresponds to a theoretical bit error rate of 10^{-3}). Assume also that the MSFTP-2 predetection bandwidth is of the order of three times the bit rate. The predetection SNR is then:

$$\text{SNR} = 9.8 - 10 \log \frac{3}{0.5} = 2 \text{ db}$$

$$\frac{S}{N} = 2 \text{ db}$$

$$N = S - 2 \text{ db}$$

The nominal signal amplitude is 2 volts peak such that, referred to one volt, the signal power is 6 db.

$$N = 6 \text{ db} - 2 \text{ db} = 4 \text{ db}$$

but

$$N = \frac{N_0}{2} \text{ BW}$$

where:

$$\text{BW} = 3 \text{ Bit Rate} = 3(51.2 \text{ KB}) = 153.6 \text{ KHz}$$

$$\frac{N_0}{2} = 4 \text{ db} - (\text{BW}) \text{ db}$$

$$\frac{N_0}{2} = 4 \text{ db} - 10 \log (1.536 \times 10^5)$$

$$\frac{N_0}{2} = -47.7 \text{ db}$$

$$\frac{N_0}{2} = 5.96 \times 10^{-5}$$

$$\text{But } \sigma_x^2 = \frac{N_0}{2} = 5.96 \times 10^{-5}$$

$$\text{therefore } \sigma_x = 7.7 \times 10^{-3}$$

Again, the probability that the noise has a magnitude equal to or greater than that necessary to cause a timing error shift (T_1) is:

$$P \left[|e_N| \geq \pi \frac{T_1}{T} \right] = P \left[T_E \geq T_1 \right] = 1 - H \left(\frac{\pi}{\sqrt{2} \sigma_x} \frac{T_1}{T} \right)$$

T_E = noise induced timing error

$$\sigma_x = 7.7 \times 10^{-3}$$

$$P \left[T_E \geq T \right] = 1 - H \left(288 \frac{T_1}{T} \right)$$

Timing error of less than or equal to 0.5 percent of a bit period ($\frac{T_1}{T} \leq 0.005$) will degrade performance by less than 0.1 db. This is shown in the curves of performance degradation versus timing error (Figures 4.5.17 through 4.5.57) of Section 4.0.

The probability of the timing error exceeding 0.5% of a bit period is:

$$P\left|T_E \geq 0.05 T\right| = 1 - H\left|288(0.005)\right|$$

$$= 1 - H(1.44)$$

$$= 1 - 0.97914^*$$

$$P\left|T_E \geq 0.005 T\right| = 0.0208$$

Thus the probability that noise induced timing error will be as great as 0.005 T, with corresponding performance degradation of 0.1 db, is approximately 2%. Therefore errors due to noise induced jitter are neglected.

*U.S. Department of Commerce, National Bureau of Standards, Applied Mathematics Series #41, "Tables of the Error Function and Its Derivative".

APPENDIX E

ANALYSIS OF THE MSFTP-2 BIT SYNCHRONIZER TUNABLE LOW PASS FILTER

1.0 INTRODUCTION AND SUMMARY

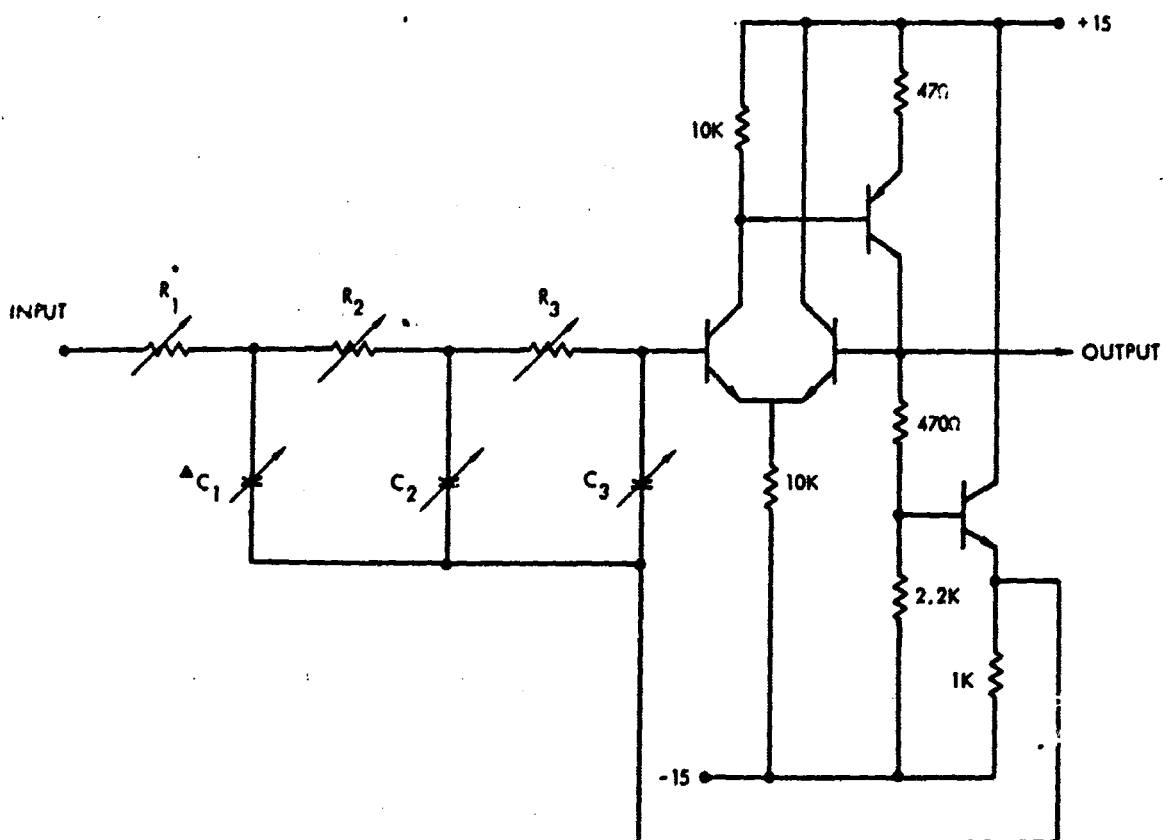
The MSFTP-2 bit synchronizer tunable low pass filter provides the filtering in the filter and sample detector and the filtering for the clock extraction (timing) loop. The accuracy of this filter, whose cut-off frequency is programmable over a range of frequencies of 0.5 Hz to 500 KHz, is critical to the operation of the bit synchronizer.

In this appendix, the following analysis on the filter is carried out:

- 1) Filter transfer function
- 2) Filter effective noise bandwidth - for use in the F&S detector analysis
- 3) Filter phase response and static timing error - for use in timing error analysis
- 4) Filter frequency response (attenuation versus detuning) - for use in DC error analysis
- 5) Filter time response to PCM data - for use in filter and sample detector analysis and in dynamic timing error analysis.

2.0 TUNABLE LOW PASS FILTER TRANSFER FUNCTION

The tunable low pass filter is shown in simplified schematic form in Figure E-1. The filter is capable of having its cut off frequency tuned to correspond to one-half the bit rate over the operating range of bit rates from 1 BPS to 1 MBPS. This is accomplished by changing R and C as a function of bit rate. Capacitors (C) are switched in by relay networks under front panel control. The variable resistors (R) are FET transistors which are voltage programmed via a digital to analog converter under front panel control.



- * VARIABLE R_s ARE VOLTAGE CONTROLLED FET TRANSISTORS
- ▲ CAPACITORS ARE SWITCHED IN BY RELAY NETWORKS AS BIT RATE IS CHANGED BY FRONT PANEL CONTROL

Figure E-1 Tunable Low Pass Filter Schematic

The nominal values of R_1 through R_3 and C_1 through C_3 are equal:

$$R_1 = R_2 = R_3 = R$$

$$C_1 = C_2 = C_3 = C$$

The feedback ratio (from Figure E1) is:

$$K = \frac{2.2}{2.2 + 0.47} \quad (\text{gain of emitter follower})$$

$$K = \frac{2.2}{2.67} \quad (.97) = 0.8$$

Referring to Figure E-2:

$$Z_3 = \frac{1}{sC} \quad (R_3 \text{ open circuit})$$

$$\frac{V_3}{V_2} = \frac{Z_3}{Z_3 + R} = \frac{\frac{1}{sC}}{\frac{1}{sC} + R} = \frac{1}{1 + sCR}$$

$$Z_2 = \frac{(Z_3 + R) \frac{1}{sC}}{Z_3 + R + \frac{1}{sC}} = \frac{1 + sCR}{s^2 C^2 R + 2sC} \quad (R_2 \text{ open circuit})$$

$$\frac{V_2}{V_1} = \frac{Z_2}{Z_2 + R} = \frac{1 + sCR}{s^2 C^2 R^2 + 3sCR + 1}$$

$$Z_1 = \frac{(Z_2 + R) \frac{1}{sC}}{Z_2 + R + \frac{1}{sC}} = \frac{s^2 C^2 R^2 + 3sCR + 1}{s^3 C^3 R^2 + 4s^2 C^2 R + 3sC} \quad (R_1 \text{ open})$$

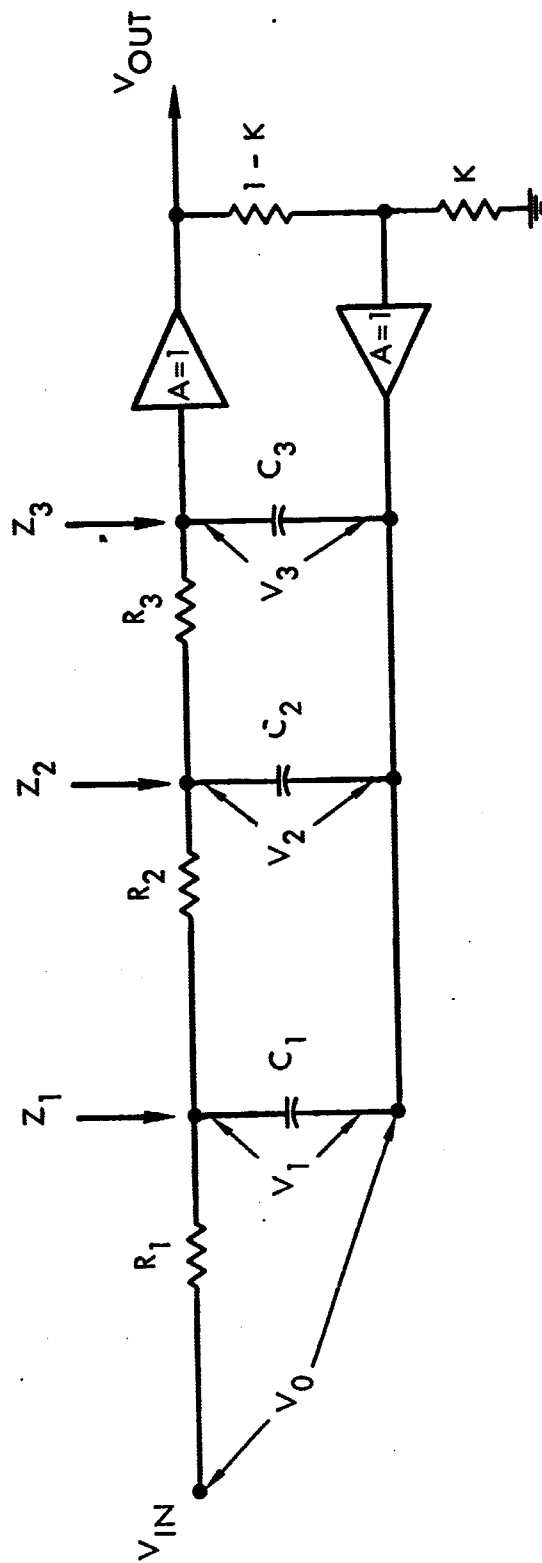


Figure E-2 Equivalent Circuit Tunable Low Pass Filter

$$\frac{V_1}{V_0} = \frac{Z_1}{Z_1 + R} = \frac{S^2 C^2 R^2 + 3SCR + 1}{S^3 C^3 R^3 + 5S^2 C^2 R^2 + 6SCR + 1}$$

$$\frac{V_3}{V_0} = \frac{V_3}{V_2} \frac{V_2}{V_1} \frac{V_1}{V_0} = \frac{1}{S^3 C^3 R^3 + 5S^2 C^2 R^2 + 6SCR + 1}$$

$$RC = T$$

$$\frac{V_3}{V_0} = \frac{1}{S^3 T^3 + 5S^2 T^2 + 6ST + 1} = \frac{1}{D}$$

$$V_3 = (1 - K) V_{out}$$

$$V_{IN} - V_0 - K V_{out} = 0$$

$$V_0 = V_{IN} - K V_{out}$$

$$\frac{V_3}{V_0} = \frac{(1 - K) V_{out}}{V_{IN} - K V_{out}} = \frac{1}{D}$$

$$(1 - K) V_{out} = \frac{1}{D} (V_{IN} - K V_{out}) = \frac{1}{D} V_{IN} - \frac{1}{D} K V_{out}$$

$$V_{out} (1 - K + \frac{K}{D}) = \frac{1}{D} V_{IN}$$

$$\frac{V_{out}}{V_{IN}} = \frac{\frac{1}{D}}{(1 - K + \frac{1}{D} K)} = \frac{1}{(1 - K) D + K}$$

$$\frac{V_{out}}{V_{IN}} = \frac{\frac{1}{1 - K}}{D + \frac{K}{1 - K}}$$

$$\frac{V_{out}}{V_{IN}} = \frac{\frac{1}{1-K}}{S^3T^3 + 5S^2T^2 + 6ST + 1 + \frac{K}{1-K}}$$

$$1 + \frac{K}{1-K} = \frac{1}{1-K}$$

$$\frac{V_{out}}{V_{IN}} = \frac{\frac{1}{1-K}}{S^3T^3 + 5S^2T^2 + 5ST + \frac{1}{1-K}}$$

$$K = 0.8$$

$$\frac{V_{out}}{V_{IN}} = \frac{5}{S^3T^3 + 5S^2T^2 + 6ST + 5} = H(S)$$

$$H(S) = \frac{\frac{5}{T^3}}{S^3 + \frac{5}{T}S^2 + \frac{6}{T^2}S + \frac{5}{T^3}}$$

$$H(j\omega) = \frac{\frac{5}{T^3}}{-j\omega^3 - \frac{5}{T}\omega^2 + j\frac{6}{T^2}\omega + \frac{5}{T^3}}$$

$$H(j\omega) = \frac{\frac{5}{T^3}}{\left(\frac{5}{T^3} - \frac{5}{T}\omega^2\right) + j\left(\frac{6}{T^2}\omega - \omega^3\right)}$$

$$H(j\omega) = \frac{1}{(1 - T^2\omega^2) + j\left(\frac{6}{5}T\omega - \frac{1}{5}T^3\omega^3\right)}$$

$$H(j\omega) = \frac{1}{[1 - (\omega T)^2] + j[1.2 \omega T - 0.2 (\omega T)^3]}$$

The phase shift through the filter at a frequency of one-half the bit rate is required to be one-half bit period (or 90°) for proper sampling.

$$\text{at } 90^\circ \text{ phase shift: } 1 - (\omega T)^2 = 0$$

$$(\omega T)^2 = 1$$

$$2\pi f T = 1$$

$$f_0 = \frac{1}{2\pi T} = \frac{1}{2} \text{ bit rate}$$

$$T = \frac{1}{2\pi f_0}$$

$$H(j\omega) = \frac{1}{[1 - (2\pi f T)^2] + j[1.2(2\pi f T) - 0.2(2\pi f T)^3]}$$

$$H(j\omega) = \frac{1}{\left[1 - \left(\frac{f}{f_0}\right)^2\right] + j\left[1.2 \frac{f}{f_0} - 0.2 \left(\frac{f}{f_0}\right)^3\right]}$$

$$\frac{f}{f_0} = \alpha$$

The response magnitude is:

$$\text{MAG} = \frac{1}{\left[(1 - \alpha^2)^2 + (1.2\alpha - 0.2\alpha^3)^2\right]^{1/2}}$$

The phase response is:

$$\text{Phase} = \tan^{-1} \left[\frac{1.2\alpha - 0.2\alpha^3}{1 - \alpha^2} \right]$$

$$\text{Log Mag} = -20 \log \left[(1 - \alpha^2)^2 + (1.2\alpha - 0.2\alpha^3)^2 \right]^{1/2}$$

The log magnitude is plotted in Figure E-3.

3.0 TUNABLE LOW PASS FILTER EFFECTIVE NOISE BANDWIDTH

The effective noise bandwidth of the tunable low pass filter, compared to the effective noise bandwidth of the I&D filter, is required in the analysis of the filter and sample (F&S) bit detector.

The effective noise bandwidth compared to the effective noise bandwidth of the I&D filter is:

$$B_o = \frac{\int_0^\infty |\text{MAG}|^2 df}{|\text{MAG}|^2 \text{ of I\&D Filter}}$$

$$|\text{MAG}|^2 \text{ of I\&D Filter} = 1$$

$$B_o = \int_0^\infty |\text{MAG}|^2 df$$

The square of the magnitude of the TLPF was integrated numerically on the computer, yielding:

$$B_o = 1.57 f_o$$

Since f_o = one-half bit rate

$$B_o = 0.785 \text{ Bit Rate}$$

Note that the TLPF noise bandwidth is 57% wider than the I&D noise bandwidth.

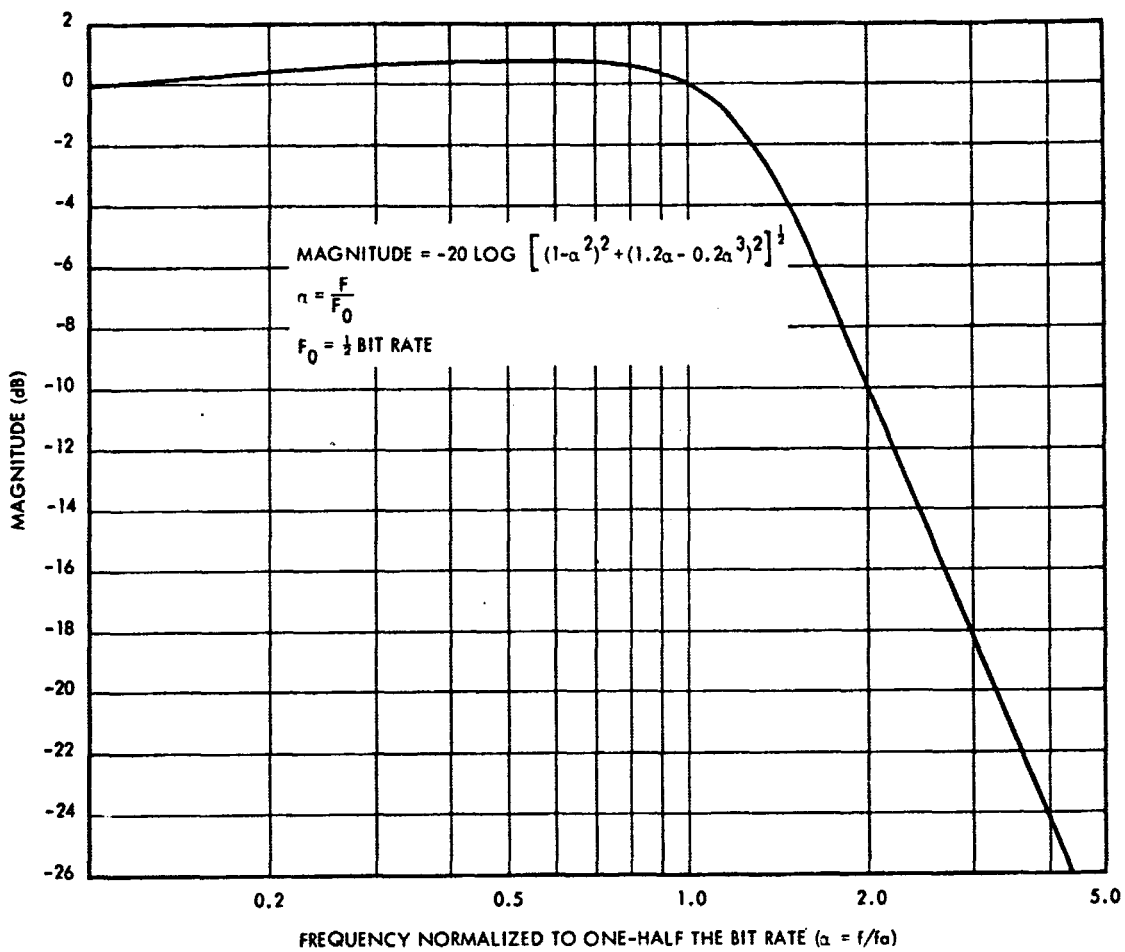


Figure E-3 Tunable Low Pass Filter Frequency Response

4.0 TUNABLE LOW PASS FILTER STATIC TIMING ERROR

For zero static phase error the filter must be tuned to exactly one-half the operating bit rate. Detuning will result in a static phase error in timing signals supplied to the integrate and dump and filter and sample detectors.

The filter delay when tuned to f_0 or, one-half the bit rate, is 90° or one-half the bit period.

$$\text{Delay at } f_0 = 90^\circ = \frac{T}{2}$$

$$T = \text{bit period}$$

$$\text{Phase delay } \phi = \tan^{-1} \frac{[1.2\alpha - 0.2\alpha^3]}{[1 - \alpha^2]}$$

$$\alpha = \frac{f}{f_0}$$

$$\Delta\phi = 90^\circ - \phi$$

$$\text{Static Timing Error } \left(\frac{\Theta}{T} \right) = \frac{\Delta\phi}{180^\circ}$$

$$\frac{\theta}{T} = \frac{90^\circ - \tan^{-1} \frac{\left[1.2 \frac{f}{f_0} - 0.2 \left(\frac{f}{f_0} \right)^3 \right]}{\left[1 - \left(\frac{f}{f_0} \right)^2 \right]}}{180^\circ}$$

Timing error $\frac{\theta}{T}$ versus filter detuning is shown in Figure E-4.

5.0 TUNABLE LOW PASS FILTER ATTENUATION VERSUS TUNING

The change in filter attenuation for small change in filter tuning is:

$$\Delta \text{attenuation} = \Delta \text{MAG} = 1 - \text{MAG}$$

$$\Delta \text{MAG} = 1 - \frac{1}{\left[(1 - \alpha^2)^2 + (1.2\alpha - 0.2\alpha^2)^2 \right]^{1/2}}$$

$$\alpha = \frac{f}{f_0}$$

Change in filter attenuation versus filter detuning is shown in Figure E-5.

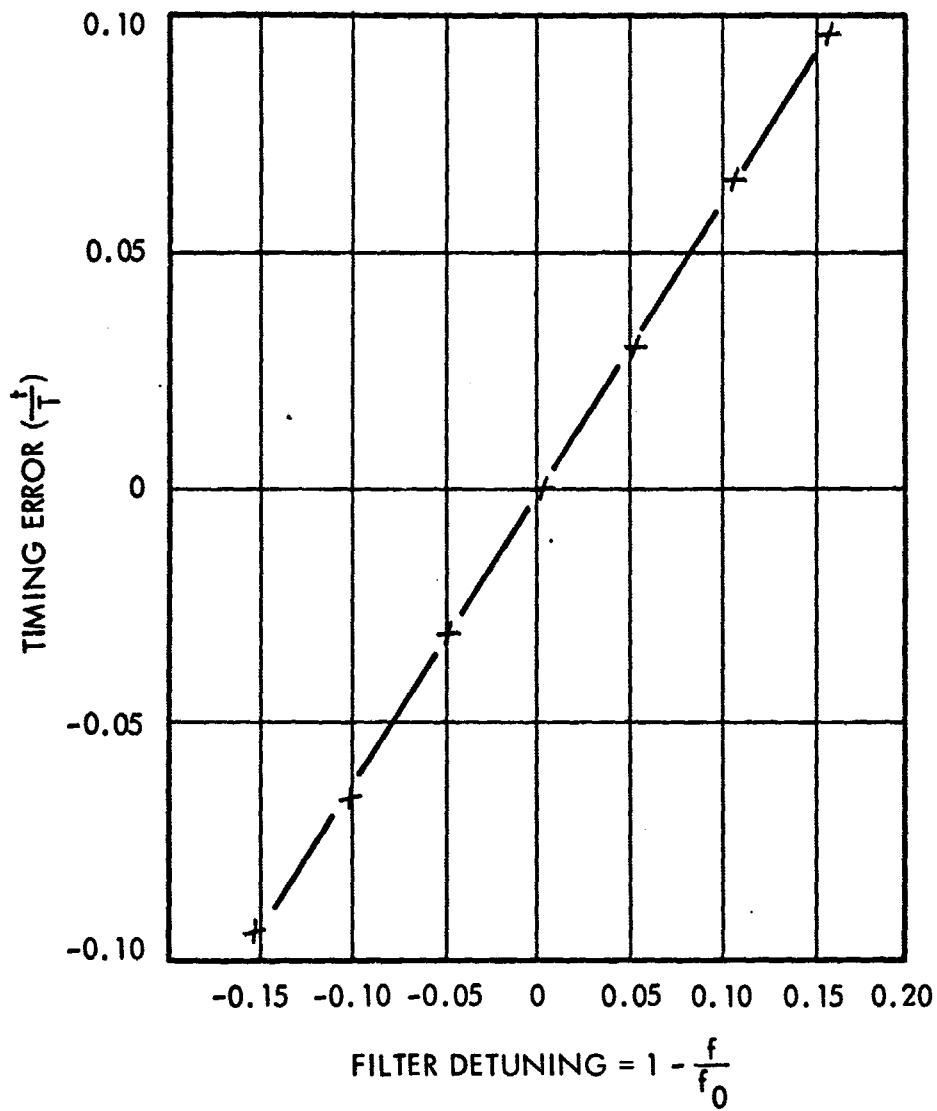


Figure E-4 Timing Error Versus Tunable Low Pass Filter Detuning

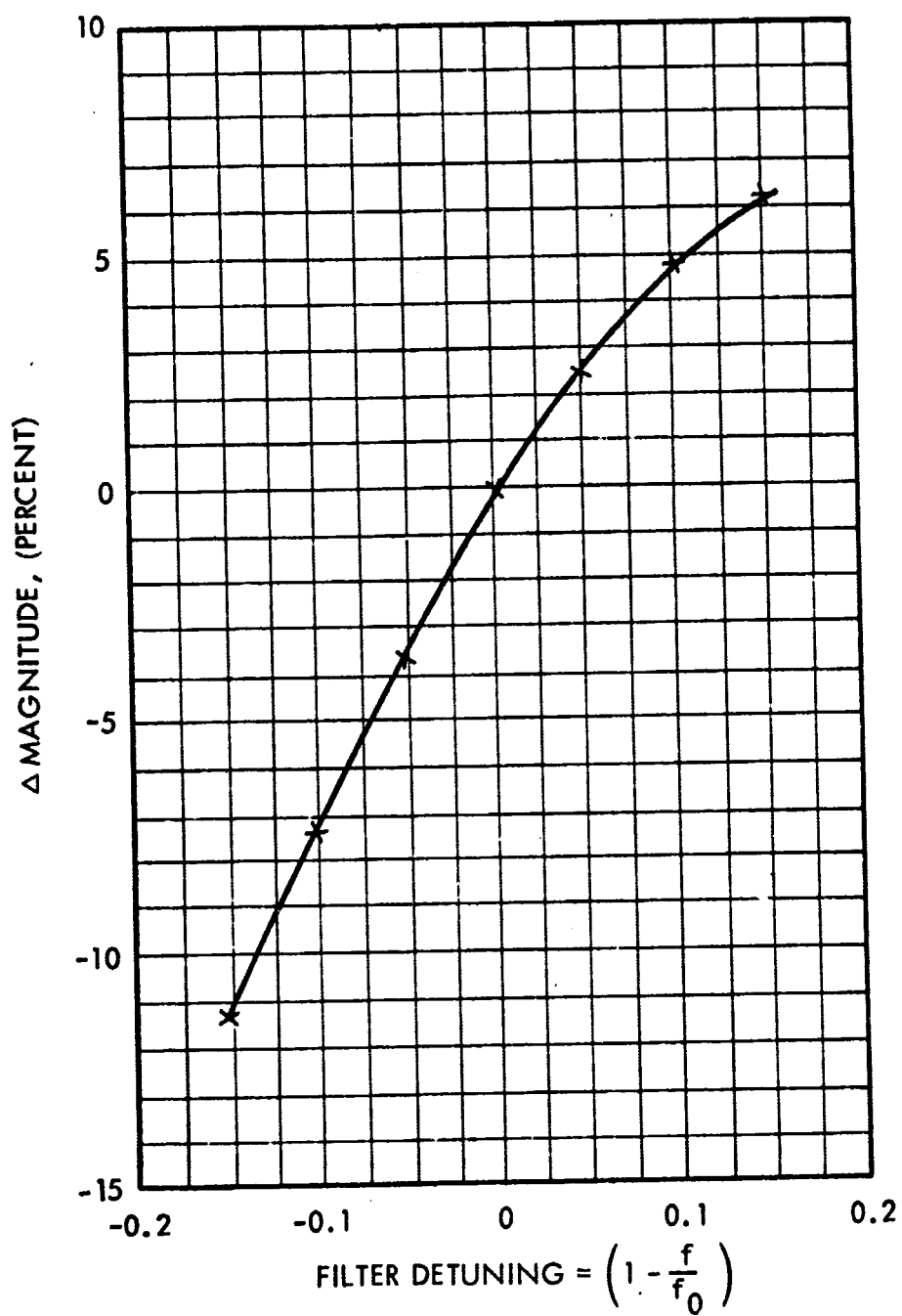


Figure E-5 Tunable Low Pass Filter Attenuation Versus Detuning

6.0 TUNABLE LOW PASS FILTER TIME RESPONSE TO PCM DATA

The transfer function of the tunable low pass filter (from Section 2.0) is:

$$H(S) = \frac{\frac{5}{T^3}}{S^3 + \frac{5}{T} S^2 + \frac{6}{T^2} S + \frac{5}{T^3}}$$

Let $T = 1$

$$H(S) = \frac{5}{S^3 + 5S^2 + 6S + 5}$$

$$H(S) = \frac{5}{(S + 3.76)(S^2 + 1.24S + 1.33)}$$

$$H(S) = \frac{5}{(S + 3.76) \left[(S + 0.62)^2 + 0.971 \right]}$$

The response to a unit step $\left(\frac{1}{S}\right)$ is:

$$E_0(S) = \frac{1}{S} H(S)$$

$$E_0(S) = \frac{5}{S(S + 3.76) \left[(S + 0.62)^2 + 0.946 \right]}$$

which is of the form

$$E_o(s) = \frac{5}{s(s+b)((s+a)^2 + \omega^2)}$$

$$a = 0.62$$

$$b = 3.76$$

$$\omega = 0.971$$

From Laplace transform tables, the time response is:

$$e_o(t) = K_0 + K_1 e^{-bt} + K_2 e^{-at} \sin(\omega t + \phi)$$

where

$$K_0 = \frac{1}{b(a^2 + \omega^2)}$$

$$K_1 = -\frac{1}{b[(a-b)^2 + \omega^2]}$$

$$K_2 = -\frac{1}{\omega \sqrt{(a^2 + \omega^2)[(a-b)^2 + \omega^2]}}$$

$$\phi = \tan^{-1}\left(\frac{\omega}{a}\right) + \tan^{-1}\left(\frac{\omega}{a-b}\right)$$

$$\omega = 2\pi f_c$$

$$R = \frac{f_c}{f_B} = 0.5$$

$$f_B = \frac{1}{T}$$

$$f_c = R \frac{1}{T}$$

$$\omega = \pi \frac{1}{T}$$

$$e_o(t) = K_0 + K_1 e^{-bt} + K_2 e^{-at} \sin\left(\pi \frac{t}{T} + \phi\right)$$

The pulse response, $e_{op}(t)$, is obtained by adding the response to a negative step at $t = T$ to the step response:

$$e_{op}(t) = e_o(t) - e_o(t - T)$$

The equations for the step and pulse response of the TLPF were programmed and a print out of the output as a function of time $\left(\frac{t}{T}\right)$ obtained. Figure E-6 is a plot of the TLPF output step and pulse response.

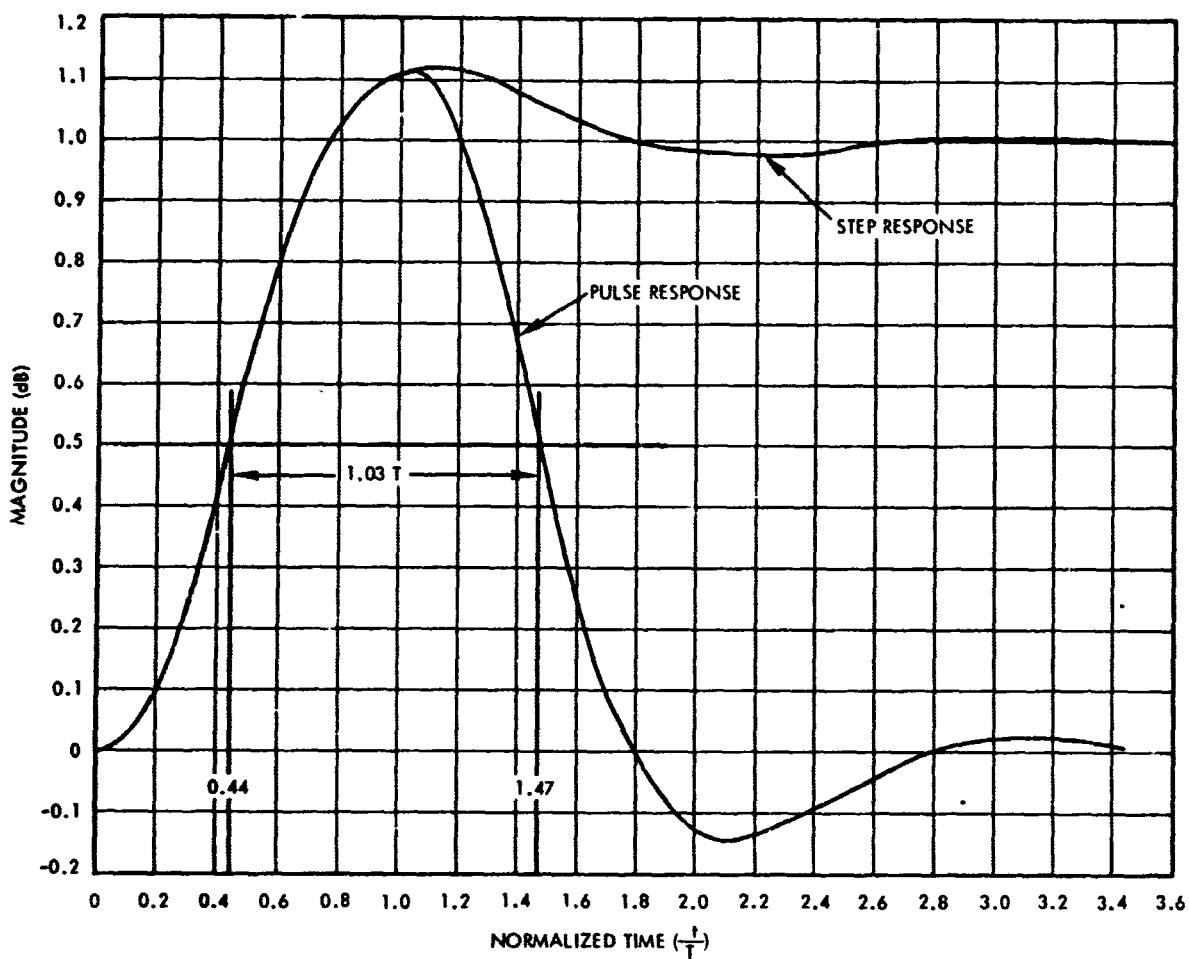


Figure E-6 Tunable Low Pass Filter Step and Pulse Response

APPENDIX F

ANALYSIS OF THE MSFTP-2 BIT SYNCHRONIZER PHASE LOCK LOOP

1.0 INTRODUCTION AND SUMMARY

The analysis presented in this appendix was undertaken in order to determine the effective noise bandwidth and static phase error in the MSFTP-2 phase lock loop (PLL). The noise bandwidth is required to determine the noise induced jitter. Both noise induced jitter and static phase error are timing errors which affect the I&D and F&S detectors.

No reference to the design values of the PLL loop bandwidth as a function of bit rate could be found in the MSFTP-2 bit synchronizer technical information. Therefore, the detailed PLL circuit configuration was determined from the schematic diagrams and a small signal analysis conducted to determine the loop bandwidth, loop noise bandwidth, and static phase error.

It was found that the loop noise bandwidth is approximately 5%, 1%, and 0.5% of bit rate for the high, medium, and low loop bandwidth settings respectively.

The static phase error was found to be $\frac{0.4}{M}$, $\frac{1.3}{M}$, and $\frac{3.0}{M}$ percent of a bit period per percent frequency uncertainty; for the high, medium and low loop bandwidth setting respectively. Where (M) is the transition density.

2.0 PHASE LOCK LOOP CONFIGURATION

The simplified schematic diagram of the phase lock loop (PLL) is shown in Figure F-1. It consists of phase detector, loop filter, isolation amplifier, and VCO and digital frequency divider. The input signal (D) to the PLL is derived from the one-half bit width one shot and is a one-half bit width pulse occurring at data transitions (no pulse occurs in the absence of transitions).

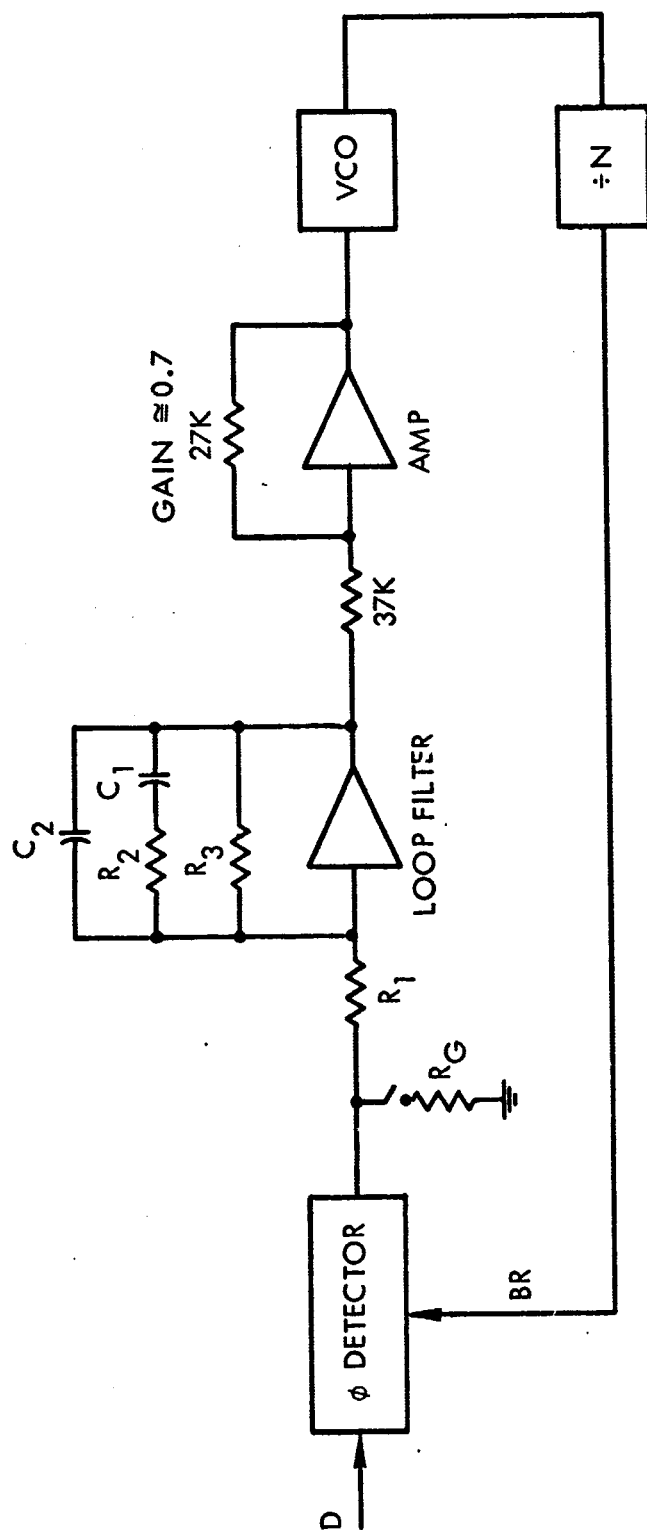


Figure F-1 Phase Lock Loop Block Diagram

2.1 PHASE DETECTOR

The phase detector circuit is shown in simplified form in Figure F-2. The phase detector gain can be changed by switching a resistor (R_G) from the phase detector output to ground (R_G is located in the loop filter) depending on the desired loop bandwidth. Three loop bandwidths are provided (Hi, Med, and Low). For the loop bandwidths R_G is open, 2.2 K, or 820 Ω , respectively. The voltage equivalent circuit for the phase detector with each value of R_G is shown in Figure F-3.

The time waveform (phase detector out) of the phase detector is shown in Figure F-4 for the condition of synchronism. It will be noted that there is no output from the phase detector when an input (D) is positive or when there are no data transitions. It will also be noted that the phase detector is "digital" in that it does not preserve the amplitude of the input signal. The output is a bipolar clipped signal whose duty cycle is a linear function of the phase angle between D and BR.

The phase detector characteristic is shown in Figure F-5. The output $\bar{e}_\phi$ is the average voltage of the phase detector as a function of the relative phase (ϕ) of D and BR.

The gain of the phase detector (K_d) is the slope of its characteristic (Figure F-5).

$$K_d = \left(\frac{1}{2}\right) M \frac{2A}{\pi} = M \frac{A}{\pi} \frac{V}{\text{Rad}}$$

A = peak voltage output

The factor of $\frac{1}{2}$ and M come from the lack of phase detector output for one-half the bit period and when transitions do not occur, respectively.

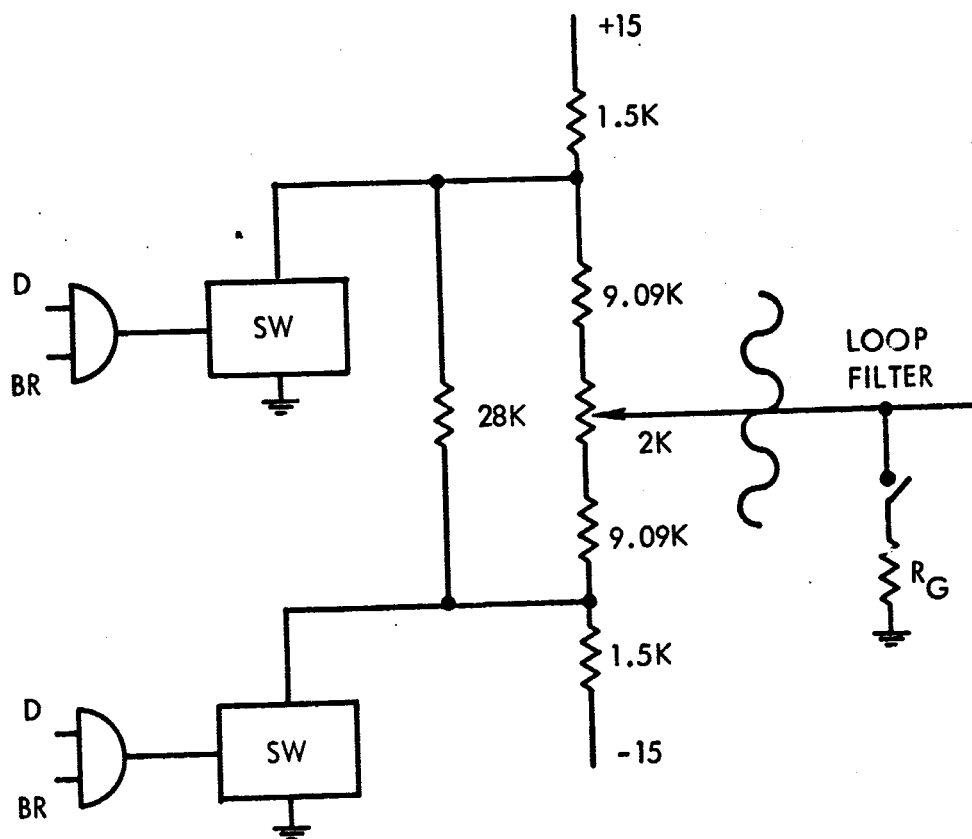


Figure F-2 Simplified Circuit of Phase Detector

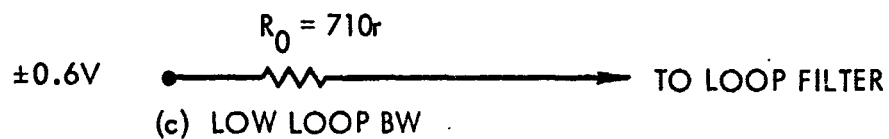
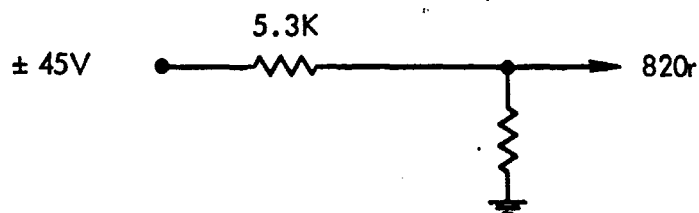
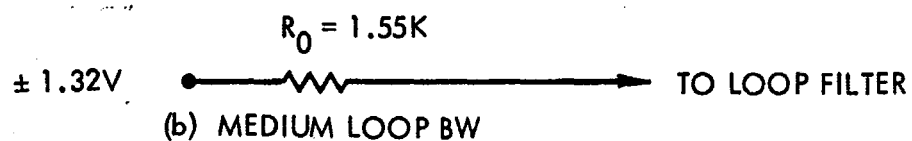
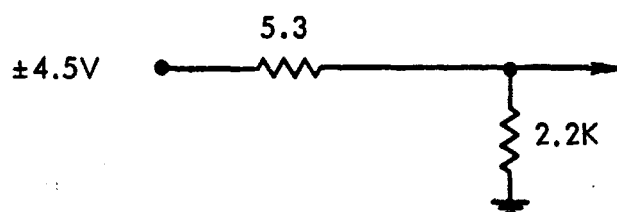
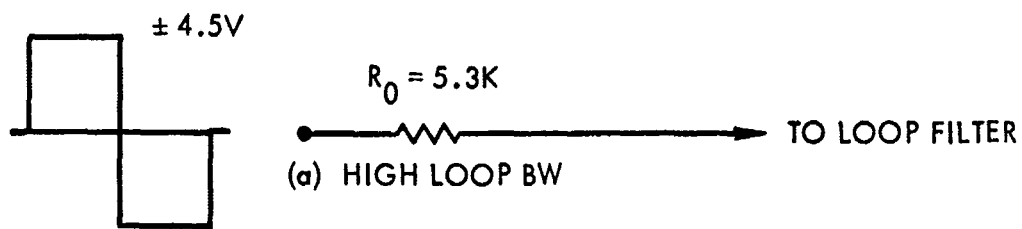


Figure F-3 Voltage Equivalent Circuit of Phase Detector

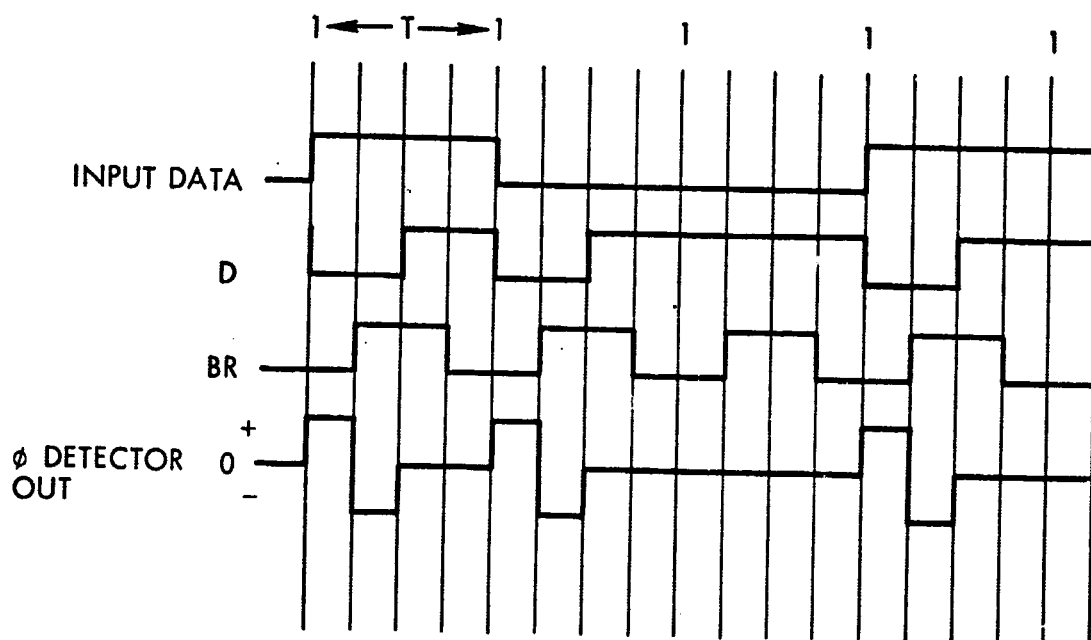


Figure F-4 Phase Detector Waveforms

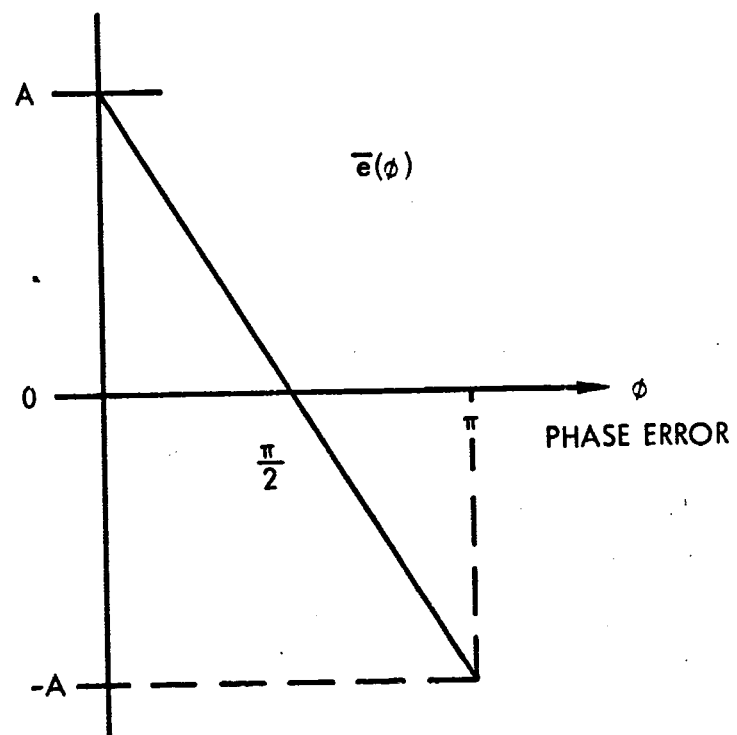


Figure F-5 Phase Detector Characteristic

The phase detector gain for each of the loop bandwidth settings are:

Loop BW	$K_d \left(\frac{V}{\text{Rad}} \right)$
Hi	$M \frac{4.5}{\pi}$
Med	$M \frac{1.32}{\pi}$
Low	$M \frac{0.6}{\pi}$

2.2 LOOP FILTER

The loop filter is shown in schematic form in Figure F-6.

The circuit constants of the filter are switched as a function of bit rate by front panel controlled relays as shown.

The filter contains 6 values of R_1 and R_3 . Based on the schematic these values of R_1 and R_3 are switched to cover the 6 decades of bit rate frequency from 1 BPS to 1 MBPS. There are 24 combinations of R_2C_1 , or four (4) combinations per decade. There are two sets of R_2C_1 , one for hi loop bandwidth, the other for low and medium loop bandwidth.

A truth table showing relay positions versus bit rate range is shown in Figure F-7. The truth table was drawn from Figure F-6. The Applo bit rates of 51.2 KB and 1.6 KB are in decades 5 and 4 respectively and correspond to positions 19 and 13.

Figure F-8 shows the filter constant for 51.2 KB for the three loop bandwidths.

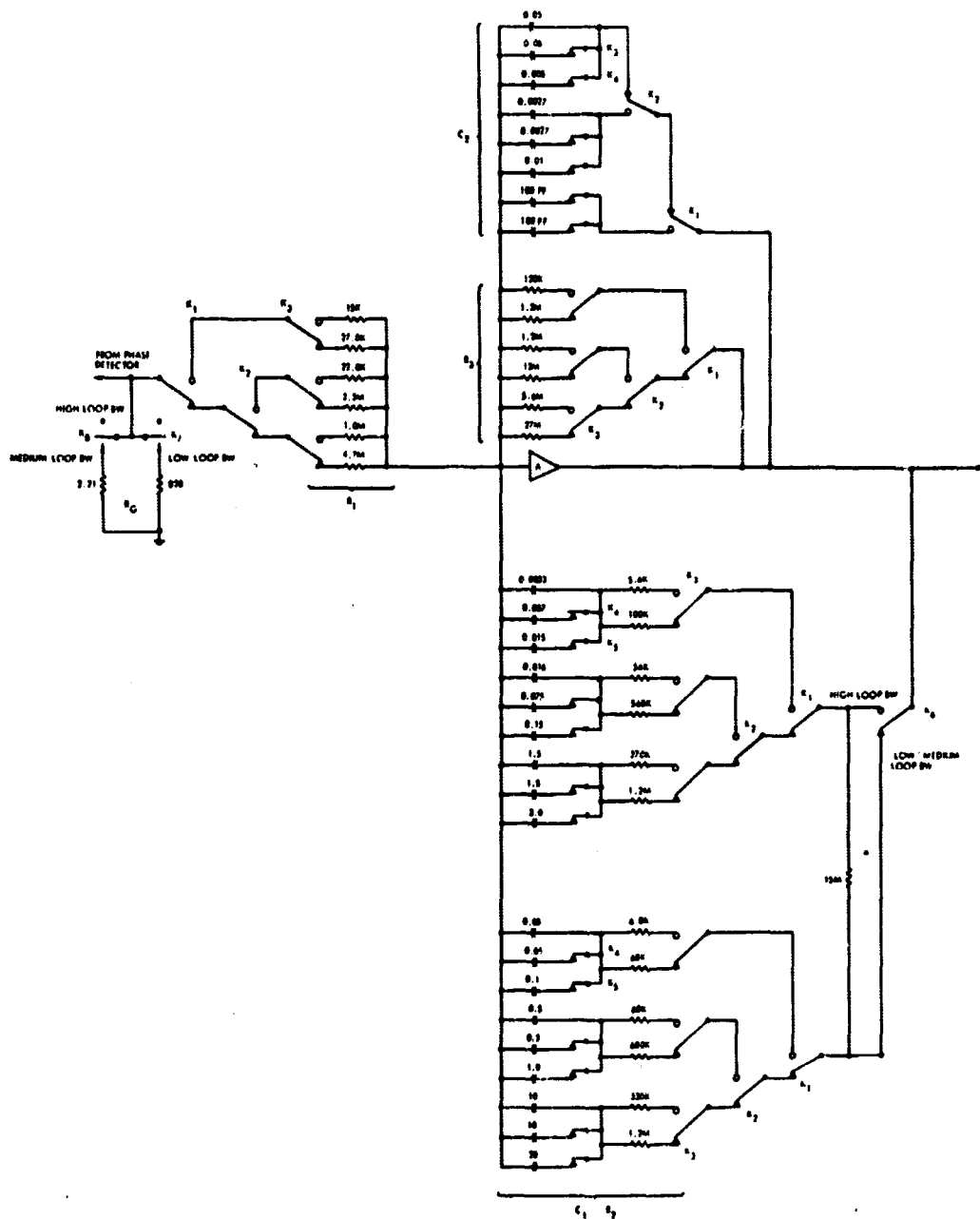


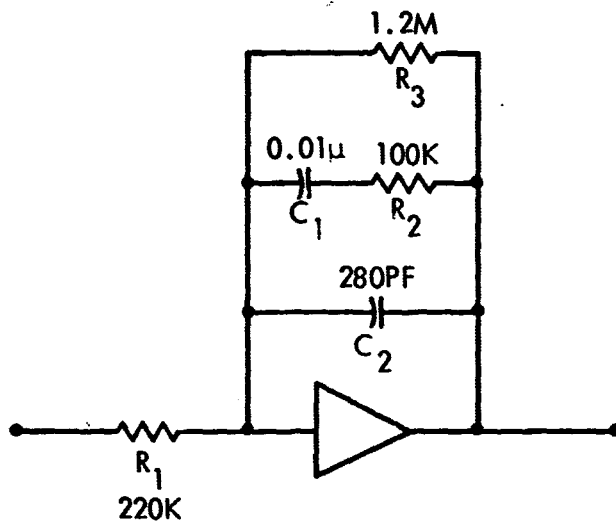
Figure F-6 MSFTP-2 Bit Synchronizer Loop Filter

TRUTH TABLE
LOOP FILTER PARAMETER SWITCHING

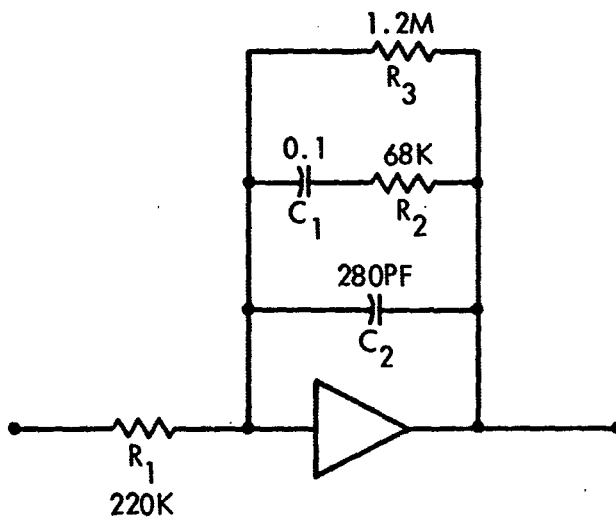
Position	Relay					Bit Range Range		Decade
	K ₁	K ₂	K ₃	K ₄	K ₅			
1	X	X	X	X	X	1 BPS	2 BPS	1
2	X	X	X	0	X	2	4	
3	X	X	X	X	0	4	8	
4	X	X	X	0	0	8 BPS	10 BPS	
5	X	X	0	X	X	10 BPS	20 BPS	2
6	X	X	0	0	X	20	40	
7	X	X	0	X	0	40	80	
8	X	X	0	0	0	80 BPS	100 BPS	
9	X	0	X	X	X	100 BPS	200 BPS	3
10	X	0	X	0	X	200	400	
11	X	0	X	X	0	400	800	
12	X	0	X	0	0	800 BPS	1000 BPS	
13	X	0	0	X	X	1 KB	2 KB	4
14	X	0	0	0	X	2	4	
15	X	0	0	X	0	4	8	
16	X	0	0	0	0	8 KB	10 KB	
17	0	0	X	X	X	10 KB	20 KB	5
18	0	0	X	0	X	20	40	
19	0	0	X	X	0	40	80	
20	0	0	X	0	0	80 KB	100 KB	
21	0	0	0	X	X	100 KB	200 KB	6
22	0	0	0	0	X	200	400	
23	0	0	0	X	0	400	800 KB	
24	0	0	0	0	0	800 KB	1.0 MB	

Loop BW	K ₆	K ₇	K ₈
Hi	0	0	0
Med	X	0	X
Low	X	X	0

X Relay Closed
0 Relay Open



(a) HIGH LOOP BW



(b) MEDIUM AND LOW LOOP BW

Figure F-8 Loop Filter Constants for 51.2 KB

2.2.1 Loop Filter Transfer Function

Assuming a high gain operational amplifier:

$$F(S) = \frac{V_o}{V_i} = \frac{Z_F(S)}{R_1} \quad Z_F = \text{Feedback impedance}$$

Z^1 = feedback impedance with C_2 open

$$Z^1 = \frac{\left(R_2 + \frac{1}{SC_1}\right) R_3}{R_2 + R_3 + \frac{1}{SC_1}} = \frac{R_3 + R_2 R_3 SC_1}{1 + (R_2 + R_3) SC_1}$$

$$Z_F = \frac{Z^1 \frac{1}{SC_2}}{Z^1 + \frac{1}{SC_2}} = \frac{R_3 + R_2 R_3 SC_1}{1 + (R_2 + R_3) SC_1 + SC_2 [R_3 + R_2 R_3 SC_1]}$$

$$Z_F = \frac{R_3 + R_2 R_3 C_1 S}{S^2 C_1 R_2 C_2 R_3 + S(C_1 R_2 + C_1 R_3 + C_2 R_3) + 1}$$

$$C_1 R_2 = \tau_1$$

$$C_1 R_3 = \tau_2$$

$$C_2 R_3 = \tau_3$$

$$F(S) = \left(\frac{R_3}{R_1}\right) \frac{1 + \tau_1 S}{S^2 \tau_1 \tau_3 + S(\tau_1 + \tau_2 + \tau_3) + 1}$$

$$\frac{R_3}{R_1} = K_F = \text{DC gain of the filter}$$

The filter time constants at 51.2 KB for the different loop bandwidth are as follows:

Loop BW	τ_1 Sec	τ_2 Sec	τ_3 Sec	$\tau_1\tau_3$ Sec ²	$\tau_1+\tau_2+\tau_3$ Sec
High	1×10^{-3}	0.012	0.34×10^{-3}	0.34×10^{-6}	13.34×10^{-3}
Low & Med	6.8×10^{-3}	0.12	0.34×10^{-3}	2.31×10^{-6}	127×10^{-3}

Hi Loop BW

$$F(S) = K_F \frac{1 + 1 \times 10^{-3} (S)}{S^2(0.34 \times 10^{-6}) + S(13.3 \times 10^{-3}) + 1}$$

Low Loop BW

$$F(S) = \frac{K_F(1 + 6.8 \times 10^{-3} S)}{S^2(2.31 \times 10^{-6}) + S(127 \times 10^{-3}) + 1}$$

Hi Loop BW

$$F(S) = K_F \frac{(S + 1 \times 10^3)}{(S + 0.294 \times 10^3)(S + 38.8 \times 10^3)}$$

$$F(j\omega) = K_F \frac{(j\omega + 1 \times 10^3)}{(j\omega + 0.294 \times 10^3)(j\omega + 38.8 \times 10^3)}$$

Low Loop BW

$$F(S) = K_F \frac{(S + .147 \times 10^3)}{(S + .011 \times 10^3)(S + 55 \times 10^3)}$$

$$F(j\omega) = K_F \frac{(j\omega + 0.147 \times 10^3)}{(j\omega + 0.11 \times 10^3)(j\omega + 55 \times 10^3)}$$

The response of the loop filter with constants set for 51.2 KB Hi Loop BW is shown in Figure F-9. The response for Medium and Low Loop BW is shown in Figure F-10. Since the third break point is substantially higher than the next closest (>10) the filter transfer function can be simplified by assuming $\tau_3 = 0$.

Then:

$$F(S) = K_F \left(\frac{\tau_1 S + 1}{S(\tau_1 + \tau_2) + 1} \right) \quad \text{loop filter transfer function}$$

2.3 VCO DRIVE AMPLIFIER

The drive amplifier gain is approximately 0.7

$$K_A = 0.7$$

2.4 VCO AND DIVIDER

The VCO frequency shift range is 1.6 MHz to 4.0 MHz. It is followed by a binary counter which is programmed to divide the VCO center frequency (f_0) down to the bit rate:

$$BR = \frac{f_0}{N} = \frac{f_0}{2^n} \quad n = \text{number of stages in the binary counter}$$

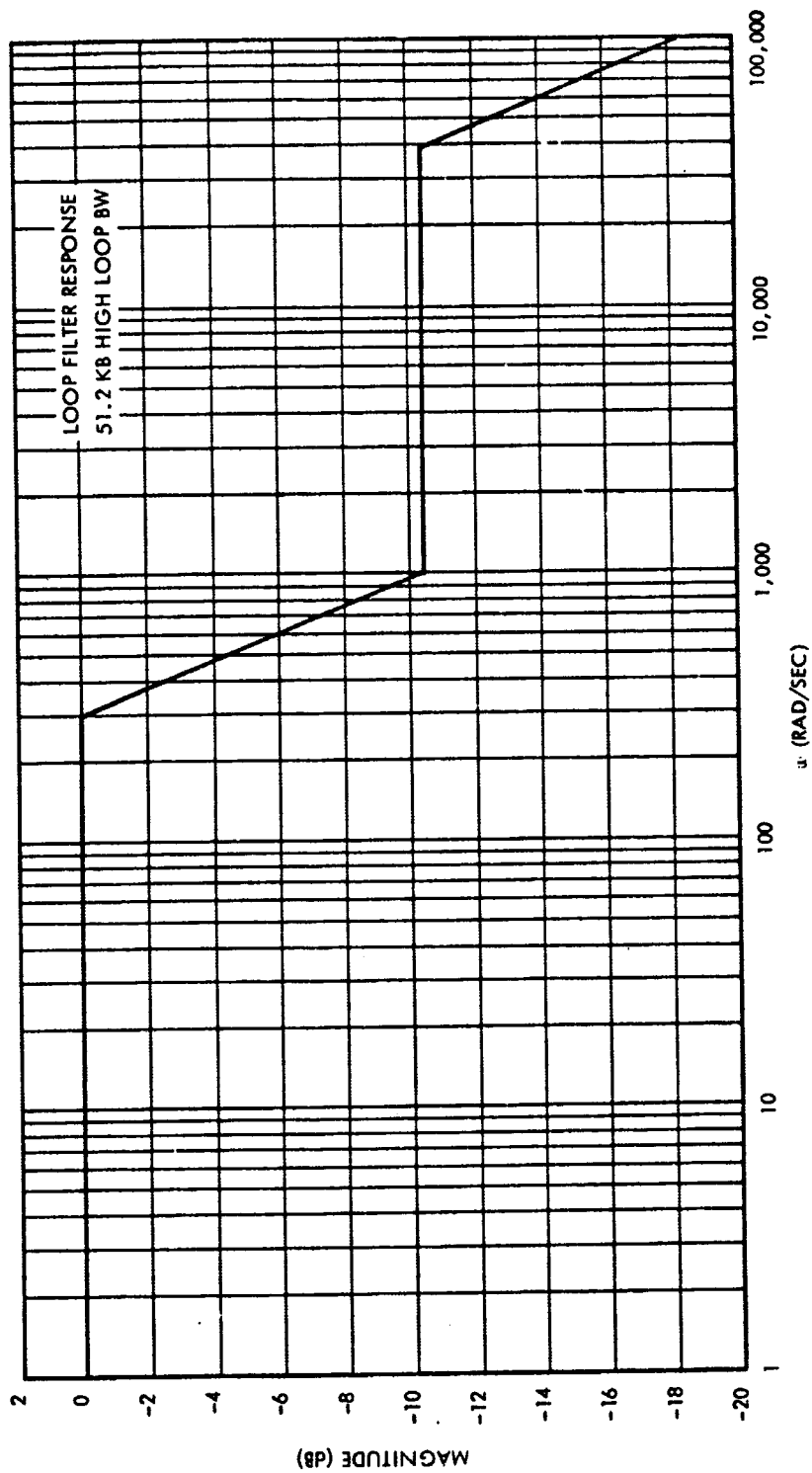


Figure F-9 PLL Loop Filter Frequency Response

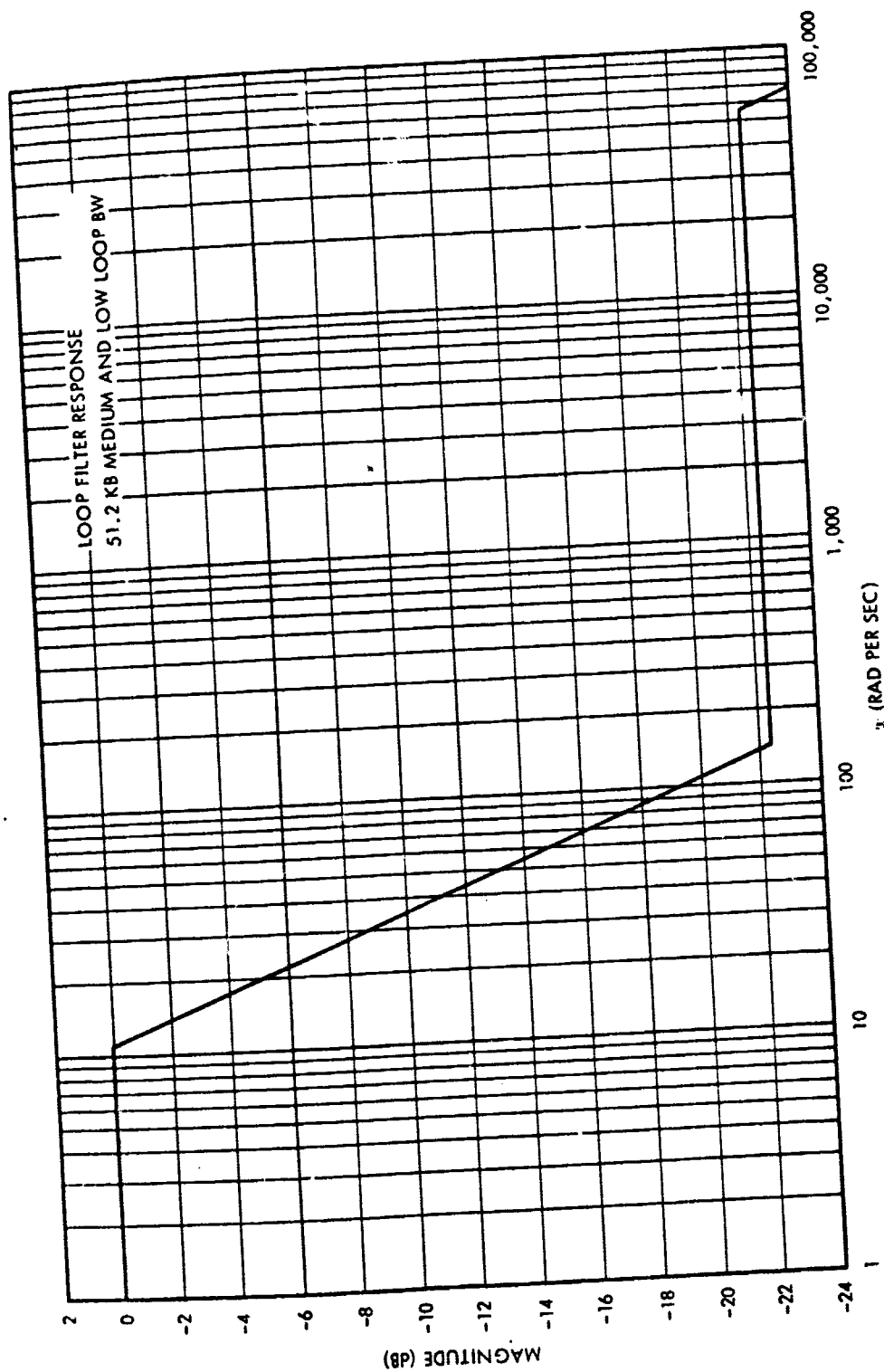


Figure F-10 PLL Loop Filter Frequency Response

When operating at 51.2 KB, $N = 64$ and $f_o = 3.2768$ MHz

$$BR = 51.2 \text{ KB} = \frac{3.2768 \text{ MHz}}{64}$$

The frequency control voltage to the VCO is approximately $\pm 10\text{V}$. So the VCO transfer function is

$$\frac{K_{VCO}}{S} = \frac{(4.0 - 1.6) \text{ MHz}}{S N (10 \text{ volts})} = \frac{240}{S N} \frac{\text{KHz}}{\text{volt}}$$

$$K_{VCO} = \frac{240}{(64)} = 3.7 \frac{\text{KHz}}{\text{volt}}$$

Let $(K_{VCO})(K_A) = K_o$ to combine the amplifier, VCO, and divider.

Then

$$\frac{K_o}{S} = 0.7 \frac{(3.7)}{S} = \frac{2.6}{S} \frac{\text{KHz}}{\text{volt}} = \frac{16,300}{S} \frac{\text{Rad}}{\text{Sec-Volt}}$$

3.0 PLL SMALL SIGNAL ANALYSIS

The PLL equivalent block diagram and transfer functions is shown in Figure F-11.

The open loop transfer function is:

$$G(S) = K_d K_F \left(\frac{\tau_1 S + 1}{S(\tau_1 + \tau_2) + 1} \right) \frac{K_o}{S}$$

$$G(S) = K_T \left[\frac{\tau_1 S + 1}{S^2(\tau_1 + \tau_2) + S} \right]$$

$$K_T = K_d K_F K_o$$

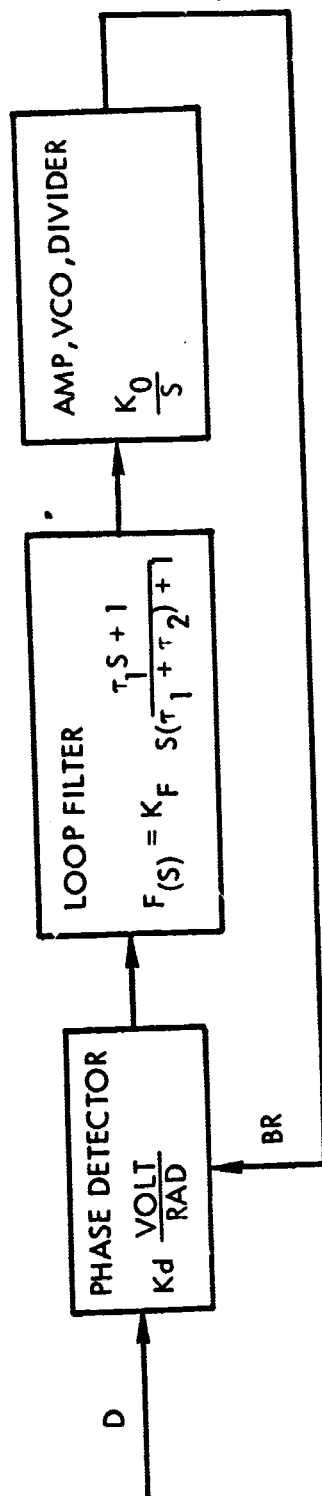


Figure F-11 Equivalent Block Diagram and Transfer Functions of Phase Lock Loop

The closed loop transfer function is:

$$H(S) = \frac{G(S)}{1 + G(S) B(S)} \quad E(S) = 1$$

$$H(S) = \frac{K_T(\tau_1 S + 1)}{S^2(\tau_1 + \tau_2) + S(K_T\tau_1 + 1) + K_T}$$

$$H(S) = \frac{\frac{K_T}{\tau_1 + \tau_2} (\tau_1 S + 1)}{S^2 + S \left(\frac{K_T\tau_1 + 1}{\tau_1 + \tau_2} \right) + \frac{K_T}{\tau_1 + \tau_2}}$$

The characteristic equation of $H(S)$ is of the form:

$$S^2 + 2 \xi \omega_n S + \omega_n^2$$

where:

$$\omega_n = \sqrt{\frac{K_T}{\tau_1 + \tau_2}} \quad \text{natural resonant frequency}$$

$$2 \xi \omega_n = \frac{K_T\tau_1 + 1}{\tau_1 + \tau_2}$$

$$\xi = \frac{1}{2} \left(\frac{K_T\tau_1 + 1}{\tau_1 + \tau_2} \right) \sqrt{\frac{\tau_1 + \tau_2}{K_T}} \quad \text{damping ratio}$$

$$\xi = \frac{1}{2} \left(\frac{K_T}{\tau_1 + \tau_2} \right)^{1/2} \left(\tau_1 + \frac{1}{K_T} \right) = \frac{\omega_n}{2} \left(\tau_1 + \frac{1}{K_T} \right)$$

$$H(S) = \frac{\omega_n^2 (\tau_1 S + 1)}{S^2 + 2 \xi \omega_n S + \omega_n^2}$$

$$H(j\omega) = \frac{\omega_n^2 (1 + j\omega\tau_1)}{-\omega^2 + j\omega \omega_n 2 \xi + \omega_n^2}$$

$$\tau_1 = \frac{2 \xi}{\omega_n} - \frac{1}{K_T}$$

$$H(j\omega) = \frac{\omega_n^2 \left[1 + j \frac{\omega}{\omega_n} \left(2 \xi - \frac{\omega_n}{K_T} \right) \right]}{\omega_n^2 - \omega^2 + j \omega \omega_n 2 \xi}$$

$$H(j\omega) = \frac{1 + j \frac{\omega}{\omega_n} \left(2 \xi - \frac{\omega_n}{K_T} \right)}{\left(1 - \frac{\omega^2}{\omega_n^2} \right) + \left(j \frac{\omega}{\omega_n} 2 \xi \right)}$$

$$MAG = \left\{ \frac{1 + \left[\frac{\omega}{\omega_n} \left(2 \xi - \frac{\omega_n}{K_T} \right) \right]^2}{\left(1 - \frac{\omega^2}{\omega_n^2} \right)^2 + \left(2 \xi \frac{\omega}{\omega_n} \right)^2} \right\}^{1/2}$$

3.1 EFFECTIVE NOISE BANDWIDTH (B_N)

$$B_N = \frac{\int_0^{\infty} |MAG|^2 dF}{|MAG|^2_{MAX}}$$

It is assumed that the noise bandwidth is approximately equal to:

$$B_N = 2\pi F_n \text{ Hz}$$

$$F_n = \frac{\omega_n}{2\pi} = \text{natural resonant frequency (Hz)}$$

The above expression is true for the critically damped, high gain second order loop.

Tables F-1 and F-2 are tabulations of pertinent data calculated for the PLL. Table F-1 shows the time constants and gain constants for the bit rate ranges which include the Apollo rates. Table F-2 shows the natural resonant frequency (ω_n) and damping ratio (ξ) for the two bit rate ranges.

Table F-2 also shows the loop noise bandwidth as a percentage of bit rate for the Apollo rates. It is seen that the noise bandwidth is approximately 5%, 1%, and 0.5% of bit rate for Hi, Med, and Low bandwidth settings, respectively.

TABLE F-1
TABULATION OF PERTINENT DATA CALCULATED FOR THE PHASE LOCK LOOP

Bit Rate Range	Loop BW	τ_1 (Sec)	τ_2 (Sec)	K_d $\frac{V}{\text{Rad}}$	K_F $\frac{V}{V}$	K_O $\frac{\text{Rad}}{\text{Sec} \cdot V}$	K_T $\frac{1}{\text{Sec}}$	$\tau_1 + \tau_2$ (Sec)	$\frac{1}{K_T}$ Sec
40 KBPS to 80 KBPS	High	1×10^{-3}	0.012	1.43(M)	5.45	16,300	127,000(M)	.013	$\frac{.785}{M} \times 10^{-5}$
	Med	6.8×10^{-3}	0.12	0.42(M)	5.45	16,300	37,400(M)	.127	$\frac{0.268}{M} \times 10^{-4}$
	Low	6.8×10^{-3}	0.12	0.191(M)	5.45	16,300	17,000(M)	.127	$\frac{.588}{M} \times 10^{-4}$
1 KBPS to 2 KBPS	High	13.5×10^{-3}	0.289	1.43(M)	5.45	510	3,970(M)	.302	$\frac{.252}{M} \times 10^{-3}$
	Med	136×10^{-3}	2.4	0.42(M)	5.45	510	1,160(M)	2.54	$\frac{0.86}{M} \times 10^{-3}$
	Low	136×10^{-3}	2.4	0.191(M)	5.45	510	530(M)	2.54	$\frac{.189}{M} \times 10^{-2}$

TABLE F-2
TABULATION OF PERTINENT DATA CALCULATED FOR THE PHASE LOCK LOOP

Bit Rate Range	Loop BW	M = 1.0		M = 0.5		
		$\frac{\text{Rad}}{\omega_n \text{ Sec}}$	ξ	$\frac{\text{Rad}}{\omega_n \text{ Sec}}$	ξ	$\frac{B_n}{\text{Bit Rate}}$
40 KB to 80 KB	High	3120	1.56	2200	1.1	4.3%
	Med	540	1.85	382	1.31	0.75%
	Low	365	1.25	258	0.88	0.5%
1 KB to 2 KB	High	114	0.785	81	0.55	5.05%
	Med	21.4	1.46	15.2	1.03	0.95%
	Low	14.5	0.99	10.3	0.7	0.64%

$$\omega_n = \sqrt{\frac{K_T}{\tau_1 + \tau_2}}$$

$$\xi = \frac{\omega_n}{2} \left(\tau_1 + \frac{1}{K_T} \right)$$

$$B_n = \omega_n (\text{Hz})$$

4.0 STATIC PHASE ERROR OF PLL

The phase error which results from a frequency difference between the incoming bit rate and the static (center frequency) of the VCO is given by:

$$\theta_o^* = \frac{\Delta\omega}{K_T}$$

where

$\Delta\omega$ = frequency difference

K_T = loop gain of PLL ($\frac{1}{\text{sec}}$)

$\Delta\omega = 2\pi \Delta f_B$ Rad/sec

$$\theta_o = \frac{2\pi \Delta f_B}{K_T} \text{ rad}$$

T = bit period = 2π rad

$$\frac{\theta_o}{T} = \frac{\Delta f_B}{K_T}$$

The above expression is the phase error normalized to the bit period and is the static phase error as a fraction of the bit period.

Static phase error calculations for the Apollo bit rates, at each of the three loop bandwidth settings, and for two transition densities are tabulated in Table F-3. The data in Table F-3 for transition densities of 0.5 and 1.0 is plotted in Figure F-12.

*Floyd M. Gardner, "Phaselock Techniques", p. 29.

TABLE F-3
CALCULATION OF STATIC PHASE ERROR OF PLL

Bit Rate	Loop BW Setting	Loop Gain K_T ($\frac{1}{\text{Sec}}$)	Transition Density (M)	Frequency Uncertainty Δf_B Fract. Hz		Static Phase Error $\frac{\theta_0}{T}$
51.2 KB	Hi	127,000 M	0.5	0.05	2560	0.0404
			1.0			0.0202
			0.5	0.1	5120	0.0808
			1.0			0.0404
	Med	37,400 M	0.5	0.05	2560	0.136
			1.0			0.068
			0.5	0.1	5120	0.272
			1.0			0.136
	Low	17,000 M	0.5	0.05	2560	0.30
			1.0			0.15
			0.5	0.1	5120	0.60
			1.0			0.30
1.6 KB	Hi	3,970 M	0.5	0.05	80	0.04
			1.0			0.02
			0.5	0.1	160	0.08
			1.0			0.04
	Med	1,160 M	0.5	0.05	80	0.138
			1.0			0.069
			0.5	0.1	160	0.276
			1.0			0.138
	Low	530 M	0.5	0.05	80	0.30
			1.0			0.15
			0.5	0.1	160	0.60
			1.0			0.30

$$\frac{\theta_0}{T} = \frac{\Delta f_B}{K_T}$$

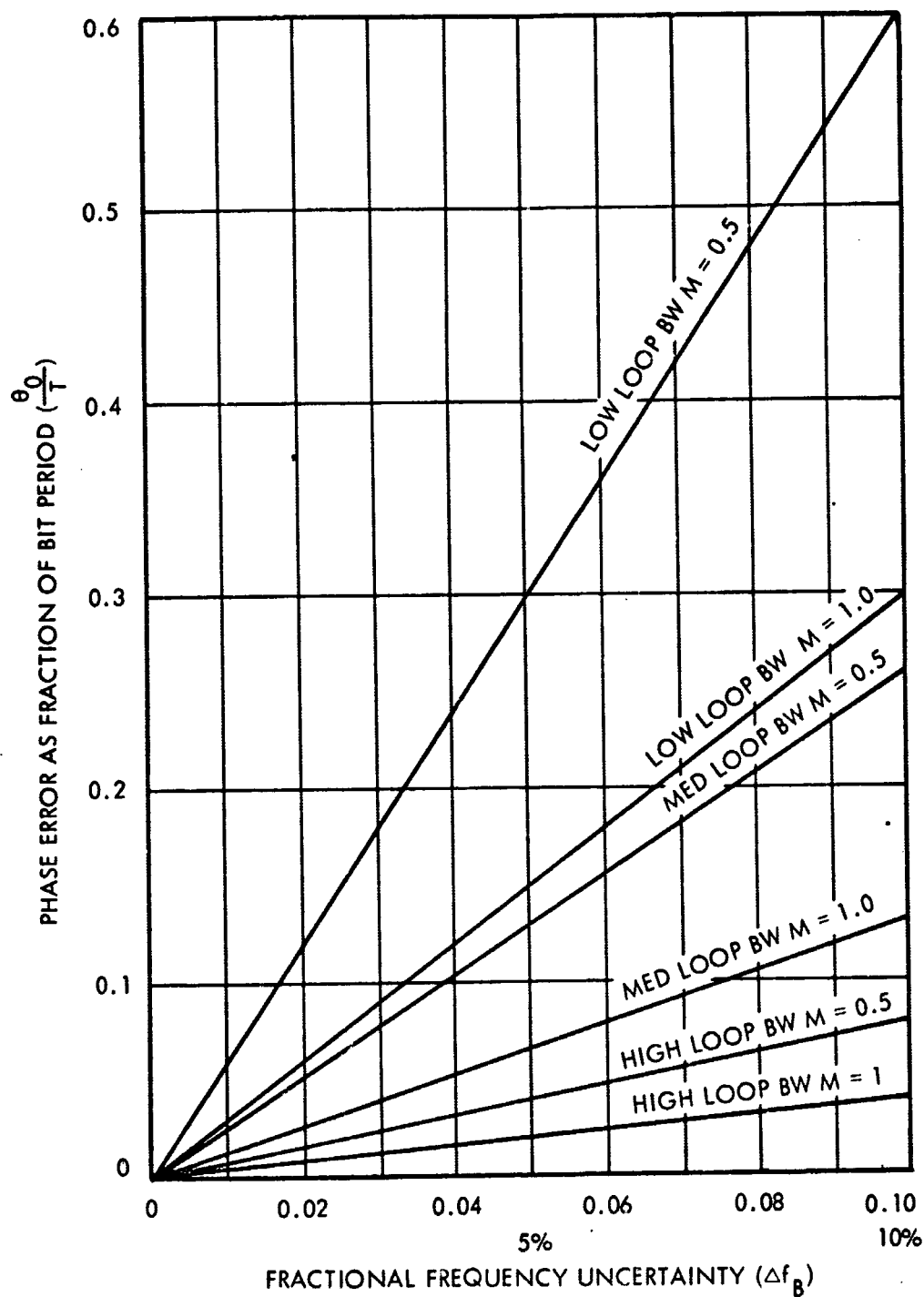


Figure F-12 PLL Static Phase Error Versus Frequency Uncertainty

This analysis shows that very severe timing errors result for frequency uncertainty of greater than 2% and reduced transition densities. Large frequency uncertainties are not expected to occur, however, because of "loop stress" metering provided at the output of the phase detector. The meter full scale reading measures maximum frequency uncertainties of 10%, such that meter accuracy of less than 10% results in static phase error of less than 1%.

From the curves of Figure F-12 the error normalized to frequency uncertainty for each loop bandwidth setting is as follows:

Hi Loop BW Setting:

$$\frac{\theta_o}{T} = \frac{0.4 \text{ Percent of bit period}}{M \text{ Percent frequency uncertainty}}$$

Med Loop BW Setting:

$$\frac{\theta_o}{T} = \frac{1.3 \text{ Percent of bit period}}{M \text{ Percent frequency uncertainty}}$$

Low Loop BW Setting:

$$\frac{\theta_o}{T} = \frac{3.0 \text{ Percent of bit period}}{M \text{ Percent frequency uncertainty}}$$

APPENDIX G

AC ANALYSIS OF THE MSFTP-2 BIT SYNCHRONIZER BASELINE CORRECTION LOOP

1.0 INTRODUCTION AND SUMMARY

The analysis presented in this appendix was undertaken to predict the AC performance of the MSFTP-2 bit synchronizer baseline correction technique and determine the resulting performance degradation due to AC baseline offset. In the analysis a linear model of the baseline corrector, which is a non-linear "bang-bang" feedback control loop, is developed and its AC response calculated. The resulting performance degradation, as a function of AC baseline offset, is estimated for the model.

The MSFTP-2 bit synchronizer technical information states that the limit of operation of the baseline corrector corresponds to AC baseline frequencies of 1% of bit rate. No reference is made to performance degradation. This analysis yields a performance degradation of approximately 2.8 db with sinusoidal input AC baseline of frequency equal to 1% of bit rate and amplitude of 100% of peak signal amplitude. No test data is available to date, due to time and equipment limitations, for comparison with calculated results.

2.0 BASELINE CORRECTOR CONFIGURATION

The baseline correction circuit is shown in simplified form in Figure G-1 and consists of the code averaging circuit (CA) and the AC baseline correction loop (BCL). The input to the circuit is the PCM data plus any AC and DC baseline offset, the output is the PCM data with baseline offsets removed or attenuated.

The low pass filter (LPF) and full wave rectifier (FWR) detect the envelope of the baseline offset by detecting the peak value of the PCM input data plus baseline. The peak value is compared with a reference threshold (E_{TH}) which is (ideally) set to the peak value of the PCM data. The circuit of Figure G-1 is simplified to that shown in G-2 by eliminating the LPF and FWR, setting the threshold (E_{TH}) to zero and letting the input

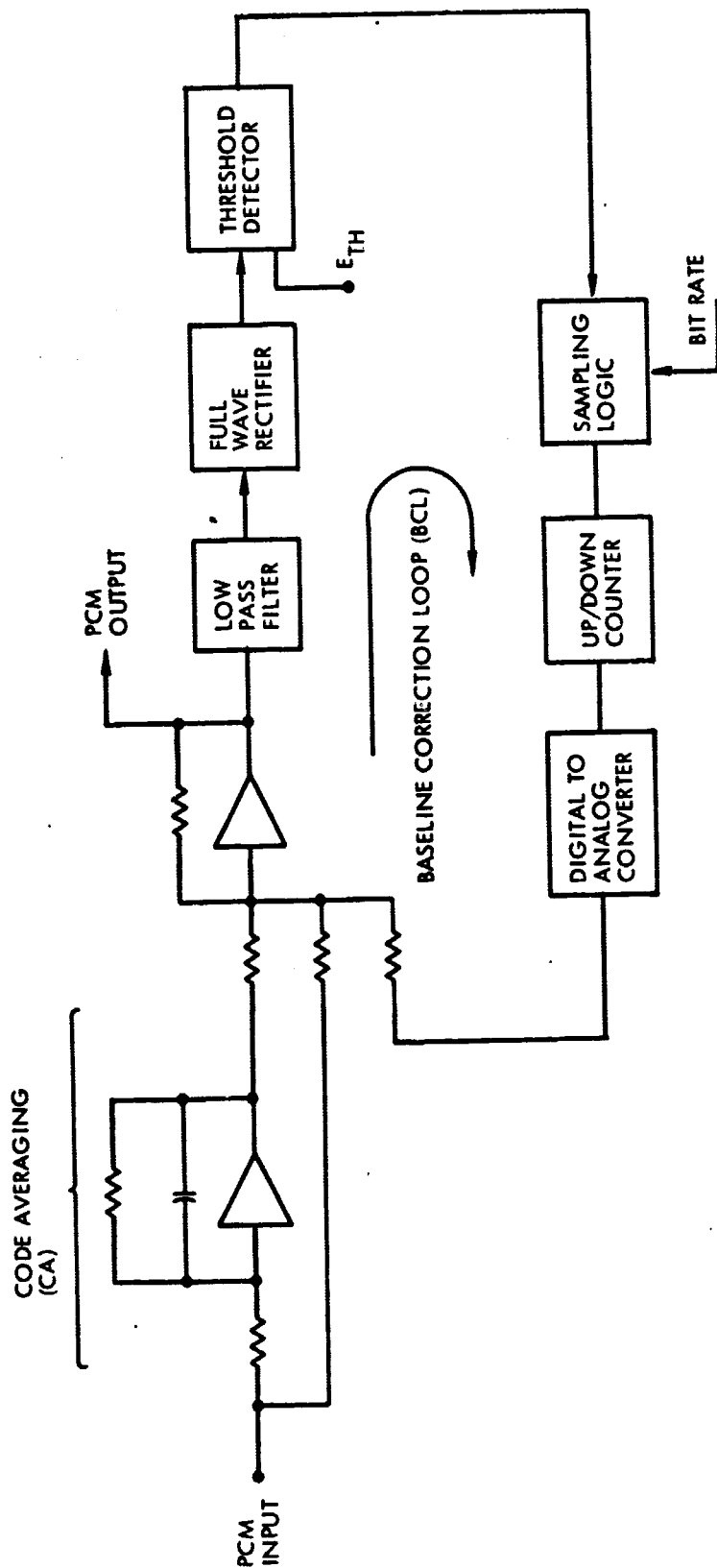


Figure G-1 Simplified Schematic of Baseline Correction Circuit

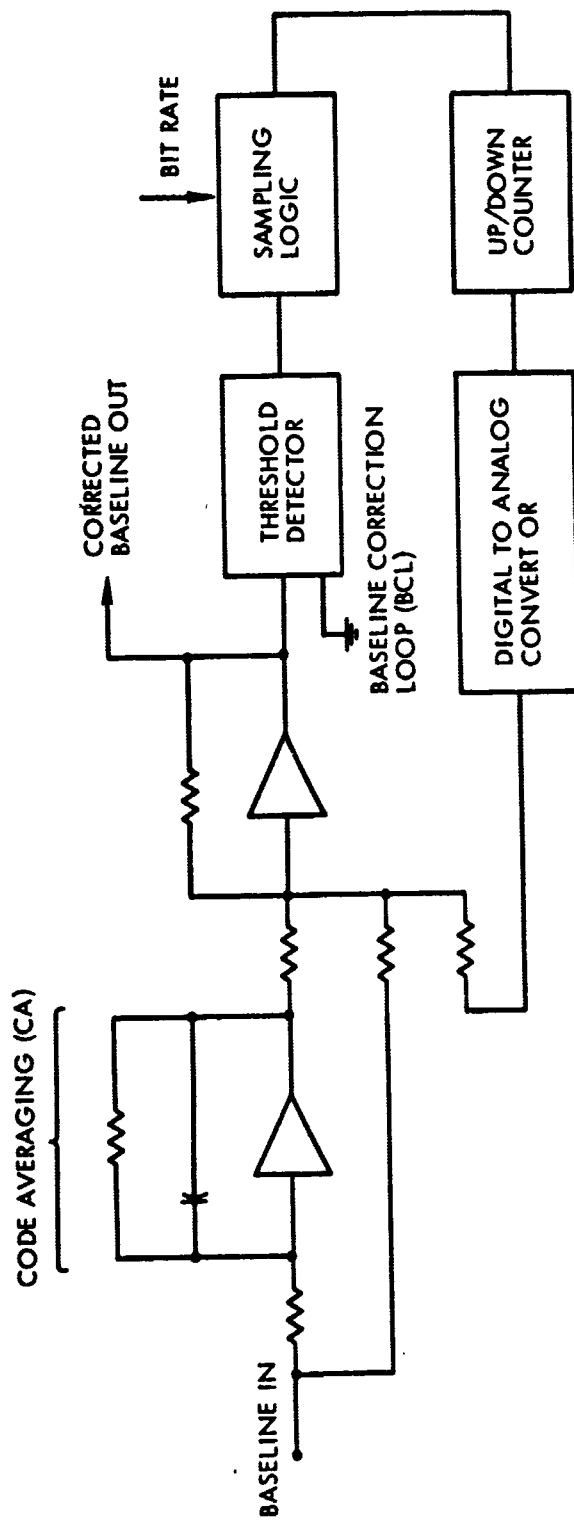


Figure G-2 Simplified Equivalent Circuit of Baseline Corrector

to the circuit be only the baseline offsets (no PCM data). This simplification is justified since the static errors due to the threshold are taken into account in the DC analysis of Appendix B.

The block diagram of Figure G-2 is further simplified to that shown in Figure G-3 by replacing the up/down counter and digital to analog converter with an ideal analog integrator. This simplification is justified in that the quantization error of the up/down counter and DAC are taken into account in the DC analysis of Appendix B. Substitution of the ideal integration linearizes the circuit, however, by eliminating the sampling logic. The result is a linear proportional control loop instead of a "bang-bang" loop.

The gain of the analog integrator ($\frac{1}{R_2 C_2}$) is set numerically equal to the maximum rate of excursion of the voltage out of the DAC. The DAC output can rise to 6V in a minimum time of 64 bit periods (T).

Thus

$$\frac{1}{R_2 C_2} = \frac{6}{64T} \text{ sec}^{-1}$$

at 51.2 KB:

$$T = \frac{1}{51.2K} = 19.2 \text{ } \mu\text{sec}$$

$$\frac{1}{R_2 C_2} = 4800 \frac{1}{\text{sec}}$$

at 1.6 KB:

$$T = \frac{1}{1.6K} = 625 \text{ } \mu\text{sec}$$

$$\frac{1}{R_2 C_2} = 150 \frac{1}{\text{sec}}$$

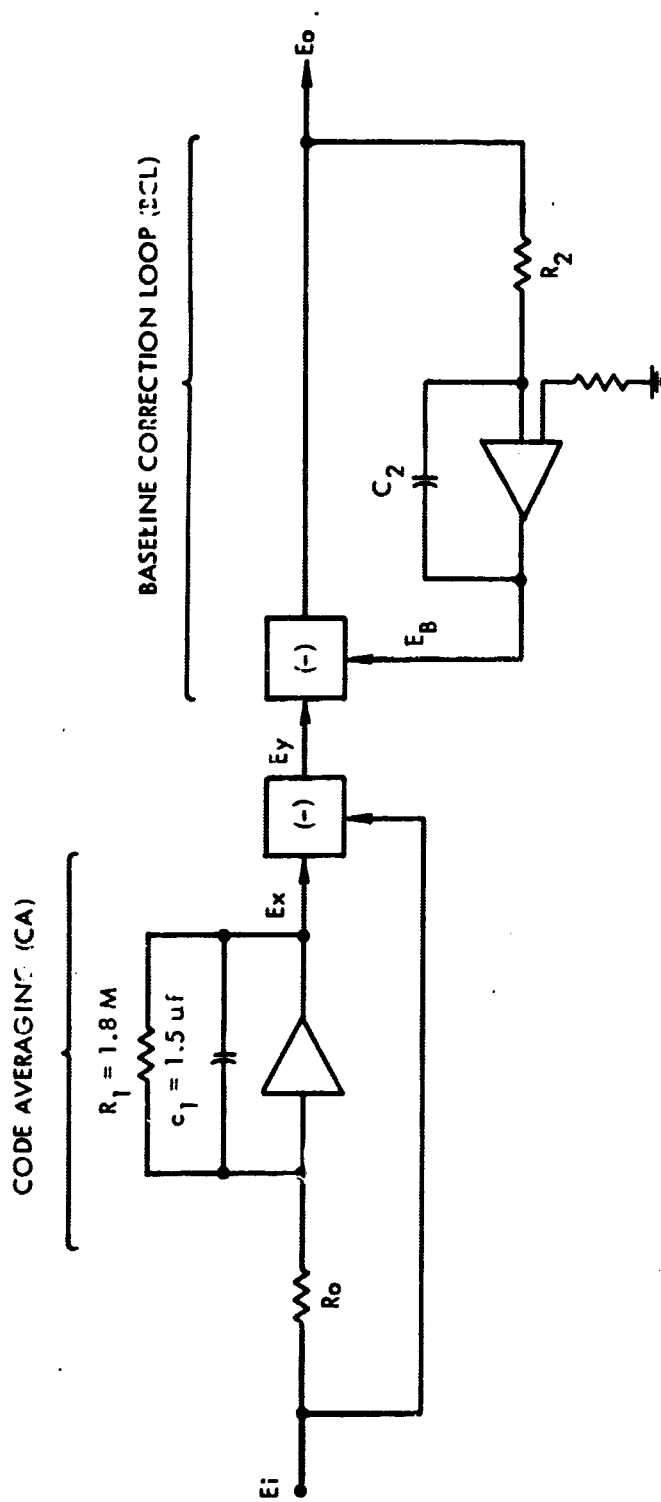


Figure G-3 Equivalent Block Diagram of Baseline Corrector

2.1 TRANSFER FUNCTION, LINEARIZED BASELINE CORRECTOR

Referring to Figure G-3:

$$\frac{E_x(s)}{E_i(s)} = \frac{R_1 \left(\frac{1}{sC_1} \right)}{\left(R_1 + \frac{1}{sC_1} \right) R_o} = \frac{R_1}{R_o} \left(\frac{1}{1 + sC_1 R_1} \right)$$

Since the overall gain of the code averaging, including the subtractor, is unity:

$$\frac{E_x(s)}{E_i(s)} = \frac{1}{1 + sC_1 R_1} = \frac{1}{1 + s\tau_1}$$

$$E_y(s) = E_i(s) - E_x(s)$$

$$E_y(s) = E_i(s) - E_i(s) \left(\frac{1}{1 + s\tau_1} \right)$$

$$\frac{E_y(s)}{E_i(s)} = 1 - \frac{1}{1 + s\tau_1} = \frac{s\tau_1}{1 + s\tau_1} = \frac{s}{s + \frac{1}{\tau_1}}$$

$$E_o(s) = E_y(s) - E_B(s)$$

$$E_B(s) = E_o(s) B(s)$$

$B(s)$ = Feedback Function

$$E_o(S) = E_y(S) - E_o(S) B(S)$$

$$E_y(S) = E_o(S) + E_o(S) B(S)$$

$$\frac{E_o(S)}{E_y(S)} = \frac{1}{1 + B(S)}$$

$$B(S) = \frac{1}{sC_2R_2} = \frac{1}{\tau_2 S}$$

$$\frac{E_o(S)}{E_y(S)} = \frac{1}{1 + \frac{1}{\tau_2 S}} = \frac{\tau_2 S}{1 + \tau_2 S} = \frac{S}{S + \frac{1}{\tau_2}}$$

The overall transfer function is:

$$H(S) = \frac{E_o(S)}{E_i(S)} = \left(\frac{E_o(S)}{E_y(S)} \right) \left(\frac{E_y(S)}{E_i(S)} \right) = \left(\frac{S}{S + \frac{1}{\tau_1}} \right) \left(\frac{S}{S + \frac{1}{\tau_2}} \right)$$

$$H(S) = \frac{S^2}{\left(S + \frac{1}{\tau_1} \right) \left(S + \frac{1}{\tau_2} \right)}$$

$$H(j\omega) = \frac{\omega^2}{\left(j\omega + \frac{1}{\tau_1} \right) \left(j\omega + \frac{1}{\tau_2} \right)}$$

$$\tau_1 = R_1 C_1 = (1.8 \times 10^6)(1.5 \times 10^{-6}) = 2.7 \text{ sec}$$

$$\frac{1}{\tau_1} = 0.37 \frac{1}{\text{sec}}$$

$$\omega_{c1} = \frac{1}{\tau_1} = 0.37 \frac{\text{RAD}}{\text{sec}}$$

$$f_{c1} = \frac{\omega_{c1}}{2\pi} = 0.06 \text{ Hz}$$

$$\tau_2 = R_2 C_2$$

at 51.2 KB:

$$\frac{1}{\tau_2} = 4800 \frac{1}{\text{sec}}$$

$$f_{c2} = \frac{1}{2\pi \tau_2} = 765 \text{ Hz}$$

at 1.6 KB:

$$\frac{1}{\tau_2} = 150 \frac{1}{\text{sec}}$$

$$f_{c2} = \frac{1}{2\pi \tau_2} = 24 \text{ Hz}$$

The baseline correction circuit is therefore a two section high pass circuit to baseline offset. Ideally it will correct DC offset with zero error and will pass AC offset in increasing amounts with increase in AC baseline frequency.

The break frequencies are:

<u>51.2 KB</u>	<u>1.6 KB</u>
0.06 Hz	0.06 Hz
765 Hz	24 Hz

The log magnitude of $H(j\omega)$ is plotted in Figure G4 for the two Apollo bit rates.

The technical information on the MSFTP-2 bit synchronizer says that the limit of operation of the baseline corrector to AC baseline offset is 1% of the bit rate or 512 Hz and 16 Hz for 51.2 KB and 1.6 KB respectively. Nothing could be found specifying the degradation expected at AC baseline offset of these frequencies.

The analysis shows (Figure G-4) that AC baseline offset of a frequency of 1% of the bit rate is attenuated by 5 or 6 db. Considerable degradation will result at these frequencies with large input AC baseline variation.

3.0 PERFORMANCE DEGRADATION DUE TO AC BASELINE OFFSETS

Exact calculation of degradation, due to AC offsets is unwieldy because the magnitude of the offset changes from bit to bit. Exact calculation would require that the fractional error probabilities, on a bit by bit basis, be calculated for the incremental change in offset voltage within each bit, due to the AC offset voltage. For example, if one cycle of sinusoidal AC offset encompasses one hundred bit periods, the individual error probability of each bit with its corresponding offset would have to be calculated and the error probabilities weighted by a value of $\frac{1}{100}$ and summed. This difficulty is avoided by using the average value of the AC offset as an approximate equivalent DC offset.

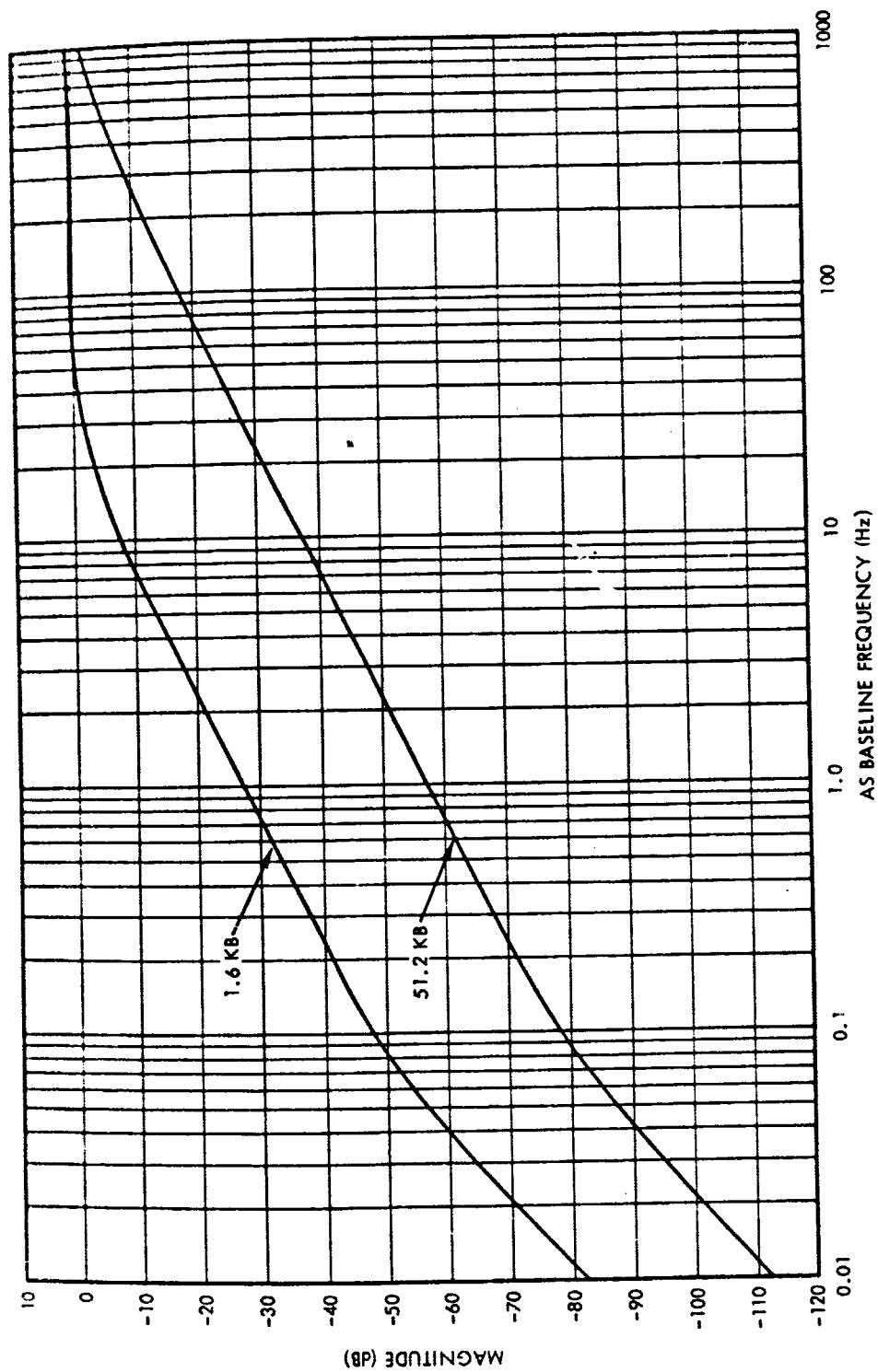


Figure G-4 Code Averaging and Baseline Correction Loop AC Response

The degradation as a function of AC baseline frequency has been estimated with input baseline amplitude of 100% of peak signal amplitude. The estimates were made by calculating the average baseline voltage out of the baseline circuit, as a function of frequency, and reading, from the DC offset curves of Section 4.0, the degradation which would result from a DC offset of the same magnitude. The estimated degradation is tabulated in Table G1 and plotted in Figures G-5 and G-6.

From Figures G-5 and G-6 it is seen that the estimated degradation at 1% of bit rate is approximately 2.8 db (again, this is with input baseline amplitude of 100% of peak signal amplitude which is comparatively large). The degradation decreases rapidly with decrease in the frequency of the AC baseline offset.

It is believed that the "shape" and the magnitude of Figures G-5 and G-6 is a reasonable representation of the MSFN bit synchronizer performance. It is recognized and pointed out, however, that the abscissa (frequency axis) may be in error due to the assumptions made in linearizing the loop, i.e., the curve may be "shifted" on the frequency axis. The shift would occur from the assumption of the value of gain ($\frac{1}{T_2}$) for the analog integrator and thus the upper break frequencies. No test data is available to date, due to time and equipment limitations, for comparison with predicted performance.

TABLE G-1

TABULATION OF ESTIMATED DEGRADATION DUE TO AC BASELINE OFFSET

AC Baseline Frequency (Hz)	Amplitude of Input AC Baseline (Fract. of Peak Signal)		Attenuation of AC Baseline (db)		Ave. Output AC Baseline (Fract. of Peak Signal)		Estimated Degradation (db)	
	Peak	Average	51.2 KB	1.6 KB	51.2 KB	1.6 KB	51.2 KB	1.6 KB
0.1	1.0	0.63	79	48	-	0.0016		0.04
1.0	1.0	0.63	58	28	-	0.02		0.8
5.0	1.0	0.63	-	14	-	0.125		2.1
10	1.0	0.63	38	8	0.008	0.25	0.04	3.4
20	1.0	0.63	32	4	0.016	0.42		
100	1.0	0.63	18	0	0.08	0.63	0.4	
200	1.0	0.63	12	0	0.16		1.2	
500	1.0	0.63	6	0	0.31		2.7	

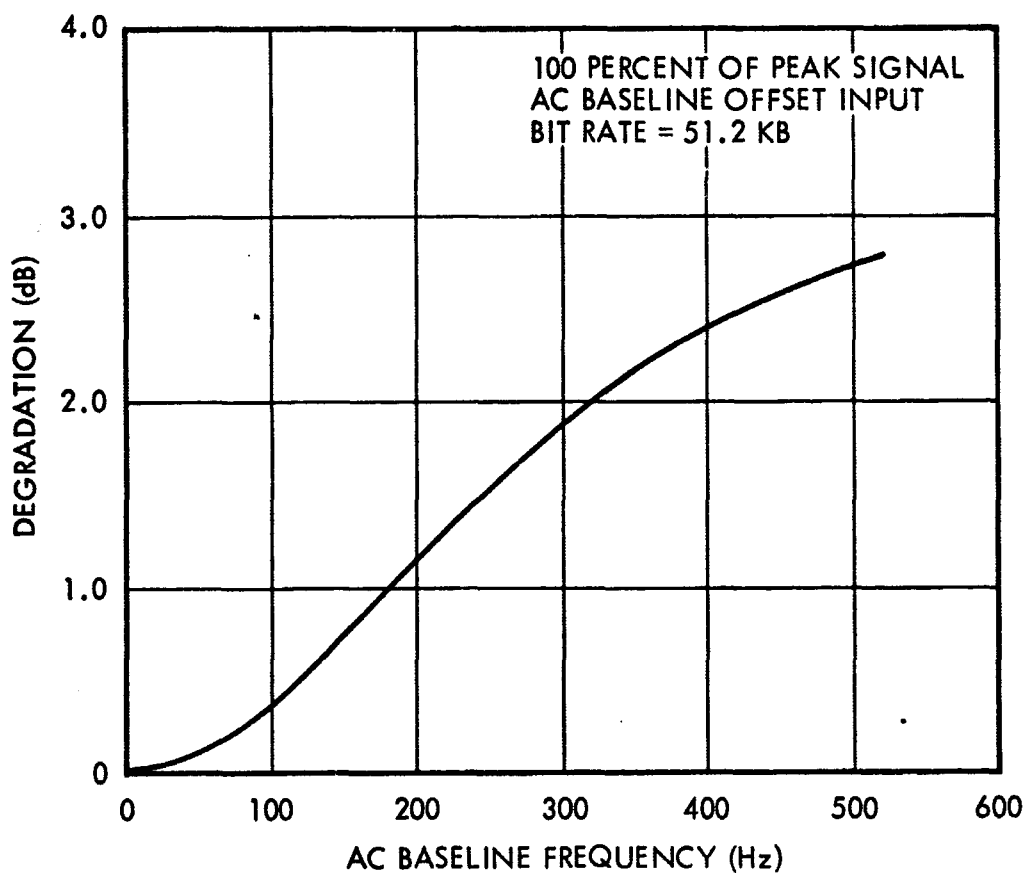


Figure G-5 Degradation Versus AC Baseline Frequency

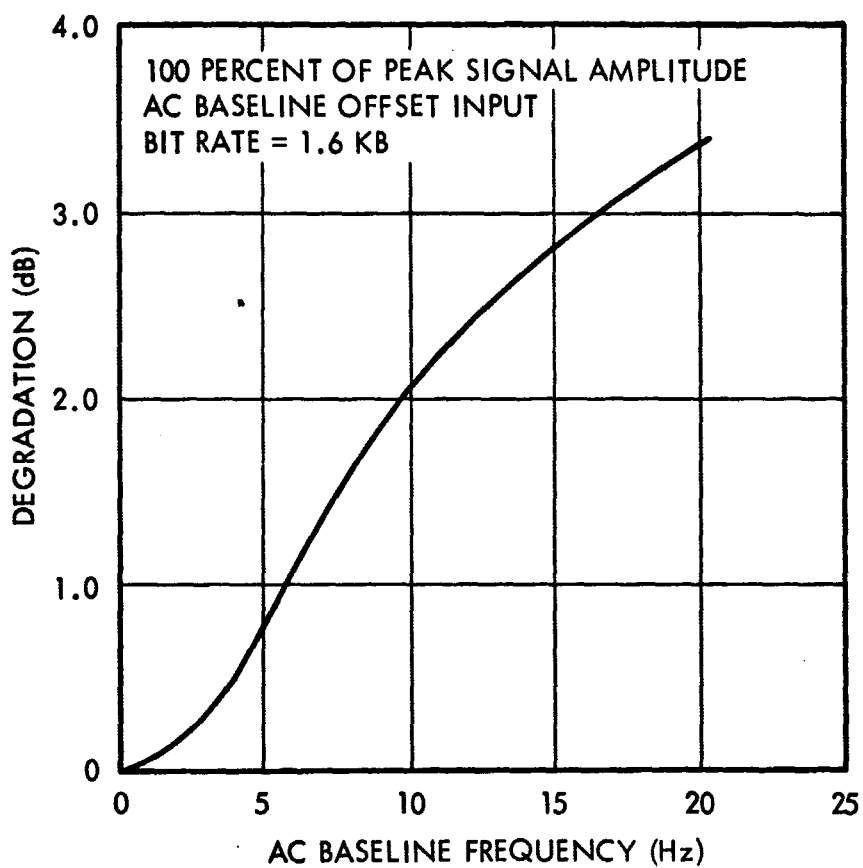


Figure G-6 Degradation Versus AC Baseline Frequency

APPENDIX H

COMPUTER PROGRAMS

The flow diagram for determining the signal-to-noise degradation in a circuit is shown in Figure H-1. The procedure is to convert the signal-to-noise ratio (SNR) into a probability error (PE) by means of the error function (ERF), determine the increase in the PE as a function of the bit density and circuit parameters, and then reconvert the new PE back into an equivalent SNR.

The computer method of determining the error function is to use the series for the solution. Thus

$$\begin{aligned}\text{ERF}(x) &= \frac{2}{\sqrt{\pi}} \int_0^x e^{-t^2} dt \\ &= \frac{2}{\sqrt{\pi}} \int_0^x \left(1 - t^2 + \frac{t^4}{2!} - \frac{t^6}{3!} + \frac{t^8}{4!} - \dots \right) dt \\ &= \frac{2}{\sqrt{\pi}} \left(x - \frac{x^3}{3} + \frac{x^5}{5 \cdot 2!} - \frac{x^7}{7 \cdot 3!} + \frac{x^9}{9 \cdot 4!} - \dots \right)\end{aligned}$$

Letting $x = 0$ th term and $\frac{-x^3}{3} = 1$ st term, the n th term

$$= \frac{(-1)^n x^{2n+1} (2n+1)}{(2n+1)(n!)}$$

The ratio of the $n+1$ st term to the n th term

$$= \frac{-(2n+1)x^2}{(2n+3)(n+1)}$$

The ratio of the 1st to the 0th term is obtained by letting $n = 0$, the 2nd to the 1st term by letting $n = 1$, etc.

Therefore the individual terms of the error function series may be obtained by initializing the series by letting $\text{ERF}(x) = \frac{2}{\sqrt{\pi}} x$ and determining additional terms by multiplying by the above ratios from $n = 0$ to the number necessary to obtain the desired accuracy. As each term is calculated it is accumulated to give a more accurate value for the error function.

The converse method of solving for x when the $\text{ERF}(x)$ is known is shown in the flow diagram in the DO loop "LOOK". The method is to assume an x , solve for the corresponding error function, obtain the difference between the true and trial error functions, divide the difference by the slope of the error function curve, $\frac{2}{\sqrt{\pi}} e^{-x^2}$, and increment the original value of the assumed x by this amount. The process is repeated until the desired accuracy is achieved. The assumed value of x must be less than the true value of x in order for the method to work.

In some subprograms used for solving for network parameters it was necessary to obtain the Si function: i.e., $\text{Si}(x) = \int_0^x \frac{\sin u}{u} du$. This was done in a manner similar to that used for the error function. The ratio of successive terms for the $\text{Si}(x)$ series is $\frac{-(2n-1)x^2}{(2n)(2n+1)^2}$. The ratio of the 2nd to the 1st term is obtained by letting $n = 1$.

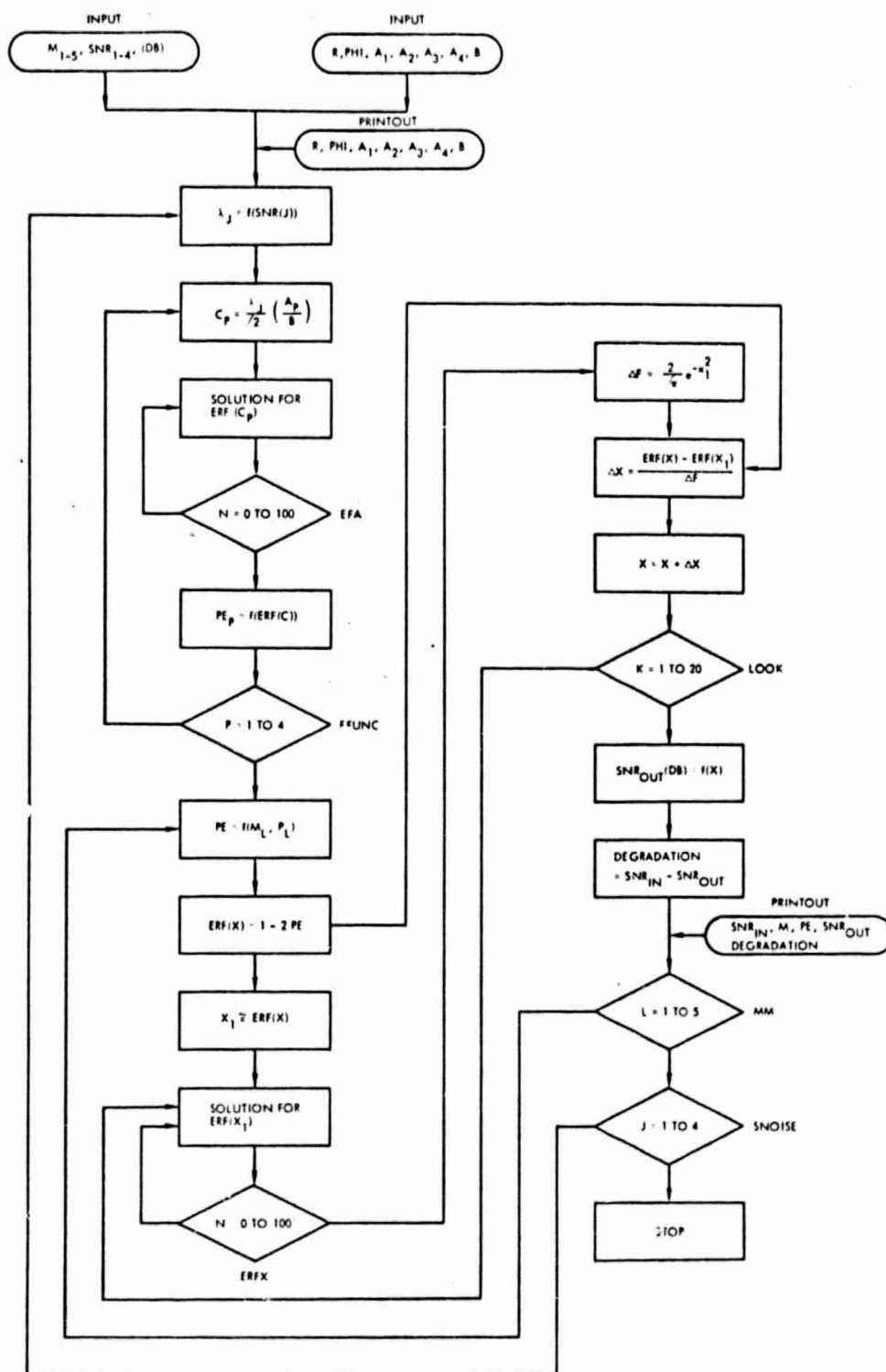


Figure H-1 Flow Diagram of Program for Determining Error Probability and Performance Degradation in db

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2. M. Schwartz, "Information Transmission, Modulation, and Noise," McGraw-Hill Book Company, 1959.
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4. U. S. Department of Commerce, National Bureau of Standards, Applied Mathematics Series #41, "Tables of the Error-Function and Its Derivative."
5. "Standard Mathematical Tables," Chemical Rubber Publishing Company, 1957.
6. TRW Systems, Report No. 05952-H509-R0-00, "Optimization of Equivalent Noise Bandwidth Measurements."
7. TRW Systems, Report No. 11176-H072-R0-00, "Test Accuracy Analysis of Downlink PM Telemetry for Electronic Systems Compatibility Laboratory."

TRW

69:7251-HDF-333
24 November 1969
Re: Task E-59C

National Aeronautics and Space Administration
Manned Spacecraft Center
Houston, Texas 77058

Attention: T. E. Ohnesorge, EE7
Tele/Communications Systems Division
Building 440, Room 216

Subject: Update of TRW Project Technical Report #11176-H236-R0-00 "MSFTP-2
Bit Synchronizer Performance Analysis", 27 May 1968.

Gentlemen:

The information contained in this memo will allow the MSFTP-2
BIT SYNCHRONIZER REPORT, TRW Document #11176-H236-R0-00 to be updated.

On page 4-2 there is an error in the definition of λ^2 . The
corrected page 4-3 should be inserted.

Pages 4-3 and 4-4 attached should replace pages 4-3 and 4-4 in
the document. These pages contain additional information to aid the reader.

The assumption of a constant output for waveform 4 of page 4-11,
Figure 4.3.2.2, while being an excellent engineering assumption (within 1%)
results in an apparent improvement in the matched filter detector from pre-
filtering for low transition densities, i.e. $\approx 10\%$. (Section 4.5.2.2, Perfor-
mance Degradation Curves of L&D Filter Due to Prefiltering, Figures 4.5.5
through 4.5.16). In reality no net improvement can be obtained by pre-
filtering before matched filter detection.

TRW SYSTEMS GROUP



H. D. Freeman, Manager
Task E-59C



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J. L. Coffman, Assistant Project Manager
Engineering Analysis
Spacecraft Systems Analysis Project

HDF:jw
Attachment

4.0 PERFORMANCE ANALYSIS UTILIZING INTEGRATE AND DUMP BIT DETECTOR

4.1 THEORETICAL PERFORMANCE OF I&D DETECTOR

The probability of occurrence of a bit error in a PCM system is the probability that the noise will exceed the signal voltage in amplitude and be of the opposite polarity, causing the detector to decide on the wrong symbol. For the case of Gaussian noise the probability of error is determined using the Gaussian probability density function, $P(X)$.

$$P(X) = \frac{1}{\sqrt{2\pi} \sigma} e^{-\frac{x^2}{2\sigma^2}} \quad (4.1.1)$$

The probability that the instantaneous noise voltage is less than the peak signal voltage, A , is:

$$\text{Prob}(X < A) = \int_{-\infty}^A P(X) dx = \int_{-\infty}^A \frac{1}{\sqrt{2\pi} \sigma} e^{-\frac{x^2}{2\sigma^2}} dx \quad (4.1.2)$$

letting $y = \frac{x}{\sigma}$

$$\text{Prob}(X < A) = \int_{-\infty}^{\frac{A}{\sigma}} \frac{1}{\sqrt{2\pi}} e^{-\frac{y^2}{2}} dy \quad (4.1.3)$$

but: $\frac{A}{\sigma} = \lambda = \frac{\text{Peak signal voltage out of the detector}}{\text{RMS noise voltage out of the detector}}$

The probability of error as a function of signal-to-noise ratio, $P_E(\lambda)$, is:

$$P_E(\lambda) = 1 - \int_{-\infty}^{\lambda} \frac{1}{\sqrt{2\pi}} e^{-\frac{y^2}{2}} dy = 1 - \phi(\lambda) \quad (4.1.4)$$

$$P_E(\lambda) = 0.5 - \int_0^{\lambda} \frac{1}{\sqrt{2\pi}} e^{-\frac{y^2}{2}} dy \quad (4.1.5)$$

$$\lambda^2 = \frac{\text{Peak signal power per bit out of the detector}}{\text{RMS Noise power out of the detector}}$$

$$\lambda^2 = \frac{A^2}{N_0 B} = \text{Detector output signal-to-noise ratio}$$

N_0 = noise spectral density (one sided)

B_N = detector bandwidth (one sided)

Therefore the probability of error, $P_E(\lambda)$, is a function of the voltage signal-to-noise ratio out of the detector and is therefore referred to the detector noise bandwidth. The one sided noise bandwidth of an integrate and dump detector with NRZ data is one half the bit rate as shown in the following.

The two sided noise bandwidth (B_N) of a linear network [6] is defined as:

$$B_N = \frac{\int_{-\infty}^{\infty} |H(j\omega)|^2 df}{|H(j\omega)|_{\text{MAX}}^2}$$

$H(j\omega)$ = magnitude of network transfer function

The transfer function of the I&D filter is:

$$H(S) = \frac{A(1 - e^{-ST})}{S} \quad (4.1.6)$$

$$H(j\omega) = \frac{A}{j\omega} (1 - e^{-j\omega T}) = \frac{A}{j\omega} \left(e^{\frac{j\omega T}{2}} - e^{-\frac{j\omega T}{2}} \right) e^{-\frac{j\omega T}{2}} \quad (4.1.7)$$

$$\sin X = \frac{1}{2j} (e^{jX} - e^{-jX})$$

$$H(j\omega) = AT e^{-\frac{j\omega T}{2}} \left[\frac{\sin \frac{\omega T}{2}}{\frac{\omega T}{2}} \right] \quad (4.1.8)$$

$$|H(j\omega)|^2 = A^2 T^2 \left[\frac{\sin \frac{\omega T}{2}}{\frac{\omega T}{2}} \right]^2 = A^2 T^2 \left[\frac{\sin \pi T f}{\pi T f} \right]^2 \quad (4.1.9)$$

$$B_N = \frac{2 A^2 T^2 \int_0^{\infty} \left[\frac{\sin \pi T f}{\pi T f} \right]^2 df}{A^2 T^2}$$

Let

$$X = \pi T f$$

$$B_N = \frac{2}{\pi T} \int_0^{\infty} \left[\frac{\sin X}{X} \right]^2 dX$$

$$\int_0^{\infty} \left[\frac{\sin X}{X} \right]^2 dX = \frac{\pi}{2}$$

$$B_N = \frac{1}{T}$$

$$B_N = \frac{1}{T} = f_B = \text{bit rate (two sided)}$$

Therefore

$$B_N = \frac{f_B}{2} = \frac{1}{2} \text{ bit rate (one sided)}$$

Sample calculation of theoretical performance for the I&D filter, using Equation 4.1.4, are shown tabulated in Table 4.1.1 and plotted in Figure 4.1.1.

The results of the preceeding discussion are adhered to throughout the MSFTP-2 bit synchronizer analysis. Performance degradation is always calculated as degradation from theoretical as shown in the figure. Signal-to-noise ratio is always referred to the I&D detector noise bandwidth.