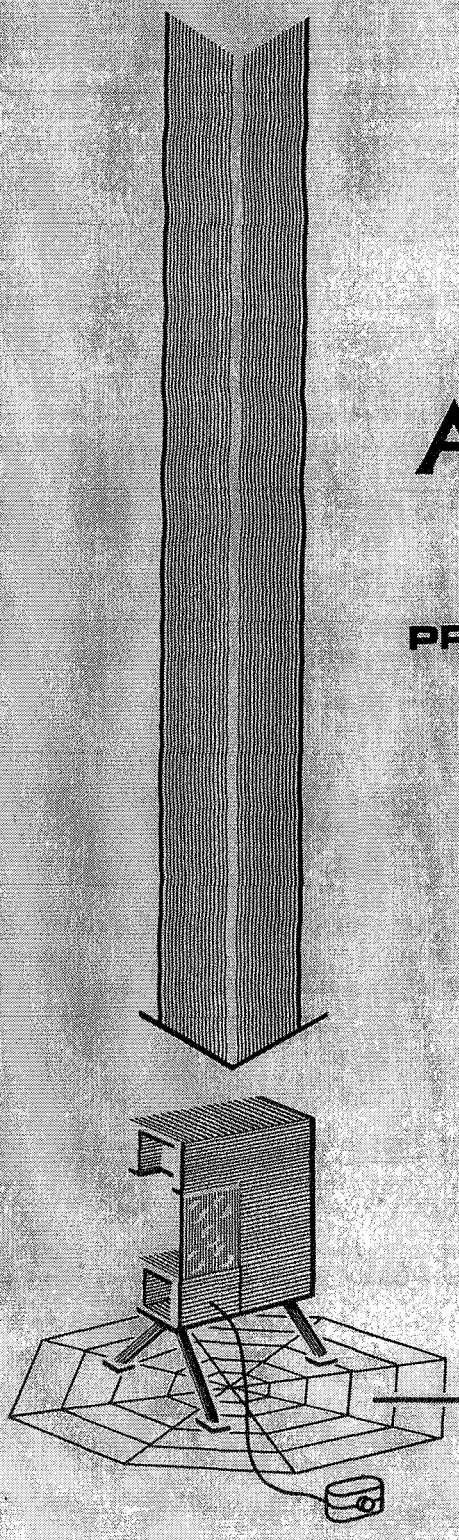
final report

volume 1

ALSEP/SIDE/CCGE

contract no. S1966-14

PRIME CONTRACT NO. NAS 9-5911



TIME-ZERO corporation

NASA CR 102046

FINAL ENGINEERING REPORT

For

ALSEP/SIDE/CCGE

(Apollo Lunar Surface Experiments Package/
Suprathermal Ion Detector Experiment/
Cold Cathode Gauge Experiment)

Contract No. S1966-14
Prime Contract No. NAS 9-5911

Prepared For

RICE UNIVERSITY

Houston, Texas

Prepared By

TIME-ZERO CORPORATION
(Formerly Marshall Laboratories)

ENGINEERING REPORT

ALSEP/SIDE/CCGE

CONTRACT NO. S1966-14

PRIME CONTRACT NO. NAS 9-5911

PREPARED BY: R. A. Rivas
R. A. Rivas
Member of the Technical Staff

PREPARED BY: Sam Pollack
Sam Pollack
Program Mechanical Engineer

APPROVED BY: William Sandstrom
William Sandstrom
Program Manager

APPROVED BY: George P. Mohler
George Mohler
Vice-President
Manager, Aerospace Division

ABSTRACT

The Suprathermal Ion Detector Experiment/Cold Cathode Gauge Experiment (SIDE/CCGE) was designed and fabricated by Marshall Laboratories as an integral part of the Apollo Lunar Surface Experiments Package (ALSEP).

The SIDE/CCGE Experiment will measure the flux, number density, velocity and energy per unit charge of positive ions in the vicinity of the lunar surface and transfer such information to the ASLEP Data Subsystem. A Low Energy (LE) detection system, consisting of a Wein Velocity selector (crossed electric and magnetic fields), an electrostatic analyzer, and a Channeltron (R) Electron Multiplier, detects positive ions with masses up to 130 AMU, and measures the differential energy spectrum of ions in a narrow velocity range having energies from 0.2 ev to 48.6 ev per unit charge. A High Energy (HE) detection system, consisting of an electrostatic analyzer and a Channeltron (R) Electron Multiplier, detects all positive ions regardless of mass, and measures the differential energy spectrum of ions having energies from 10 ev to 3500 ev per unit charge. The ions passing through the electrostatic analyzers of each detection system are focused on their respective Channeltron (R) Electron Multiplier (2 per SIDE), whose output is amplified by their Detector Amplifiers (2 per SIDE). A data accumulator (0 to 10^6 counts per sample interval) stores the amplified channeltron output pulses during each accumulation interval. Parallel data paths direct to the ALSEP Analog-to-Digital (A/D) converters are provided for the High Energy and Low Energy detection systems. Outputs of the converters consist of eight bits of digital information, which are commutated into one output. Housekeeping data is also monitored by the SIDE A/D Converters. A Master Timing Generator controls all timing functions as follows: (1) provides an address for each frame in a cycle (SIDE FRAME count), (2) provides sequencing information for the electrostatic analyzer stepping voltages, velocity selector voltages, and Ground Plane Screen voltages, and (3) provides sequencing and timing signals for various portions of the experiment. The Ground Plane Screen furnishes a stepped reference potential on the lunar surface for the entire experiment. A Command System consisting of five command lines furnishes any of 16 command input combinations.

The CCGE experiment will determine (1) the density of any lunar ambient atmosphere corresponding to pressures of 10^{-6} torr to approximately 10^{-12} torr, including any temporal variations either of a random character or associated with lunar local time or solar

activity, and (2) the rate of loss of contaminants left in the landing area by the astronauts and the Lunar Module. The sensor is a plasma discharge device which effects conversion of density to direct current. An Auto Ranging, Auto Zero electrometer monitors currents in the 10^{-14} to 10^{-6} amperes range, and the data is processed by the A/D converters in the SIDE. The gauge produces a magnetic field of 1020 gauss, and operates at an anode voltage of 4500 volts. A Seal Mechanism provides protection against premature contamination of the sensor, and is released when the proper command is executed from the ground station.

Special equipment requirements include an Experiment Test Set (ETS) to completely check out the entire experiment package. The ETS consists of the following major subassemblies: (1) Data Processor, Printer Unit, Data Phone Unit; (2) Display Unit; (3) ALSEP Simulator Unit; (4) Monitor Unit; and (5) Oscilloscope/ Counter Unit. The function of the ETS is to process data from the SIDE/CCGE, display it in decimal form, print out the data or transmit it through the dataphone, provide timing and command signals to simulate the function of ALSEP, and supply power to the SIDE/ CCGE.

TABLE OF CONTENTS

FIGURES AND ILLUSTRATIONS

TABLES

ACKNOWLEDGEMENT

The authors wish to express their gratitude to all Rice University and Time-Zero Corporation (formerly Marshall Laboratories) personnel who contributed maximum assistance in the preparation of this document.

1.0 INTRODUCTION

This engineering report describes the ALSEP/SIDE/CCGE Experiment designed, fabricated, tested, and delivered by Marshall Laboratories in accordance with Rice University Contract No. S1966-14.

The function of the experiment is to measure the flux, number density, velocity and energy per unit charge of positive ions near the lunar surface, and to detect any lunar ambient atmospheric pressure. The experiment will measure the differential energy spectrum of ions having energies from 0.2 ev to 3500 ev per unit charge.

The report covers electrical, thermal, and mechanical descriptions of the instrument. Also included is a description of the Experiment Test Set.

The following figures provide an introductory summary of pertinent features of the ALSEP/SIDE/CCGE Experiment:

a)	Figure 1.0-1	Lunar Surface Deployment
b)	Figure 1.0-2	Close-Up Photograph, SIDE/CCGE in deployed Configuration
c)	Figure 1.0-3	ALSEP System Objectives
d)	Figure 1.0-4	SIDE/CCGE Objectives Summary
e)	Figure 1.0-5	Stowed Configuration
f)	Figure 1.0-6	Deployment for ALSEP
g)	Figure 1.0-7	SIDE/CCGE Deployment
h)	Figure 1.0-8	ALSEP Objectives
i)	Figure 1.0-9	ALSEP Experiments
j)	Figure 1.0-10	SIDE/CCGE General Features

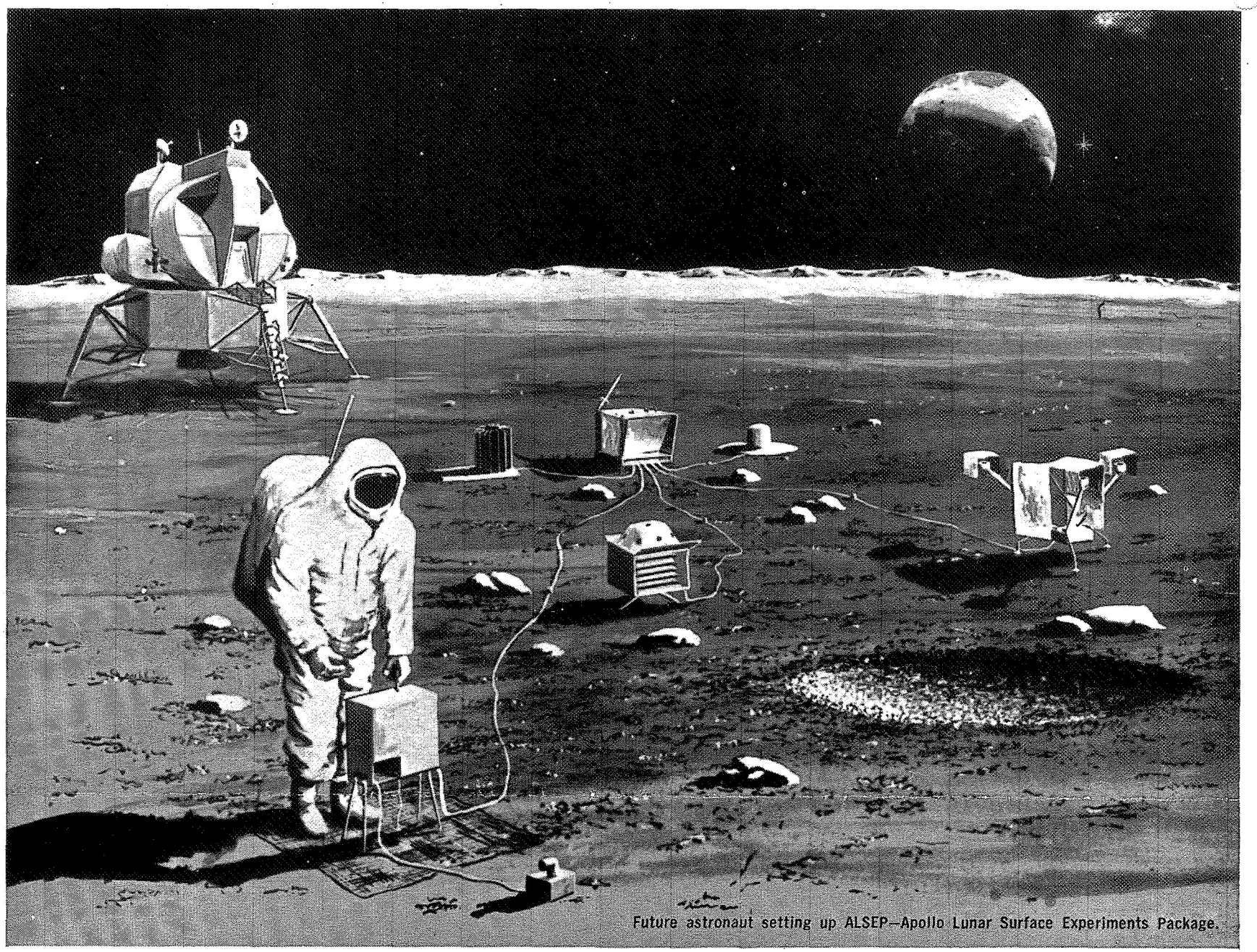


FIGURE 1.0-1 LUNAR SURFACE DEPLOYMENT

This Widely Published Illustration Features Time-Zero's Suprathermal Ion Detector Built For Rice University
(Artist's Conception)

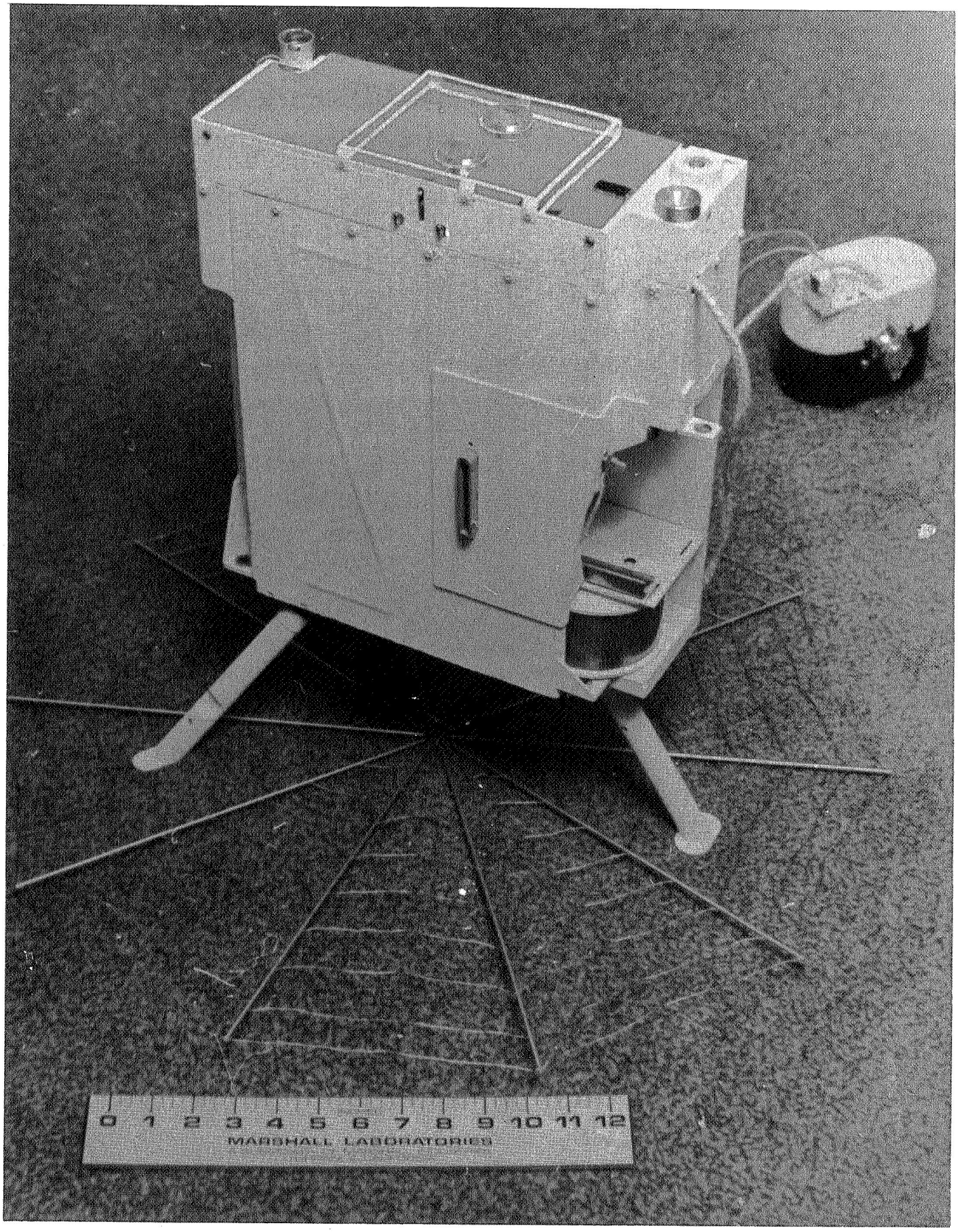


FIGURE 1.0-2 SIDE/CCGE DEPLOYED CONFIGURATION - PROTOTYPE

ALSEP SYSTEM OBJECTIVES

DETERMINE LUNAR CHARACTERISTICS

- INTERNAL STRUCTURE & COMPOSITION
- STATE OF INTERIOR
- COMPOSITION OF ATMOSPHERE
- GENESIS OF SURFACE FEATURES

THIS LUNAR INFORMATION WILL PROVIDE NEW INSIGHTS INTO THE GEOLOGY & GEOPHYSICS OF THE EARTH.

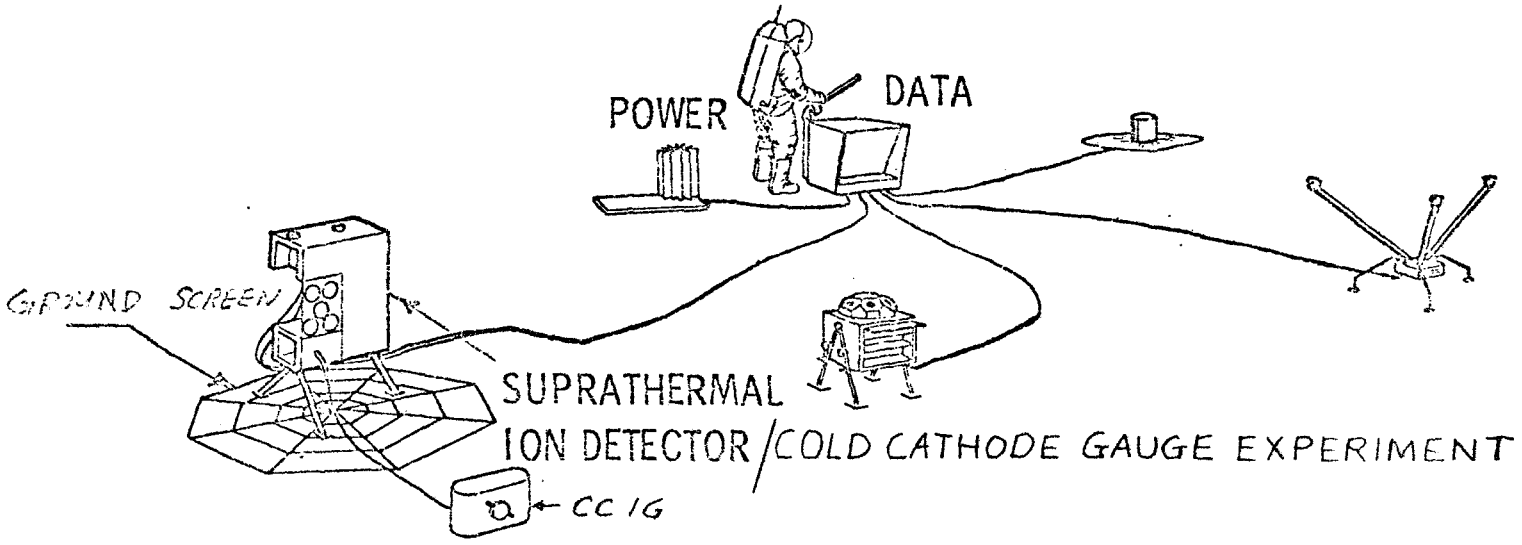


FIG 1.0-3

SUPRATHERMAL ION DETECTOR / COLD CATHODE GAUGE EXPERIMENT
NASA No. SO36

OBJECTIVE: IONOSPHERE/ATMOSPHERE CHARACTERISTICS, POSSIBILITY OF VOLCANIC PROCESSES, AMBIENT ELECTRIC FIELD EFFECTS.

MEASUREMENT: FLUX, COMPOSITION, ENERGY, & VELOCITY OF LOW-ENERGY POSITIVE IONS; HIGH-ENERGY SOLAR WIND FLUX; TOTAL PRESSURE

EQUIPMENT: TWO CURVED - PLATE ANALYZERS (ONE WITH VELOCITY FILTER), GROUND PLANE, COLD CATHODE ION GAGE

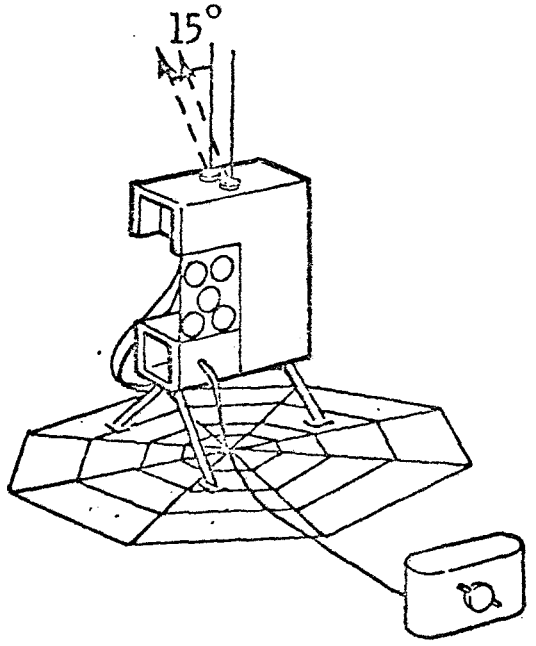


FIG 1.0-4 SIDE/CCGE OBJECTIVES SUMMARY

STOWED CONFIGURATION

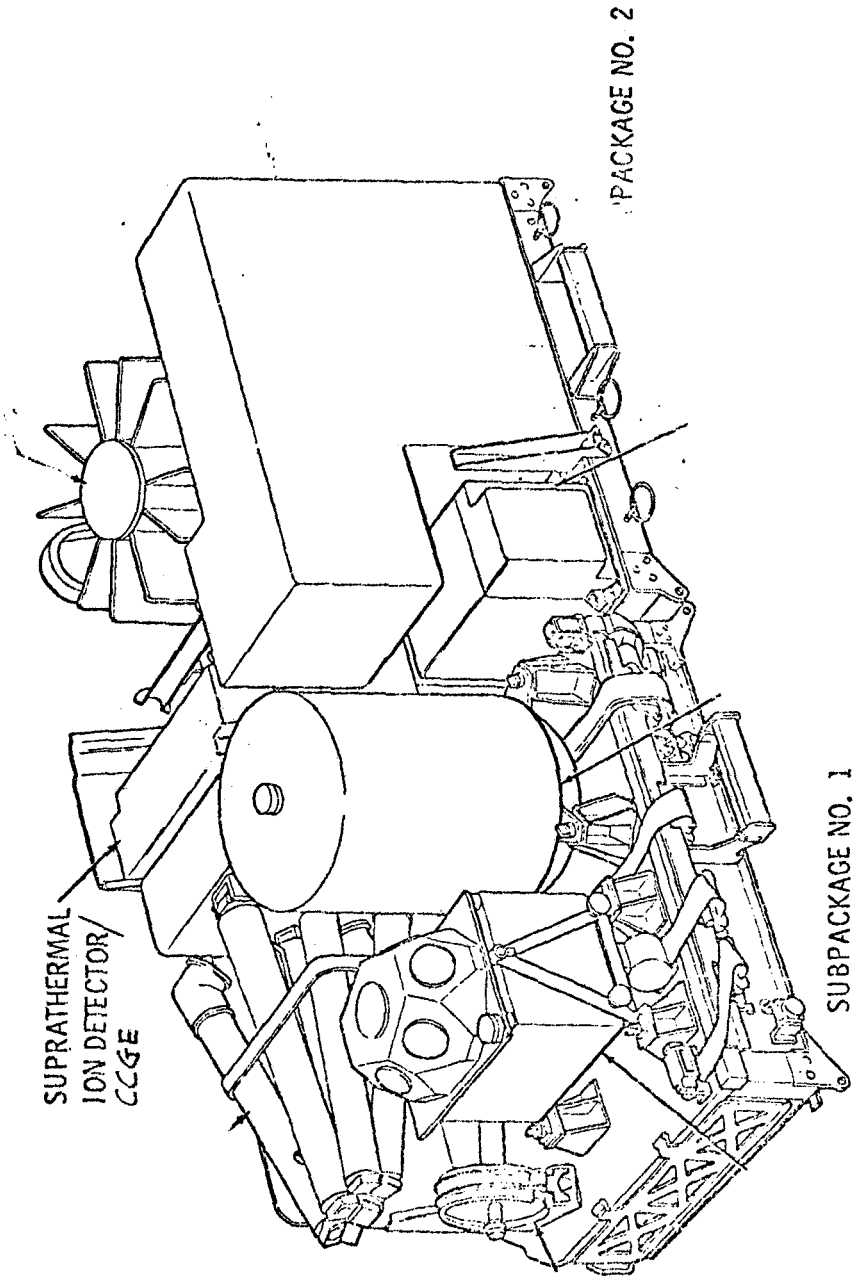


FIG 1.0-5

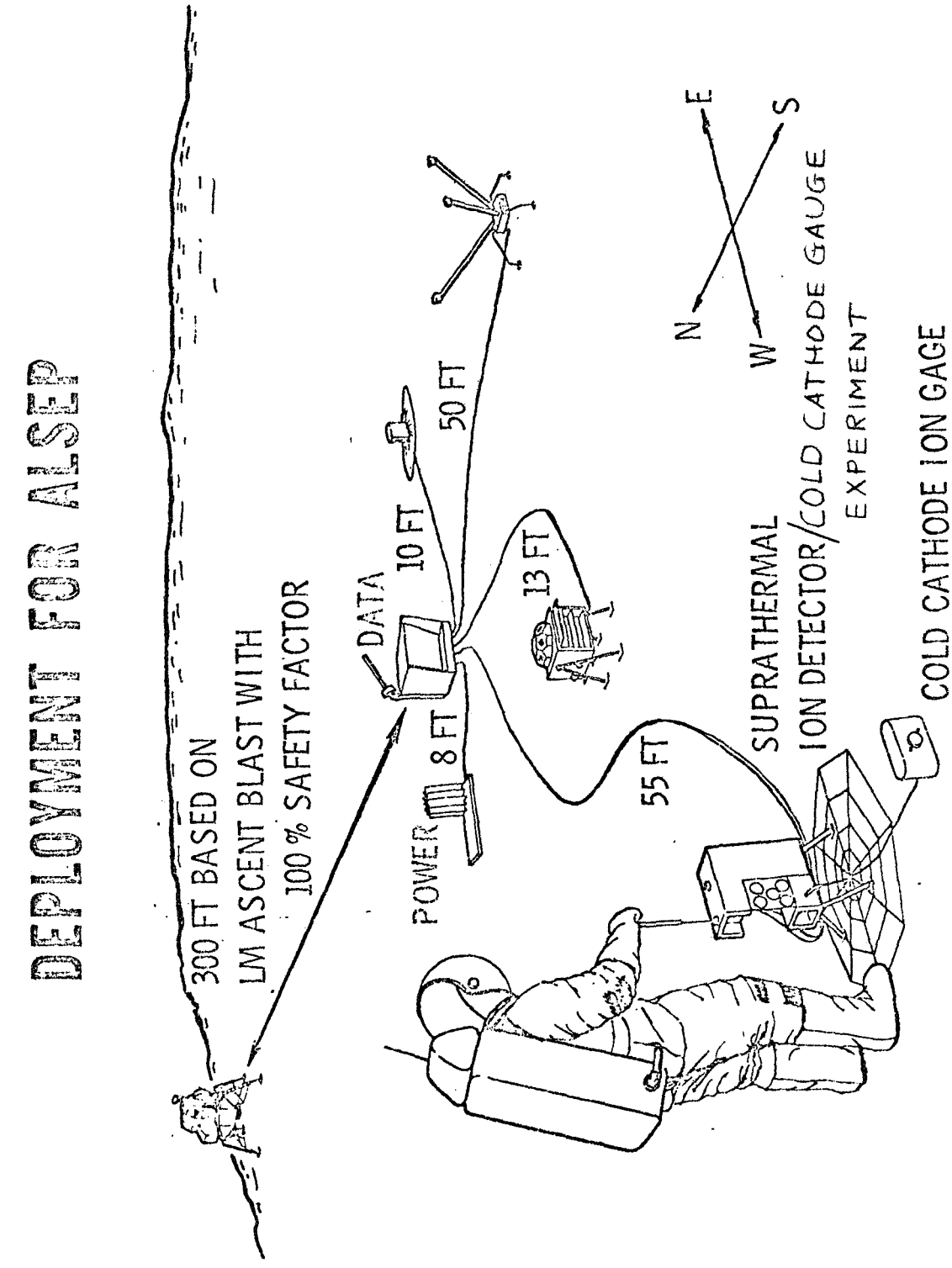

DEPLOYMENT FOR ALSEP
300 FT BASED ON
LM ASCENT BLAST WITH
100 % SAFETY FACTOR
DATA
10 FT
50 FT
13 FT
POWER
8 FT
55 FT
N
E
W
S
SUPRATHERMAL
ION DETECTOR/COLD CATHODE GAUGE
EXPERIMENT
COLD CATHODE ION GAGE

FIG 10-6

SUPRATHERMAL ION DETECTOR EXPERIMENT / CCGE

(SIDE)

- COMPONENTS & FUNCTIONS
- DEPLOYMENT
- COMMANDS & DATA

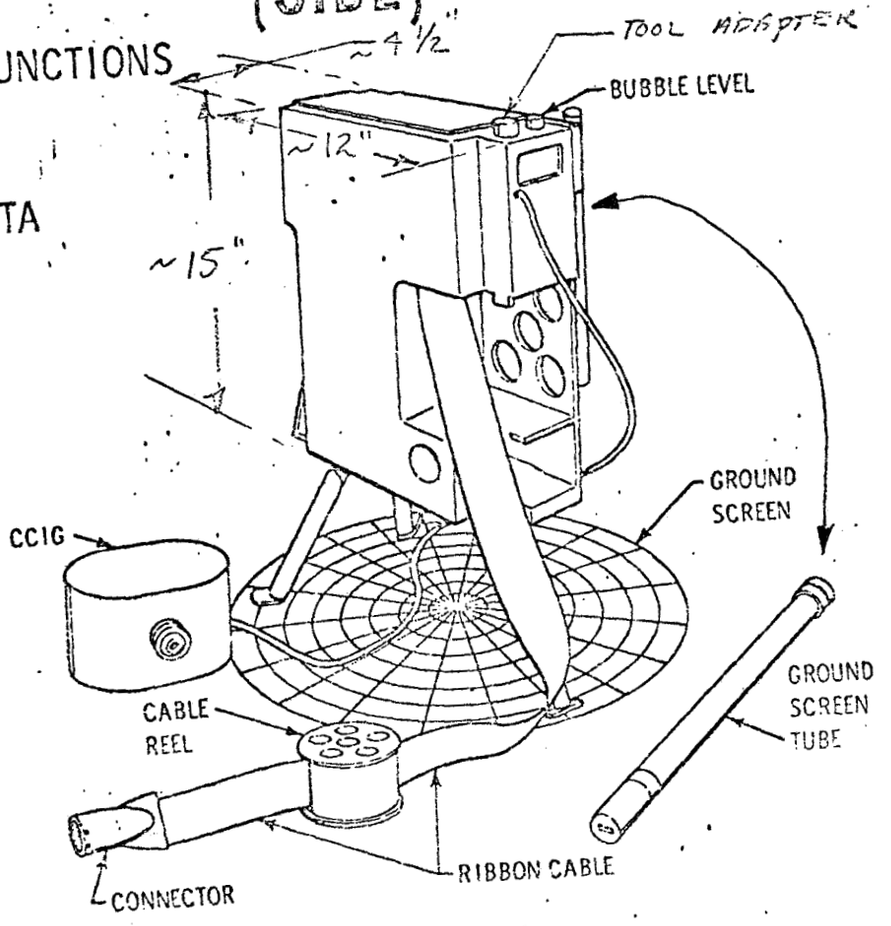


FIG 1.0-7 SIDE/CCGE DEPLOYMENT

ALSEP EXPERIMENT OBJECTIVES

EXPERIMENTS	OBJECTIVES: INTERNAL STRUCTURE & COMPOSITION	STATE OF INTERIOR	COMPOSITION OF ATMOSPHERE	GENESIS OF SURFACE FEATURES
PASSIVE SEISMIC	X	X		X
ACTIVE SEIMIC	X			X
MAGNETOMETER	X	X		X
SOLAR WIND	X		X	X
SUPRATHERMAL ION		X	X	X
HEAT FLOW	X	X		X
CHARGED - PARTICLE			X	

FIG 1.0-8

ALSEP EXPERIMENTS

NASA NO.	EXPERIMENT	PRINCIPAL INVESTIGATOR
S031	PASSIVE SEISMIC	DR. G.V. LATHAM, COLUMBIA
S033	ACTIVE SEISMIC	DR. R.L. KOVACH, STANFORD
S034	MAGNETOMETER	DR. C.P. SONNETT, ARC
S035	SOLAR WIND	DR. C.W. SNYDER, JPL
S036	SUPRATHERMAL ION	DR. J.W. FREEMAN, RICE
S037	HEAT FLOW	DR. M.G. LANGSETH, COLUMBIA
S038	CHARGED - PARTICLE	DR. B.J. O'BRIEN, RICE
S058	COLD CATHODE GAUGE*	DR. F.S. JOHNSON, U OF TEXAS DALLAS
S059	LUNAR FIELD GEOL.**	DR. E.M. SHOEMAKER, USGS

* INCLUDED IN SUPRATHERMAL ION ON CERTAIN FLIGHTS

** EQUIP. PARTIALLY CARRIED BY ALSEP

FIG 1.0-9

SIDE GENERAL FEATURES

MEASURE IONIC ENVIRONMENT OF MOON

DETECT POSITIVE IONS
- RESULTING FROM UV IONIZATION OF THE LUNAR ATMOSPHERE
- FREE STREAMING & THERMALIZED SOLAR WIND

DETERMINED BY CCIG:
- DENSITY OF LUNAR ATMOSPHERE (INC CHANGES WITH TIME)
- RATE LOSS OF CONTAMINANTS LEFT BY ASTRONAUT & LM
- MEASURES DENSITY OF NEUTRAL ATOMS (THIS, WITH TEMP OF GAUGE, ALLOWS CALCULATION OF LUNAR ATMOSPHERE PRESSURE)

HIGH ENERGY CURVED PLATE ANALYZER (HECPA)	LOW ENERGY CURVED PLATE ANALYZER (LECPA)
• NO VELOCITY FILTER • DETERMINES FLUX (PARTICLES/SEC) WITHIN STEPPED RANGES OF ENERGY PER UNIT CHARGE	• PRECEDED BY VELOCITY FILTER (CROSSED ELECTRIC & MAGNETIC FIELDS) • DETERMINES FLUX (PARTICLES/SEC) WITHIN STEPPED RANGES OF VELOCITY & ENERGY PER UNIT CHARGE

- PLACED ON GROUND PLANE (WIRE MESH SCREEN) WITH VOLTAGE APPLIED BETWEEN INSTRUMENT & SCREEN TO ASSESS LUNAR SURFACE ELECTRICAL FIELD EFFECTS
- SIDE ELECTRONICS INPUT CIRCUITS PROVIDE ISOLATION FROM ALSEP (POWER & SIGNAL)

FIG 1.0-10

2.0 PROGRAM HISTORY

2.1 Introduction

The ALSEP/SIDE/CCGE Experiment was designed, fabricated, tested, and delivered by Marshall Laboratories, Torrance, California, under contract to William Marsh Rice University, Houston, Texas. The original contract was executed on 8 June 1966; delivery of the last unit took place in December of 1968.

Designated contract number is S1966-14, under Prime Contract number NAS 9-5911.

The following presentation of program highlights includes a summary of major design and status meetings, design evolution, delivery schedules, problem areas, solutions, and improvements.

2.2 Program Meetings

During the course of the project, numerous program and review meetings were conducted to insure proper continuity of direction, configuration, design, and rework. Various design features and their problems were discussed in these meetings, as well as new designs implemented to further improve the instrument. Progress of the program was periodically reviewed.

Typical of the major design reviews held are the following:

In November of 1966, an ALSEP Preliminary Design Review was held at Bendix Aerospace Systems Division to review the Bendix system design, with emphasis given on the interfaces between the various experiments. Particular attention was given to vibration and shock problems, and to power system interface problems.

A major Experiment Status Review meeting was held at Marshall Laboratories in December, 1966. Major topics included program management, scheduling, staffing, and costing; status of design, fabrication, parts procurement, and other technical aspects of the program were discussed in depth.

Typical of the Program Review Meetings was the meeting held at Marshall Laboratories in June, 1967. Design status was reviewed including electrical, thermal, and mechanical design features. Costs and schedules were analyzed in depth. In addition to Rice University and Marshall Laboratories participants, attendees included representatives from NASA/MSC, SCAS and Bendix Corporation.

The Critical Design Review (CDR) was conducted at Marshall Laboratories in August, 1967. The purpose of the meeting was to cover problem areas brought to light by the engineering and prototype models. The CDR also set up as a baseline for configuration control. Various faults and virtues of the experiment design

were discussed, and recommendations for further improvements were introduced. The presentations covered both the electrical and mechanical aspects of the equipment. A major ALSEP Interface Meeting was held at Bendix in September (1967), with the Principal Investigators of each ALSEP experiment in attendance. Topics of interest were organizational status reports, overall schedule status, accomplishments to date, and problem areas.

Another major Program Review Meeting took place at Rice University in February of 1968. Items reviewed were the CCGE status (including fabrication, delivery schedule, and calibration). SIDE status and discrepancy reports were covered in addition to interface and technical problem areas. Astronaut deployment problems were reviewed.

The foregoing were typical of the main review meetings which were held periodically to insure smooth progress of the program and successful attainment of its goals.

2.3 Design Evolution

The initial design concept of the experiment was an extension of the Suprathermal Ion Experiment for the Advanced Technology Satellite (ATS) - B spacecraft, with the addition of a crossed field analyzer to serve as a velocity filter. This concept was later modified to include a second detector to measure higher energy ions, with open retarding grids for particle deflection. The addition of the CCGE experiment was anticipated early in the program but parameter definitions and corresponding contractual documentation were not available until after the preliminary design phases of the program.

Significant design changes were introduced which produced a radically different instrument than that originally conceived, making it much more valuable as a scientific instrument. These changes were implemented successfully in spite of demanding schedule requirements. With an intensive design effort, Marshall Laboratories succeeded in producing a complex, highly sophisticated instrument incorporating over 500 transistors and a similar number of integrated circuits.

A summary review of the major design changes follows:

Instead of the proposed time-shared retarding potential analyzer system with a 39 bit digital readout, the design of the instrument evolved into two simultaneously operating curved plate analyzer ion detectors with 100-bit digital readout. As mentioned previously, the Cold Cathode Gauge was incorporated including a separate +4.5 kV power supply and a five decade multi-ranging electrometer. The CCGE sensor had a major impact on form factor and thermal design constraints. The original velocity filter concept was to sequentially step

through one to five different energies in order to gather data in each of the selected velocity bands. The velocity filter redesign incorporated sequencing steps which tracked a parabolic curve of voltage versus time. This introduced many additional voltage steps with a corresponding increase in design complexity.

During the design of the ALSEP Experiment, it was suggested that a backup (analog) data link be established between the experiment and the analog signal processing circuitry of the ALSEP. Rice University agreed that the addition of this circuitry was a benefit to the experiment and authorized the addition of the log count rate meters to the experiment design. In effect, the addition of this circuitry improved total system reliability by providing a redundant, though less precise, path around much of the circuitry of the instrument.

The decision to include a magnetic shield for the CCIG had considerable impact upon weight problems and subsequent weight reduction efforts. Similarly, a larger size cable reel for the flat-tape cable resulted in problems involving weight and thermal control considerations.

These challenges were met in major mechanical and thermal redesign efforts to produce an instrument which would survive the specified environmental design constraints. Refer to Section 7.0 for details on mechanical and thermal design.

2.4 Test and Delivery Schedules

Successful integration of the experiment breadboard with the breadboard ALSEP Central Station was accomplished at Bendix Systems Division in December, 1966. Interface tests on the CCIG with the electrometer and high voltage power supply breadboards were performed the following month at NRC, Boston, Massachusetts. Acceptance tests for the SIDE and CCGE breadboards, were conducted in February, 1967. At this time, ETS (Experiment Test Set) acceptance tests were also performed. All test objectives were satisfactorily completed.

Severe schedule pressure characterized much of the program's activities. This was necessitated by the need to conform to overall ALSEP Program schedule requirements. Early in 1968, an incentivized redefinition of the contract provided for a new delivery schedule in which delivery of instruments would be accomplished at six week intervals. Marshall Laboratories successfully met all schedules and thus qualified for the incentive fee as provided for in the modified contract.

The following is a brief summary of the required delivery dates for incentivized purposes and actual delivery dates.

System	Incentivized Contractual Delivery Date	Actual Delivery Date	Remarks (See Section 2.5 for details)
ML322-1 (Engineering Model 1)	N/A	May 1967	Shipped with authorized tolerance discrepancies
ML322-2 (Engineering Model 2, prototype)	N/A	July 1967	
ML323-1 (Qual Model 2)*	N/A	Sept. 1967	HV arcing at Rice, Nov. 1967
ML323-2 (Qual Model 1) (Flight 1)	N/A	Jan. 1968	HV arcing, Feb. - March 1968 at Rice
ML323-3 (Flight 2)	April 1968	March 1968	-3.5KV and Elect. problems at Rice
ML323-4 (Flight 1) (Spare)	May 1968	May 1968	
ML323-5 (Flight 3)	July 1968	July 1968	
ML323-6 (Qual. 2)	August 1968	August 1968	
ML323-7 (Flight 3) (Spare)	Sept. 1968	Sept. 1968	
ML323-8 (Flight Spare)	Nov. 1968	Nov. 1968	
ML323-9 (Flight Spare)	Dec. 1968	Dec. 1968	

See Appendix III for a system test procedure and typical test results.

* The Qualification Model No. 1 instrument had been reidentified as Qualification Model No. 2. Therefore all data acceptance documentation prior to 2 January 1968 referenced to Qualification Model No. 1 is now applicable to the re-identified Qualification Model No. 2 instrument.

Two Astronaut Training Units (ATU) were developed and delivered to the customer. The ATU's provide a means for accurate physical simulation of the actual instrument. The development of the ATU's was influenced by human interface requirements involving the astronauts' training needs.

ATU serial number 1 was completed and shipped to Bendix in May of 1967. It was subsequently returned to Marshall Laboratories for modifications in September, 1967. After updating, ATU No. 1 was then shipped to MSC in December of the same year.

ATU No. 2 was completed and delivered in February, 1967.

2.5 Problem Areas and Solutions

Engineering Model 1 (EM 1, ML 322-1), was tested and shipped with minor tolerance discrepancies due to non-screened, lower precision substitute components used in the system. These lower precision parts were authorized for EM 1, a non-flight configuration, and applied only to EM 1. Blivet 800 (see Sect. 3.0 for description) not in final configuration, was to be retrofitted at a later date, as was the 700 Blivet.

A failure was observed in the instrument ML 323-1 during tests at Rice University in November of 1967. Failure occurred when the + 4.5 kV power supply was turned on in the vacuum chamber (at pressure of 2×10^{-6} torr). All negative power supply voltage readings were 255 (on ETS data display readout unit) except for the -5 volt supply. All internal temperatures read out 000.

The problem was traced to damage caused by high voltage arcing. Rerouting of critical ground connections and the addition of arc protective devices in the applicable modules corrected the problem. The -3.5 kV high voltage to the channeltrons was originally an independent connection from the 700 blivet. It now encompasses two connections, one from the 700 blivet to the low energy channeltron and one connecting the low energy channeltron to the high energy channeltron. Refer to Engineering Change Proposals (ECP) 116 through 122 (Appendix III). The instrument was shipped back to Rice University in December.

Qual Model 1, ML 323-2 was returned to Marshall Laboratories in February 1968 for the following repairs and modifications:

- Installation of Ground Screen Spring
- Installation of Latch Pin Lanyard
- Modification of CCIG Lanyard Wire to Stainless Steel Wire
- Retrofit Dust Cover Springs
- Addition of two (2) Apertures to LECPA

- Addition of two (2) Pole Straps to LECPA Magnet Assembly

- Repair of 600 Blivet Assembly to Correct the Following Conditions:

  a) Temperature Monitor No. 6
  b) -3.5 kV Arcing
  c) -3.5 kV Monitor

- Repair of 700 Blivet Assembly to Correct the Following Conditions:

  a) -3.5 kV Monitor
  b) 4.5 kV Command Sequence
  c) -3.5 kV Arcing

Refer to ECP's 187 and 188 for changes involving protective circuitry to prevent damage due to high voltage arcing (Appendix III).

This instrument was retested and shipped to Rice University in March, 1968.

In the same month, ML 323-2 (Qual Model 1) was subjected to massive high voltage arcing and the instrument was returned to Marshall Laboratories. Investigation showed damage to a number of modules due to the arcing. Various changes were initiated to prevent further failures of this type. Refer to ECP's 210 and 218 (Appendix III). The instrument was repaired, final tested, and returned to Rice University in April, 1968.

The Qual Model spare (ML 323-3) was final tested and shipped to Rice University in March (1968). During system vacuum tests at Rice, the -3.5 kV supply would turn on and off intermittently. An electrometer failure was also observed, apparently due to a ground loop problem in the Rice University system test configuration. After the instrument was returned to Marshall Laboratories, repairs were performed on the equipment; final re-test and shipping occured in May.

In April, 1968, instrument number ML 323-1 (Qual Model 2) reportedly exhibited a power short during tests at Bendix. The instrument was subsequently returned to Marshall Laboratories.

Upon receipt of the SIDE/CCGE instrument at Marshall Labs, a thorough investigation of the reported power short was performed. A variety of turn on sequences and operations were tested in addition to physical movement of the package and associated cables. It was impossible to induce a short circuit failure. After disassembly of the instrument, a visual inspection of potential areas of short circuits was performed and no defects were found.

ML did not have a suitable adapter cable to test the instrument in the same cable configuration as at Bendix. From the evidence provided, it appeared that a short circuit existed at the power input to the instrument due to an intermittent condition in either the SIDE/CCGE, the ETS, the cables, or cable connectors. From the information provided, it was not possible to isolate the particular cause of the short.

During vacuum tests of ML 323-1 at Bendix in August (1968), the environmental chamber had a port window implode, resulting in loss of vacuum and causing oil to spew over the instrument. Debris was also thrown on the instrument due to this port failure. During the time of the implosion, the SIDE high voltage was on, causing damage of an A/D converter. The instrument was subsequently returned to Marshall Laboratories, and was repaired and shipped out in September, 1968.

In summary, the major problems associated with early systems were damages resulting from high voltage arcing. Investigations concluded that arcing resulted from a combination of circumstances including insufficient gap distances, outgassing, improper cable routing in test chamber, etc. These problems were subsequently corrected and the SIDE/CCGE circuitry was modified to provide a greater degree of arc protection to sensitive circuits. The success of these efforts is evidenced by the virtual elimination of arc damage during tests conducted on later systems after Serial Number 4.

3.0 EXPERIMENT DESCRIPTION

This section describes the overall operation of the SIDE and CCGE experiments. A general description of the experiment, plus references to the appendix of typical test procedures and results, design notes, and other pertinent data is included in this and other appropriate sections.

Physically, the SIDE/CCGE experiment consists of three major sections:

a) Sensors
b) Electronics
c) Housing

The sensors portion includes the Low Energy ion detector, the High Energy ion detector, and the Cold Cathode Ion Gauge (CCIG). The electronic portion consists of nine subassemblies or blivets numbered 100 to 900 and two channeltron preamplifiers. The housing portion is in two parts - the internal chassis and the external chassis (Refer to Section 7.0 - Mechanical and Thermal Design). The internal chassis contains the sensors and the electronics, while the external chassis provides protection and thermal insulation to the internal chassis assembly. Each subassembly, or blivet, is tested in house over the applicable temperature range.

The following is a summary of the SIDE/CCGE subassemblies (blivets) and their major functions:

a)	Blivet 100	Logic Timing, Command System, Strobe Gates, SIDE Frame Counter, Accumulators.
b)	Blivet 200	A/D Converters, ALSEP/SIDE Interface Networks, Logic Timing, Sub-commutators, CCGE Cal Command Generator, Dust Cover Removal Circuit, Cal Dividers
c)	Blivet 300	Step Voltage Counters & Generators, Cal Pulse Generator
d)	Blivets 400/ 500	Low Voltage Power Supply
e)	Blivet 600	Cal Shapers, Deadtime Circuits, Log Count Rate Meters, -3.5 kV Regulator
f)	Blivet 700	-3.5 kV Converter & Multiplier, 4.5 kV Multiplier and Output Divider

g)	Blivet 800	Electrometer for CCGE
h)	Blivet 900	4.5 kV Regulator and Converter, Electrometer Range Relay Drivers & Power Supply, CCGE Seal Break Circuit

See Section 7.0 Mechanical and Thermal Design, for the physical configuration of the blivets within the experiment package.

Since the experiment is thermally insulated and heated by an automatic heater control circuit, it will operate throughout the range of the lunar temperatures (-157^{o}C to $+121^{o}$C) while the temperature inside the unit is maintained between -10^{o}C and $+60^{o}$C.

Electrically, the system is completely isolated from the ALSEP to achieve an ideal floating ground configuration. The direct-current isolation resistance is greater than 10 MΩ. The isolation voltage is greater than ± 50 volts.

A Ground Plane screen is placed beneath the instrument as it is deployed on the lunar surface (See Figures 1.0-2, 1.0-3 and 1.0-7, and Section 7.1.8). A stepped voltage is applied to the Ground Plane to modify the ambient lunar surface potential.

The system is linked to the ALSEP Central Processing Station by a flat-tape cable. Power, commands, timing signals, and data are transmitted through this cable.

Refer to the following figures for the system block diagram and data formats:

a)	Figure 3.0-1,	Simplified Block Diagram, SIDE/CCGE Experiment
b)	Figure 3.0-2,	SIDE/CCGE Operational Diagram
c)	Figure 3.0-3,	A/D & Status Sub-Com Sequence
d)	Figure 3.0-4,	Data Format

Functionally, the instrument consists of four major portions: a) a low energy ion detection system, b) a high energy ion detection system, c) the CCGE, and d) the support electronics. Provisions are also made for in-flight calibration. A calibration pulser drives through logic controlled by the Master Timing Generator (SIDE Frame Counter and associated logic timing circuits), and provides calibration signals to the Channeltron Preamplifiers during the experiment's calibration cycle.

ALSEP COMMAND SUB-SYSTEM

POWER LINES

COMMAND LINES

EXECUTE COMMAND LINE

SHIFT PULSE, FRAMEMARK & EVEN FRAMEMARK LINES

DATA OUTPUT

LOW VOLTAGE POWER SUPPLIES

INPUT ISOLATION AMPS

ONE TIME REGISTER

ONE TIME COMMANDS

COMMAND INPUT REGISTER

MODE REGISTER

COMMAND DECODER

COMMANDS

EXECUTE GATE

LOGIC TIMING

ADV

SYNC

HE COUNTER N/20

VEL FIL CTR N/20

LOW ENERGY COUNTER N/6

G.P. COUNTER N/23

GROUND PLANE STEP VOLTAGE GENERATOR

HIGH ENERGY CPA STEP VOLTAGE GENERATOR

LOW ENERGY CPA STEP VOLTAGE GENERATOR

VEL FILTER STEP VOLTAGE GENERATOR

PARITY GENERATOR

STATUS SUBCOM

GP CALIBRATE

ELECTROMETER RANGE

DC + SPECIAL

MR

CTR

SIDE FRAME COUNTER

14 LINES

A/D CONVERTERS

HOUSEKEEPING ANALOG DATA

STROBE GATE

OUTPUT ISOLATION AMP

DATA OUTPUT TO ALSEP

CAL

SIDE

DISC

LCRM

ALSEP A/D

HIGH ENERGY ACC.

LOW ENERGY ACC.

FROM VEL FILTER STEP VOLTAGE GENERATOR

FROM L.E. CPA STEP VOLTAGE GENERATOR

FROM HE CPA STEP VOLTAGE GENERATOR

FROM GP STEP VOLTAGE GENERATOR

VEL FILTER

3.5KV

GROUND PLANE

CCIG P.S.

CCIG

CALIBRATION CURRENT GEN

ELECTROMETER

TO A/D COMMUTATOR

SHIFT PULSES FROM LOGIC TIMING

N/O

FIGURE 3.0-1 Simplified Block Diagram, SIDE/CCGE Experiment

Figure 3.0-2. SIDE/CCGR Operational Diagram.

0	GPS	8	GPS	16	GPS	24	GPS	32	GPS	40	GPS	48	GPS	56	GPS	64	GPS	72	GPS	80	GPS	88	GPS	96	GPS	104	GPS	112	GPS	120
	4 VOLTS ANALOG		4.5 KV		5 VOLTS		4 VOLTS ANALOG		4.5 KV		+60 VOLTS		CCGE RANGE		5 VOLTS ANALOG		4.5 KV		+60 VOLTS		CCGE RANGE		5 VOLTS ANALOG		4.5 KV		+60 VOLTS		CCGE RANGE START POINT ADDR
1	CIR	9	ELECTROMETER RANGE	17	CCGE	25	ELECTROMETER RANGE	33	CCGE	41	ELECTROMETER RANGE	49	CIR	57	ELECTROMETER RANGE	65	ELECTROMETER RANGE	73	CCGE	81	CIR	89	ELECTROMETER RANGE	97	CIR	105	ELECTROMETER RANGE	113	CIR	121
	CCGE		CCGE		+30 VOLTS		+3C MV CAL		CMD TIME COMMAND RLY STATUS		+30 VOLTS		CCGE		PRE-REG DUTY FACTOR		CCGE		+3C VOLTS		+3C +1V CAL		CMD TIME COMMAND REG/STR STATUS		CCGE		+30 VOLTS		CAL RATE 2
2	GPS	10	GPS	18	GPS	26	GPS	34	GPS	42	GPS	50	GPS	58	GPS	66	GPS	74	GPS	82	GPS	90	GPS	98	GPS	106	GPS	114	GPS	122
	TEMP #1		CCGE RANGE RESET PULSE		+5V DIGITAL		+A/D REF VOLTS		TEMP #1		+5V D DIGITAL		+A D REF VOLTS		TEMP #1		CCGE RANGE		+5 VOLTS DIGITAL		+A/D REF VOLTS		DUST COVER & SEAL		CCGE RANGE		+5V DIGITAL		CAL RATE 3
3	MR	11	MR	19	MR	27	MR	35	MR	43	MR	51	MR	59	MR	67	MR	75	MR	83	MR	91	MR	99	MR	107	MR	115	MR	123
	CCGE		TEMP #4		GND		+1V CAL		CMD TIME COMMAND RESISTOR VOLTS		TEMP #4		+1V CAL		DUST COVER & SEAL		TEMP #4		GND		+1V CAL		CMD TIME COMMAND RESISTOR VOLTS		TEMP #4		GND		CAL RATE 4
4	GPS	12	GPS	20	GPS	28	GPS	36	GPS	44	GPS	52	GPS	60	GPS	68	GPS	76	GPS	84	GPS	92	GPS	100	GPS	108	GPS	116	GPS	124
	TEMP #6		-5 VOLTS		+12 V CAL		TEMP #5		TEMP #2		-5 VOLTS		+12 V CAL		TEMP #2		-5 VOLTS		TEMP #5		+12 V CAL		TEMP #3		TEMP #5		-5 VOLTS		CAL RATE 1
5	CIR	13	CIR	21	CCGE	29	CIR	37	CIR	45	CIR	53	CIR	61	CIR	69	CIR	77	CIR	85	CIR	93	CIR	101	CIR	109	CIR	117	CIR	125
	CCGE		-30 VOLTS		+12 V CAL		TEMP #2		-30MV CAL		TEMP #6		-30 VOLTS		TEMP #3		SOLAR CELL		TEMP #6		-A/D REF VOLTS		TEMP #3		-30MV CAL		TEMP #6		CAL RATE 5
6	GPS	14	GPS	22	GPS	30	GPS	38	GPS	46	GPS	54	GPS	62	GPS	70	GPS	78	GPS	86	GPS	94	GPS	102	GPS	110	GPS	118	GPS	126
	TEMP #3		SOLAR CELL		-A/D REF VOLTS		TAPE #3		-30MV CAL		TEMP #6		-3.5 KV		TEMP #3		SOLAR CELL		TEMP #6		-A/D REF VOLTS		TEMP #3		-30MV CAL		TEMP #6		CAL RATE 6
7	DUST COVER & SEAL	15	MR	23	MR	31	MR	39	DUST COVER & SEAL -12V CAL	47	MR	55	MR	63	MR	71	DUST COVER & SEAL	79	MR	87	MR	95	MR	103	DUST COVER & SEAL -12V CAL	111	MR	119	MR	127
	CCGE		GPV		GPV		-3.5 KV		RESET POINT MODE 3		-3.5 KV		-12V CAL		RESET POINT MODE 2		GPV		-3.5 KV		GPV		-12V CAL		GPV		-3.5 KV		CAL RATE 4

Figure 3.0-3. A/D and Status Sub-com Sequence.

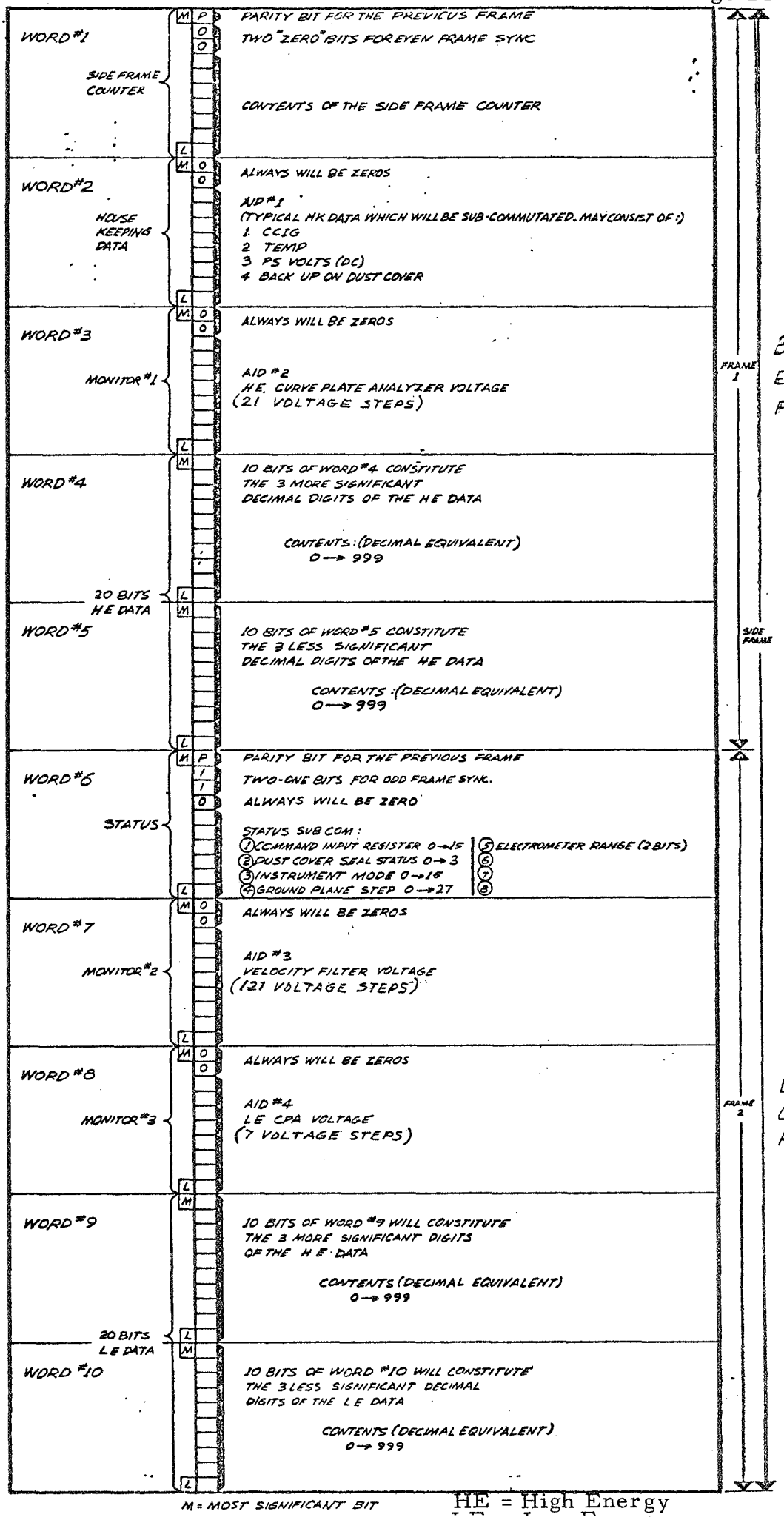


FIGURE 3.0-4 Data Format

M = MOST SIGNIFICANT BIT

HE = High Energy

Appendix II shows the Master Drawing List for the SIDE/CCGE.

Shown in Appendix III is the test procedure for the SIDE/CCGE experiment, along with typical test data sheets and results.

3.1 Low Energy Ion Detection System

The purpose of the Low Energy (LE) Ion Detection System is to detect positive ions with masses up to 130 AMU, and to measure the differential energy spectrum of ions in a narrow velocity range having energies from 0.2 ev to 48.6 ev per unit charge.

Positive ions enter an aperture and pass into a Wein Velocity Filter (crossed electric and magnetic fields) which will pass only those ions in a narrow velocity range. The surviving ions then enter an electrostatic Curved Plate Analyzer (CPA) which will pass only those ions in the energy range mentioned above.

The ions passing through the Low Energy CPA are then focused on a Channeltron Electron Multiplier. (See Section 7.0, Mechanical and Thermal Design, for description of the Channeltron multiplier). Each ion, after multiplication by secondary emission of electrons within the coated glass walls of the tube, causes a negative going pulse at the input of a stable, high gain, wide-band amplifier (Channeltron Preamplifier). Output of the Channeltron Preamplifier drives the discriminator/deadtime circuit, whose function is to shape the incoming narrow pulse into a 0.4 μsec pulse, and to limit the maximum frequency to approximately 1 MHz.

The discriminator/deadtime circuit then feeds the Low Energy Accumulator, which temporarily stores the number of ions sensed during each SIDE Frame, and the Log Count Rate Meter (LCRM). Information stored in the accumulator is then read out to the ALSEP Central Station for transmission. After each readout, the accumulator is cleared in preparation for new data. The LCRM produces a dc voltage proportional to the log of the input count rate. Output of the LCRM feeds the ALSEP Central Station Analog-to-Digital Converters.

The master timing generator provides sequencing information to a Velocity Filter (VF) Step Voltage Generator and a Low Energy (LE) Step Voltage Generator. The LE Step Voltage Generator effects energy resolution by supplying a stepped, balanced potential on each plate of the LE CPA. Six voltage levels in the range of 0.1 V to 24.3 V plate-to-plate, are generated to achieve the required energy ranges. The VF and LE voltages are monitored by the Analog to Digital (A/D) Converters and are transferred as digital information through the Strobe Gates to the readout system.

Mass resolution is achieved in the detector with a constant magnetic field and a stepped electric field. Magnetic field strength is approximately 900 Gauss. The VF Step Voltage Generator supplies a stepped, balanced potential to the two parallel electric field plates. 120 voltage steps, in the range of 0.12 V to 28 V plate-to-plate, are generated.

Table 3.1A shows the six energy levels. Twenty voltage levels are thus generated for each energy level.

Energy Step	Energy (eV)
1	48.6
2	16.2
3	5.4
4	1.8
5	0.6
6	0.2

TABLE 3.1A: Energy Levels, Low Energy Ion Detector

3.2 High Energy Ion Detection System

The High Energy (HE) Ion Detection System detects all positive ions regardless of mass, and measures the differential energy spectrum of ions having energies from 10 eV to 3500 eV per unit charge.

Positive ions enter an aperture and pass into the High Energy electrostatic Curved Plate Analyzer. The ions detected pass into the HE Channeltron Electron multiplier. The data path is then identical to that of the Low Energy detection system, employing a separate, identical channel of amplifier, discriminator/deadtime circuit, LCRM, and accumulator. The HE plate voltages are similarly monitored by the A/D Converters and read out as digital data.

The master timing generator sequences the HE Step Voltage Generator, which supplies a stepped, balanced potential on each plate of the CPA to achieve energy resolution. Twenty voltage steps, in the range of 2.5 V to 875 V plate-to-plate, are generated to select the desired energy steps. Table 3.2A shows the energy levels for each HE step.

TABLE 3.2A: Energy Levels, High Energy Ion Detector

Step Number	Energy (eV)
1	3500
2	3250
3	3000
4	2750
5	2500
6	2250
7	2000
8	1750
9	1500
10	1250
11	1000
12	750
13	500
14	250
15	100
16	70
17	50
18	30
19	20
20	10

3.3 Cold Cathode Gauge Experiment

The Cold Cathode Gauge Experiment (CCGE) determines, a) the density of any lunar ambient atmosphere corresponding to pressures of 10^{-6} torr to approximately 10^{-12} torr, including any temporal variations either of a random character or associated with lunar local time or solar activity, and b) the rate of loss of contaminants left in the landing area by the astronauts and the Lunar Module (LM).

Refer to Figure 3.3-1 for the block diagram of the CCGE experiment.

The CCGE consists of the following subassemblies:

a) Electrometer

b) Sensor (CCIG)

c) Seal Mechanism Power Supply

d) Seal Mechanism

e) 4500 Volt Power Supply

f) Temperature Sensor & Monitoring Circuit

The gauge is sealed and pumped down to a pressure of 10^{-7} torr or lower. A break-off device is provided to open the seal and expose the sensor to the lunar environment. The seal will not be broken until after the (LM) has left the lunar surface.

A lock-out plug, removed prior to launch, prevents accidental breaking of the seal during ground tests.

3.4 Support Electronics

3.4.1 Power

There are two power lines for the system: a) Operating Power and b) Survival Power. Both lines come from a single +29 volt power source within the ALSEP. When operating power is ON, the system is in an operative mode in which the instrument performs all its functions and collects data for the Central Station. When survival power is ON, the system will be in a survival mode in which only the heater control circuit is operative. Under no circumstances are both lines ON simultaneously.

When operating power is ON, +29 volts is supplied to the Low Voltage Power Supply. The Low Voltage Power Supply then provides the dc voltages required to operate the system, as well as two 4 kHz, ± 5V squarewaves required to drive the High

PARTS DISPOSITION	DWG NO.	REV
1. USE 2. REWORK 3. CANNOT BE REWORKED 4. RECORD 5. ____	609234	

REVISIONS

DISP	EFF	ZONE	REV	DESCRIPTION	BY	CK	DATE	APPROVAL

375 → +5V ANALOG
376 → +5V RETURN
381 → +60V CURRENT SOURCE
382 → +60V RETURN

377 → SIDE LOW VOLTAGE POWER SUPPLY
379 → SIDE LOW VOLTAGE POWER SUPPLY

+30V DC
-30V DC
ELECTROMETER POWER SUPPLY 609150 DS
+8V DC
+25V DC REGULATED
± 5 VDC
AUTO ZERO COMMAND
AUTO ZERO CKT 609150 DS

378 → ELECTROMETER GRD (A/D REF GRD)
374 → POWER RETURN

CALIBRATE COMMANDS

LINE# 589 & 590 → CAL CURRENT 1 (READ ZERO, SIDE FRAME 120)
LINE# 327 → CAL CURRENT 2 (CORRECT ZERO 121 & 122)
LINE# 328 → CAL CURRENT 3 (SIDE FRAME 124 & 125)
LINE# 329 → CAL CURRENT 4 (SIDE FRAME 126 & 127)

± 30 VDC
± 5 VDC
CURRENT CALIBRATOR 609151 DS
INPUT FILTER
MODE SELECTOR 609150 DS
ZERO
INPUT
GRD
ELECTROMETER AMPLIFIER 609150 DS

377 → +30VDC
392 → +30V RETURN
+4500 VPS 609153 DS
RIPPLE ± 2.2 V MAX
580 → POWER ON-OFF
AID COMMAND
ETS
1364 → LOCK-OUT
1365 → LOCK-OUT
+8VDC
497 → BREAK SEAL COMMAND
134 → SEAL BREAK POWER SUPPLY
SENSOR CASE GRD
ANODE
CATHODE
CCIG
SEAL MECHANISM
TEMPERATURE SENSOR
CCGE DETACHABLE SECTION 609155DS
+28V DC REGULATED
TEMPERATURE SENSOR CURRENT SOURCE
A/D REF GRD (378)
ETS
657 → A/D CONVERTER CCGE TEMPERATURE READOUT
RANGE 1
RANGE 2
138 → ELECTROMETER DIGITAL RANGE READOUT
654 → ELECTROMETER ANALOG RANGE READOUT TO A/D CONVERTER
→ ELECTROMETER OUTPUT TO A/D CONVERTER
+8V DC
± 5 VDC
AUTO RANGE CKT 609150 DS

Figure 3.3-1. CCGE Block Diagram.

NOTES: UNLESS OTHERWISE SPECIFIED

PART NO.	SPECIFICATION	NOMENCLATURE OR DESCRIPTION	SUG. REP. QTY	CODE IDENT	ZONE	ITEM NO.

LIST OF MATERIALS

QTY REQD PER NOTED ASSY
CONFIGURATION
LAYOUT NO.
NEXT DWG 6-090 A-H

INTERPRET THIS DRAWING PER STANDARDS IN MIL-D-70327
DIMENSIONS ARE IN INCHES
TOLERANCES ON
DECIMALS X ± .1, XX ± .03, XXX ± .005
ANGLES ± 0° 30'
XXXX ± .0005
✓ SURFACE ROUGHNESS
HOLE DIA. TOLERANCE

CONTRACT NO. S1966-IH
DRAWN F. Lentz 27 JULY 66
CHECK
ENGR APPR. L. Levine 7-10-67
PROJ ENGR C. Bellington 7-10-67
APPR.
QUALITY APPR.
MFG APPR.

MARSHALL LABORATORIES
TORRANCE, CALIFORNIA

TITLE
CCGE EXPERIMENT
BLOCK DIAGRAM
SYSTEM IV

SIZE D | CAGE CODE NO. 13124 | DWG NO. 609234 | REV

SCALE | WEIGHT | SHEET 1 OF 1

Energy modulator. A Duty Cycle Monitor supplies a voltage inversely proportional to the Low Voltage Power Supply input voltage. This provides a means of checking the condition of the input voltage.

A -3.5 kV power supply and a +4.5 kV power supply provide, respectively, a bias potential for the Channeltron Electron Multipliers and the anode voltage for the Cold Cathode Ion Gauge (CCIG). During tests at ambient air pressures, the lockout plug inhibits operation of the high voltage supplies.

3.4.2 Logic Timing: Command System

Timing signals are furnished by the ALSEP Central Station to control the demand and synchronization of data. These timing signals and their functions are:

a) Shift Pulse - controls the rate at which data is transferred.

b) Data Demand - a logic level which causes the readout of the experiment data registers.

c) Even Frame Mark - a short duration pulse used to synchronize the SIDE frame counter in the experiment.

Within the experiment, an internal timing system (master timing generator) controls the programming of the calibration system, the step voltage generators, and the synchronization and processing of data and commands. See Figure 3.4.2-1 for the timing diagram of ALSEP timing signals. Figures 3.4.2-2, 3.4.2-3 and 3.4.2-4 show the timing relationships between ALSEP and SIDE/CCGE timing signals.

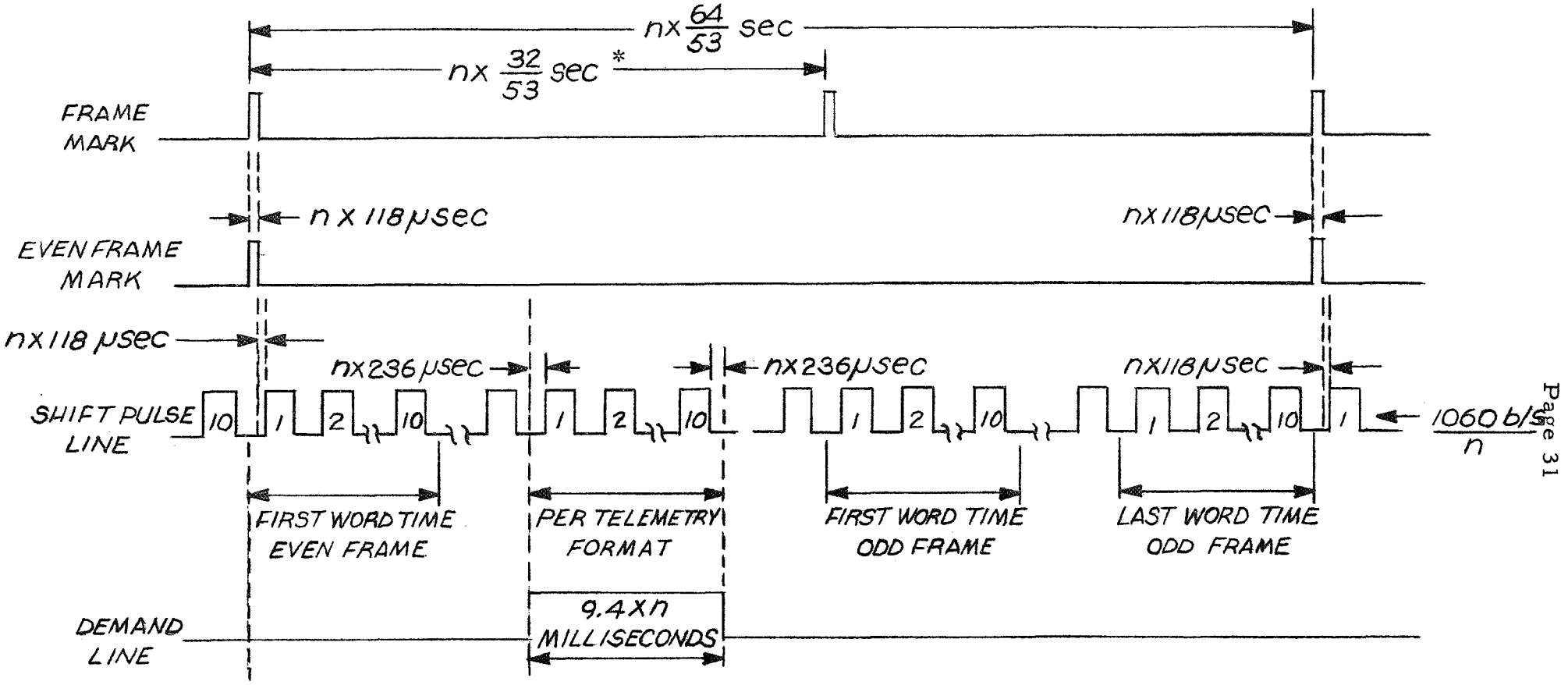
All IC's used in logic circuits in this system are of the Fairchild flat-package type DTμL:

- o 933 Dual Four Input Extender Element
- o 9040 Clocked Flip Flop
- o 9041 Dual Three Input Nand Gate
- o 9042 Dual Three Input Nand Gate with Extender Inputs

See Appendix I for pertinent data sheets on the applicable Fairchild IC's.

Logic levels used by Fairchild IC's in the system are defined as follows:

- o Logic "1" = 4.7 V ± 0.3V (unloaded)
- o Logic "0" = 0.1V ± 0.1V



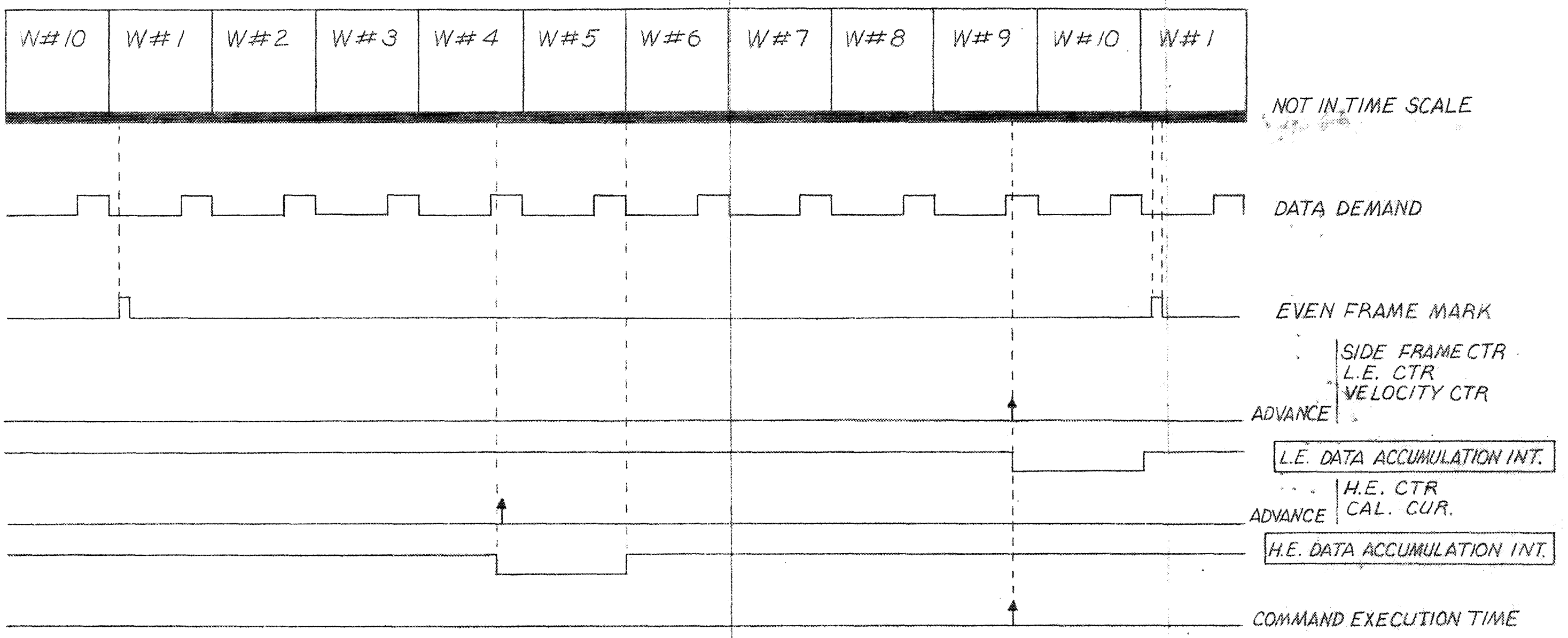
n = 1 for normal mode of 1060 B/S

n = 2 for slow mode of 530 B/S

Data Processor Reads Data at Positive going Edge of Shift Pulse

* $\frac{32}{53}$ sec = $\frac{640 \text{ bits/frame}}{1060 \text{ bits/sec}}$ All other times are accurate only to the significant figure shown.

FIG 3.4.2-1, ALSEP TIMING SIGNALS

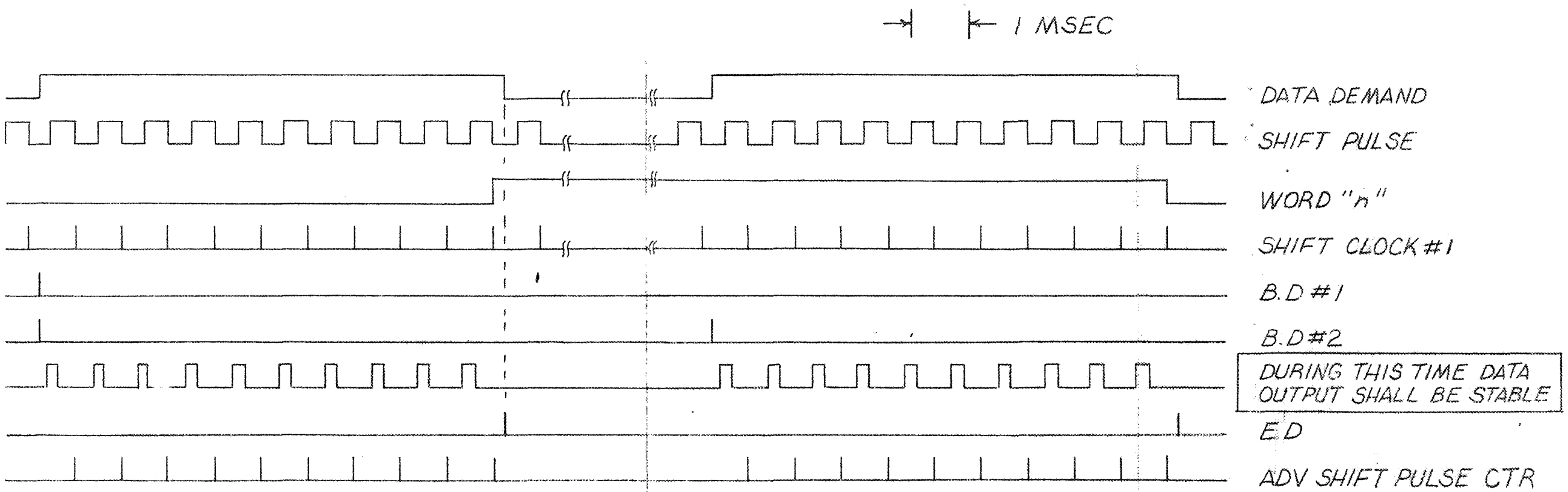


NOT TO SCALE

(REF. DRAWING NUMBER SK607715, LOGIC TIMING)

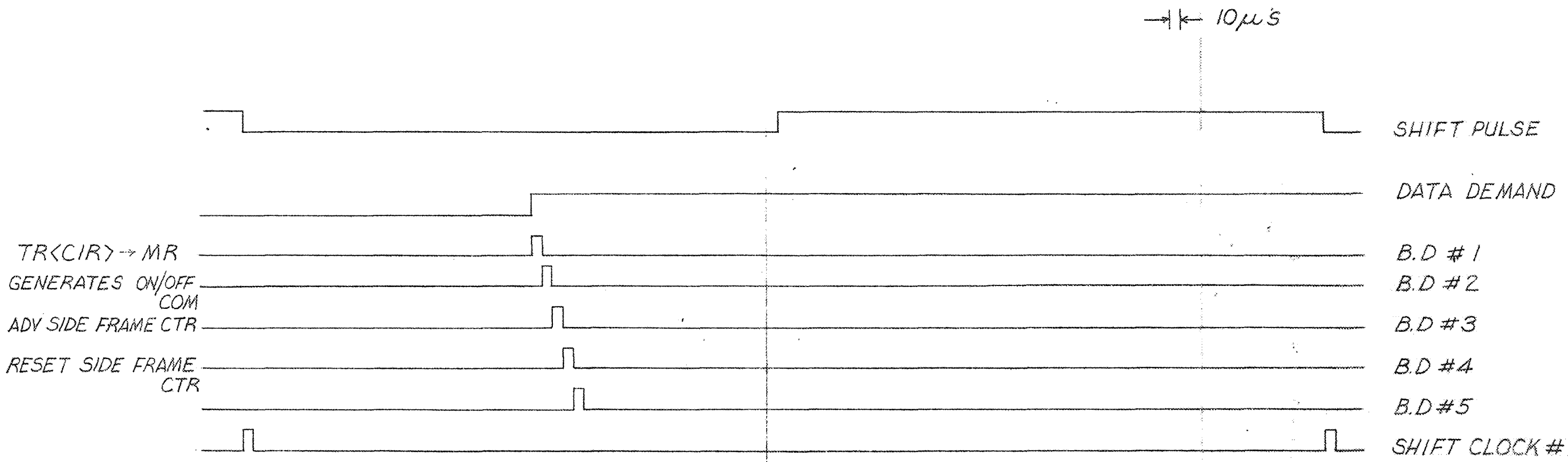
FIGURE 3.4.2-2
ALSEP/SIDE/CCGE
TIMING SIGNALS

DD	SP
9.4 MS	1060 BPS
.94 MS	10600 BPS



(REF DRAWING NUMBER SK609715, LOGIC TIMING)

FIGURE 3.4.2-3
ALSEP/SIDE/CCGE
TIMING SIGNALS



(REF DRAWING NUMBER SK609715, LOGIC TIMING)

FIGURE 3.4.2-4
ALSEP/SIDE/CCGE
TIMING SIGNALS

The command system receives any combination of four commands, decodes the combination and executes (upon command) the internal function designated by the command combination. Commands are decoded but not executed until an "Execute" command is generated.

The first execution of a command containing Command B causes the CCIG seal to break. The first execution of a command containing command D causes the Dust Cover to open.

See Table 3.4.2A for a summary of the SIDE/ CCGE commands and their functions.

TABLE 3.4.2: ALSEP COMMAND TABLE

One-Time Command No.	Repeatable Command No.	Command Name
2		Break CCIG Seal
8		Blow Dust Cover
	1	Ground Plane Stepper ON/OFF
	2	Solar Wind/CCIG (Reset SIDE Frame Counter at 10)
	3	16.2 eV to 48.6 eV (Reset SIDE Frame Counter at 39)
	4	AMU < 20 (Reset Velocity Filter Counter at 9)
	5	eV > 0.6 only (Reset SIDE Frame Counter at 79)
	6	AMU < 20, eV > 0.6 (Reset SIDE Frame Counter at 79 and reset Velocity Filter Counter at 9)
	7	X10 Accumulation Interval ON/OFF
	8	Master Reset
	9	Velocity Filter Volts ON/OFF
	10	L. E. CPA Volts ON/OFF
	11	H. E. CPA volts ON/OFF
	12	Force Continuous Calibration (SF120-127)

Continued on Following Page

TABLE 3.4.2 ALSEP COMMAND TABLE (Cont.)

One-Time Command No.	Repeatable Command No.	Command Name
	13	CCIG High Voltage ON/OFF
	14	Channeltron High Voltage ON/ OFF
	15	Reset Command Input Register

3.4.3 Dust Cover and Seal

The SIDE sensors are physically located at the top of the instrument. A spring-loaded aluminum dust cover is provided to protect the sensors' entrance apertures and the second surface mirrors (see Section 7.2, Thermal Design) from lunar dust and contaminants caused by the ascent of the Lunar Module.

A solenoid in the dust cover mechanism retracts a pin to release the dust cover latch when the dust cover relay is activated. This occurs during first-time execution of a command containing command "D". Dust Cover activation is monitored digitally by the Status Sub-com, and by a solar cell which is illuminated (during lunar day) when the dust cover is opened.

The CCIG Seal is provided for protection against premature contamination of the sensor. The Seal Circuit energizes a pyrotechnic device in the CCIG unit to deploy the seal. This occurs during first-time execution of a command containing command "B". During test, the lock-out plug inhibits deployment of the seal.

3.4.4 Analog-to-Digital Conversion

The Analog-to-Digital Converters convert data from analog to digital, and transfer the information through the Strobe Gate to the Data Output. The binary output is proportional to the log of the voltage input. Two converters are used: one positive and one negative. The operation of the two converters is identical to one another except for the polarities involved.

The voltages applied to the CPA's, Velocity Filter, and Ground Plane are monitored and converted by the A/D Converters and transferred through the Strobe Gates to the Data Output. Also monitored and processed are the housekeeping data, high voltages, CCGE data and experiment status analog information. The potentials monitored are voltages attenuated by suitable voltage dividers, as shown in applicable sections.

Figure 3.4.4-1 (A/D Conversion Chart) plots the digital output in counts versus the analog input voltage.

The A/D Subcommutator multiplexes the analog information which is to be presented to the converters and eventually transferred to the Strobe Gates. Output data is then read out in specified SIDE Frames and Words according to the format in drawing 609206 (Figure 3.0-3 A/D Status, Sub-Com Sequence) and in Figure 3.0-4, Data Format.

3.4.5 Temperature Sensor: Heaters

Six temperature sensing devices (constant current sources driving into thermistor and sensistor networks) are employed to monitor temperatures throughout the experiment. Voltages developed across the sensors are transformed into digital data by the converters for final readout.

The Heater Control Circuit controls the temperature within the entire experiment. The heaters are distributed throughout the experiment within the electronics assembly.

When the expiment is OFF, survival power is supplied to the heater circuit. When the experiment is ON, the SIDE/CCGE operating power is applied to the heater circuits. The two power sources to the heater will never be applied simultaneously.

3.4.6 Ground Plane Generator

The Master Timing Generator provides sequencing information to the Ground Plane Step Voltage Generator. The Ground Plane Step Voltage Generator supplies a stepped potential to the Ground Plane Screen. Twenty-four voltage steps (twelve positive and twelve negative), in the range of 0 V to ± 27.6 V, are generated to provide the required surface potential.

The Ground Plane voltage is monitored by the A/D Converters and fed to the Strobe Gates for outputting to the readout system.

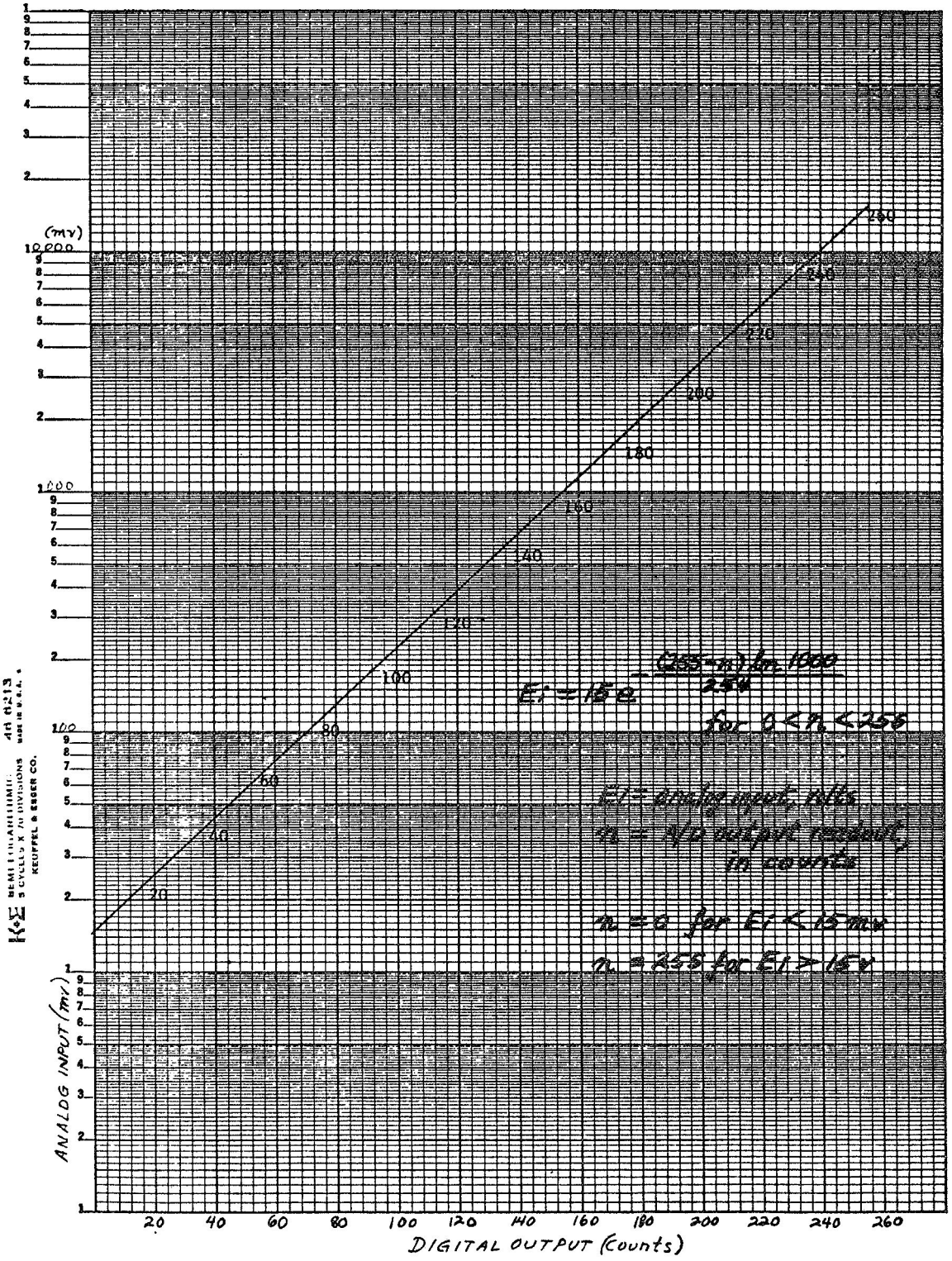


FIGURE 3.4.4-1 A/D CONVERSION CHART

4.0 ALSEP INTERFACES

4.1 Mechanical Interfaces

Mechanical interfaces are discussed in Section 7.0, Mechanical and Thermal Design. Outer structure, cabling, connectors, handling, and human performance are outlined in the referenced section, with additional notes in the Appendix.

Interface requirements are met as specified by Bendix specifications.

4.2 Electrical Interfaces

4.2.1 Primary Power Interface

Power stimuli for the SIDE/CCGE are described in the following sections:

- o 5.1.1 Low Voltage Power Supply
- o 5.2.2 (-) 3500 V Power Supply
- o 5.4.5 +4500 V Power Supply
- o 4.2.2 Signal Interfaces (See Figure 4.2.2-1 for Block Diagram)

Isolation Amplifiers are used to meet interface requirements with the ALSEP Command System and Data Processor. Complete isolation of input and output lines and ALSEP and SIDE signal grounds is affected.

4.2.2.1 Input Isolation Amplifiers

The Input Isolation Amplifiers for Negative Pulses function as the interface for the five ALSEP Command lines. They are non-inverting amplifiers; an input pulse from the ALSEP Command Generator in the range of 2V to 4.5V will drive an amplifier to an output of 3V to 5V pulse. Output pulses from the Command System Isolation Amplifiers drive the Command Input Registers (CIR), and, in the case of Commands B, D, and E, also drive the One Time Command Registers.

The Input Isolation Amplifiers for Positive Pulses are similar to those for negative pulses, except that the driving sources interfaced are the Shift Pulse, Even Frame Mark, and Data Demand. The outputs drive the Shift Pulse and Word Generators.

REF DRAWING SK609730 (OR W7151) FOR INPUT ISO. CIRCUIT FOR POSITIVE PULSES
SK609733 (OR W7148) FOR INPUT ISO. CIRCUIT FOR NEGATIVE PULSES
SK609729 (OR W7154) FOR OUTPUT ISO. AMPLIFIER

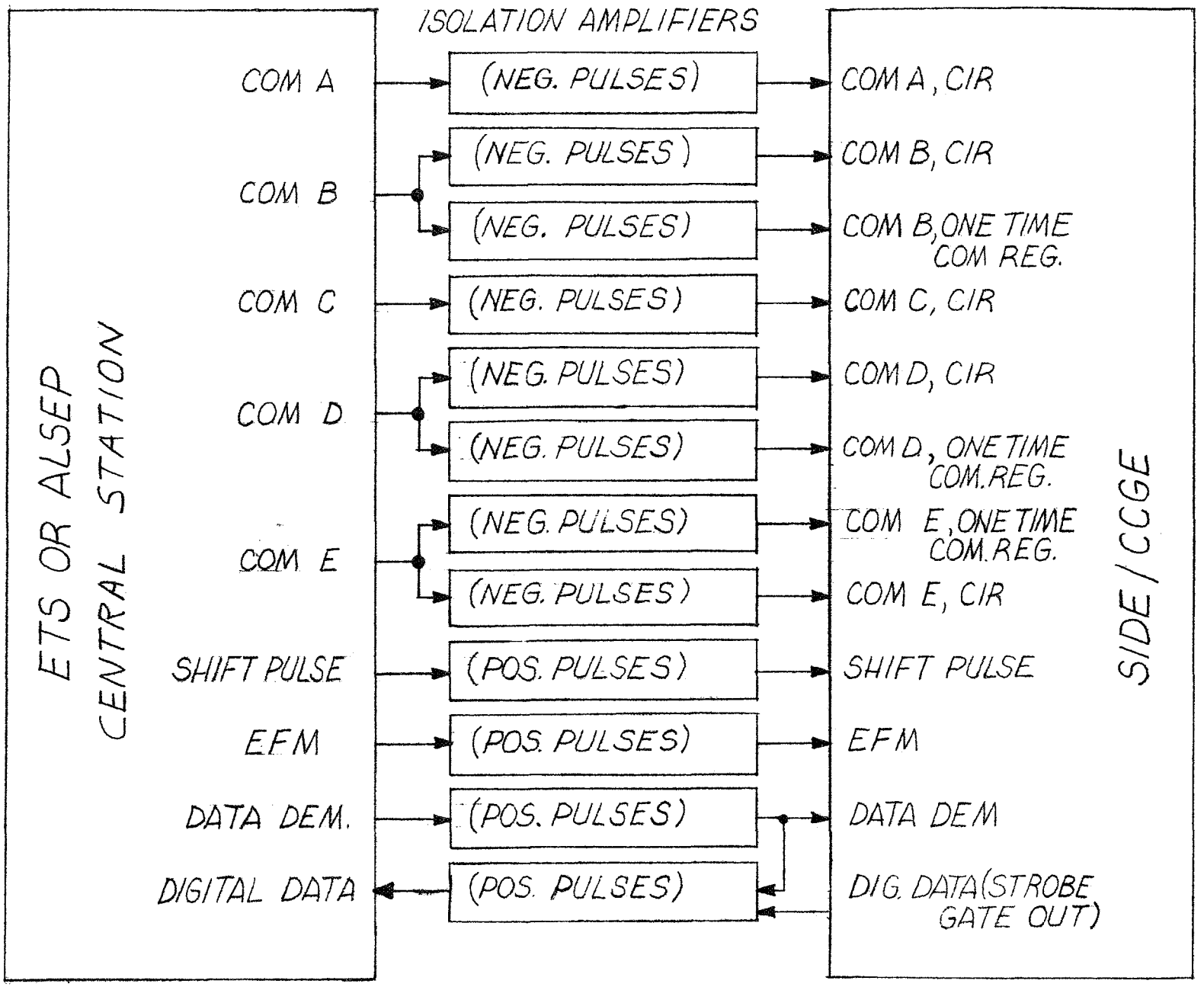


FIG. 4.2.2-1, SIGNAL INTERFACES

4.2.2.2 Output Isolation Amplifier

The Output Isolation Amplifier interfaces the Strobe Gate output with the ALSEP (Digital Data). Its input is AND-ed with the SIDE Data Demand pulse, so that data is presented to the ALSEP or ETS only when Data Demand is present.

5.0 SYSTEM DESCRIPTIONS

5.1 Logic and Support Electronics

5.1.1 Low Voltage Power Supply

A simplified block diagram of the Low Voltage Power Supply is shown in Figure 5.1.1-1. The power supply provides the necessary dc voltages to enable all circuits to meet their specified performance.

The Low Voltage Power Supply consists basically of three sections: 1) Input protection circuitry (surge current limiter and over-voltage protection), 2) switching-mode regulator, and 3) converter.

+29V power is applied from the ALSEP Central Station or the ETS. The Surge Current Limiter reduces current transients produced during power turn-on, while the over-voltage protection circuit shorts out the input power through an SCR when the input voltage reaches about 36 volts.

The Power Supply meets interface requirements including generated noise, surge current and over-voltage limiting, and ground isolation. Input power of the instrument is approximately 6 watts maximum during lunar day.

The regulator section maintains a dc-supply voltage for the converter of +22V. A feedback comparator senses any changes due to input voltage or loading, and automatically readjusts the regulator output. The Duty Cycle Monitor provides a dc voltage inversely proportional with the Power Supply input voltage and is monitored and converted to digital data by the A/D Converters. Figure 5.1.1-2 shows the Duty Cycle Voltage vs Input Voltage.

The converter section chops the +22V dc into a 4 kHz square wave, which is coupled through a transformer to the output rectifier filters. The Low Voltage Power Supply delivers the following output voltages:

+ 10V A/D
+ 60V A/D
+ 5V A/D
- 5V A/D
+ 30V A/D
- 30V A/D
± 5V Square Wave, 4 kHz (1)
± 5V Square Wave, 4 kHz (2)
+ 5V Digital

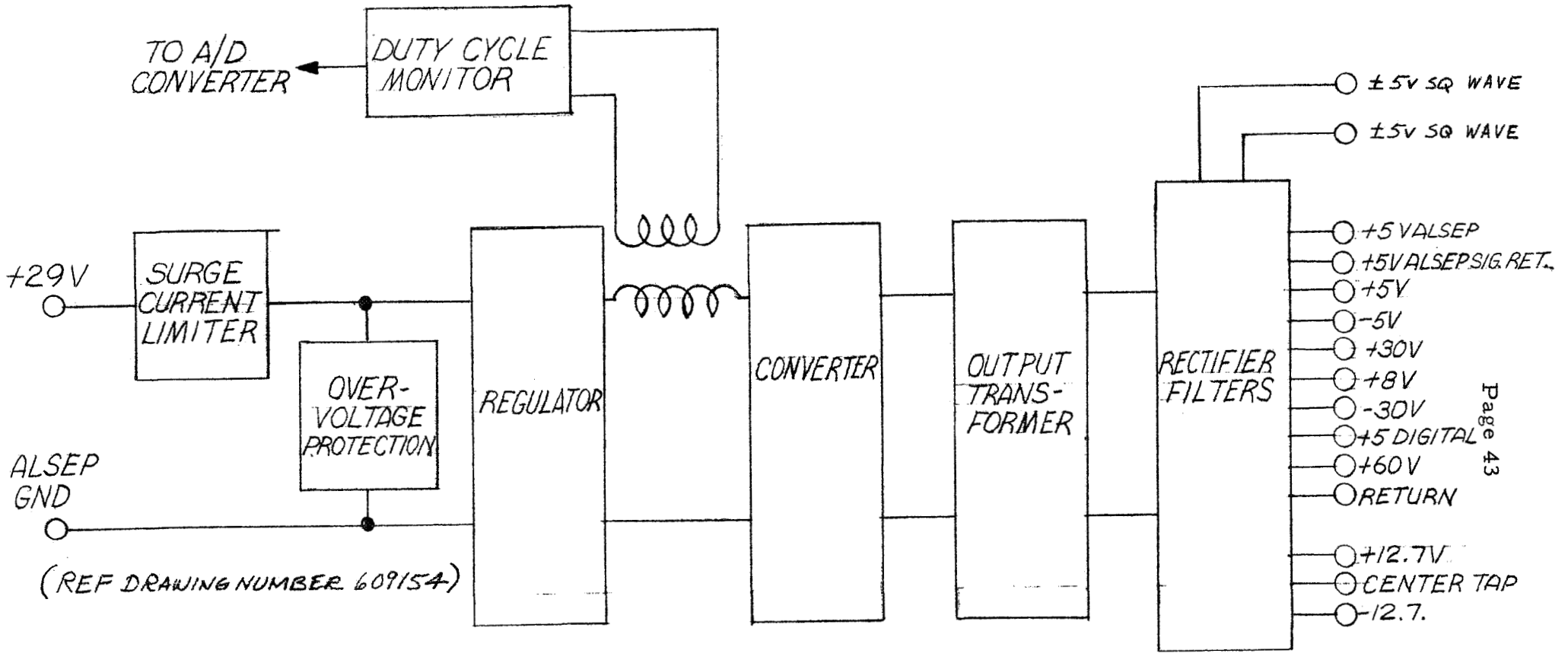


FIG 5.1.1-1, BLOCK DIAGRAM, LOW VOLTAGE POWER SUPPLY

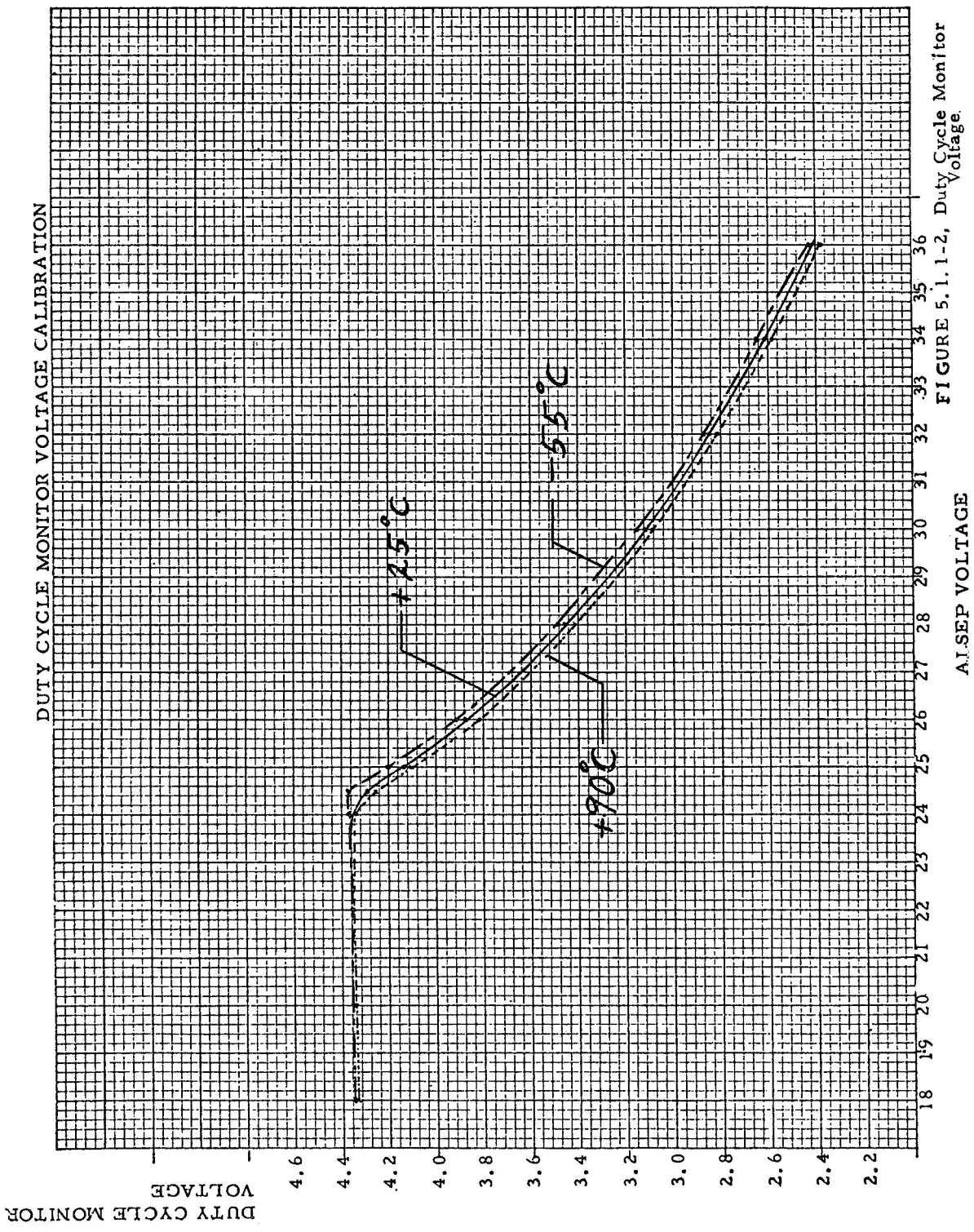


FIGURE 5.1.1-2, Duty Cycle Monitor Voltage

+ 8V A/D (Divider and Zener diode from +30V Output)
+ 5V Alsep
+12V Alsep
-12V Alsep

The two square waves are out of phase with each other, and are used to drive the High Energy modulator.

Figure 5.1.1-3 shows the SIDE/CCGE Power Profile for all operating conditions.

5.1.2 Temperature Monitors

A simplified block diagram of the Temperature Monitors is shown in Figure 5.1.2-1.

Six Temperature Monitors are situated throughout the system as shown in the block diagram. A reliable indication of temperatures within the blivets can thus be realized.

A typical Temperature Monitor consists of a constant current source driving into a thermistor. Voltage drop across the thermistor will decrease as the resistance decreases with an increase in temperature; this voltage is fed to the Analog-to-Digital converters for conversion to digital information. See Table 5.1.2A for resistance vs temperature data for the thermistors.

The sensor for temperature 1, unlike the others, has a positive temperature coefficient.

All current sources deliver 50μa, with the exception of temperature 1 (CCGE), which delivers 100 μa.

5.1.3 Command System

A simplified block diagram of the Command System is shown in Figure 5.1.3-1.

The command stimuli are transmitted from either the ALSEP Central Station or the Experiment Test Set (ETS) via five lines and through a set of Isolation Amplifiers. Four of the command lines are binary coded (1-2-4-8) to represent the command number. The fifth command line is the Execute Command.

Two one-time commands and fifteen repeatable commands are generated from the four command lines and the one Execute Command line. The one-time commands can be executed only once after system power has been applied. Thus, to repeat a one-time command, power must be removed, and then reapplied.

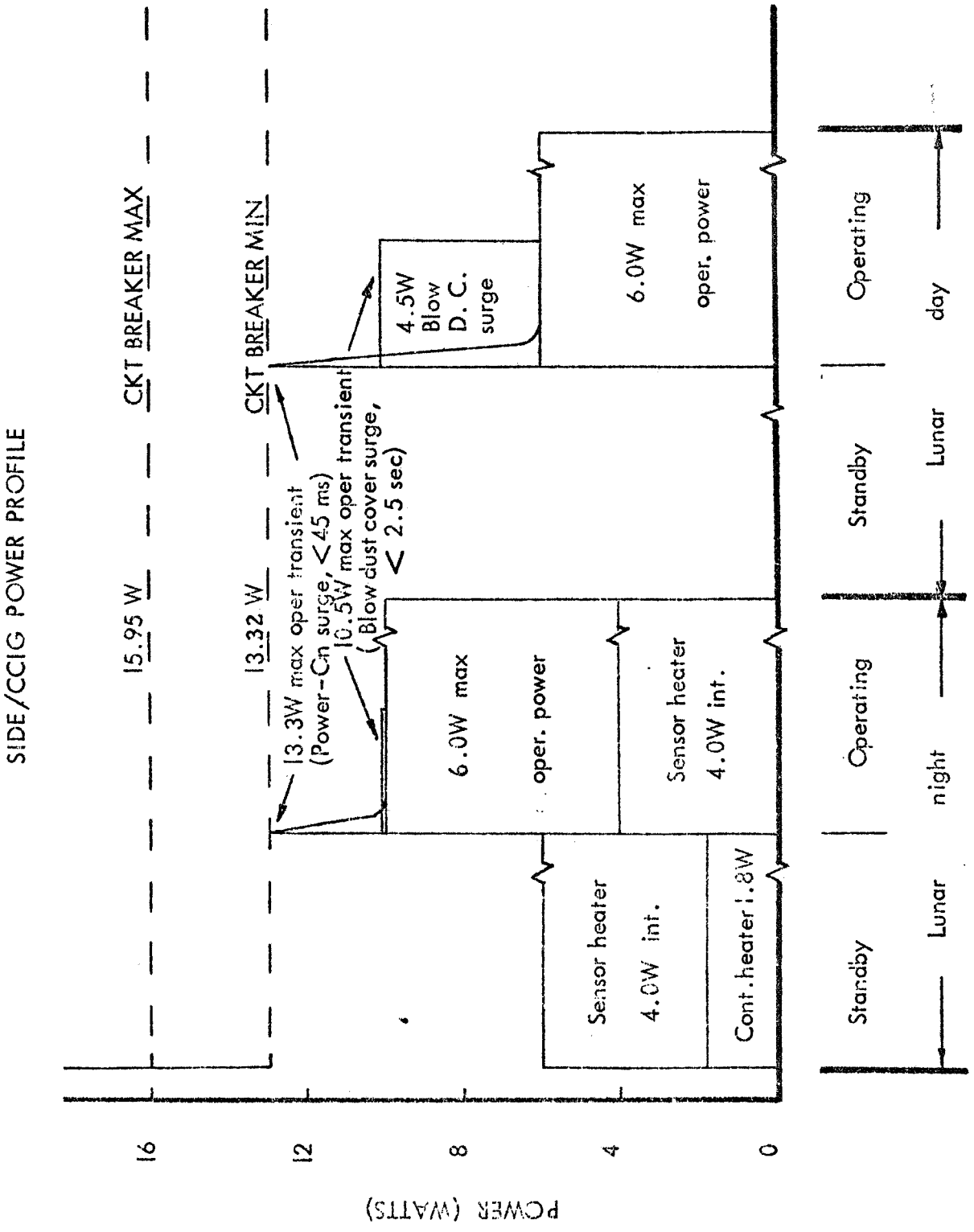


FIGURE 5.1.1-3 SIDE/CCGE Power Profile

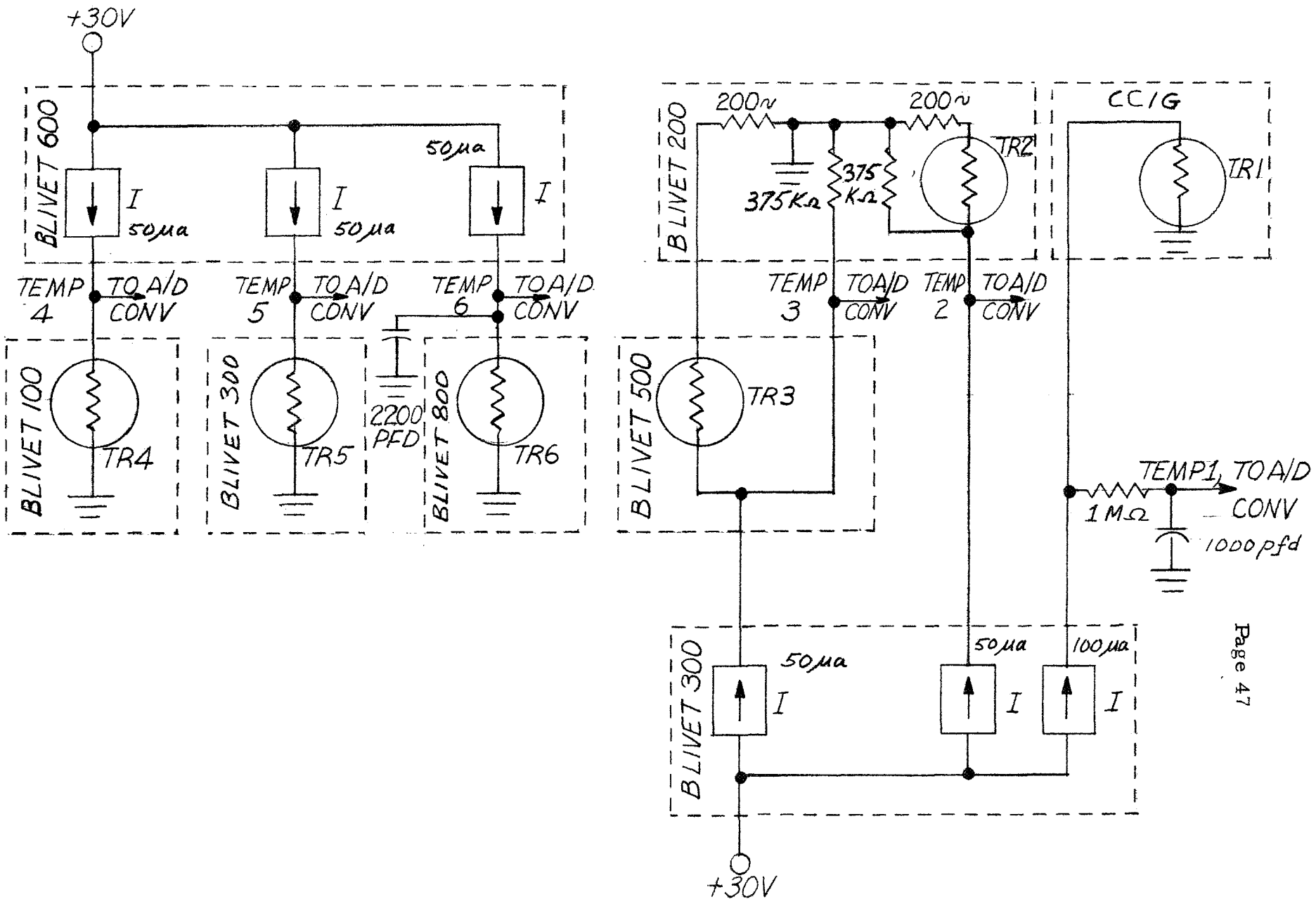
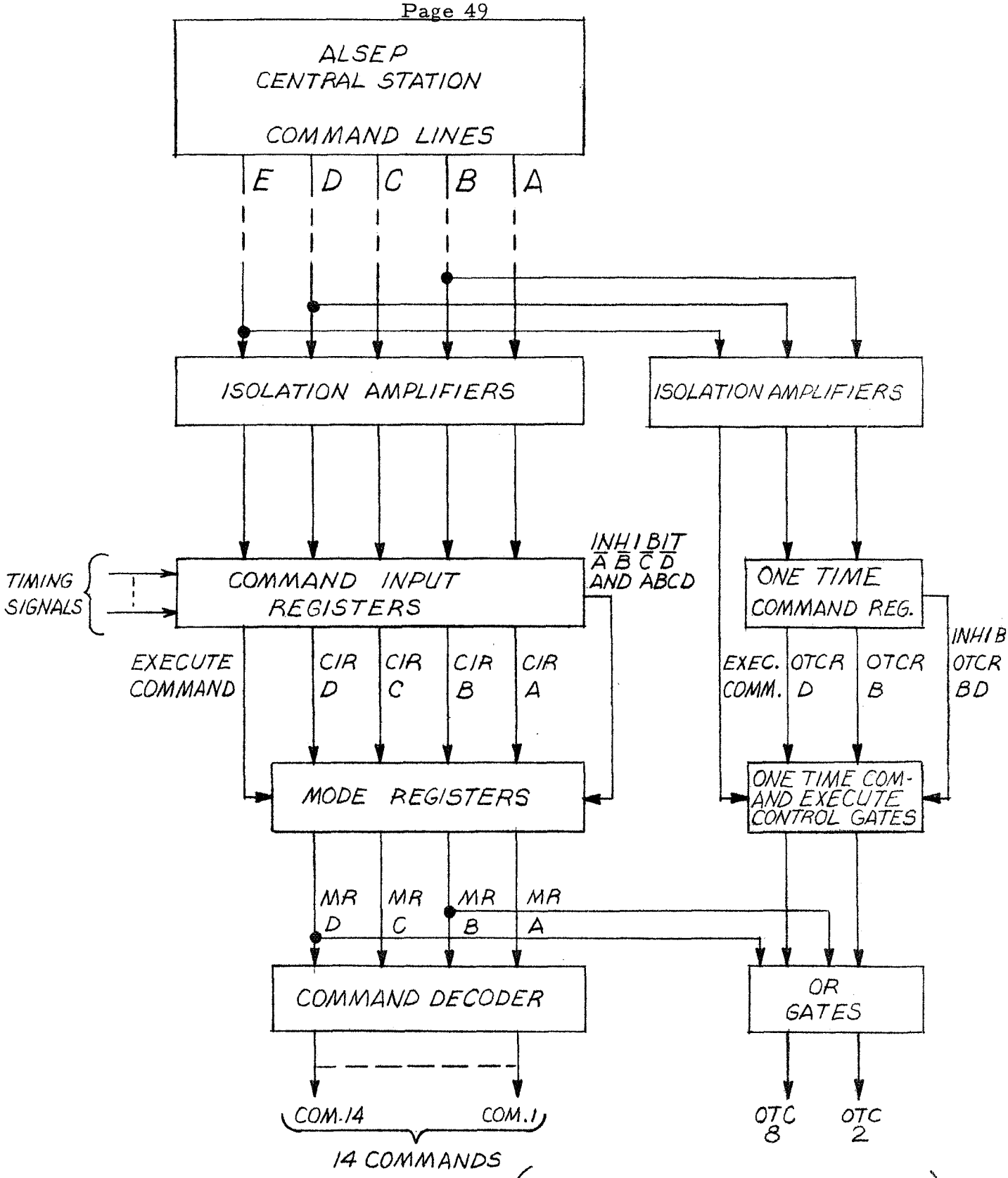


FIG 5.1.2-1, BLOCK DIAGRAM OF TEMPERATURE SENSORS

RESISTANCE VERSUS TEMPERATURE -80°C to +150°C

TEMP°C	RES.	TEMP°C	RES.	TEMP°C	RES.	TEMP°C	RES.	TEMP°C	RES.	TEMP°C	RES.	TEMP°C	RES.
-80	2211K	-44	132.2K	-8	14.90K	28	2633	64	647.1	100	203.8	136	77.6
79	2022K	43	123.5K	7	14.12K	29	2523	65	624.7	101	197.9	137	75.8
78	1851K	42	115.4K	6	13.39K	30	2417	66	603.3	102	192.2	138	73.9
77	1696K	41	107.9K	5	12.70K	31	2317	67	582.6	103	186.8	139	72.2
76	1555K	40	101.0K	4	12.05K	32	2221	68	562.8	104	181.5	140	70.4
75	1426K	39	94.48K	3	11.44K	33	2130	69	543.7	105	176.4	141	68.8
74	1309K	38	88.46K	2	10.86K	34	2042	70	525.4	106	171.4	142	67.1
73	1202K	37	82.87K	-1	10.31K	35	1959	71	507.8	107	166.7	143	65.5
72	1105K	36	77.66K	0	9796	36	1880	72	490.9	108	162.0	144	64.0
71	1016K	35	72.81K	1	9310	37	1805	73	474.7	109	157.6	145	62.5
70	935.4K	34	68.30K	2	8851	38	1733	74	459.0	110	153.2	146	61.1
69	861.4K	33	64.09K	3	8417	39	1664	75	444.0	111	149.0	147	59.6
68	793.7K	32	60.17K	4	8006	40	1598	76	429.5	112	145.0	148	58.3
67	731.8K	31	56.51K	5	7618	41	1535	77	415.6	113	141.1	149	56.9
66	675.2K	30	53.10K	6	7252	42	1475	78	402.2	114	137.2	150	55.6
65	623.3K	29	49.91K	7	6905	43	1418	79	389.3	115	133.6		
64	575.7K	28	46.94K	8	6576	44	1363	80	376.9	116	130.0		
63	532.1K	27	44.16K	9	6265	45	1310	81	364.9	117	126.5		
62	492.1K	26	41.56K	10	5971	46	1260	82	353.4	118	123.2		
61	455.3K	25	39.13K	11	5692	47	1212	83	342.2	119	119.9		
60	421.5K	24	36.86K	12	5427	48	1167	84	331.5	120	116.8		
59	390.5K	23	34.73K	13	5177	49	1123	85	321.2	121	113.8		
58	361.9K	22	32.74K	14	4939	50	1081	86	311.3	122	110.8		
57	335.7K	21	30.87K	15	4714	51	1040	87	301.7	123	107.9		
56	311.5K	20	29.13K	16	4500	52	1002	88	292.4	124	105.2		
55	289.2K	19	27.49K	17	4297	53	965.0	89	283.5	125	102.5		
54	268.6K	18	25.95K	18	4105	54	929.6	90	274.9	126	99.9		
53	249.7K	17	24.51K	19	3922	55	895.8	91	266.6	127	97.3		
52	232.2K	16	23.16K	20	3748	56	863.3	92	258.6	128	94.9		
51	216.0K	15	21.89K	21	3583	57	832.2	93	250.9	129	92.5		
50	201.1K	14	20.70K	22	3426	58	802.3	94	243.4	130	90.2		
49	187.3K	13	19.58K	23	3277	59	773.7	95	236.2	131	87.9		
48	174.5K	12	18.52K	24	3135	60	746.3	96	229.3	132	85.7		
47	162.7K	11	17.53K	25	3000	61	719.9	97	222.6	133	83.6		
46	151.7K	10	16.60K	26	2872	62	694.7	98	216.1	134	81.6		
-45	141.6K	-9	15.72K	27	2750	63	670.4	99	209.8	135	79.6		

TABLE 5.1.2A, Temperature Sensor, Resistance vs. Temperature Characteristics.



CIR COMMAND INPUT REGISTER

MR MODE REGISTER

OTCR ONE TIME COMMAND REGISTER

(REF DRAWING NUMBER SK 609720)

FIG. 5.1.3-1 COMMAND SYSTEM BLOCK DIAGRAM

Table 3.4.2A lists the commands and their function. The execution of any command containing one-time command B closes the discharging path of a charged capacitor through the CCIG seal. The CCIG seal is broken by squib activation. The execution of any command containing one-time command D actuates the dust-cover solenoid which releases the dust-cover. The functions of the repeatable commands are as shown in the Command Table (Table 3.4.2A).

When the lockput plug is installed, the seal-break action is automatically inhibited.

When a command is received, the SIDE will respond to the new instruction immediately after execution of command. With the exception of commands 1, 7, 9, 10, 11, 13, and 14, a command will be replaced by the new command. A repeatable command is generated as follows:

A command, made up of a combination of command inpulses A, B, C, and/or D (1-2-4-8 binary coded), is transmitted from the ALSEP Central Station (or the ETS) through the tape cable. This command is first electrically isolated by the Isolation Amplifiers and then stored in the Command Input Register (CIR). This stored command is transferred to the Mode Register (MR) when the Execute command (E) is transmitted. The contents of the MR are then decoded into the fourteen command logic control functions (Commands 1 through 14).

The CIR is automatically cleared after its contents have been transferred to the Mode Register. Before execution, a command can be erased by executing Command 15. This will reset the CIR and inhibit the transferring of the command to the MR.

5.1.4 SIDE Frame Counter

A block diagram is shown in Figure 5.1.4-1.

The SIDE Frame Counter is the main time reference of the system. It is a 7-bit parallel counter which in the normal mode functions as a divide-by-128 counter. Depending upon the command generated, it can also function as a divide-by-10, -39, or -79 counter. The SIDE Frame Counter controls the Ground Plane Step Voltage Generator, the sub-commutators, the A/D Converters, and the synchronization of the High Energy, Velocity Filter, and Low Energy counters.

The SIDE Frame Counter is advanced by the SIDE Frame Counter Advance pulse, generated by the Logic Timing Section. The SIDE Frame Counter establishes the activation of each of the 128 SIDE Frames, in sequential order, and by means of its 7-bit output, controls the Status and A/D Subcommutators and the Strobe Gates to produce output data conforming to the format in Figure 3.0-3. At SIDE Frame 127 (during normal mode), a detect

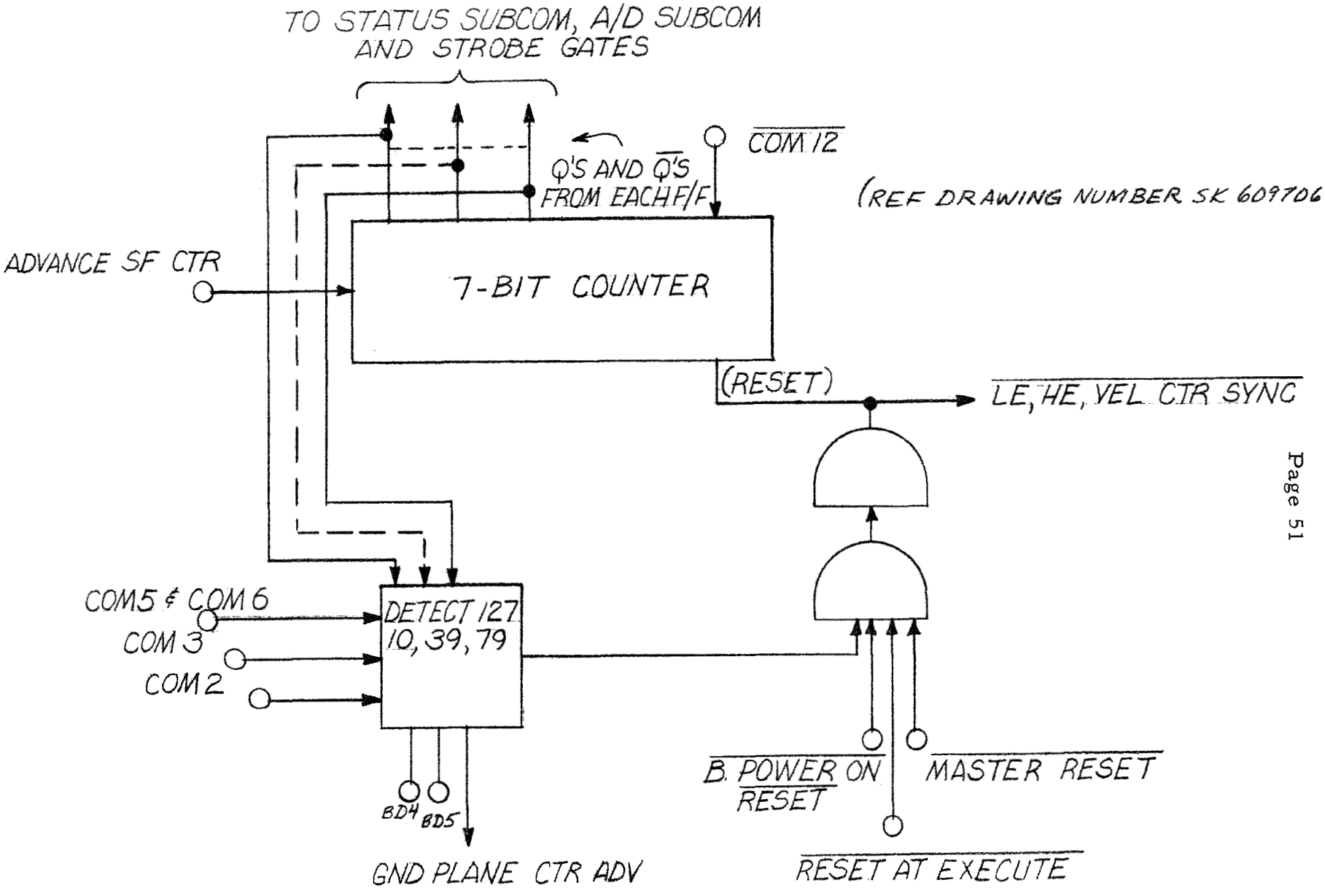


FIG 5.1.4-1 BLOCK DIAGRAM, SIDE FRAME COUNTER

-127 circuit generates a Ground Plane Counter Advance pulse, and a $\overline{\text{LE, HE, VEL Ctr Sync}}$ pulse which resets the SIDE Frame Counter and initiates resetting of the Low Energy, High Energy, and Velocity Filter counters. See Figure 5.2.8-2 for Advance SIDE Frame Counter timing, and Figure 5.2.8-4 for $\overline{\text{LE, HE, VEL Ctr Sync}}$ timing.

The following commands affect the resetting of the SIDE Frame Counter:

- Command 2, Reset SIDE Frame Counter at 10
- Command 3, Reset SIDE Frame Counter at 39
- Command 5, Reset SIDE Frame Counter at 79

When any one of the above commands is executed, the appropriate command line (see Figure 5.1.4-1) switches to a "1" state and causes detection of the SIDE Frame at which the SIDE Frame is to be reset, as indicated by the particular command executed. This generates a Ground Plane Counter Advance pulse and a $\overline{\text{LE, HE, VEL, Ctr Sync}}$ pulse which resets the SIDE Frame Counter and initiates resetting of the Low Energy, High Energy, and Velocity Filter counters. Thus, the $\overline{\text{LE, HE, VEL Ctr Sync}}$ and the Ground Plane Counter Advance pulses are generated when the SIDE Frame Counter resets due to detection of either SIDE Frame 127, 10, 39, or 79.

The $\overline{\text{LE, HE, VEL Ctr Sync}}$ is also generated under the following additional conditions:

- Power is applied to the system.
- A command is executed which resets the SIDE Frame Counter.

When either of the above two conditions exist, the appropriate line ($\overline{\text{Power On Reset, Reset at Execute}}$, or $\overline{\text{Master Reset}}$) pulses to a "0" state, generating the $\overline{\text{LE, HE, VEL Ctr Sync}}$ pulse.

When command 12 (Force Continuous Calibrate) is executed, the $\overline{\text{Com 12}}$ logic control function switches to a "0" state, and remains until a command is generated which removes the SIDE Frame Counter from Continuous Calibrate mode. When $\overline{\text{Com 12}}$ is at a "0" state, the last four flip-flops (bits 8, 16, 32, and 64) are forced to a set or "1" state, causing the counter to sequence repeatedly from 120 to 127.

5.1.5 Status Sub-commutator

Digital data representing status indications is multiplexed by the Status Sub-commutator and presented to the Strobe Gates for outputting. The status information is read out at Word 6 according to the format shown in drawing 609206, A/D & Status Sub-Com Sequence, Figure 3.0-3.

The following status information can thus be monitored throughout the experiment sequencing:

a) Ground Plane Stepper Status

b) Command Input Register Status

c) Calibration Cycle Status

d) Electrometer Range Status

e) Dust Cover and CCIG Seal Status

f) Command Mode Register Status

g) Calibration Rate Status

Refer to Figure 3.0-1, Simplified Block Diagram, SIDE/CCGE Experiment.

5.1.6 Shift Pulse and Word Generator

A simplified block diagram of the Shift Pulse and Word Generator is shown in Figure 5.1.6-1.

Data Demand, Shift, and Even Frame Mark pulses are transmitted from the ALSEP Central Station or the ETS to the SIDE. The Data Demand pulses are each coupled through an Isolation Amplifier, while the Even Frame Mark and Shift pulses are each coupled through an Isolation Amplifier and a Pulse Shaper.

The Shift Pulse Generator consists of a four-bit divide-by-ten counter and a decoder. The Shift Pulses and the Data Demand Pulses are gated through an AND gate to form Advance Shift Pulse Counter pulses. These pulses then advance the Shift Pulse Counter.

Ten Shift Pulses are gated by each Data Demand Pulse. Thus, the Shift Pulse Counter is advanced by ten Shift Pulses only when the Data Demand pulse is present. The Counter output is decoded by the Shift Pulse Decoder to generate ten bits of timing signals to affect parallel-to-serial conversion of data at the Strobe Gates.

The Shift Pulse Counter and the Word Counter are both reset by the Even Frame Mark at the beginning of each SIDE frame.

The Word Counter also consists of a four-bit counter and a decoder. The counter is identical to the Shift Pulse

REF DRAWING NUMBER SK 609711 (SHIFT & WORD COUNTER)
SK 609712 (SHIFT PULSE COUNTER DECODER)
SK 609715 (LOGIC TIMING : WORD DECODER)

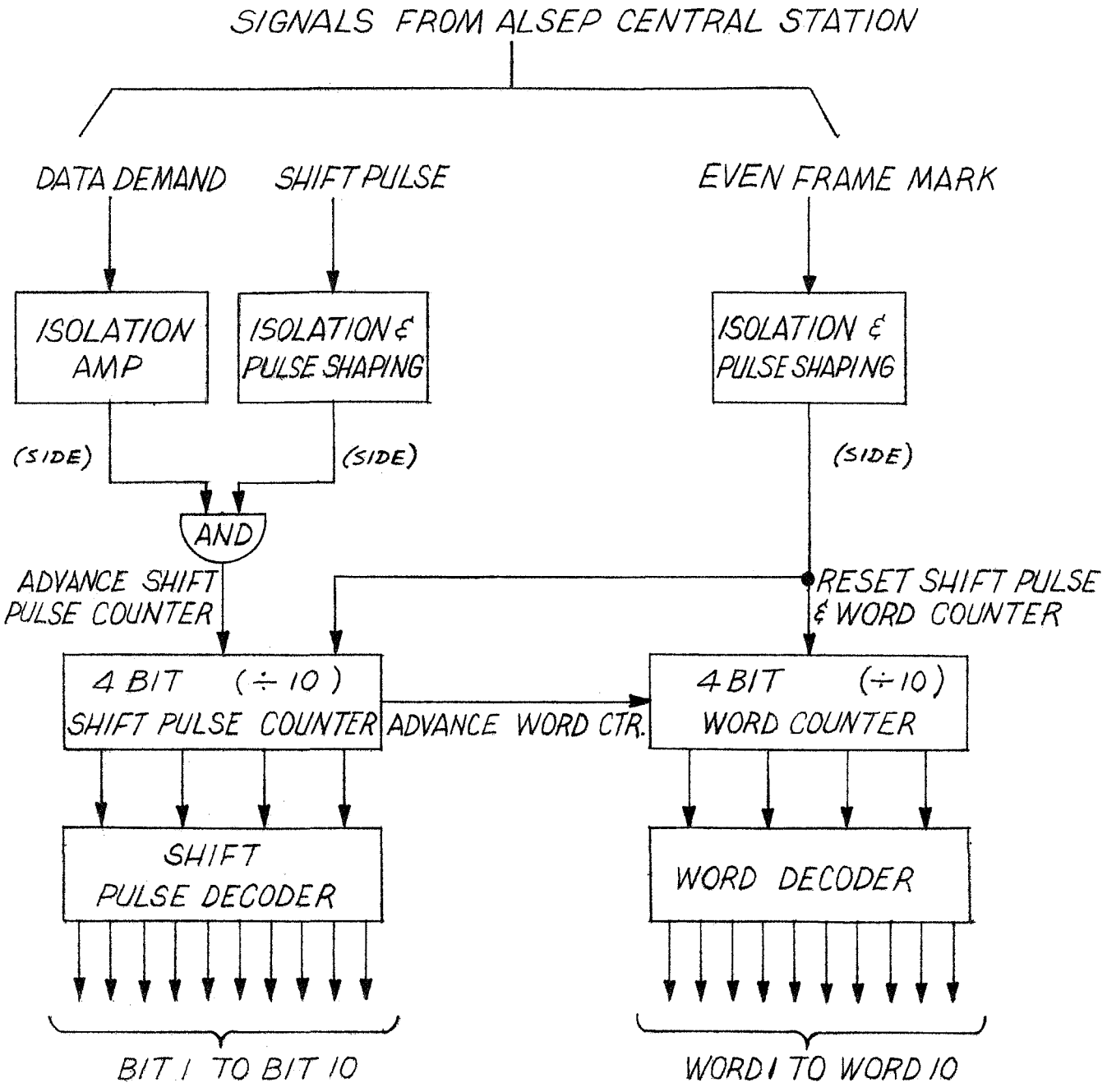


FIG 5.1.6-1, BLOCK DIAGRAM OF THE SHIFT PULSE AND WORD GENERATOR

Counter, except that the Word Counter is advanced by the Advance Word Counter pulse, generated by the Shift Pulse Counter at the end of Bit 10. Since ten Data Demand pulses are generated between two adjacent Even Frame Marks, ten words are generated within one SIDE Frame.

The ten bits and the ten words are used in the Strobe Gate sections as timing signals.

The timing diagram for the Shift Pulse and Word Generators is shown in Figure 5.1.6-2.

5.1.7 Logic Timing and Strobe Gates; Power On Detect

The Logic Timing controls all internal programming. Various major logic circuits are described in other sections of this report; specific networks involving the generation of several timing and control signals are described in this section.

See Figures 3.4.2-1, 3.4.2-2, 3.4.2-3, and 3.4.2-4 for relationships between ALSEP timing signals and SIDE/CCGE timing signals.

5.1.7.1 X10 Mode

See Figure 5.1.7-1 for a simplified block diagram of the X10 Mode generation.

When power is applied to the system, the B. Power On Reset pulse resets the X10 mode control flip-flop. The system now operates in normal mode. The Q output (X10 Mode) of the flip-flop is at a "0" state, and the $\overline{Q}$ ($\overline{\text{X10 Mode}}$) output is at a "1" state. This inhibits gates A and C and opens gates B and D, thus allowing the Advance SIDE Frame Counter pulse and the Advance HE Counter pulse to be generated at normal rates (see Figures 5.2.8-2 and 5.3.7-4, respectively, for timing of the Advance SIDE Frame Counter and Advance HE Counter pulses). Pulses BD3, Word 4, and Word 9 are transferred through the applicable gates to produce the two above-mentioned signals.

When Command 7 (X10 Accumulation Interval ON/OFF) is executed to effect the X10 mode, the state of the control flip-flop changes, inhibiting gates B and D and releasing gates A and C. In this case, gates A and C can transfer information only when the output of the divide-by-ten counter is at a "1" state. Since the divide-by-ten counter is advanced by Word 6, gates A and C are "open" only every ten SIDE Frames. Thus, the Advance SIDE Frame Counter and the Advance HE Counter pulses are generated at one-tenth the normal rate.

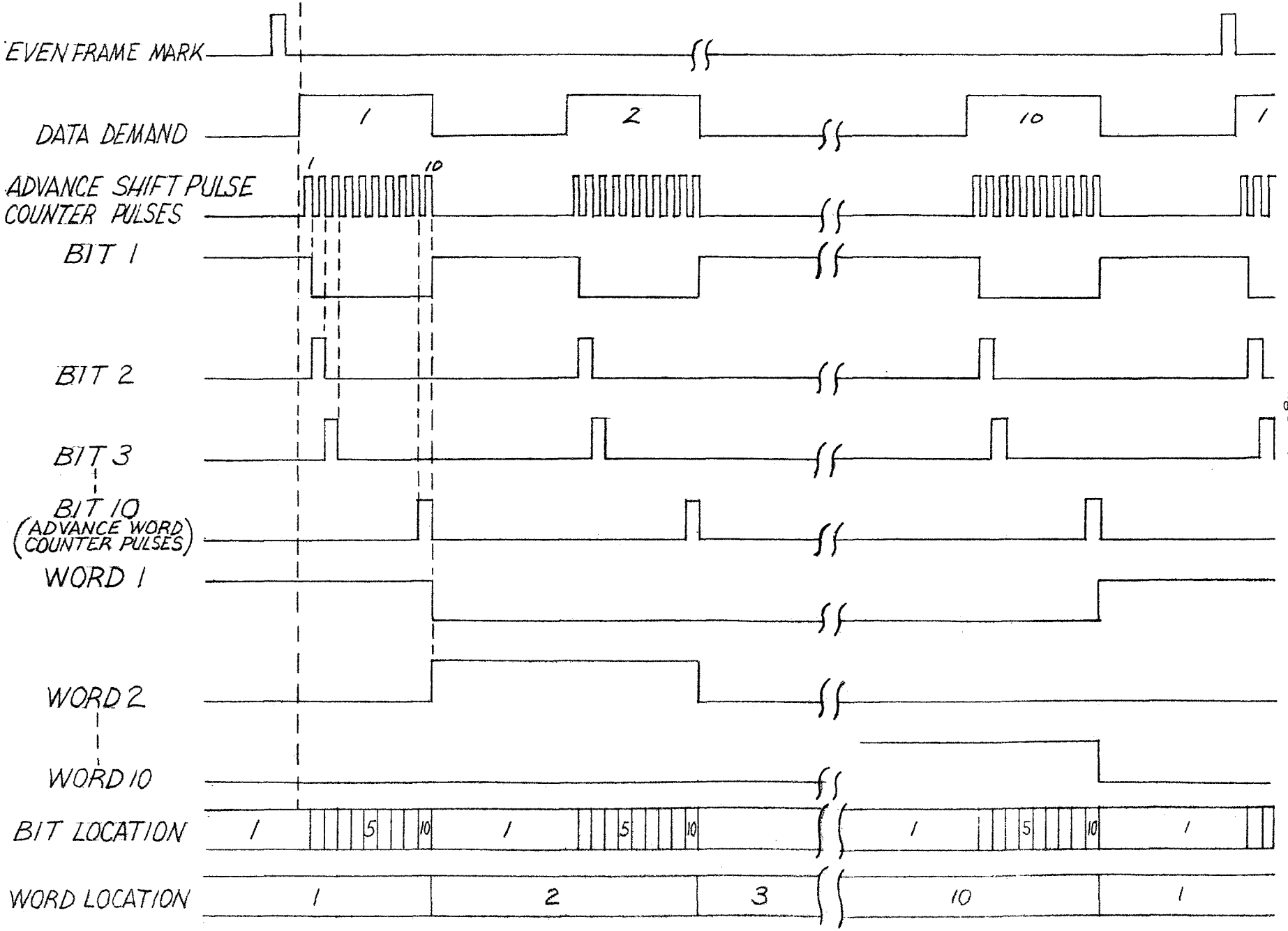


FIG 5.1.6-7 TIMING DIAGRAM OF THE SHIFT PULSE & WORD GENERATOR

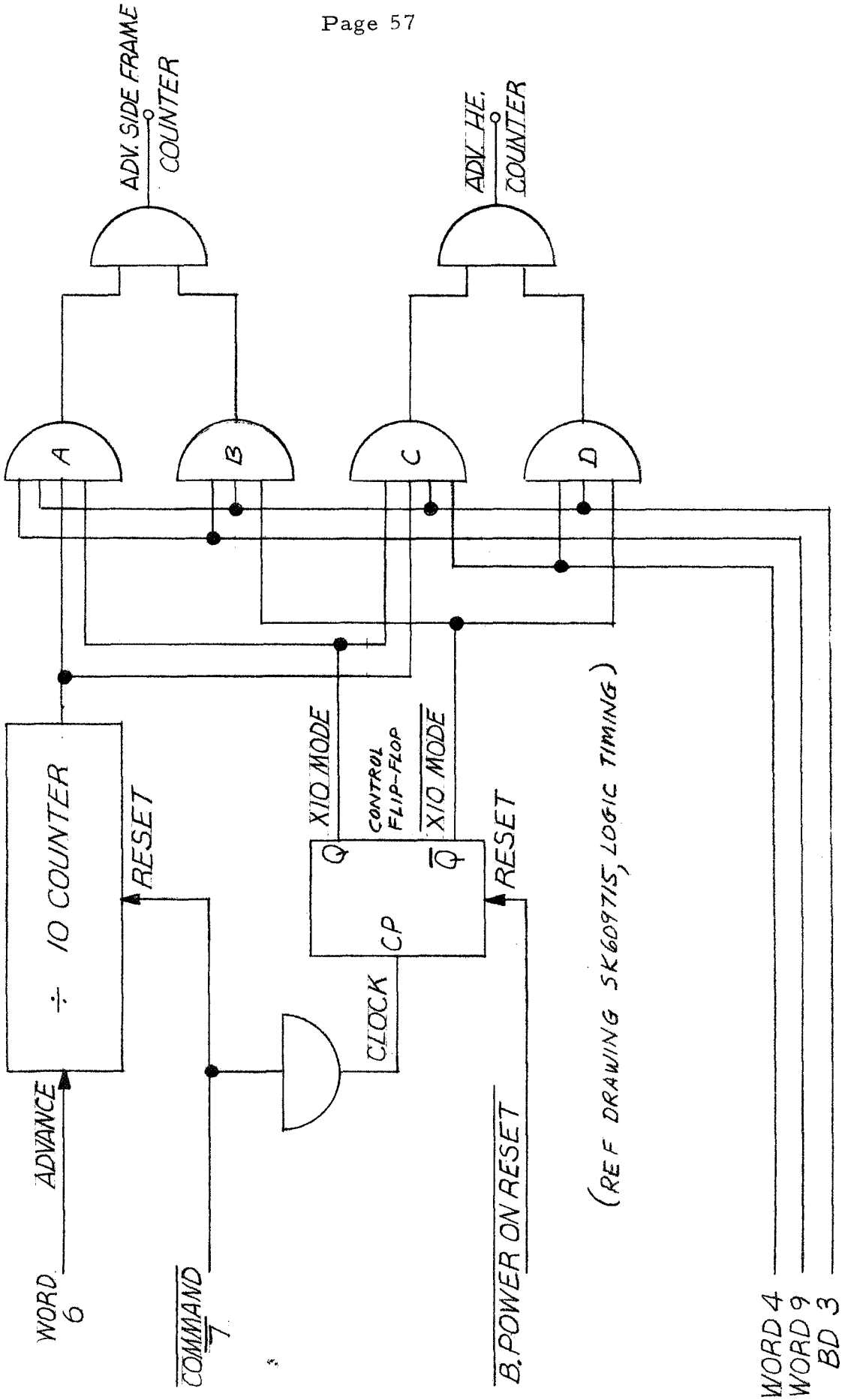


FIG. 5.1.7-1, X10 MODE LOGIC SIMPLIFIED BLOCK DIAGRAM

The $\overline{\text{Command 7}}$ resets the divide-by-ten counter when Command 7 is originally executed.

Executing Command 7 again to effect normal mode operation will toggle the flip-flop to its original state as defined above.

5.1.7.2 Synchronizing Pulses

Five Begin Data (BD) pulses and one End Data (ED) pulse are generated by the Logic Timing to synchronize events throughout the system. The five BD pulses are designated BD1 through BD5.

The BD pulses are generated by 15-μsecond one-shots which are each triggered by the trailing edge of the previous BD pulse (i.e., trailing edge of BD2 triggers BD3). The leading edge of the Data Demand pulse triggers the BD1 pulse.

The ED pulse is generated by a 2.5 msecond one-shot which is triggered by the trailing edge of the Data Demand pulse.

5.1.7.3 Word NOR-Gates; Start A/D Pulse

The three Word NOR-gates perform the following functions:

a) Words 2, 3, 7 and 8 are NOR-gated to produce the Word (2 + 3 + 7 + 8) pulse. The Word (2 + 3 + 7 + 8) pulse is NAND-gated with the End Data pulse to generate the Start A/D pulse for control of the A/D converters.

b) Words 4 and 5 are NOR-gated for timing of the High Energy data through the Strobe Gates.

c) Words 9 and 10 are NOR-gated for timing of the Low Energy data through the Strobe Gates.

5.1.7.4 Power On Detect

Refer to Figure 5.1.7-4 for a block diagram of the Power On Detect circuit.

The Power On Detect circuit synchronizes the system when operating power is applied.

When the system operating power is applied, the dc reset line of the flip-flop (Figure 5.1.7-4) is held down by the power-on detector through an inverter. Thus, the flip-flop is held at reset state.

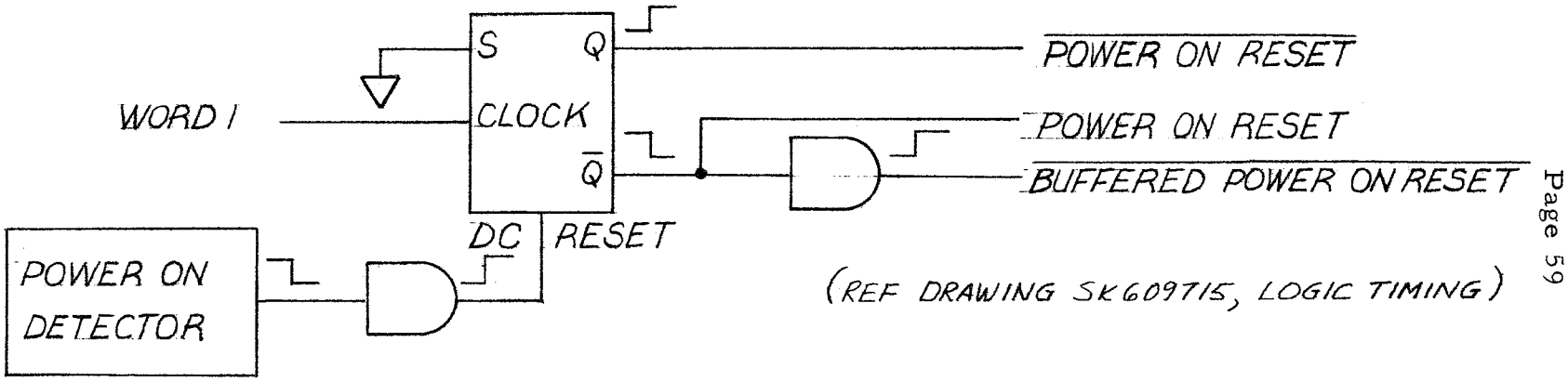


FIG 5.1.7-4, POWER ON DETECT CIRCUIT

This reset state is maintained for approximately 150 msec. The flip-flop will then be set by the first Word 1 pulse to be generated. At the moment the flip-flop is set, the normal operation of all subsystems is initialized.

A typical initialized subsystem can be represented by the reset lines of a typical counter, initially at a "0" and switching to a "1", allowing the operation of the counter to commence from a reset condition.

5.1.7.5 Command Gates

The four gated command signals are described in this section.

- A Master Reset pulse which resets most of the system's logic is generated by gating $\overline{\text{Command 8}}$, Command Input Register 5, $\overline{\text{Inhibit Execution}}$, and BD4.

- A Reset at Execute pulse, which provides resetting to appropriate circuits, is generated by gating Command Input Register 5, BD4, $\overline{\text{Inhibit Execution}}$, and one of the following - $\overline{\text{Command 2}}$, $\overline{3}$, $\overline{4}$, $\overline{5}$, $\overline{6}$, or $\overline{12}$.

- Command 4 and Command 6 are NOR-gated to produce the (Com 6 + Com 4) pulse. This pulse is used to control the operation of the Detect -9 circuit in the Velocity Filter Counter.

- Command 5 and Command 6 are NOR-gated to produce the (Com 5 + Com 6) pulse. This pulse is used to initiate detection of SIDE Frame 79 to effect resetting of the SIDE Frame counter at that SIDE Frame.

5.1.7.6 Reset High Energy Counter Pulse

A Reset High Energy (HE) Counter pulse is generated by the BD4 pulse when the SIDE Frame Counter is reset or re-cycled. See Figure 5.3.7-3 for timing of the Reset HE Counter pulse complement.

5.1.7.7 HE Accumulator Logic Timing

The $\overline{\text{Reset HE Accumulator}}$ pulse and the Advance HE Accumulator pulses are described in this section.

The $\overline{\text{Reset HE Accumulator}}$ pulse is generated by the ED pulse at the beginning of every Word 6 (in normal mode) and every tenth Word 6 in X10 mode. See Figure 5.3.6-1, HE Accumulator Timing Relationships.

The Advance HE Accumulator pulses represent the HE ion detector digital data gated by the control logic. The control

logic permits the data to be transferred to the HE Accumulator from the beginning of Word 6 to the beginning of the next Word 4's Data Demand, and inhibits the data accumulation during the intervening interval.

Data is read out during the period data accumulation is inhibited. Overflow protection is also provided by inhibiting data accumulation when the accumulator is filled to 999,996 counts.

5.1.7.8 LE Accumulator Logic Timing

The $\overline{\text{Reset LE Accumulator}}$ pulse and the Advance LE Accumulator pulse are discussed in this section.

The $\overline{\text{Reset LE Accumulator}}$ pulse is generated by the ED pulse at the beginning of every Word 1 (in normal mode) and every tenth Word 1 in X10 mode. See Figure 5.2.6-1, LE Accumulator Timing Relationships.

The Advance LE Accumulator pulses represent the LE ion detector digital data gated by the control logic. The control logic permits the data to be transferred to the Accumulator from the beginning of Word 1 to the beginning of the next Word 9's Data Demand, and inhibits the data accumulation during the intervening interval.

Data is read out during the period data accumulation is inhibited. Overflow protection is also provided by inhibiting data accumulation when the accumulator is filled to 999,996 counts.

5.1.7.9 Converter and Stepper Voltage ON/OFF Controls

This section describes the ON/OFF control of the +4.5 kV (CCGE HV) and -3.5 kV (Channeltron HV) converters and the VF, LE, and HE Step Voltage generators.

The ON/OFF controls consist of five toggle-mode flip-flops, one for each control. The flip-flops are initially set by the Power On detect when power is applied to the system. This causes the following logic control functions to be at a "1" state and their complements at a "0" state.

- VF Volts ON/OFF
- LE CPA Volts ON/OFF
- HE CPA Volts ON/OFF
- CCGE HV ON/OFF
- Channeltron HV ON/OFF

Thus, the ON/OFF controls cause the above-listed voltage generators to be ON. Refer to the sections describing the individual voltage generators.

The first ON/OFF command executed after application of system power will toggle the corresponding flip-flop and, will turn OFF the appropriate voltage. The next ON/OFF command will turn it ON. This same alternating sequence will continue for subsequent commands.

Function	Command
VF Volts ON/OFF	9
LE CPA Volts ON/OFF	10
HE CPA Volts ON/OFF	11
CCGE HV ON/OFF	13
Channeltron HV ON/OFF	14

5.1.7.10 Strobe Gates

The Strobe Gates provide a means for converting parallel digital data into serial form. The data is commutated from various digital storage elements to the output isolation amplifier.

Refer to Figure 5.1.7-5 for the block diagram of the Strobe Gates. Data is NAND-ed with the assigned Word and bit pulse (see Section 5.1.6 for operation of the Word and Shift Pulse generators). Outputs of the NAND gates (one for each corresponding bit) are NOR-ed and then NAND-gated again with the assigned Word pulse. Outputs of this second group of NAND-gates are then NOR-gated to produce the final data output. Data is then fed to the output Isolation Amplifier for coupling to the ALSEP Central station.

5.1.8 Parity Generator

Two bits of parity are generated by an even parity generator in each SIDE Frame. They are located in the most significant bit of Word 1 and Word 6.

Parity monitoring the data in Word 1 to Word 5 is located in Word 6. The other parity monitoring the data in Word 6 to Word 10 is located in Word 1. Should the data contain an odd number of logic "1"'s , a logic "1" will be added to make the number of logic "1"'s even. Thus, the parity generator provides error detection of the data.

5.1.9 Analog-to-Digital Converter, A/D Sub-Commutator

A simplified block diagram of the Analog-to-Digital (A/D) Converter is shown in Figure 5.1.9-1.

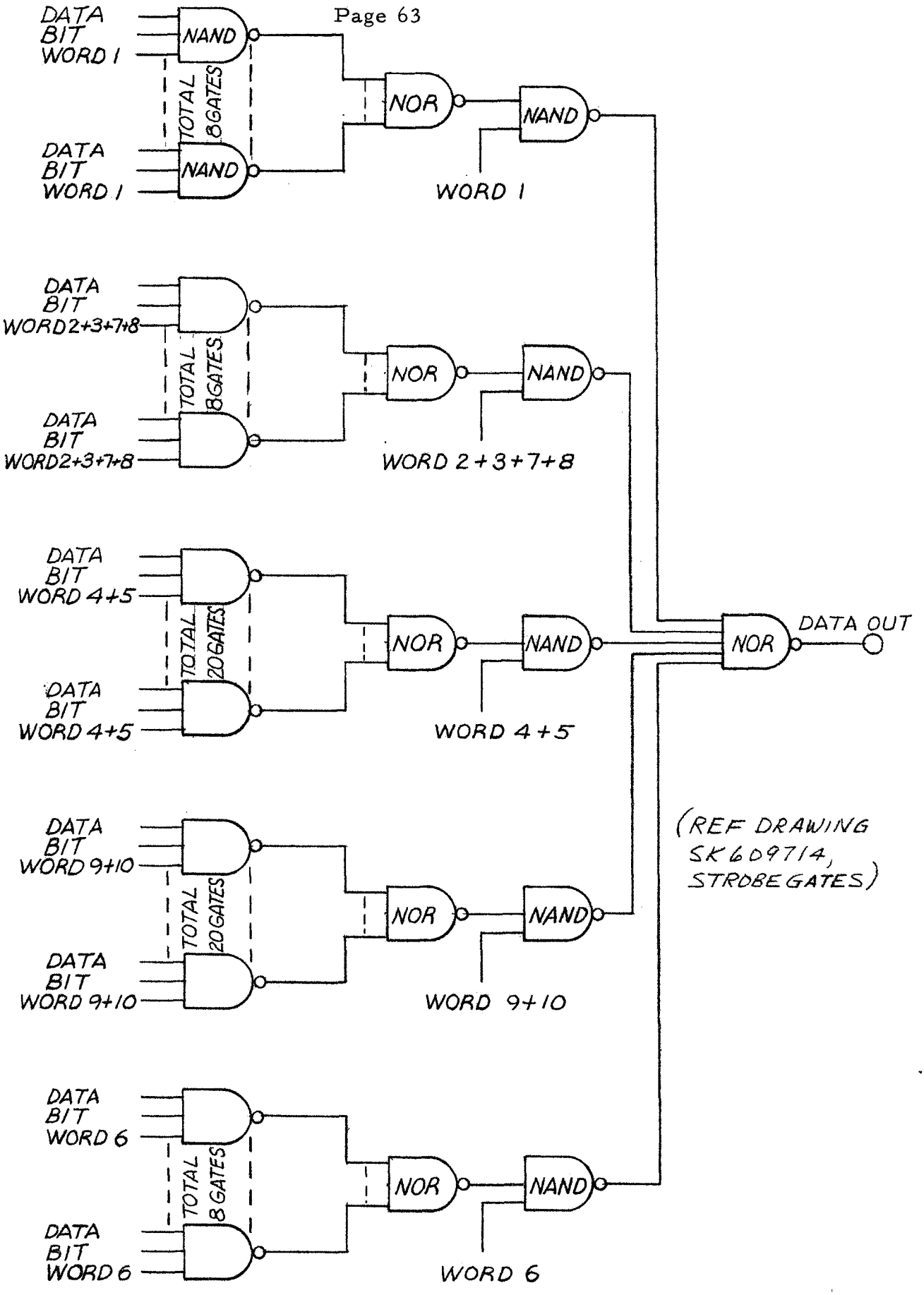


FIG 5.1.7-5, STROBE GATES BLOCK DIAGRAM

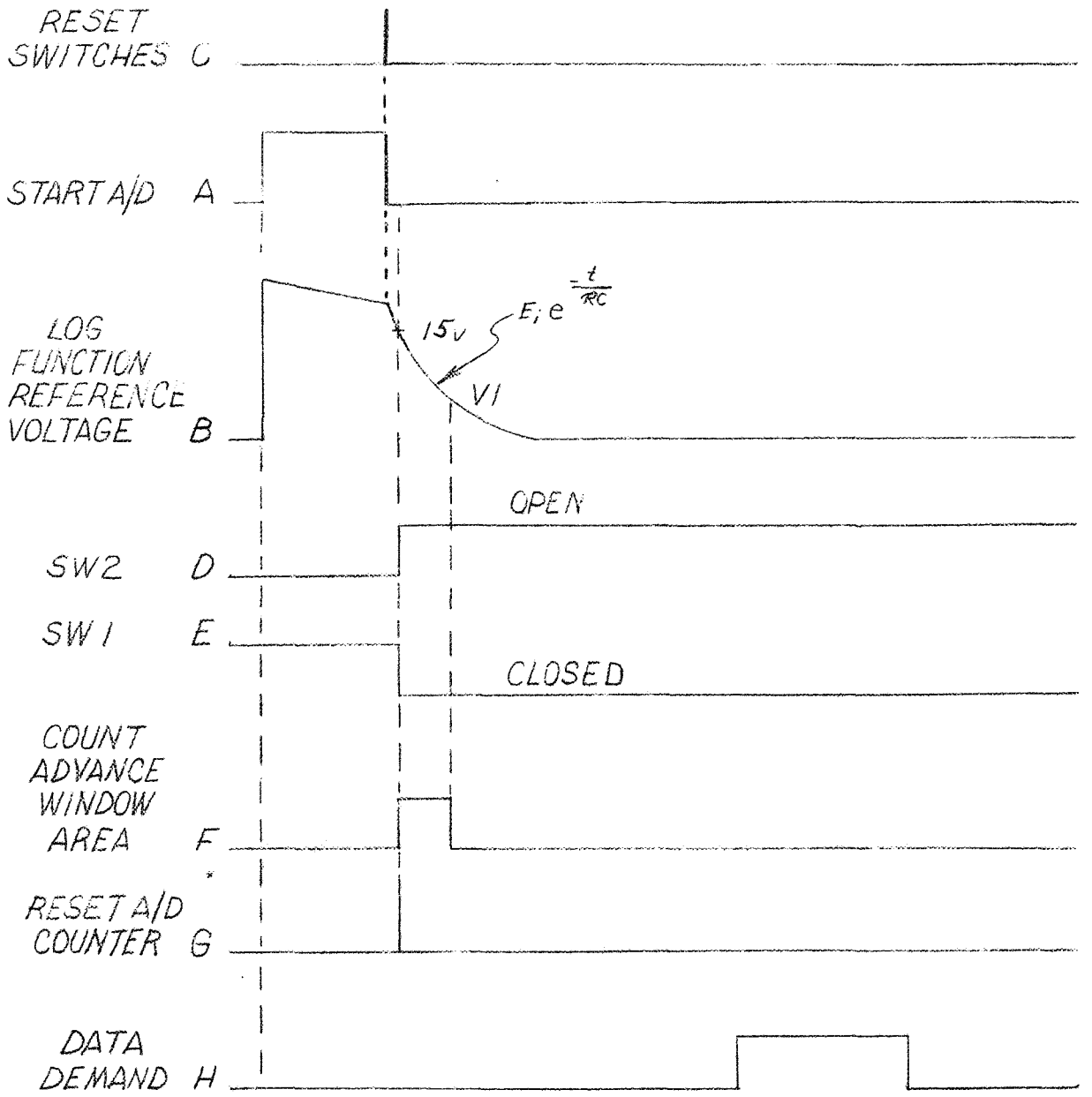


FIG 5.1.9-2, TIMING DIAGRAM OF A/D CONVERTER SIGNALS

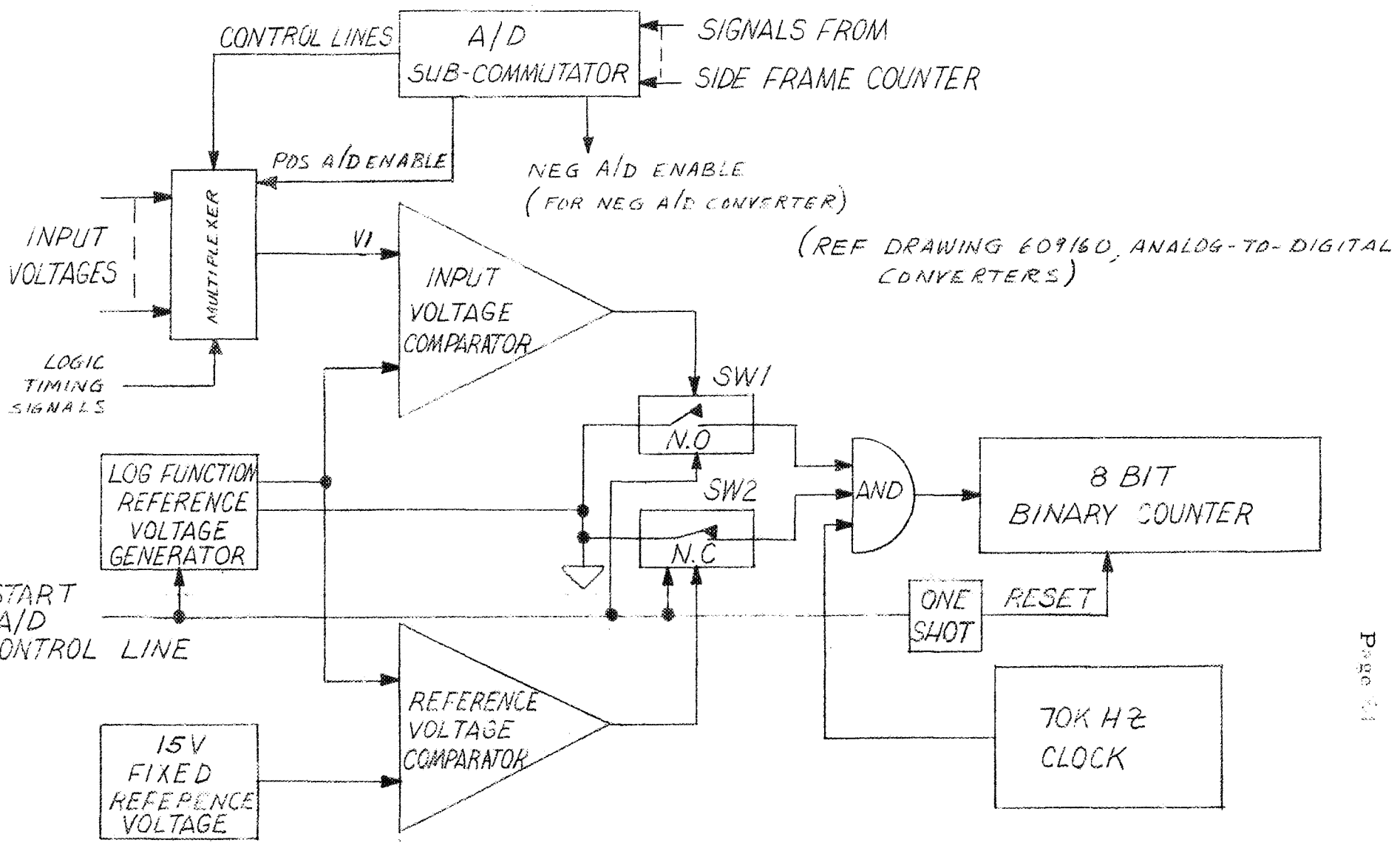


FIG 5.1.9-1, BLOCK DIAGRAM OF ANALOG TO DIGITAL CONVERTOR

Two A/D Converters are included in the SIDE. The Positive A/D Converter transforms positive voltages into digital counts, while the Negative A/D Converter transforms negative voltages. Since both A/D Converters are functionally identical, except for polarity, only the Positive A/D Converter will be described here.

Multiplexing of the input voltages is done in a multiplexer controlled by the A/D Sub-Commutator. The A/D Sub-Commutator generates the logic for thirty-three control lines, one for each A/D input voltage, by decoding the SIDE Frame Counter. These control signals are generated to select the monitored voltages for each SIDE Frame according to the format in drawing 609206 (Figure 3.0-3). Two polarity control lines (one positive and one negative) select for positive or negative A/D conversion.

The A/D Converter consists of two comparators: the input voltage comparator and the reference voltage comparator. The input voltage comparator compares the multiplexer's selected input voltage with a log function reference voltage. The reference voltage comparator compares the log function reference voltage with a fixed precision +15 volts. These two comparators are followed by two switches which gate the 70 kHz clock output into an 8-bit binary counter.

Figure 5.1.9-2 shows the timing of the A/D conversion signals. The analog input voltages are compared in the following manner:

A Start A/D pulse (Waveform A) initiates the conversion process. The log function reference voltage generator is turned on and holds its output level higher than 15 volts during the duration of the Start A/D pulse. At the end of the pulse, two events occur simultaneously.

a) A reset switch pulse (Waveform C) resets both switches so that switch SW1 is open and SW2 is closed. Thus, SW2 inhibits the AND-gate, preventing the 70 kHz clock from driving the counter.

b) The log function reference voltage generator begins to discharge its output from its initial value (>15V) to zero through a precision RC network. The discharging curve is represented by the curve marked

"$E_i e^{-t/RC}$" at Waveform B.

A reference voltage comparator monitors the discharging curve. A Reset A/D Counter pulse is generated when the discharging voltage reaches +15 volts. At the same time, the comparator opens SW2 and allows the 70 kHz clock to drive the counter.

SW2, which is normally open, remains open until the discharging log function reference voltage equals the input voltage V1.

When both voltages are equal, SW1 closes. This inhibits the AND-gate, preventing the 70 kHz clock from driving the counter. Thus, the number of counts accumulated by the counter is a function of the duration between the opening of SW2 and closing of SW1. This interval (t_1) is represented by Waveform F.

The relationship between the input voltage and the number of counts is expressed in the following equation:

$$E_i = 15e^{-\frac{(255-n)\ \mathrm{In}\ 1000}{254}}$$

where E_i = input voltage (volts)

n = number of counts

The data in the counter is read out by the Strobe Gates when the next Data Demand pulse is present. The process of Analog-to-Digital conversion is then complete.

The system contains a total of twenty-three positive channels and ten negative channels, as listed below:

POSITIVE A/D CHANNELS

- High Energy Curved Plate Analyzer (HECPA) Plate Voltage
- Low Energy Curved Plate Analyzer (LECPA) Plate Voltage
- Velocity Filter (VF) Voltage
- +30 MV Calibration Voltage
- +1 V Calibration Voltage
- +5 V Analog Supply Voltage
- +5 V Digital Supply Voltage
- + A/D Reference Voltage
- +12V Calibration Voltage
- +30V Supply Voltage
- +60V Supply Voltage
- Temperature No. 1 Voltage

- Temperature No. 2 Voltage
- Temperature No. 3 Voltage
- Temperature No. 4 Voltage
- Temperature No. 5 Voltage
- Temperature No. 6 Voltage
- +4.5 kV Monitoring Voltage
- Ground Plane Voltage
- CCGE Electrometer Range
- Dust Cover and Seal Monitoring Voltage
- Low Voltage Power Supply, Pre-regulator Duty Cycle Monitoring Voltage
- One-Time-Command Status

NEGATIVE A/D CHANNELS

- -30 MV Calibration Voltage
- -1V Calibration Voltage
- -5V Supply Voltage
- -A/D Reference Voltage
- -12V Calibration Voltage
- -30V Supply Voltage
- -3.5 kV Monitoring Voltage
- Solar Cell Voltage
- CCGE Electrometer Output Voltage
- A/D Ground (Reference) Potential

HE CPA, LE CPA, and VF voltages are read out every SIDE Frame in Words 3, 8, and 7 respectively. All other voltages are read out in Word 2, during the cycle of 128 SIDE Frames, according to the format in Figure 3.0-3, A/D and Status Sub-Com Sequence.

Figure 3.4.4-1, A/D Conversion Chart, plots the digital output in counts versus the analog input voltage.

5.1.10 Heater Control Circuit

Figure 5.1.10-1 shows a simplified schematic of the Heater Control Circuit.

The Heater Control Circuit supplies heater power to the Survival Heater (mounted near the Curved Plate Analyzers) and the Blivet (operational) Heater for operation at low temperatures.

Normal operating mode - Operating power (+29V) applied to the SIDE is also applied to the Heater Control Circuit through a set of normally closed contacts in the Blow Dust Cover Relay. At high temperatures, the value of thermistor T (See Figure 5.1.10-1) maintains the control voltage to the comparator amplifier below the reference voltage, causing the output of the amplifier to be low, and the output transistor Q1 to be cut off. Thus, no heater current is drawn. When temperature drops to $0^{\circ}C \pm 8^{\circ}C$, the amplifier is turned on, Q1 conducts, and heater current is drawn by the blivet heaters. Activation of the Dust Cover temporarity removes +29V power from the Heater Control circuit. Note that no Survival Heater current is drawn under normal operating conditions.

Power - OFF mode - Survival power is applied to the Heater Control Circuit, which is energized in the same manner as described above. The Survival Heater draws continuous heater current whenever survival power is applied.

Table 5.1.10A shows heater power drawn under various operating conditions. Table 5.1.10B shows resistance versus temperature characteristics for the thermistor.

5.1.11 Dust Cover Circuit; Solar Cell

Refer to Figure 5.1.10-1 for a block diagram of the Dust Cover Circuit.

The Dust Cover circuit energizes the Dust Cover Relay which, when activated, momentarily opens the relay contacts through which power is supplied to the Heater Control circuit, and closes another set of contacts to supply power to the Dust Cover solenoid. The Dust Cover solenoid then releases the latch, allowing the Dust Cover to open.

The Dust Cover Circuit one-shot is driven by the SIDE Command System. Any first-time command containing D (binary 8) causes the input to the Dust Cover circuit one-shot to switch and remain at a logic "1". The one-shot then drives the Dust Cover relay for approximately two seconds.

BLOW DUST COVER AND HEATER CONTROL CIRCUIT

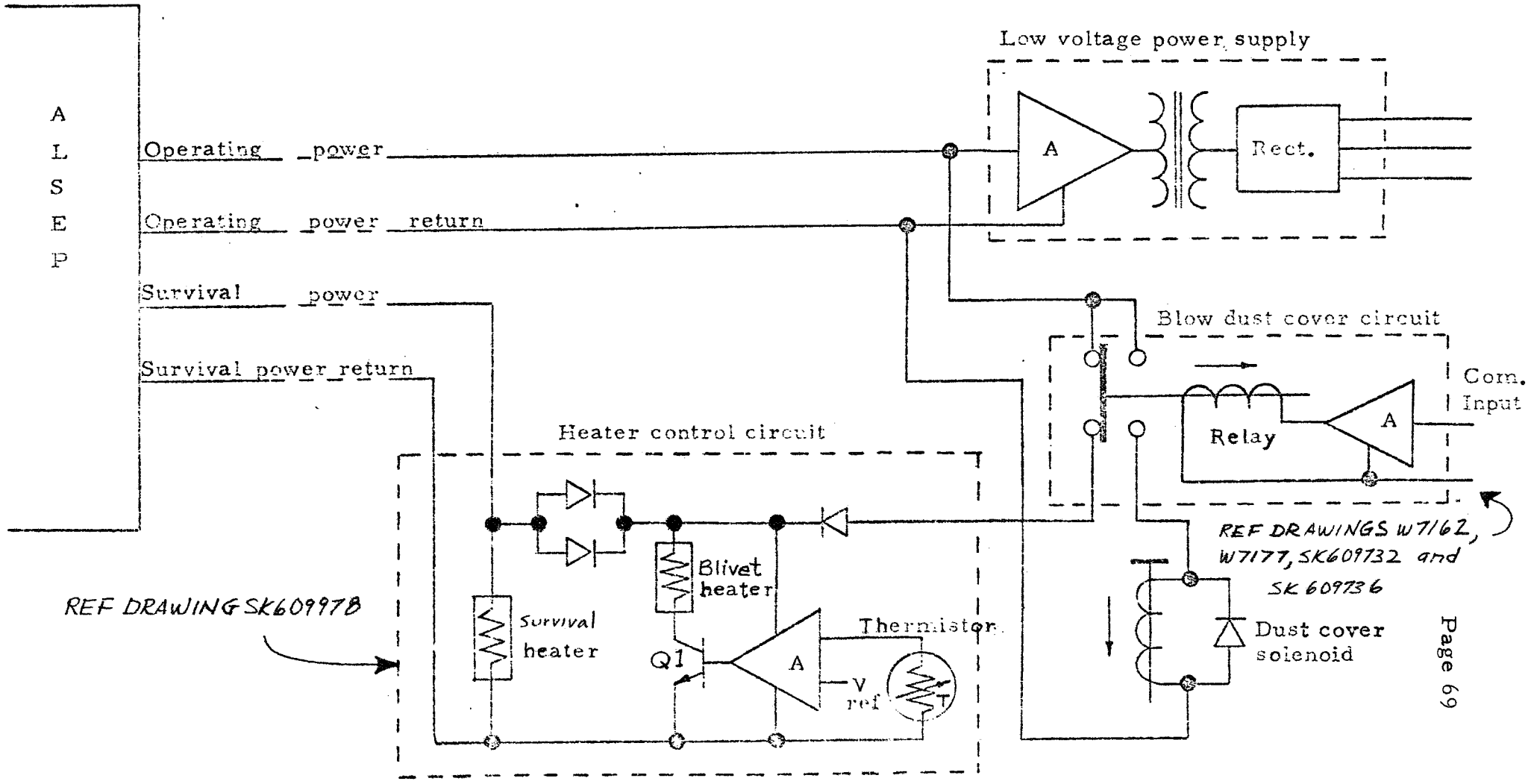


FIGURE 5.1.10-1, Blow Dust Cover and Heater Control Circuit

	MAX. POWER		PRESENT CALCULATED POWER		
	EXPERIMENT	SURVIVAL	INSTRU.	HEATER	TOTAL
DAY	6.0 W	0	6.0 W	0	6.0 W
NIGHT	10.0 W	0	6.0 W	4.0 W	10.0 W
EXPT. OFF	0	6.0 W	0	6.0 W	6.0 W

TABLE 5.1.10 A, Heater Power

RESISTANCE VERSUS TEMPERATURE -40°C to +150°C

TEMP°C	RES.Ω	TEMP°C	RES.Ω	TEMP°C	RES.Ω	TEMP°C	RES.Ω	TEMP°C	RES.Ω	TEMP°C	RES.Ω
-40	884.6K	-4	116.0K	32	22.33K	68	5738	104	1840	140	701.2
39	830.9K	3	110.3K	33	21.43K	69	5545	105	1788	141	684.1
38	780.8K	2	104.9K	34	20.57K	70	5359	106	1737	142	667.5
37	733.9K	-1	99.80K	35	19.74K	71	5180	107	1688	143	651.3
36	690.2K	0	94.98K	36	18.96K	72	5007	108	1640	144	635.6
35	649.3K	1	90.41K	37	18.21K	73	4842	109	1594	145	620.3
34	611.0K	2	86.09K	38	17.49K	74	4682	110	1550	146	606.5
33	575.2K	3	81.99K	39	16.80K	75	4529	111	1507	147	591.1
32	541.7K	4	78.11K	40	16.15K	76	4381	112	1465	148	577.1
31	510.4K	5	74.44K	41	15.52K	77	4239	113	1425	149	563.5
30	481.0K	6	70.96K	42	14.92K	78	4102	114	1386	150	550.2
29	453.5K	7	67.66K	43	14.35K	79	3970	115	1348		
28	427.7K	8	64.53K	44	13.80K	80	3843	116	1311		
27	403.5K	9	61.56K	45	13.28K	81	3720	117	1276		
26	380.9K	10	58.75K	46	12.77K	82	3602	118	1241		
25	359.6K	11	56.07K	47	12.29K	83	3489	119	1208		
24	339.6K	12	53.54K	48	11.83K	84	3379	120	1176		
23	320.9K	13	51.13K	49	11.39K	85	3273	121	1145		
22	303.3K	14	48.84K	50	10.97K	86	3172	122	1114		
21	286.7K	15	46.67K	51	10.57K	87	3073	123	1085		
20	271.2K	16	44.60K	52	10.18K	88	2979	124	1057		
19	256.5K	17	42.64K	53	9807	89	2887	125	1029		
18	242.8K	18	40.77K	54	9450	90	2799	126	1002		
17	229.8K	19	38.99K	55	9109	91	2714	127	976.3		
16	217.6K	20	37.30K	56	8781	92	2632	128	951.1		
15	206.2K	21	35.70K	57	8467	93	2552	129	926.7		
14	195.4K	22	34.17K	58	8166	94	2476	130	903.0		
13	185.2K	23	32.71K	59	7876	95	2402	131	880.0		
12	175.6K	24	31.32K	60	7599	96	2331	132	857.7		
11	166.6K	25	30.00K	61	7332	97	2262	133	836.1		
10	158.0K	26	28.74K	62	7076	98	2195	134	815.0		
9	150.0K	27	27.54K	63	6830	99	2131	135	794.6		
8	142.4K	28	26.40K	64	6594	100	2069	136	774.8		
7	135.2K	29	25.31K	65	6367	101	2009	137	755.6		
6	128.5K	30	24.27K	66	6149	102	1950	138	736.9		
-5	122.1K	31	23.28K	67	5940	103	1894	139	718.8		

TABLE 5.1.10 B, Heater Control Sensor, Resistance vs Temperature Characteristics

An important design feature of the one-shot provides immunity from premature firing during system power turn-on. In addition, the Command System logic allows the one-shot to be activated only once; power to the SIDE must be removed and then re-applied to re-active dust cover removal.

The Solar Cell is a standard N-material photoelectric cell. Figure 5.1.11-1 shows the electrical schematic. The Solar Cell is used to indicate the state of the Dust Cover (open or closed) by supplying a voltage to the A/D Converters when the Dust Cover is open and the cell is illuminated.

Refer to Figure 5.1.11-2 for the Current-Voltage characteristics of the Solar Cell.

5.1.12 Voltage Dividers

Schematic diagrams of the Voltage Dividers are shown in Figures 5.1.12-1 (positive Calibration Voltage Divider), 5.1.12-2 (Negative Calibration Voltage Divider), and 5.1.12-3 (+30, -30, +60V Divider).

The Voltage Dividers are used to calibrate the A/D Converters and provide attenuation for the +30V, -30V, and +60V to be monitored. Outputs of the Voltage Dividers are converted to digital data by the A/D Converters and are read out according to the format in drawing 609206, A/D and Status Sub-Com Sequence (Figure 3.0-3).

The Positive Cal Voltage Divider divides the +15V Reference Voltage to a precision +12V, +1V, and +30mV. The Negative Cal Voltage Divider uses a zener diode, along with a standard resistor divider, to divide down the -30V to a precision -12V, -1V, and -30 mV. The +30, -30, +60V Divider is a 10 to 1 voltage divider.

Thus, with the precision dividers, the calibration of the A/D Converter can be checked; with the +30V, -30V, +60V Divider, the Power Supply +30V -30V, and +60V can be checked. The other Power Dupply dc voltages are monitored by the A/D Converter without attenuation.

5.1.13 One-Time Command Status/Break Seal - Dust Cover Monitor

Schematic diagram of the One-Time Command Status/Break Seal-Dust Cover Monitor is shown in Figure 5.1.13-1.

The One-Time Command Status monitor is a ladder network used to indicate the status of the One-Time Command registers. Inputs to the ladder are One-Time Command Register (OTCR) 2 and OTCR 4. When no commands are initiated, OTCR2 and OTCR4 are at a "0" level, and the analog output of the ladder is approximately 100 mV. This is monitored by the A/D converters.

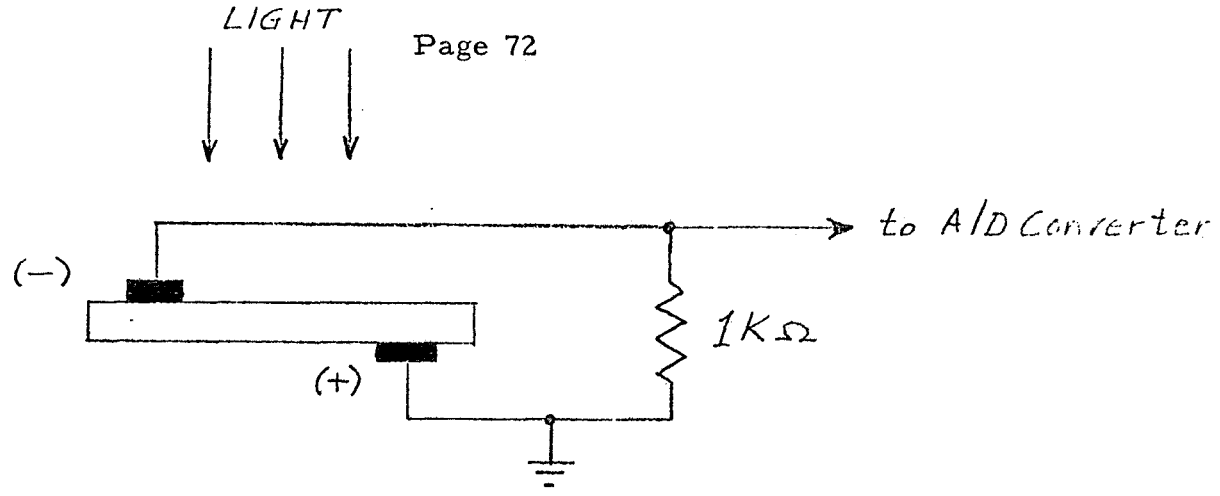


FIGURE 5.1.11-1, Solar Cell, Schematic

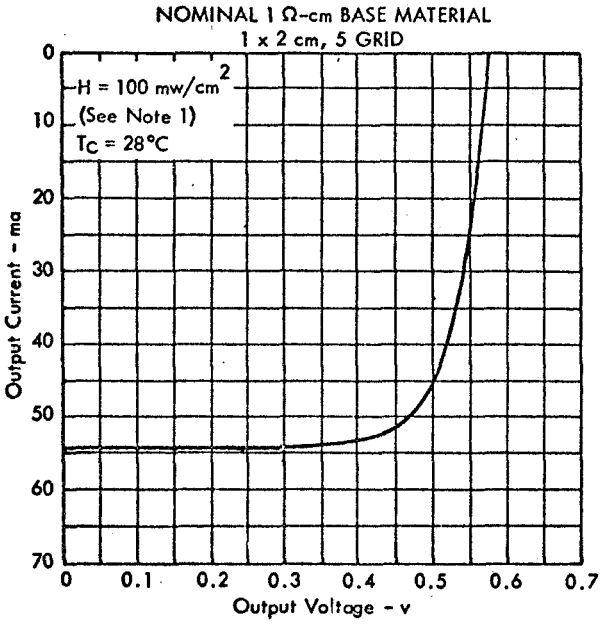


FIGURE 5.1.11-2, Solar Cell Current-Voltage Characteristics

NOTE 1: Input light intensity is equivalent to 100 mw/cm^2 of sunlight at the earth's surface. The source is reflector-type tungsten-filament bulbs operating at 2800°K ± 50°K color temperature filtered by 3 cm of deionized water and one thickness of 1/4 inch plate glass.

PARTS DISPOSITION				SK609725
1. USE 2. REWORK	3. CANNOT BE REWORKED 4. RECORD	5.....		

REVISIONS

DISP	EFF	SYM	DESCRIPTION	BY	DATE	CK'D	APPROVAL

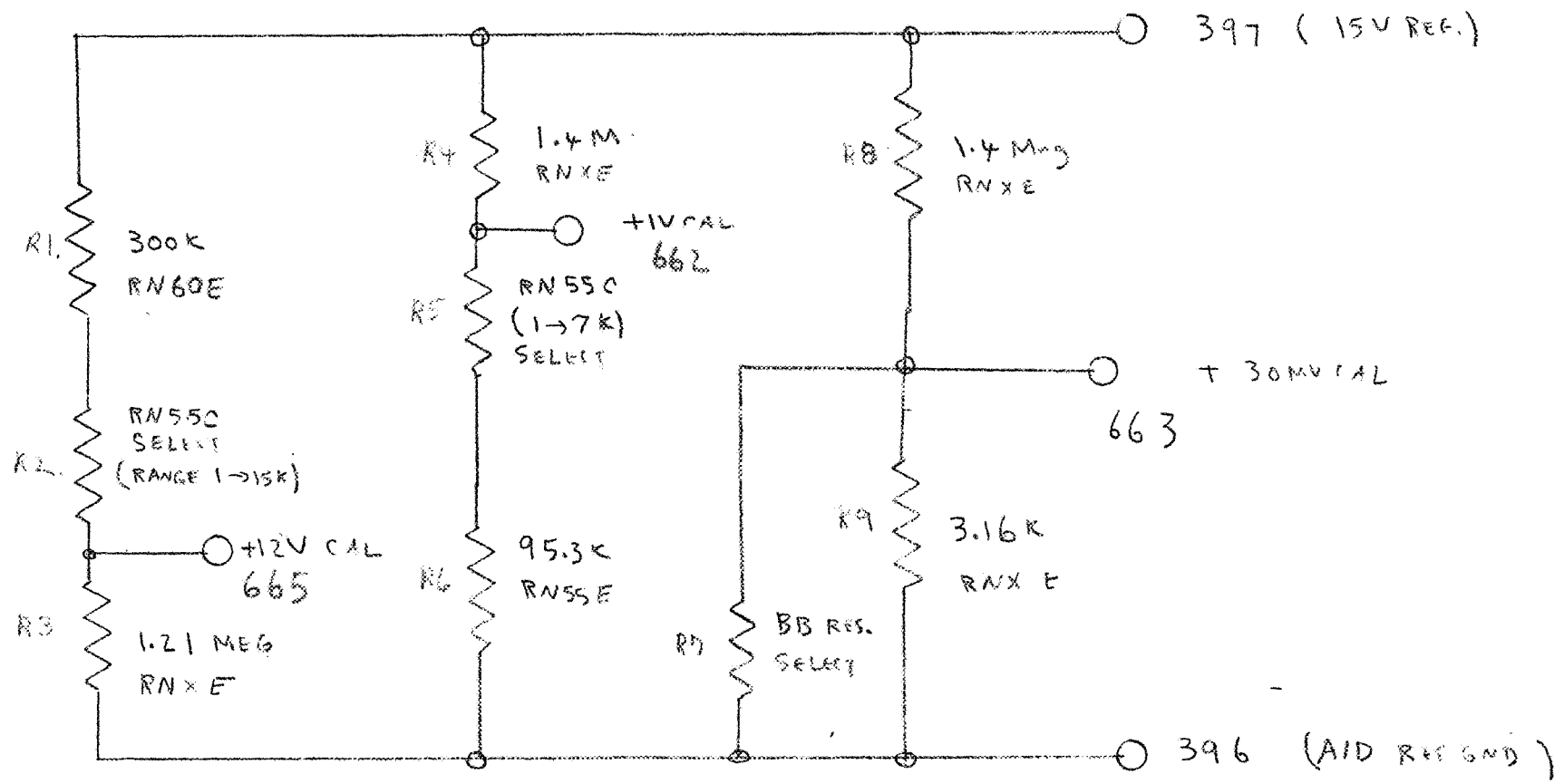


Figure 5.1.13-1. Positive Calibration Voltage Divider.

REQD	PART NO	DESCRIPTION	CKT REF	ITEM

LIST OF MATERIALS

FINISH

HEAT TREAT

DO NOT SCALE DRAWING

NEXT ASSY	USED ON	NEXT ASSY	FINAL ASSY
APPLICATION		QTY REQD	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS IN INCHES

HOLE DIA.	TOLERANCE
.0135 THRU .125	+.004-.001
.126 THRU .250	+.005-.001
.251 THRU .500	+.006-.001
.501 THRU .750	+.008-.001
.751 THRU 1.000	+.010-.001
1.000 THRU 2.000	+.012-.001
2.001 AND OVER	LINEAR

LINEAR TOLERANCES
.XXX = ±.010
.XX = ±.03
.X = ±.1

ANGLES = ±0°30'
SURFACE ROUGHNESS PER MIL-STD-10 ✓

DRAWN	[illegible]	2 Feb 68
CHECK	[illegible]	2/9/68
STRESS		
APP'D		
APP'D		
APP'D		

+ CALIBRATION VOLTAGE DIVIDER W7164

SCALE | WEIGHT

MARSHALL LABORATORIES

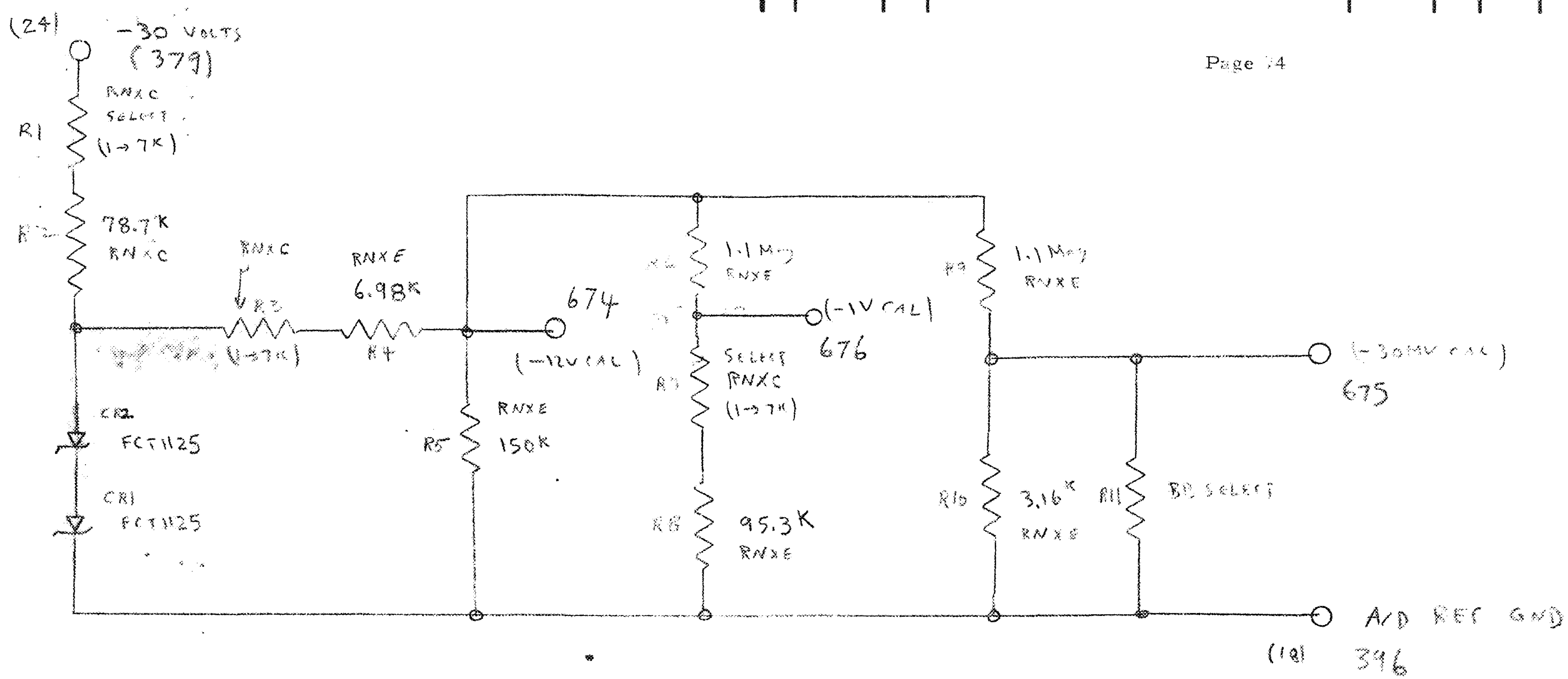
DWG SIZE B | SK609725 | SHEET 1 OF 1

S1966-14 FEB 1 6 1968 CODE IDENT NO. 13126

PARTS DISPOSITION		SK609738
1. USE 2. REWORK	3. CANNOT BE REWORKED 4. RECORD 5......	

REVISIONS

DISP	EFF	SYM	DESCRIPTION	BY	DATE	CK'D	APPROVAL



REQD	PART NO	DESCRIPTION	CKT REF	ITEM

LIST OF MATERIALS

FINISH

HEAT TREAT

Figure 5.1.12-?. Negative Calibration Voltage Divider.

DO NOT SCALE DRAWING

UNLESS OTHERWISE SPECIFIED		
DIMENSIONS IN INCHES		
HOLE DIA.	TOLERANCE	LINEAR TOLERANCES
.0135 THRU .125	+.004-.001	.XXX = ±.010
.126 THRU .250	+.005-.001	.XX = ±.03
.251 THRU .500	+.006-.001	.X = ±.1
.501 THRU .750	+.008-.001	
.751 THRU 1.000	+.010-.001	ANGLES = ±0°30'
1.000 THRU 2.000	+.012-.001	SURFACE ROUGHNESS
2.001 AND OVER	LINEAR	PER MIL-STD-10

NEXT ASSY	USED ON	NEXT ASSY	FINAL ASSY
APPLICATION		QTY REQD	

DRAWN	[signature]	9 Feb 8
CHECK	[signature]	2/1/68
STRESS		
APPD		
APPD		
APPD		

NEGATIVE CAL.
DIVIDER
W7176

SCALE | WEIGHT

MARSHALL LABORATORIES

DWG SIZE B | SK609738

SHEET 1 OF 1

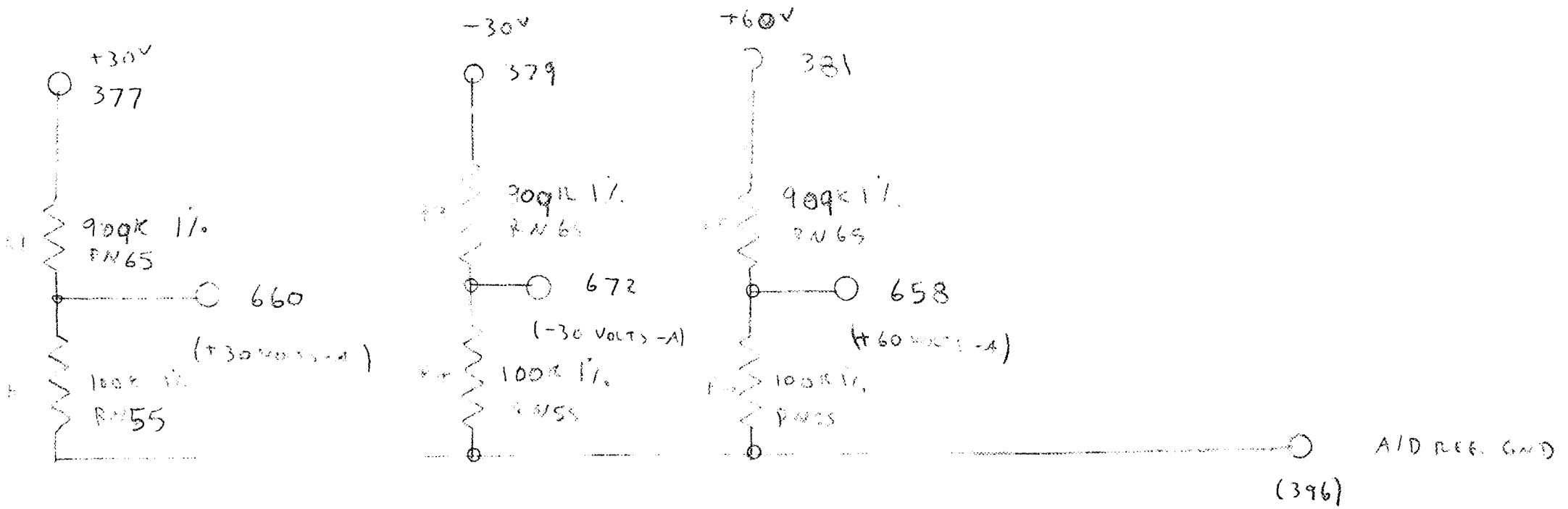
CODE IDENT NO. 13126

S1966-14

PARTS DISPOSITION				DWG NO	REV
1. USE 2. REWORK	3. CANNOT BE REWORKED 4. RECORD	5.		SK609735	

REVISIONS

DISP	EFF	ZONE	REV	DESCRIPTION	BY	CK	DATE	APPROVAL



QTY REQD PER NOTED ASSY					
CONFIGURATION					
LAYOUT NO					
DIST CODE					
DASH NO	MODEL NO	NEXT ASSEMBLY	MODEL NO	FINAL ASSEMBLY	MODEL NO
APPLICATION					

PART NO	SPECIFICATION	NOMENCLATURE OR DESCRIPTION	ELEC REF DES	CODE IDENT	ZONE	ITEM NO

LIST OF MATERIALS

INTERPRET THIS DRAWING PER STANDARDS IN MIL D-70327

DIMENSIONS ARE IN INCHES

TOLERANCES ON
DECIMALS
X ± .1
XX ± .03
XXX ± .010
ANGLES ± 0° 30'
XXXX ± .0050

SURFACE ROUGHNESS

HOLE DIA	TOLERANCE
.0185 THRU .125	±.004 .001
.126 THRU .250	.005 .001
.251 THRU .500	.006 .001
.501 THRU .750	.008 .001
.751 THRU 1.000	.010 .001
1.001 THRU 2.000	.012 .001
2.001 AND OVER	LINEAR

CONTRACT NO	
DRAWN	DATE
CHECK	
MECH ENG	
ELECT ENG	
PROJ MGR	
APPR	
DESIGN ACTIVITY APP'D	
CUSTOMER	

MARSHALL LABORATORIES
TORRANCE, CALIFORNIA

TITLE
+30, -30, +60V
DIVIDER
W7172

Figure 5.1.12-3

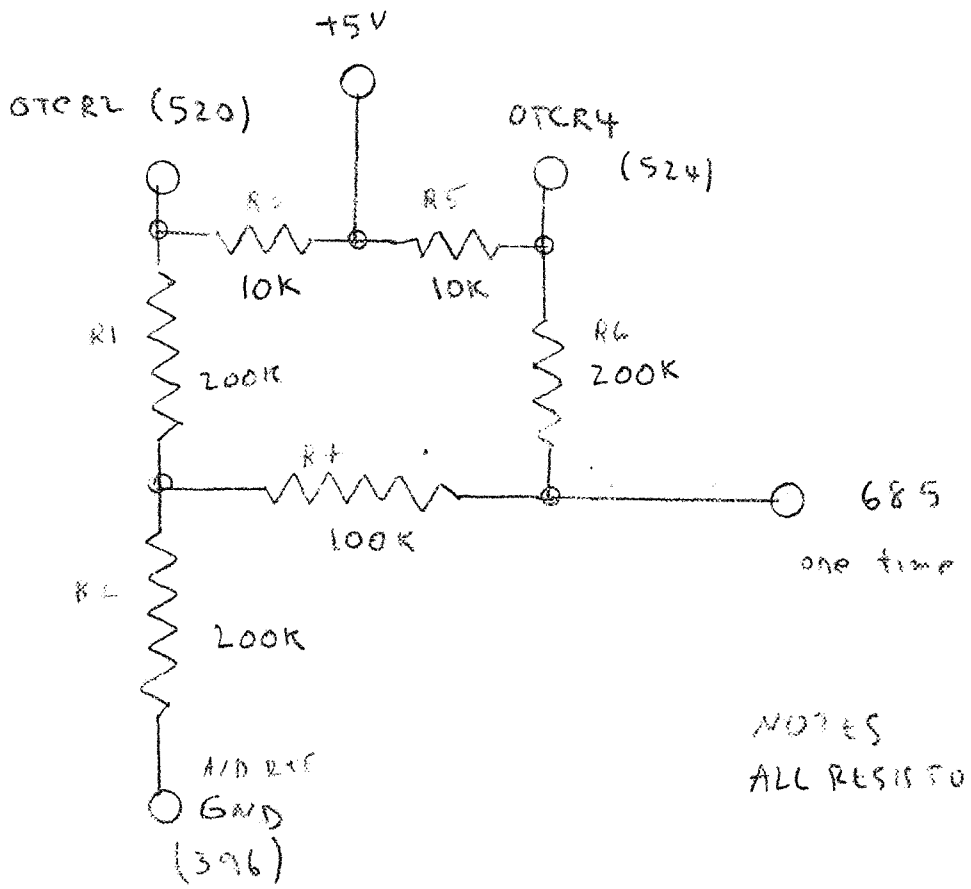
SIZE	CODE IDENT NO	DWG NO	REV
B	13126	SK609735	

SCALE | RELEASED | SHEET 1 OF 1

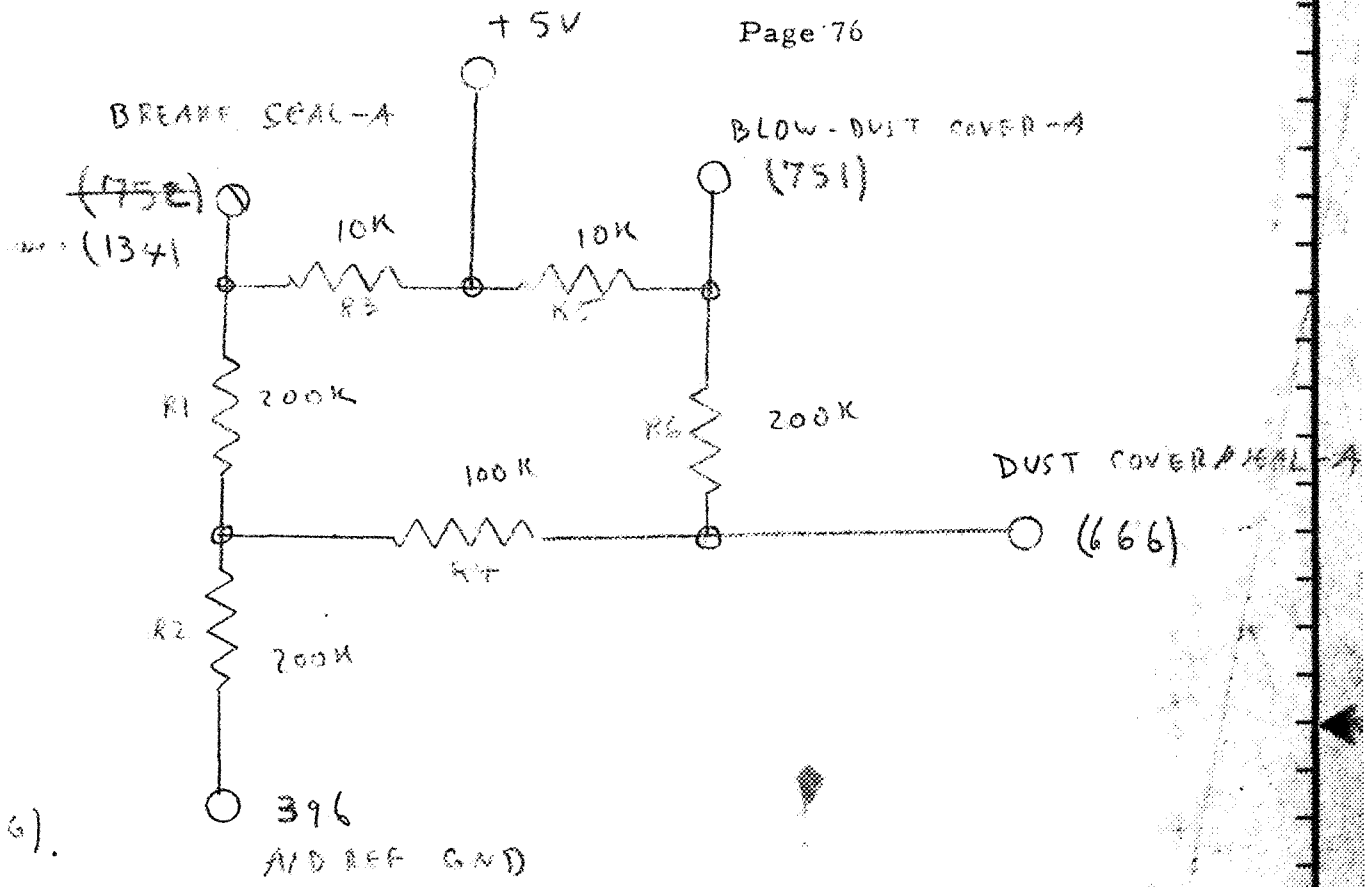
PARTS DISPOSITION					DWG NO.	REV
1. USE 2. REWORK	3. CANNOT BE REWORKED 4. RECORD	5.			SK609727	

REVISIONS

DISP	EFF	ZONE	REV	DESCRIPTION	BY	CK	DATE	APPROVAL



NOTES
ALL RESISTORS 8B



PART NO.	SPECIFICATION	NOMENCLATURE OR DESCRIPTION	ELEC REF DES	CODE IDENT	ZONE	ITEM NO.

LIST OF MATERIALS

DASH NO.	MODEL NO	NEXT ASSEMBLY	MODEL NO	FINAL ASSEMBLY	MODEL NO

APPLICATION

QTY REQD PER NOTED ASSY
CONFIGURATION
LAYOUT NO.
DIST CODE

INTERPRET THIS DRAWING PER STANDARDS IN MIL-D-70327
DIMENSIONS ARE IN INCHES
TOLERANCES ON DECIMALS
X ± 1
XX ± 03
XXX ± 010
XXXX ± 0050
ANGLES ± 0 30'
√ SURFACE ROUGHNESS

HOLE DIA	TOLERANCE
0135 THRU 125	.004 - 001
126 THRU 250	.005 - 001
251 THRU 500	.006 - 001
501 THRU 750	.008 - 001
751 THRU 1.000	.010 - 001
1.001 THRU 2.000	.012 - 001
2.001 AND OVER	LINEAR

CONTRACT NO	S1966-10	
DRAWN	J. Lunke	DATE 9 Feb 68
CHECK		
MECH ENG		
ELECT ENG	D... A. S...	2/12/68
PROJ MGR		
APPR		
DESIGN ACTIVITY APPD		
CUSTOMER		

M L **MARSHALL LABORATORIES**
TORRANCE, CALIFORNIA

TITLE
ONE TIME COMMAND STATUS / BREAK SEAL / DUST COVER - W7172
Figure 5.1.13-1

SIZE	CODE IDENT NO.	DWG NO.	REV
B	13126	SK609727	

SCALE | RELEASED FEB 13 1968 | SHEET 1 OF 1

ML FORM 197

When one-time commands 2 and 8 (Break Seal and Blow Dust Cover, respectively) are initiated, OTCR2 and OTCR4 are at a "1" level, and the output of the ladder is approximately 3.5V. Thus the digital status of the OTCR's is processed by the A/D Sub Com and read out to the readout system.

The Break Seal Dust Cover monitor is a ladder network which monitors the status of the CCIG Seal and of the Dust Cover. Inputs to the ladder are:

- Break Seal Monitor: A level taken from the CCGE Electrometer Seal Break circuit. This level is normally at "1".
- Blow Dust Cover Monitor: A normally up output of the Dust Cover Monitor flip-flop.

See Table 5.1.13A for the Break Seal - Dust Cover monitor output for each status condition. Output of the ladder is monitored by the A/D Converters.

TABLE 5.1.13A: Break Seal - Dust Cover Monitor Status

Seal Broken	Dust-Cover Open	Monitor Output
No	No	3.5V
Yes	No	2.4V
Yes	Yes	0.09V
No	Yes	1.2V

5.2 Low Energy Ion Detector

5.2.1 Calibration Pulser; Calibration Rate Counter

The Calibration Pulser provides a means of calibrating and checking the SIDE system. It is a 560 kHz crystal oscillator; its output is divided down to 17.5 kHz and 137 Hz by the

Calibration (Cal) Rate Counter, and is controlled by a programming system to feed the Channeltron preamplifiers.

Figure 5.2.1-1 shows a block diagram of the SIDE In-Flight Calibration. The Cal Rate Counter accepts the 560 kHz output from the Calibration Pulser, and divides it down to 17.5 kHz and 137 Hz. The Cal Rate Counter Decoder has two programmed outputs: one for High Energy Cal Rate (HE Cal Shaper), one for Low Energy Cal Rate (LE Cal Shaper). The outputs are present only during the Calibration Cycle. At that time, the outputs are gated such that the generated frequencies are presented to the Cal Shapers in the format shown in Table 5.2.1A.

TABLE 5.2.1A: Calibrate Frequencies

SIDE FRAME	FREQUENCY (Hz)
120	0
121	137
122	17.5 k
123	560 k
124	0
125	137
126	17.5 k
127	560 k

The Cal Shapers provide a fast transition time necessary to drive through the 1 pfd Calibration Input capacitors of the Channeltron Preamplifiers. Outputs of the Cal Shapers drive their respective Channeltron preamplifiers, outputs of which feed the discriminators which drive the Log Count Rate Meters and Accumulators.

Information from the SIDE Frame Counter and the High Energy Counter forms the programming logic which selects the Cal Rate frequency.

REF DRAWING W7132 (CALIBRATION PULSER)
SK609713 (CAL RATE COUNTER)

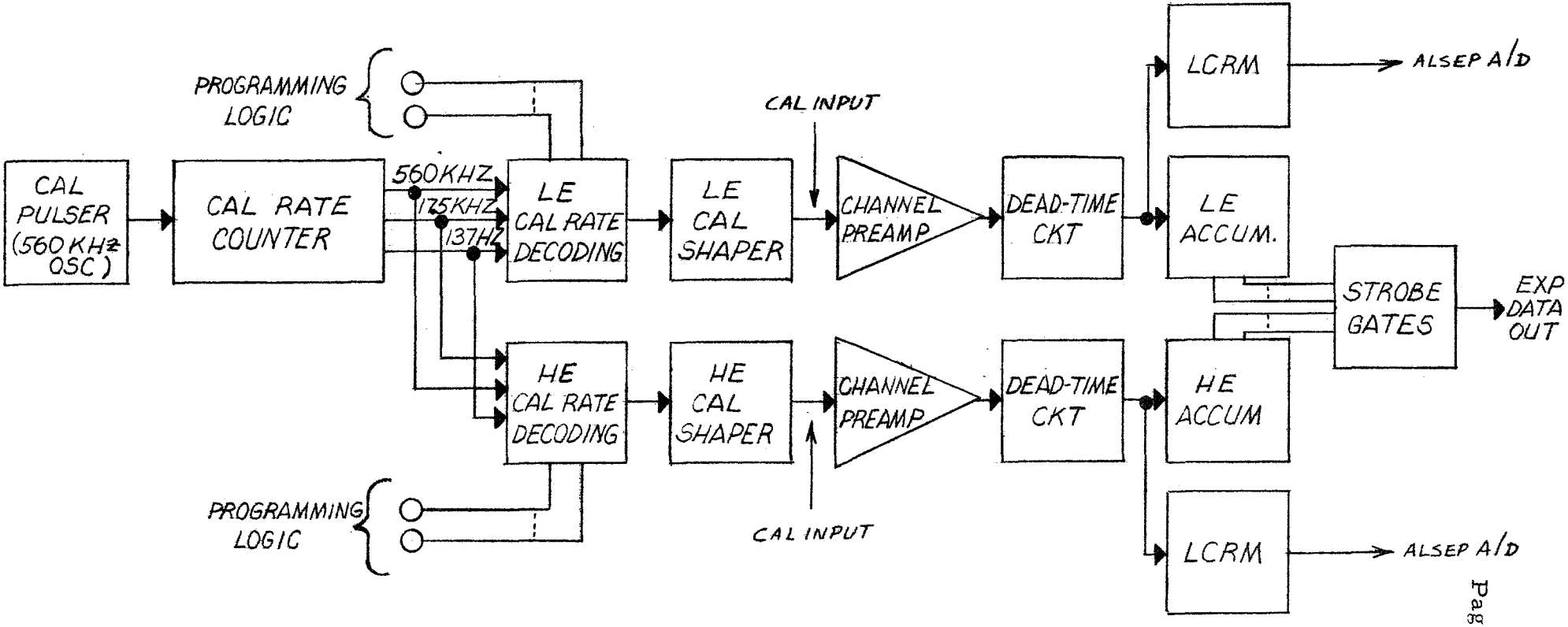


FIG. 5.2.1-1 SIMPLIFIED BLOCK DIAGRAM, SIDE IN-FLIGHT CALIBRATION

5.2.2 -3.5 kV Power Supply

Figure 5.2.2-1 shows a Block diagram of the -3.5 kV Power Supply.

The -3.5 kV Power Supply is used to develop a negative 3500 volt bias potential for the Channeltron (R) Electron Multipliers in the High Energy and Low Energy Channeltron Amplifiers.

The supply consists basically of a regulator, converter, a voltage-multiplier network, and associated feedback networks and ON/OFF control. The regulator is driven by the +30V output of the Low Voltage Power Supply. The regulator furnishes approximately 25V to the converter for conversion to a 5 kHz square wave to be applied to the converter transformer. Output of the converter transformer is applied to a voltage multiplier network (stacked standard doublers). The output is then filtered and applied to both Channeltrons. The output is also divided down for Analog-to-Digital conversion, and monitored at various SIDE Frames (during Word 2) according to the format in drawing 609206 (Figure 3.0-3).

During pre-flight tests at ambient air pressures, a lockout plug is connected to the system, grounding the collector of Q1 (Figure 5.2.2-1, Block Diagram of -3.5 kV Power Supply). This causes the regulator to be inhibited and the high voltage output to be zero. Prior to flight (or simulated flight), the lockout plug is removed, causing the -3.5 kV Power Supply to be ON automatically when power is applied to the system (the $\overline{\text{-3.5 kV ON/OFF}}$ logic control function is normally at a "0" state). When Command 14 (Channeltron High Voltage ON/OFF) is executed, the -3.5 kV ON/OFF logic control function switches to a "1" state, turning "ON" Q1. This inhibits the regulator and turns the high voltage OFF. Executing Command 14 once more turns the high voltage back ON.

5.2.3 Channeltron Preamplifier

The Channeltron Preamplifier accepts the current pulses from the Channeltron and provides an input to the discriminator/deadtime circuit. The Channeltron Preamplifier is optimized for the expected signal characteristics of the channeltrons and allows for variations from channel to channel, life degradation, supply voltage changes, and the statistical variations in Channeltron output.

The Channeltron Preamplifier consists of a front-end charge-sensitive amplifier (CSA) and a discriminator set for a threshold level of about 40 mV. See Figure 5.2.3-1 for the block diagram of the Channeltron Preamplifier.

(REF DRAWING 609585)

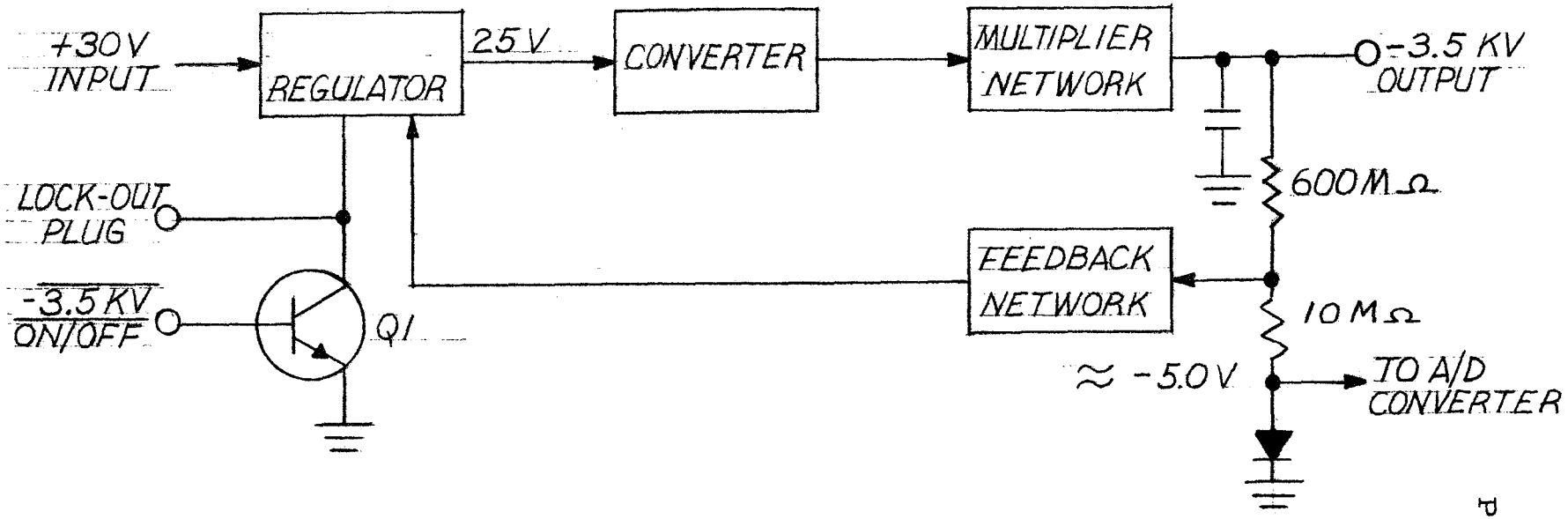


FIG. 5.2.2-1 SIMPLIFIED BLOCK DIAGRAM, -3.5 KV POWER SUPPLY

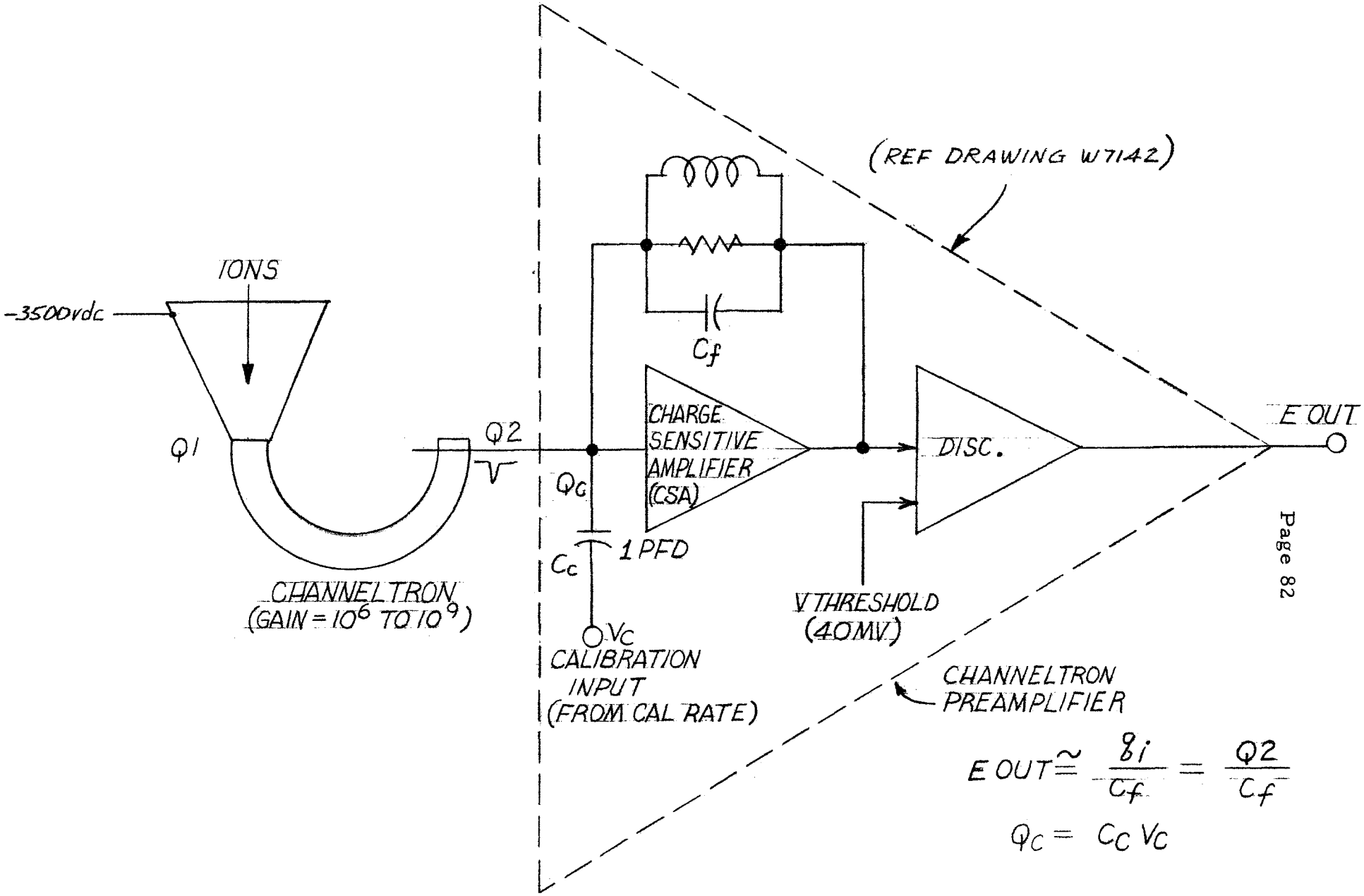


FIG. 5.2.3-1 BLOCK DIAGRAM, CHANNELTRON PREAMPLIFIER

Positive ions enter the funnel of the channeltron, causing secondary emission of electrons within the coated glass walls. An amplifier charge (negative pulse) is seen by the input to the front section of the preamplifier, the CSA. Gain of the Channeltron is about 10^6 to 10^9. Thus,

$$Q2 \cong (10^6 \text{ to } 10^9)\ Q1$$

See Figure 7-9 and Table 7B (Section 7.0, Mechanical and Thermal Design) for specifications of the Channeltron (R) Electron Multiplier.

Output of the charge-sensitive amplifier is given by

$$Eout \cong \frac{q_i}{C_f} \cong \frac{Q_2}{C_f}$$

The discriminator detects the output of the CSA above 40 mV, and then drives the dead time circuit. Final output to the dead time circuit is from 0.2V to 3V, negative pulse of approximately 50 nanoseconds pulse width.

The preamplifier also accepts calibration input pulses. This is done as part of the calibration system. Output of the Cal Rate drives the Cal Shaper which provides a fast transition time in order to couple through the calibration input capacitor of the Channeltron Preamplifier. In this case, the charge Qc presented to the CSA is

$$Q_c = C_c V_c$$

where V_c = Cal Voltage Input

C_c = Cal Coupling Capacitor

Figure 5.2.3-2 shows a computer-derived gain-phase frequency plot of the Charge Sensitive Amplifier, open loop condition.

5.2.4 Dead Time Circuit

See Figure 5.2.4-1 for the block diagram of the Dead Time Circuit.

The Dead Time Circuit consists of a non-inverting, unity-gain buffer amplifier and two one-shots with a built-in

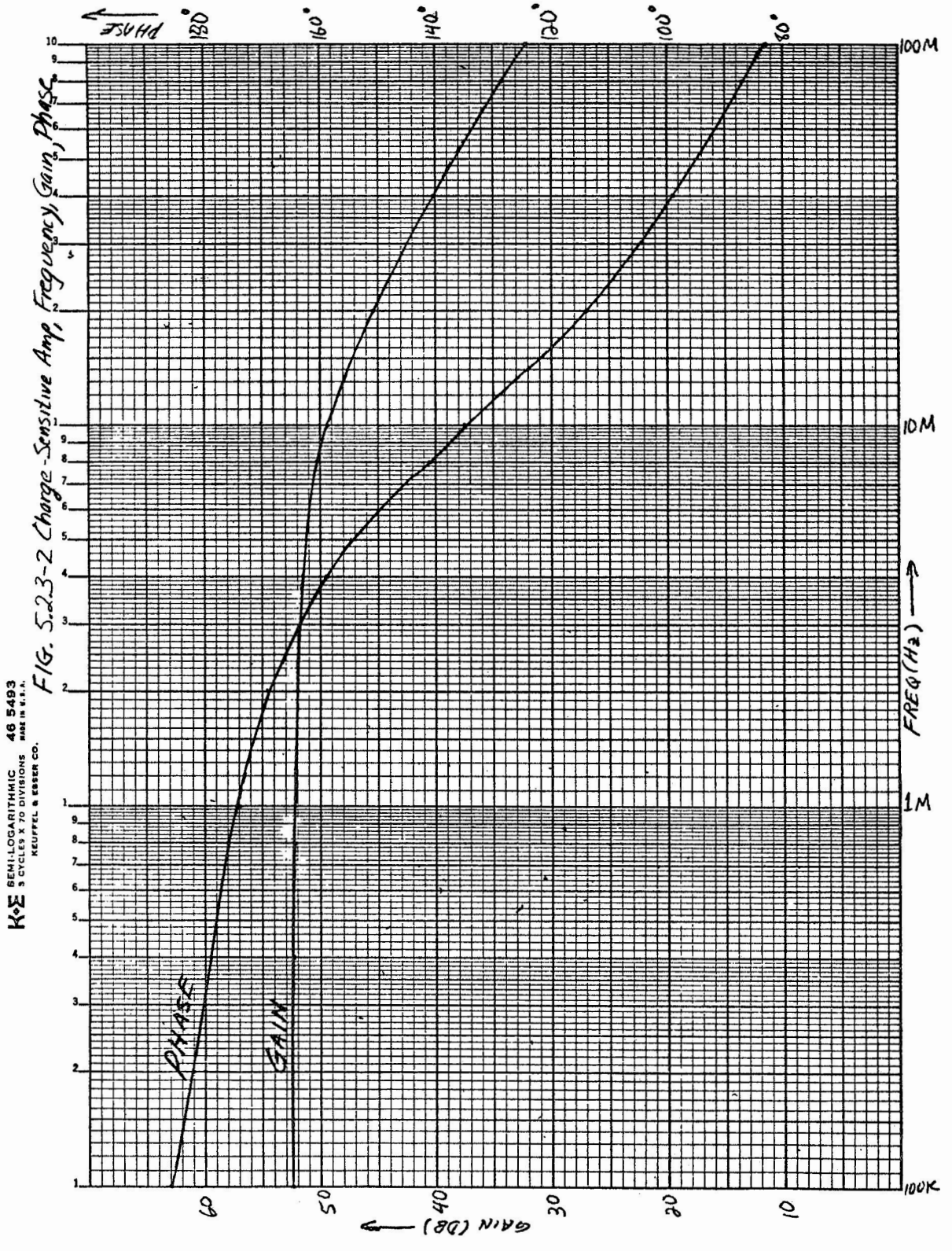


FIG. 523-2 Charge-Sensitive Amp, Frequency, Gain, Phase

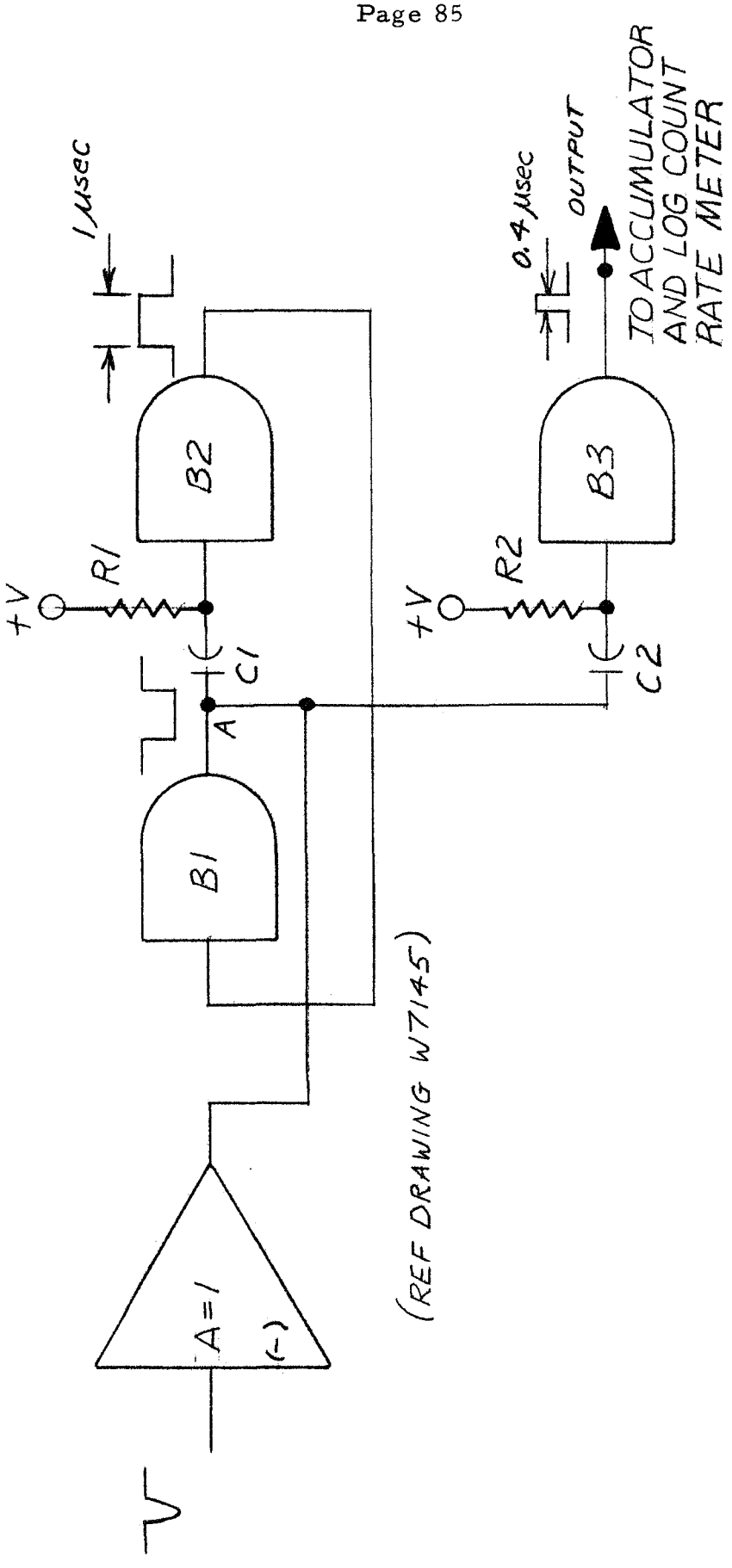


FIG. 5.2.4-1, BLOCK DIAGRAM, DEAD TIME CIRCUIT

frequency-limiting feature. A Dead Time Circuit is provided for each detection system, HE and LE.

The Dead Time Circuit accepts the 50 nanosecond wide output pulses from the Channeltron Preamplifier. After passing through the unity-gain amplifier, the pulse is applied to a coupling capacitor. The normally UP output of nand-gate B1 (point A, Figure 5.2.4-1) is also tied to the output of the unity-gain amplifier.

After ac coupling to nand-gate B2, the pulse is inverted and fed back to the input of B1. Thus, regeneration holds the output of B1 down, until the charging rate of R_1C_1 allows the input of B2 to be driven and thus forces the output of B2 back down. This pulse width, determined by R_1C_1, is approximately 1 μsec.

When the output of B1 initially switches down, C2 couples the output, causing B3's normally-down output to switch to a "1". The charging rate of R_2C_2 causes the output of B3 to switch back down after 0.4 μsec.

During the time the regeneration process holds the output of B1 down, an incoming channeltron pulse will have no effect. Therefore, for a period of up to 1 μsec (the "dead time" period) after the incidence of an input pulse, additional pulses are inhibited. Frequency limiting is thus affected.

The 0.4 μsec output pulse of the Dead Time Circuit is applied to the Accumulator and the Log Count Rate Meter.

5.2.5 Log Count Rate Meter

Refer to Figure 5.2.5-1 for a simplified block diagram of the Log Count Rate Meter (LCRM). The LCRM serves as a back-up and a "quick-look" device. It consists of a one-shot circuit which produces a 0.3 μsec pulse for every input pulse for the Dead Time circuit. The one-shot output is fed into a non-linear circuit with logarithmic characteristics.

The dc output of the non-linear circuit is proportional to the logarithm of the input frequency. It is fed to a differential amplifier; the output of the amplifier is thus a dc level which is a function of the log of the repetition rate of the incident ions on the Channeltron (R) Detectors. The output is fed to the ALSEP Central Station A/D Converters for conversion to digital data.

Table 5.2.5A tabulates the LCRM Amplifier output as a function of specified input frequencies for a typical system.

REF DRAWING W7173 (LOG COUNT RATE METER)
W7174 (LCRM AMPLIFIER)

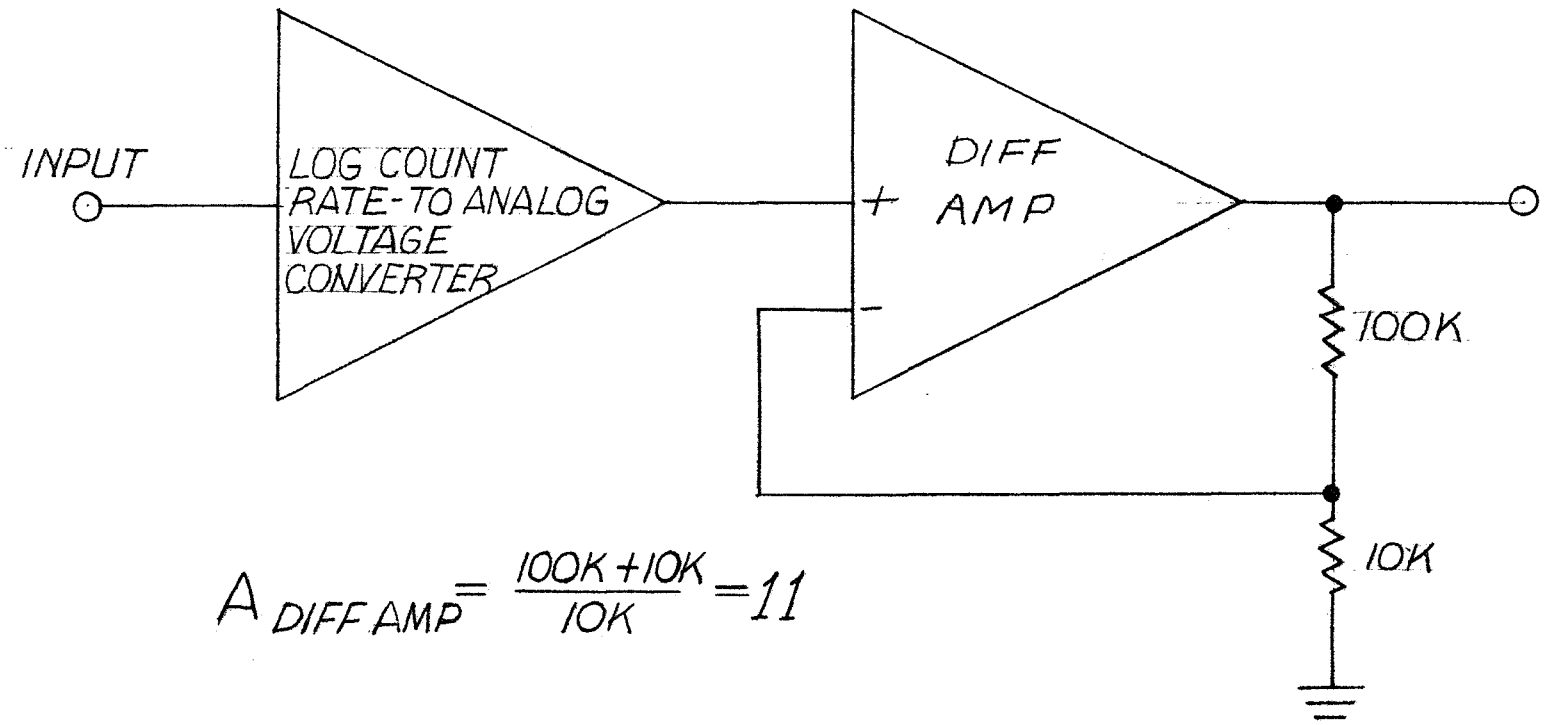


FIG. 5.2.5-1 SIMPLIFIED BLOCK DIAGRAM, LOG COUNT RATE METER

Figure 5.2.5-2 shows a typical plot of output voltage versus input frequency, for temperatures ranging from -50°C to + 90°C.

TABLE 5.2.5A: Log Count Rate Meter, Output vs Frequency

Frequency, (Hz)	Output, (Volts)
0	0.013
17	0.629
139	1.400
2.19K	2.500
17.5K	3.360
70K	3.830
560K	4.400

5.2.6 Low Energy Accumulator

The Low Energy Accumulator is a twenty-bit counter which accumulates the number of output pulses of the Low Energy Descriminator (Dead Time Circuit) during the accumulation interval. The Low Energy Accumulation interval is the period of time between the beginning of Word 1 and the beginning of Word 9's BD1 pulse. See Figure 5.2.6-1 for timing relationships of the accumulation interval and readout.

See Figure 5.2.6-2 for a block diagram of the accumulator.

The accumulator consists of two ten-bit counters with associated logic. The accumulation process is as follows.

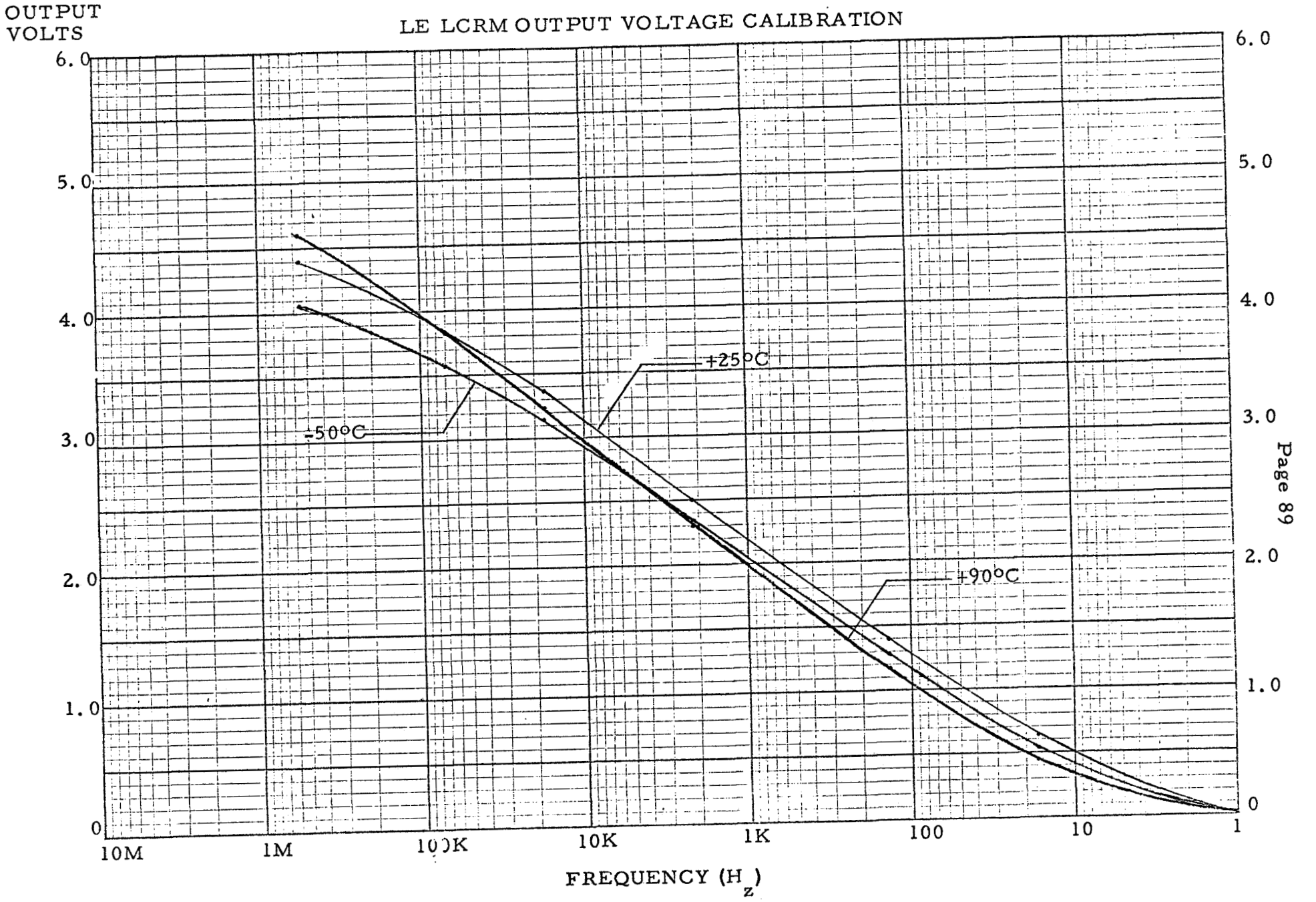


Figure 5.2.5-2 LCRM Output, Typical System

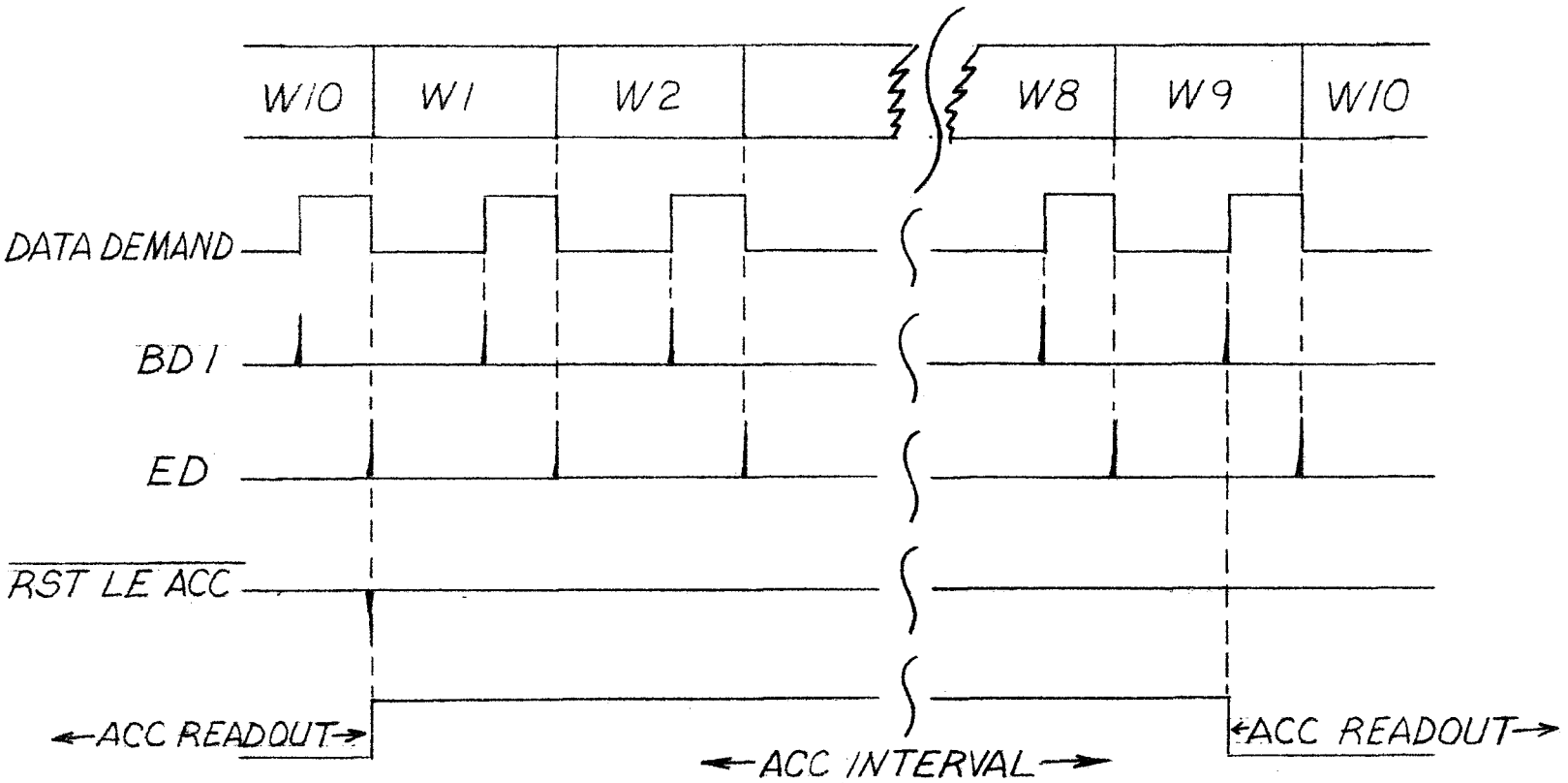
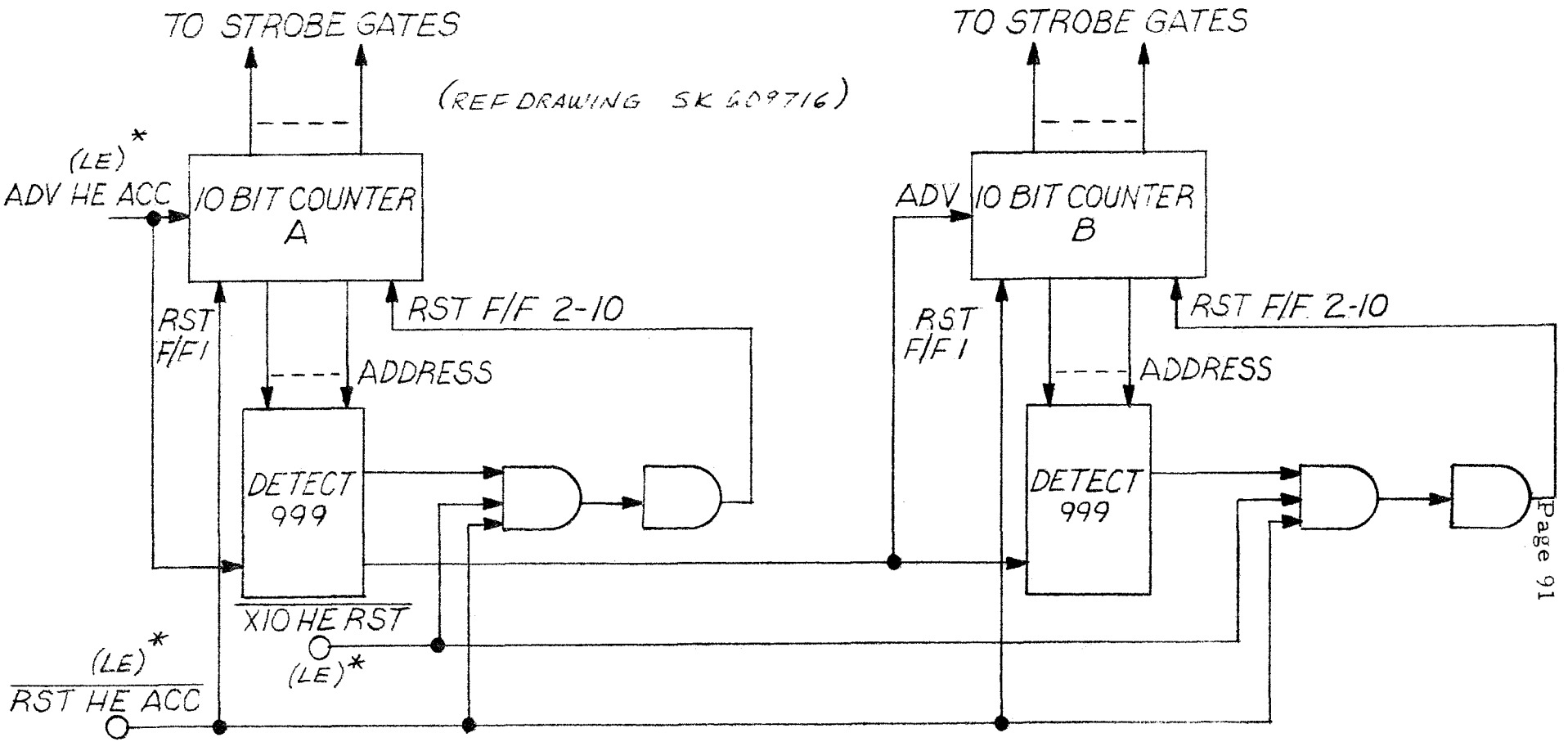


FIG. 5.2.6-1, LOW ENERGY ACCUMULATOR TIMING RELATIONSHIPS



*NOTE: SIDE CONTAINS 2 ACCUMULATORS. ALTERNATE LINE TITLES APPLY TO THE CORRESPONDING DETECTION SYSTEM

FIG. 5.2.6-2, ACCUMULATOR (HIGH ENERGY & LOW ENERGY) BLOCK DIAGRAM

The counters initially are cleared when the first Word 1 occurs after application of power. At Word 1, the Logic Timing gates the output pulses of the Low Energy Discriminator (Dead Time Circuit to produce the Advance LE Acc pulses.

The ten-bit counter A (Figure 5.2.6-2 addresses the detect -999 circuit. When 999 counts have been detected, a toggle pulse is generated to advance the ten-bit counter B. At the same time, ten-bit counter A is reset. At this time, for example, the decimal equivalent of the contents of the counters are as follows:

Counter B (Most Significant Digits) Counter A (Least Significant Digits)

0 0 1 0 0 0

or 001,000

Thus, Counter A represents the least significant digits and Counter B the most significant digits of the total accumulation count.

The Advance LE Accumulator pulse is inhibited by a detect -999996 circuit in the Logic Timing section to prevent overfill of the counters. The Reset LE Acc pulse is generated to reset the accumulator when either of the two following situations occur:

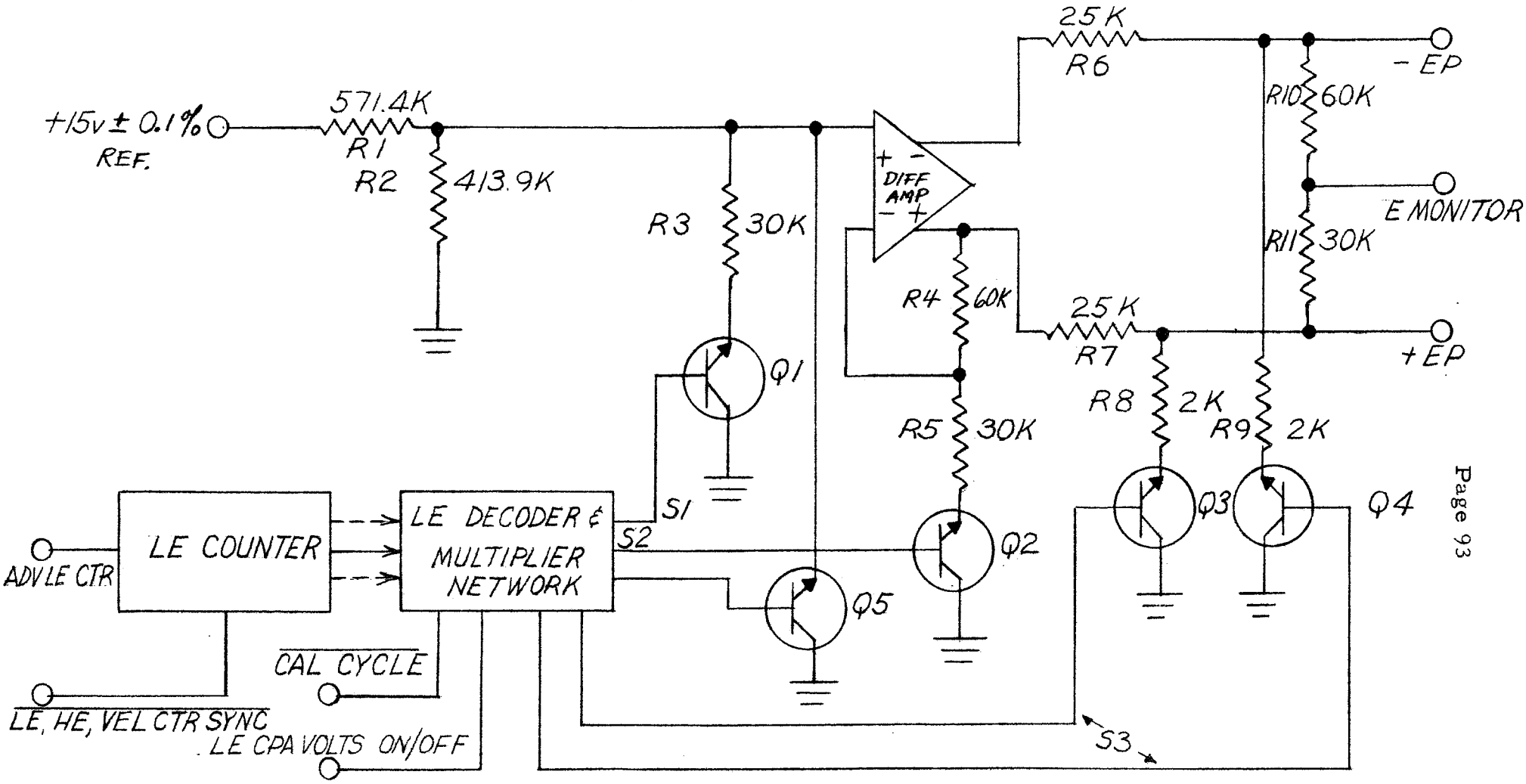
- When the End Data (ED) pulse and Word 1 are present.
- When X10 Accumulation Interval mode is in effect and the 10th accumulation interval in each SIDE frame is reached. See Figure 5.2.6-1, Accumulator Timing Relationships, for the exact timing of the Reset LE Acc pulse.

The accumulator also addresses the Strobe Gates, which convert the data to serial form for readout. Low Energy Accumulator data is read out in Word 9 and 10 as shown in Figure 5.2.6-1.

5.2.7 Low Energy Step Voltage Generator

A simplified block diagram of the Low Energy Step Voltage Generator is shown in Figure 5.2.7-1. The purpose of the Low Energy Step Voltage Generator is to generate a total of six voltage steps (positive and negative) to be applied to both plates of the Low Energy Curved Plate Analyzer. The potentials generated are shown in Table 5.2.7A. Also shown are the voltages monitored for analog-to-digital conversion.

REF DRAWINGS SK609707 (VELOCITY FILTER AND LOW ENERGY COUNTER)
SK609959 (LOW ENERGY CPA STEP VOLTAGE GENERATOR)



SIMPLIFIED BLOCK DIAGRAM LOW ENERGY STEP VOLTAGE GENERATOR, FIG 5.2.7-1

TABLE 5.2.7A: Low Energy CPA and A/D Monitor Voltages

Energy Step	Plate Voltage	Monitor Voltage
1	12.22	4.07
2	4.07	1.36
3	1.29	0.429
4	0.430	0.143
5	0.143	0.0474
6	0.0476	0.0158

(Plate voltage carries the sign of the associated plate, and is referenced to ground)

Low Energy Voltage data is read out during Word 8. Appendix IV shows a worst case error analysis of the LE Step Voltage Generator.

5.2.7.1 Low Energy Counter

The Low Energy Counter is a parallel three-bit counter, providing a binary count necessary to properly address the Low Energy Decoders. The output counting sequence of the Low Energy Counter is shown in Table 5.2.7B.

The counter is advanced through six energy steps by the Advance Low Energy Counter pulse, which is generated at Word 9 by the Velocity Filter Detector 19 or Detect 9 circuit. Under normal conditions, the Detect -19 circuit is operative, and generates the Advance Low Energy Counter pulse at the twentieth velocity step. When Command 4 or Command 6 is generated, the Velocity Filter Detect-9 circuit is operative, and the Advance Low Energy Counter pulse is generated at the tenth Velocity Step. After counting through the six energy steps, the Low Energy Counter will recycle to Step 1 to begin the counting sequence over again. Figure 5.2.7-2 shows the timing relationships for the Advance Low Energy Counter pulse.

The Low Energy Counter is reset by the $\overline{\text{LE, HE, VEL Ctr Sync}}$ pulse when any of the following conditions exist:

- Side Frame 127 (or 10, 39, or 79, depending upon the ground command executed) is reached.
- Power is applied to the system.
- A command is executed which resets the SIDE Frame Counter.

See Figure 5.2.8-3 for timing relationships between Power On and the $\overline{\text{LE, HE, Vel Ctr Sync}}$ level.

5.2.7.2 Low Energy Decoder and Multiplier Network

The three-bit output of the Low Energy Counter is fed to the Low Energy Decoder. The Low Energy Decoder, after decoding its input address from the counter, controls the state of the Multiplier Network.

The Multiplier Network switches are represented by transistors Q1, Q2, Q3, Q4, and Q5 in Figure 5.2.7-1, Simplified Block Diagram of the Low Energy Step Voltage Generator. The Multiplier Network, through the switching of Q1-Q5 in accordance with Table 5.2.7C, Address to Multiplier Network, controls the overall transfer function of the amplifier from the precision +15V source to the output to the Curved Plate Analyzer.

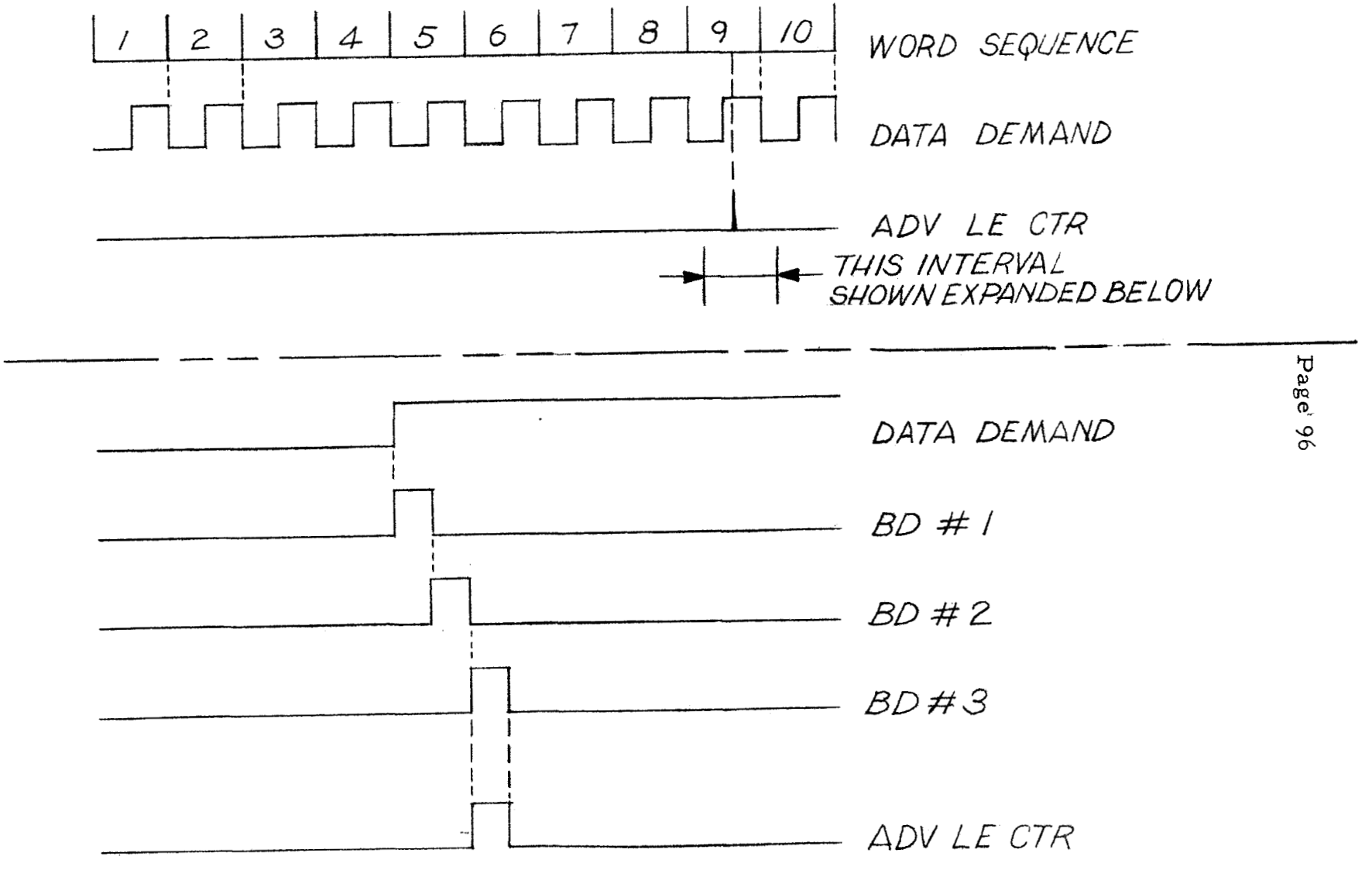


FIG 5.2.7-2 ADVANCE LE COUNTER TIMING

TABLE 5.2.7B: Low Energy Counter Output

Energy Step	LE Counter Output (Address to Decoder)		
	LE CTR 3	LE CTR 2	LE CTR 1
1	1	1	1
2	1	0	0
3	1	0	1
4	0	1	0
5	0	1	1
6	1	1	0

TABLE 5.2.7C: Address to Low Energy Multiplier Network

Energy Step	Address to Multiplier Network		
	S3	S2	S1
1	0	1	0
2	0	0	0
3	0	1	1
4	0	0	1
5	1	1	1
6	1	0	1

5.2.7.3 Low Energy Amplifier

The Low Energy Differential Amplifier is a single input, balanced double-output differential amplifier. The amplifier is driven by a precision +15V from the Velocity Filter +15V Reference Buffer. Input attenuation to the Low Energy Differential Amplifier is controlled by the switching of Q1 (See Figure 5.2.7-1). The feedback function is controlled by Q2, which shorts or opens R5 from ground. The output attenuation is controlled by the switching of Q3 and Q4.

Figure 5.2.7-3 shows the two standard configurations for the Low Energy Amplifier as Q2 is switched ON and OFF. Also shown are the gain equations for each case. See Table 5.2.7D for the input attenuation, amplifier gain, and output attenuation for each energy step and Multiplier address.

The Low Energy Step Voltage Generator is driven to produce zero output under the following two conditions:

- o During Calibrate Cycle: The $\overline{\text{Cal Cycle}}$ logic control function switches to a "0" state, turning Q5 "ON", and thus grounding the input to the Differential Amplifier. At the same time, S2 is switched to a "0" state, cutting off Q2. This reduces the gain of the Differential Amplifier to unity. Also, S3 is simultaneously switched to a "1" state, turning on Q3 and Q4 and connecting the positive and negative plate voltages to ground through a pair of 2 kilohm resistors.

- o Upon a Manual Low Energy CPA Volts ON/OFF Command: When an OFF command is transmitted, the LE CPA Volts logic control function switches to a "0" state. The OFF mode of the LE Step Voltage Generator is then generated in the same manner as during Calibrate Cycle, Step (b) above.

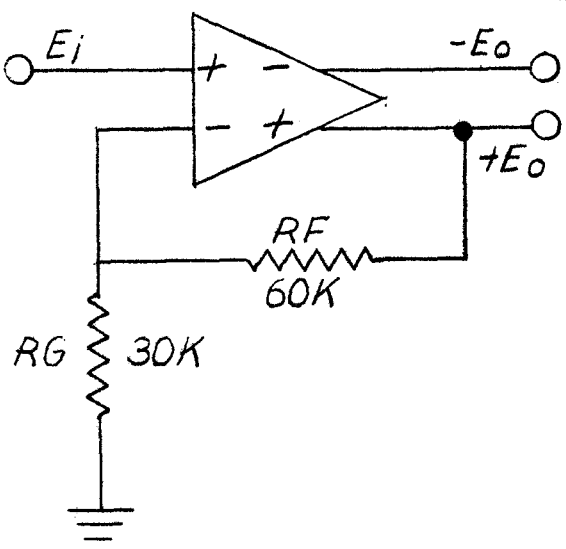
See Figure 5.2.7-4 for timing of the $\overline{\text{Cal}}$ Cycle logic control function.

The output divider circuit provides a stepped down voltage used for monitoring and analog-to-digital conversion. Table 5.2.7A shows the Low Energy Monitor voltages.

The monitor voltage is given by

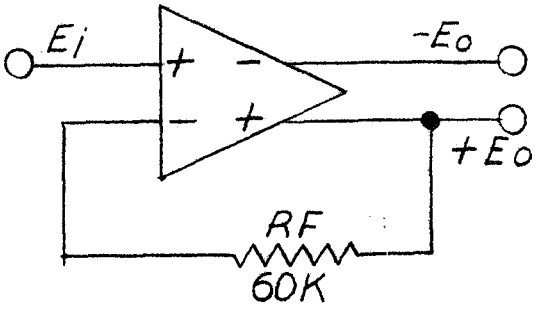
$$E_{mon} = \frac{+E_p}{3}$$

The monitored voltages are then fed to the analog-to-digital converters (q.v.). The commutated voltages are therby transformed by the A/D Converter into a binary readout proportional to the log of the monitored voltage.



$$GAIN = \frac{E_o}{E_i} = \frac{RF + RG}{RG} = \frac{90K}{30K} = 3$$

(a.) Q2 ON



$$GAIN = \frac{E_o}{E_i} = UNITY$$

(b) Q2 OFF

FIG 5.2.7-3, TWO CONFIGURATIONS OF THE LOW ENERGY DIFFERENTIAL AMPLIFIER

Energy Step	Input Attenuator		Feedback Function		Output Attenuator	
	S1	Transfer Function	S2	Diff. Amp Gain	S3	Transfer Function
1	OFF	.423	ON	3.00	OFF	.643
2	OFF	.423	OFF	1.00	OFF	.643
3	ON	.0446	ON	3.00	OFF	.643
4	ON	.0446	OFF	1.00	OFF	.643
5	ON	.0446	ON	3.00	ON	.0712
6	ON	.0446	OFF	1.00	ON	.0712

TABLE 5.2.7D

LOW ENERGY AMPLIFIER TRANSFER FUNCTIONS

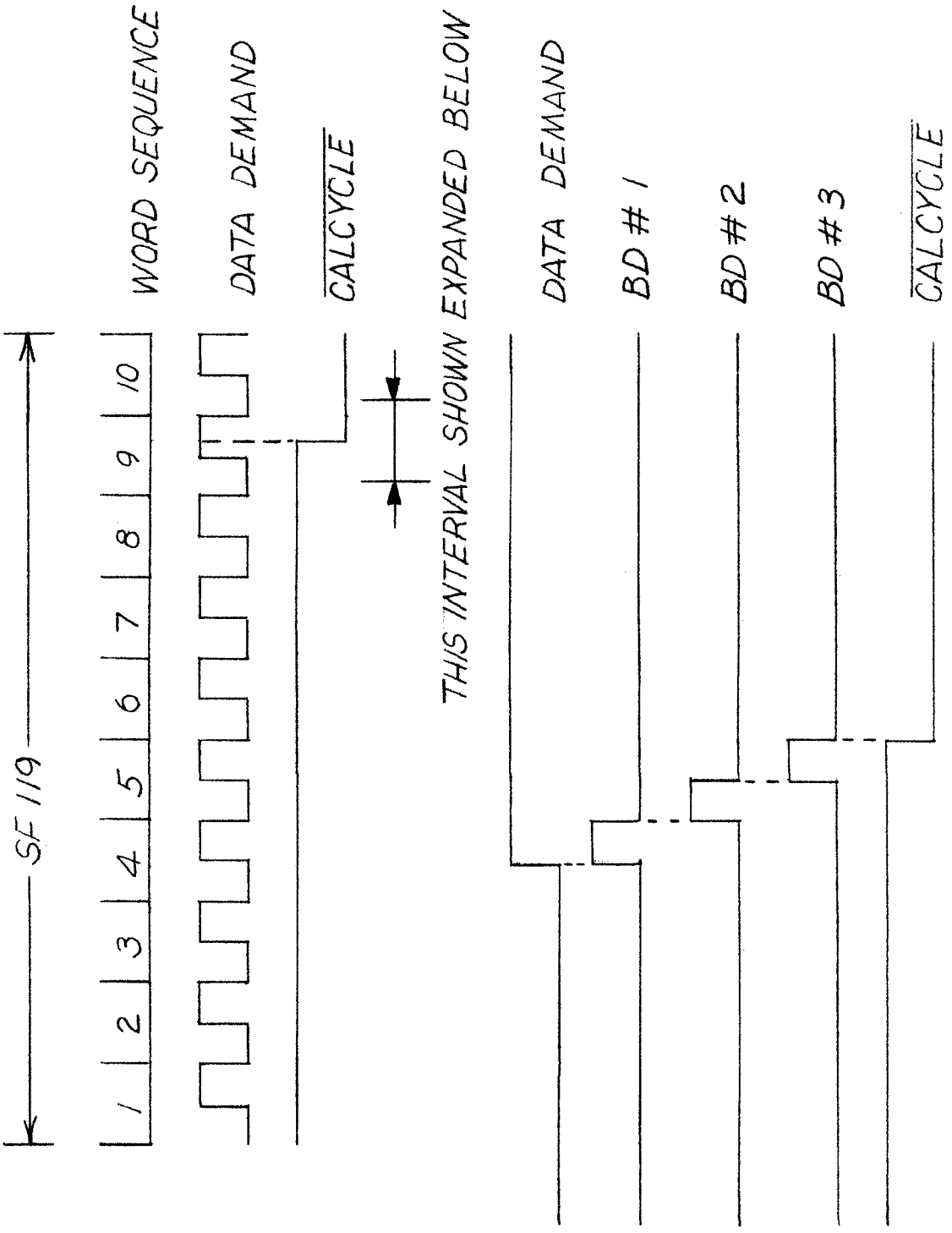


FIG 5.2.7-4 CALCYCLE TIMING

5.2.8 Velocity Filter Step Voltage Generator

A simplified block diagram of the Velocity Filter Step Voltage Generator is shown in Figure 5.2.8-1.

The purpose of the Velocity Filter Step Voltage Generator is to generate a maximum of 120 voltage steps which are applied to the Velocity Filter plates. These 120 voltage steps are sub-divided into six energy ranges of twenty velocity steps each, or of ten velocity steps each, depending upon the reset mode in effect (See Section 5.2.8.1 below).

The potentials generated are shown in Table 5.2.8A. Voltages monitored for analog-to-digital conversion are shown in Table 5.2.8B. Velocity Filter Voltage data is read out during Word 7.

Appendix F shows a worst case error analysis of the Velocity Filter Step Voltage Generator.

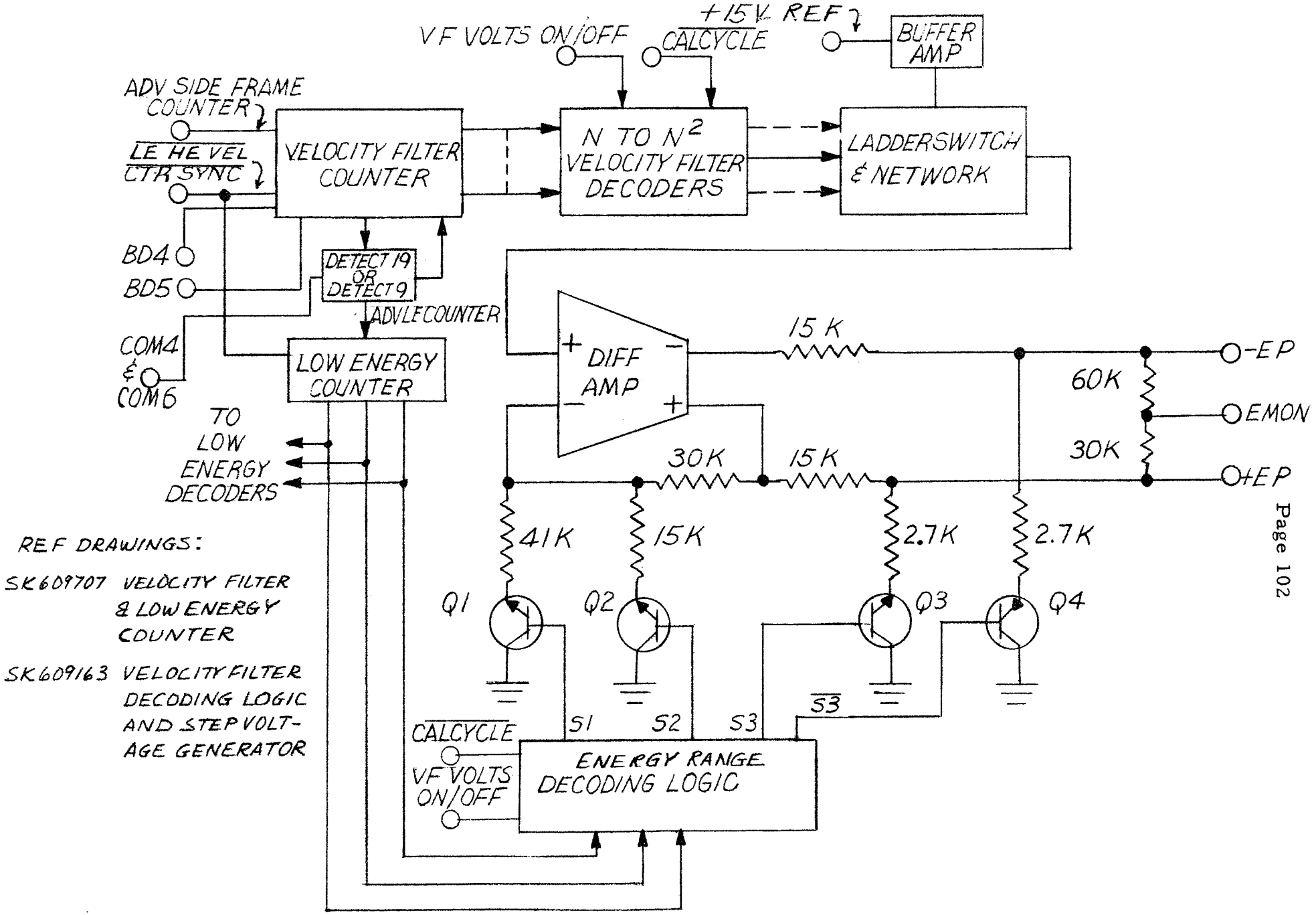
5.2.8.1 Velocity Filter Counter

The Velocity Filter Counter is a five-bit parallel counter, operated either in a divide-by-20 or a divide-by-10 configuration. The Counter provides a binary count necessary to properly address the Ladder Switch and Network.

The counter is stepped once per SIDE Frame (at Word 9) by the Advance SIDE Frame Counter pulse (generated in the Logic Timing Section) to produce a total of twenty velocity steps or (when Command 4 or Command 6 is executed), a total of ten velocity steps.

The Command 4 and Command 6 logic control function is normally at "0" state. During this condition, the Detect-19 circuit is operative. At the twentieth velocity step, an Advance Low Energy Counter pulse is generated by the Detect -19 circuit during Word 9 to advance the Low Energy Counter one step. When Command 4 or Command 6 is executed, the Command 4 and Command 6 logic control function switches to a "1" state. During this condition, the Detect -9 circuit is operative, and the Advance Low Energy Counter pulse is generated during Word 9 at the tenth Velocity step. (See Section 5.2.7.1, Low Energy Counter). Figure 5.2.8-2 shows timing relationships for the Advance SIDE Frame Counter pulse.

After counting through the Twenty Velocity Steps (or, when Command 4 or Command 6 is executed, the first ten Velocity steps), the Velocity Filter Counter is reset by means of the Detect -19 or Detect -9 circuits and associated logic to begin the counting sequence over again.



REF DRAWINGS:

SK609707 VELOCITY FILTER & LOW ENERGY COUNTER

SK609163 VELOCITY FILTER DECODING LOGIC AND STEP VOLTAGE GENERATOR

FIG 5.2.8-1, SIMPLIFIED BLOCK DIAGRAM – VELOCITY FILTER STEP VOLTAGE GENERATOR

Velocity Step	Energy Step 1	Energy Step 2	Energy Step 3	Energy Step 4	Energy Step 5	Energy Step 6
1	28.9505	16.7146	9.6502	5.5715	3.2167	1.8572
2	26.3036	15.1864	8.7679	5.0621	2.9226	1.6874
3	23.7924	13.7366	7.9308	4.5789	2.6436	1.5263
4	21.4170	12.3651	7.1390	4.1217	2.3797	1.3739
5	19.1773	11.0720	6.3924	3.6907	2.1308	1.2302
6	17.0734	9.8753	5.6911	3.2858	1.8970	1.0953
7	14.5672	8.4203	4.8300	2.8068	1.6100	0.9556
8	13.2727	7.6630	4.4200	2.5543	1.4700	0.8514
9	11.5759	6.6834	3.8586	2.2278	1.2862	0.7426
10	10.0149	5.7821	3.3383	1.9274	1.1128	0.6425
11	8.5897	4.9593	2.8632	1.6531	0.9544	0.5510
12	7.3002	4.2148	2.4334	1.4049	0.8111	0.4683
13	6.3513	3.6669	2.1171	1.2223	0.7057	0.4074
14	5.1283	2.9609	1.7094	0.9870	0.5698	0.3290
15	4.2460	2.4515	1.4153	0.8172	0.4718	0.2724
16	3.4995	2.0204	1.1665	0.6735	0.3888	0.2245
17	2.8887	1.6678	0.9629	0.5559	0.3210	0.1853
18	2.4136	1.3935	0.8045	0.4645	0.2682	0.1548
19	2.0742	1.1956	0.6914	0.3992	0.2305	0.1331
20	1.8706	1.0800	0.6235	0.3600	0.2078	0.1200

TABLE 5.2.8A: Velocity Filter Plate Voltages
(Plate-to-Plate)

Velocity Step	Energy Step 1	Energy Step 2	Energy Step 3	Energy Step 4	Energy Step 5	Energy Step 6
1	4.8251	2.7858	1.6084	0.9286	0.5361	0.3095
2	4.3839	2.5311	1.4613	0.8437	0.4871	0.2812
3	3.9654	2.2894	1.3218	0.7632	0.4406	0.2544
4	3.5695	2.0609	1.1898	0.6870	0.3966	0.2290
5	3.1962	1.8453	1.0654	0.6151	0.3551	0.2050
6	2.8456	1.6459	0.9485	0.5476	0.3162	0.1826
7	2.4279	1.4034	0.80600	0.4678	0.26900	0.1593
8	2.2121	1.2772	0.73800	0.4257	0.24500	0.1419
9	1.9293	1.1139	0.6431	0.3713	0.2144	0.1238
10	1.6692	0.9637	0.5564	0.3212	0.1855	0.1071
11	1.4316	0.8266	0.4772	0.2755	0.1591	0.0918
12	1.2167	0.7025	0.4056	0.2342	0.1352	0.0781
13	1.0586	0.6112	0.3529	0.2037	0.1176	0.0679
14	0.8547	0.4935	0.2849	0.1645	0.0950	0.0548
15	0.7077	0.4086	0.2359	0.1362	0.0786	0.0454
16	0.5833	0.3367	0.1944	0.1123	0.0648	0.0374
17	0.4815	0.2780	0.1605	0.0927	0.0535	0.0309
18	0.4023	0.2323	0.1341	0.0774	0.0447	0.0258
19	0.3457	0.1993	0.1152	0.0665	0.0384	0.0222
20	0.3118	0.1800	0.1039	0.0600	0.0346	0.0200

TABLE 5.2.8B: Velocity Filter A/D Monitor Voltages

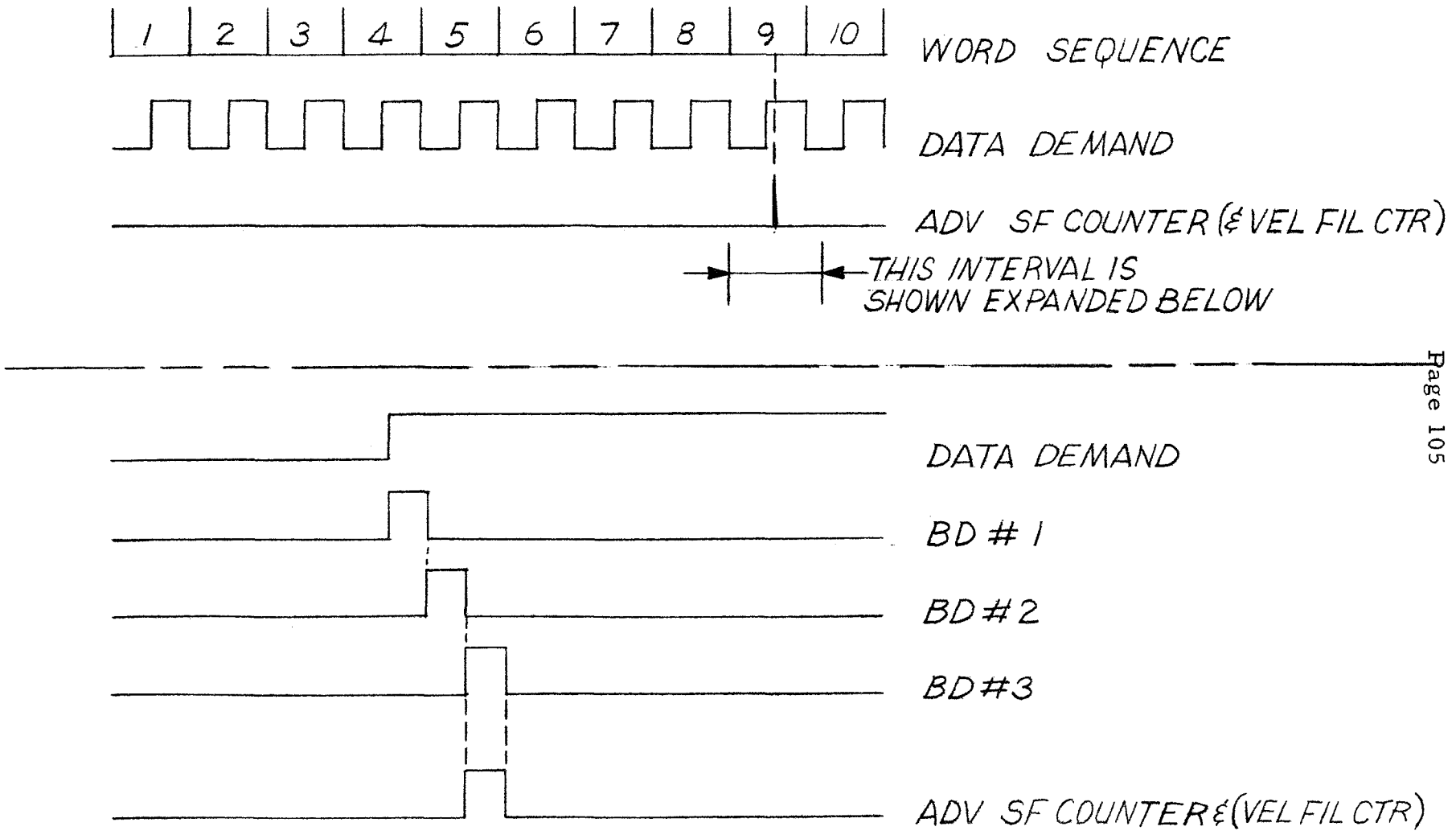


FIG 5.2.8-2 ADVANCE SIDE FRAME CTR TIMING

The Velocity Filter Counter is reset when any of the following conditions exist:

- o The Velocity Filter Counter reaches the twentieth Velocity step (or, when Command 4 or Command 6 is executed, the tenth Velocity step).

  or

- o The SIDE Frame Counter is reset, which is caused by the following by means of the $\overline{\text{LE, HE VEL Ctr Sync}}$ pulse:

  1) SIDE Frame 127 (or 10, 39, or 79, depending upon the ground command in effect is reached.

  2) Power is applied to the system.

  3) A command is executed which resets the SIDE Frame Counter.

Resetting is performed to synchronize the Velocity Filter Counter with the SIDE Frame Counter. See Figure 5.2.8-3 for timing relationships between Power On and the $\overline{\text{LE, HE, VEL Ctr Sync}}$ level.

See Figure 5.2.8-4 for timing of the $\overline{\text{LE, HE, VEL Ctr Sync}}$ pulse. The BD5 pulse is used to reset an element within the Velocity Filter reset networks.

Table 5.2.8C shows the binary output address of the Velocity Filter Counter.

5.2.8.2 Velocity Filter Decoders: Ladder Switch and Network

The output of the Velocity Filter Counter feeds an "N to N^2" Decoder. The Decoder output addresses the Velocity Filter Ladder Switch and Network. The Ladder network furnishes an analog voltage to the amplifier, depending upon the address programming the Ladder network. Table 5.2.8D shows the complements of the decoded states addressing the Ladder network. See Figure 5.2.8-5 for the equivalent circuit of the Ladder Network. Command 9 (VF Volts On/Off) is executed to turn the Velocity Filter voltage OFF, the $\overline{\text{VF Volts On/Off}}$ logic control function switches to a "0" state. This causes the $\overline{\text{"N to N}^2\text{"}}$ decoder to address the Ladder Network to furnish 0 volts to the amplifier. At the same time, the Range Decoding Logic is caused to address the output divider and feedback network of the amplifier as follows:

S1	S2	S3
0	0	1

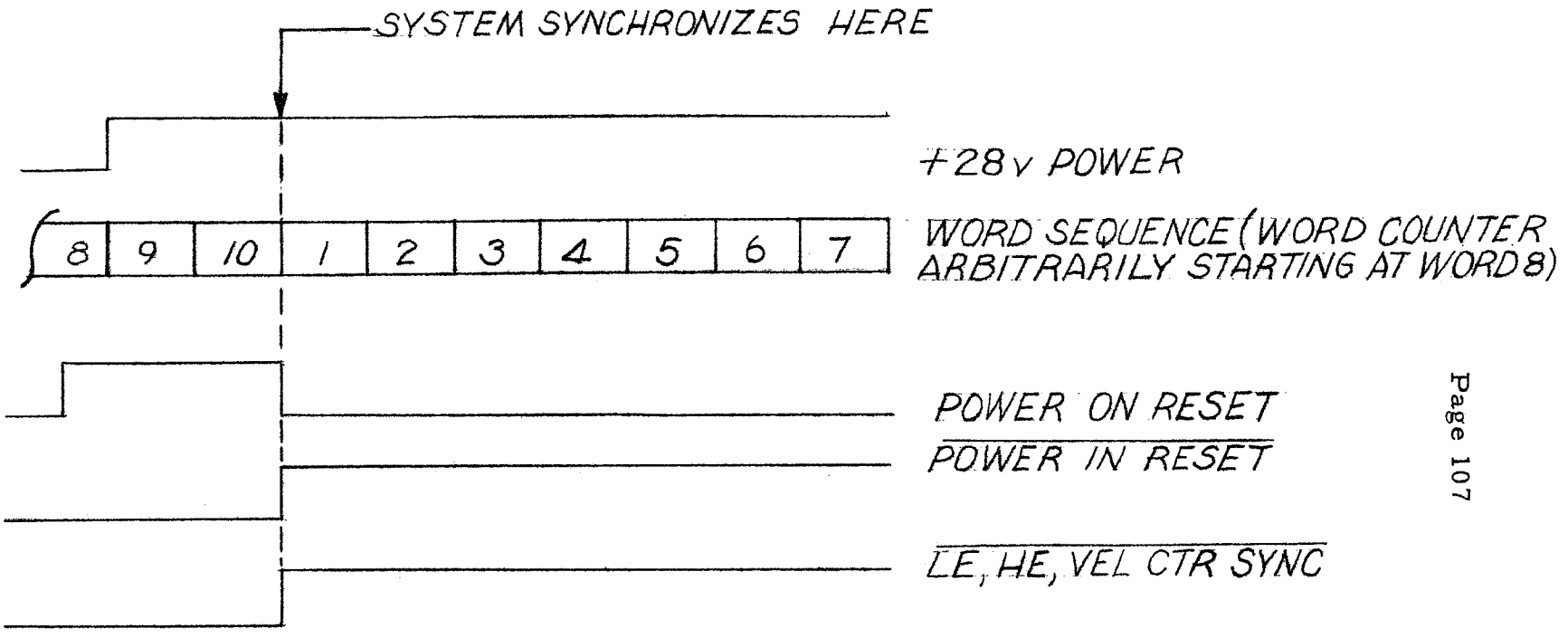


FIG 5.2.8-3 POWER ON AND $\overline{\text{LE HE VEL COUNTER SYNC}}$ TIMING

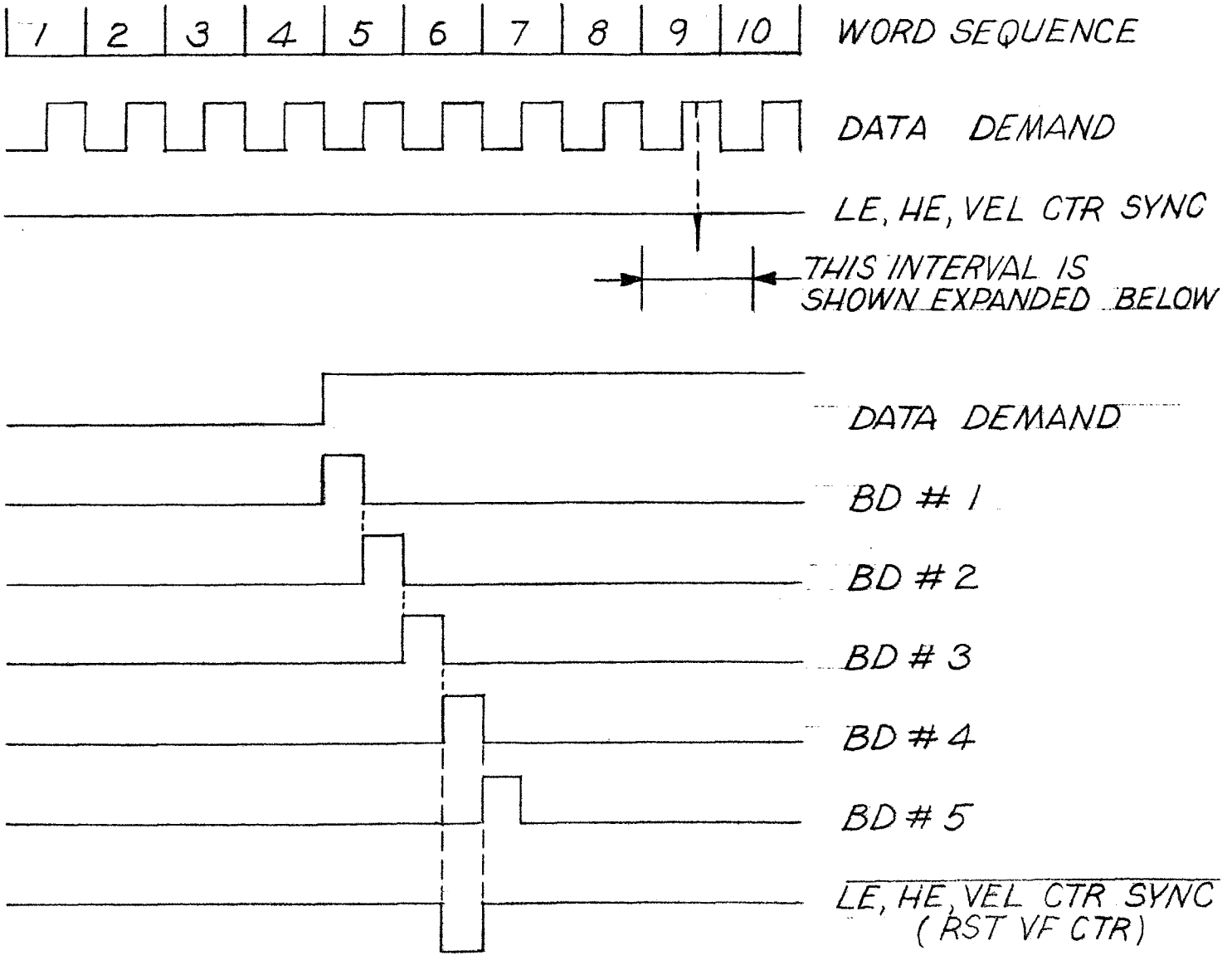


FIG 5.2.8-4 LE HE VEL CTR SYNC TIMING

TABLE 5.2.8C: Velocity Filter Counter Output Address

Velocity Step	Velocity Counter				
	5	4	3	2	1
1	0	0	0	0	0
2	0	0	0	0	1
3	0	0	0	1	0
4	0	0	0	1	1
5	0	0	1	0	0
6	0	0	1	0	1
7	0	0	1	1	0
8	0	0	1	1	1
9	0	1	0	0	0
10	0	1	0	0	1
11	0	1	0	1	0
12	0	1	0	1	1
13	0	1	1	0	0
14	0	1	1	0	1
155	0	1	1	1	0
16	0	1	1	1	1
17	1	0	0	0	0
18	1	0	0	0	1
19	1	0	0	1	0
20	1	0	0	1	1

TABLE 5.2.8D: Velocity Filter Ladder Address (Output of N to N^2 Decoder)

Velocity Step	Decoded States - FN									Decimal F
	256	128	64	32	16	8	4	2	1	
1	1	1	0	0	1	0	0	0	0	400
2	1	0	1	1	0	1	0	0	1	361
3	1	0	1	1	0	0	1	0	0	324
4	1	0	0	1	0	0	0	0	1	289
5	1	0	0	0	0	0	0	0	0	256
6	0	1	1	1	0	0	0	0	1	225
7	0	1	0	1	1	1	1	0	0	188
8	0	1	0	1	0	1	0	0	1	169
9	0	1	0	0	1	0	0	0	0	144
10	0	0	1	1	1	1	0	0	1	121
11	0	0	1	1	0	0	1	0	0	100
12	0	0	1	0	1	0	0	0	1	81
13	0	0	1	0	0	0	0	1	1	67
14	0	0	0	1	1	0	0	0	1	49
15	0	0	0	1	0	0	1	0	0	36
16	0	0	0	0	1	1	0	0	1	25
17	0	0	0	0	1	0	0	0	0	16
18	0	0	0	0	0	1	0	0	1	9
19	0	0	0	0	0	0	1	0	0	4
20	0	0	0	0	0	0	0	0	1	1

NOTE: Logical Outputs are to be in Form of $\overline{F_N}$.

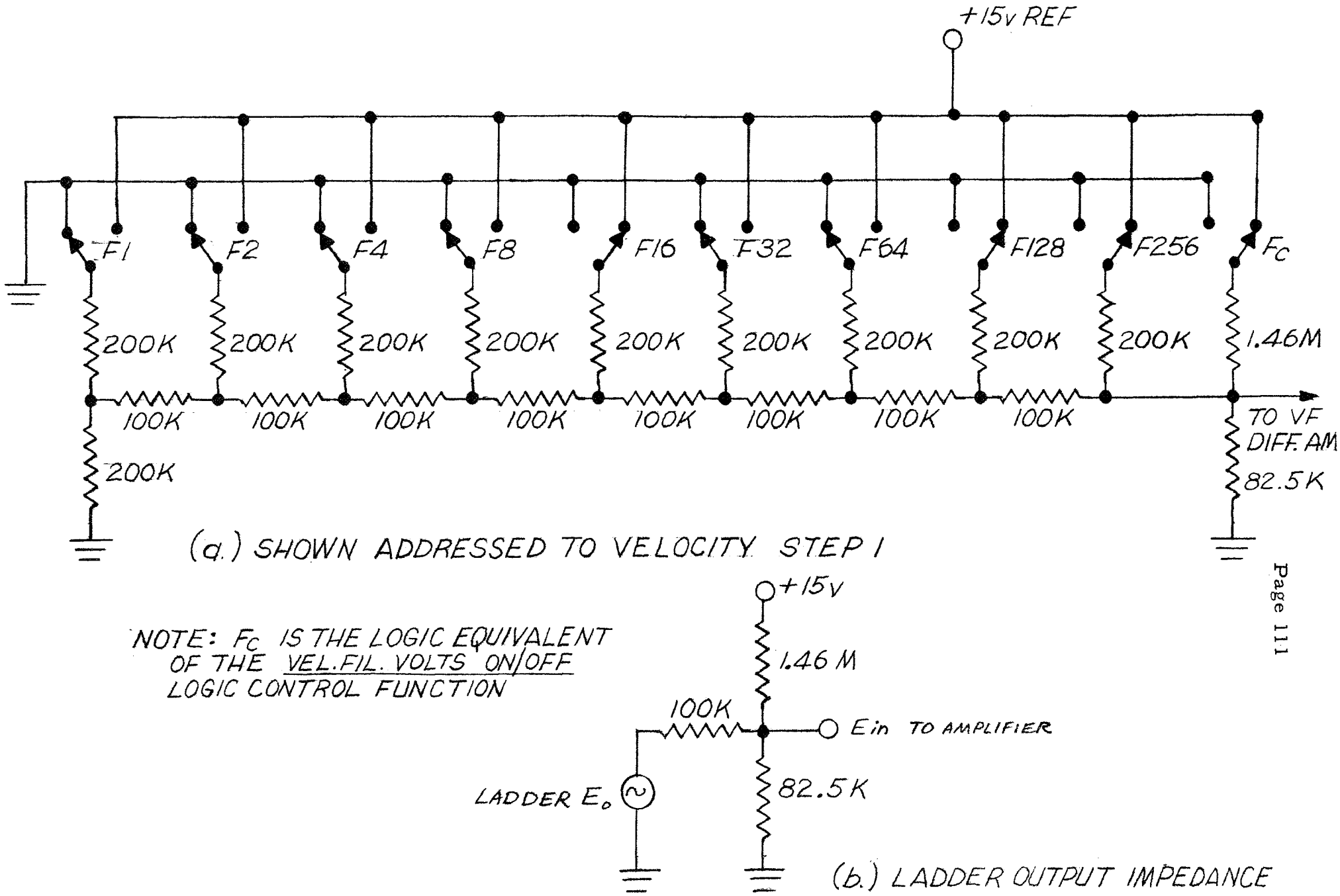


FIG 5.2.8-5, VEL. FIL. LADDER NETWORK EQUIVALENT CIRCUIT

This causes Q1 and Q2 to be cut OFF (refer to Figure 5.2.8-1) and Q3 and Q4 to be ON. Thus, amplifier gain is minimum (unity) and output attenuation is maximum. The Velocity Filter generator is now OFF.

During Calibration Cycle (Side Frame 120-127), the $\overline{\text{Cal Cycle}}$ logic control function switches to a "0" state. The "N to N^2" decoder and the Range Decoding Logic are thus addressed to maintain the Velocity Filter voltage at a level above Velocity step 5 (Energy level 1).

As mentioned previously, the Low Energy Counter is advanced once for each twenty or ten Velocity steps, depending on whether the Detect 19 or Detect - 9 circuit is operative. The Low Energy Counter, in addition to driving the Low Energy Decoder (q.v.) also addresses the Energy Range Decoding Logic. Its output decoded state (see Table 5.2.8E) controls the feedback (and hence the gain) and the output attenuation of the Differential Amplifier.

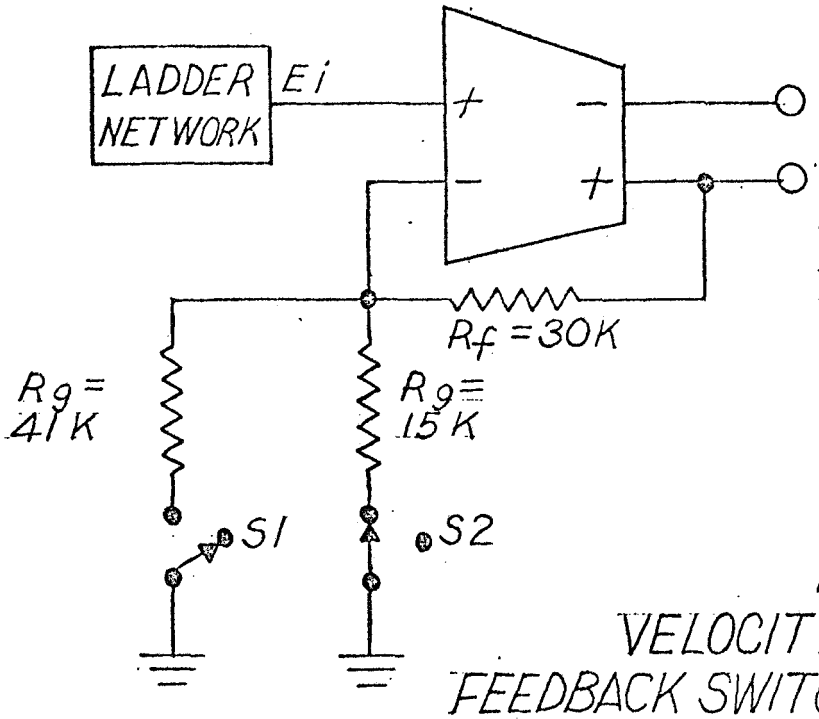
5.2.8.3 Velocity Filter Amplifier

The Velocity Filter Amplifier is a single input, double output balanced differential amplifier. The switching of Q1, Q2, Q3, and Q4 (Simplified Block Diagram, Figure 5.2.8-1 is controlled by the output of the Energy Range Decoding Logic to change feedback impedances (and hence gain) and the output attenuation. Figure 5.2.8-6 shows a simplified schematic of the Velocity Filter Amplifier feedback switching, addressed to Energy step 1.

Since the Range Decoding Logic is addressed by the Low Energy Counter, it is evident that the overall transfer function of the Velocity Filter Amplifier is adjusted each time the Low Energy Counter is advanced. Since the Velocity Filter Counter is reset at the same time the Low Energy Counter is advanced, the Ladder network and the Energy Range Decoding Logic step the amplifier through six energy ranges of twenty (or ten, if Command 4 or Command 6 is executed) Velocity steps each. Table 5.2.8F shows the Ladder network output voltage for each Velcoity step, and Table 5.2.8E shows the amplifier gain and output transfer function for each Energy step. The output divider, consisting of the 60K and 30K resistors (Figure 5.2.8-1) provides a stepped down monitor voltage for analog-to-digital conversion (Table 5.2.8B).

The monitor voltage is given by

$$E_{mon} = \frac{V_{plate\text{-}to\text{-}plate}}{6}$$



$$GAIN = \frac{Eo}{Ei} = \frac{Rf + Rg}{Rg}$$

(WHERE Rg IS THE VALUE SWITCHED TO GROUND, DEPENDING UPON THE STATE OF S1 OR S2)

GAIN = UNITY WHEN S1 = S2 = 0

FIG 5.2.8-6
VELOCITY FILTER AMPLIFIER FEEDBACK SWITCHING (SHOWN SWITCHED TO ENERGY STEP 1, S1 = 0, S2 = 1)

Energy Step	Energy Range Decoding Logic			Amplifier Gain	Output Transfer Function
	S3	S2	S1		
1	0	1	0	3	0.75
2	0	0	1	$\sqrt{3}$	0.75
3	0	0	0	1	0.75
4	1	1	0	3	0.144
5	1	0	1	$\sqrt{3}$	0.144
6	1	0	0	1	0.144
	Attenuator Switching	Feedback Switching			

Table 5.2.8E Energy Range Decoding Logic Output Address; Velocity Filter Amplifier Gain; Output Transfer Function.

TABLE 5.2.8F: Velocity Filter Ladder Output Voltage

Velocity Step	Ladder Output Voltage (Volts)	E_{10} to Amplifier (Volts)
1	11.72	6.47
2	10.57	5.87
3	9.48	5.31
4	8.46	4.78
5	7.50	4.38
6	6.59	3.81
7	5.51	3.25
8	4.94	2.96
9	4.22	2.59
10	3.54	2.24
11	2.93	1.92
12	2.37	1.63
13	1.964	1.421
14	1.435	1.148
15	1.054	0.951
16	0.732	0.784
17	0.468	0.648
18	0.264	0.543
19	0.117	0.467
20	0.029	0.421

The monitored voltages are then fed to the analog-to-digital converters. The commutated voltages are thereby transformed by the A/D Converter into a binary readout proportional to the log of the monitored voltage.

5.3 High Energy Ion Detector

5.3.1 Calibration Pulser: Calibration Rate Counter

The High Energy calibration system employs the same Calibration Pulser and Counter used by the Low Energy calibration system. Separate decoders, however, are used. See Section 5.2.1.

5.3.2 -3.5 kV Power Supply

Section 5.2.2 covers the operation of the -3500 Volt Power Supply, which supplies power to both the Low Energy and High Energy channeltrons.

5.3.3 Channeltron Preamplifier

The High Energy Channeltron Preamplifier is electrically identical to that used in the Low Energy Detection system. See Section 5.2.3.

5.3.4 Dead Time Circuit

The High Energy Dead Time Circuit is electrically identical to that used in the Low Energy Detection system. See Section 5.2.4.

5.3.5 Log Count Rate Meter

The High Energy Log Count Rate Meter is electrically identical to that used in the Low Energy Detection system. See Section 5.2.5.

5.3.6 High Energy Accumulator

The High Energy Accumulator is a twenty-bit counter which accumulates the number of output pulses of the High Energy Descriminator (Dead Time Circuit) during the accumulation interval. The High Energy accumulation interval is the period of time between the beginning of Word 6 and the beginning of the next Word 4's BD1 pulse. See Figure 5.3.6-1 for timing relationships of the accumulation interval and readout.

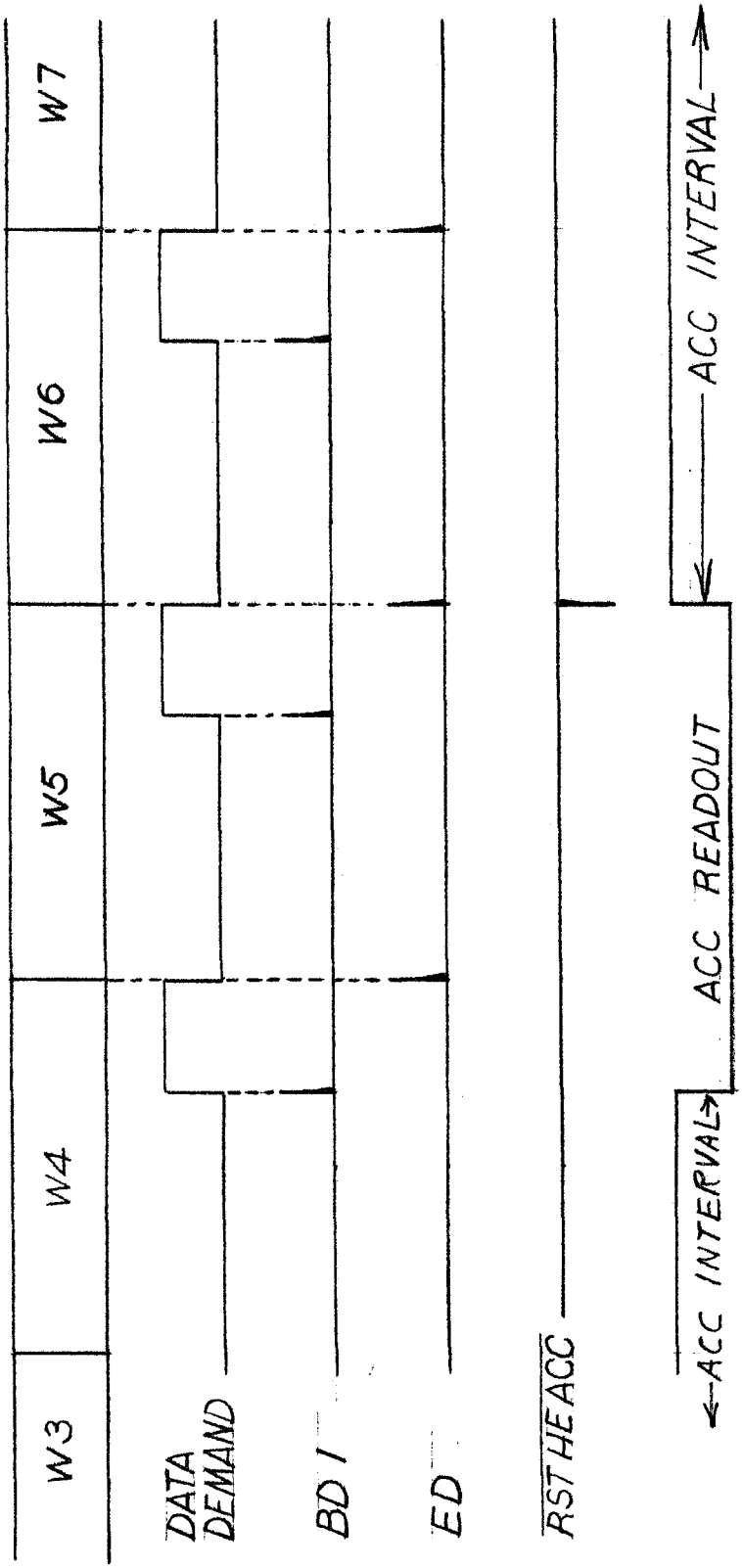


FIG. 5.3.6-1 HIGH ENERGY ACCUMULATOR TIMING RELATIONSHIPS

See Figure 5.2.6-2 for a block diagram of the accumulator.

The accumulator consists of two ten-bit counters with associated logic. The accumulation process is as follows:

The counters initially are cleared when the first Word 6 occurs after application of power. At Word 6, the Logic Timing gates the output pulses of the High Energy Discriminator (Dead Time Circuit) to produce the Advance HE Acc pulses.

The ten-bit counter A (Figure 5.2.6-2) addresses the Detect - 999 circuit. When 999 counts have been detected, a toggle pulse is generated to advance the ten-bit oounter B. At the same time, ten-bit counter A is reset. At this time, for example, the decimal equivalent of the contents of the counters are as follows:

Counter B(Most Significant Digits) Counter A (Least Significant Digits)

0 0 1 0 0 0

or, 001,000

Thus, Counter A represents the least significant digits and Counter B the most significant digits of the total accumulation count.

The Advance HE Accumulator pulse is inhibited by a Detect -999996 circuit in the Logic Timing section to prevent overfill of the counters. The Reset HE Acc pulse is generated to reset the accumulator when either of the two following situations ocuur:

a) When the End Data (ED) pulse and Word 6 are present.

b) X10 Accumulation Interval mode is in effect and the 10th accumulation interval in each SIDE frame is reaehed. See Figure 5.3.6-1, HE Accumulator Timing Relationships, for the exact timing of the Reset HE Acc pulse.

The accumulator also addresses the Strobe Gates, which convert the data to serial form for readout. High Energy Accumulator data is read out in Words 4 and 5 as shown in Figure 5.3.6-1.

5.3.7 High Energy Step Voltage Generator

A simplified block diagram of the High Energy Step Voltage Generator is shown in Figure 5.3.7-1. The purpose of the High Energy Step Voltage Generator is to generate a total of twenty voltage

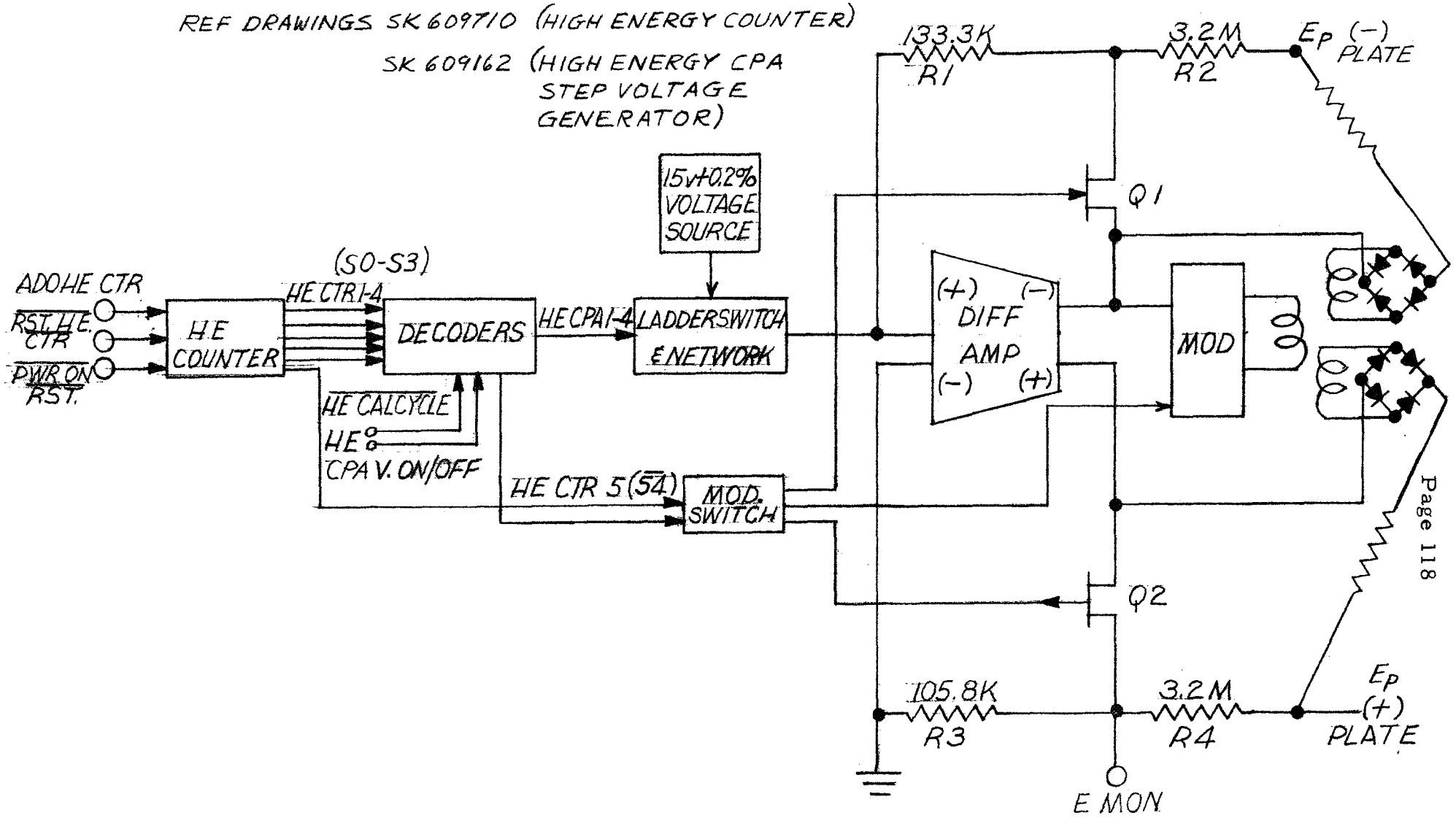


FIG 5.3.7-1, HIGH ENERGY STEP VOLTAGE GENERATOR BLOCK DIAGRAM

steps which are applied to each plate of the High Energy Curved Plate Analyzer. For each voltage step, a positive and negative potential is generated, one for each plate. The potentials generated are shown in Table 5.3.7A. Also shown are the voltages monitored for analog-to-digital conversion. High Energy Voltage data is read out during Word 3. Appendix VI shows a worst-case error analysis of the High Energy Step Voltage Generator.

5.3.7.1 High Energy Counter

The High Energy Counter is a divide-by-twenty parallel five-bit counter, providing a binary count necessary to properly address the Ladder Switch and Network. The counter is advanced once per SIDE Frame (at Word 4) by the Advance High Energy Counter pulse, which is generated by the Logic Timing Section, to produce a total of twenty energy steps.

The output counting sequence of the High Energy Counter is shown in Table 5.3.7B. This is the address to the High Energy Decoders. After counting through the twenty energy steps, the High Energy Counter will recycle to Step 1 to begin the counting sequence over again. The complements of the five bits shown also are available to perform additional logic functions in the system, as described in other sections of this report.

The High Energy Counter will reset to Step 1 whenever the SIDE Frame Counter is reset. This occurs under the following conditions:

- o SIDE Frame 127 (or 10, 39, or 79, depending upon the ground command in effect) is reached.
- o Power is applied to the system.
- o A command is executed which resets the SIDE Frame Counter.

Resetting is performed in order to synchronize the High Energy Counter with the SIDE Frame Counter.

Figure 5.3.7-2 shows timing relationships between Power-On and the Power On Reset logic control function.

Figure 5.3.7-3 shows the timing for the Reset HE Counter logic control function.

Figure 5.3.7-4 shows the timings for the Advance High Energy Counter pulse.

TABLE 5.3.7A: High Energy CPA and A/D Monitor Voltages

Energy Step	Nominal CPA Voltage, Volts *(For Positive & Negative Plate)	Monitor Voltage, Volts
1	437	14
2	406	13
3	375	12
4	344	11
5	312	10
6	281	9
7	250	8
8	219	7
9	187	6
10	156	5
11	125	4
12	93.6	3
13	62.5	2
14	31.2	1
15	12.5	12.5
16	8.75	8.75
17	6.25	6.25
18	3.75	3.75
19	2.50	2.50
20	1.25	1.25

*The nominal plate voltage is with respect to ground, and will carry the sign of the associated plate.

TABLE 5.3.7B: High Energy Counter Output Address

Energy Step	S_0	S_1	S_2	S_3	S_4	Decimal Equivalent
1	0	1	1	1	0	14
2	1	0	1	1	0	13
3	0	0	1	1	0	12
4	1	1	0	1	0	11
5	0	1	0	1	0	10
6	1	0	0	1	0	9
7	0	0	0	1	0	8
8	1	1	1	0	0	7
9	0	1	1	0	0	6
10	1	0	1	0	0	5
11	0	0	1	0	0	4
12	1	1	0	0	0	3
13	0	1	0	0	0	2
14	1	0	0	0	0	1
15	0	1	0	1	1	26
16	1	1	1	0	1	23
17	1	0	1	0	1	21
18	1	1	0	0	1	19
19	0	1	0	0	1	18
20	1	0	0	0	1	17

S_4 = HE CTR 5
S_3 = HE CTR 4
S_2 = HE CTR 3
S_1 = HE CTR 2
S_0 = HE CTR 1

} Ladder Address

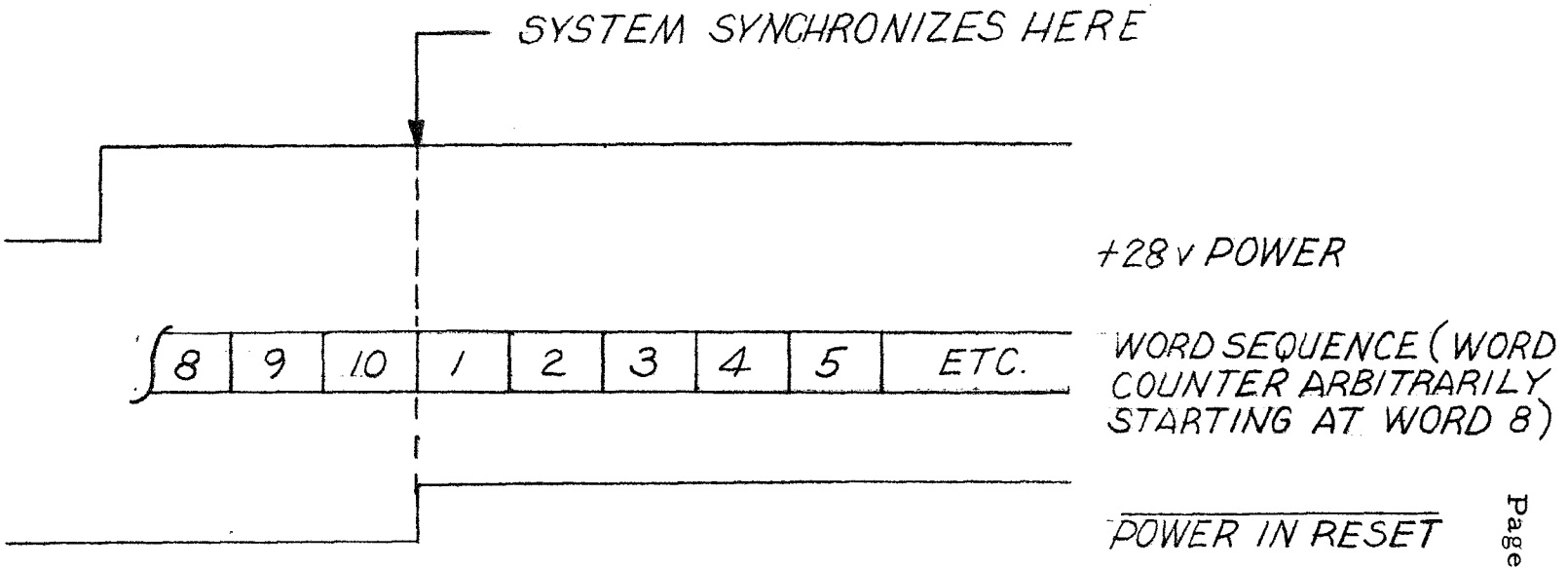


FIG 5.3.7-2 POWER ON AND $\overline{\text{PWRONRST}}$ TIMING

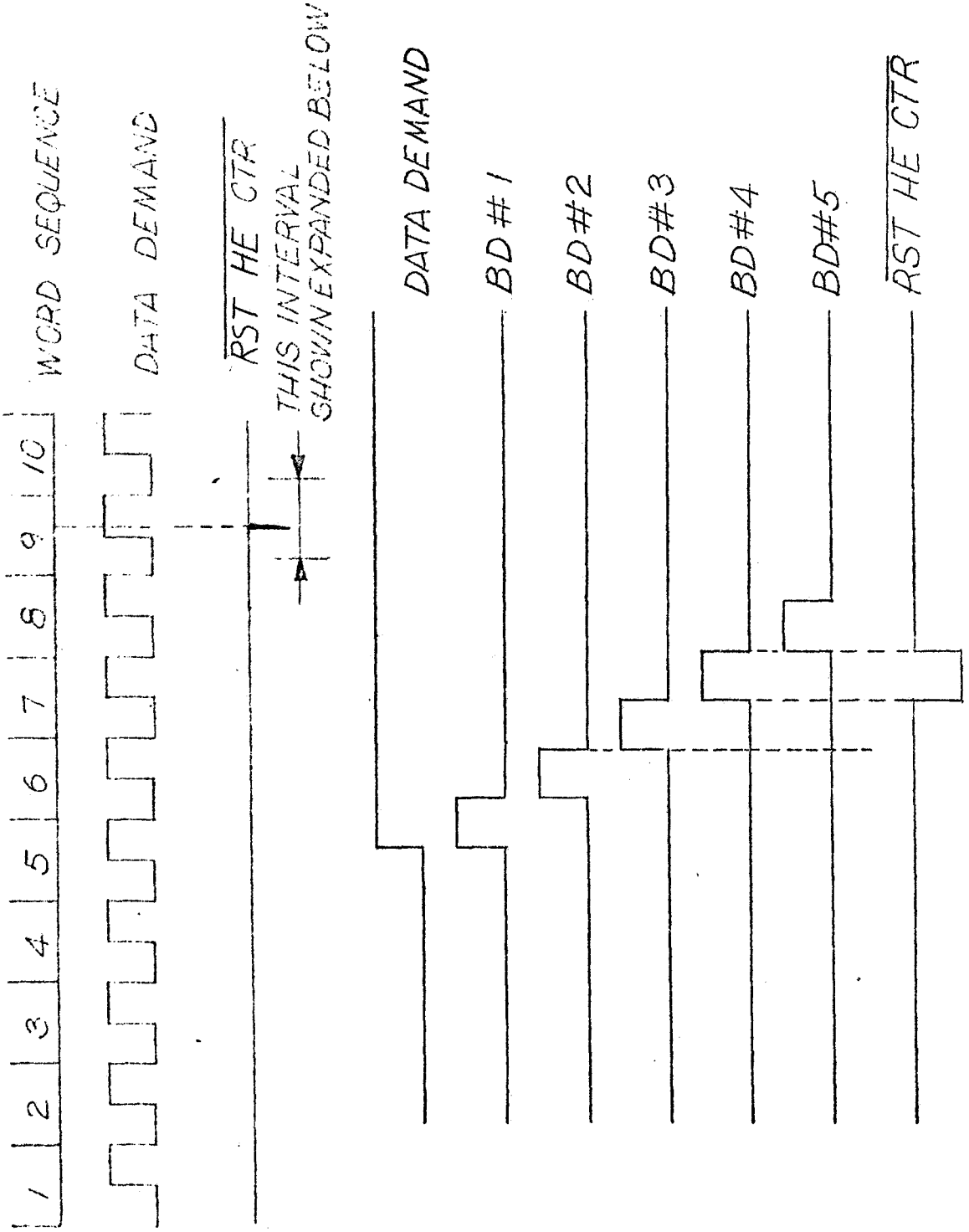


FIG 5.3.7-3 RESET HE CTR TIMING

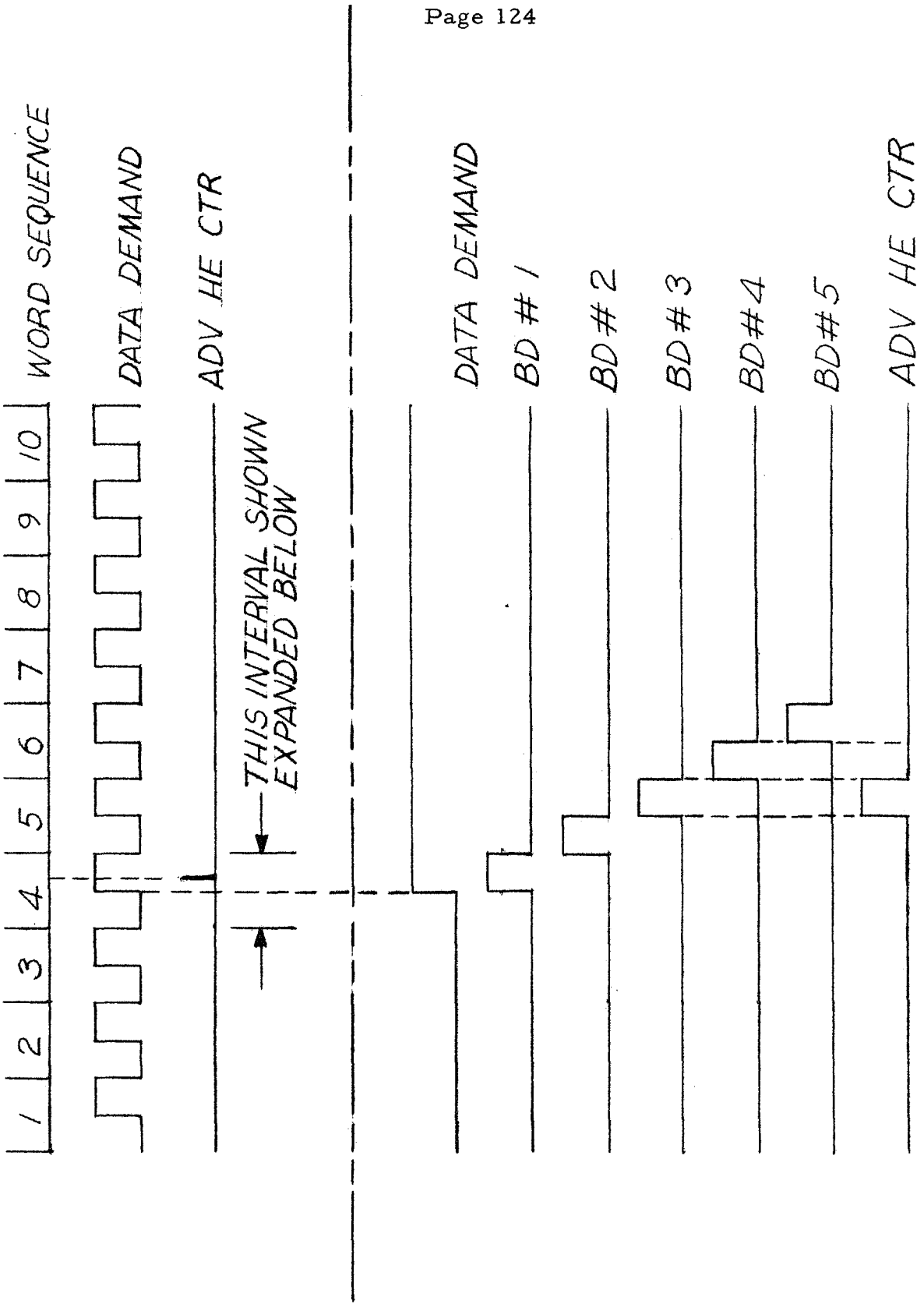


FIG 5.3.7-4 ADVANCE HE COUNTER TIMING

5.3.7.2 High Energy Decoder

The five-bit binary output of the High Energy Counter to be decoded is carried along five lines. The first four bits, the Ladder Address, (S_0, S_1, S_2, and S_3, Table 5.3.7B) are fed to the High Energy Decoders, while the complement of the fifth bit is used to control the switching of the Modulator.

The High Energy Decoder inverts the first four bits (S_0, S_1, S_2 and S_3, Table 5.3.7B) of the counter output, which are then used to drive the Ladder Switch and Network.

The High Energy Decoder can be inhibited upon command when it is desired to turn off the High Energy CPA voltage. When command 11 (High Energy CPA Volts On/Off) is executed, the HE CPA Volts On/Off logic control function switches to a "0" state. This inhibits the High Energy Decoder, drives the Ladder Switch and Network to produce zero output and causes the Modulator Switch to turn the Modulator off.

The High Energy Decoder is inhibited automatically during the system's calibration cycle (SIDE Frames 120 through 127). At this time, the High Energy Cal Cycle logic control function switches to a "0" state. This will inhibit the High Energy Step Voltage Generator as above.

See Figure 5.3.7-5 for the timing of the $\overline{\text{HE Cal Cycle}}$ logic control function.

5.3.7.3 Ladder Switch and Network

Outputs of the Decoder (4 bits) feed the Ladder Switch and Network, which converts the Decoder digital output to an analog voltage. The Ladder Network is referenced by a precision voltage source (+15V ± 0.2%) buffered by the +15V Buffer Amplifier. Figure 5.3.7-6 shows the equivalent circuit for the Ladder Network. The Ladder is shown as addressed to High Energy Step 1.

5.3.7.4 Modulator Switch

The Modulator Switch is controlled by two inputs. One input is the complement of the fifth bit (S4, HE Ctr 5, Table 5.3.7B) of the five-bit binary count generated by the High Energy Counter. During High Energy Steps 15 through 20, bit $\overline{\text{HE Ctr 5}}$ is at "0" state. During High Energy Steps 1 strough 14, this bit is at a "1" state.

The other input to the Modulator Switch is taken from the High Energy Decoder.

HE data is read out at Word 3, therefore the OFF-state of the High Energy Step Voltage Generator will not be seen until SIDE Frame 121.

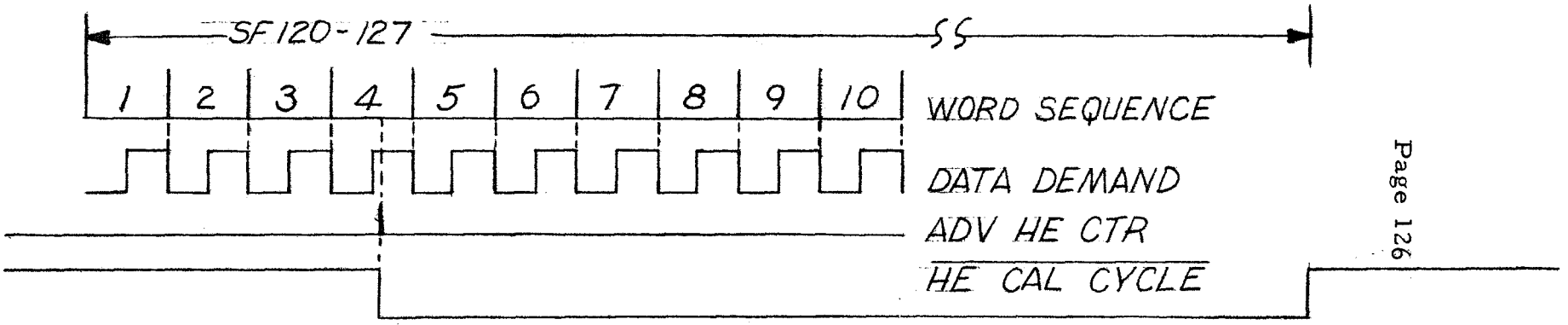
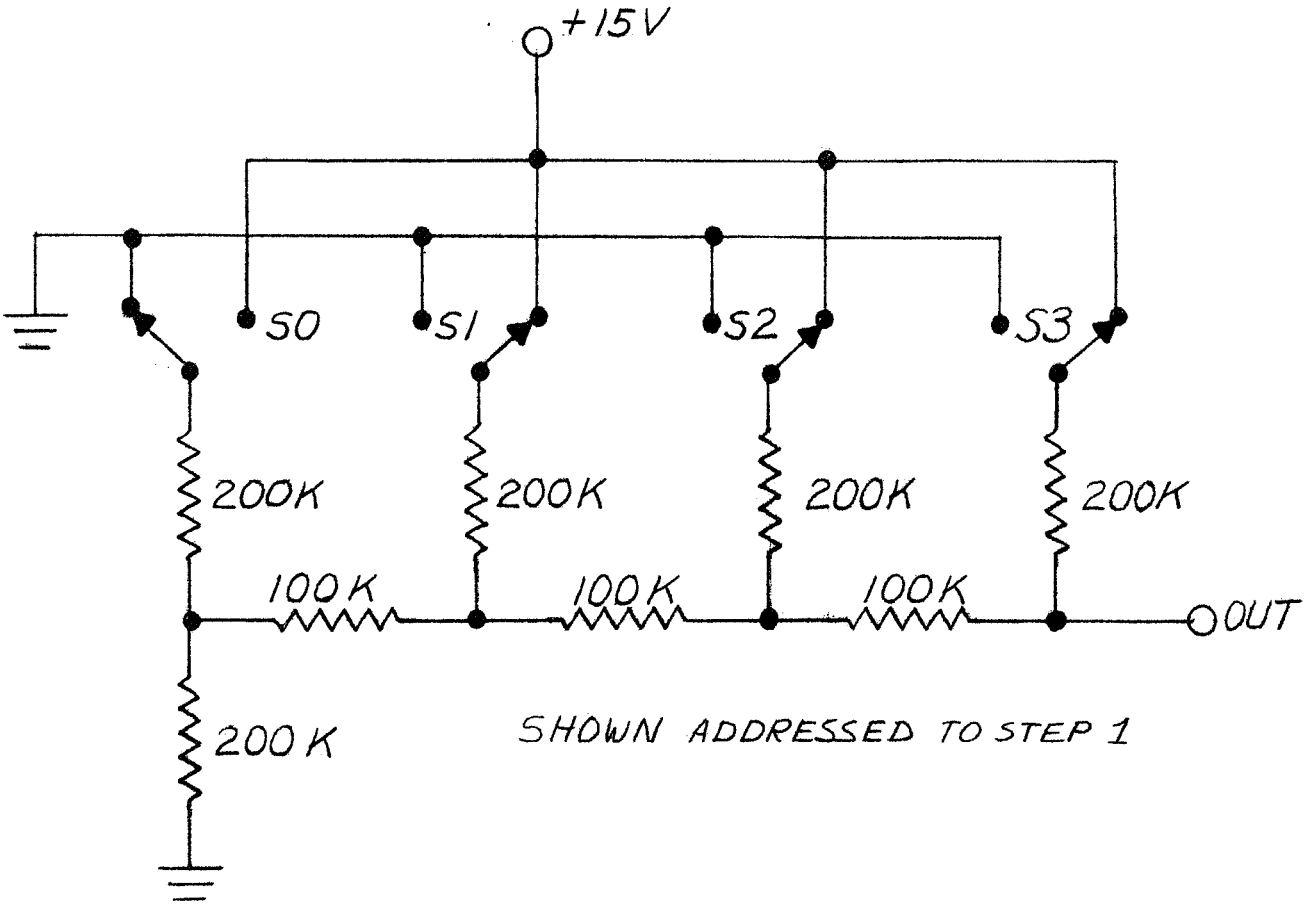
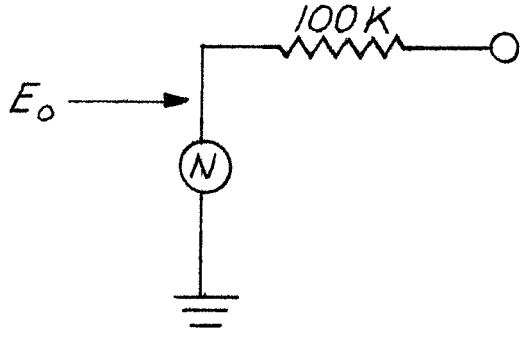


FIG 5.3.7-5 $\overline{\text{HE CAL CYCLE}}$ TIMING



a.) LADDER SWITCH & NETWORK EQUIVALENT CIRCUIT



b) LADDER OUTPUT IMPEDANCE

FIGURE 5.3.7-6 HIGH ENERGY LADDER EQUIVALENT CIRCUITS

Normally, this input will be at a "1" state. When Command 11 (High Energy CPA Volts ON/OFF) is executed, or during SIDE Frames 120 through 127, this input will switch to a "0" state (See Figure 5.3.7-5 for timing during Cal Cycle).

When either of the two inputs to the Modulator Switch is at a "0" state, the Modulator is turned off.

5.3.7.5 High Energy Amplifier

The equivalent circuit of the High Energy Amplifier is shown in Figure 5.3.7-7. Refer also to Figure 5.3.7-1.

The High Energy Amplifier section consists of a single-input balanced-output Differential Amplifier, a chopper-amplifier (modulator), a 1-to-18 step-up transformer, and a pair of bridge rectifiers (one rectifier for each of the two transformer secondaries). The modulator is driven by two ± 5V square waves, 180° out of phase with each other.

During High Energy Steps 1 through 14, the Modulator Switch causes the switching FET's Q1 and Q2 (represented in Figure 5.3.7-7, HE Amplifier Equivalent Circuit, by SW1 and SW2) to be open, and the Modulator section to be operating. E1 and E2, in Figure 5.3.7-7 represent each transformer secondary and its associated rectifier.

Gain is then given as that of a standard inverting differential amplifier:

$$\text{Gain} = \frac{E_o}{E_i} = \frac{R_1 + R_2}{R_o}$$

$$= \frac{3.33 \text{ M ohm}}{0.1 \text{ M ohm}}$$

Where R_o = output impedance of the Ladder Switch and Network = 100 K

$$\text{Gain} = 33.3$$

During High Energy Steps 15 through 20, the switching FET's are closed and the Modulator is turned off. Amplifier gain is then given by:

$$\text{Gain} = \frac{R_1}{R_o}$$

$$= \frac{133\text{K ohm}}{100\text{K ohm}}$$

$$\text{Gain} = 1.33$$

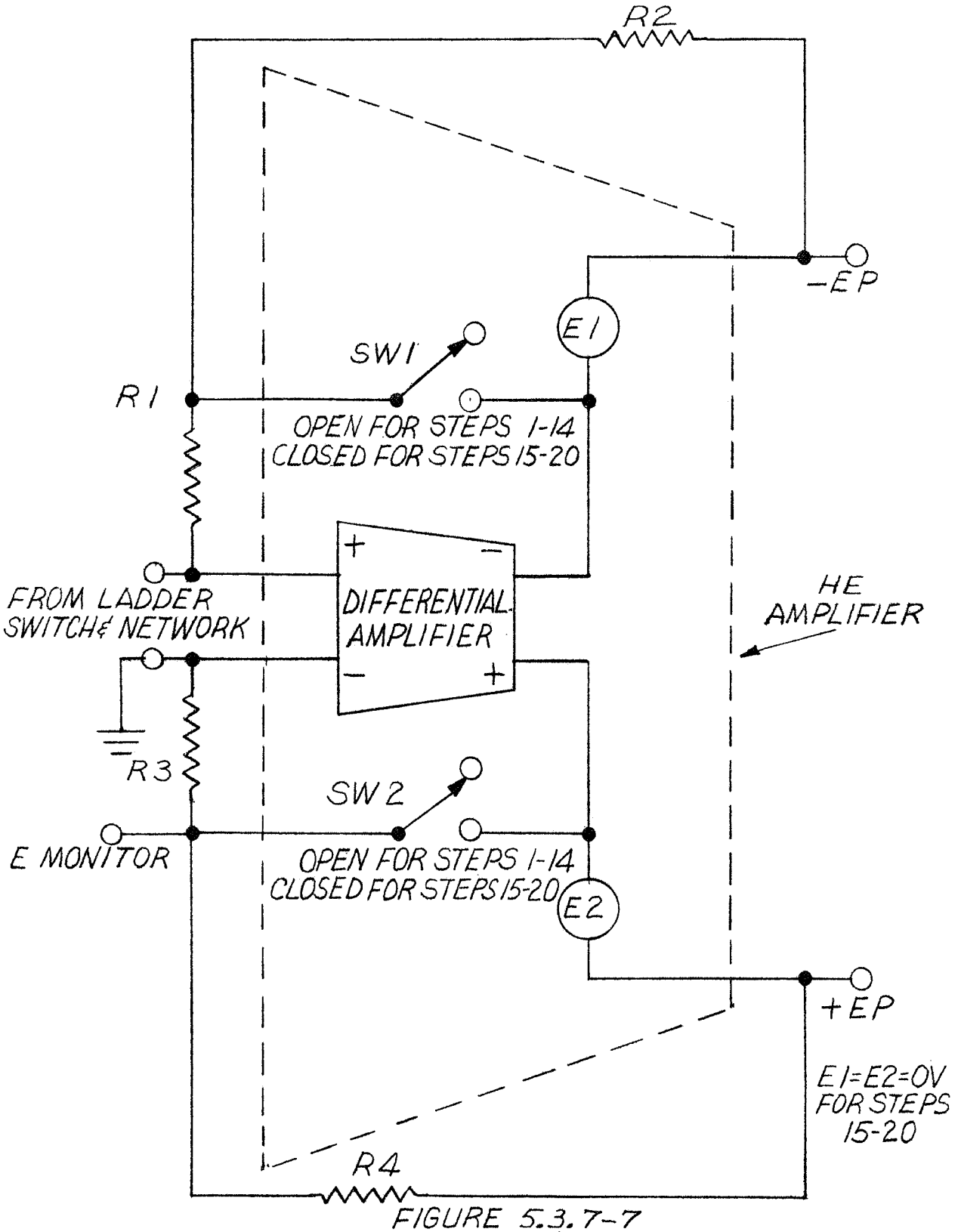


FIGURE 5.3.7-7
HIGH ENERGY AMPLIFIER EQUIVALENT CIRCUIT

Table 5.3.7C shows the Ladder output voltage, amplifier gain, and nominal plate voltage for each energy step.

Voltages monitored for analog-to-digital conversion are taken from the divider formed by R4 and R3 (Figure 5.3.7-1).

For the high steps, 1-14, monitor voltage is given by

$$E_{mon} = \frac{+E_p R_3}{R_3 + R_4}$$

For the low steps, 15-20, monitor voltage is given by

$$E_{mon} = +E_p$$

Table 5.3.7A shows the monitor voltages for each High Energy voltage step

The monitored voltages are then fed to the analog-to-digital converters (q.v.). The commutated voltages are thereby transformed by the A/D Converter into a binary readout proportional to the log of the monitored voltage.

5.4 Cold Cathode Gauge Experiment

5.4.1 Electrometer

An Auto-Ranging, Auto Zero Electrometer monitors current outputs from the sensor or the Calibration Current Generators in the 10^{-13} ampere to 10^{-6} ampere range. Its output ranges from -15 millivolts to +15 volts. Output of the Electrometer is fed to the A/D converters for analog-to-digital conversion and is read out according to the format in Figure 3.0-3, A/D and Status Sub-Com Sequence.

See Figure 5.4.1-1 for a simplified block diagram of the Electrometer. The Electrometer consists of a high-gain, low leakage differential amplifier with switched high impedance feed-back resistors and auto-zero network.

TABLE 5.3.7C: High Energy, Ladder Output, Amplifier Gain, and Nominal Plate Voltages

Energy Step No.	Ladder Adder Output Voltage	Amp Gain	*Nominal Plate Voltage
1	13.12V	33.3	437V
2	12.18V	33.3	406V
3	11.25V	33.3	375V
4	10.32V	33.3	344V
5	9.38V	33.3	312V
6	8.43V	33.3	281V
7	7.50V	33.3	250V
8	6.57V	33.3	219V
9	5.62V	33.3	187V
10	4.68V	33.3	156V
11	3.75V	33.3	125V
12	2.81V	33.3	93.6V
13	1.87V	33.3	62.5V
14	0.938V	33.3	31.2V
15	9.38V	1.33	12.5V
16	6.57V	1.33	8.75V
17	4.68V	1.33	6.25V
18	2.81V	1.33	3.75V
19	1.87V	1.33	2.50V
20	0.938V	1.33	1.25V

*With respect to ground, carries the sign of the associated plate.

(REF DRAWING 609546, CCGE ELECTROMETER SYSTEM)

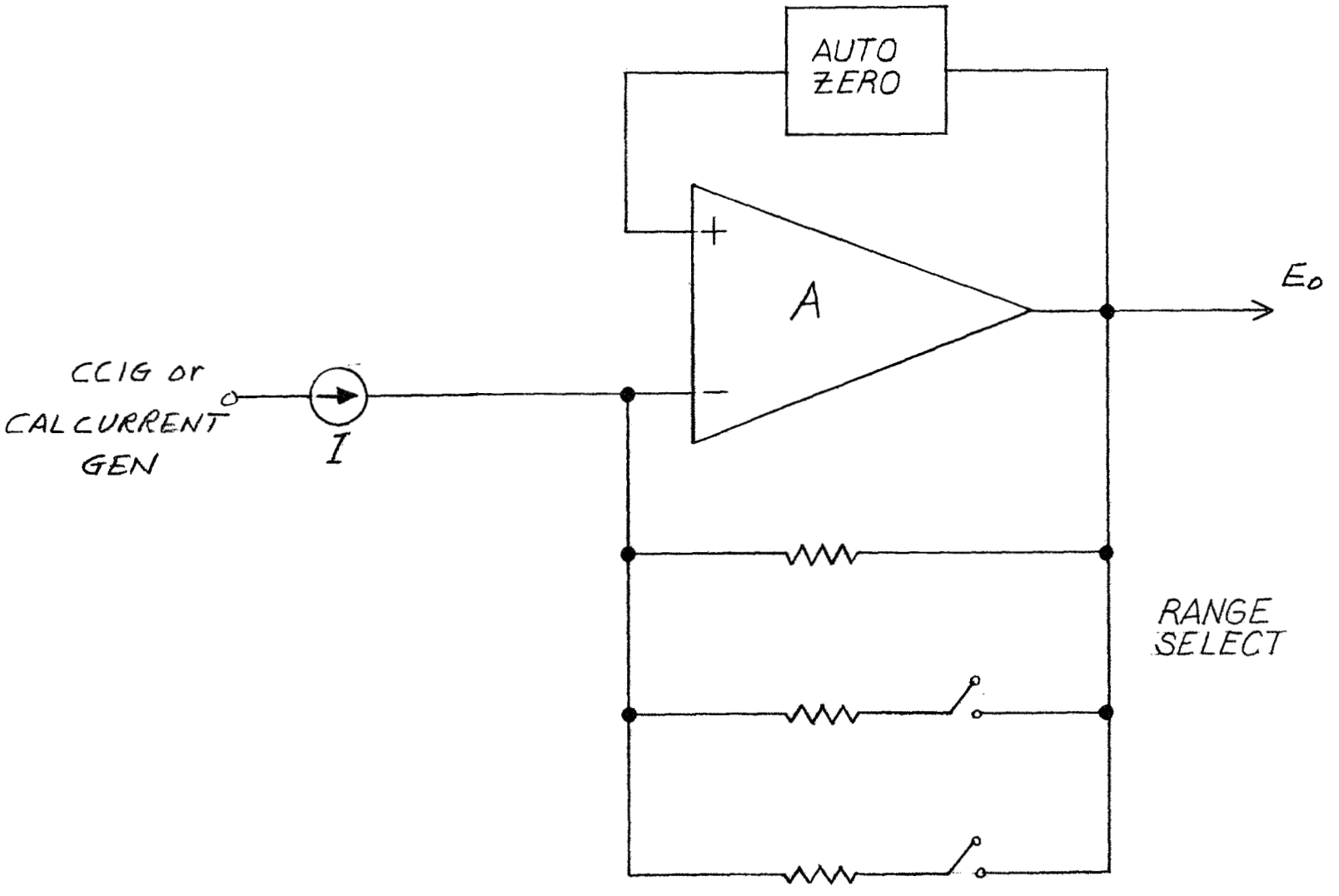


FIG. 5.4.1 -1 ELECTROMETER SIMPLIFIED BLOCK DIAGRAM

The output voltage and input current are related by the following expression:

$$E_o = R_f (I + I_L)$$

Where E_o = Output of Electrometer

I = Input Current

I_L = Leakage Current

R_F = Feedback Resistance

When input current is zero, output voltage should be zero; however, due to leakage and other factors such as temperature variations, output voltage becomes $R_F (I_L)$. This voltage is the Electrometer offset voltage and is cancelled by introducing an error signal (Auto Zero network) that is equal but opposite to the offset voltage into the amplifier. Zero adjustments are thus performed to compensate for error factors.

The electrometer operates in three automatically selected overlapping ranges:

Range 1 (Most Sensitive)
Range 2 (Mid-Range)
Range 3 (Least-Sensitive)

Range 1 senses currents from approximately 10^{-13} to 9.3×10^{-11} amps.

Range 2 senses currents from approximately 3.3×10^{-12} to 3.2×10^{-9} amps.

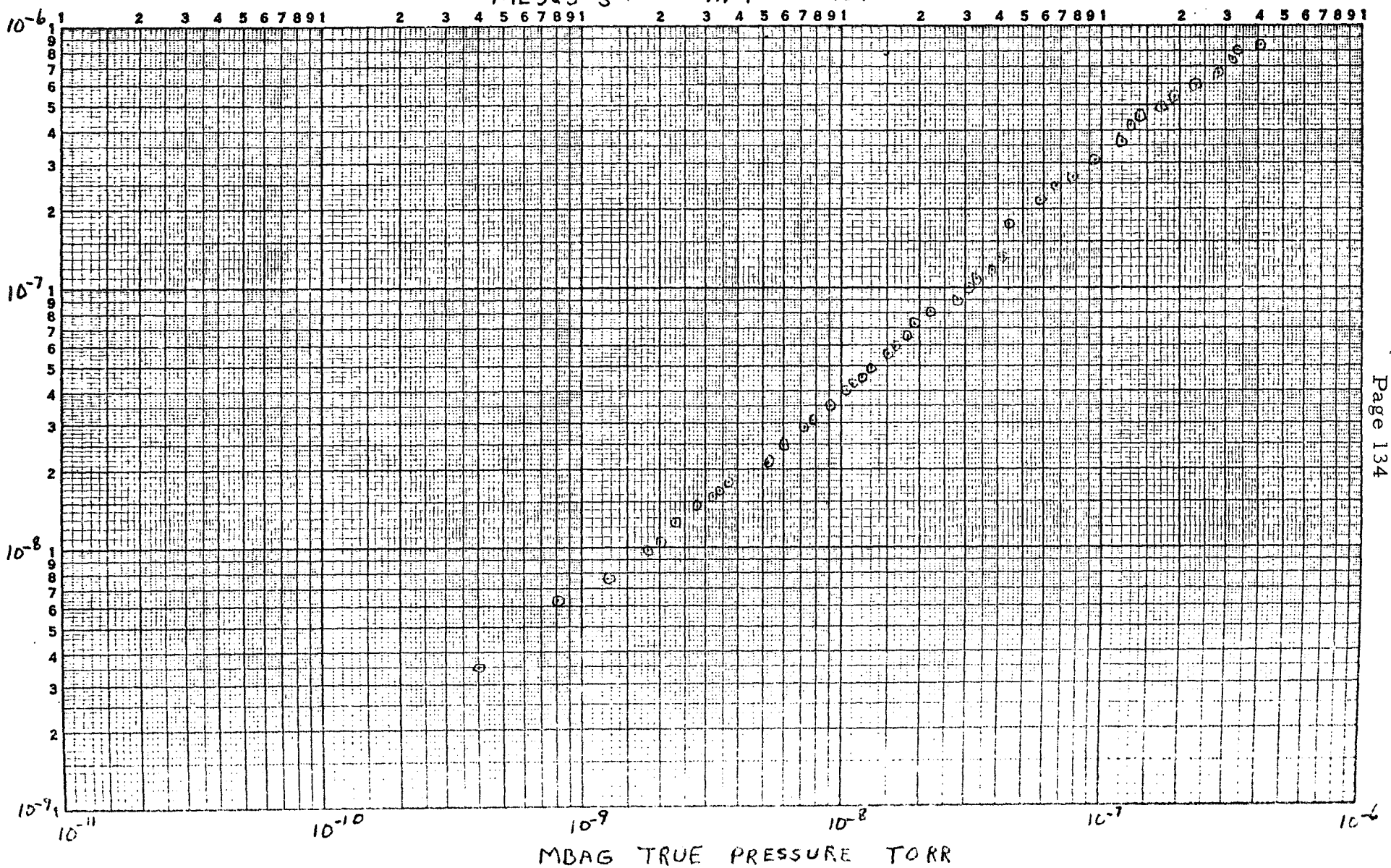
Range 3 senses currents from approximately 10^{-9} to 9.3×10^{-7} amps.

Figure 5.4.1-2 shows a typical plot of pressure vs. CCIG current in the range of 10^{-6} torr to 10^{-11} torr and 10^{-6} amperes to 10^{-9} amperes. Figure 5.4.1-3 shows the Electrometer transfer function, A/D readout counts vs. input current (theoretical curves and measured curves), for a typical system.

See Figure 5.4.1-4 for a simplified block diagram of the Electrometer Range, Auto Zero, and Calibrate switching. Automatic Range switching is accomplished by the switching of two feedback resistors across a permanent feedback

800 BLIVET 6-12-68

ML323-5 S/N 4 SYS7



PUMP PRESSURE CURRENT
CHART MODEL 921-0013
CCIG SN 13 QUAL SPARE

FIG 5.4.1-2 PRESSURE VS CCIG CURRENT

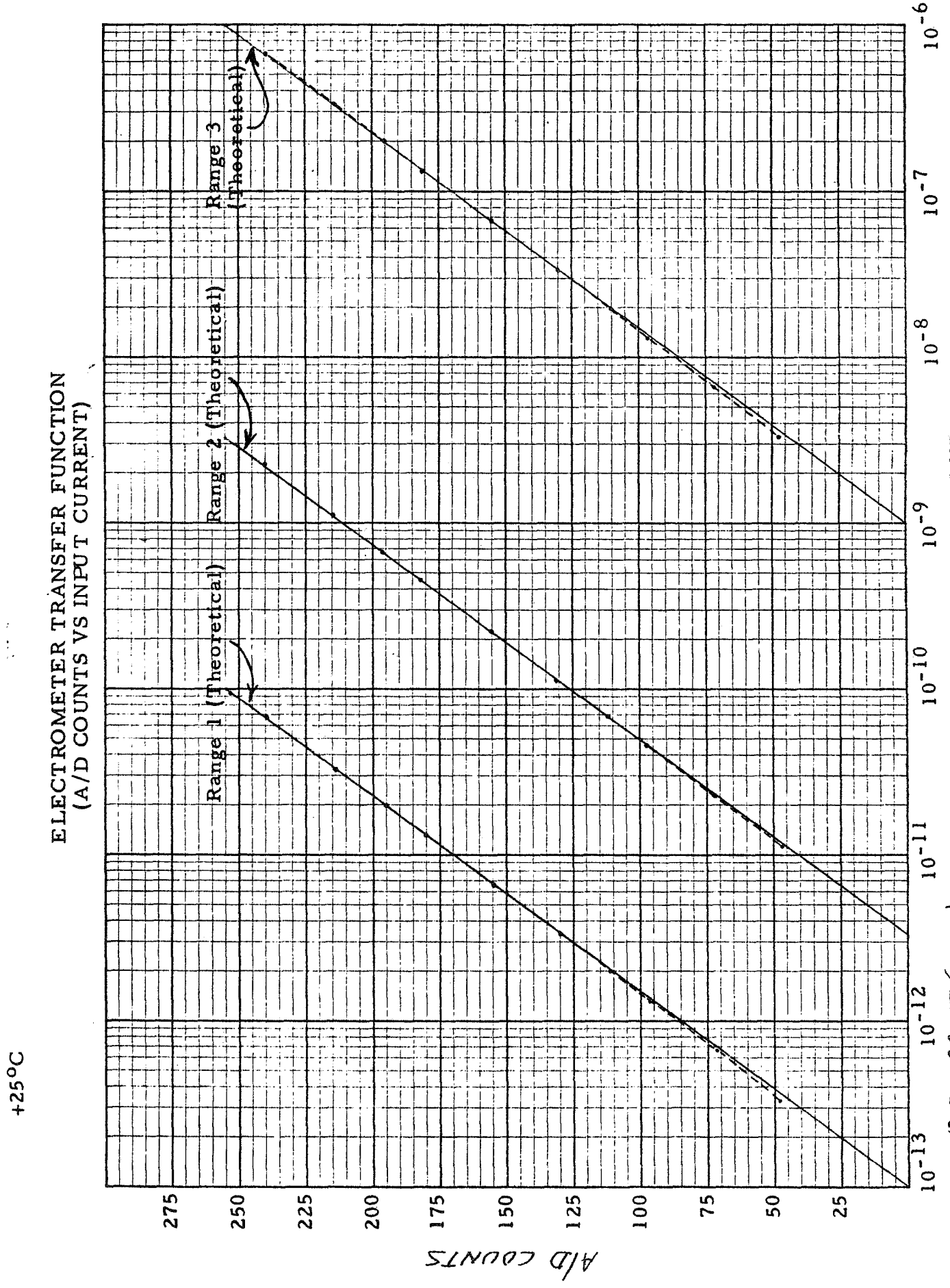


FIG 5.4.1-3 ELECTROMETER TRANSFER FUNCTION

resistor. Auto-zeroing is accomplished by switching in the Drift Correction amplifier in the feedback network. Calibration is effected by switching in one of three calibration current generators.

Figure 5.4.1-5 (a) shows a simplified block diagram of the range comparators. Figure 5.4.1-5(b) shows the comparator logic. The state of the outputs of the two comparators is shown for each corresponding Electrometer output level. The feedback resistors and the calibrate current generators' limiting resistors are switched in automatically to cause the output of the Electrometer to be at midrange (15 mV to 15V). Figure 5.4.1-6 shows the Electrometer comparator decoding network. States of the relay drive logic are shown for each range.

Figure 5.4.1-7 shows a typical relay-driver configuration.

Automatic ranging is accomplished as follows:

The Electrometer output is divided down and compared against a -15 mV reference and a -2.95V reference by means of the two comparators. Output of the comparators feed the comparator decoding logic (Figures 5.4.1-5(b) and 5.4.1-6). Output of the decoding logic is gated to drive the relays which will insert the proper feedback resistors to cause the output of the Electrometer to be in the range of -15 mV to -15V. At the same time, the proper current generator will be switched in to complete the requirement that the output of the Electrometer be between -15 mV and -15V should the instrument be in Calibrate mode. The decoding logic specifies that if the input current to the Electrometer is too small, relays will close or open to adjust feedback to drive the Electrometer to the next more sensitive range. If the input current is too large, relays will close or open to adjust feedback to drive the Electrometer to the next less sensitive range. In both cases, this process will continue until the Electrometer output is mid-range and the comparator outputs are both at a "1" level (see Figure 5.4.1-5(b).

During Cal Mode, output from the CCIG sensor will be automatically disconnected from the Electrometer input and connected to ground through a 10 kΩ resistor.

Refer to Figure 5.4.1-7 for timing diagrams of the Electrometer switching. Timing for Auto-Zero, CCIG switching, and current calibration is shown. Since switching of the Auto-range feedback network and the individual current generators is a function of range, typical timing only is shown for switching of an individual current generator.

(REF DRAWING 609546, CCGE ELECTROMETER SYSTEM)

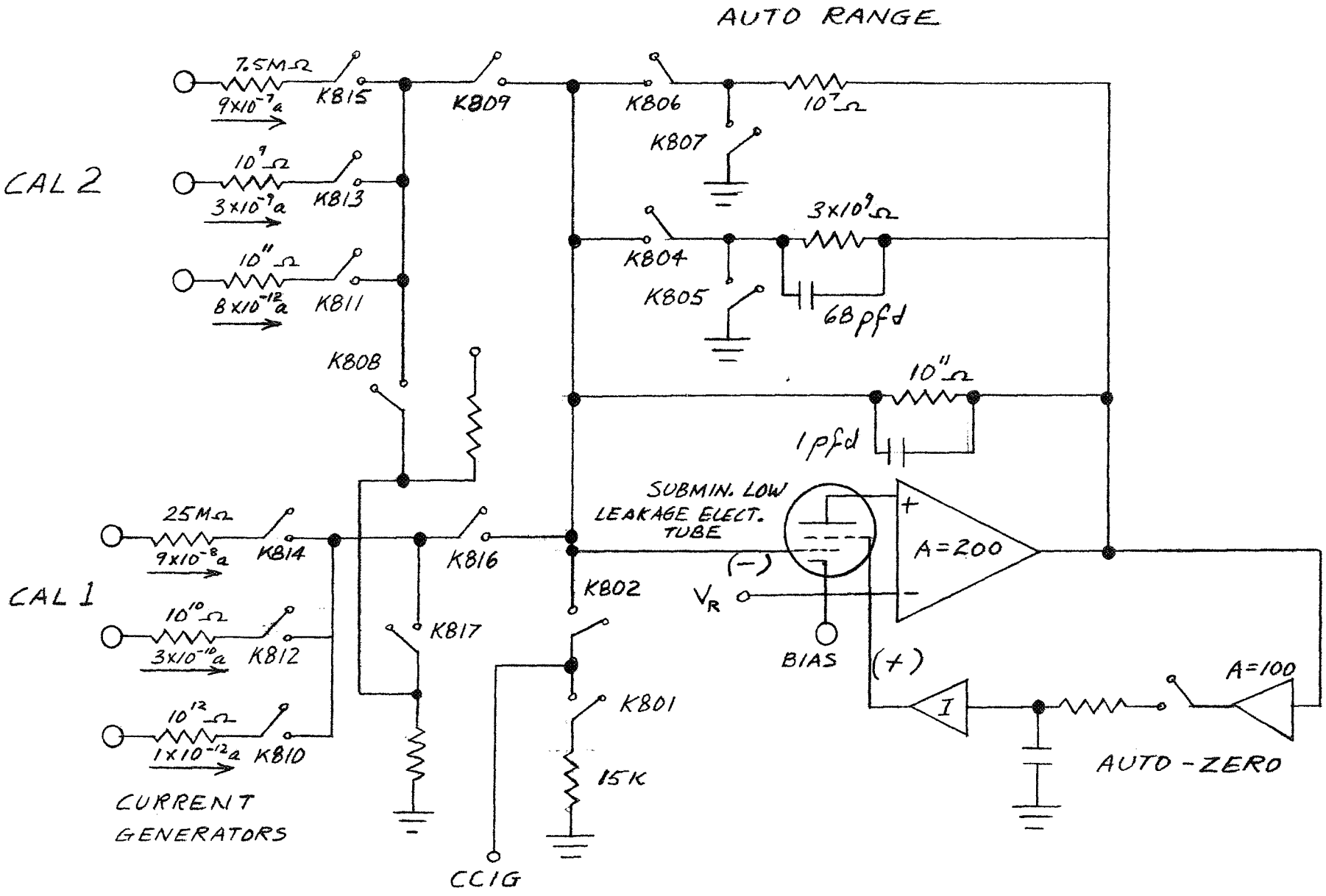
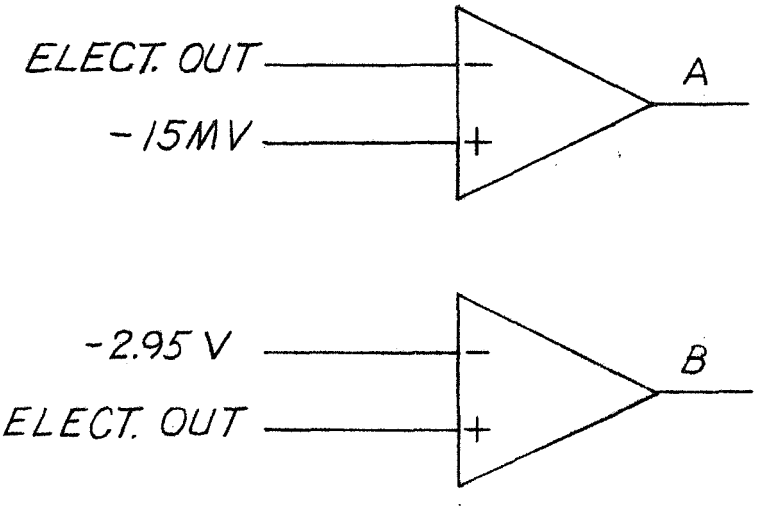


FIG 5.4.1-4 ELECTROMETER RANGE, AUTO ZERO, and CALIBRATE SWITCHING



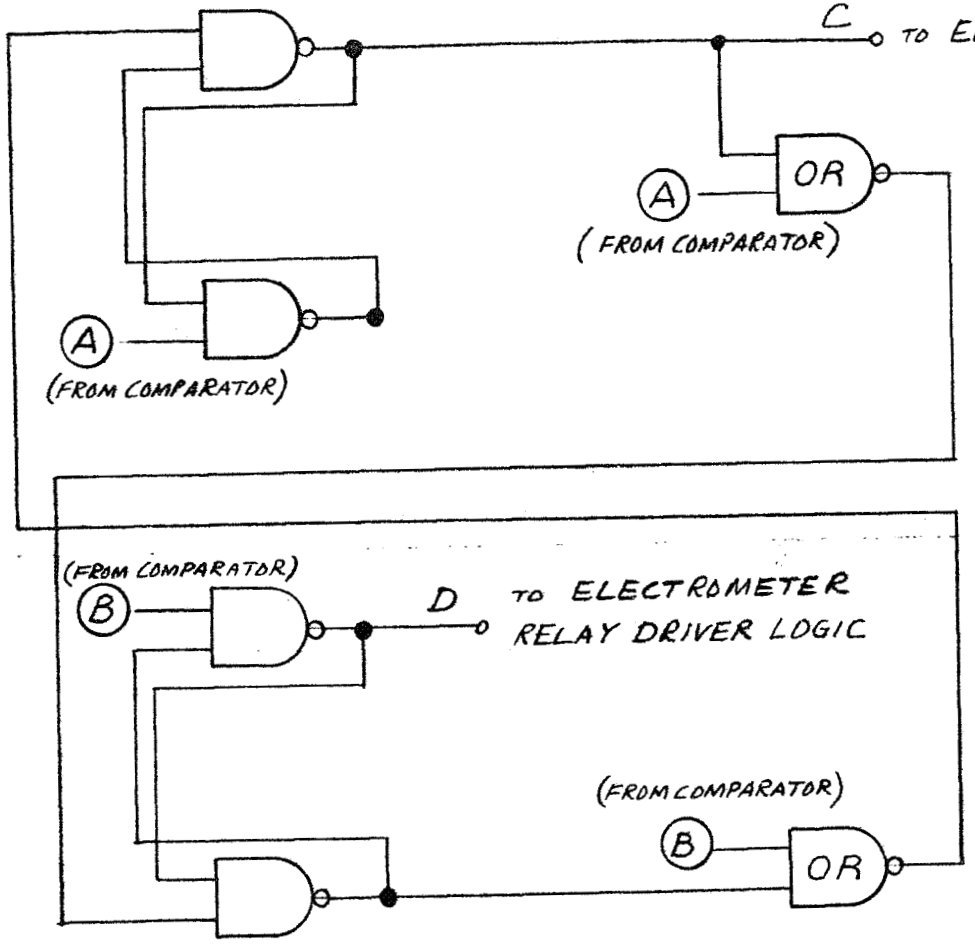
(a) COMPARATORS

COMPARATOR OUTPUTS		ELECTROMETER OUTPUT (MILLIVOLTS)
A	A	0
0	1	≈15
1	1	
1	0	≈15,000

(b) LOGIC

FIG 5.4.1-5, SIMPLIFIED ELECTROMETER RANGE LOGIC

(REF 609546, CCGE ELECTROMETER SYSTEM)



	C	D
RANGE 1	0	0
RANGE 2	0	1
RANGE 3	1	0

FIG 5.4.1-6 ELECTROMETER COMPARATOR DECODING

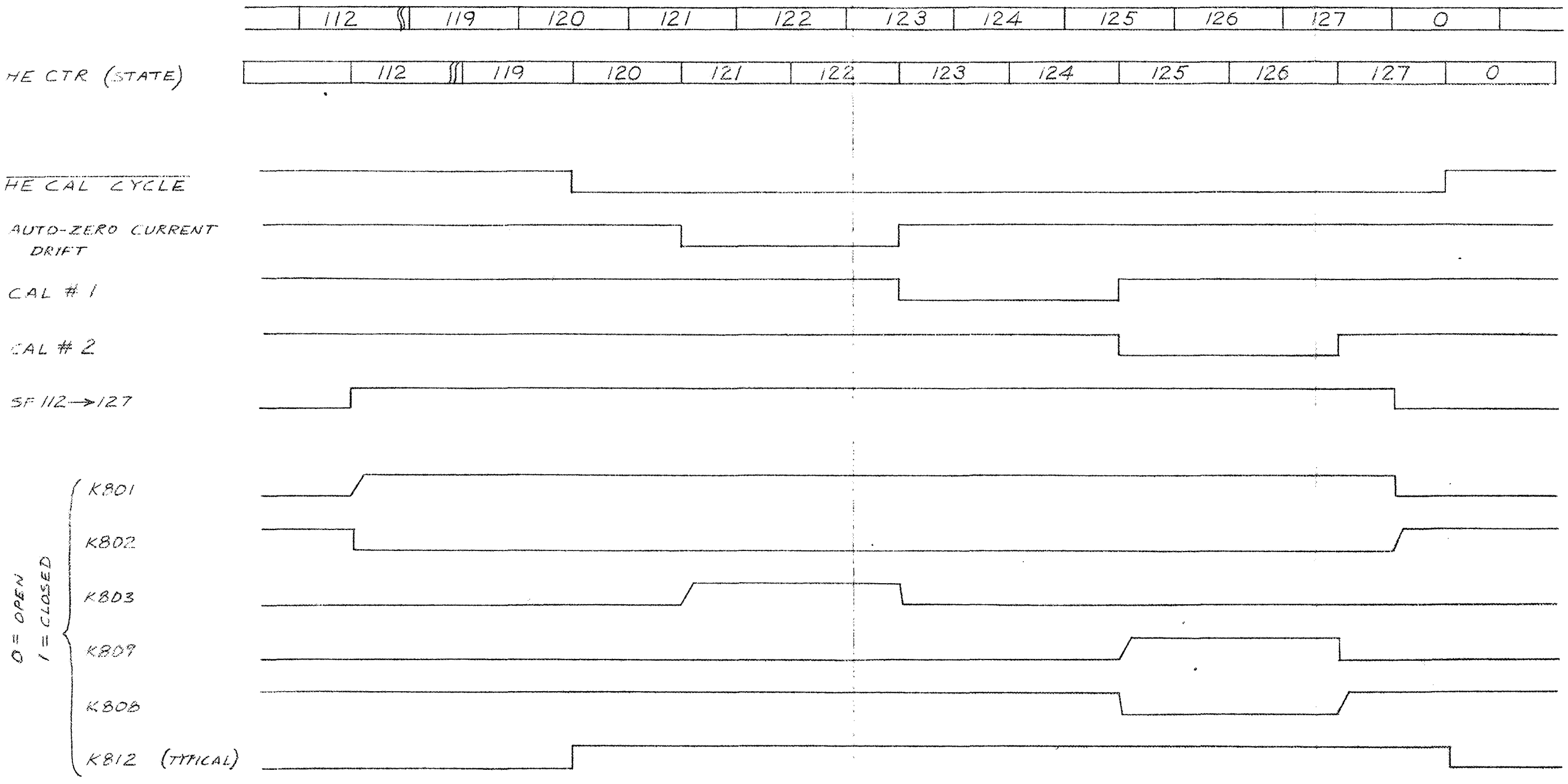


FIGURE 5.4.1-7
ELECTROMETER SWITCHING
TIMING DIAGRAM

The Electrometer Power Supply furnishes the following supply voltages:

- o +8V to Seal Break Circuit
- o 0.625V to Electrometer Tubes

The range monitor network is a voltage divider operating off the Electrometer power supply and the range-select relay coils. Its output level indicates the Electrometer range in effect:

RANGE	DC LEVEL MONITORED
1	Approximately 8V
2	Approximately 4V
3	Approximately 2.7V

The relay coils are driven by a load-and-temperature compensated power supply consisting of a programmed voltage divider. The +8V source is divided down to +5.5V which is regulated by thermistors and a switched load. The +5.5V is the power source for the relay coils.

5.4.2 Sensor

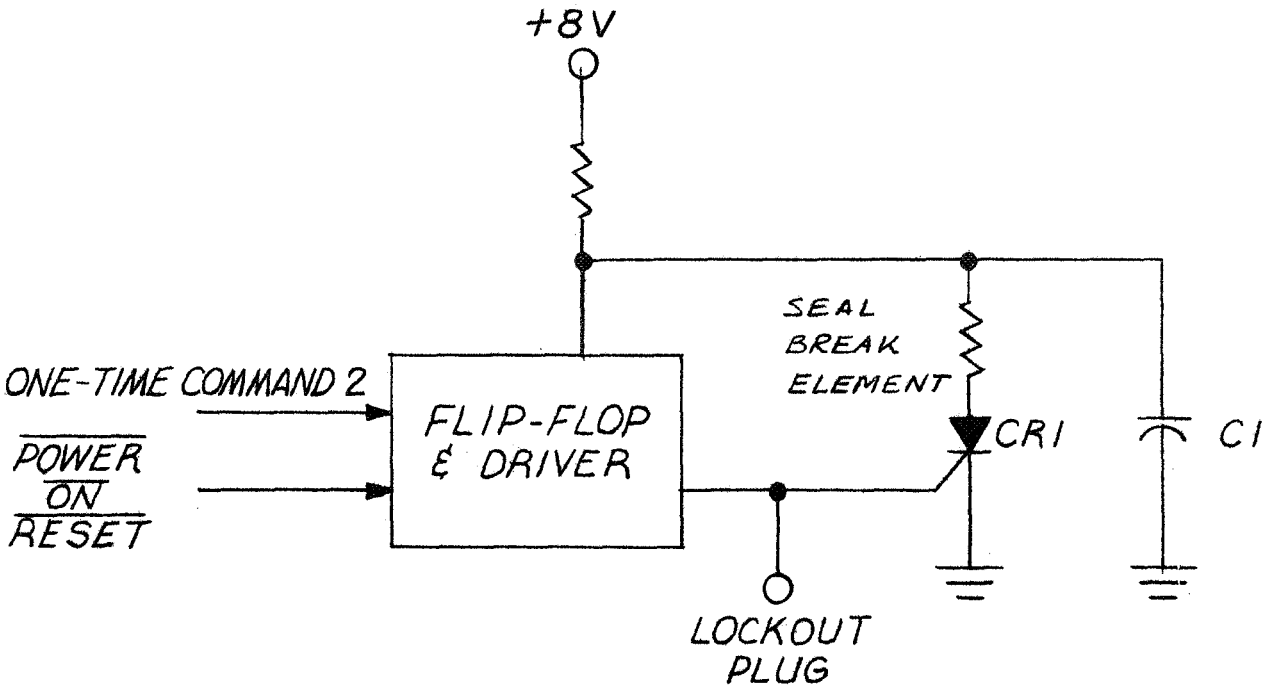
The CCGE sensor is a plasma discharge device which effects conversion of density to direct durrent. It is mounted in a sealed case and protected by a dust-cover seal from premature contamination. The Cold Cathode Ion Gauge assembly (CCIG) is shown in Figure 7-1.

The sensor is powered by 4.5 kV and draws approximately 1 μA maximum. Output current to the electrometer is a function of pressure, and is shown plotted in Figure 5.4.1-2 for pressures from 10^{-6} torr to 10^{-11} torr.

5.4.3 Seal Mechanism Power Supply

See Figure 5.4.3-1 for a simplified block diagram of the Seal Mechanism Power Supply.

When system power is applied, the $\overline{\text{Power On Reset}}$ logic control function pulses momentarily to a "0" state, resetting the flip-flop. This causes the driver to hold the SCR CR1 off. C1 charges to +8V.



(REF DRAWING W7194)

FIG. 5.4.3-1 BLOCK DIAGRAM, SEAL MECHANISM POWER SUPPLY

When any command containing Command 2 is executed, one-time Command 2 causes the flip-flop to set, thus allowing the driver to fire the SCR. C1 discharges through the seal-break element and the SCR. The CCIG seal is then broken by the heat generated by the energy transfer.

The lock-out plug holds the gate of CR1 at ground potential. This prevents firing of the seal during ground tests.

The Seal Monitor provides a dc level to the One-Time Command Status monitor to indicate status of the seal. A "0" level at the Seal Monitor indicates the seal has fired.

5.4.4 Seal Mechanism

The Seal Mechanism (squib) is customer furnished equipment. It is a pyrotechnic device attached to one end of the CCIG seal. Breaking of the mechanism releases the seal to expose the CCIG to the lunar environment. See Section 5.4.3.

5.4.5 4500 Volt Power Supply

Figure 5.4.5-1 shows a simplified Block diagram of the 4500 volt Power Supply.

The 4500 volt Power Supply is used to develop a 4500 volt potential to be applied to the Cold Cathode Ion Gauge (CCIG) anode.

The supply consists basically of a regulator, converter, a voltage-multiplier network, and associated feedback network of the Low Voltage Power Supply. The regulator furnishes approximately 24V to the converter for conversion to a 5kHz squarewave to be applied to the converter transformer. Output of the converter transformer is applied to a voltage multiplier network (stacked standard doublers). The output is then filtered and applied to the CCIG anode. The output is also divided down for Analog-to-Digital conversion, and monitored at various SIDE Frames (during Word 2) according to the format in drawing 609206.

During pre-flight tests at ambient air pressures, a lockout plug is connected to the system, grounding the collector of Q2 (Figure 5.4.5-1, Simplified Block Diagram of the 4.5kV Power Supply). This causes the regulator to be inhibited and the high voltage output to be zero. Prior to flight (or simulated flight), the lockout plug is removed, causing the 4.5kV Power Supply to be ON when power is applied to the system (the CCGE HV ON/OFF logic control function is normally at a "1" state). When Command 13 (CCIG High Voltage ON/OFF) is executed, the CCGE HV ON/OFF logic control function switches

(REF DRAWING 609584)

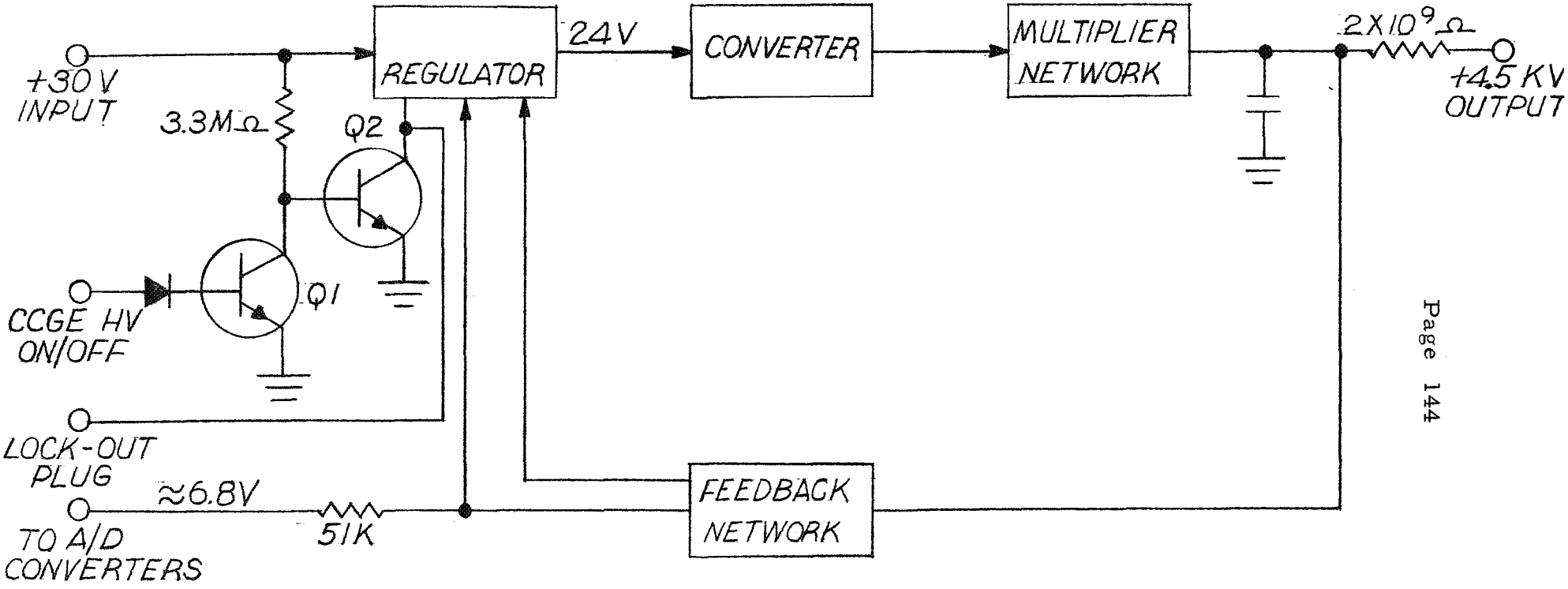


FIG. 5.4.5-1 SIMPLIFIED BLOCK DIAGRAM, 4500V POWER SUPPLY

to a "0" state, turning OFF Q1. This causes the base of Q2 to be driven, turning Q2 ON. This in turn inhibits the regulator and turns the high voltage OFF. Executing Command 13 once more turns the high voltage back ON.

5.4.6 Temperature Sensor and Monitoring Circuit

See Section 5.1.2 for a general description of the Temperature Sensors and Monitoring Circuits.

5.5 Ground Plane

5.5.1 Ground Plane Step Voltage Generator

A simplified block diagram of the Ground Plane Step Voltage Generator is shown in Figure 5.5-1. The purpose of the Ground Plane step Voltage Generator is to generate a total of twenty-four voltage steps (twelve positive and twelve negative) which are applied to the Ground Plane screen. The generator is stepped using five bits of digital information from the Ground Plane Counter.

The potentials generated are shown in Table 5.5A. Also shown are the voltages monitored for analog-to-digital conversion. Ground Plane Voltage data is read out during Word 2 of SIDE Frames 13, 15, 29, 31, 45, 47, 61, 63, 69, 77, 79, 93, and 95.

Appendix VII shows a "worst case" error analysis of the Ground Plane Step Voltage Generator.

5.5.1.1 Ground Plane Counter

The Ground Plane Counter is a five-bit binary counter, providing a binary count necessary to properly address the Ladder Switch and Network. The counter is stepped by the Ground Plane Counter Advance pulse, which is generated when the SIDE Frame Counter recycles to 000. The Ground Plane Counter Advance pulse is generated at Word 9 during the last SIDE Frame before stepping to SIDE Frame 000. The Ground Plane Counter is automatically reset by the Power On Reset pulse when power is first applied. This is done in order to synchronize the Ground Plane Counter with the SIDE Frame Counter.

Under normal conditions, the $\overline{\text{Command 1}}$ logic control function is at a "1" state, preventing the Counter Inhibit circuit from operating. This allows the Ground Plane Counter to be stepped. When Command 1 (Ground Plane Stepper On/Off) is executed, $\overline{\text{Command 1}}$ switches to a "0" state for 17 microseconds. This then causes the Counter Inhibit circuit to be operative, thus preventing the Ground Plane Counter from being stepped.

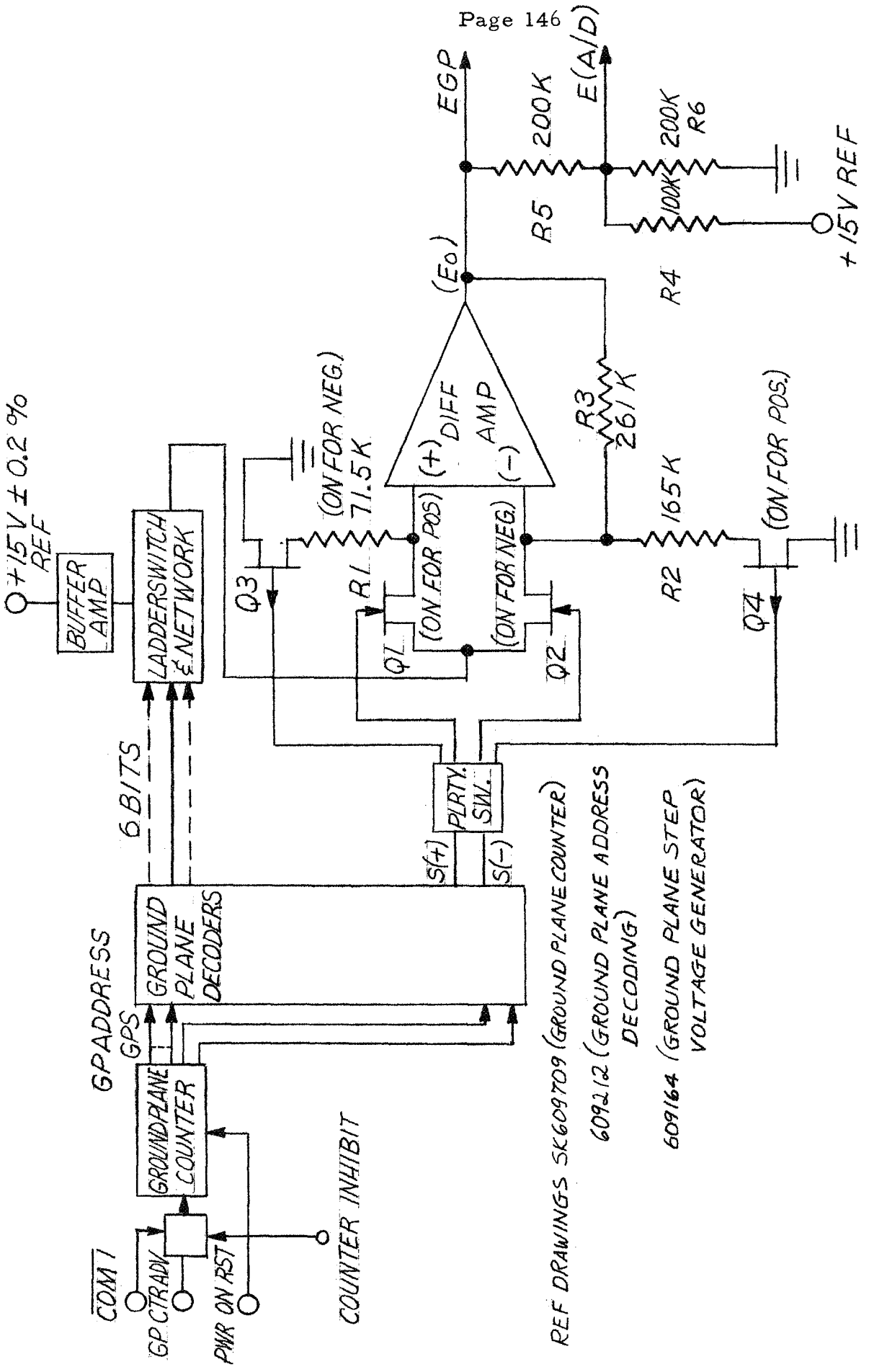


FIG 5.5-1, SIMPLIFIED BLOCK DIAGRAM OF GROUND PLANE STEP VOLTAGE GENERATOR

TABLE 5.5A: Ground Plane and A/D Monitor Voltages

Ground Plane Voltage Step	E_{GP}	A/D Monitor Voltage
1	0	7.50V
2	0.6	7.65
3	1.2	7.80
4	1.8	7.95
5	2.4	8.10
6	3.6	8.40
7	5.4	8.85
8	7.8	9.45
9	10.2	10.05
10	16.2	11.55
11	19.8	12.45
12	27.6	14.40
13	0	7.50
14	- 0.6	7.35
15	- 1.2	7.20
16	- 1.8	7.05
17	- 2.4	6.90
18	- 3.6	6.60
19	- 5.4	6.15
20	- 7.8	5.55
21	-10.2	4.95
22	-16.2	3.45
23	-19.8	2.55
24	-27.6	0.60

When Command 1 is again executed, $\overline{\text{Command 1}}$ switches to a "0" state for 17 microseconds. This causes the Counter Inhibit circuit to be operative once more, allowing the Ground Plane Counter to be stepped again.

Figure 5.5-2 shows the timing relationships for the Ground Plane Counter Advance pulse. Table 5.5B shows the Ground Plane Counter binary output. See Figure 5.2.8-3 for timing of the Power On Reset pulse.

5.5.1.2 Ground Plane Decoders; Ladder Switch and Network

The output of the five-bit counter addresses the Ground Plane Decoders and Polarity Switches. The decoded output of the Ground Plane Decoder is a six-bit address which is used to control the Ladder Switch and Network. The Ladder Switch and Network, referenced by a precision +15V source through the +15V Buffer Amplifier, furnishes an analog voltage to the Ground Plane Stepper Amplifier, depending upon the address programming the Ladder Network. Refer to Table 5.5C for the Ladder network output voltages.

Figure 5.5-3 shows the equivalent circuits for the Ladder network and Polarity Switches. The Ladder is shown addressed to Step 1, and the Polarity Switches are shown in Positive Configuration.

Table 5.5B shows the binary address available from the Ground Plane Counter. Also shown in Table 5.5B is the address to the Ladder network and Polarity Switch.

5.5.1.3 Ground Plane Amplifier

The amplifier consists of a single-input, single-output differential amplifier with associated feedback and terminating impedances, along with an output divider and bias circuit to provide a monitor voltage for analog-to-digital conversion.

The amplifier is operated in two configurations:

- Positive configuration. As the Ground Plane Counter is stepped through the first twelve voltage steps, the Polarity Switches cause Q1 and Q4 to be ON and Q2 and Q3 to be OFF (See Figure 5.5-1).

  Refer to Figure 5.5-4 for the equivalent circuit and gain equations. This is the standard configuration for a non-inverting differential amplifier.

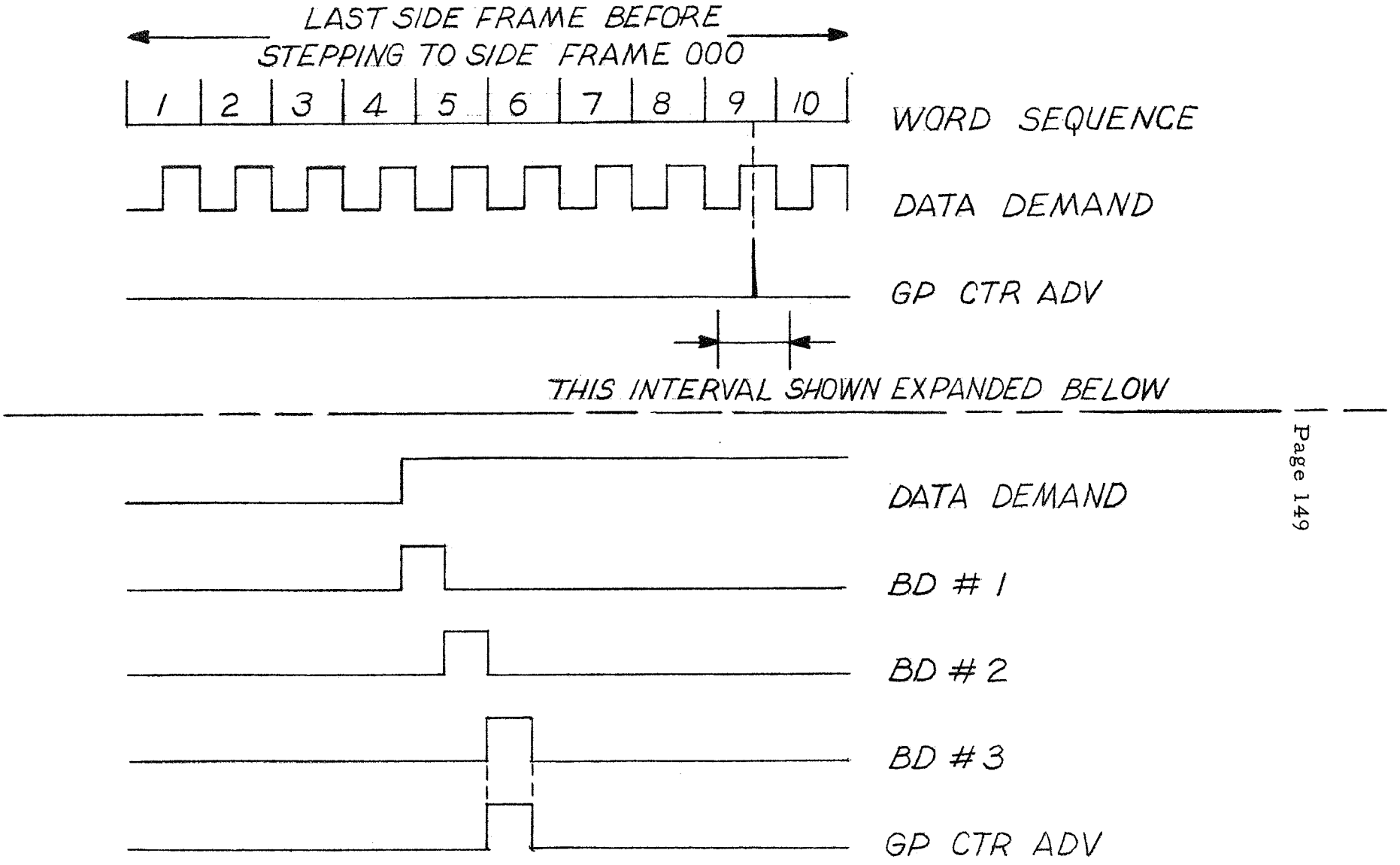
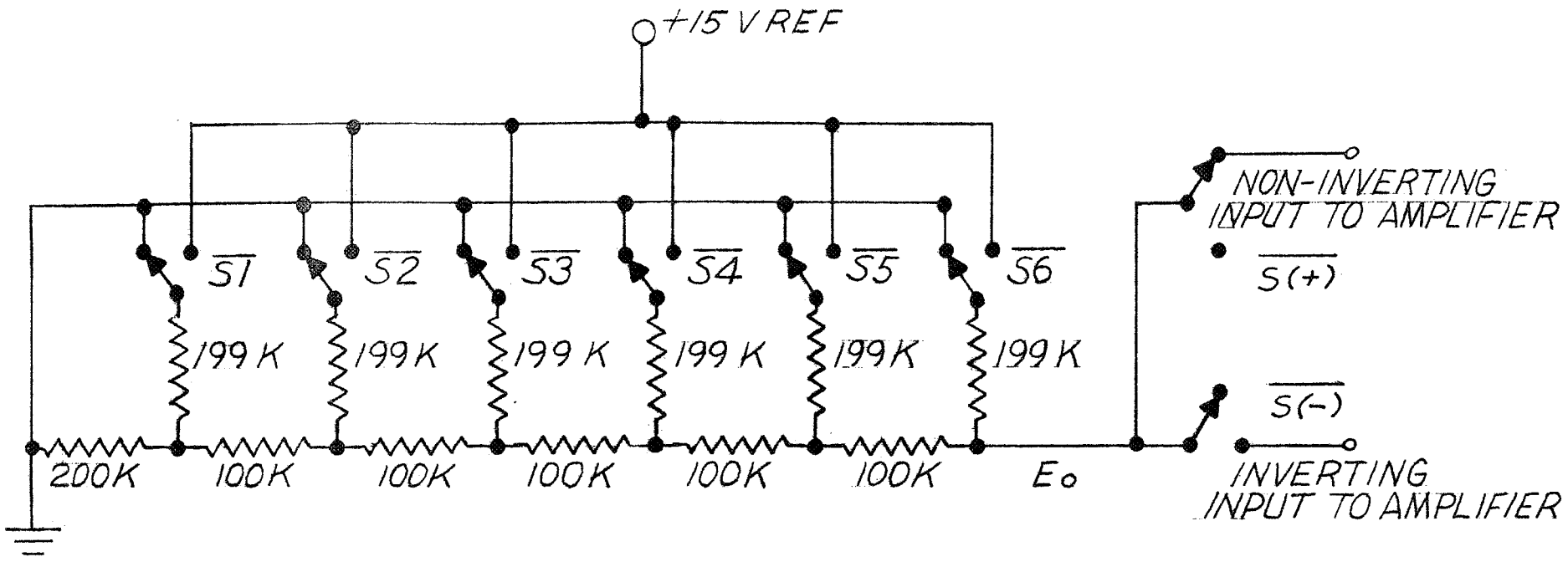


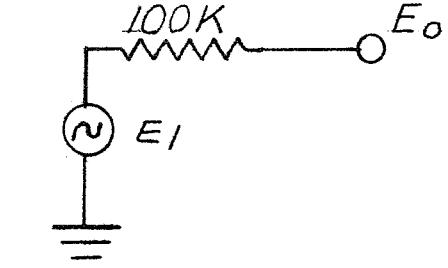
FIG 5.5-2, GROUND PLANE CTR ADVANCE TIMING



LADDER SWITCH & NETWORK
(SHOWN ADDRESSED TO GROUND PLANE STEP 1)

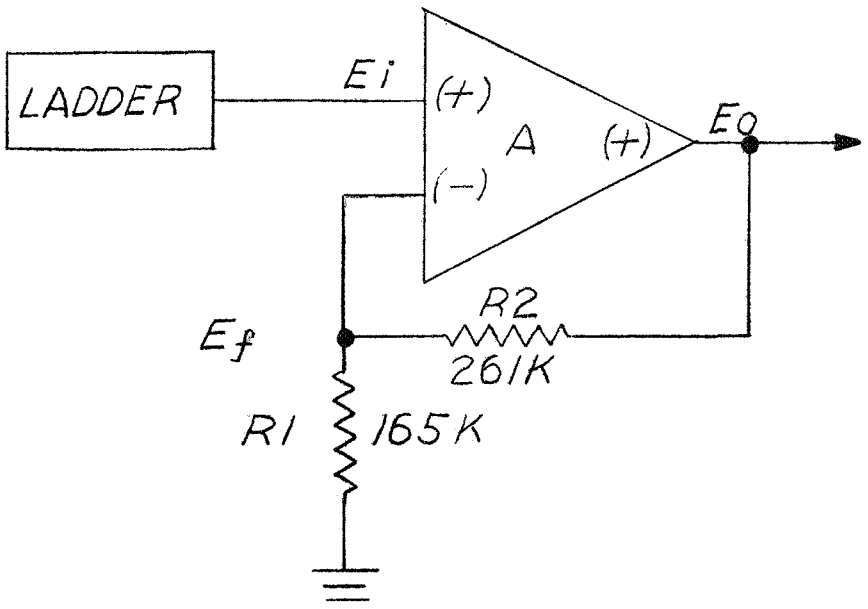
POLARITY SWITCHES
(SHOWN FOR POSITIVE CONFIGURATION)

FEEDBACK SWITCHING NETWRK
NOT SHOWN- SEE FIG 5.5-1



LADDER OUTPUT
IMPEDANCE

FIG 5.5-3, EQUIVALENT CIRCUIT: LADDER SWITCH & NETWORK & POLARITY SWITCHES



$$E_f = \frac{E_o R_1}{R_1 + R_2}$$

$$E_i = E_f$$

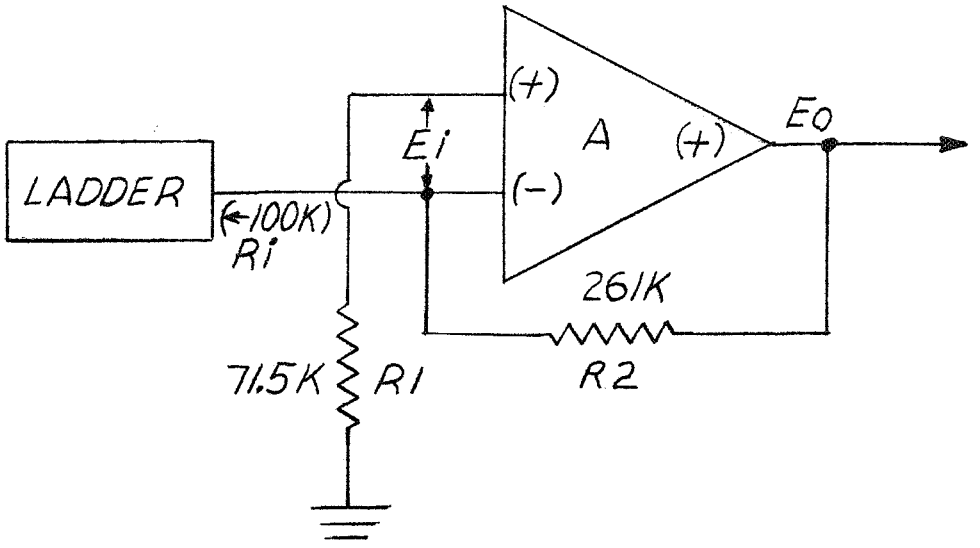
$$E_i = \frac{E_o R_1}{R_1 + R_2}$$

$$\text{GAIN} = \frac{E_o}{E_i} = \frac{R_1 + R_2}{R_1}$$

$$= \frac{165 + 261}{165}$$

$$\text{GAIN} \cong 2.6$$

FIG 5.5-4 GND PLANE AMP. POS CONFIGURATION EQUIVALENT CIRCUIT



$$\frac{E1 - Ei}{Ri} + \frac{E_o - Ei}{R_2} = 0$$

$$E_i = -\frac{E_o}{A}$$

$$E_i \to 0 \Big|_{A \to \infty}$$

$$\frac{E_1}{R_i} + \frac{E_o}{R_2} = 0$$

$$\frac{E_1}{R_i} = -\frac{E_o}{R_2}$$

$$\text{GAIN} = \frac{E_o}{E_1} = \frac{-R_2}{R_i} \approx 2.6$$

WHERE:

E1 = LADDER OPEN CIRCUIT OUTPUT VOLTAGE

Ri = LADDER OUTPUT Z

FIG 5.5-5 GND PLANE AMP. NEG CONFIGURATION EQUIVALENT CIRCUIT

TABLE 5.5B: Ground Plane Stepper Address Logic

Step No.	Ground Plane Counter					Address to Ladder (Output of Decoders)						Polarity Switch	
	GPS5	GPS4	GPS3	GPS2	GPS1	S6	S5	S4	S3	S2	S1	S+	S-
1	0	0	0	0	0	0	0	0	0	0	0	1	0
2	0	0	0	0	1	0	0	0	0	0	1	1	0
3	0	0	0	1	0	0	0	0	0	1	0	1	0
4	0	0	0	1	1	0	0	0	0	1	1	1	0
5	0	0	1	0	0	0	0	0	1	0	0	1	0
6	0	0	1	0	1	0	0	0	1	1	0	1	0
7	0	0	1	1	0	0	0	1	0	0	1	1	0
8	0	0	1	1	1	0	0	1	1	0	1	1	0
9	0	1	0	0	0	0	1	0	0	0	1	1	0
10	0	1	0	0	1	0	1	1	0	1	1	1	0
11	0	1	0	1	0	1	0	0	0	0	1	1	0
12	0	1	0	1	1	1	0	1	1	1	0	1	0
13	1	0	0	0	0	0	0	0	0	0	0	0	1
14	1	0	0	0	1	0	0	0	0	0	1	0	1
15	1	0	0	1	0	0	0	0	0	1	0	0	1
16	1	0	0	1	1	0	0	0	0	1	1	0	1
17	1	0	1	0	0	0	0	0	1	0	0	0	1
18	1	0	1	0	1	0	0	0	1	1	0	0	1
19	1	0	1	1	0	0	0	1	0	0	1	0	1
20	1	0	1	1	1	0	0	1	1	0	1	0	1
21	1	1	0	0	0	0	1	0	0	0	1	0	1
22	1	1	0	0	1	0	1	1	0	1	1	0	1
23	1	1	0	1	0	1	0	0	0	0	1	0	1
24	1	1	0	1	1	1	0	1	1	1	0	0	1

TABLE 5.5C: Ground Plane Ladder Network Output Voltage

Ground Plane Voltage Step	Ladder Output Voltage
1	0
2	0.232
3	0.464
4	0.696
5	0.928
6	1.392
7	2.088
8	3.016
9	3.944
10	6.264
11	7.656
12	10.672
13	0
14	0.232
15	0.464
16	0.696
17	0.928
18	1.392
19	2.088
20	3.016
21	3.944
22	6.264
23	7.656
24	10.672

The output of this configuration is a positive voltage, which is applied to the Ground Plane Screen.

o Negative Configuration. As the Ground Plane Counter is stepped from the 13th through 24th voltage step, the Polarity Switches cause Q2 and Q3 to be ON, and Q1 and Q4 to be OFF(See Figure 5.5-1).

Refer to Figure 5.5-5 for the equivalent circuit and gain equations. This is the standard configuration for an inverting differential amplifier.

The output of this configuration is a negative voltage, which is applied to the Ground Plane Screen.

The output divider and bias circuit provide stepped-down monitor voltage (positive for all twenty-four steps) for analog-to-digital conversion.

This E_{mon} is given by: $E_{mon} = \frac{15 + \frac{E_{GP}}{2}}{2}$ volts.

Table 5.5A shows the monitor voltages for each Ground Plane voltage step.

The monitored voltages are then fed to the analog-to-digital converters. The commutated voltages are thereby transformed by the A/D Converter into a binary readout proportional to the log of the monitored voltage.

6.0 EXPERIMENT TEST SET

The Experiment Test Set (ETS) is provided to perform the functions needed to test and verify the proper operation of the SIDE/CCGE Experiment.

These functions are:

- o ALSEP Simulation - Providing the operation power, command signals and communication signals required to operate the Experiment.
- o Data Reduction and Conversion - Processing the derived SIDE/CCGE data for visual display, printing and transmission.
- o ALSEP Interface Monitoring - Providing operation monitoring when ALSEP is interfaced with the SIDE/CCGE Experiment.
- o Trouble-shooting - Providing the diagnostic equipment necessary to locate and analyze equipment malfunctions.

Figures 6.0-1, 6.0-2, and 6.0-3 show, by block diagram, the possible ALSEP/SIDE/CCGE/ETS interfaces. Figure 6.0-4 shows the block diagram of the ETS. Figure 6.0-5 shows a typical Instrument/ETS Test Setup. Figure 6.0-6 shows a front view of the ETS configuration.

See Appendix VIII for the Master Drawing List for the ETS. The major subassemblies of the ETS are:

Data Processor: Accepts digital data from the SIDE/CCGE, processes the data, and routes it to the Printer, Data Phone, and Display Unit.

Printer Unit: Prints hard copy data from the Data Processor/Print/Phone Unit.

Display Unit: Displays data from the Data Processor/Print/Phone Unit visually on nixie tubes.

ALSEP Simulator Unit: Transmits timing and command signals which simulate the function of ALSEP and supplies power to the SIDE/CCGE during test.

Monitor Unit: Monitors various data points, supply voltages, and interface signals. A Hewlett-Packard 3439A Digital Voltmeter is mounted in this unit.

Oscilloscope/Counter Unit: Contains a type 422 Tektronix oscilloscope, and a Hewlett-Packard 3734A counter.

6.1 Display Unit

The Display Unit is a passive instrument used to visually monitor various functions of the SIDE/CCGE Experiment. Operating controls consist of the power ON/OFF switch and the Overflow Lamp

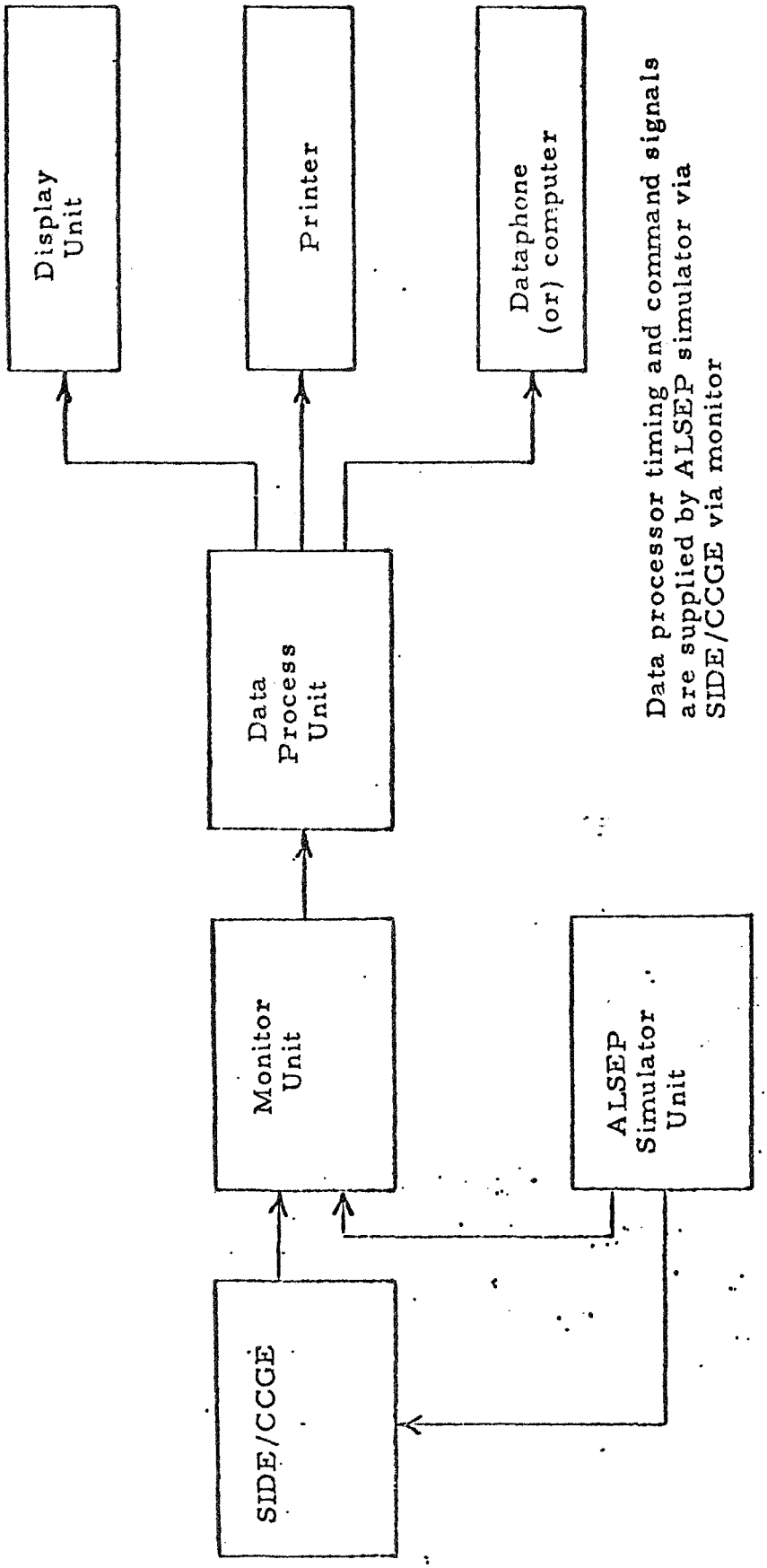


Fig. 6.0-/ System Interface - Configuration 1

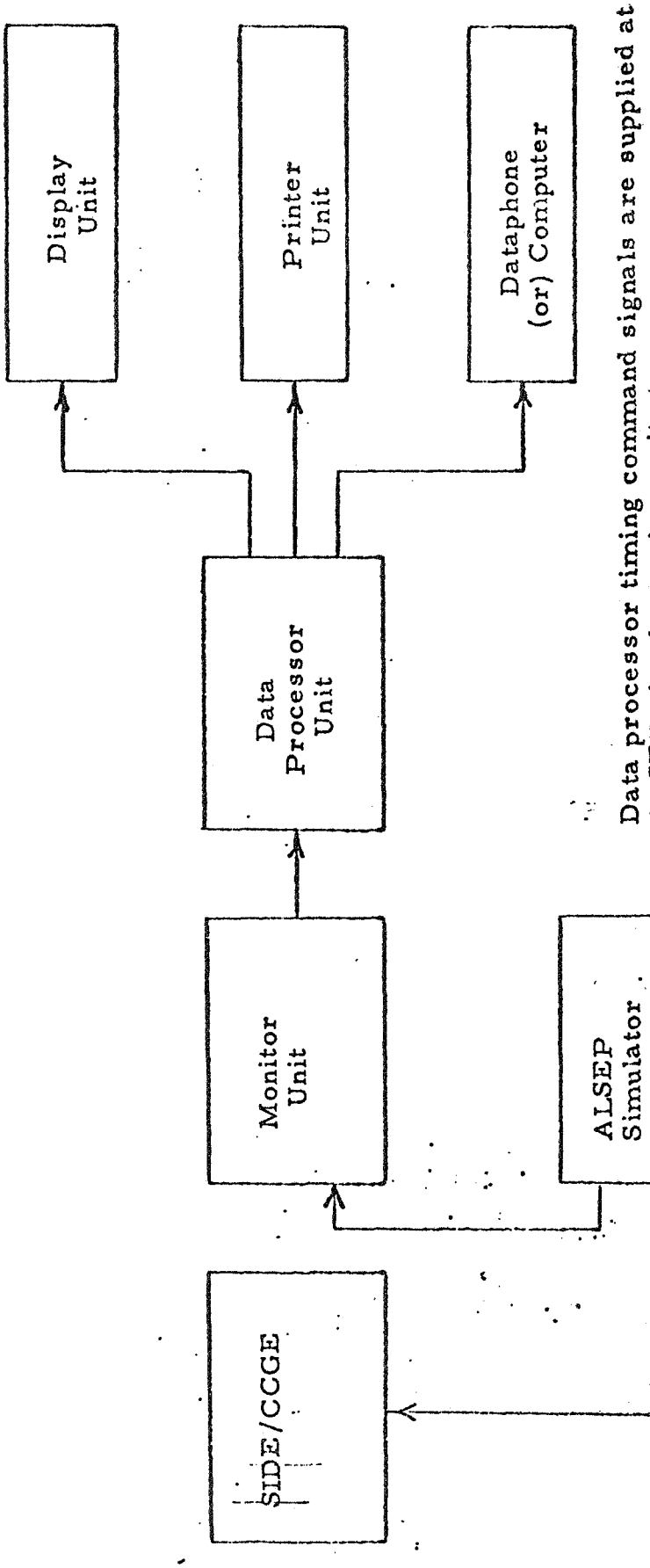


Fig. 6.0-2, System Interface - Configuration 2

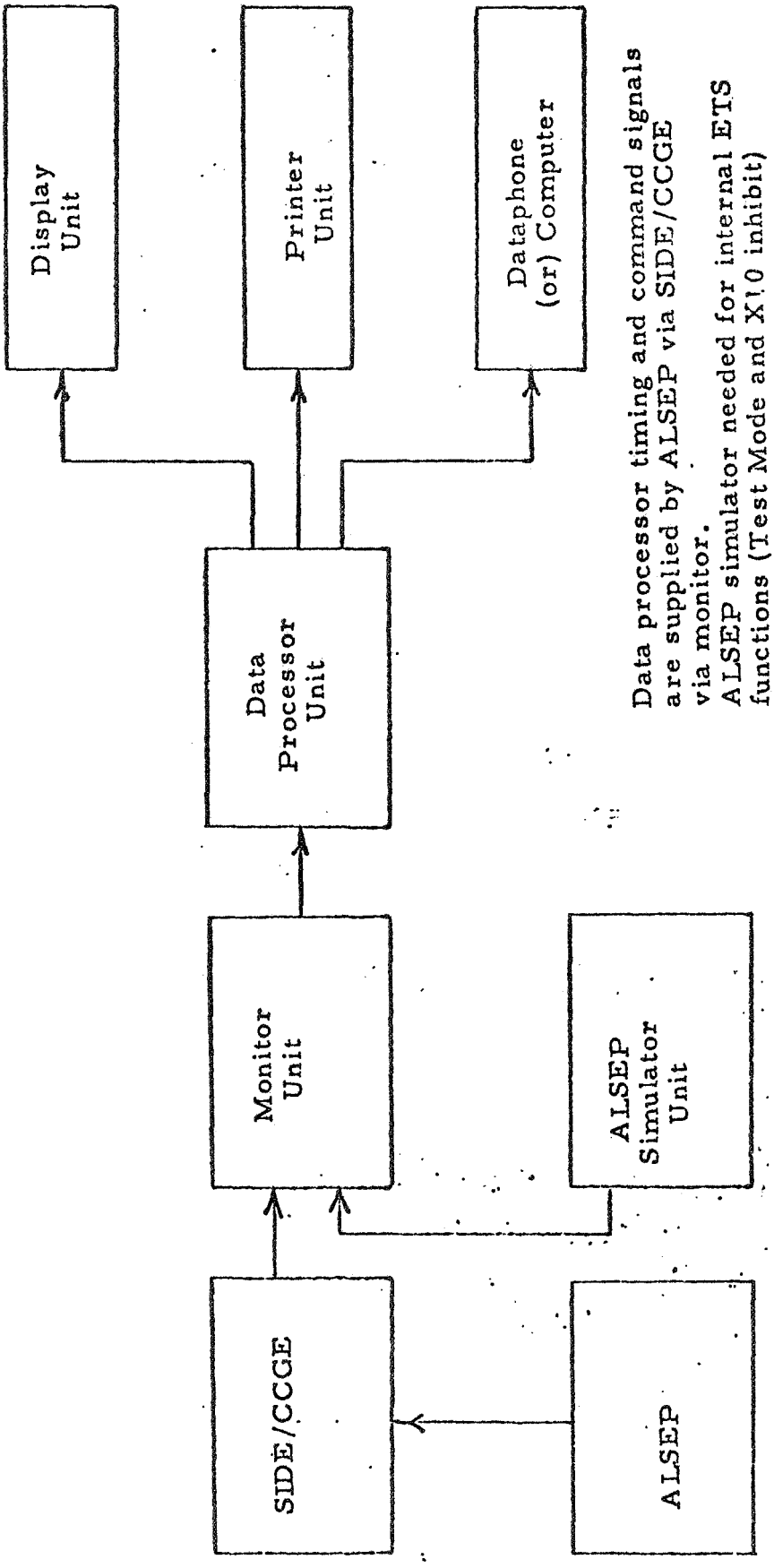


Fig. 6.0-3 System Interface - Configuration 3

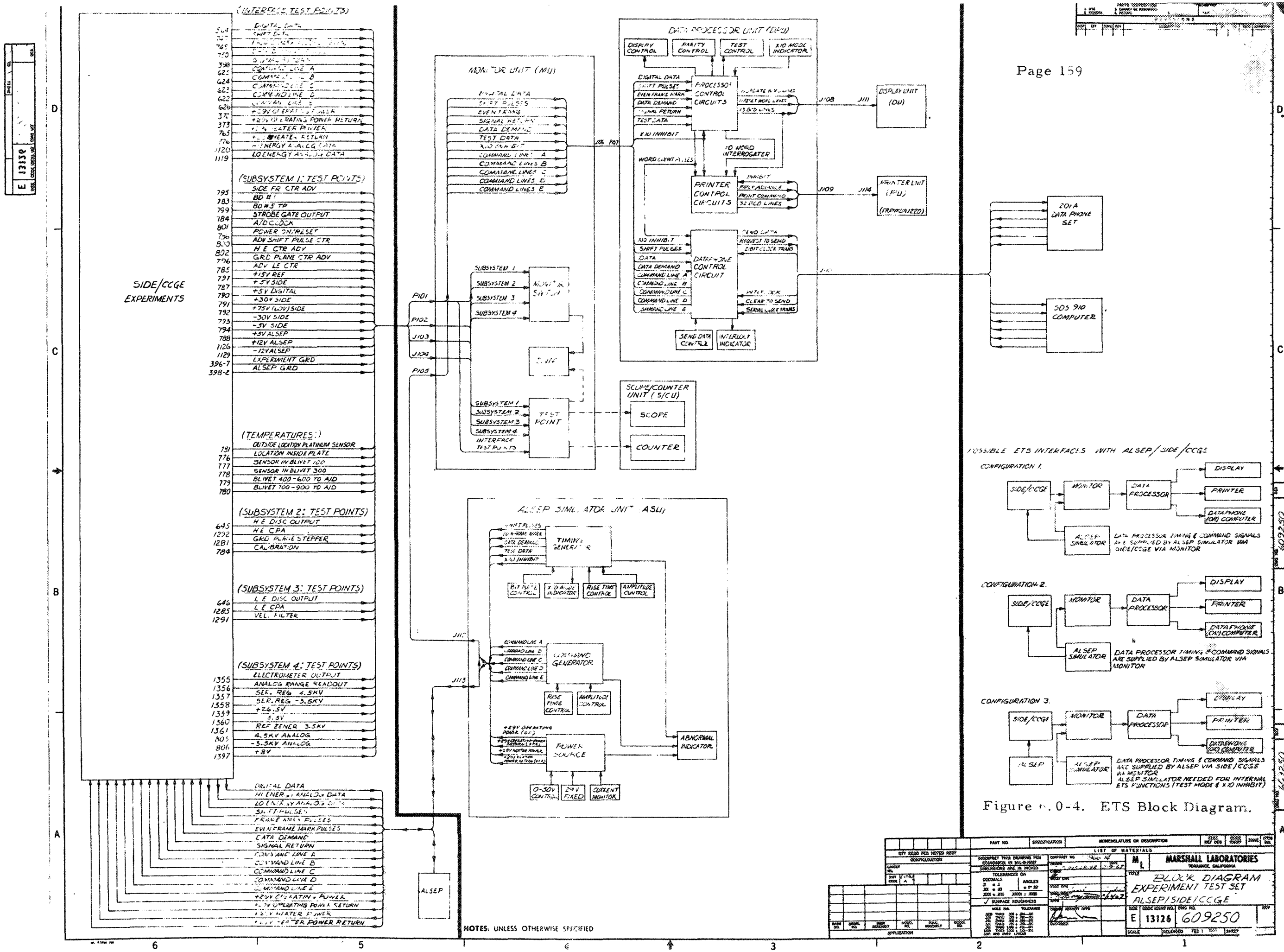


Figure 6.0-4. ETS Block Diagram.

NOTES: UNLESS OTHERWISE SPECIFIED

SIZE	E
CAGE IDENT NO.	13126
DWG NO.	609250
SCALE	
RELEASED	FEB 1

MARSHALL LABORATORIES, TORRANCE, CALIFORNIA

TITLE: BLOCK DIAGRAM EXPERIMENT TEST SET ALSEP/SIDE/CCGE

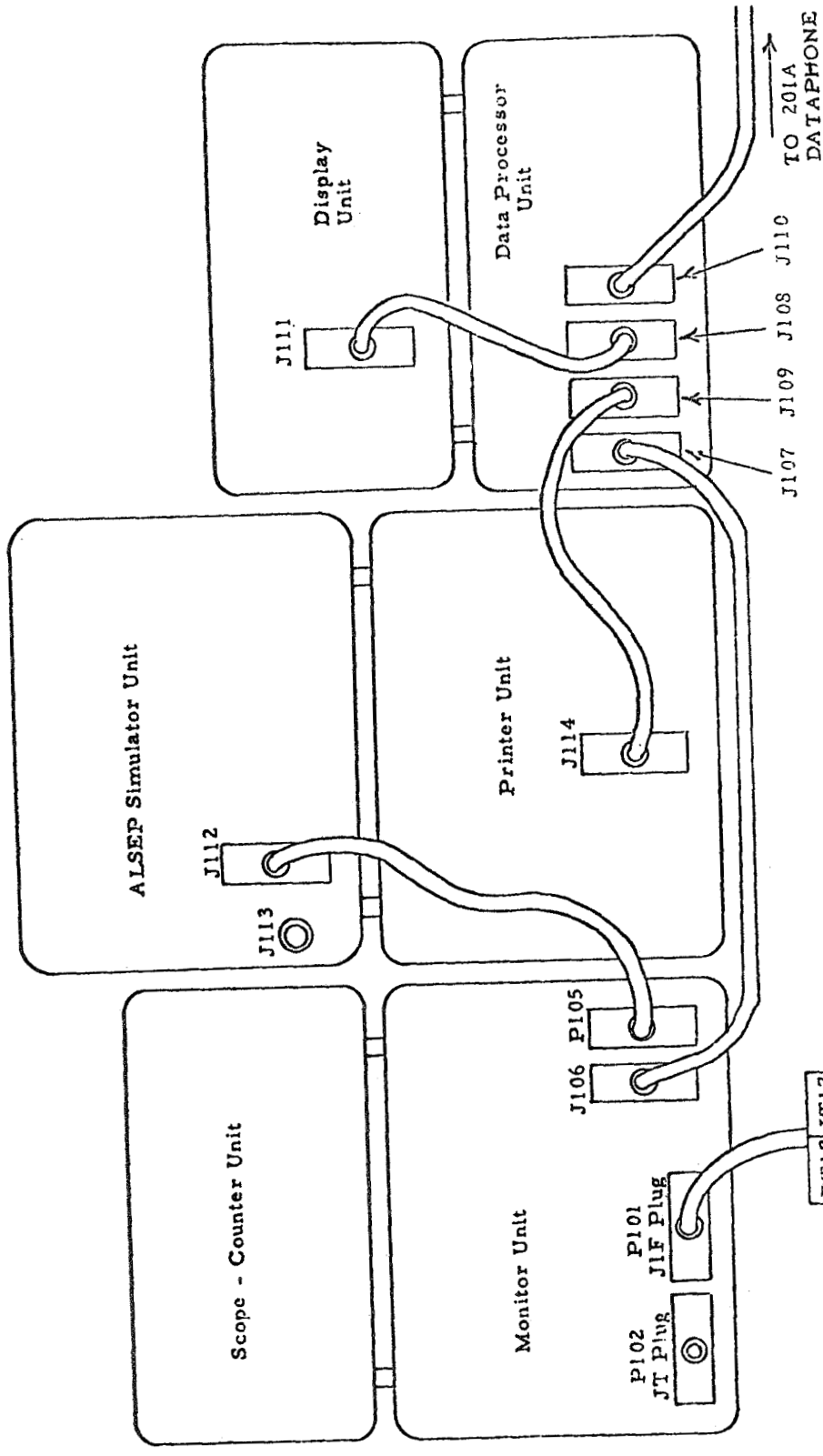


FIGURE 6.0-5 INSTRUMENT/ETS TEST SET UP (TYPICAL)

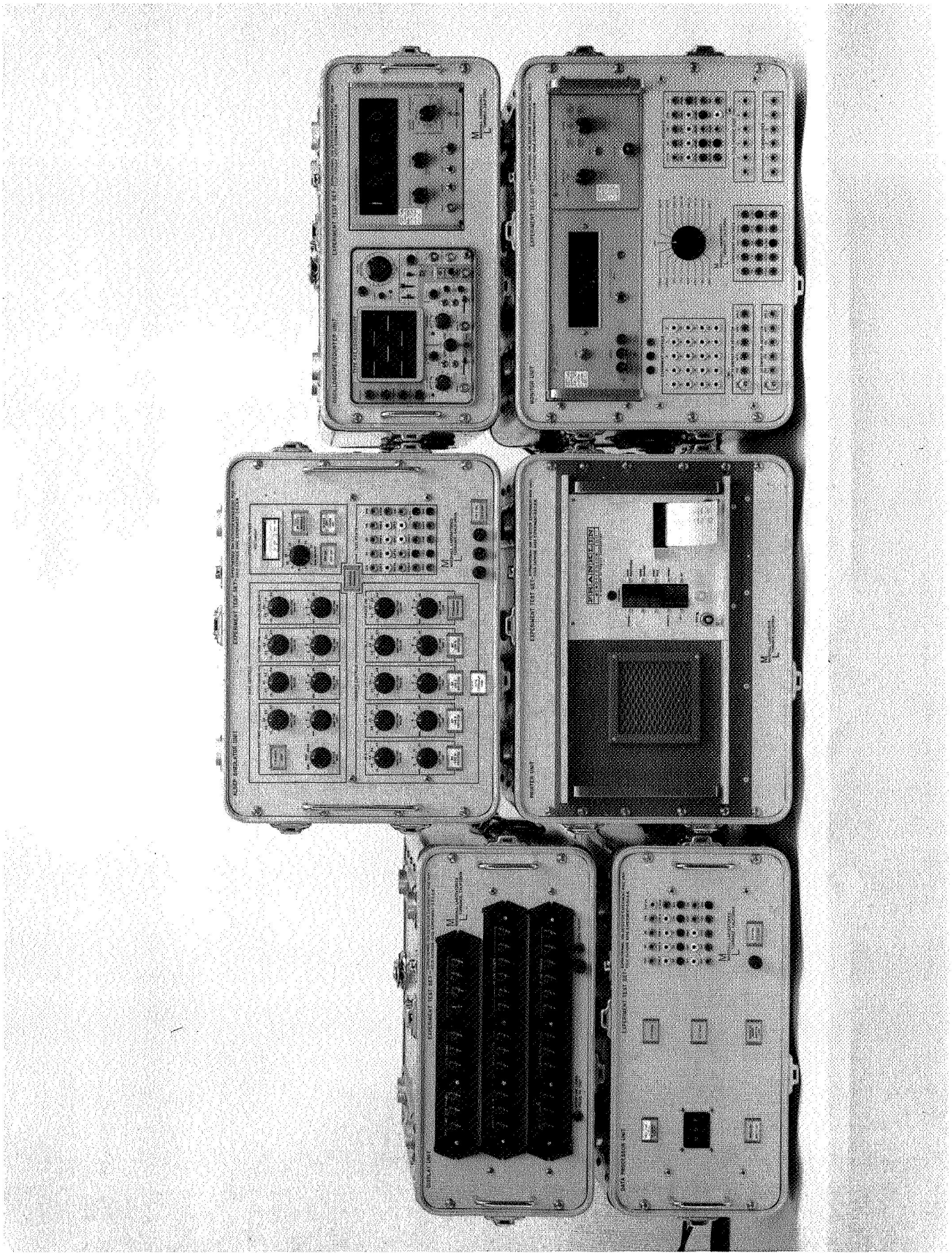


FIGURE 6.0-6 ETS CONFIGURATION

test switch. The test switch is used to verify lamp operation prior to each Experiment test. No other operation of the Display Unit is required.

The visual display presented by the unit represents a binary to decimal decoding of the ten words contained in each SIDE frame. A total of 127 SIDE frames are displayed during each Experiment cycle. The following is an explanation of the data contained in each SIDE Frame.

SIDE FRAME (Word 1) - For display purposes, two separate readouts are provided for Word 1. REAL TIME SIDE FRAME indicates the status of the SIDE Frame Counter in the Experiment. The SIDE FRAME display will normally be the same but can be made to hold upon reaching a selected frame by operating the Frame Select switch on the Data Processor Unit. Normal readout will be a number from 000 to 127 representing the decoding of the last seven bits of Word 1. The first bit of the ten bit word is the parity bit giving the odd or even status of the previous SIDE frame. The second and third bits are 0's and represent Word 1. These two bits are used for cueing during printing, Data-phone transmission or when interfaced with ALSEP. When the Parity On switch is operated on the Data Processor Unit, all ten bits are decoded. This results in a readout from 512 to 639. The overflow lamps will light whenever the count exceeds 999.

STATUS (Word 6) - The STATUS display is a four digit readout representing the decimal decoding of a ten bit word indicating the status of the Ground Plane Stepper, Command Input Register, Electrometer Range, Mode Register, Dust Cover and CCIG Seal and Calibration Rates 1 thru 4. Only the last seven bits are normally decoded giving a decimal display of 0000 to 0127. When the Parity On switch is operated the first or parity bit and the second and third bits, 1's indicating Word 6, are also decoded giving a decimal display of 0384 to 1023. To determine the function being monitored, refer to Figure 3.0-3, A/D and Status Sub-Com Sequence.

ANALOG SUB-COM (Word 2) - Temperatures, voltages and other Experiment functions being monitored by the Analog-to-Digital Converter of the Experiment are displayed under ANALOG-SUB-COM. The three digit display represents a decimal decoding of the A/D Converter's eight bit output. The function being monitored by the A/D converter can be determined by referring to Figure 3.0-3. Decoding of the eight bit word will give a decimal readout of 000 to 255. Any number in excess of 255 and/or the lighting of the overflow lamps indicates a malfunction. The correct display of the A/D Converter's output will be found in the Test Specification for the unit undergoing test.

HECPA VOLTS (Word 3), LECPA VOLTS (Word 8), VELOCITY FILTER VOLTS (Word 7), - These three-digit readouts are also decoded displays of the output of the A/D Converter. Interpretation of the display is the same as for ANALOG SUB-COM.

HE ION COUNTS (Words 4 & 5), LE ION COUNTS (Words 9 & 10) - These six-digit displays are derived from the decoding of a 20-bit storage register in the experiment. The registers automatically reset at 999,997, therefore, lighting of either the right or left overflow lamps indicates a malfunction. Two overflow lamps are provided since the six-digit read-out is composed of two ten-bit binary numbers.

For the block diagram of the Display Unit, See Figure 6.1-1. The schematic is shown in drawing 609667. Figure 6.1-2 shows a front view of the Display Unit.

6.2 Data Processor Unit

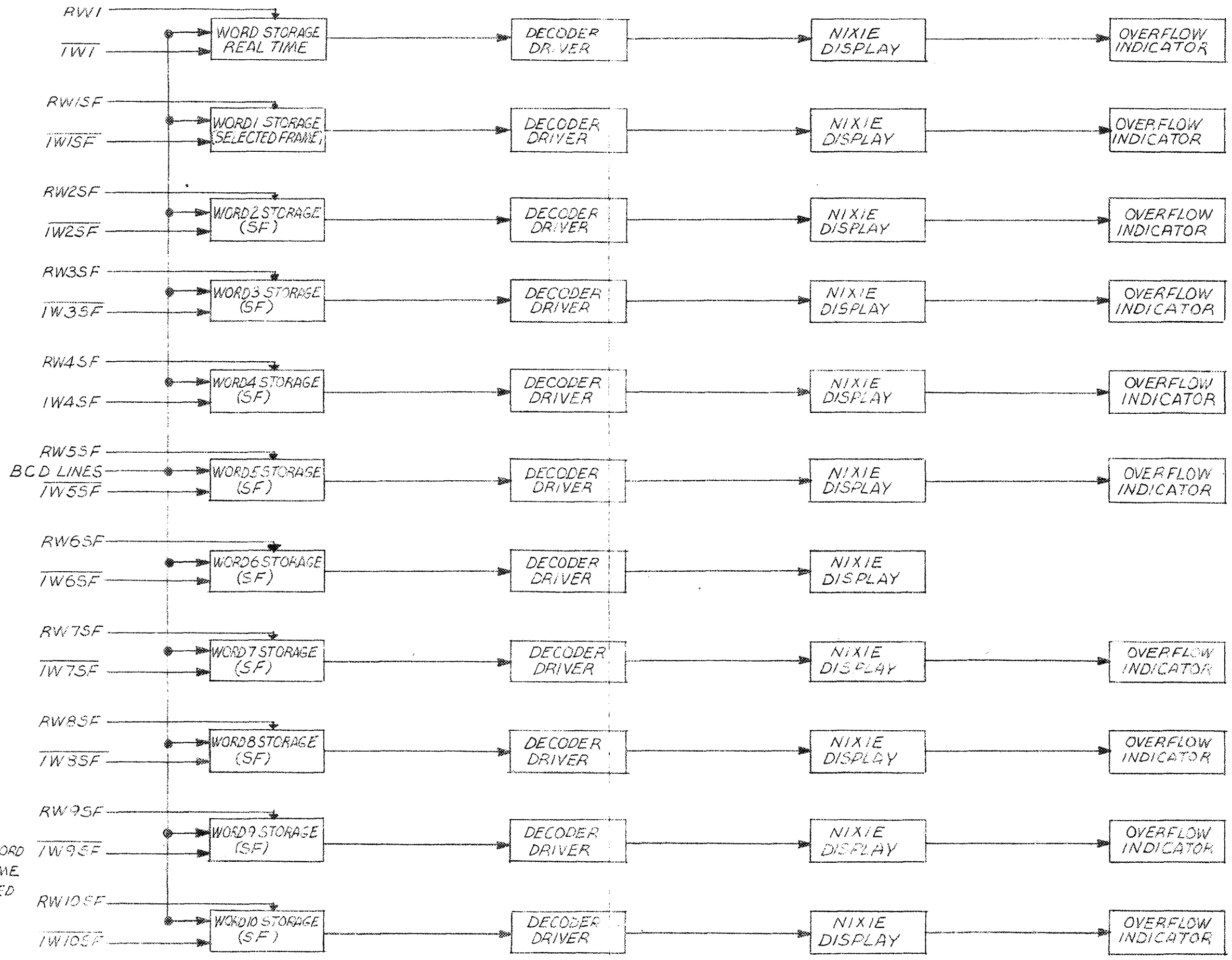
Drawing 609685 shows the schematic diagram of the Data Processor Unit. See Figure 6.2-1 for the block diagram. Figure 6.2-2 shows the Data Processor Unit, front view. The Data Processor Unit receives both the experiment data from the SIDE/CCGE Experiment and the timing signals from the ALSEP Simulator Unit, and provides the decoding logic necessary for the operation of the Dataphone Set, Franklin Printer, and Display Unit.

Also provided by the Data Processor Unit are the controls for parity check, accelerated mode of operation, test mode, Dataphone transmission, and selection and retaining of displayed data for a desired SIDE frame. Also provided are the following buffered test points:

Oscillator	Command A
Shift Pulse	Command B
Data Demand	Command C
Even Frame Mark	Command D
Experiment Data	Command Execute

The following additional test points are furnished:

SD (Send Data	The data to be transmitted appears at this test point.
IT (Interlock)	A positive six-volt potential is provided by the Dataphone Set when the Dataphone is prepared to send or receive data. This Interlock signal is used by the Data Processor logic gates to indicate that the Dataphone is ready.
RS (Request to Send)	When the Dataphone Set is prepared to send or receive data, and the Data On Line switch is



RW = RESET WORD
IW = INTERROGATE WORD
SF = SELECTED FRAME
BCD = BINARY CODED DECIMAL

FIG. 6.1-1
BLOCK DIAGRAM-
DISPLAY UNIT

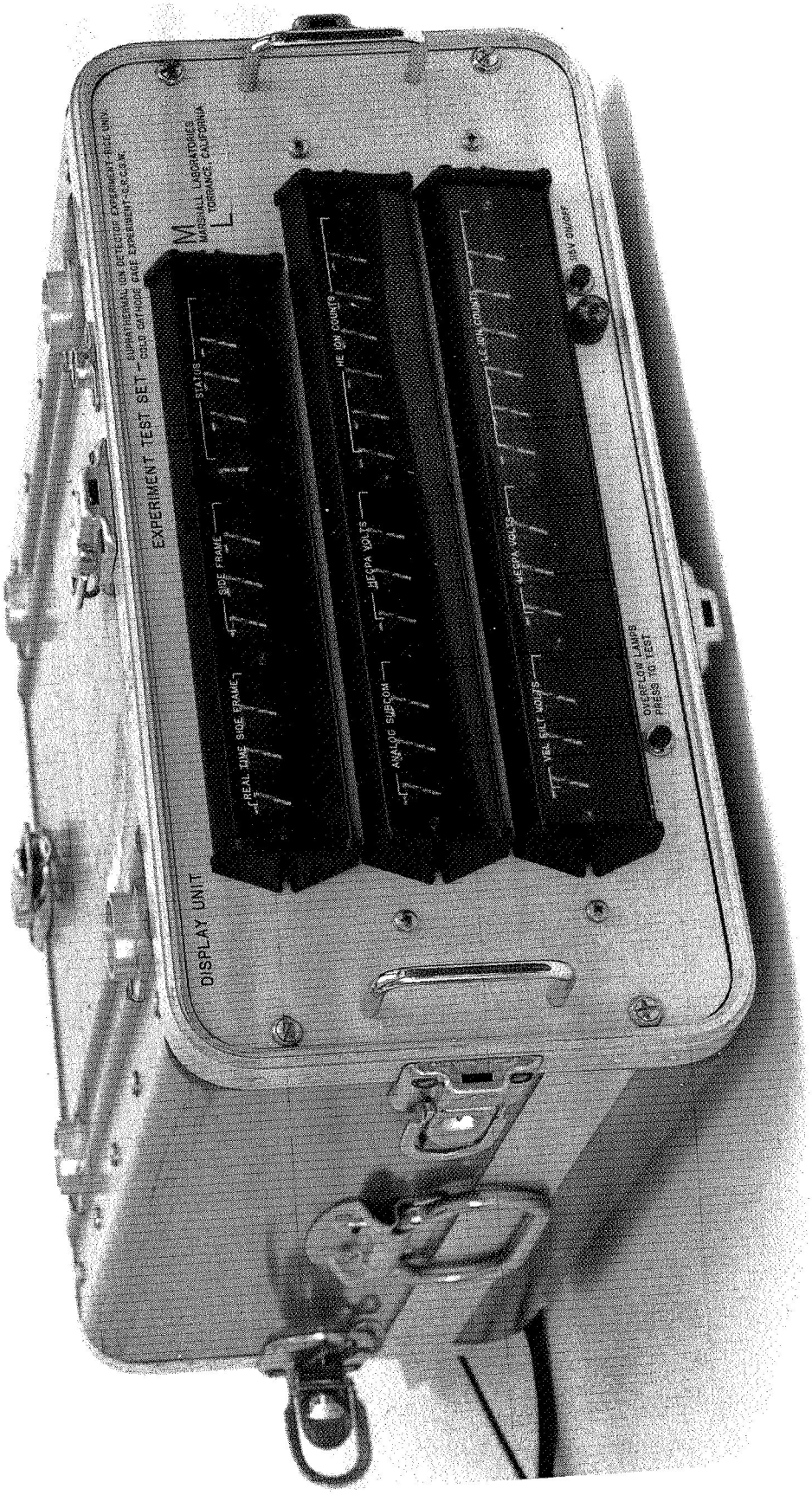


FIGURE 6.1-2 DISPLAY UNIT

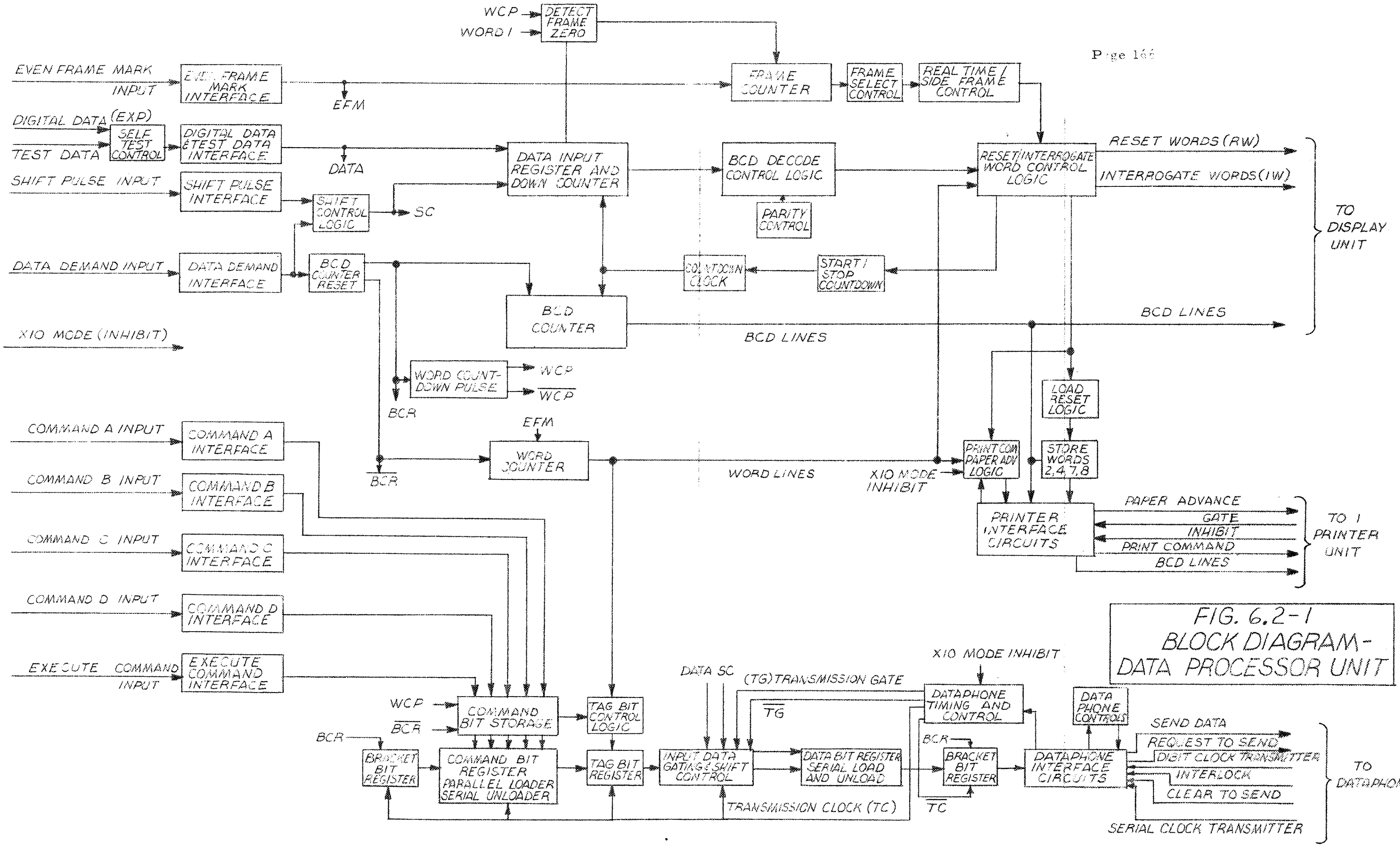


FIG. 6.2-1
BLOCK DIAGRAM-
DATA PROCESSOR UNIT

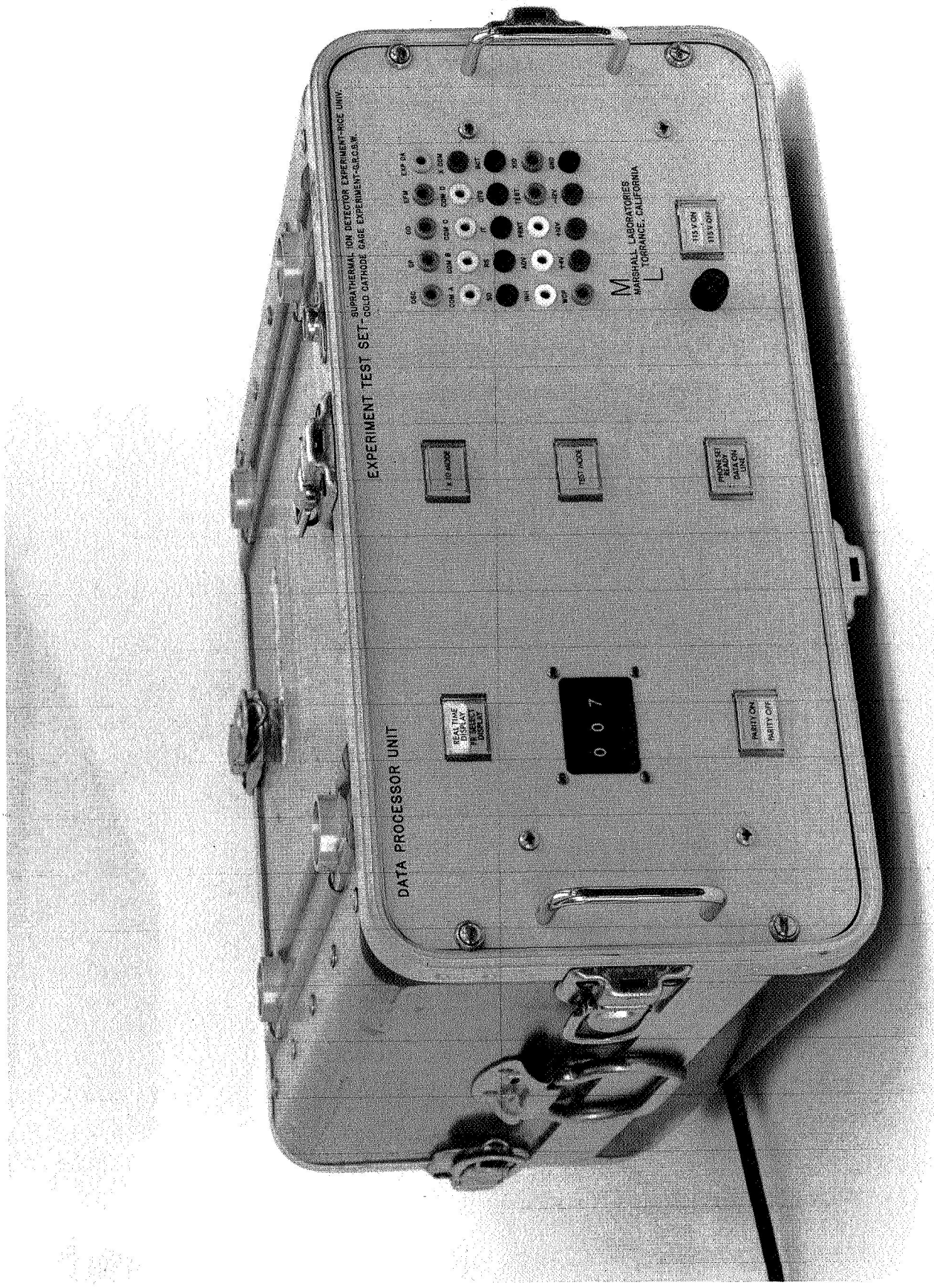


FIGURE 6.2-2 DATA PROCESSOR UNIT

	actuated, RS will switch from -10V dc to +10V dc; this level is sent to the Dataphone Set.
CTS (Clear to Send)	When the Dataphone Set receives the RS (Request to Send) signal, it will provide the CTS signal to the Data Processor. That is, CTS will switch from -6 V dc to +6 V dc. This indicates that the Dataphone will now accept data.
SCT (Serial Clock Transmitter)	This is a 2 kHz square wave constantly furnished by the Dataphone Set as a modulating signal for the Data Processor.
INH, ADV, PRNT	Due to design changes, these test points are no longer used.
X10	This test point monitors the inhibit signal which de-activates the Printer and the Dataphone whenever the ALSEP Simulator is operated in the accelerated mode.
WCP (Word Count Pulse)	This test point monitors the Word Pulses for each SIDE Frame.

In addition, test points are provided for monitoring the following supplies: +4V, +12V, and ground.

When the Display Select switch is operated, either of two conditions may be selected:

- When the Real Time Display portion of the switch is lit, the Display Unit will display real time data.
- When the Frame Select Display portion of the switch is lit, the Display Unit will, when the SIDE Frame counter reaches the SIDE Frame selected by the SIDE Frame Select thumbwheel, display and hold data for that particular SIDE Frame only.

For operation of the Parity ON/OFF switch, see Section 6.1, Display Unit Operation.

When the ALSEP Simulator is operated in the accelerated mode, the X10 Mode indicator will light.

When the Test-Mode switch is actuated, the ALSEP Simulator provides test data for checking out the ETS. The Test Data advances the SIDE Frame display from 000 to 127, then back to 000. The test Data also advances the counts on all displayed words.

A 110 V - 3 amp fuse is also provided.

6.3 ALSEP Simulator Unit

Refer to Figure 6.3-1 for the block diagram of the ALSEP Simulator Unit. Drawing 609668 shows the schematic diagram. See Figure 6.3-2 for a front view of the Simulator Unit. The ALSEP Simulator Unit consists of three experiment control sections, test points to monitor the internal functions of the unit, a running time meter, the power-on/off switch and fuse for the unit itself, and the SIDE/CCGE experiment. The fuses are, from right to left, the ALSEP Simulator Unit, experiment operating power, and a spare. The spare experiment operating power fuse is provided since this fuse will be blown in testing the experiment's over-voltage protection circuit. The following is a description of the individual experiment control sections.

The Timing Controls section simulates all of the ALSEP digital interface signals. These signals are derived from a crystal controlled oscillator operating as a clock generator. The rates of the digital signals are determined by dividing counters within the unit. Each interface line is variable in amplitude and rise time in order to test operating limits of the SIDE/CCGE experiment. The normal operating position for the Amplitude and rise time switches is 4.0V amplitude and 6 μs rise time. When these switches are in any other position the Abnormal Operation indicator will light.

Four timing function controls are provided on the front panel of the ALSEP Simulator Unit. However, Frame Mark is no longer operational due to design changes in the experiment.

The amplitude, rise time, and rate of the Shift Pulse signal is variable. The normal rate is 1060 bits per second. If the Bit Rate switch is set to either 530 or 10,600 BPS, the Abnormal Operation indicator will light. In addition, in the 10,600 BPS position, the X10 Mode indicator will light on both the ALSEP Simulator Unit and the Data Processor Unit, and the Printer Unit will be inoperative. The X10 Mode of operation is used only to test the experiment under accelerated operating conditions or in order to arrive at a selected SIDE Frame in less time. The data displayed during X10 Mode operation is not valid. A Stop switch is included as an operating function of the X10 Mode indicator. When this switch is actuated the clock generator is turned off and the Timing Controls are not operative. The Shift Pulse controls the rate at which data is shifted into both the experiment and the Data Processor Unit.

All of the Timing Controls and Command Controls are interrelated in that they are derived from the same clock generator. The Data Demand pulse is a dc level change maintained for one word time causing the readout of the experiment data registers. The Even Frame Mark pulse is a short duration pulse used to synchronize the SIDE Frame Counter in the Experiment.

The Command Controls section simulates the five commands from ALSEP to the experiment. The Amplitude and Rise Time controls

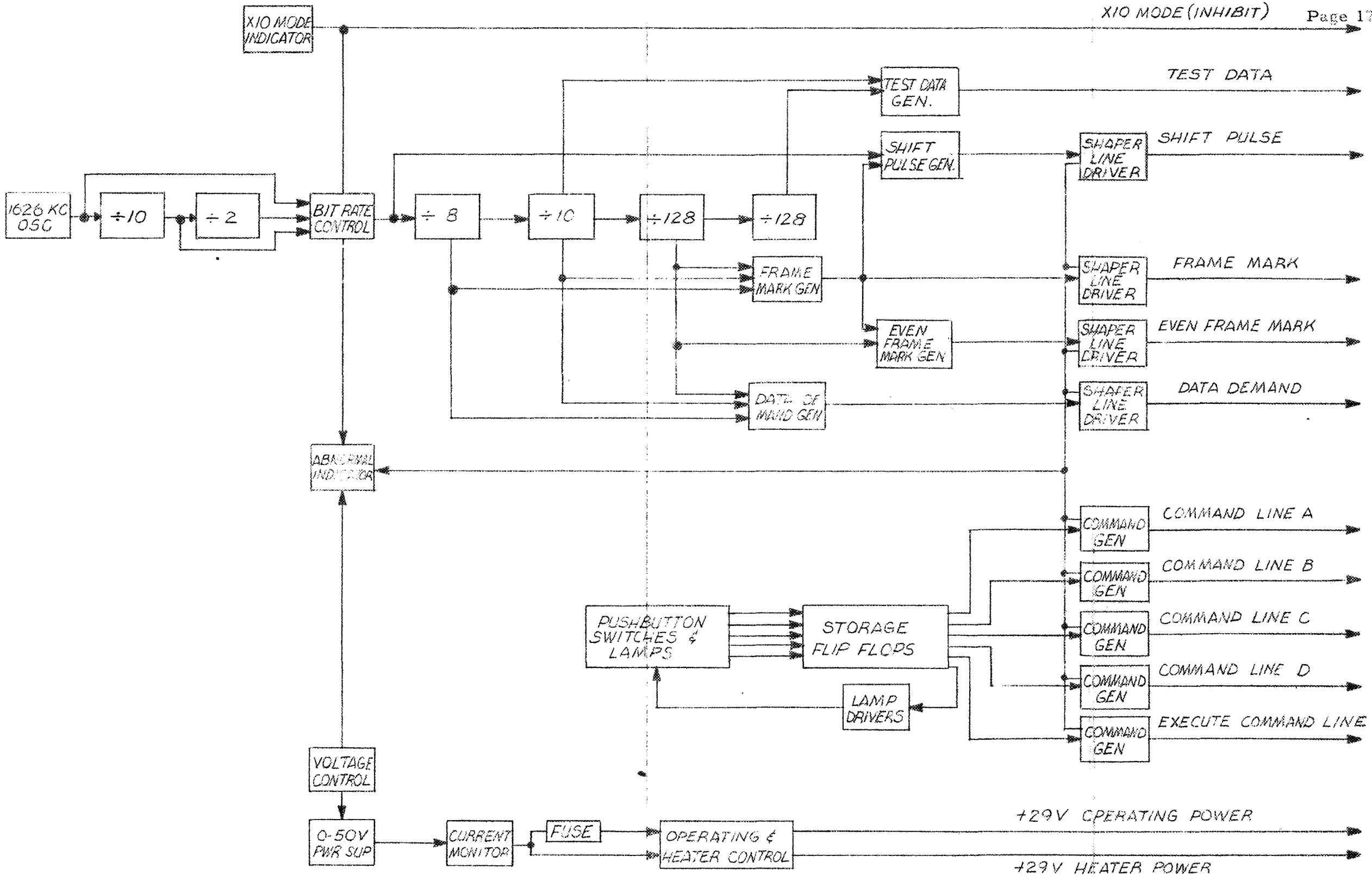


FIG. 6.3-1
BLOCK DIAGRAM
ALSEP SIMULATOR UNIT

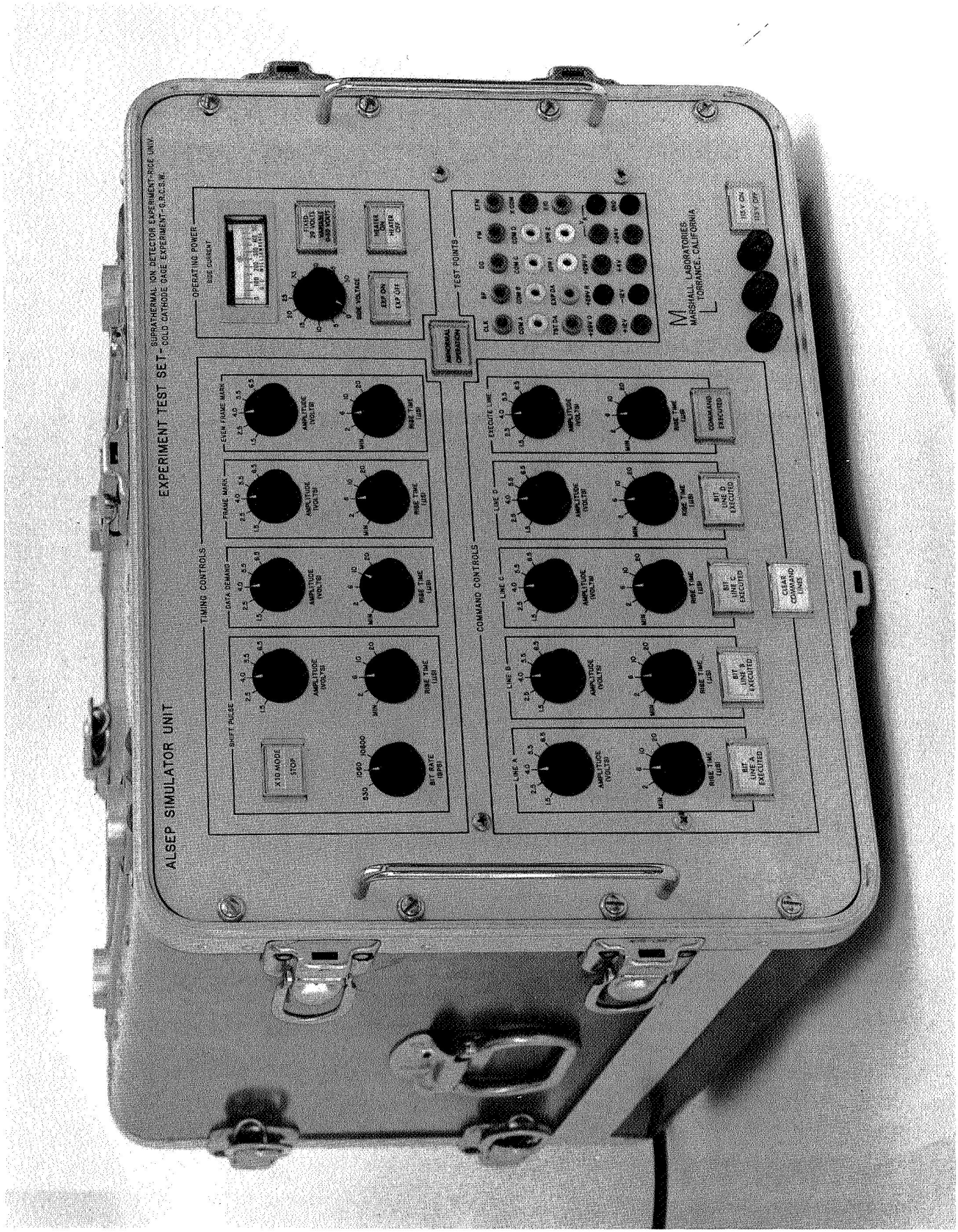


FIGURE 6.3-2 ALSEP SIMULATOR UNIT

operate in the same manner as those in the Timing Controls section. Any deviation from the 4.0V and 6μs settings will cause the Abnormal Operation indicator to light. Each command is set by actuating the lighted switch below the selected command function. Shifting of the commands into the Command Input Register of the experiment is accomplished by operating the Command Executed switch. The five command switches will light when actuated. After actuating the Command Executed switch, the Clear Command Lines switch will light. This switch must be operated before further commands can be sent to the experiment. The rate at which the commands are shifted into the Command Input Register of the experiment is determined by the Bit Rate Switch.

The Operating Power section of the ALSEP Simulator Unit consists of three switches, a variable voltage control and a current meter. Functionally, these components control the operation and output of a 0-50V power supply contained within the unit.

The Fixed 29 Volts/Variable 0-50 Volts switch makes the SIDE Voltage control operative. In the Variable 0-50 Volts position, both the heater voltage and operating voltage are continuously variable. The Abnormal Operation indicator will light whenever this switch is in the variable position.

During normal operation, the Exp On/Exp Off switch provides a fixed +29V to the experiment and also starts the running time meter located on the connector panel of the ALSEP Simulator Unit. The total operating time of the experiment is recorded on this meter.

The Heater On/Heater Off switch provides a fixed +29V to the heaters in the experiment. Normal operation of the experiment is possible with this switch in the OFF position except when the experiment is undergoing environmental testing.

The SIDE Current meter indicates the "total" current being drawn by the experiment from the 0-50V power supply. The meter reading will vary depending upon the positions of the Operating power switches and/or Side Voltage Control

6.4 Monitor Unit

The Monitor Unit provides a means of continuously or selectively monitoring the interface lines between ALSEP and the SIDE/CCGE experiment. Due to design changes in the SIDE/CCGE instrument, only the INTERFACE test points and the switch positions corresponding to the INTERFACE test points are now functional.

The Digital Voltmeter installed in the Monitor Unit can be used independently or as an integral part of the unit. By jumpering

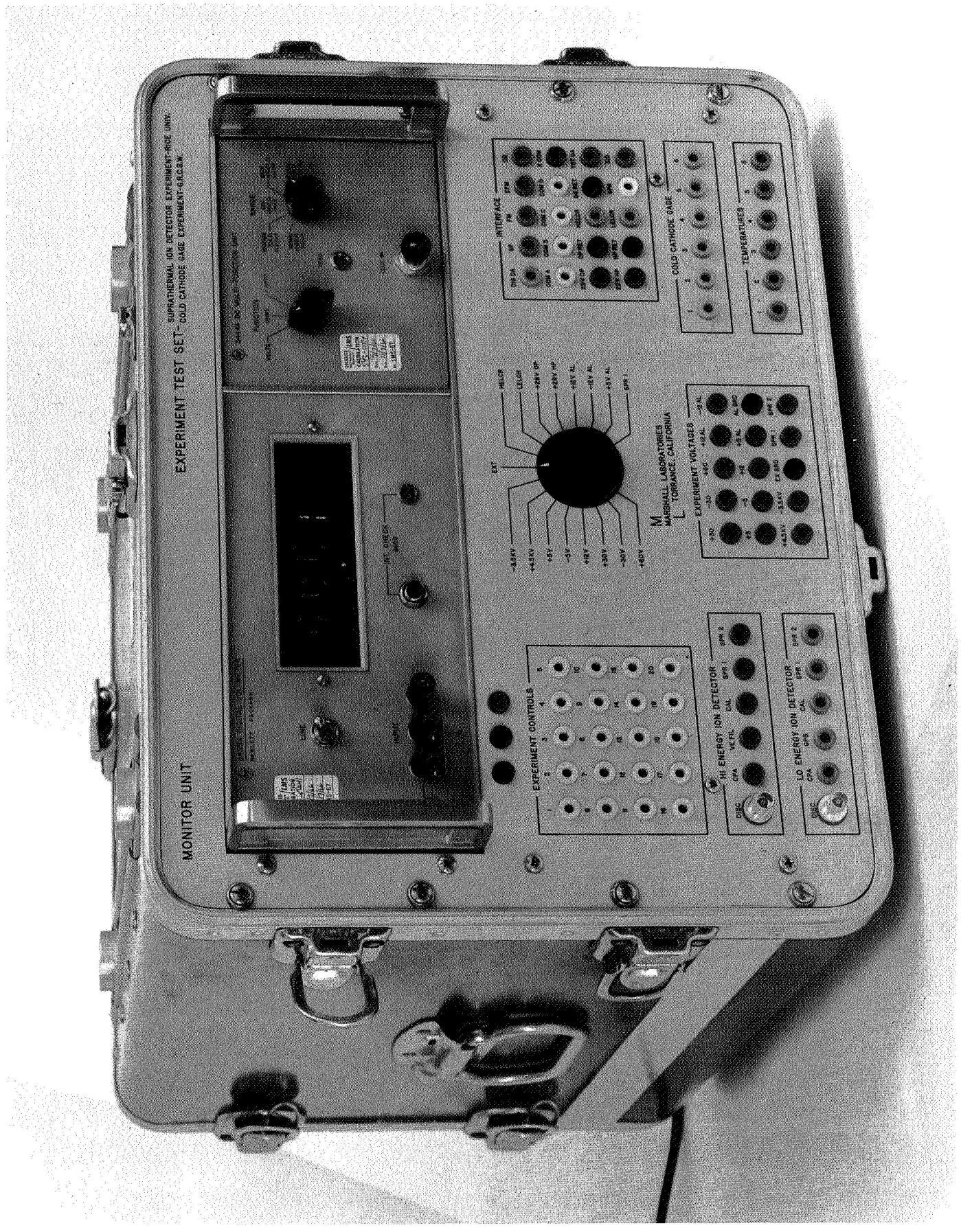


FIGURE 6.4-1 MONITOR UNIT

the input jacks of the DVM to the adjacent test jacks on the Monitor Unit panel, the test points selected by the central switch will be displayed by the DVM. In order to use the DVM independently without disconnecting the jumpers, rotate the central switch to the EXT position.

Interface test points that are not dc functions can be monitored by connecting the oscilloscope or counter directly into the appropriate test jack. These signals are available at the test jacks regardless of the position of the central switch.

For the schematic of the Monitor Unit, see drawing 609669, Figure 6.4-1 which shows a front view of the unit.

6.5 Printer Unit

The Printer Unit is a commercially available Franklin Printer, Model C1220D-8-6B12-SR. The data format for the printer is shown below. See Figure 6.5-1 for a front view of the Printer Unit.

	WORD 9	WORD 10
	WORD 7	WORD 8
	000	WORD 6
	WORD 4	WORD 5
	WORD 2	WORD 3
Cue Dot	. 000	WORD 1

DATA FORMAT - PRINTER TAPE

CAUTION: The Operate/Inhibit switch should always be in the Inhibit position before turning the power switch on.

6.6 Oscilloscope/Counter Unit

The Oscilloscope/Counter Unit contains a commercially available type 422 Tektronix Oscilloscope and a Hewlett-Packard 3734A Counter.

Figure 6.6-1 shows a front view of the Oscilloscope/Counter Unit.

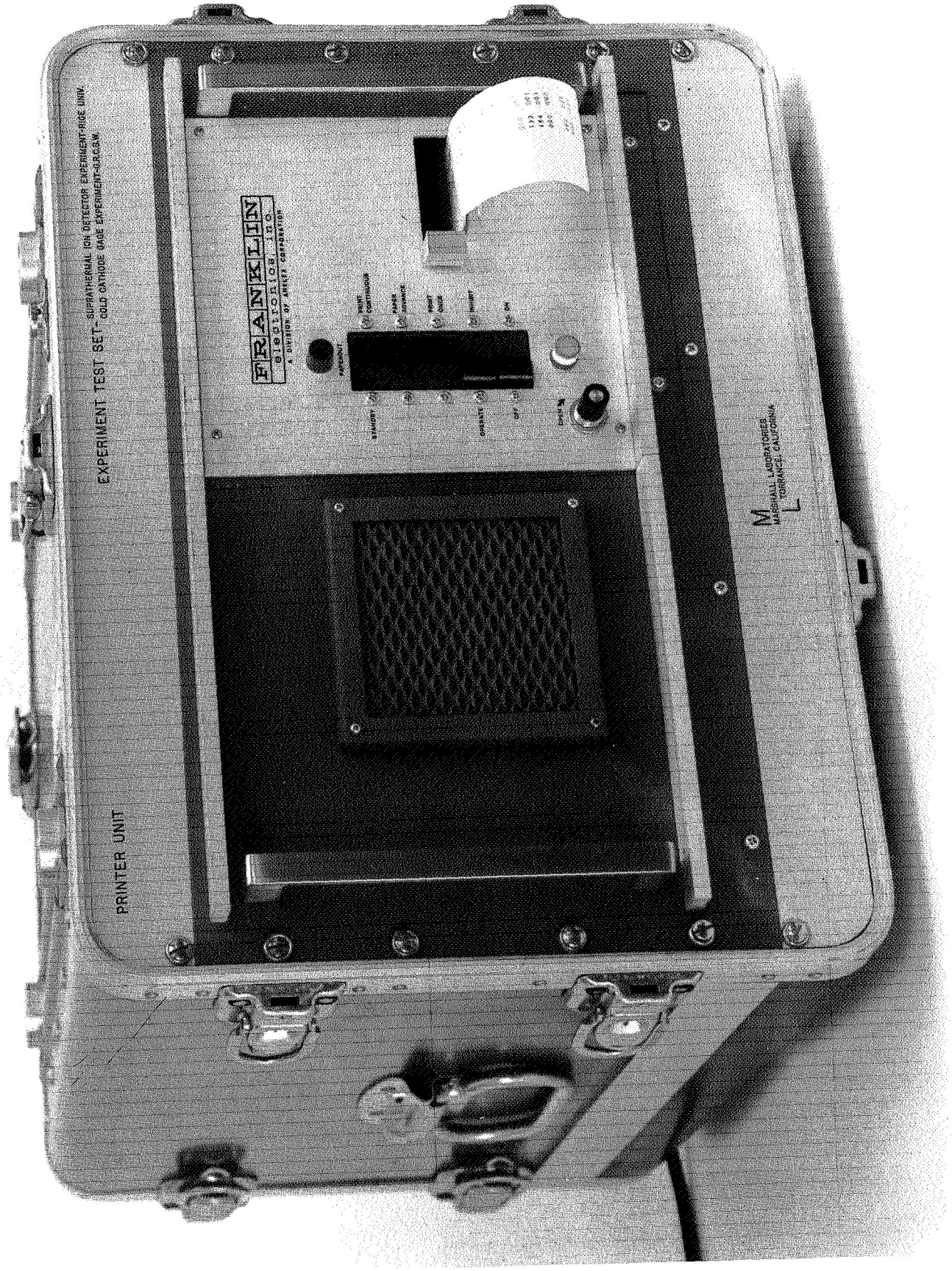


FIGURE 6.5-1 PRINTER UNIT

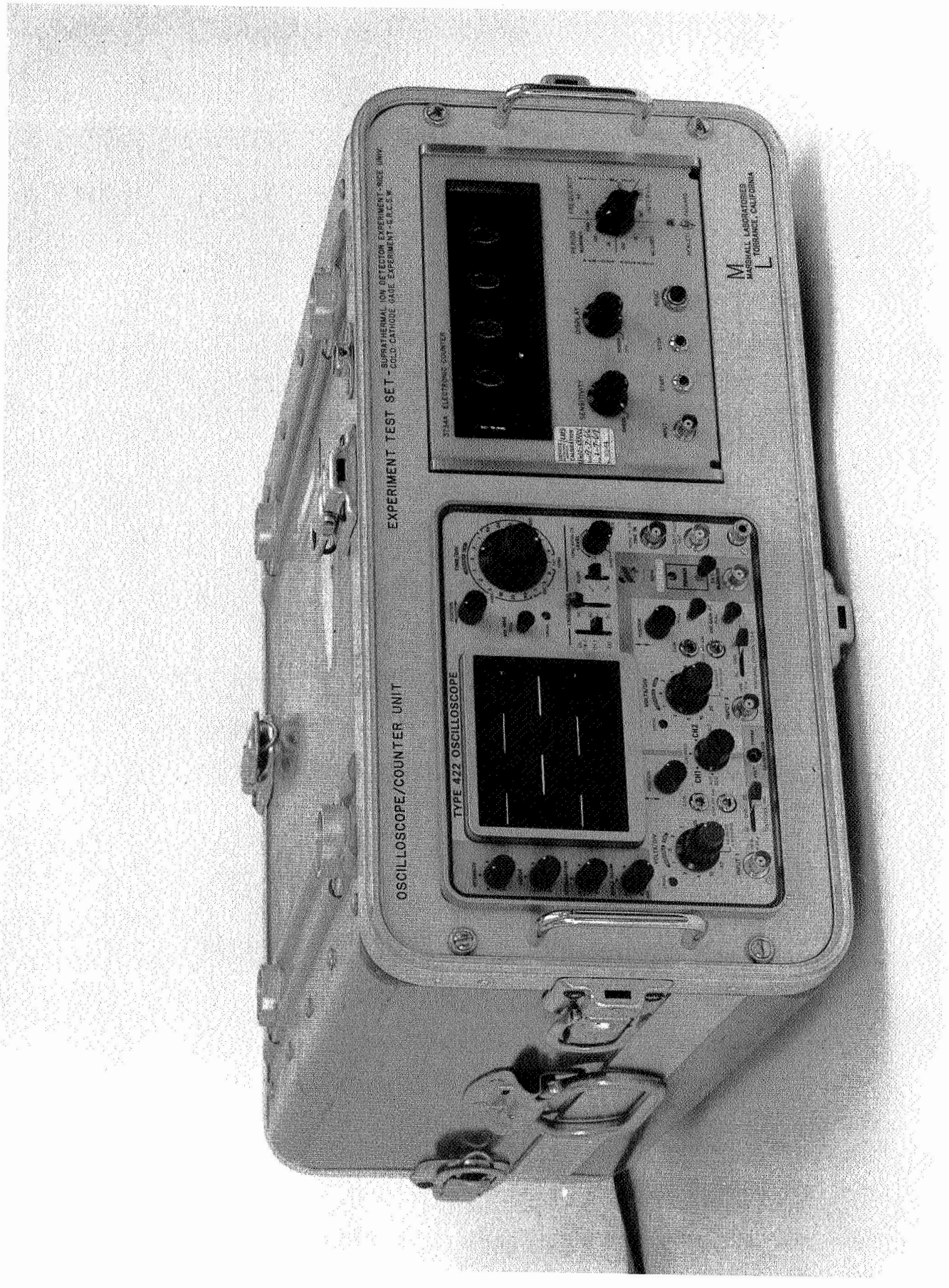


FIGURE 6.6-1 OSCILLOPE/COUNTER UNIT

7.0 MECHANICAL/THERMAL DESIGN

A brief introduction to the ALSEP objectives, associated experiments, and the "SIDE" general features can be seen in Tables 7-A, 7-B and 7-C.

7.1 Basic Mechanical Design Configuration

The Suprathermal Ion Detector Experiment (SIDE), designed to measure the flux, number density, velocity and energy per unit charge of positive ions in the vicinity of the lunar surface, consists of an aluminum parallelepiped electronic package approximately 15" x 12" x 4-1/2" (undeployed configuration) and weighs approximately 20 lbs. (earth weight). See Figures 1.0-1 through 1.0-6. (Appendix D shows special handling instructions.)

A Cold Cathode Gauge Experiment (CCGE) used to determine the lunar ambient density and the rate of loss of contaminants left by the Lunar Module (LM) and Astronauts is separately packaged (by National Research Corporation) and housed in the Suprathermal Ion Detector housing. Data from the SIDE and CCGE Experiments are transmitted by means of a special flat ribbon cable (also physically housed in the SIDE package) to the ALSEP Central Data Station for telemetering to earth. Although several packaging configurations, internal and external, were designed and tested the resulting final configuration shall be discussed herein. The composite SIDE has demonstrated, through various modes of testing, the capability to survive a mock launch, lunar descent, and lunar thermal extremes ($\pm 250^{\circ}$F). Various unique devices are employed in ALSEP/SIDE for its "earth to lunar" excursion. Several mechanical features to be discussed herein are: dust cover, solenoid and latching mechanism, ground screen deployment, tool handling adapter, folding lunar legs, lanyards for dust cover, leg and CCIG deployment, leveling gauge, various special electronic welded modules, and select materials such as thermal paints, epoxies, mirrors, etc.

Special handling instructions are shown in Appendix D.

7.1.1 ALSEP/SIDE/CCGE Deployment on Lunar Surface

See Figures 1.0-1, 1.0-2, 1.0-6 and 1.0-7. The Suprathermal Ion Detector (SIDE/CCGE) is attached to a Pallet subassembly by means of four (4) Boyd Bolt fasteners (provided by customer). The astronaut disengages the fasteners and the instrument with a special cane-like tool. The SIDE is then carried with the astronaut handling tool, engaged in the top plate adapter (on the upper end of this experiment), to an appropriate deployment site. A ground screen secured to the SIDE experiment is then removed and deployed. The ground screen deployment is similar in action to that of the opening of an umbrella. The ground screen will spring open when removed from

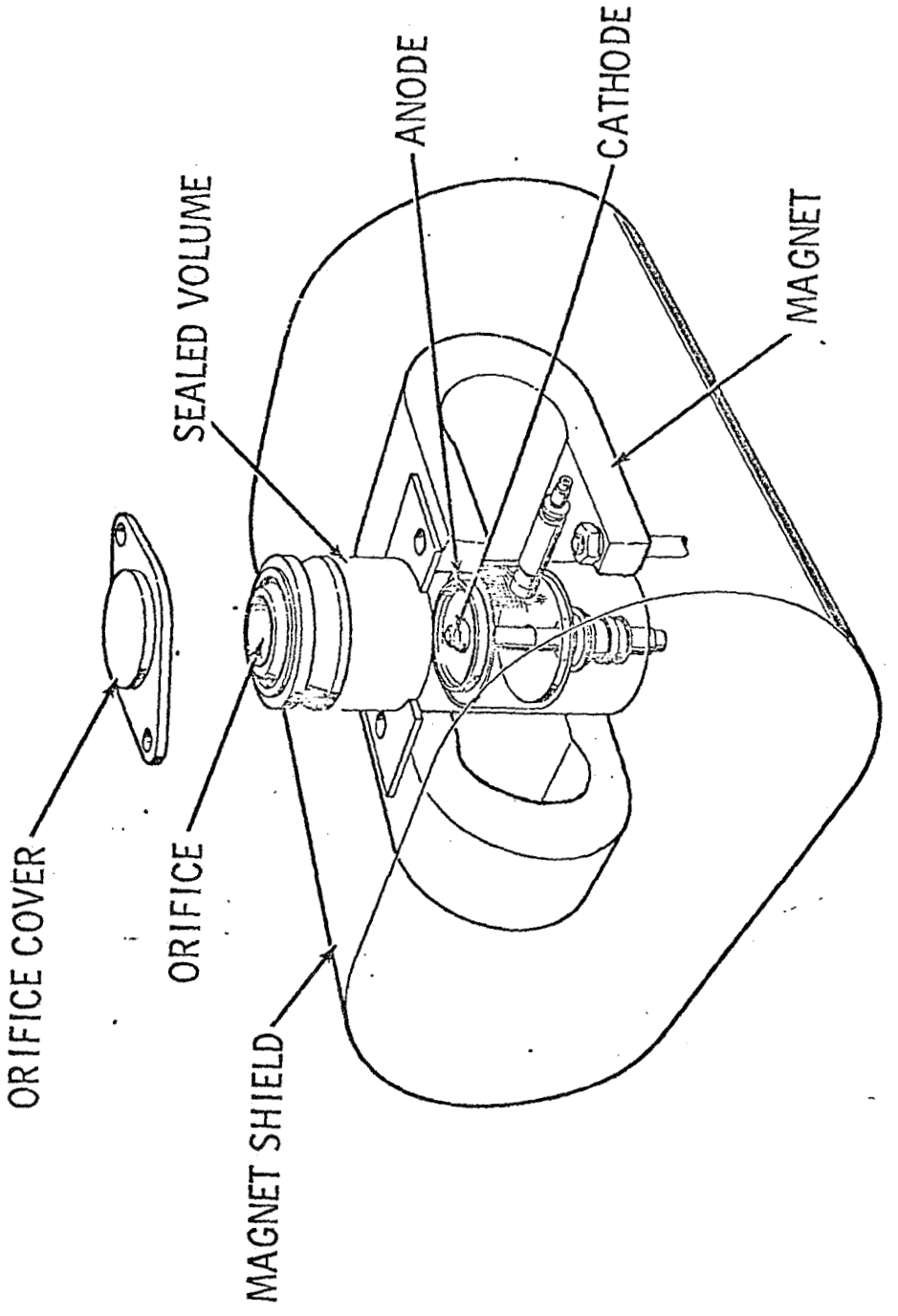

CCIG INSTRUMENT
ORIFICE COVER
ORIFICE
SEALED VOLUME
ANODE
CATHODE
MAGNET
MAGNET SHIELD

FIG 7-1

CABLES, REELS AND CONNECTORS

CONDUCTORS (COPPER)
- WIDTH 0.025 IN. } EQUIV #32 AWG
- THICKNESS 0.002 IN. }
- SPACING 0.050 IN. CENTER TO CENTER
- RESISTANCE:

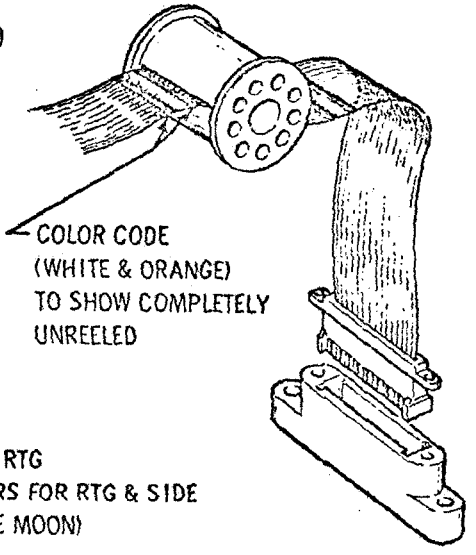
TEMP, °C	OHMS/1000 FT
-175	4.4
20	18.8
125	26.5

- MUTUAL CAPACITANCE: 5 PF/FT

INSULATION ("KAPTON" H-FILM, FEP TEFLON SANDWICH)
- KAPTON: 0.002 IN. THICKNESS (OUTER)
- FEP TEFLON: 0.002 IN. THICKNESS (INNER)
- RESISTANCE: 3×10^6 MEG OHMS/FT

CABLE
- WEIGHT ≈ 0.5 LB/1000 FT/ CONDUCTOR
- ALSEP USES OVER 4000 CONDUCTOR-FT (SAVES 10 LB COMPARED TO ROUND CABLE)
- USES MULTIPLE CONDUCTORS IN PARALLEL FOR HEAVY CURRENTS
- CONNECT EVERY OTHER LEAD FOR SHIELDING

UNREELS IN BOTH DIRECTIONS SIMULTANEOUSLY



COLOR CODE (WHITE & ORANGE) TO SHOW COMPLETELY UNREELED

SPECIAL CABLE FOR RTG
SPECIAL CONNECTORS FOR RTG & SIDE (TO BE MATED ON THE MOON)

DEC 67 5178.3.46

FIGURE 7-7

its carrying tube; it is to be placed on the lunar surface prior to full deployment of the SIDE. The combined leg and dust cover lanyard is then removed to permit the thermal isolation legs (3) to be fully extended and to "arm" the dust cover release solenoid. The package is placed over the ground screen; and the Cold Cathode Ion Gauge (CCIG) cover is then removed by the astronaut. Removal of the CCIG cover exposes the CCIG and its lanyard for deployment. See Figure 7-1.

7.1.2 CCIG (Cold Cathode Ion Gauge) Deployment

The CCIG is rigidly held in a cavity in the SIDE package on two "Holding and Positioning" delrin pins, and clamped in place with a vertically adapted Boyd-type bolt. The connecting cable and releasing lanyard is stowed and held in place by a special spring loaded cover. See assembly procedure for the stowing of cable on lanyard (Appendix D). The astronaut deploys the CCIG by first unlocking the CCIG vertical bolt with a disassembly tool. The CCIG cable cover is then removed by the astronaut by gripping the CCIG cable cover and lifting the cover while moving the bottom section outward. A slight downward motion will then free the cover. With the cover removed, the cable and lanyard are exposed for removal of the CCIG. A pull on the uncoiled lanyard releases the CCIG from the support of the delrin pins. The CCIG slides out on its spring-like nesting slides and is then deployed on the lunar surface beyond the edge of the ground screen (See Table 7A).

7.1.3 Operation of Dust Cover and Solenoid Mechanism

An aluminum dust cover 12" x 4-1/2" x 3/4" is used to protect the entrance apertures and the second surface mirrors from lunar dust caused by the ascent of the LM. The cover is spring-loaded to open by means of an earth command signal. The command signal, when given, energizes an electro-mechanical solenoid and mechanism arrangement. This in turn trips a dust-cover hold down latch, causing the dust cover (single unit) to spring open, thereby exposing the two apertures, a top screen grid, and the second surface mirrors. A solar cell detector senses the sun to provide a signal which indicates that the dust cover operation is completed and the cover has been opened.

7.1.4 Deployment of ALSEP/SIDE Interconnecting Flat Ribbon Cable

The astronaut utilizes a tiedown release tool to release the Boyd-bolt fastener in front of the Bendix cable reel which allows the reel to be ejected from the base of the SIDE package. This makes it accessible for the astronaut to fully remove and deploy.

SIDE EMPLACEMENT CRITERIA

	PARAMETER	REQUIREMENT	PRIORITY	INDICATOR	COMMENTS
DETECTOR	DISTANCE FROM SUBPACKAGE 1	55 ±5 FT	2	60 FT CABLE	TO MINIMIZE INTERFERENCE AT LSM LOCATION
	DIRECTION FROM SUBPACKAGE 1	$110^0 \pm 10^0$ FROM LSM (I.E., $\approx 70^0$ FROM LM)	2	EYEBALL	TO OBTAIN 80 FT SEPARATION FROM LSM & PREFERABLY 100 FT
	SITE SELECTION	SMOOTH	1	EYEBALL	SUITABLE FOR SCREEN
	LEVEL, WITH RESPECT TO INDICATOR	5^0 OF VERTICAL	1	BUBBLE	INTERACTS WITH ALIGNMENT
	ALIGN, WITH RESPECT TO SUN LINE	5^0 OF E-W	2	ARROW*	THERMAL & SCIENTIFIC REQUIREMENT
ION GAUGE	POSITION	OFF SCREEN, OPPOSITE LM, 5 FT FROM DETECTOR	1	5 FT CABLE	TO SATISFY ALIGNMENT REQUIREMENTS
	ALIGN ORIFICE	20^0 OF N OR S	2	PAINT	AWAY FROM ($\pm 90^0$) ALL SUBSYSTEMS, LM, SUN & EARTH
	EXPERIMENT INTERRELATION	HEAVY MAGNET IN ION GAGE IS SHIELDED. IT AND MAGNETIC FIELD OF DETECTOR MUST BE SEPARATED FROM LSM (DIRECTION CRITERIA NOT PERTINENT ON OTHER EXPERIMENT COMBINATIONS)			
	SPECIAL REQUIREMENTS	*ARROW MUST POINT TOWARD SUBEARTH POINT (E OR W); HENCE, EXPERIMENT IS NOT BIDIRECTIONAL. FINAL ALIGNMENT IS BY SHADOWS ON LONG SIDES OF DETECTOR.			

7.1.5 Packaging Design, Inner and Outer Assemblies

- Inner Assembly Design: The inner assembly is constructed of a gold-plated aluminum flat web assembly flanged on the periphery with four thermal insulation hold down bolts. This inner assembly physically supports nine (9) electronic subassemblies of varying dimensions and configurations called Blivets. See Figure 7-3. The inner assembly also contains the low energy and high energy channeltrons and their respective curved-plate analyzers. Several Blivet assemblies are interconnected through a special connector terminal board. The CCIG cable and ALSEP/SIDE interconnect cable which originates in this area is then brought out through a special access opening. When the Inner assembly has been assembled, gold-plated covers are installed to provide a protective and thermal barrier. These covers have mylar liners. Four large 8-1/2 inch long by 1/4 inch threaded fiber glass G-10 bolts provide the thermal isolation and physical tie-down to the exterior housing. The fundamental principle of the thermal design is such that the inner electronics housing is isolated from the outer housing to the maximum degree possible (There are no direct paths - only thermal high-impedance connections).

- External Housing Design: The external housing is a welded aluminum shell, approximately 15" x 12" x 4-1/2", designed to house: 1) the inner electronic assembly; 2) the Cold Cathode Ion Gauge; 3) the ALSEP/SIDE inter-connecting cable reel. The inner surface of the exterior housing is gold plated to provide the "Dewar"(Thermos Bottle) effect. The collapsible ground screen is mounted on the exterior surface of the external housing for accessibility. A thermal spacer assembly with the gold-plated apertures, secondary surface mirrors, and dust cover are assembled to the top of the external housing. Other accessories added to the over-all external assembly are: top screen grid, bubble level, carrying tool adapter, earth-direction arrow, CCIG and lanyard assembly, collapsible legs and lanyard, thermal base blanket and name plate. The exterior is painted with S13-G (Appendix H) thermal paint. The leveling (bubble) gauge is provided in order to permit the astronaut to align the experiment within five degree tolerance level with the lunar surface.

7.1.6 ALSEP/SIDE Collapsible Leg Design and Deployment

The ALSEP/SIDE package, when fully deployed, rests on three outstretched legs and foot pads made of G-10 fibre glass material. The legs are spring-loaded and fold beneath the external housing where they are retained by means of

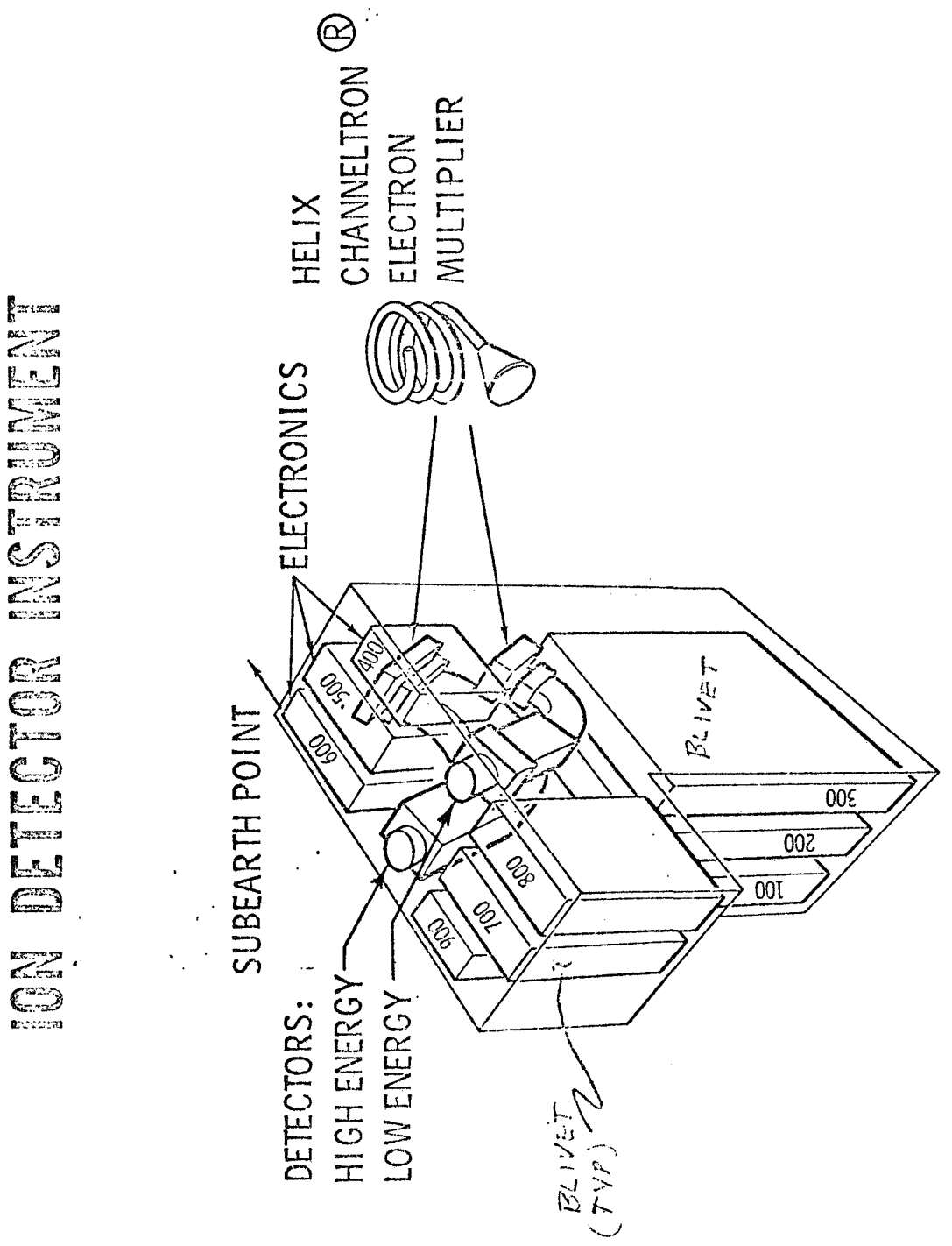

ION DETECTOR INSTRUMENT
HELIX
CHANNELTRON ®
ELECTRON
MULTIPLIER
ELECTRONICS
SUBEARTH POINT
DETECTORS:
HIGH ENERGY
LOW ENERGY
BLIVET
(TYP)
BLIVET
300
200
100
800
700
900
500
600
400

FIGURE 7.2

a pull pin and lanyard arrangement. The legs are foam filled and reinforced at the foot pad end by Castall 301 bonding material and by special collars and pins at the upper pivotal end. The top end is pivoted within a magnesium yolk on a steel pin (See Figure 7-4). Legs are painted white with 3M paint.

7.1.7 Sine and Random Vibration Tests

Extensive sine vibration tests were conducted at AETL (Advanced Engineering Test Labs Facility) on a mechanical ALSEP /SIDE simulator to establish a high confidence level of the structural design. Tests were conducted in the acceptance and qualification test levels in both random and sine vibration modes. The levels of testing were established in accordance with Bendix interface specifications. These tests resulted in the highlighting and subsequent correction of several areas of weakness.

Additional tests were performed at AETL for all the flight high-voltage blivets (700 + 900) to further ensure a higher physical margin of safety. See typical test data and reports in Appendix A.

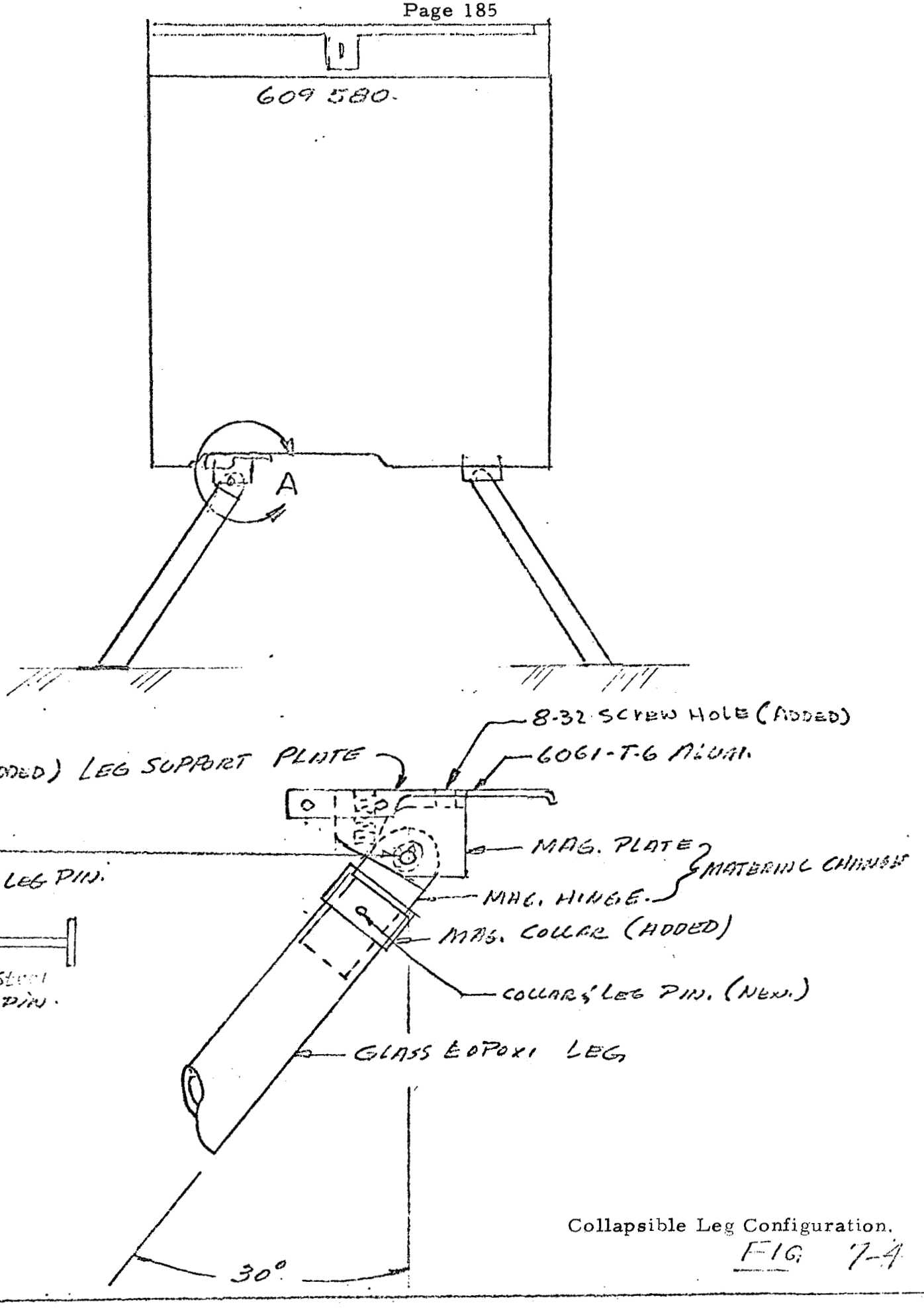
7.1.8 Ground Screen Design and Deployment

The Ground Screen (see Assembly drawing 609439, Appendix C) consists of aluminum rods and one steel rod (1/8" diameter) forming the ribs of an umbrella approximately 26 inches in diameter. These rods or ribs are held in a circular pattern by a thin steel braided wire making 8 rows or webs. At the center of this pattern is a spring-loaded hub which mechanically deploys the Ground Screen from a closed umbrella position to that of a flat, circular pattern. An extractor or astronaut tool adapter is pinned to the tip of the steel rod to provide a means for the astronaut to extract the Ground Screen from its encasement tube. See deployment procedures in Appendix D.

7.1.9 Electronic Packaging Welded Module and Blivet Assembly

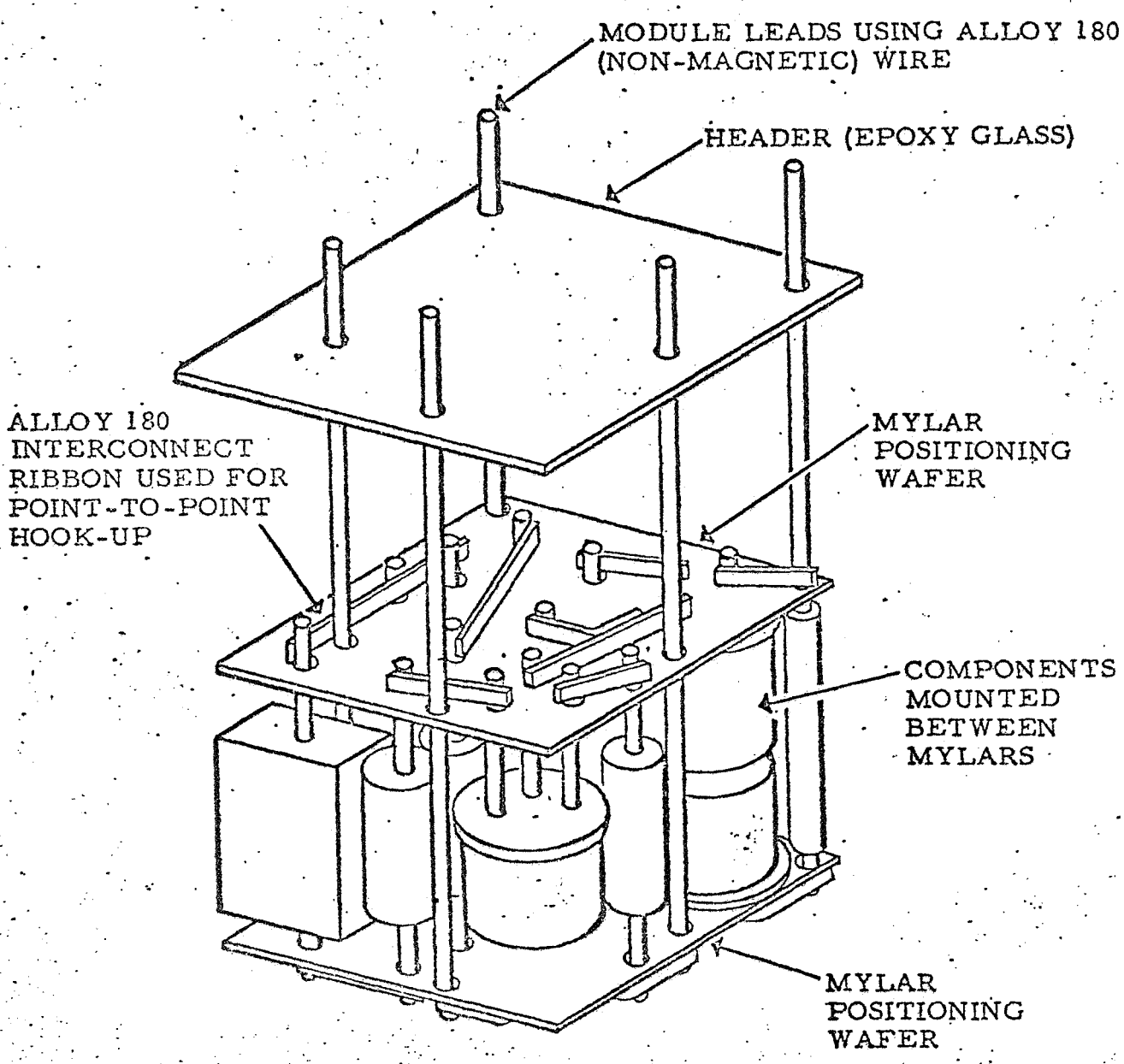
The electronic packaging design is based upon the cordwood welded module concept in order to achieve the required packaging density within the volume available. Discrete components are positioned between mylar positioning wafers and welded with wire ribbon as shown in Figure 7-5 (typical). Welded modules containing integrated circuit flat-packs are shown in Figures 7-6 and 7-7 (typical).

The modules are welded together to form an electronic subassembly, called a blivet, by means of epoxy glass positioning boards, mylar matrix, epoxy glass hook-up boards and interconnecting weld ribbon. See Figure 7-8 for a typical assembly. Nine (9) blivets



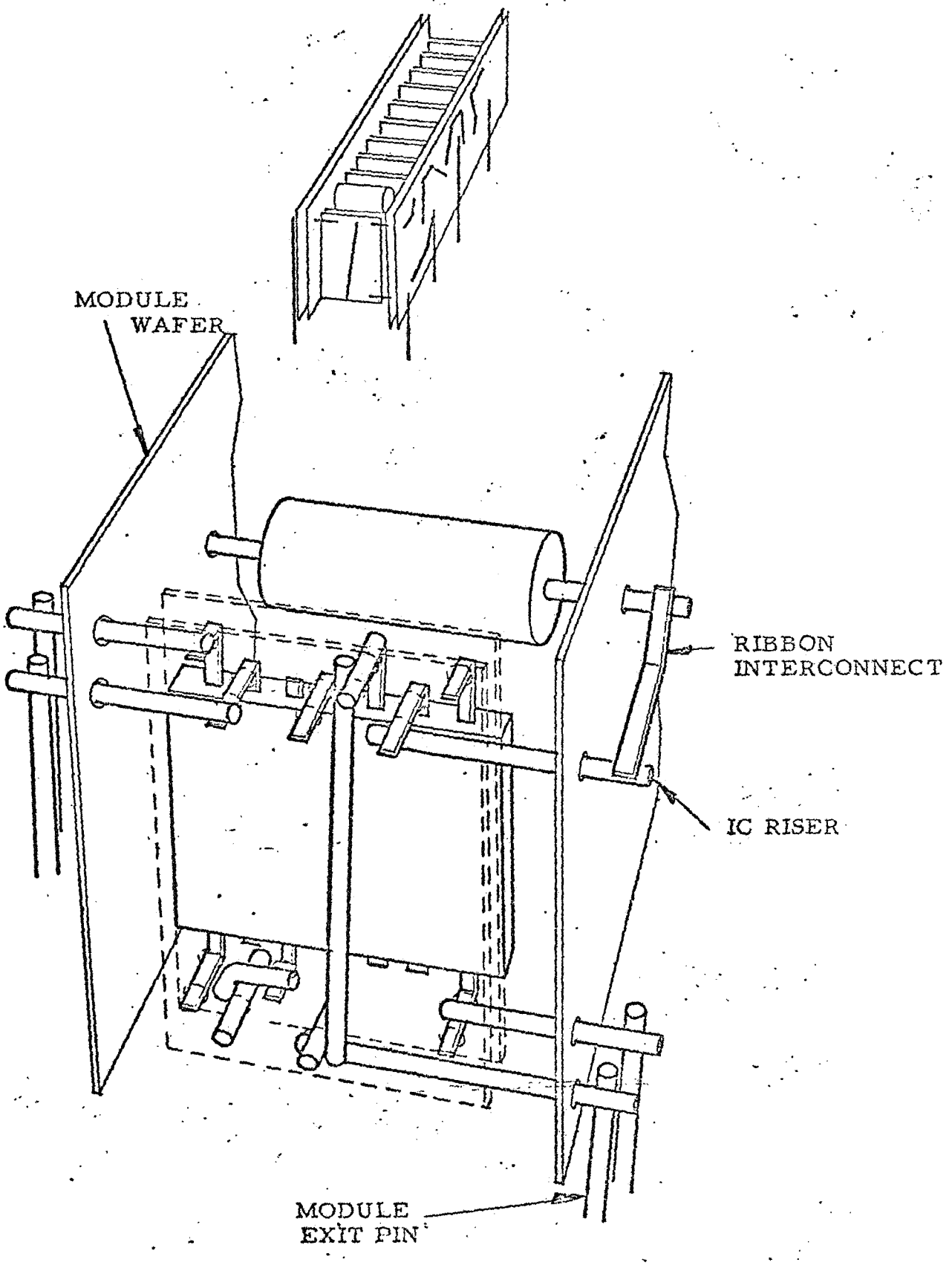
Collapsible Leg Configuration.

FIG. 7-4



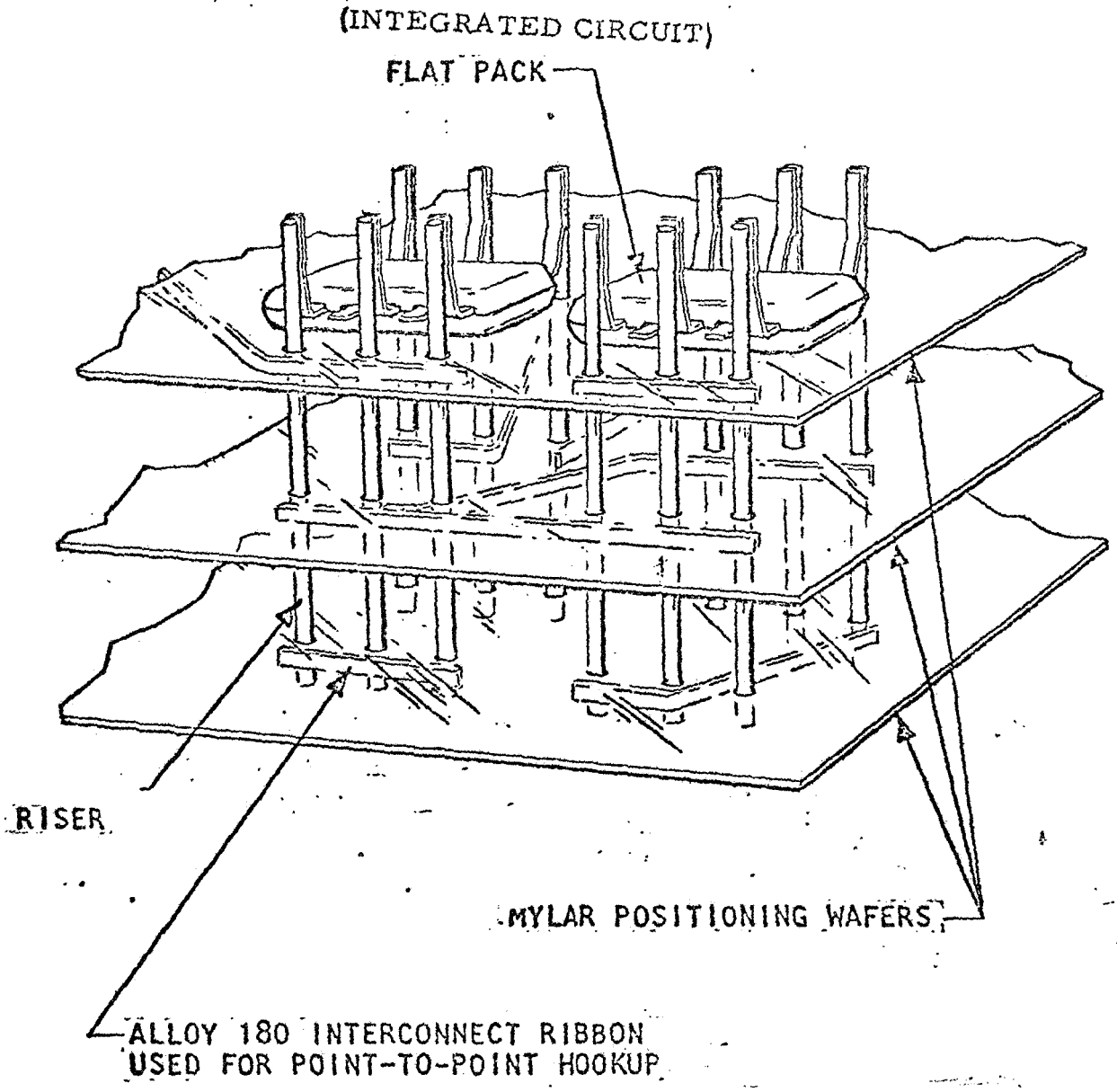
Module, Discrete (Typical)

FIGURE 7-5



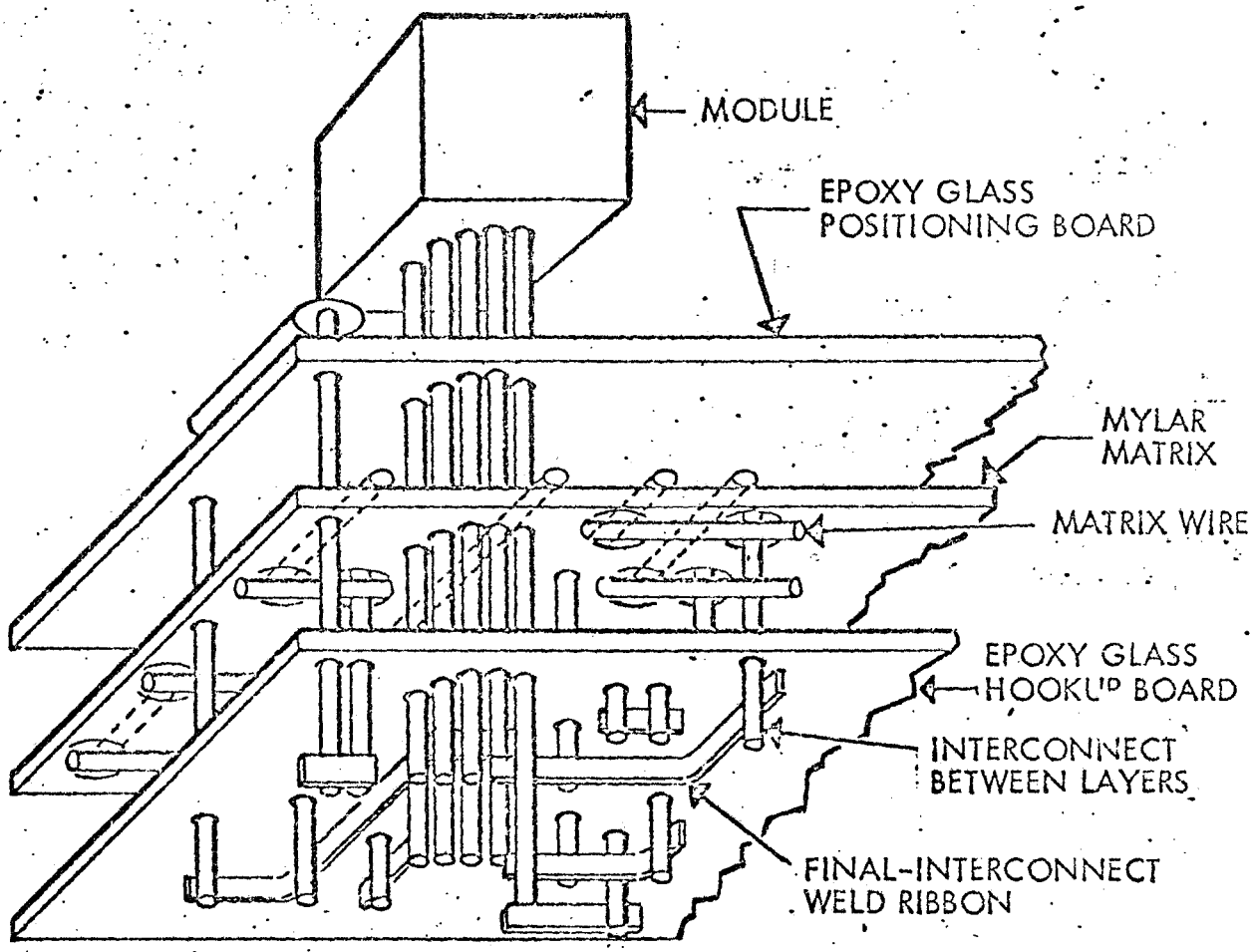
Package - Riser Weld (Typical)

Fig. 7-6



Flatpack Interconnection (Typical)

FIG 7



MODULE INTERCONNECT MATRIX (Typical)

FIG 7-8

are required for the ALSEP/SIDE assembly. The relative locations and positions of these Blivets in the inner housing assembly are shown in Figure 7-3. Blivet 100 assembly with its respective hookup and positioning board drawings is somewhat typical of the basic blivet concept and is shown in Appendix C - drawings 609519, 609520, and 609521.

7.1.10 Channeltron Mechanical Configuration (High Energy and Low Energy)

The channeltron type used in the ALSEP/SIDE package is shown in Figure 7-9, Reference Table 7B. The channeltron is potted in a specially designed potting cup with Castall 301. This subassembly is then assembled and sylgard potted into its respective welded module. Copper shielding and hook-up leads are then installed to complete the channeltron assembly, Low Energy or High Energy. The relative position and location of the channeltrons can be seen in Figure 7-3.

7.1.11 ALSEP/SIDE/CCGE Qualifications Vibration

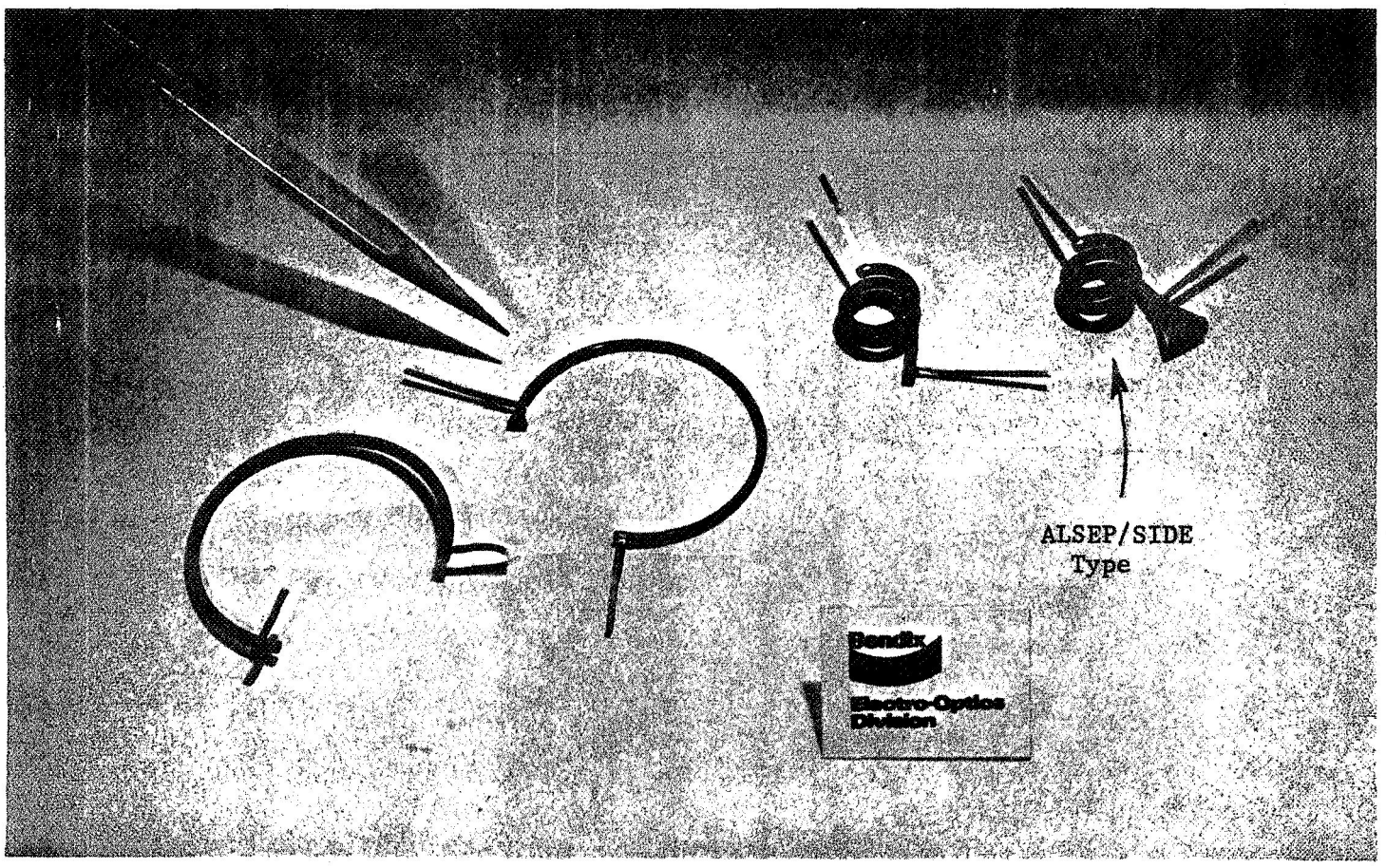
The ALSEP/SIDE/CCGE systems 2 and 4 were extensively tested at Bendix on Pallet 2 for the full sine and random vibration requirements. Although a pallet and side mounting support failed on S/N 2 (believed due to excessive "g" load; see attached letter dated 6 November, 1967 in Appendix A), the four SIDE mounting supports were subsequently redesigned and successfully re-tested. See Appendix A for pertinent test data correspondence and test requirements related to Bendix testing.

7.1.12 Special Studies and Calculations

Special studies or calculations relating to the mechanical/thermal consideration of the ALSEP/SIDE Package are tabulated below:

Item	Description	Remarks
A	Stress analysis, ALSEP legs, new design.	Appendix F
B	Outgassing rate of inner package assembly.	Appendix F
C	Solenoid testing.	Appendix F
D	Thermal expansion calculation, dust cover.	Appendix F

CHANNELTRON® ELECTRON MULTIPLIERS



MODELS: CEM-4010, CEM-4013, CEM-4020, CEM-4028

ALSEP/SIDE
Type

FIGURE 7-9

Bendix

SPECIFICATIONS

CHANNELTRON® ELECTRON MULTIPLIERS

ALSEP/SIDE

CHARACTERISTIC	MODEL			
	4010	4013	4020	4028
MECHANICAL:				
SHAPE	CIRCULAR	CIRCULAR	HELIX	HELIX
SUBTENDED ARC	270°	270°	840°	840°
CONE DIAMETER*	None	3mm	None	8mm
CONE ANGLE	—	45°	—	45°
CHANNEL I.D.	0.040"	0.040"	0.040"	0.040"
CHANNEL O.D.	0.080"	0.080"	0.080"	0.080"
RADIUS OF CURVATURE	0.85"	0.85"	0.24"	0.24"
ELECTRICAL:				
SPECTRAL RESPONSE	1500 Å to below 2 Å			
MINIMUM GAIN	5×10^7 with 3000 vdc applied			
OUTPUT PULSE HEIGHT DISTRIBUTION	Full width half maximum 50%			
OUTPUT CURRENT PULSE WIDTH	20 nanoseconds (nominal) at 5×10^7 gain			
BACKGROUND COUNT RATE** (avg) at 3000 vdc	< 0.5/sec	< 1.5/sec	< 0.5/sec	< 4.0/sec
DYNODE SURFACE RESISTANCE	$1 \times 10^9 \Omega$	$1 \times 10^9 \Omega$	$1 \times 10^9 \Omega$	$1 \times 10^9 \Omega$
MAX. OPERATING PRESSURE	1×10^{-4} Torr	1×10^{-4} Torr	1×10^{-4} Torr	1×10^{-4} Torr
MAX. OPERATING VOLTAGE	4 kv	4 kv	4 kv	4 kv
MAX. DC ANODE CURRENT FOR LINEAR ANALOG RESPONSE	10% OF BIAS CURRENT SEE NOTE 2	10% OF BIAS CURRENT SEE NOTE 2	10% OF BIAS CURRENT SEE NOTE 2	10% OF BIAS CURRENT SEE NOTE 2

NOTE: 1. ALL SPECIFICATIONS ARE NOMINAL UNLESS OTHERWISE NOTED.

2. BIAS CURRENT IS EQUAL TO THE OPERATING VOLTAGE DIVIDED BY THE DYNODE SURFACE RESISTANCE.

* MODEL CEM-4010 WITH 10MM CONE AVAILABLE AS CEM-4019. MODEL CEM 4020 WITH 10MM AXIAL CONE AVAILABLE AS CEM 4039

**<4.0/SEC FOR MODELS CEM-4019 & CEM-4039

TABLE 7-B

E	Mirror inspection criteria	ML Memo dated 16 May 1968
F	Solar cell acceptance criteria	ML Memo dated 22 May 1968
G	Dust cover study	Appendix F
H	Thermal paint meeting and notes	ML Memo dated 8 May 1968
I	Dust cover paint evaluation	Appendix F
J.	Stress and deflection calculation of external housing	Appendix F
K	Channeltron stress report, Sylgard encapsulate	Appendix F
L	Bubble-level; design and test evaluation at Wyle Labs	ML Memo dated 12 June 1967

7.1.13 ALSEP/SIDE/CCGE Material List and Miscellaneous Vendor Literature

Various materials utilized in the ALSEP/SIDE are listed in Appendix H. These materials were selected initially from the ALSEP program approved lists and added materials were submitted and approved during the course of the program.

7.1.14 ALSEP/SIDE/CCGE Assembly Plans

An assembly plan typical of the complex fabrication procedures required for the ALSEP/SIDE Package is shown in Appendix E (Chassis Assembly Plan AP609512).

7.1.15 Master Drawing List

The Master Drawing List (MDL) is a complete listing of all Marshall Laboratories' drawings relating to each ALSEP/SIDE/CCGE System. All configuration variations such as part number additions, deletions, or revisions are so noted in the MDL. Typical MDL's are MDL 609770-102, ML323-6 and up (Appendix II) and the flight spare number 2 (spare parts list) ML323-9.

7.1.16 Interface and Top Assembly Drawings

The interface drawing P/N 609778 (Appendix C) depicts the mechanical parameters determined during the various

stages of test, development and fabrication of the Bendix pallet, the Marshall Laboratories SIDE package, and the NCR CCIG unit. This drawing establishes the latest SIDE configuration at this time.

The final assembly drawing P/N 609770-102 covers the overall mechanical features of the ALSEP/SIDE package such as the geometry, special instructions, notes, supporting drawings, and partial material lists.

7.1.17 Special Tools and Fixtures

Special tools and fixtures, both simple and complex, were extensively used throughout the fabrication of the ALSEP/SIDE package. Various fixtures for the potting of blivets, potting of channeltrons, alignment fixtures for the curved plate analyzers, as well as special housing fabrication tools were developed in the course of the ALSEP/SIDE/CCGE development.

The alignment fixtures developed for the high energy and low energy detectors, P/N T-609277 and P/N 609279 (Appendix G) respectively, are typical of the varied and complex tools required in the ALSEP/SIDE fabrication operations.

7.1.18 Cleaning Materials

Several cleaning materials are available for cleaning operation of mirrors, gold surfaces, and painted surfaces. Materials are listed below:

- Alcohol - Methyl
- Freon - TF (Pure)
- Freon - TP-35+ (Isopropyl Alcohol)
- Freon - TE-35+ (Ethyl Alcohol)
- BonAmi + Distilled Water

The following are recommended cleaning materials to be used with respective surfaces. Note: all cleaning materials are to be applied with clean, soft cloth for ease of application and minimum residue.

SURFACE	CLEANING FLUID
White Painted Surface	
o 3M Paint	Freon TP-35, Apply very lightly
o S13G Paint	Use BonAmi plus distilled water
Mirrors	Use methyl alcohol with soft cloth
Gold Plated Surfaces	
o Metal (Deposit - Electro)	Freon TP-35
o Lexan Vacuum-Deposits	Freon TP-35; Caution: Very light rubbing permitted only.
Gold Tape	Freon TF - Pure

7.2 Thermal Design

7.2.1 Thermal Simulator

Extensive thermal design studies and tests have provided a system capable of withstanding the lunar thermal environment designated in Bendix specifications. (See Tables 7C and 7D.) A thermal mechanical simulator was fabricated with actual ALSEP/SIDE housing, legs, secondary surface mirrors, thermal legs, thermal spacer, thermal paint, simulated internal masses and electronic equivalent heaters. Thermocouples were placed throughout the SIDE package to obtain an accurate temperature profile during the simulated lunar day and night tests. See Thermal Simulator Wiring Diagram SK609992 (Appendix B).

The thermal simulator has demonstrated its capability to maintain the temperature of the internal electronics at -40°C to $+80^{\circ}$C during a simulated lunar day temperature of $+120^{\circ}$C and a lunar night temperature of -157°C. See Appendix B.

7.2.2 ALSEP/SIDE/CCGE Thermal Design Features

The following is a list of the final built-in thermal design features employed to withstand the lunar thermal extremes.

ALSS System Environments

Environment Considered	Storage Unpackaged	Storage Packaged (Applied to Package)	Movement to the Pad	Factory & Assembly Bldg. Checkout	Launch Pad Environment	Flight	Lunar Operations
Humidity	15 to 50% relative	N/A	15 to 100% relative	Max 50%	Max 50%	N/A	N/A
Sand and Dust	N/A	N/A	N/A	N/A	N/A	N/A	*
E.M.I.	N/A	N/A	N/A	LM Std	LM Std.	N/A	3.2.5 herein
Acceleration	1.0 g Vert. preferred axis	2.67 g Vert. with 1 g lateral	1.0 g Vert.	N/A	N/A	5 g's -**	N/A
Vibration	N/A	*	*	N/A	N/A	3.1.2.2.1.1 and 3.1.2.2.1.2 herein	N/A
Shock	*	*	*	N/A	N/A	3.1.2.2.3 herein **	N/A
Temperature	-20° to +110°F	-65°F to 160°F	-20° to +110°F	+50°F to +100°F	+50°F to 100°F	0°F to 160°F	*
Radiation	N/A	N/A	N/A	Negligible	Negligible	Less than lunar opn *	*
Solar Radiation	360 BTU/ft^{2}hr. 6 hr/day	N/A	N/A	N/A	N/A	N/A	*
Meteoroids	N/A	N/A	N/A	N/A	N/A	N/A	Document DS-21
Pressure	Ambient	Sea level to 50,000 ft	Ambient	Ambient	Ambient	<1 x 10^{-8} m.m. Hg	*
Acoustics	N/A	N/A	N/A	N/A	N/A	*	N/A

* Document LSD 520-12

** - Refer to paragraph 3.1.2.2.3 for qualification test levels.
(BENDIX REPORT JC 31405)

PLSS/SPACE SUIT SYSTEM ENVIRONMENT TABLE IC

Page 196

TABLE IC

ALSEP/SIDE/CCAE ENVIRONMENTAL DUTY CYCLE

TABLE 7D

Environment Considered	Storage Unpackaged	Storage Packaged	Movement to Pad	Factory & KSC Checkout	Launch Pad Environment	Flight	Lunar Operations
Humidity	3 Days	90 Days	1 Day	180 Days	13 Days	N/A	N/A
Acceleration	N/A	N/A	N/A	N/A	N/A	Approx. 25 min*	N/A
Vibration	N/A	1 Day	1 Day	N/A	N/A	25 min*	N/A
Shock	Single Shock	Single Shock	N/A	N/A	N/A	One Shock	N/A
Temperature	3 Days	90 Days	1 Day	180 Days	13 Days	3.5 Days	182 days hi 183 days lov
Radiation	N/A	N/A	N/A	Negligible	Negligible	3.5 Days	365 Days
Solar Radiation	6 hr/day 3 Days	N/A	N/A	N/A	N/A	N/A	182 Days
Meteoroids	N/A	N/A	N/A	N/A	N/A	N/A	365 Days
Pressure	90 Days	90 Days	1 Day	180 Days	13 Days	3.5 Days	365 Days
Acoustics	N/A	N/A	N/A	N/A	N/A	5 Min	N/A

*Includes lunar descent.

Environmental Duty Cycles

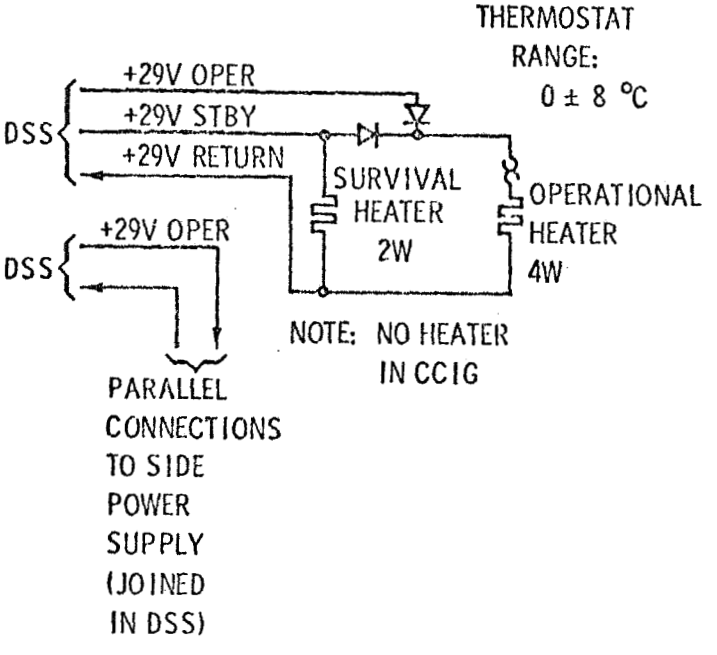
TABLE 7D

ALSEP/SIDE THERMAL DESIGN FEATURES

Item	General Description	Remarks
1	Thermal Survival Heater	See Figure 7-10
2	Second Surface Mirrors	See Appendix B
3	Inner housing assembly with external gold-plated covers suspended within external housing facing gold plated inner housing walls - air gap and thermal support bolts provided.	The Dewar (Thermos Bottle) Principle is applied here. (See Figure 7-11, ALSEP/SIDE/CCGE Internal Assembly).
4	Thermal Space Assembly (Top section of inner and outer assembly)	Supports thermal mirrors and thermally isolates inner and outer housing by means of plastic bumper screws (Reference drawing 609770).
5	Thermal (S-13G) paint	This paint is applied to exterior housing surface, (Specification S-43012) provides thermal control with minimum degradation due to solar radiation.
6	Aluminized mylar and silk mesh thermal blanket on bottom exterior of case.	This blanket is placed on bottom of external housing between the three thermal insulation legs.
7	G10 fiber-glass base on external housing.	Reduces thermal leakage path from external housing to inner housing.
8	Thermal isolation legs; support and isolation of lunar surface from ALSEP/SIDE package.	G-10 fiber-glass provides low thermal leakage path.

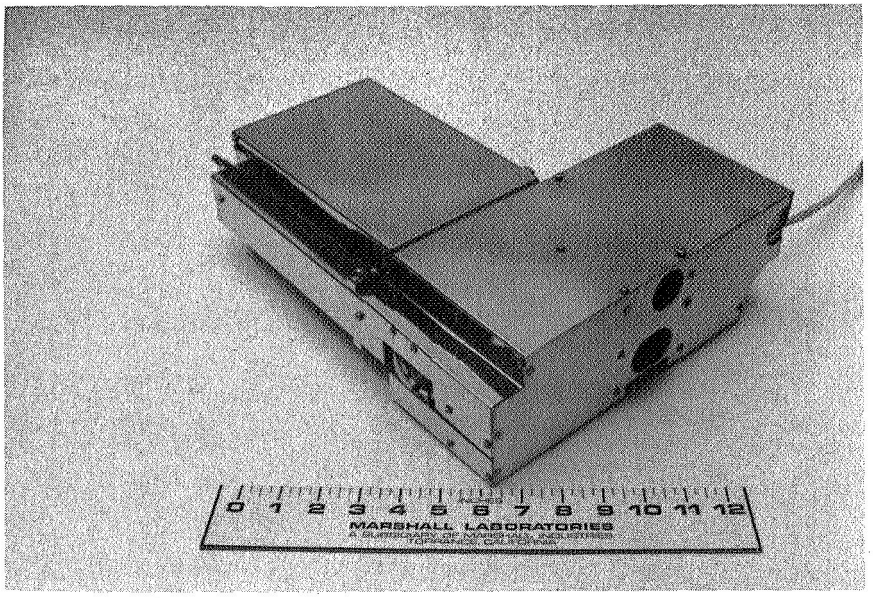
SIDE THERMAL CONTROL

ELECTRICAL

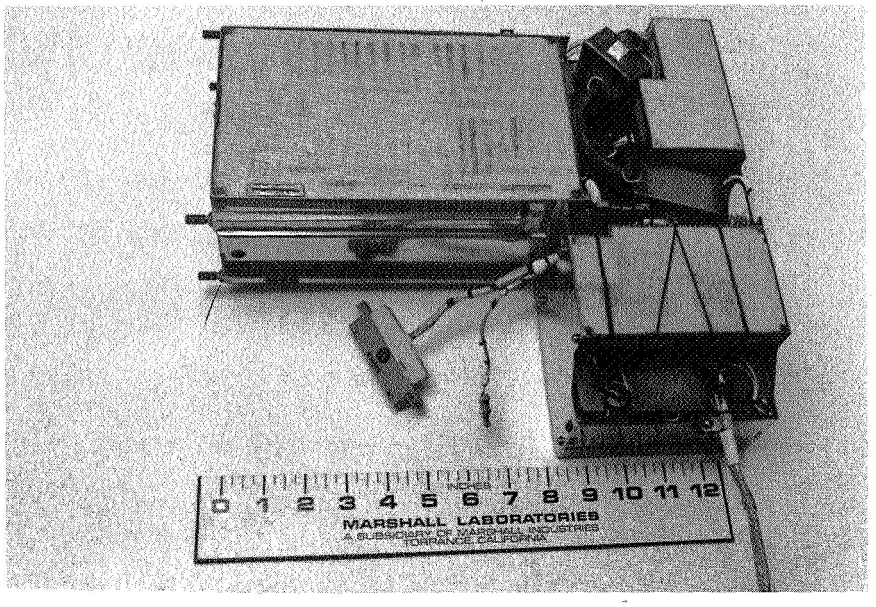


(See Section 5.1.10 for more detailed description.)

FIGURE 7-10



a) Gold-Plated Cover in Place



b) Gold Cover Removed

FIGURE 7-11 ALSEP/SIDE/CCGE INTERNAL ASSEMBLY

7.2.3 Summary of Thermal Studies and Tests Performed (See also Appendix B)

Item	Report No.	Description
a	M/L Technical Note 1500.94 (13 January 1967)	Test Report, Thermal Simulator ALSEP/SIDE.
b	Aerotherm Report No. 67-14 (10 July, 1967)	Thermal Design of ALSEP/SIDE, Early Design and Redesign.
c	Aerotherm Report No. 67-17 (25 August, 1967)	Lunar environmental simulation testing of ALSEP/SIDE simulator.
d	Aerotherm Report No. 67-22 (16 October, 1967)	Lunar night simulation tests.
e	Test specification for S/N 6 dust cover and solenoid - June 1967	Lunar night dust cover and solenoid evaluation, S/N 6 Test Specification.
f	NASA Report 44-07-24 (23 August, 1967)	ALSEP/SIDE Thermal model test (For lunar day environment).
g	Correspondence from Aerotherm (30 April 1968)	SIDE ThermalPerturbation due to holes in Inner Radiation Shield.
h	Marshall Labs Thermal Leg Considerations (12/19/67)	Thermal considerations with new leg support design.
i	Bendix Letter 9713-09-407 (20May 1968)	Bendix Thermal/Vacuum Test Analysis "SIDE" Experiment.
j	Aerotherm Ref. P.O. No. 24883 (30 April 1968)	SIDE Thermal Perturbation due to holes in the Inner Radiation Shield.

7.3 Astronaut Training Unit

The Astronaut Training Unit (ATU) is identical to the flight models in the areas of outer envelope structure, mounting configuration, weight (Lunar and Earth) and center of gravity. Lunar and Earth weights are achieved by removal or installation of a special lead weight.

The interior of the ATU is empty except for the special weight. The dust cover, identical in appearance to that of the flight units, is nonoperable.

Astronaut training requirements influenced the development and modification of various features of the ATU. Among the modifications that led to the final unit were the detent, cradle and strap for ground screen support, the lockout plug, earth arrow marking, and simulated thermal blanket. See Figure 7-12 for the assembly drawing of the ATU.

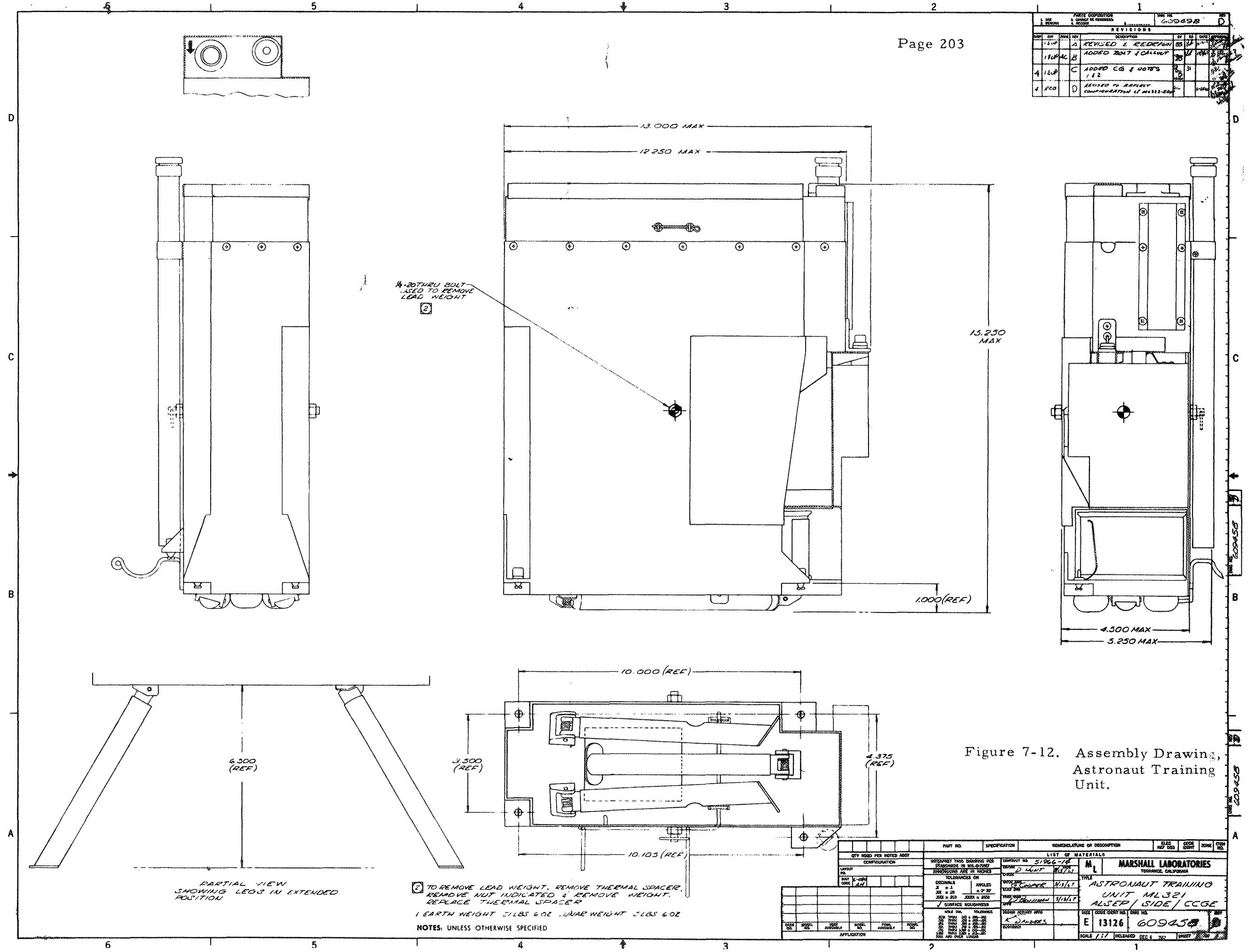


Figure 7-12. Assembly Drawing, Astronaut Training Unit.

8.0 NEW TECHNOLOGY

Reporting Organization: Time-Zero Corporation, Torrance, California. Contract Number: S1966-14.

8.1 Thermal Design Techniques, ALSEP/SIDE/CCGE Mechanical Structure

I Title of Disclosure

Thermal Design Techniques, ALSEP/SIDE/CCGE Mechanical Structure

II Abstract

Substantial Thermal Design activity resulted in an instrument capable of withstanding extreme lunar thermal environments, ranging from +120°C to -157°C, ambient. Internal temperatures are maintained between +80°C and -40°C. This accomplishment was achieved through relatively sophisticated thermal control coatings, second-surface mirrors, a special thermal blanket, utilization of the Dewar principle, and other techniques.

III Description

a) General Purpose: See item II

b) Improvements and/or advantages: See item (c)

c) Various techniques were used which advanced the art of thermal design. Among these are special treatments of surfaces of the SIDE/CCGE instrument. A summary of studies and investigations made on various surface treatment techniques follows:

Low α/ϵ (ratio of thermal absorption to emittance)

1. Second Surface Mirror (SSM). The SSM probably has the lowest α and lowest ratio α/ϵ of all available coating systems. It also exhibits negligible ultra-violet (u.v.) degradation, at least for the SIDE application. According to References 9, 10, and 11, ground and flight (Orbiting Solar Observatory) data on 1" x 1" squares or 1" diameter discs demonstrate that $\alpha = 0.05$ and $\epsilon = 0.78$ have been reliably achieved. SSM's are commercially available (e.g., Optical Coatings Laboratory Incorporated, Santa Rosa, California, per Reference 12).

2. White Paints. The solar absorption of white paints has repeatedly been demonstrated to degrade from exposure to u.v. radiation; e.g., see Reference 4. The Illinois Institute of Technology

Research Institute (IITRI), among other organizations, has been developing white paints with reduced susceptibility to u.v. degradation.

a. Z-93 (IITRI Coating). Based on References 13, 14, and 15, this is the best white paint from the standpoint of low α/ϵ and low u.v. degradation. Experience has demonstrated, however, that Z-93 is difficult to apply, requires a high cure temperature (at least 270°F), and is brittle after application.

Properties, obtained from Reference 14, for a new coating are:

$0.13 \leq \alpha \leq 0.18$

$0.79 \leq \epsilon \leq 0.92$

for $75^{\circ} \geq \theta \geq 0^{\circ}$

where θ = angle between normal to surface and direction of radiation

$\epsilon_{\text{Hemispherical}} = 0.88$

b. S-13G (IITRI Coating). Based on Reference 15, this is the coating recommended for use on the SIDE wherever white paint is required. S-13G does not exhibit thermal properties as favorable as those of Z-93; however, S-13G is easy to apply and does not require a high-temperature cure.

Properties, from Reference 15, are:

$\alpha_{\text{New Coating}} \approx 0.2$; $\alpha_{\text{after 1000 sun-hours of u.v. radiation}} \approx 0.3$

c. NASA Goddard Coating No. 9. Properties, from Reference 15, are:

$\alpha_{\text{New Coating}} \approx 0.22$; $\alpha_{\text{after 1000 sun-hours of u.v. radiation}} \lesssim 0.37$

d. Dow Corning White, No. Q-92-007. Properties, from Reference 15, are:

$\alpha_{\text{New Coating}} \approx 0.22$; $\alpha_{\text{after 1000 sun-hours of u.v. radiation}} \lesssim 0.37$

e. 3-M Velvet Coating No. 202-A10 White. This is the coating originally planned for the complete exterior of the SIDE. Based on TRW measurements and Reference 15 the performance of this coating is similar to that of Dow Corning Q-92-007.

$\alpha/\epsilon \leq 1$ and Low ϵ

1. Silica, SiO_2, ($\sim$ 3000 Å thick) over silver ($\sim$ 2000 Å thick) over aluminum. This coating is discussed in Reference 9, and can apparently exhibit $\alpha \approx \epsilon \approx 0.1$. An inherent problem with this coating system is guaranteeing that SiO_2 is used and not SiO (or SiO_x), because SiO is rapidly degraded by u.v. radiation. For example, data quoted in Reference 13 for a similar coating system employing SiO indicate that α increased from 0.16 to 0.25 after 96 sun-hours exposure to u.v. radiation. O.C.L.I. (based on Reference 12) can apply silica, silver and aluminum directly to the SIDE or to appropriate sheets, in the thickness desired; verification of coating resistance to u.v. radiation is advisable.

2. Boeing Barrier Anodize Coating. According to the discussions of Reference 10, the Boeing Company has developed a special anodizing process for aluminum. Available properties are $\alpha \approx 0.1$ and $0.05 < \epsilon < 0.5$, depending on the thickness of the anodized layer. Hardware must first be coated with a layer of pure aluminum. Based on the information obtained from References 10 and 16 the coating exhibits very good resistance to u.v. radiation.

3. Sand-Blasted Aluminum Alloy. $\alpha \approx \epsilon \approx 0.15$ can be achieved but α is very sensitive to the degree of sandblast, based on the discussions of Reference 10. Surface contamination is a potential problem with this surface because it is porous and difficult to clean.

4. Mosaic Pattern of Second Surface Mirror and Specular Aluminum. On the basis of analyses performed, it appears that $\alpha \approx \epsilon \approx 0.15$ can be readily achieved if approximately 10 percent of the surface is covered with SSM's and the remaining 90 percent with vacuum deposited aluminum. In this case, reasonable properties of the aluminum are $\alpha \approx 0.12$ and $\epsilon \approx 0.03$. With such a system it is important to assure that adhesive used to attach the SSM's does not outgas and contaminate the surfaces. Also, if the aluminum is applied by adhesive, gas escape holes should be incorporated. This basic system was proposed during the conversation of Reference 10.

5. Mosaic Pattern of Second Surface Mirror and Specular Gold. This system is basically the same as No. 4. Here, reasonable properties for the gold are $\alpha \approx 0.25$ and $\epsilon \approx 0.03$.

6. Mosaic Pattern of White Paint and Aluminum or Gold. This system is the same in principle as those of Nos. 4 and 5. With about 20 percent of the surface covered by white paint (degraded by roughly 2000 sun-hours of u.v.) and 80 percent covered by aluminum or gold, $\alpha \approx \epsilon \approx 0.25$ can be obtained. The advantage of this system is its relative ease of application compared to Nos. 4 and 5.

7. Mosaic Front Surface Aluminized Kapton. Such a coating system is available from the Schjeldahl Company and is currently designated G102000-3; according to Reference 13 the properties are $\alpha \approx 0.20$ and $\epsilon \approx 0.15$. Schjeldahl is developing a process for controlling the amount of aluminum in order to achieve $\alpha \approx \epsilon \approx 0.15$ for a specific TRW application. Based on References 13 and 17 the level of u.v. degradation for this type of coating system is minimal. Approximately 90 percent of the exposed surface of this system is vapor-deposited aluminum and 10 percent is Kapton.

Coating Numbers 1, 2, 3 and 7, above, are regarded to be in the developmental stage so far as usage on the SIDE is concerned.

Very Low ϵ

1. Specular Aluminum or Gold, Vacuum Deposited Directly on SIDE Hardware. Discussions of References 10, 13, and 18 indicate that when aluminum or gold is vacuum deposited on polished surfaces $\epsilon \approx 0.03$ is readily achievable (neglecting corners, holes, etc.). Also, both materials have adequate atmospheric oxidation resistance.

2. Specular Aluminum or Gold Tape. Several commercial products are available. One is Pressure Sensitive Gold Reflective Tape No. Y-9184, Minnesota Mining and Manufacturing Company.

S-13G paint was selected for use on the SIDE outer package. The 3M Velvet was also used, to a lesser extent, on the dust cover. Further details on thermal design can be found in Appendix B.

Following is a summary of SIDE/CCGE thermal design features:

SIDE/CCGE THERMAL DESIGN FEATURES

Item	General Description	Remarks
1.	Thermal Survival Heater	See Figure 7-10
2.	Second Surface Mirrors	See Appendix B

SIDE/CCGE THERMAL DESIGN FEATURES (Cont.)

Item	General Description	Remarks
3.	Inner housing assembly with external gold plated covers suspended within external housing facing gold plated inner housing walls - air gap and thermal support bolts provided.	See Drawing 609770. The Dewar (Thermos Bottle) Principle is applied here.
4.	Thermal Space Assembly (Top Section of inner and outer assembly).	Supports thermal mirrors and thermally isolates inner and outer housing by means of plastic bumper screws. See Drawing 609770.
5.	Thermal (S-13G) paint	This paint is applied to exterior housing surface, (Specification S-43012) provides thermal control with minimum degradation due to solar radiation.
6.	Aluminized mylar and silk mesh thermal blanket on bottom of case.	This blanket is placed on bottom of external housing between the three thermal insulation legs.
7.	G10 fiber glass base on external housing.	Reduces thermal leakage path from external housing to inner housing.
8.	Thermal isolation legs; support and isolation of luner surface from ALSEP/ SIDE package.	G10 fiber glass provides low thermal leakage path

NOTES REGARDING ATTACHMENT OF SECOND SURFACE MIRRORS TO STRUCTURAL SUBSTRATES

1. Range of expected top plate temperatures for operating Suprathermal Ion Detector Experiment:

   (300°R to 600°R) = (-160°F to $+140^{\circ}$F) = (-106°C to $+60^{\circ}$C)

2. Adhesive between second surface mirrors and substrate should be sufficiently flexible to allow for differential coefficient of thermal expansion. This problem is reduced by using small mirrors.

3. For thermal reasons it is advantageous that the adhesive between second surface mirrors and substrate be white, if the adhesive is visible in the gaps between adjacent mirrors.

4. A controlled gap should be incorporated between adjacent mirrors. The gap width during mirror installation process should be such that adjacent mirrors will not touch one another over the entire top plate operational temperature range as well as the adhesive cure cycle temperature range.

5. All materials (adhesives, paints, etc.) should be outgassed and second surface mirrors carefully cleaned prior to delivery of each instrument.

6. The following companies are known to have experience in the use of second surface mirrors: LMSC, Boeing, TRW, Hughes, and Aerojet.

NOTES

1. Standard size of second surface mirrors produced by OCLI is: Length = 1 inch; Width = 1 inch. Other sizes can also be produced.

2. OCLI recommends that quartz be cut to final size prior to deposition of coating system. Second surface mirrors can be cut by scribing the quartz and breaking the mirror but this procedure weakens the bond between coating system and quartz.

3. Corning commercial grade number 7940 fused silica is the recommended substrate for the coating system.

4. The coating system (silver under inconel) is designated OCLI SI-IDD Solar Reflector coating.

Features believed to be new: Design approach and application.

Does the contractor intend to file a patent application? No

IV Applications

Military and aerospace thermal control

V Degree of Development

Development completed.

VI Technological Significance

Major Improvement

REFERENCES

1. "Thermal Analysis of Top Plate and Grid at Lunar Noon with Dust Covers Open, ALSEP/SIDE/CCGE", February 6, 1967. (Marshall Laboratories Informal Engineering Report)

2. "Thermal Analyses, ALSEP/SIDE/CCGE Top Plate and Grid, Lunar Noon, Dust Cover Open", Rev. 1, February 17, 1967, and April 10, 1967. (Marshall Laboratories Informal Engineering Reports)

3. "Results of Qualification Testing on 3-M Velvet Coating No. 020-A1) White", April 12, 1967. (Marshall Laboratories Informal Engineering Report)

4. "Ultraviolet Stability of Some White Thermal Control Coatings Characterized in Vacuum", by P. Blair, Jr., G. Pezdirtz, and R. Jewell, AIAA Paper No. 67-345.

5. "Test Report, Thermal Simulator for ALSEP/SIDE/CCGE Program Technical Note 1500.94, Marshall Laboratories, Prepared for Rice University, Contract No. S1966-14.

6. "Analysis of Temperature Distribution and Radiant Heat Transfer Along a Rectangular Line of Constant Thichness", by S. Lieblein, NASA TN D-196.

7. "Performance of Multilayer Insulation Systems for the 300° to 800°K Temperature Range, Materials Report No. 1", Contract NAS 2-2441, 4-05-65-9, August 1965, Lockheed Missiles & Space Co., Palo Alto.

8. "Performance of Multilayer Insulation Systems for the 300° to 800°K Temperature Range, Materials Report No. 2", Contract NAS 2-2441, 4-05-65-9, March, 1967 Lockheed Missiles and Space Co., Palo Alto.

9. S. Greenberg, D. Vance, E. Streed, "Low Solar Absorptance Surfaces with Controlled Emittance: A Second Generation of Thermal Control Coatings, AiAA Paper No. 67-343, AIAA Thermophysics Specialist Conference, New Orleans, La., April 17-20, 1967.

10. Telephone communications: S. Greenberg (Lockheed Missiles and Space Co., Palo Alto, Calif.) and K. Reseck (Aerotherm Corp.) regarding thermal control coatings, on May 10, 18, 1967.

11. Telephone communication: E. Streed (NASA Ames Research Center, Mountain View, Calif.) and K. Reseck (Aerotherm Corp.) regarding thermal control coatings, on May 5, 1967.

12. Telephone communications and trip to OCLI: V. Yen (optical Coatings Laboratory, Inc.) and K. Reseck (Aerotherm Corp.) regarding thermal coatings, on May 5, 9, 10, 12, 15, 16, 1967.

13. Telephone Conference: E. Luedke (TRW Systems, El Segundo, Calif.), J. Smith (NASA, Manned Spacecraft Center, Houston, Texas), and K. Reseck (Aerotherm Corp.) regarding thermal control coatings, May 24, 1967.

14. Telephone communication: J. Smith (NASA, Manned Spacecraft Center, Houston, Texas) and K. Reseck (Aerotherm Corp.) regarding thermal control coatings, May 26, 1967.

15. Telephone communication: E. Luedke (TRW Systems, El Segundo, California) and K. Reseck (Aerotherm Corp.) regarding thermal control coatings, June 8, 1967.

16. W.F. Carrell, "Coatings Development and Environmental Effects", Jet Propulsion Laboratory Internal Report, no date.

17. "Measurements Report: Evaluation of Unidirectional Thermal Radiation Properties of Materials, Thompson Ramo Woolridge Report for contract number NAS 9-5073, May 1967.

18. Telephone communication: Mr. Kopel (Vacuum Metalizing Co., Van Nuys, Calif.) and K. Reseck (Aerotherm Corp.) regarding thermal control coatings.

19. Final Report No. 67-14, "Thermal Design of ALSEP Suprathermal Ion Detector Experiment - Evaluation of Early-Design Adequacy and Summary of Analytical Redesign Effort" - K. G. Reseck.

8.2 Design of High-Speed, Maximum Stability Charge-Sensitive Amplifier

I Title of Disclosure

Design of High-Speed, Maximum Stability Charge-Sensitive Amplifier. (General Purpose - See Item II below)

II Description

a. The purpose of the charge-sensitive preamplifier is to amplify and shape the output pulses from the detectors with the least addition of noise, and with maximum stability.

b. Improvements - the circuit represents a noticeable improvement in the design of a charge-sensitive amplifier possessing maximum stability and high-speed.

c. The following is a simplified description to illustrate how the basic feed-back technique produces a highly stable charge-sensitive preamplifier.

What is commonly referred to as "charge sensitive preamplifier," is an operational amplifier with both capacitive and resistive feedback, as shown in Figures 8.2-1 and 8.2-2.

A charge sensitive amplifier was designed for the following characteristics:

- Low Noise Figure
- Minimal Stray Capacitance Effect
- Higher Gain Stability
- Minimal Output dc Drift
- Better Temperature Stability
- Circuit Simplicity and Higher Reliability

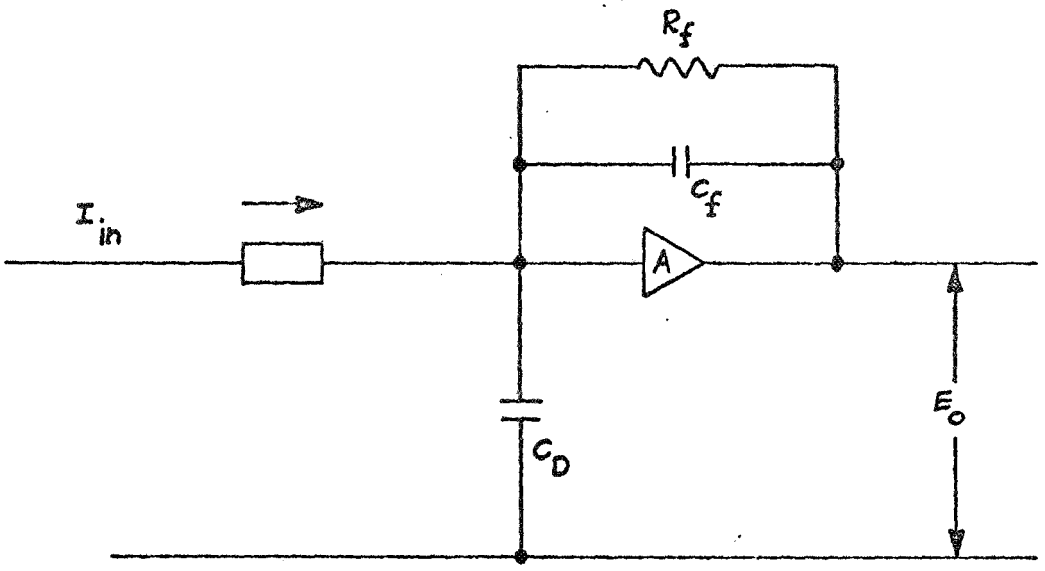


FIGURE 8.2-1, CHARGE SENSITIVE PREAMP BLOCK DIAGRAM

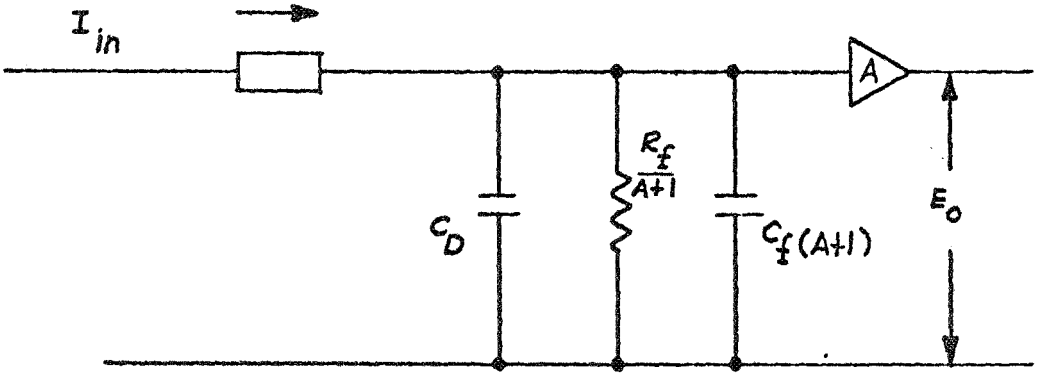


FIGURE 8.2-2, PREAMP EQUIPMENT CIRCUIT

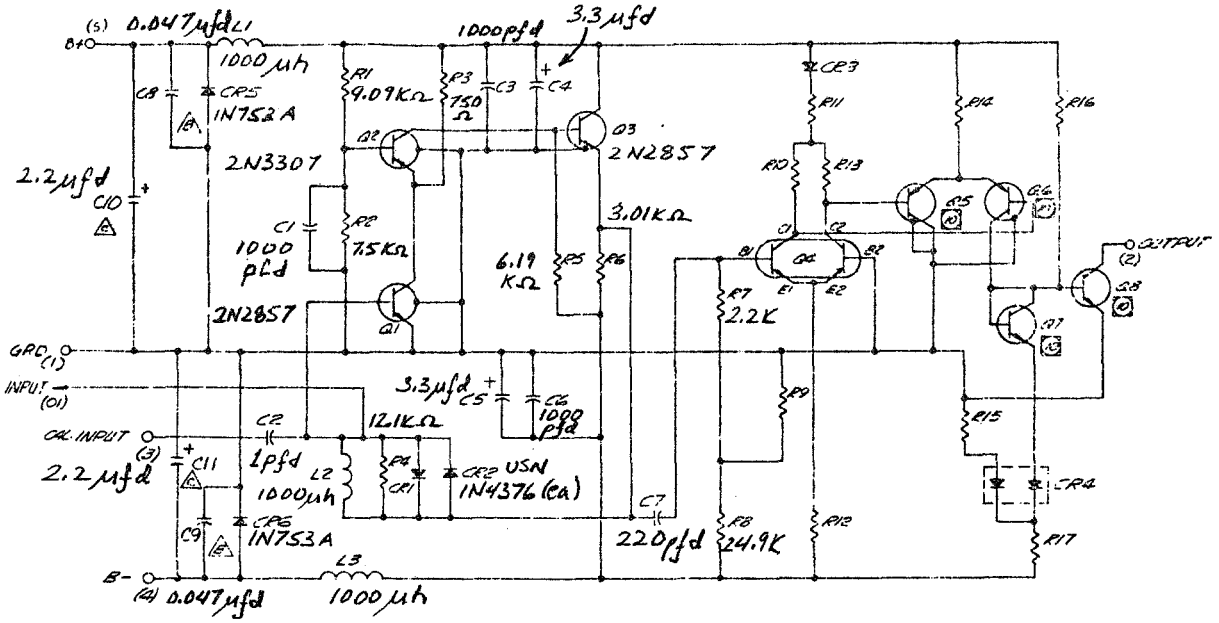


FIG. 8.2-3 CHARGE-SENSITIVE AMPLIFIER (WITH OUTPUT DETECTOR) SCHEMATIC

If the assumption is made that the incoming signal pulse width is small compared to the RC decay time, the following expression is obtained from the equivalent circuit for E_0. Then

$$E_o \cong \frac{Q_{in}}{\frac{(C_D + C_f)}{A} + C_f} \times e^{\frac{-t}{\tau}}$$

where $\tau \cong R_f C_f$ if $A > 10$ and $C_D \ll C_f (A + 1)$

Examination of this response function, for values used, shows the gain decreases by only 1.7% for a 5 pf change in detector capacity. However, in a pulse count mode operation, the threshold levels are usually set at a magnitude 10 to 100 times below the average pulse height. A change of 1.7% at the threshold level virtually does not affect the pulse count accuracy. Changes in open loop gain can also affect the accuracy. It can be shown that a change in open loop gain of 50% then, changes the output of the amplifier by only about 4.3%. Thus, a 50% gain variation also does not affect the pulse count accuracy for the same reason as previously described.

The amplifier is a direct coupled complementary design which offers the inherent benefits of simplicity and the associated reliability of a minimum number of components and a rapid recovery and protection from large signals and system transients. Extremely fast signals approaching a "delta-function" can be passed by this amplifier.

Refer to Figure 8.2-3. Transistors Q1 and Q2 provide a cascade pair input. This combination results in minimal input capacity, feed thru capacity, maximum voltage gain with a minimum phase shift enabling stable operation even with unity feedback. Q3, a common collector state, provides the current gain necessary to drive the feedback network and following stages. Performance of an amplifier of this type is voltage gain of better than one hundred (100) with bandwidth in excess of 50 MHz and an input capacity less than five (5) picofarads.

d. List any previous publications of the disclosure: none.

III Degree of Development

Development Completed

IV Technological Significance

Design Improvement

8.3 Free-Running Switching Mode Power Regulator

I Title of Disclosure

Free-Running Switching Mode Power Regulator

II Abstract

Free-running switching-mode power regulator is used to achieve higher efficiency, greater thermal control, reduced electrical stresses on components, and reduced size and ratings of components and heat - dissipating devices.

III Description

a) General Purpose: Non-linear power regulator is used to achieve higher efficiency.

b) Improvements or advantages: See item (c).

c) Description: The requirement for high efficiency power regulators for space applications is well known. Conventional linear regulators are usually inefficient, and require higher rated components due to increased electrical stresses. Linear regulators continuously dissipate power in the transistor, and thus require larger heat sinks.

The main advantage of switching voltage regulators over conventional linear series regulators is their greater efficiency. Efficiency ratings of up to about 90% can be realized.

The free-running switching-mode regulator consists of a series switch between the voltage source and load. The switch is closed when the output voltage drops below a specified level, and opened when the output voltage rises above another specified level. The switching frequency and the output ripple are related to the difference between the two specified levels (system hysteresis), the loop filter and other design parameters. Refer to Figure 8.3-1 for a block diagram. The transistor serves as a switch and is either shut off or saturated. Thus when the current is high, the voltage is low, so the

power dissipated in the transistor is minimum. The error (or comparator) amplifier may be any suitable type of dc amplifier. The cycle is divided in two. During the first part, t_1, in Figure 8.3-2, the transistor is conducting and the diode is back-biased by the total input voltage. Since the voltage across the choke is assumed to be constant, the current through the choke, which is also the transistor current, will increase linearly with time, according to $E_i - E_o = L\Delta i/\Delta t$. When the output voltage reaches a predetermined level, a voltage comparator circuit turns the transistor off. At that time, the current in the choke has reached the value I_{max}, which is the maximum value of current that will flow through either the pass transistor or the choke.

During the second part of the cycle when the transistor is shut off, the current in the choke starts to decrease; the voltage across the choke reverses polarity. This polarity change is in a direction to turn on the diode, and the choke then becomes clamped to the capacitor, which has the output voltage E_o across it. The choke current therefore decreases linearly, according to $E_o = L\Delta i/\Delta t$. When the choke current falls below the load current, the capacitor will supply the difference to the load. The capacitor will then discharge. When the voltage across the capacitor falls below a level determined by the voltage comparator circuit, the transistor will again be turned on. The ripple frequency will vary with fluctuations in input voltage and load requirements.

d) Does the contractor intend to file a patent application? No.

e) List publications pertaining to this item and where they may be obtained. IEE Transactions on AEROSPACE; Volume AS-2, Number 4, October 1964.

III Applications

Power regulators, where efficiency, thermal control and component size and ratings is critical.

IV Degree of Development

Development Completed.

V Technological Significance

Major Improvement

8.4 Vacuum-Encapsulation of High-Voltage Modules

I Title of Disclosure

Vacuum-encapsulation of high-voltage (3.5 to 4.5 kV) modules to ensure sufficient outgassing to prevent arcing, leakage, and corona effects.

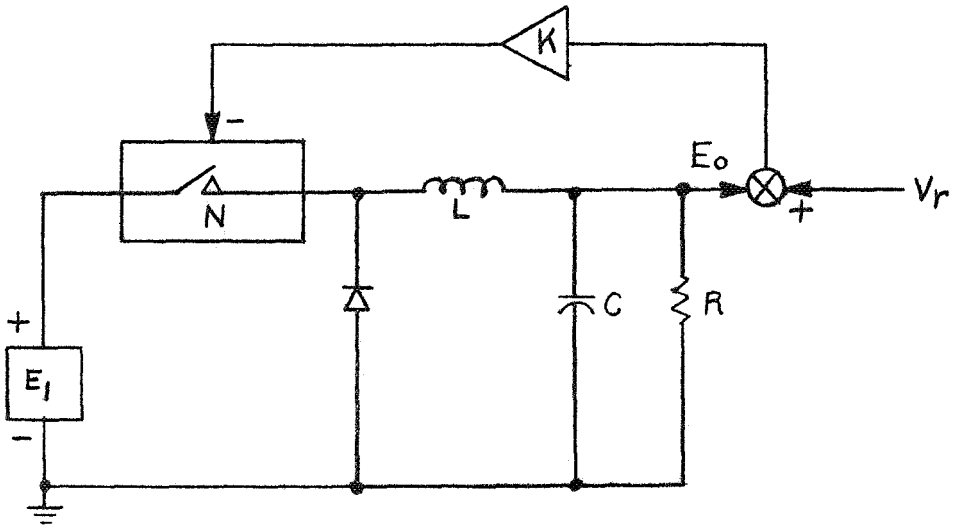


FIG 8.3-1, BASIC SWITCHING-MODE REGULATOR

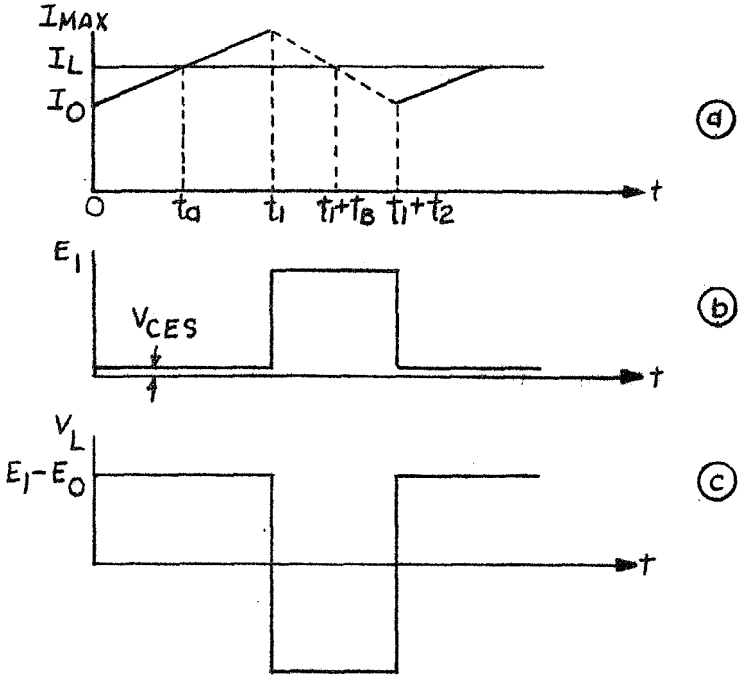


FIG 8.3-2, WAVE-FORMS, SWITCHING MODE REGULATOR

II Abstract

Sylgard 182 potting resin is used in critical high-voltage subassemblies. Encapsulation is performed under vacuum to ensure elimination of trapped air or gas bubbles. This process in combination with designed vent holes and gap lengthening techniques minimizes the possibility of arcing, leakage, and/or corona effects in high voltage supplies for space operation. Sylgard 182 has a further advantage of non-carbonization when subjected to high voltage arcing.

III Description

a) General Purpose: See item II

b) Improvements and/or advantages: Encapsulation is performed under vacuum to remove trapped air from the potting material to protect against outgassing in subsequent vacuum operation.

c) Description: Manufacturer's specifications for Sylgard 182 potting resin are attached. The following is a discussion on the vacuum-potting technique used. Typical encapsulation of a high voltage power supply subassembly is discussed.

ENCAPSULATION PROCEDURE

Surface Cleaning: Assembly is cleaned thoroughly using 99% isopropyl alcohol followed with de-ionized distilled water. All dirt, grease, resin and foreigh contaminants are removed before proceeding.

Mold Preparation: Module molds are made of plexiglass and/or plate glass to assure visual inspection during pouring and curing operation. Molds are released with Vel or Dreft detergent and water solution. Mold sealing is done with a Sylgard dam along all seams and exits.

Barrier Coat 1332: Is applied to areas where cure inhibitors are present. See S40638 3.5.

Primer Application: Surfaces to be treated with Sylgard primer are cleaned and dried before application. The primer is applied by brushing or wiping to surfaces that are at room temperature. The excess is drained on a paper towel and air dried at room temperature for at least 30 minutes.

Measuring: The ratio of Sylgard to the curing agent is 100:10 parts by weight. Use of a thinner to vary viscosity is prohibited since the thinner has a high rate of outgassing. Unwaxed lily cups or glass beakers are used for mixing. All mixing is done with care to minimize entrapment of air.

NOTE: Moisture and impurities are kept from entering resin. It is of prime importance that the mixing not be done in the presence of epoxies. The Sylgard mixture is placed under vacuum (5 mm of mercury) and degassed until all bubbles break.

Embedding: A dispensing cartridge is filled with Sylgard and an air hose connected (See Figure 8.4-1). A dispensing needle is inserted as close to bottom of assembly as possible leaving approximately 1/16" clearance and is secured into position. A 15 psi pressure is introduced to allow Sylgard to slowly wet the assembly from bottom to one-half the height of the assembly. After visual inspection to assure absence of air bubbles, the remainder of the assembly is filled and another visual inspection is performed. Upon completion, dispensing equipment is withdrawn and the assembly is placed into a clean area and allowed to cure for 24 hours at the specified curing temperature.

IV Degree of Development

Development Completed.

V Technological Significance

Major Improvement.

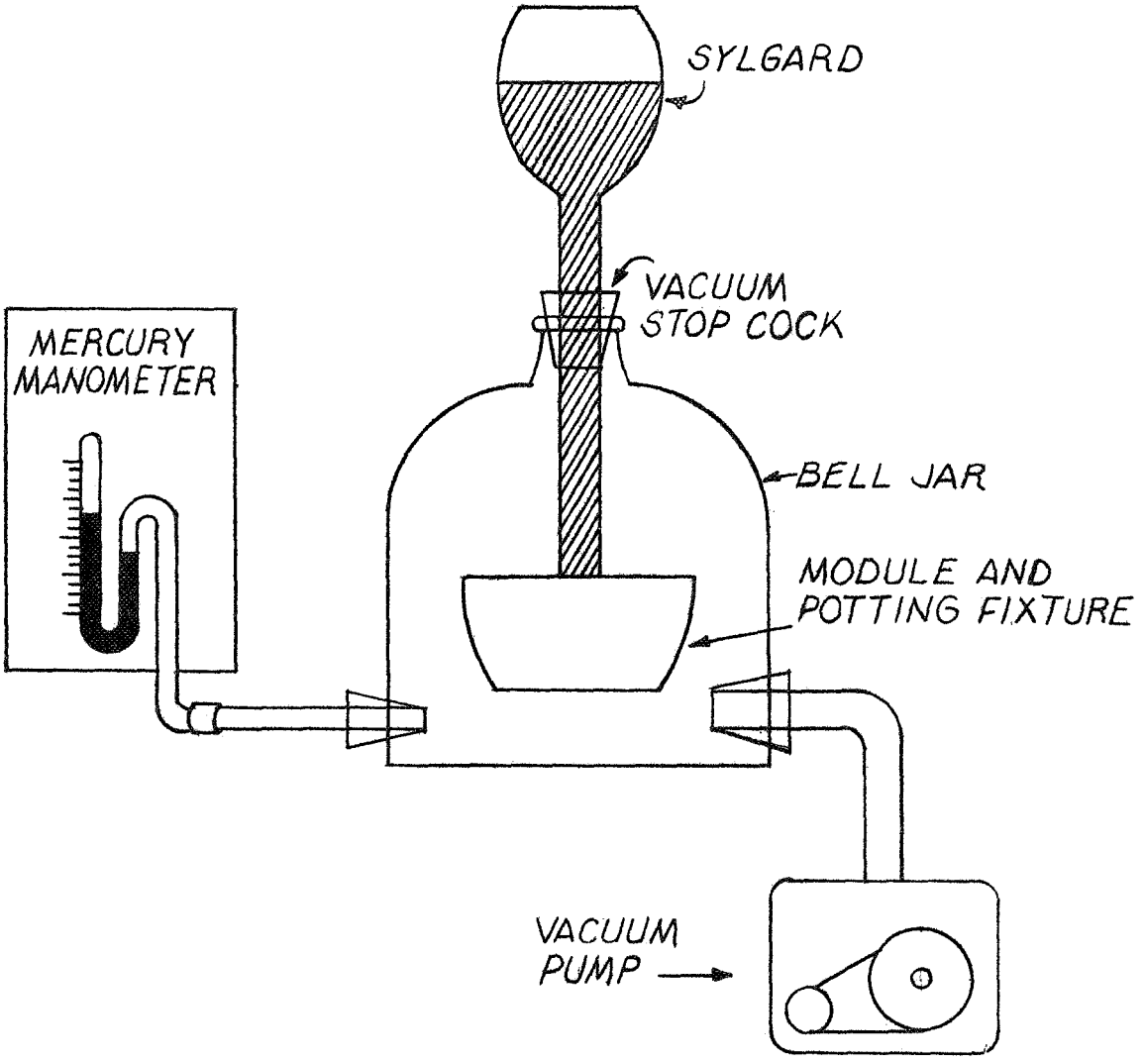


FIG 8.4-1 VACUUM ENCAPSULATION SETUP

SYLGARD 182 Potting and Encapsulating Resin

Sylgard* 182 resin is a low viscosity, solventless silicone resin designed for potting, filling, embedding and encapsulating. It is supplied as a nearly colorless fluid that flows easily, even around intricate parts.

Features of the Fluid Resin

Sylgard 182 resin is easy to process and use. The resin and its curing agent blend readily, and the low viscosity of the catalyzed material (under 4,000 centipoises) coupled with its long pot life (about 8 hours at 77 F) make it practical to use in automatic dispensing equipment.

Neither the resin nor the curing agent is known to produce any toxic effect upon contact with the skin, nor to give off any noxious fumes during mixing or curing.

Sylgard 182 resin cures at moderate temperatures, and without exotherm. When mixed with the correct amount of curing agent, the resin will cure in 4 hours at 65 C (149 F); cure can be accelerated by using higher temperatures. The rate of cure is constant regardless of sectional thickness, or the degree of confinement.

Features of the Cured Resin

When set up, Sylgard 182 resin needs no further afterbake. It can be placed in service at once, at any operating temperature between −65 C to 200 C. Other features of the cured resin are:

- *transparency* — embedded parts can be inspected visually;
- *easy repairability* — sections of the resin can be cut out for replacement of components; new resin can be poured in place and cured to re-form a tight seal;
- *physical and electrical stability* — retains properties from −65 to 200 C (−85 to 392 F), over a wide range of frequency and humidity;
- *firmness and flexibility* — Shore A Scale hardness of approximately 40; elongation of approximately 100 percent;
- *mechanical strength* — tensile strength in the range of 800 to 1,000 psi;
- *good damping qualities* — low transmission of vibration and shock;
- *self-extinguishing* — as tested in accordance with ASTM D 635;
- *no depolymerization* — will not depolymerize when heated in confined space;
- *fungus resistance* — non nutrient when tested in accordance with MIL-E-5272.

SPECIFICATIONS FOR SYLGARD 182 RESIN

(These values are Dow Corning quality control standards)

As Supplied	
ASTM D-1298, Specific Gravity at 25° C	1.05±0.03
ASTM D-445, Viscosity at 25° C centistokes	4,000 to 6,500
Shelf Life at 25° C, minimum	1 year
Pot Life at 25° C (with 10 pph curing agent added), minimum	8 hours
APHA Color, maximum	250
Cured properties using 10 parts by weight of curing agent to 100 parts by weight of resin.	
After 4 Hours at 65° C:	
ASTM D-792, Method A, Specific Gravity	1.05±0.03
ASTM D-676 Hardness, Shore A Scale Durometer points, minimum	35
ASTM D-149 Electric Strength*, volts per mil, minimum	500
ASTM D-150 Dielectric Constant, maximum, at 10^2 cps	2.88
at 10^5 cps	2.88
ASTM D-150 Dissipation Factor, maximum, at 10^2 cps	0.002
at 10^5 cps	0.002
ASTM D-257 Volume Resistivity, ohm-cm, minimum	1×10^{13}
After 1 hour at 150° C:	
ASTM D-412 Die C, Tensile Strength, psi, minimum	800
ASTM D-412 Die C, Elongation, % minimum	100

* Tested on specimen 0.062 inch thick, using ¼-inch standard ASTM electrodes, 500 volts per second rate of rise.

(Continued on next page)

DOW CORNING

BULLETIN: 07-214 DATE: AUGUST, 1966

ELECTRONICS PRODUCTS DIVISION
DOW CORNING CORPORATION
MIDLAND, MICHIGAN 48640

ATLANTA BOSTON CHICAGO CLEVELAND DALLAS LOS ANGELES NEW YORK

Mixing

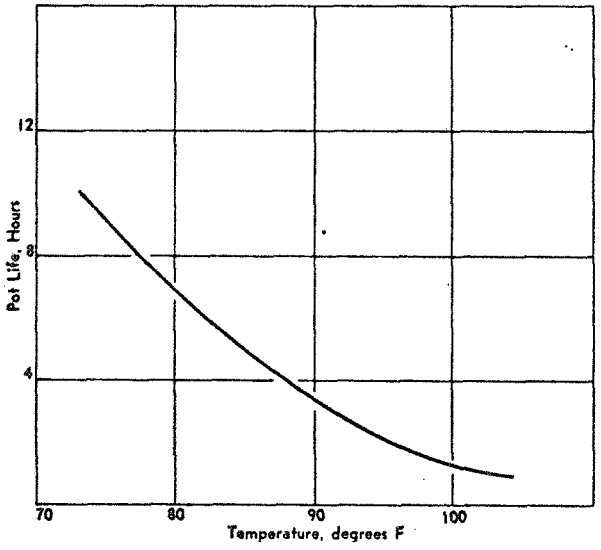
A curing agent for Sylgard 182 resin is supplied with each order. Just prior to use, the two are blended in the ratio of 100 parts of resin to 10 parts of the curing agent, by weight. Thorough mixing is easy, since both resin and curing agent are supplied as low viscosity fluids. During mixing, care should be taken to minimize entrapment of air. Any entrapped air should be removed before the resin is poured.

If the resin is allowed to stand for about one hour, most of the entrapped air will escape. For more complete de-airing, the use of a vacuum is required. The vacuum should be applied slowly; otherwise, the material may foam and overflow the container. (As a rule, containers should be no more than half full.) Maximum vacuum should be held for 3 to 5 minutes after all bubbles have collapsed.

The pot life of Sylgard 182 resin depends upon the temperature. The following graph illustrates this point.

Pot Life vs. Temperature

(The criterion of pot life is the increase in viscosity beyond which the material no longer handles conventionally.)



The pot life of the activated resin can be significantly increased by refrigeration. For instance, holding the material at −20 C (−4 F) will extend pot life to about thirty days.

NOTE: Moisture should not be allowed to get into the resin.

Varying Curing Agent Concentration

Variations of up to ten percent in the concentration of curing agent in Sylgard 182 resin have little effect upon set-up time or on the properties of the final cured part. Lowering the curing agent concentration by more than 10 percent will result in a softer, weaker material; increasing the concentration by more than 10 percent will result in an overhardening of the cured resin, and will tend to degrade physical and thermal properties.

Varying Resin Consistency

The consistency, or viscosity, of Sylgard 182 resin in its uncured form can be lowered by the addition of a thinner devised especially for use with Sylgard brand resins. This thinner may be used in amounts ranging up to 35 parts of thinner per 100 parts of resin, by weight. Used in these amounts, the pot life and curing time of the activated resin are not significantly affected. Certain properties of the cured resin, however, are affected by the use of thinner — namely hardness, brittle point, and weight loss. Details are given on the data sheet describing the thinner.

Preparing Containers and Components

Containers, molds, or components which come into contact with Sylgard 182 resin should be clean and dry. Containers or molds which have been used to handle room temperature vulcanized silicone rubber, organic rubber, or plastics should not be used, since traces of these materials may inhibit the cure of Sylgard 182 resin.

Adhesion

Whenever maximum adhesion between the cured resin and the surface it contacts during cure is desired, a Sylgard® brand primer should be used. This primer is available from Dow Corning; instructions for use are provided with the primer.

Suitable Release Agents

When Sylgard 182 resin is to be cured in molds, the mold should first be treated with a release agent to prevent the part from sticking.

Suitable release agents include Lunn-lease*, Dupanol WAQ or household detergents such as Vel or Dreft. Lunn-lease is diluted to about 10% concentration in acetone before application; Dupanol WAQ, to a 3 to 5% concentration with isopropanol; and Vel or Dreft, to a 2 to 5% concentration with water.

Potting and Embedding Procedure

When pouring Sylgard 182 resin into the container in which it is to be cured, care should be taken to minimize air entrapment within the system. Where practical, it is suggested that pouring be done under vacuum, particularly if the component being potted or embedded has many fine voids. When this technique cannot be used the unit should be evacuated after the resin has been poured.

* Lunn Laminates, Inc., Huntington Sta., New York, N. Y.

PREPARATIONS AND CURING (continued)

Curing

Activated Sylgard 182 resin can be cured with dry heat or by techniques involving immersion in hot liquids. Satisfactory sources of dry heat include circulating or noncirculating ovens, infra-red lamps, or heat guns.

Cure temperatures for Sylgard 182 resin range from 65 C (149 F) to 150 C (302 F); longer curing times are necessary at the lower temperatures, as is shown in the following chart.

*Curing Schedules**

Temperature	*Time*
65 C (149 F)	4 hours
100 C (212 F)	1 hour
150 C (302 F)	15 minutes

* With relatively massive parts, additional time in the oven should be allowed to bring the part up to temperature.

A resin film on dip-coated parts may be set up by immersing the coated part for 30 to 60 seconds in a glycerine bath maintained at a temperature of 150 C, followed by a post-cure in dry heat, for about 10 minutes at 150 C.

Another method used in dip-coating is to preheat the part to a temperature of 150 C, then immerse it in unheated activated Sylgard 182 resin for 30 to 60 seconds. Experimentation may show that the time should be varied somewhat to obtain the desired resin thickness. After the part is removed from the resin and allowed to drain, it is cured in an oven for 10 to 15 minutes at 150 C.

The success of this method is dependent upon the heat capacity and the configuration of the component being dip-coated. Suitability should be determined on a trial basis before being employed on a large scale.

APPLICATIONS

Sylgard 182 resin is used as an embedding and potting compound to provide resilient environmental protection for modules, relays, power supplies, delay lines, or complete electronic units.

This silicone resin can also be used as a dip coating material for encapsulating components and circuit boards.

ENGINEERING DATA

Operating Temperature Range

Cured sections of Sylgard 182 resin are usable over a temperature range of —65 to 200 C (—85 to 392 F).

When parts are embedded in Sylgard 182 resin, differences in thermal expansion values between the resin and the embedded parts — and the shape of these parts — may influence temperature limits at which such systems may be used. For this reason, thermal operating limits for embedded components should be accurately determined by laboratory tests before large scale use.

Compatibility

Sylgard 182 resin has been cured in contact with a large number of different materials that are found in electronic units. The materials tested included metals, plastics, glass, asbestos, natural and synthetic fibers, and ceramics. Sylgard 182 resin was found to cure satisfactorily in the presence of nearly all such materials. Exceptions that have been noted are butyl and chlorinated rubbers, some room-temperature-vulcanizing silicone rubbers, and unreacted residues of curing agents used with a few types of plastics.

Corrosion

No corrosion has been observed on common metals — notably copper — when used with Sylgard 182 resin.

TYPICAL PHYSICAL PROPERTIES

(These values are not intended for use in preparing specifications)

As Supplied

Color	Light Straw
Silicone Resin Content, percent	100
Specific Gravity at 25 C (77 F)	1.05
Viscosity at 25 C, centistokes	5,500
Viscosity, immediately after adding curing agent, centistokes	3,900
Shelf Life at 25 C	1 year
Pot Life* at 25 C (with curing agent added)	8 hours

* Time required for catalyzed viscosity to double at 25 C.

As Cured (4 hours at 65 C)

Color	Transparent; colorless to light straw
Hardness, Shore A Scale	40
Specific Gravity	1.05
Thermal Conductivity, cal per [(cm) (degree C) (sec)]	3.5×10^{-4}
Linear Coefficient of Thermal Expansion, in/in/degree C (—55 to 150 C)	300×10^{-6}
MIL-I-16923 C Thermal Shock Resistance, from —55 to 155 C	Passes 10 cycles
Weight Loss*, percent,	
after 1,000 hrs at 150 C (302 F)	1.6
after 1,000 hrs at 200 C (392 F)	3.2
Water Absorption, percent after 7 days immersion at 25 C (77 F)	0.10
Brittle Point, degrees C, lower than	—70
Refractive Index	1.430
Radiation Resistance, Cobalt 60 Source	Still usable after exposure to 200 megarads; hard and brittle after 500 megarads
Flammability (ASTM D 635)	Self-extinguishing

* Specimen size: 1 inch by 1½ inches by 1/16 inch thick.

TYPICAL ELECTRICAL PROPERTIES

(These values are not intended for use in preparing specifications)

General Data*

	As Cured	*Cured, then Aged 1,000 hours at 200 C (392 F)*
ASTM D 150 Dielectric Constant,		
60 cps	2.70	2.65
10^5 cps	2.70	2.65
ASTM D 150 Dissipation Factor,		
60 cps	0.001	0.001
10^5 cps	0.001	0.001
ASTM D 257 Volume Resistivity, ohm-cm	2×10^{15}	2×10^{14}
ASTM D 149 Electric Strength, volts per mil†	550	600

* 0.062 inch-thick specimens, cured 4 hours at 65 C.

† ¼ inch Standard ASTM Electrode, 500 volts per second rate of rise.

High Frequency Data‡

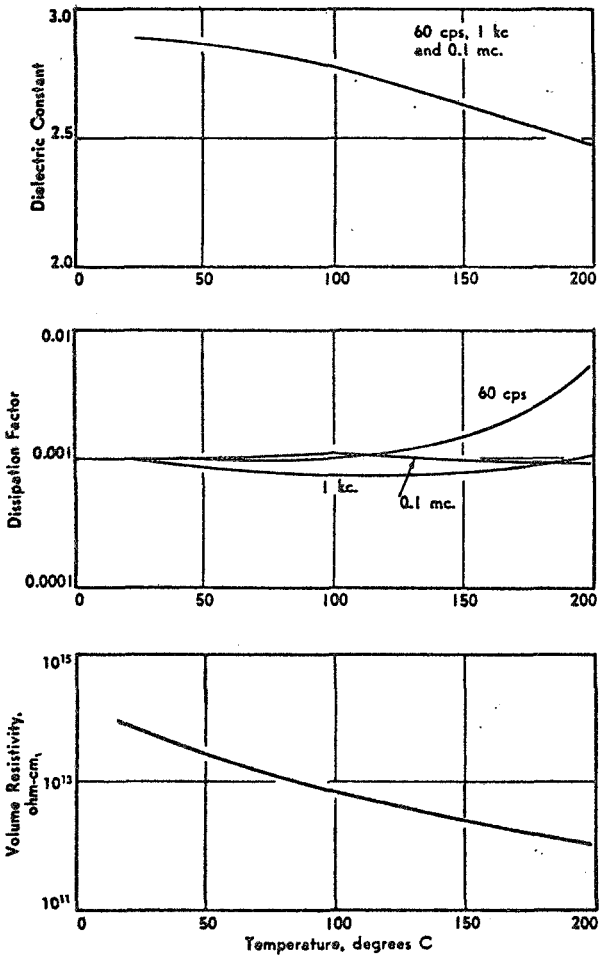
Properties	*at —55 C*	*at 23 C*	*at 150 C*
Dielectric Constant (ASTM D 150)			
at 1×10^6 cps	2.90	2.79	2.50
at 3×10^9 cps	2.86	2.77	2.48
at 8.5×10^9 cps	2.81	2.73	2.45
Dissipation Factor (ASTM D 150)			
at 1×10^6 cps	0.0200	0.0081	0.0026
at 3×10^9 cps	0.0240	0.0120	0.0040
at 8.5×10^9 cps	0.0290	0.0199	0.0073

‡ These values were determined at the Massachusetts Institute of Technology Laboratory for Insulation Research.

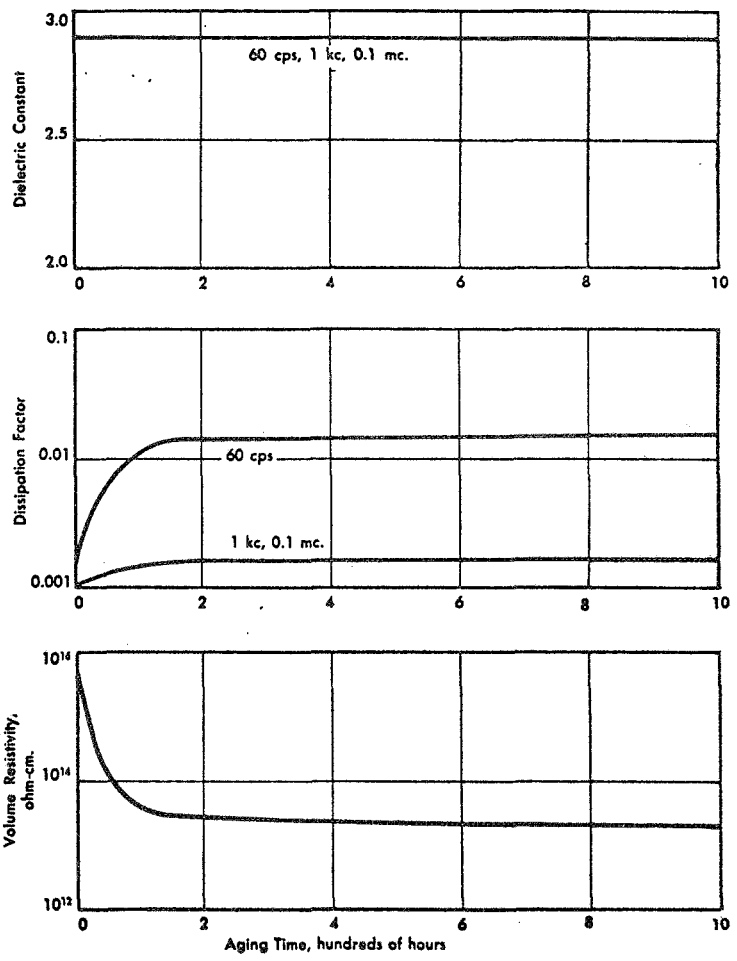
(Continued on next page)

EFFECTS OF ENVIRONMENT ON ELECTRICAL PROPERTIES OF THE CURED RESIN*

Effect of Temperature



Effect of Aging at 96% Humidity and 23 C



* Using 54 mmfd fixed air capacitors, Cardwell type ER-50-FS, ASTM D 150.

ELECTRIC STRENGTH VS. RESIN THICKNESS