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SUMMARY REPORT
On
Network Modeling of Manufacturing and Related Processes Using GERT

Research Sponsored
By
Electronics Research Center
National Aeronautics and Space Administration
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TABLE OF CONTENTS

Synopsis of Publications. 1

GERT EXCLUSIVE-OR Program 4

GERT Simulation Program Using Remote Batch Processing 6

Planning GERT Developments 6

APPENDICES

I. Distribution List for Computer Programs 9

II. Changes to GERT EXCLUSIVE-OR Program 10

SUMMARY REPORT

Synopsis of Publications

Figure 1 presents the publications on GERT associated with NASA contract No. NASA-12-2035 prepared at Arizona State University during the period October 1968 to June 1969. The technical reports listed in Figure 1 constitute the technical activities performed on this contract. These reports have been submitted separately to NASA as were copies of the papers, dissertations and theses.

Research during the past year was divided into three parts. The first part dealt with the modeling of a manufacturing process in order to demonstrate the capability of GERT to assist in the analysis and improvement of such a process. The five steps of the GERT approach to problem solving were employed. First a thorough study of an actual manufacturing operation was performed, and a network constructed to represent the process. Data collection and analysis was then necessary to obtain inputs for GERT EXCLUSIVE-OR program. This program provided statistical information to evaluate the manufacturing process. Alternative manufacturing operations for the process were then evaluated. For one sub-section of the process a sensitivity analysis was performed. The conclusion of this research was that GERT can be used as a method for analyzing manufacturing processes. It provides a convenient mechanism for discussing, designing, and improving such processes.

Technical Reports

- *GERT Simulation Program II (GERTS II)* by A. Alan B. Pritsker and Phillip C. Ishmael
- *An Analysis of a Manufacturing Process Using the GERT Approach* by William J. Thompson, F. Stanley Settles, and A. Alan B. Pritsker
- *Planning R & D Projects Using GERT* by Ronald A. Enlow and A. Alan B. Pritsker

Papers

- "Four GERT Views of R & D Planning," A. Alan B. Pritsker and Ronald A. Enlow. Presented at the Thirty-Fourth National Meeting of the Operations Research Society of America, November 1968.
- "The Status of GERT," A. Alan B. Pritsker. To be presented at INTERNET 1969 in Amsterdam, Holland, October 1969.
- "GERT: Part III - Further Statistical Results; Counters, Renewal Times, and Correlations," Gary E. Whitehouse and A. Alan B. Pritsker. *AIIE Transactions Industrial Engineering Research and Development*, 1:45-50, March 1969.
- "GERT Networks," A. Alan B. Pritsker. *The Production Engineer*, 47:499-506, October 1968.

Dissertations and Thesis (1969)

- "A GERT Network Approach to the Study of Queueing Phenomena," David John Gallagher.
- "On Determining a Distribution Function Known Only by Its Moment and/or Moment Generating Function," Thomas W. Hill, Jr.
- "GERT Network Models of Production Economics," F. Stanley Settles.
- "Consumer Brand Choice: A GERT Network Approach," David L. Eyestone.

Figure 1. ASU Publications on GERT Associated with NASA Contract NASA-12-2035, October 1968-June 1969

The second research activity involved the description of a research and development planning process. In this part of the research, GERT was used to study a generic area that involved the conceptualization of the process of planning in the form of a GERT network. This activity is significantly different from the modeling of an on-going process and involves heroic assumptions concerning the research and development process. However, the network developed provides an important element in the communication between researchers working on the description of R and D processes. For the GERT network description developed, the GERT computer programs were used to obtain results that illustrate a procedure for selecting between two suggested structures for a R and D process. Research was also performed on review procedures for assessing the worth of an on-going R and D project.

The third research effort involved the re-development of the GERT simulation program. The efficiency of the GERT simulation program was improved significantly. Of more importance, however, was the introduction into the GERT simulation program of three new concepts: (1) new node and branch characteristics; (2) modifications to the network depending on the activities completed; (3) incorporation of counting mechanisms. The new simulation program, GERTS II, brings to GERT new capabilities in terms of logical operations, information processing, and non-Markovian analysis. The further investigation of these concepts represents a challenging new aspect for GERT researchers.

During the contract period the GERT EXCLUSIVE-OR program was modified and improved. Copies of the source decks for both the EXCLUSIVE-OR

and simulation programs have been sent to NASA. A list of the individuals to whom these programs were distributed is included in Appendix I. A bibliography on GERT and related topics was also completed and submitted during the contract period.

The remainder of this report will summarize this year's GERT related research activities not reported in the technical reports.

GERT EXCLUSIVE-OR Program

Two basic changes were made in the GERT EXCLUSIVE-OR program. These are

(1) Changing the order for calculating path value.

(2) Reversing the print-out options codes.

By changing the order of path value calculations, it is possible to eliminate the storage of the nodes in all paths of a network. In this manner each path is analyzed sequentially to obtain its equivalent function. The revised version of the program records all first order loops in the LOOP array and then calculates the loop values. The nodes for a particular path are then located and stored in the LOOP array. The equivalent values for the path is then calculated taking into account all loops of the network. When the equivalent function for a path has been calculated, the nodes for the next path are determined and stored in the LOOP array in the same positions as the previous path. In this way only enough loop locations to record all the nodes in the longest path (the path with the largest number of nodes) plus all first order loops is required. Currently LOOP is dimensioned at 3000.

The second change in the program involves the option dealing with the print-out of loop and path nodes. In the revised version it is necessary to indicate that loop and path nodes should be printed, i.e., a 1 is required for this control variable. Computer time will be much less for large problems when print-out of loop and path values is suppressed. Thus, only when the analyst desires the loop and path values should they be printed.

Since the first change requires a slight increase in computing in order to save storage space, tests were made to compare the run time for both programs (considering the same print-out option). For all tests made there was no significant increase between the run times of the old and new version. However, problems which could not be run with the old version due to storage limitations were capable of being run with the new version.

The changes made in the GERT EXCLUSIVE-OR program are listed in Appendix II.

Additional research on the GERT EXCLUSIVE-OR program involved a comparison between NASAP Procedures for flow graph evaluation and the procedures used in the GERT EXCLUSIVE-OR program. The mapping procedure involves a one dimensional array with a complex pointing procedure. A method has been evolved to combine these two concepts to obtain a one dimensional mapping procedure which describes a network and which also can be easily interpreted. A second feature of one of the NASAP programs that enables the analysis of large networks is the recalculation of loop values whenever they are needed. This eliminates the need for storing

first order loops of a network which is the most restrictive storage element of the program. Analysis of the use of this technique for GERT networks is currently being explored. If feasible, it will permit the analysis of larger networks but will involve slower running times. For networks with less than 300 branches and 70 first order loops the current version of the GERT EXCLUSIVE-OR program is an efficient analysis tool.

GERT Simulation Program Using Remote Batch Processing

During the contract period the GERT simulation program was converted to a remote batch processing mode for a GE 600 series computer. This conversion facilitated the running of simulation problems by alleviating the data input requirements associated with the original GERT simulation program. With the development of GERTS II, the need for a remote batch processing capability was diminished and this activity was terminated. Remote batch processing does, however, offer some distinct advantages when many similar networks are to be analyzed. A copy of the draft report describing the remote batch processing simulation program has been forwarded to NASA.

Planning GERT Developments

As a first step in planning future activities, the current status of GERT developments was reviewed. This resulted in the paper "The Status of GERT." From this review it was determined that applications of GERT represent the greatest need with respect to making it an operational tool. It appears that GERT can be applied at both the gross and the detailed

level. This causes communication difficulties with those unfamiliar with GERT concepts. At the gross or systems level, GERT can be used as a modeling and communication aid. At the detailed level, GERT is an analysis technique that can yield relevant statistics concerning the process under study. Applications can and should be made at both levels and, in fact, a hierarchy of GERT network models can be evolved to relate the gross level to the detailed level. Practical applications of GERT at both levels is the most efficient way of introducing GERT to the scientific and technical community. Further, applications will pinpoint specific areas where additional research is required.

During the contract period, assistance was provided in organizing a group research effort to explore practical applications of GERT. The areas of application selected for this cooperative effort are:

(1) Planning the procedures for test and failure diagnostics

(2) Modeling and analyzing component fabrication

(3) Planning the development of procedures for traffic control

(4) Planning the allocation of resources for research and development of component systems which are used in many systems.

Figure 2 illustrates areas of research related to GERT broken down according to application, theoretical and computational lines. The areas listed in Figure 2 are not meant to be exhaustive but only illustrative of the types of research pertinent to GERT. Since GERT combines the concepts of stochastic networks and processes, signal flowgraphs, PERT and decision trees into a single framework, the number of research areas associated with GERT is extensive.

APPLICATIONS

- Gross Level
  - Systems Analysis Modeling
  - Planning R & D
  - Resource Allocations
  - Teaching
- Detailed Level
  - Stochastic Processes
  - Quality Control Plans
  - Manufacturing Processes
  - Marketing Promotions
  - Design Activities
  - Sequencing Rules

THEORETICAL

- Decision Structure — Chance versus Choice Events
- Performance Components
  - Cost
  - Time
  - Cost-Time (man-hours)
  - Reliability
- Review Procedures
  - Updating
  - Sensitivity
  - Improvement
  - Optimizations

COMPUTATIONAL

- Improved Efficiency
  - Storage
  - Speed
- Calculation of Higher Elements
- Inversion Techniques
- Simplified Input Requirements
- Flexible Statistics Collection
- Versatile Output Format
- Programming of Review Procedures

Figure 2. Areas of Research Related to GERT Development

APPENDIX I

DISTRIBUTION LIST FOR COMPUTER PROGRAMS

Mr. Richard W Counts
Aerospace Research Applications Center
Indiana University Foundation
Indiana Memorial Union
Bloomington, Indiana 47401

Mr. Thorleif Enger
Civil Engineering Department
University of Colorado
Boulder, Colorado 80302

Dr. S. Drezner
The RAND Corporation
1700 Main Street
Santa Monica, California 90406

Mr. Ramon S. Gomez
Industrial Engineering and Systems Analysis
Post Office Box 8294
University of Miami
Coral Gables, Florida 32124

Mr. Henry Metcalf
NASA/ERC, Code TCA
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Cambridge, Massachusetts 02139

Mr. Clifford C. Petersen
Motorola, Inc.
Government Electronics Division
8201 East McDowell Road
Scottsdale, Arizona

Dr. Joseph Moder
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Miami, Florida

Dr. G. Raju
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Athens, Ohio 45701

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Fayetteville, Arkansas 72701

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Lehigh University
Bethlehem, Pennsylvania 18015

Dr. Gary E. Whitehouse
Department of Industrial Engineering
Lehigh University
Bethlehem, Pennsylvania 18015

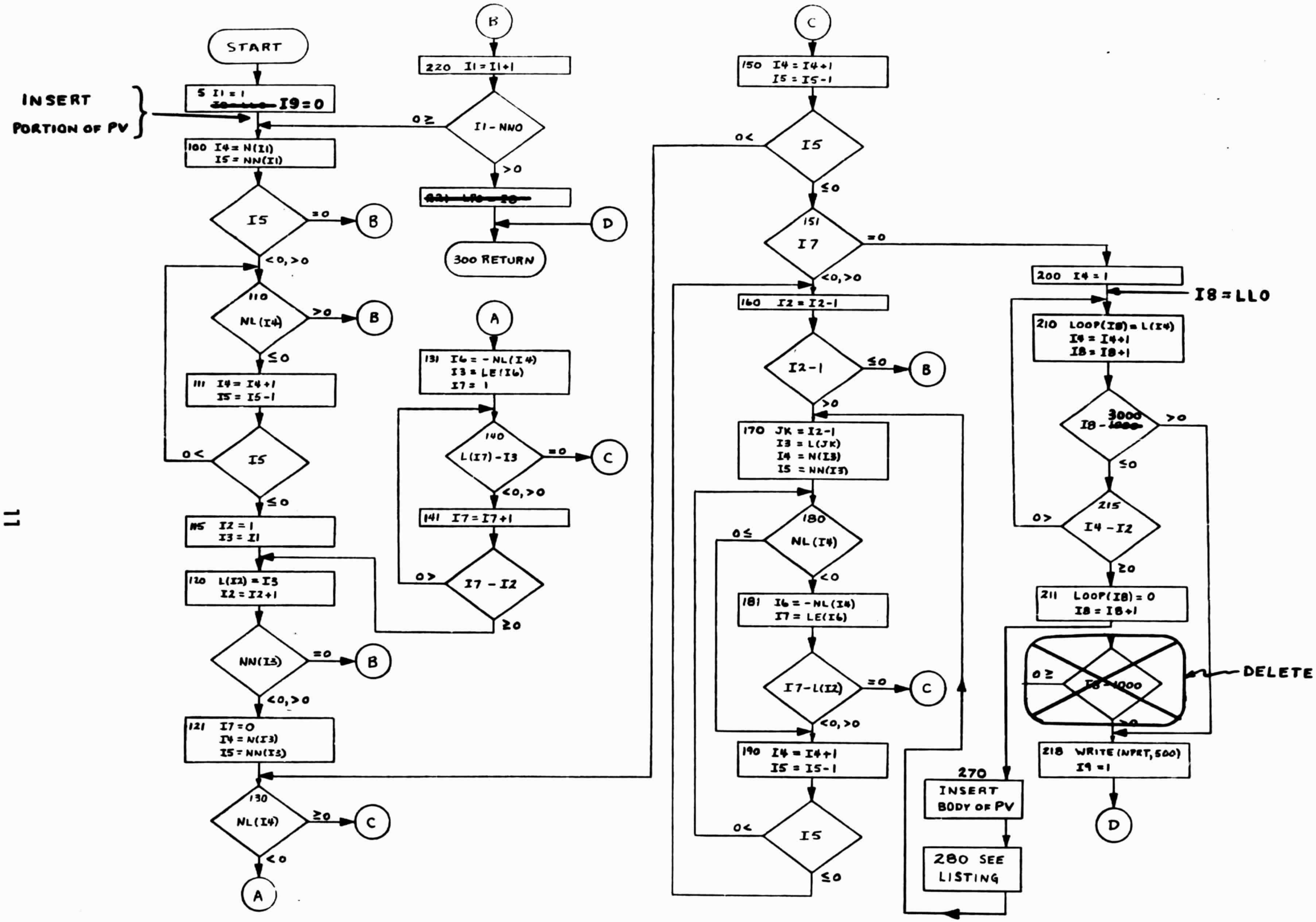
Miss Diane Zukowski
Western Electric
Corporate Education Center
Post Office Box 900
Princeton, New Jersey

APPENDIX II

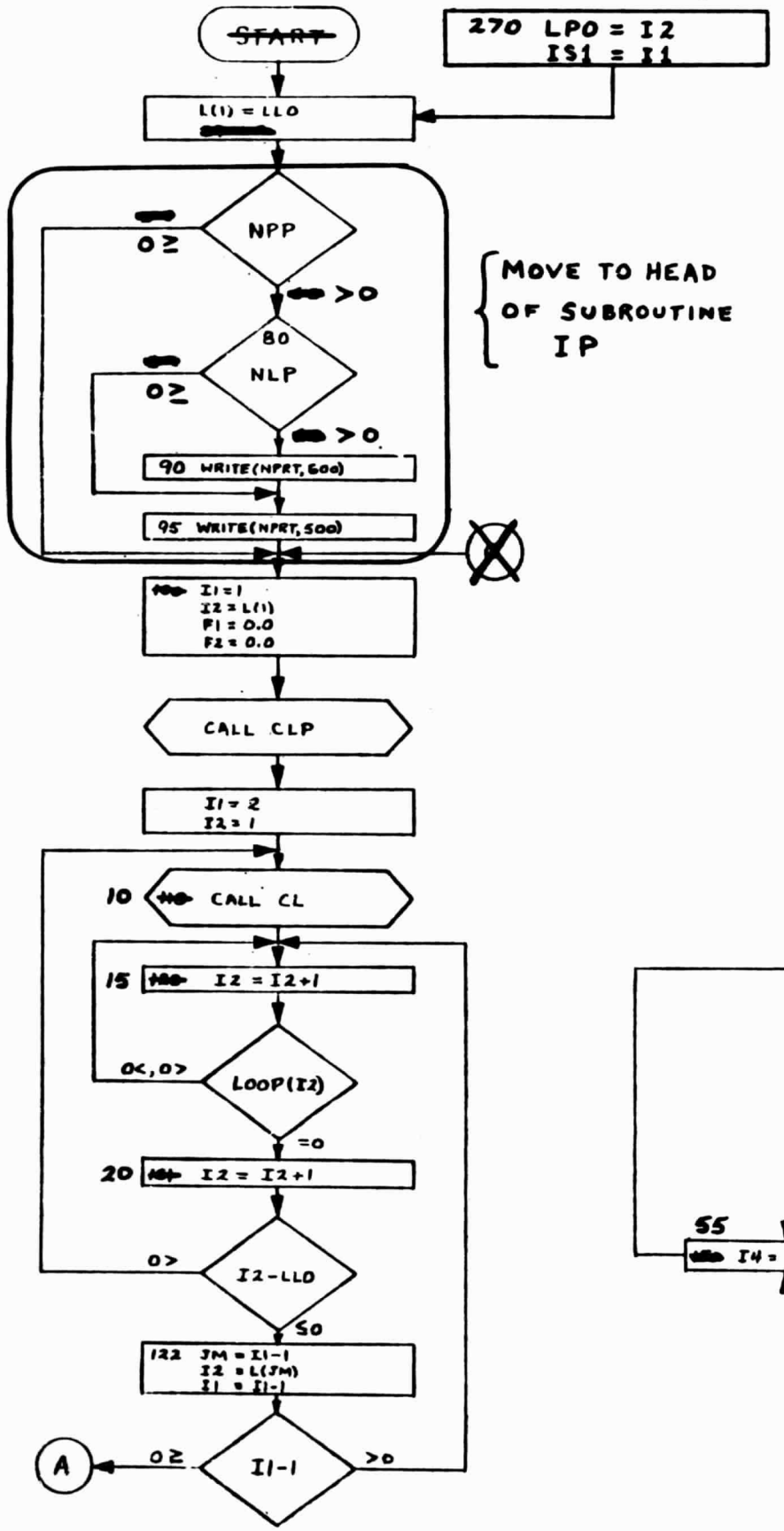
CHANGES TO GERT EXCLUSIVE-OR PROGRAM

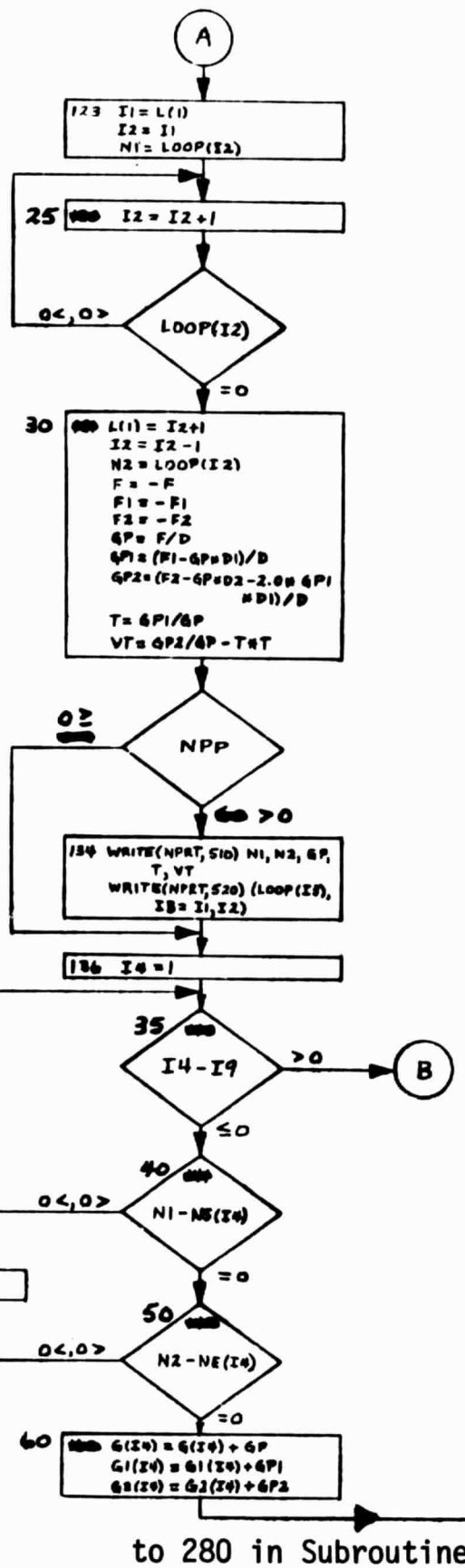
	Sequence Number	New Card
Main Program	GERT 320 GERT 330 GERT 340 GERT 350	CALL LV CALL IP IF(I9)100,115,115 [I9 is negative 115 CALL PRP for error]
Subroutine INPUT	INPT 320 INPT 340 INPT 410	DO 99 I1 = 1,600 DO 100 I1 = 1,300 DO 101 I1 = 1,300 } for new dimensions
Subroutine CLP	CLP 650	152 IF(NLP)200,200,153
Subroutine PRP	PRP 260 PRP 270	70 IF(NPP)80,80,90 80 IF(NLP)100,100,90

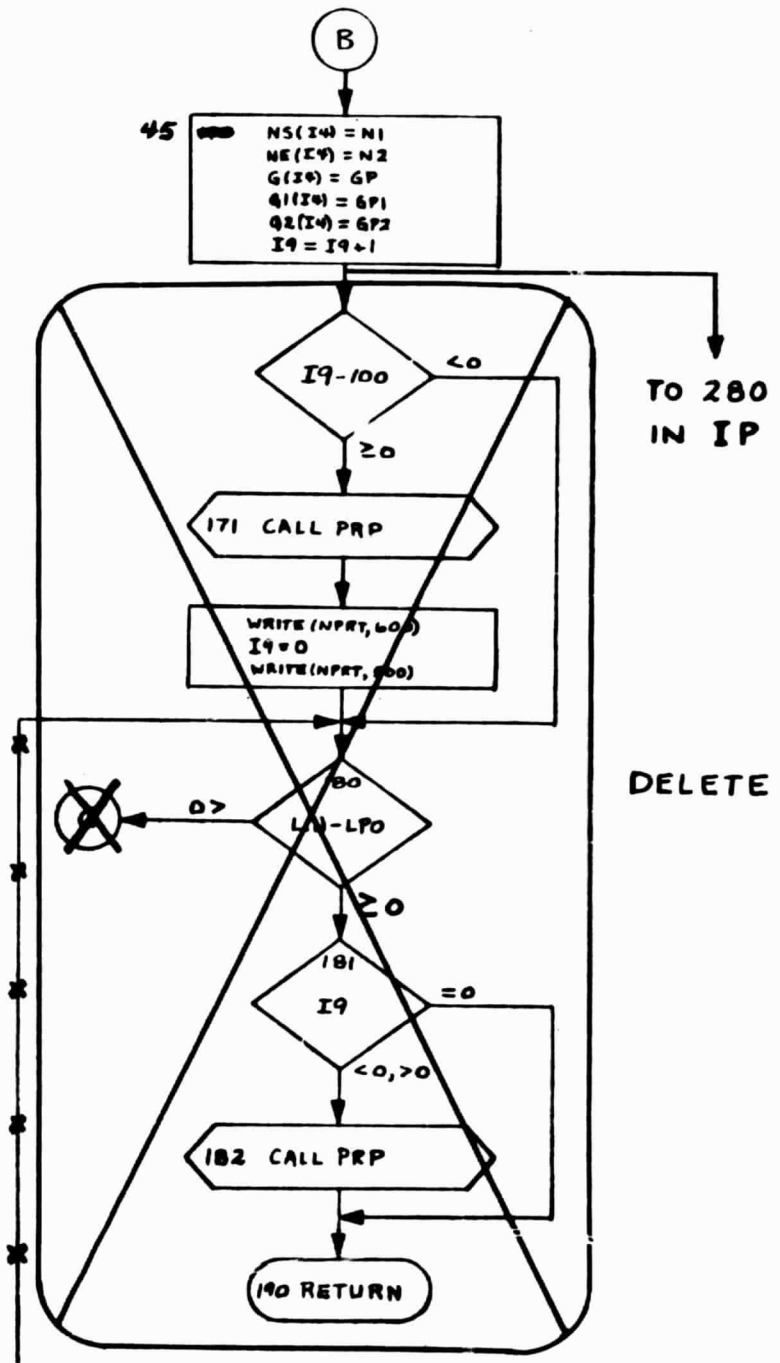
A major change was made by eliminating subroutine PV and putting the operations performed in PV in subroutine IP. To indicate the changes, the flow charts of the original versions of subroutines PV and IP are given on the next two pages with the modifications indicated. The new FORTRAN listing of subroutine IP is then given.



Flow Chart of Subroutine IP with Modifications







Flow Chart of Subroutine PV with Modifications

```
// JOB
// FOR CENTR
*ONE WORD INTEGERS
*NONPROCESS PROGRAM
*LIST ALL
      SUBROUTINE IP                                                          IP     1
C
C*****IDENTIFY PATHS AND CALCULATE PATH VALUES                               IP     2
C
       COMMON I1,I2,I3,I4,I5,I6,I7,I8,I9,                                    IP     3
     1        NNO,NLO,LLO,LPO,NLP,NPP,NCRD,NPRT,JCOR,                       IP     4
     2F,F1,F2,F3(70),F4(70),F5(70),F6(70),P(300),                           IP     5
     3        D,D1,D2,N1,N2,GP,GP1,GP2,T,VT,                                IP     6
     4T1(300),T2(300),LS(300),LE(300),N(300),NN(300),NL(600),L(300)         IP     7
       COMMON LOOP(3000),NS(100),NE(100),G(100),G1(100),G2(100),K(3),       IP     8
     1B(8),J(9),NAME(6),NJOB(2),MON,NDY,NYR,DEL                             IP     9
C
C*****IDENTIFY AND RECORD ALL PATHS THRU THE NETWORK                         IP    10
C
       IF(NPP)5,5,80                                                        IP    11
   80  IF(NLP)95,95,90                                                      IP    12
   90  WRITE(NPRT,600)                                                      IP    13
   95  WRITE(NPRT,505)                                                      IP    14
    5  I1=1                                                                 IP    15
       I9=0                                                                 IP    16
  100  I4=N(I1)                                                             IP    17
       I5=NN(I1)                                                            IP    18
       IF(I5)110,220,110                                                    IP    19
  110  IF(NL(I4))111,111,220                                                IP    20
  111  I4=I4+1                                                              IP    21
       I5=I5-1                                                              IP    22
       IF(I5)115,115,110                                                    IP    23
  115  I2=1                                                                 IP    24
       I3=I1                                                                IP    25
  120  L(I2)=I3                                                             IP    26
       I2=I2+1                                                              IP    27
       IF(NN(I3))121,220,121                                                IP    28
  121  I7=0                                                                 IP    29
       I4=N(I3)                                                             IP    30
       I5=NN(I3)                                                            IP    31
  130  IF(NL(I4))131,150,150                                                IP    32
  131  I6=-NL(I4)                                                           IP    33
       I3=LE(I6)                                                            IP    34
       I7=1                                                                 IP    35
  140  IF(L(I7)-I3)141,150,141                                              IP    36
  141  I7=I7+1                                                              IP    37
       IF(I7-I2)140,142,142                                                 IP    38
  142  GO TO 120                                                            IP    39
  150  I4=I4+1                                                              IP    40
       I5=I5-1                                                              IP    41
       IF(I5)151,151,130                                                    IP    42
  151  IF(I7)160,200,160                                                    IP    43
  160  I2=I2-1                                                              IP    44
       IF(I2 - 1) 220,220,170                                               IP    45
  170  JK=I2-1                                                              IP    46
       I3=L(JK)                                                             IP    47
       I4=N(I3)                                                             IP    48
       I5=NN(I3)                                                            IP    49
  180  IF(NL(I4))181,190,190                                                IP    50
  181  I6=-NL(I4)                                                           IP    51
```

```
      I7=LE(I6)                                                          IP   520
      IF(I7-L(I2))190,150,190                                            IP   530
  190 I4=I4+1                                                            IP   540
      I5=I5-1                                                            IP   550
      IF(I5)191,191,180                                                  IP   560
  191 GO TO 160                                                          IP   570
  200 I4=1                                                               IP   580
      I8=LLO                                                             IP   590
C
C*****RECORD NUMBERS OF NODES CONTAINED IN THIS PATH                      IP   600
C
  210 LOOP(I8)=L(I4)                                                     IP   610
      I4=I4+1                                                            IP   620
      I8=I8+1                                                            IP   630
      IF(I8-3000)215,215,218                                             IP   640
  215 IF(I4-I2)210,211,211                                               IP   650
C
C*****A LOOP(I8) VALUE OF ZERO SEPARATES THE PATHS                        IP   660
C
  211 LOOP(I8)=0                                                         IP   670
      I8=I8+1                                                            IP   680
      GO TO 270                                                          IP   690
C
C*****DIMENSION OF LOOP(I8) IS TOO LARGE, TERMINATE PROBLEM EXECUTION     IP   700
C
  218 WRITE(NPRT,500)                                                    IP   710
  500 FORMAT(//20X,17HPROBLEM TOO LARGE//)                               IP   720
      I9=-1                                                              IP   730
      GO TO 300                                                          IP   740
  220 I1=I1+1                                                            IP   750
      IF(I1-NN0)100,100,300                                              IP   760
  270 LP0=I2                                                             IP   770
      IS1=I1                                                             IP   780
  505 FORMAT(10X,2HNS,4X,2HNE,3X,4HPROB,7X,3HM T,7X,3HV T)               IP   790
  510 FORMAT(7X,I5,1X,I5,1X,F9.6,1X,F9.4,1X,F9.4)                        IP   800
  520 FORMAT(50X,15I5)                                                   IP   810
  600 FORMAT(1H1)                                                        IP   820
C
C*****INITIALIZE PATH SEARCH                                             IP   830
C
      L(1)=LLO                                                           IP   840
      I1=1                                                               IP   850
C
C*****L(1) IS THE FIRST NODE IN A PATH                                   IP   860
C
      I2=L(1)                                                            IP   870
      F=0.0                                                              IP   880
      F1=0.0                                                             IP   890
      F2=0.0                                                             IP   900
C
C*****CLP IS CALLED TO CALCULATE VALUES FOR THE BRANCHES IN THE PATH      IP   910
C
      CALL CLP                                                           IP   920
      I1=2                                                               IP   930
      I2=1                                                               IP   940
C
C*****CL IS CALLED TO LOCATE DISJOINT LOOPS***IT CALLS CLP TO            IP   950
C*****CALCULATE VALUES IF DISJOINT LOOPS ARE FOUND                       IP   960
```

```
C
    10 CALL CL                                                          IP   970
    15 I2=I2+1                                                          IP   980
       IF(LOOP(I2))15,20,15                                             IP   990
    20 I2=I2+1                                                          IP  1000
       IF(I2-LLO)10,122,122                                             IP  1010
   122 JM=I1-1                                                          IP  1020
       I2=L(JM)                                                         IP  1030
       I1=I1-1                                                          IP  1040
       IF(I1-1)123,123,15                                               IP  1050
   123 I1=L(1)                                                          IP  1060
       I2=I1                                                            IP  1070
       N1=LOOP(I2)                                                      IP  1080
    25 I2=I2+1                                                          IP  1090
       IF(LOOP(I2))25,30,25                                             IP  1100
C
C*****PATH VALUES ARE CALCULATED AND PRINTED OUT                        IP  1110
C
    30 L(1)=I2+1                                                        IP  1120
       I2=I2-1                                                          IP  1130
       N2=LOOP(I2)                                                      IP  1140
       F=-F                                                             IP  1150
       F1=-F1                                                           IP  1160
       F2=-F2                                                           IP  1170
       GP=F/D                                                           IP  1180
       GP1=(F1-GP*D1)/D                                                 IP  1190
       GP2=(F2-GP*D2-2.0*GP1*D1)/D                                      IP  1200
       T=GP1/GP                                                         IP  1210
       VT = GP2/GP-T*T                                                  IP  1220
C
C*****IF NPP IS GT ZERO, PATH PRINTOUT IS OBTAINED                      IP  1230
C
       IF(NPP)136,136,134                                               IP  1240
   134 WRITE(NPRT,510) N1,N2,GP,T,VT                                    IP  1250
       WRITE(NPRT,520) (LOOP(I3),I3=I1,I2)                              IP  1260
   136 I4=1                                                             IP  1270
    35 IF(I4-I9)40,40,45                                                IP  1280
C
C*****DETERMINE START AND END NODE FOR THE PATH                         IP  1290
C
    40 IF(N1-NS(I4))55,50,55                                            IP  1300
    50 IF(N2-NE(I4))55,60,55                                            IP  1310
    55 I4=I4+1                                                          IP  1320
       GO TO 35                                                         IP  1330
C
C*****START AND END NODE ARE THE SAME AS A PREVIOUS PATH***CONTINUE     IP  1340
C*****TO ACCUMULATE VALUES FOR PATHS WITH THESE SAME NODES              IP  1350
C
    60 G(I4)=G(I4)+GP                                                   IP  1360
       G1(I4)=G1(I4)+GP1                                                IP  1370
       G2(I4)=G2(I4)+GP2                                                IP  1380
       GO TO 280                                                        IP  1390
C
C*****START OR END NODE IS NOT THE SAME AS THE PREVIOUS PATH***BEGIN    IP  1400
C*****TO ACCUMULATE THE VALUES FOR THE NEW SET OF NODES                 IP  1410
C
    45 NS(I4)=N1                                                        IP  1420
       NE(I4)=N2                                                        IP  1430
```

```
      G(I4)=GP                                                          IP  1440
      G1(I4)=GP1                                                        IP  1450
      G2(I4)=GP2                                                        IP  1460
      I9=I9+1                                                           IP  1470
  280 I2=LPO                                                            IP  1480
      I1=IS1                                                            IP  1490
      I8=LLO                                                            IP  1500
      I4=1                                                              IP  1510
   65 L(I4)=LOOP(I8)                                                    IP  1520
      I4=I4+1                                                           IP  1530
      I8=I8+1                                                           IP  1540
      IF(LOOP(I8))170,170,65                                            IP  1550
  300 RETURN                                                            IP  1560
      END                                                               IP  1570
```