

FINAL REPORT ON
VOLTAGE CONTROLLED MONOLITHIC OSCILLATOR
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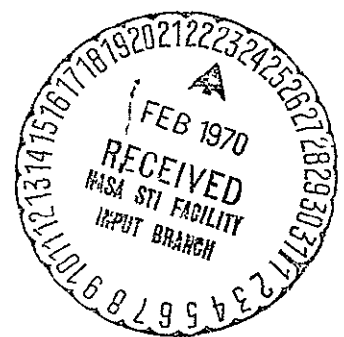
VOLTAGE CONTROLLED MONOLITHIC OSCILLATOR

CONTRACT NO. NAS8-20692

June, 1967 to March 1969

Written by: L. V. Colvson
T. V. Sikina

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Prepared for:

George C. Marshall Space Flight Center
Huntsville, Alabama

SOLID STATE VOLTAGE CONTROLLED OSCILLATOR (VCO)

ABSTRACT

A voltage-controlled oscillator has been developed by the Electronic Components Division of United Aircraft Corp. utilizing two silicon monolithic integrated circuit chips and a TaN thin film resistor chip. The oscillator has a typical fixed frequency stability of 0.0002% per degree centigrade. A 1% modulation linearity was obtained over a $\pm 15\%$ frequency bandwidth. The basic oscillator operated successfully from 400 Hz to 8 MHz, with integrated components. The oscillator has two outputs (complimentary) that are compatible with TTL circuits. The complete oscillator is packaged in a 3/8 by 3/8 inch flat package. The oscillator consumes approximately 250 mw from a 14 volt supply, or 150 mw from an 11 volt supply.

The oscillator program was concerned with significantly advancing the state-of-the-art in voltage-controlled oscillators. A system design that was compatible with molecular technology was chosen as a basis for the oscillator circuit configuration.

The primary design goals for the oscillator were:

1. 19.2 Khz with provisions for obtaining higher frequencies by connecting external resistors or shorting pins together at the package interface.
2. frequency stability of 10 ppm over a temperature range from -25°C to $+110^{\circ}\text{C}$.

3. package the complete oscillator in a 3/8 by 3/8 inch flat package.

The details of the oscillator design, the device design and fabrication, and the assembly and test of the final oscillator are thoroughly discussed. The information obtained in this program forms a sound basis for future development that will provide for a higher performance, lower potential cost and reduced size voltage-controlled oscillator.

FINAL REPORT
ON
VOLTAGE CONTROLLED MONOLITHIC OSCILLATOR

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SOLID STATE VOLTAGE CONTROLLED OSCILLATOR (VCO)

1.0 INTRODUCTION AND SUMMARY

The overall objective of the silicon monolithic oscillator program was to design, develop and fabricate one prototype unit and 10 final configuration units. The goals of the applied research and development program were to achieve a smaller, more stable and more reliable oscillator with the application of silicon semiconductor monolithic techniques.

The Electronic Components Division of United Aircraft has demonstrated its capabilities in the fabrication of stable, reliable and microminiature VCO oscillators utilizing the hybrid circuit approach. Although the basic circuit configuration used in the hybrid oscillator was proposed, with some process refinements to fabricate the silicon monolithic oscillator, subsequent test and analytical investigations indicated that the originally proposed circuit would not give the desired results. The stability of the selected oscillator could be improved by approximately 50% by using a controlled heating element to reduce the temperature range experienced by critical components in the oscillator. In the sections that follow, the details of a unique oscillator design, the device design and fabrication, and the assembly and test of the oscillator are presented. Technical problems encountered and their solutions are discussed.

2.0 DESIGN CONCEPTS

In order to facilitate the oscillator design, the essential oscillator functions are itemized as follows:

- a. frequency determining elements;
- b. oscillator stability elements;
- c. variable frequency control components;
- d. oscillator output characteristics.

The requirements imposed upon the individual and collective oscillator functions will determine the oscillator design technique that offers the best possibility for success. In particular, it is desirable that any oscillator function be generated or controlled separately without adversely affecting the remaining oscillator functions. The need for individually controlled functions is a necessary requirement because of parasitics and coupling effects associated with the monolithic integrated fabrication. Contrary to conventional circuit design using discrete components, circuits can best be optimized by using relatively large numbers of transistors and diodes at the expense of resistors and capacitors in the monolithic design approach.

2.1 Oscillator Circuit Approaches Considered

The oscillator circuit techniques considered were limited to those having to some degree separate and realizable oscillator function discussed in paragraph 2.0 and compatible with the silicon monolithic approach. The oscillators considered can be classified as follows:

- a. Wien bridge (resistor-capacitor controlled)
- b. Phase Shift (resistor-capacitor controlled)
- c. Multivibrator (resistor-capacitor controlled)
- d. Multivibrator (current-voltage-capacitor controlled)

2.1.1 The Wien bridge type oscillator has four (4) first order components weighted by a square root function in its frequency defining function as shown below:

$$f = \frac{A}{\sqrt{R_1 R_2 C_1 C_2}} \quad (1)$$

The Wien type oscillator does not have direct provisions for frequency control or frequency stability. The physical size of the timing capacitor would present a problem for mounting the complete oscillator in a 3/8 by 3/8 inch flat package. Thin film resistors are required to obtain frequency stability.

2.1.2 The phase shift oscillator has all the problems associated with the Wien type oscillator in addition to inherent susceptibility of parasitic capacitance and the larger size timing capacitors required.

2.1.3 The resistor-capacitor controlled multivibrator operates in the voltage-charge-time domain and can be analyzed by the three primary operating modes: (1) steady-state, (2) storage, and (3) transient. The oscillator frequency defining function has four first order voltages weighted by a logarithmic function and two first order components (RC) as shown as follows:

$$f = \frac{1}{RC \frac{L}{N} \left[\frac{(V_{CC} + V_C^1 - V_{besat}) - (V_{besat} - V_{cesat})}{V_{CC} - V_{besat}} \right]} \quad (2)$$

or

$$f = \frac{1}{RC \frac{L}{N} \left[\left(\frac{V_X}{V_Y} \right) \right]} \quad (3)$$

The resistor and capacitor can be temperature compensated because they are linearly related. However, referring to equation 2, the supply voltage V_{CC} , V_C^1 , V_{besat} and V_{cesat} have different temperature coefficients. They are related logarithmically to the timing capacitor and resistor. The steady-state condition provides suitable provisions for frequency control. The fast switching mode assures well defined output characteristics. However, the size of the timing capacitor for 19 KHz and the thin film resistors required for frequency stability would necessitate special packaging provision to assemble the complete oscillator in a 3/8 by 3/8 inch flat package.

2.1.4 Selected Oscillator Design - Current-Voltage-Capacitor-Controlled Multivibrator

The oscillator frequency defining function is determined from the principle that a linear voltage versus in time is developed across a capacitor when the charging current amplitude is constant. Mathematically, the charge-time relationship can be defined by the following integral:

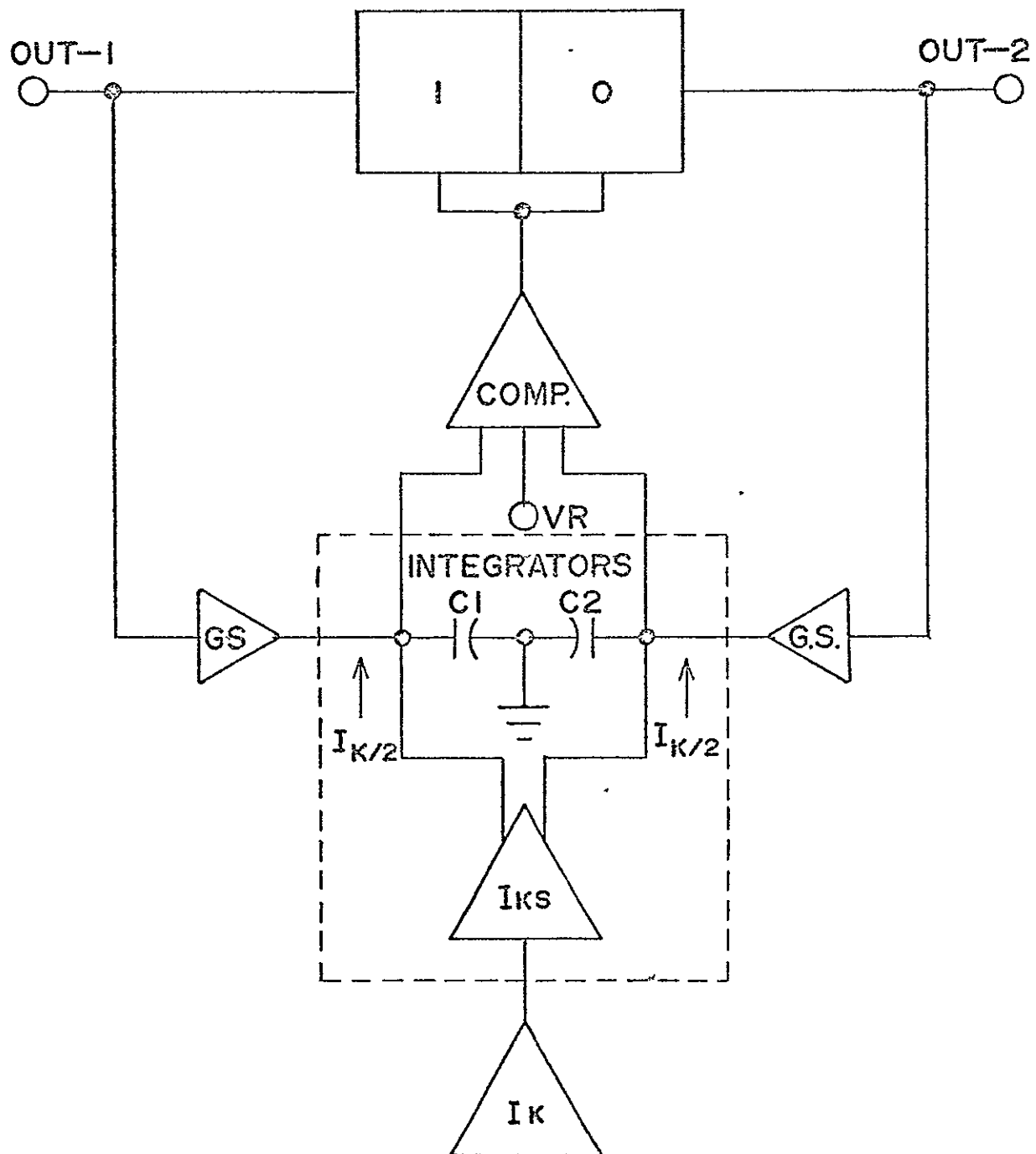
$$\int_{t_1}^{t_2} dv = \frac{1}{C_T} \int_{t_1}^{t_2} I_k dt = \left(\frac{I_k}{C} \right) \int_{t_1}^{t_2} dt \quad (4)$$

$$V(t) = \frac{I_k}{C_T} (t_2 - t_1) \quad (5)$$

If a mechanism can be found, such that, the capacitor is allowed to charge from times t_1 to t_2 and be discharged at t_2 , a linear sawtooth voltage $V(t)$ will be developed across the capacitor C_T . The technique used includes the comparator, flip-flop and a ground switch as shown in Figure 1. By using two integrating functions, two sawtooth voltages are generated. The dual channel comparator with a single output, flip-flop and ground switches forms an exclusive ORING function. Therefore, only one capacitor is allowed to charge at any one time. The sequential charging of alternate capacitors develops a continuous sawtooth voltage at the comparator's output. The comparator develops a continuous clock pulse that toggles the flip-flop at rate which is governed by the current supply $I_k/2$, capacitor C_T and the comparator reference voltage. The oscillator frequency defining function can thus be expressed as:

$$f_o = \frac{I_k}{2C_T V_{tt}} \text{ Khz} \quad (6)$$

where k is determined by the propagation delays through the comparator, the flip-flop and the ground switch. It is, therefore, necessary that the k be held constant in order not to become a frequency determining parameter. It can be observed that parameters within the oscillator frequency formula are linearly related and thus can be implemented with linear circuits. It is necessary to implement the constant k parameter with digital circuits for the reasons stated.



FUNCTIONAL OSCILLATOR SCHEMATIC

FIGURE 1

2.1.5 Circuit Analysis

The effective amplitude of the sawtooth voltage $V(t)$ is related to the constant current I_k , transistor leakage current, I_{co} , the comparator reference voltage V_r , and the ground switch offset voltage V_{ces} . The oscillator's generalized frequency formulae becomes:

$$f = \left[\frac{I_k + I_{co} K}{2C_T [V(t) \pm V_{ces} + V_{be}]} \right] \text{ Hz} \quad (7)$$

In the actual circuit, the leakage current from the NPN transistors used in the comparator supplies the leakage current for the PNP transistors used in the integrators. Thus, the net transistor leakage current available to charge capacitor C_T is the difference in leakage currents between the NPN and PNP transistors. The voltages V_{ces} and V_{be} have opposing temperature coefficients; therefore, the net comparator comparison voltage is the difference between the temperature coefficient of V_{ces} and V_{be} . The temperature dependence of the oscillator frequency stability can be expressed as follows:

$$F(I_k, V_t, C_t) = \frac{I_k}{2 C_t V_t} \text{ Hz} \quad (8)$$

$$\frac{\partial F}{\partial T} = \frac{1}{(2C_T V_T(t))} \left(\frac{d(I_k)}{dT} - \frac{I_k}{(2C_T V_t^2)} \frac{(dV)}{(dT)} - \frac{I_k}{(2C_T^2 V_t)} \frac{(dC_t)}{(dT)} \right) \quad (9)$$

$$\partial F = \left(\frac{1}{2C_T V_t} \right) dI_k - \left(\frac{I_k}{(2C_T V_t^2)} \right) dV_t - \left(\frac{I_k}{2C_T^2 V_t} \right) dC_t \quad (10)$$

$$\frac{\Delta F}{F} = \frac{2C_T V_T}{I_k} \left[\frac{\Delta I_k}{C_T V_T} - \frac{I_k}{C_T V_T} \left(\frac{\Delta V}{V_T} \right) - \frac{I_k}{C_T V_T} \left(\frac{\Delta C}{C_T} \right) \right] \quad (11)$$

The frequency dependency of individual parameters can be written as:

$$f_1 = f (\Delta I_k) \quad (8a)$$

$$f_2 = f (\Delta v) \times \left(\frac{\Delta v}{v} \right) \quad (9a)$$

$$f_3 = f (\Delta c) \times \left(\frac{\Delta c}{c} \right) \quad (10a)$$

$$\text{Then } \frac{\Delta F}{F} = [f_1 - f_2 + f_3] \text{ Hz} \quad (11a)$$

The frequency stability in parts per million can be written as:

$$\text{ppm} = \left[f_1 - (f_2 + f_3) \right] \times \frac{10^6}{F} \quad (12)$$

It can be seen from the oscillator stability derivations presented that the linear relationship for the frequency determining parameters holds for all conditions.

2.2 Selection of Oscillator Technique

Table I summarizes the significant features of the oscillator approaches discussed. This table shows the practical limitations of several oscillators that were considered and related values of components versus frequency. Thus, the approach taken, although selected as the most suitable from the standpoint of completely integrated circuits, is ideally suited for the hybrid operation since critical elements are independently related to the total oscillator requirements.

OSCILLATOR TYPE	FREQUENCY VS. COMPONENTS			
	FREQUENCY RANGE	COMPONENT RANGE	OUTPUT WAVEFORM	OPERATING POWER
Wien-Type $F_o = \frac{A}{(R_{1-2})(C_{1-2})}$	1 KHz to 1 Mhz	100 pf to 10000 pf 10 K to 100 K	Sinewave	50 mw to 100 mvw
Astable Multivibrator $F_o = \frac{1}{R_1 R_1 \left[\ln \frac{V_x}{V_y} \right]}$	2 KHz to 2 MHz	100 pf to 10000 pf	Squarewave	75 mw to 125 mvw
Astable CIV Type Multivibrator $F_o = \left[\frac{I_k}{2 C_T V_T} \right] K$	500 Hz to 8 Mhz	$I_k = 20 \text{ a to } 1.0 \text{ ma}$ $C_T = 100 \text{ pf to } 10000 \text{ pf}$ $V_T = 1.5V \text{ to } 3.0V$	Squarewave	200 mw to 300 mw

TABLE 1.
OSCILLATOR TYPE COMPARISON

Although all components used in the selected oscillator adhere to the monolithic integrated circuit approach, various functions were partitioned to minimize processing constraints and maximize performance. It was felt that the partitioning approach taken would be of considerably greater value than simply demonstrating an all integrated approach that would not advance the present state-of-the-art in performance, size and reliability.

2.2.1 Functional Circuits

The operation of the selected oscillator can best be explained by referring to Figure 1. The functional oscillator schematic consists of the following four circuit elements:

- a. clocked flip-flop
- b. dual input comparator
- c. dual channel integrator
- d. constant current supply

Assuming the flip-flop is in a stable state, then the ground switch controlled by the logic TRUE side of the flip-flop will allow the associated timing capacitor $C(t)$ to charge. The capacitor will charge until the voltage across the capacitor exceeds the comparator's reference voltage; the comparator generates a clock pulse that resets the flip-flop. The second ground switch, enables the second capacitor to charge and the first ground switch completely discharges the initially charged capacitor. The coincidence of the charging voltage across the second capacitor and the availability of a comparator reference voltage causes the flip-flop to reset and thus, oscillation is sustained.

2.2.2 Flip-flop

The flip-flop is required to change state on the negative transition of the pulse from the comparator. The flip-flop is constructed using TTL circuit technique, which provides for a low output impedance, approximately 20ns rise and fall times and 20ns transition delays. These fast switching times will minimize oscillator frequency deviations for changes in supply voltage, output loading and temperature changes.

2.2.3 Comparator

The comparator provides the necessary interface between the linear and digital operation of the oscillator. The comparator should provide a full output transition for a 1.0 mV differential at its input.

2.2.4 Integrators

The integrators convert the constant current (I_K) to a linear sawtooth voltage. The voltage amplitude and time interval of the sawtooth waveform constitutes the "heart" of the oscillator frequency range, output pulse symmetry and stability. The ground switches assure that the capacitor is completely discharged to a constant voltage.

2.2.5 Constant Current Supply

As shown in the oscillator frequency defining function, as shown in equation 5, the current supply has the greatest influence on total oscillator performance. The current supply can compensate for changes in the remaining frequency determining parameters, including temperature coefficient, oscillator frequency, range and stability.

To illustrate the versatility of the constant current supply, the following analysis is pertinent. Assume that a 20 μ A current is required to obtain a given oscillator frequency. The 20 μ A can be obtained readily with the current source and sink combination as follows:

$$\text{define } I_k = I_{\text{source}} - I_{\text{sink}}$$

$$\text{thus } I_k = 200 - 180 \mu\text{A} = 20 \mu\text{A}$$

The current source (I_{so}) and sink (I_{sk}) circuits are shown in Figure 2. Since the current source and sink are identical except for transistor types, only the current source need be analyzed. Refer to Appendix I for details.

2.3 Oscillator Breadboard Performance

After extensive circuit design, the various oscillator functional breadboard circuits using discrete devices were combined to form the integrated oscillator. The initial oscillator configuration used only the current source for the constant current supply. Test results of the four circuit modules when combined are shown in Figure 3. The results of the various circuit modules that make up the oscillator are described in the following paragraphs.

2.3.1 Flip-Flop

The flip-flop module gave excellent performance over the 135°C temperature range. Changes in rise and fall times and transition delays were less than 5ns. The flip-flop clock pulse had a 4 ± 1 volt amplitude range. The clock pulse fall time could vary by ± 20 ns.

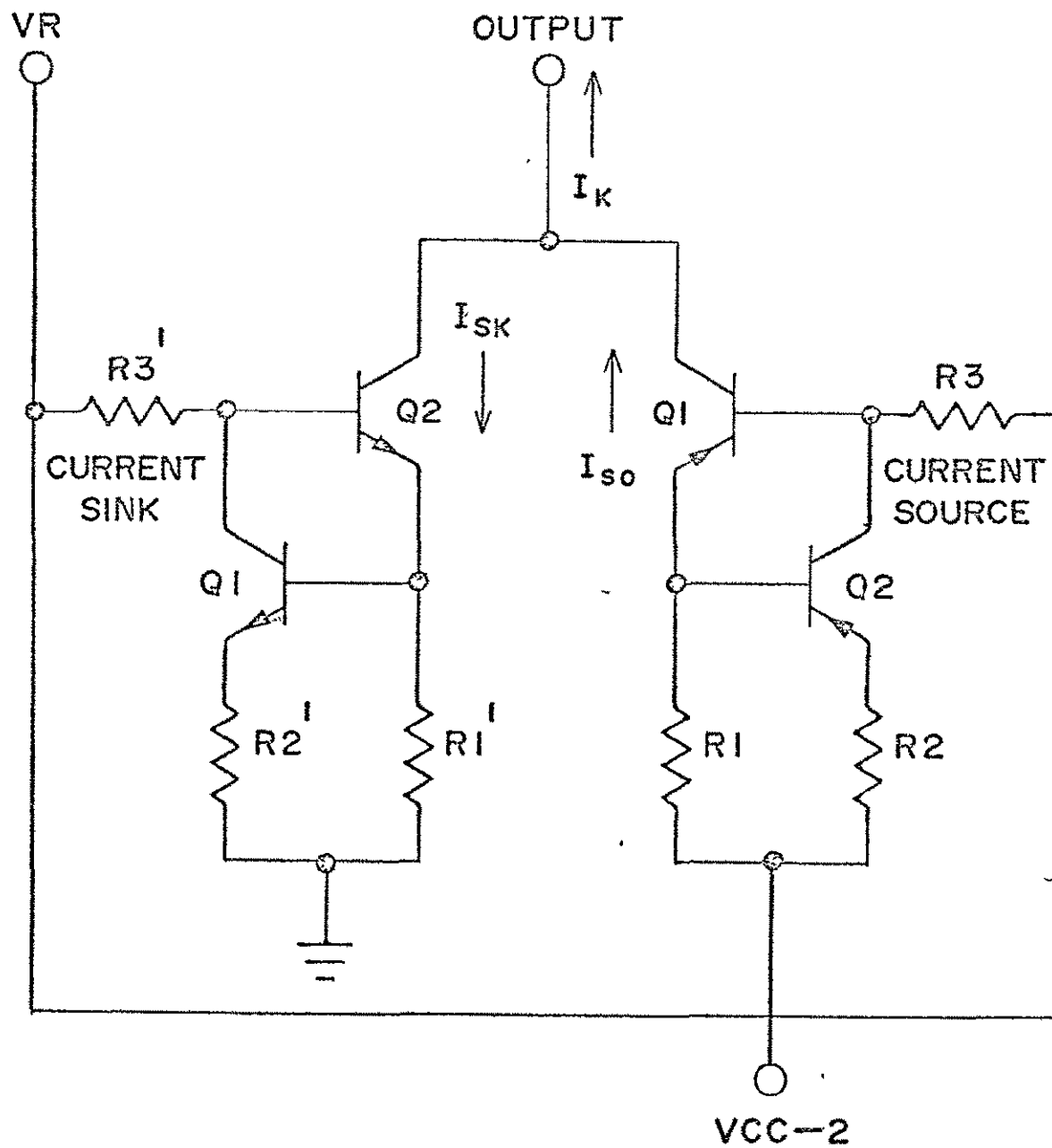


FIGURE 2 CONSTANT CURRENT SUPPLY

OSCILLATOR FREQUENCY STABILITY
VS
SINGLE CURRENT SOURCE CONTROL

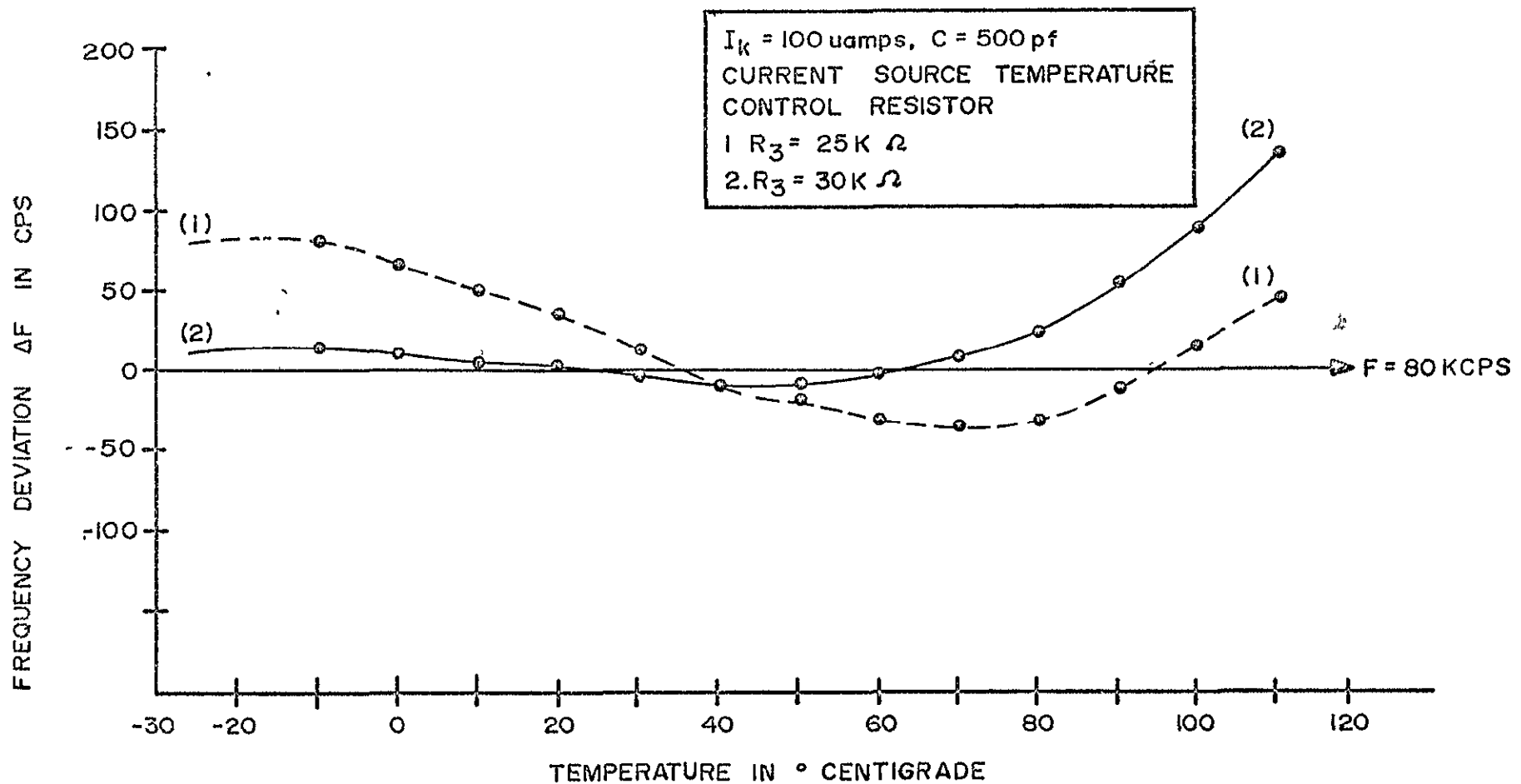


FIGURE 3 BREADBOARD OSCILLATOR FREQUENCY SENSITIVITY
TO TEMPERATURE CHANGES.

2.3.2 Comparator

The comparator's input current loading and off-set input currents required high current gain transistors ($hFE \sim 300$) to minimize output drift and to provide sufficient voltage gain for a 1.0 mV differential input voltage and a 40ns rise time. A Darlington input configuration was used to minimize the high current gain ($hFE \sim 300$) for the integrated circuit version of the comparator. As the comparator's output vs. temperature curve indicates in Figure 4, a non-linear input off-set and output voltage is obtained from the Darlington connection. However, the current source and sink working together is capable of minimizing this non-linearity as shown in Figure 5.

2.3.3 Integrators

The integrators gave excellent performance over the 135°C specified temperature range. However, the performance obtained with discrete PNP transistors will be reduced due to the reduction in the integrated lateral PNP transistor parameters, (β , hFE , I_{co}). The integrated PNP transistor will have the advantage of better parameter matching and temperature tracking.

2.3.4 Current Source

The current source had a very nearly zero temperature coefficient ($0.00067\% ^\circ C$) over the 135°C temperature range. The current source had a "near-linear" positive or negative coefficient from $-20^\circ C$ to $+80^\circ C$. At the extreme ends of the required temperature range ($-25^\circ C$ and $+110^\circ C$) transistor parameters (V_{be} , hFE , I_{co}) became the predominating factors on

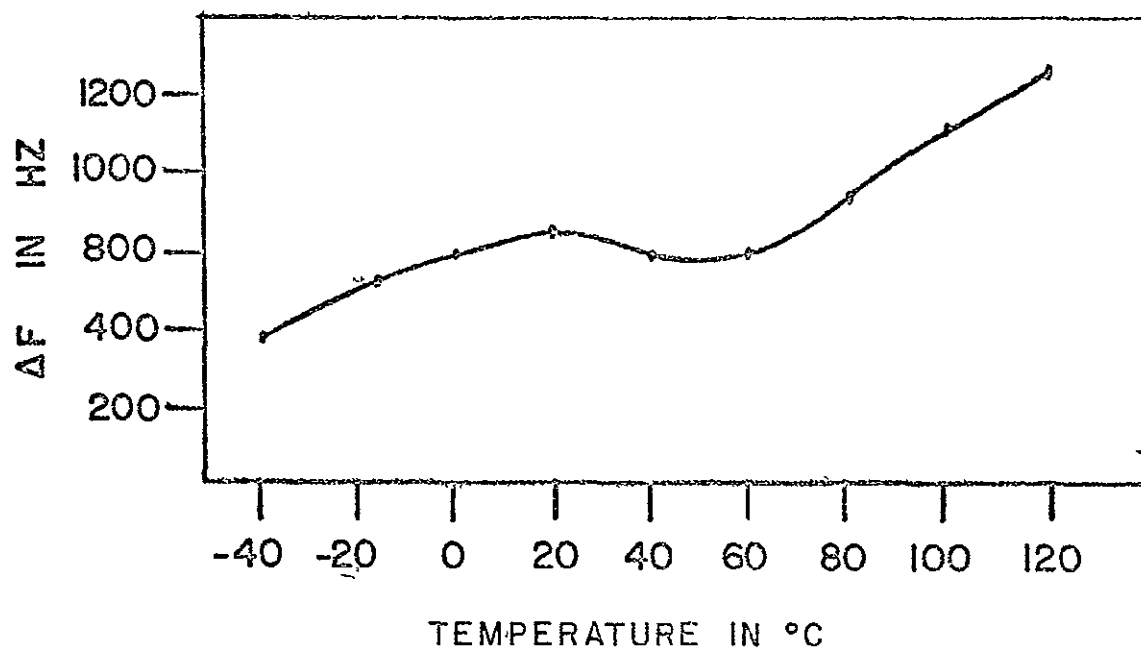


FIGURE 4 OSCILLATOR FREQUENCY STABILITY VERSUS COMPARATOR SENSITIVITY TO TEMPERATURE CHANGES.

OSCILLATOR FREQUENCY STABILITY
VS
DOUBLE CURRENT SOURCE CONTROL

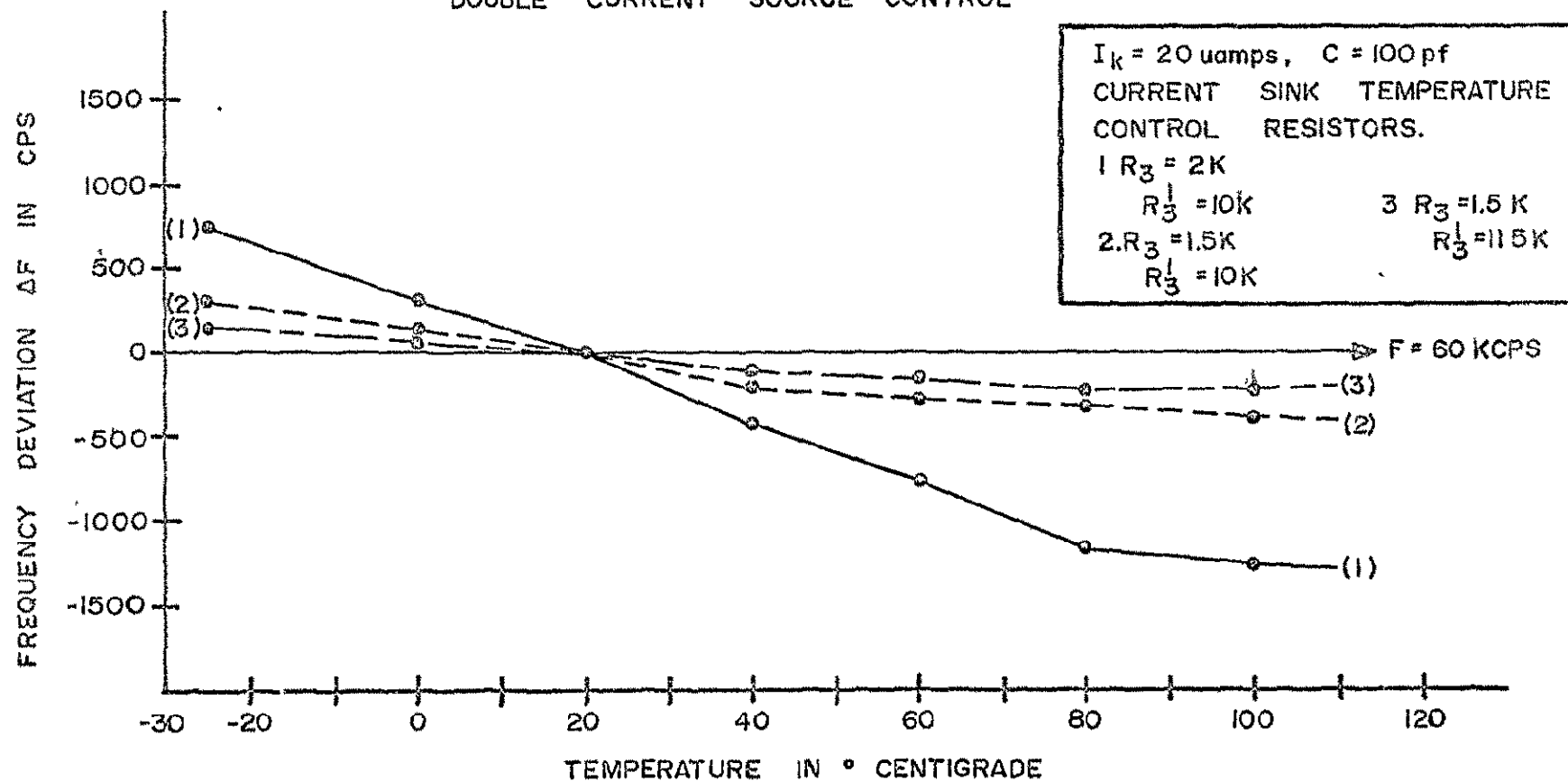


FIGURE 5

the circuit output current. At least one of the temperature extremities could be eliminated by selectively heating critical components.

2.4 Integrated Component Oscillator Performance

Successful oscillator operation was obtained from 400 Hz to 5MH by selecting the required current, timing capacitors, and the comparator reference voltage. Oscillator frequency stability vs. temperature for various current controls are shown in Figure 6.

Due to the large amount of feedback incorporated in the oscillator, external starting provisions are required. The oscillator will not start if the supply voltage is increased at a slower rate than the lowest frequency the oscillator is capable of operating. This restriction is due to the available gain in the comparator. An automatic starting circuit was designed and tested, but it was not included as a part of the final oscillator circuits in order to keep the size of the linear chip as small as possible and to obtain optimum device yields.

Presently, the oscillator can be started by momentarily shorting the current source to ground. When the "short" is removed the oscillator will start to oscillate. Essentially, the timing capacitors are discharged when the short is made. Removal of the short permits both capacitors to recharge until the comparator generates the required trigger pulse for the flip-flop, then oscillation is sustained.

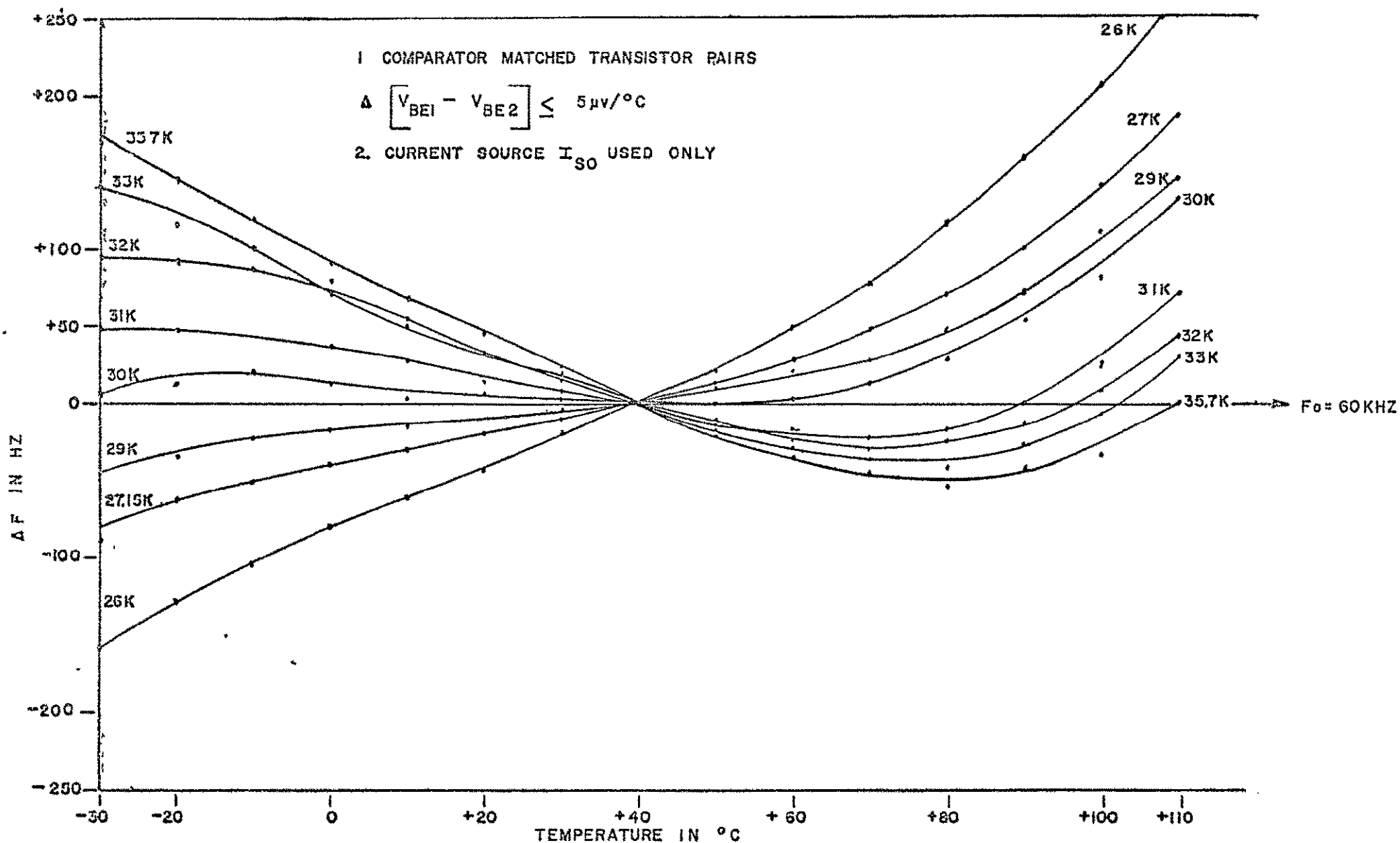


FIGURE 6 OSCILLATOR FREQUENCY STABILITY VS TEMPERATURE CHANGES FOR VARIOUS VALUES OF THE CURRENT SOURCE TEMPERATURE CONTROL RESISTOR, R13

The oscillator breadboard performance established basic guidelines for component values, tolerance, matching and tracking requirements. From the integrated circuit viewpoint, some of the parameters could be improved, while others could not be obtained. It was decided that compatible integrated components and thin film resistors should be incorporated in the breadboard phase before committing the various functional modules for monolithic integrated circuit fabrication. A master die multi-bloc that contained representative linear transistors (PNP-NPN), diodes and diffused resistor was developed. Compatible high frequency gold diffused transistors and diodes were obtained from the Electronic Component Division's circuit product line. A circuit schematic of the Multi-bloc for achieving linear components is shown in Figure 7.

2.4.1 Integrated Circuit Design

The design of the monolithic NPN transistor structures presented no technical problems except for the high current gain ($h_{FE} > 100$) requirement. Transistors that required close tracking and matched parameters were placed close together and on the same topological plane. Zener diode structures were laid out for the N^+ , P^+ "stopper" diode to ensure sharp breakdown characteristics and a low internal resistance. The lateral PNP transistor structure was selected to minimize processing constraints that are associated with the vertical PNP transistor. A compromise design was made between the relative high common emitter (h_{FE}) and constant common base (α) current gains of the lateral PNP transistor structure. The PNP

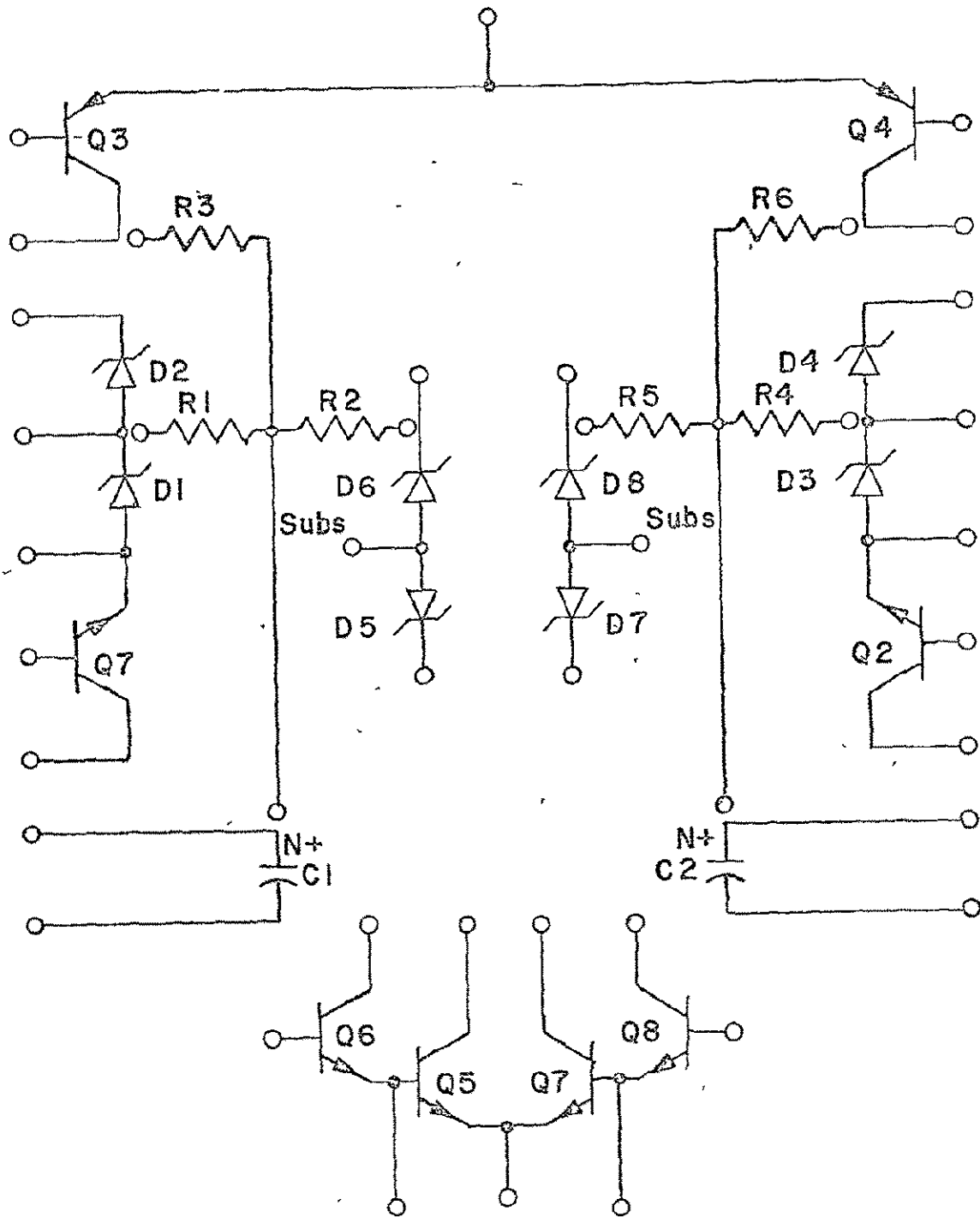


FIGURE 7 MULTI BLOCK SCHEMATIC

transistor structure and processing was set for a minimum h_{FE} of 10 and β of 0.80 at 20 to 200 microamps of collector current.

2.4.2 TaN Thin Film Resistor Design

A standard line width for resistors was used to maintain good resistor ratio tracking over the 135°C temperature range. The ratio of the largest to the smallest resistor values (aspect ratio) was set at 20 to 1. A TaN sheet resistance of 100 ohms per square was selected for the desired resistor stability of -100 ppm/°C.

2.5 Processing Difficulties

Several process runs were made before acceptable devices could be obtained from the Multi-bloc. Some of the causes for not meeting specifications were:

(a) NPN Transistors

Faulty Epitaxy: High dislocation counts in the epitaxial N-layer resulted in low NPN current gains and high leakage currents. This problem was corrected by careful wafer preparation and a more extensive evaluation of the silicon epitaxial layer.

(b) PNP Transistors

N+ Sub-Diffusion: The N+ sub-diffusion minimizes the conduction of the vertical parasitic PNP transistor associated with the lateral PNP transistor. The omission of the N+ sub-diffusion resulted in the

lateral PNP having an $h_{FE}=1$. This problem was corrected by adding the N^+ sub-diffusion in the Multi-bloc mask set.

2.6 Integrated Components and Multi-block Evaluation

Various Multi-block interconnecting patterns were used to combine the desired electrical functions on a common chip. The selected components were mounted in TO-5 packages. In addition, gold diffused switching transistors and thin film resistors were also mounted in TO-5 packages and electrically evaluated.

The oscillator was assembled with components from the Multi-bloc, thin film resistors and integrated gold diffused switching transistors. Oscillator performance obtained with the integrated components was very similar to the results obtained with discrete components.

3.0 Integrated Circuit Development

Guidelines for the integrated circuit design of the complete oscillator was established after extensive testing of the oscillator assembled with integrated components. The guidelines that were established are summarized as the following:

3.1 Component Partitioning

- a. Digital: Any part of the oscillator circuit that contains saturating circuits or where fast rise and fall times are required was considered "digital". Gold diffusion will be used on all fast switching diodes and transistors. All resistors and capacitors used in the digital section will be planar diffused structures.

- b. Linear: Any part or section of the oscillator that requires high current gain transistors or close matching of active parameters was considered "linear". Resistors that are not critical ($\pm 5\%$), and are associated with linear active devices were assigned in the linear section.

An MOS type capacitor was selected for the timing capacitor and it was assigned to the linear section.

- c. TaN Thin Film Resistors: All resistors used in the constant current supply and the oscillator frequency control will be TaN thin film type resistors that are applied to oxidized silicon substrates.

3.2 Circuit Partitioning

- a. Digital: All components in the flip flop ground switches, and part of the comparator forms the digital section. The oscillator digital section is shown schematically in Figure 8.
- b. Linear: All linear transistors, diodes and diffused resistor make up the linear section. The linear section of the oscillator is shown on Figure 9.
- c. Thin Film Resistors: The resistor section consists of all resistors used in the current source, sink and the oscillator frequency control. The resistor section is shown in Figure 10.

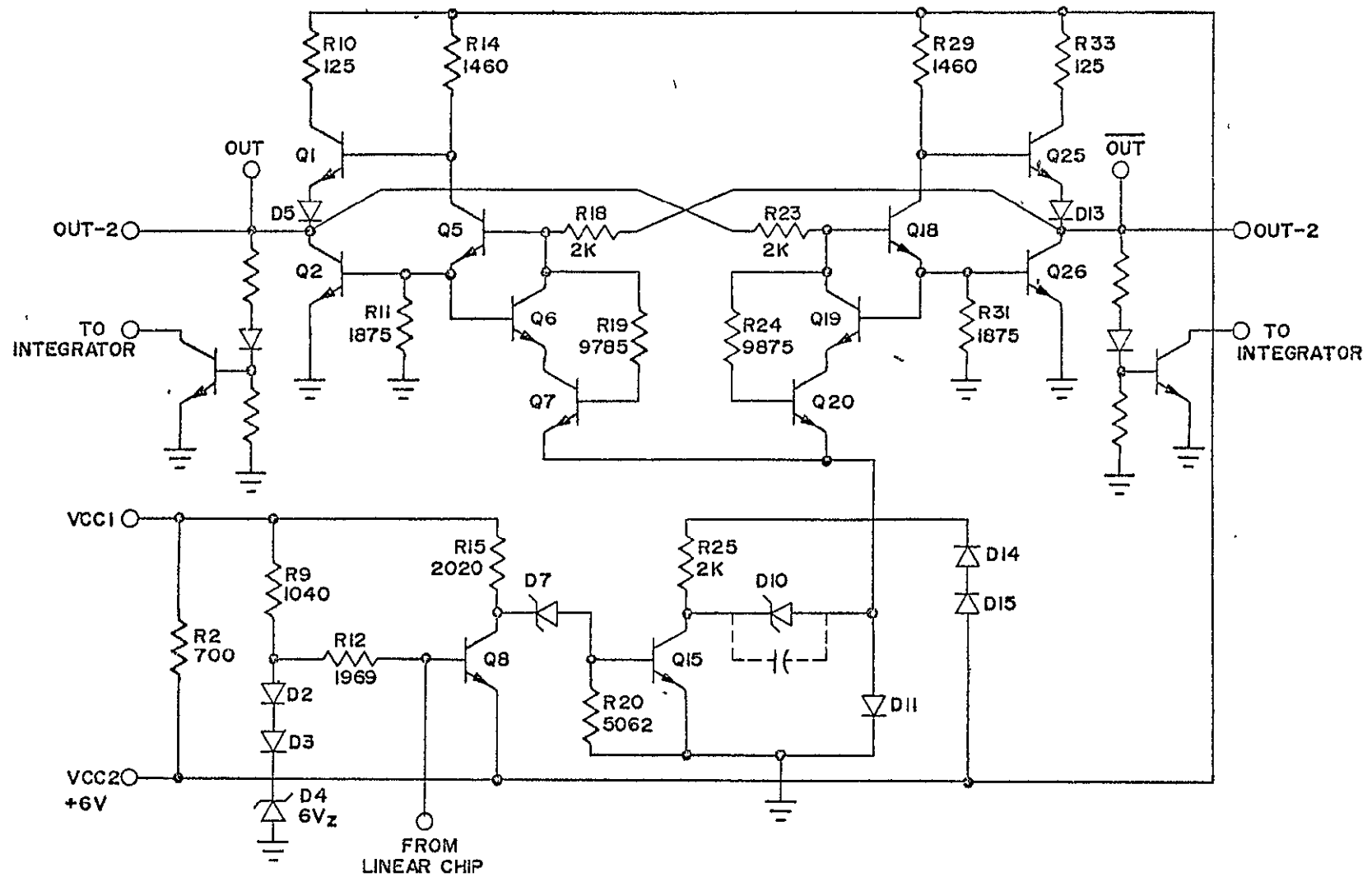


FIGURE 8 DIGITAL CHIP SCHEMATIC

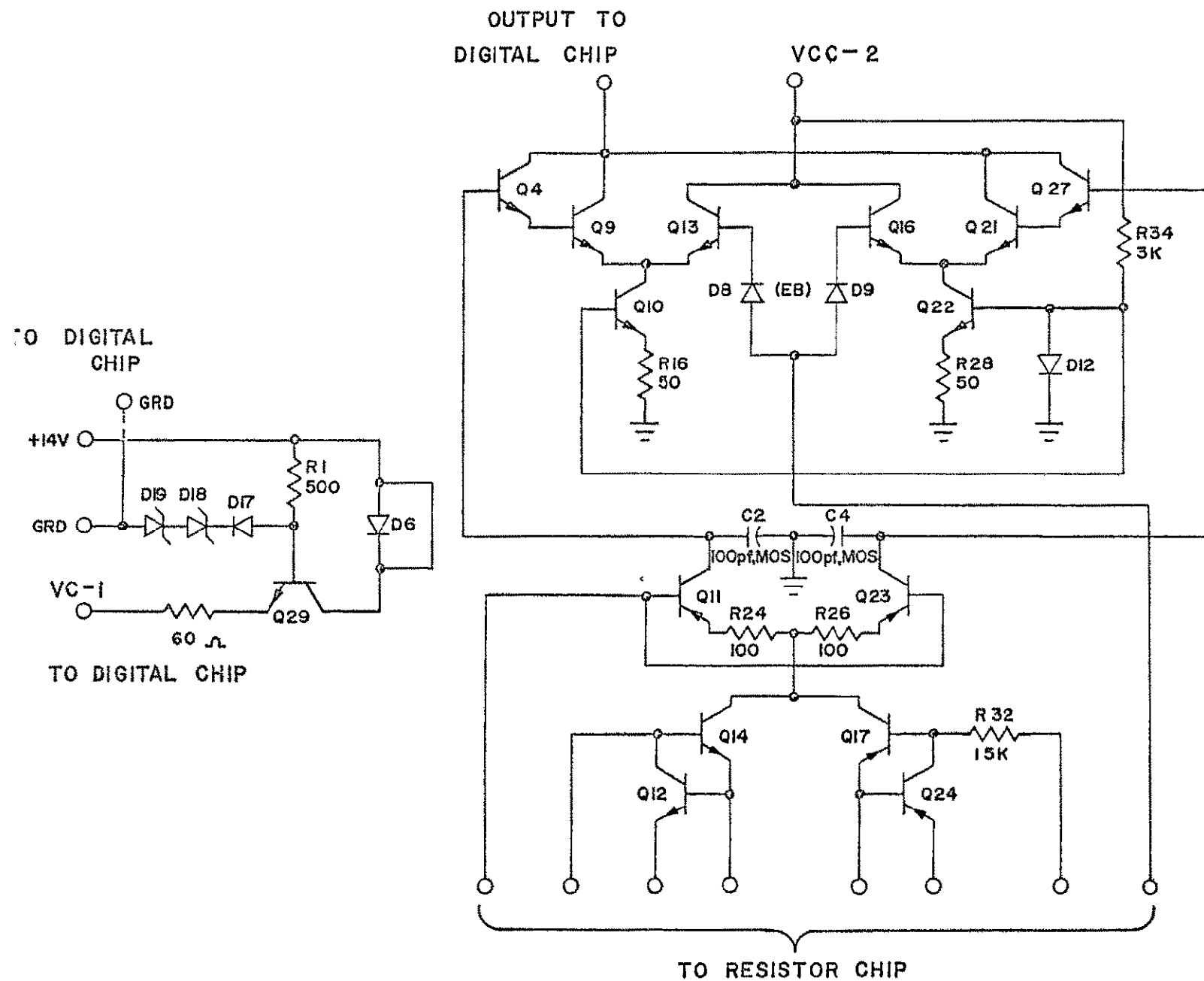


FIGURE 9 LINEAR CHIP SCHEMATIC

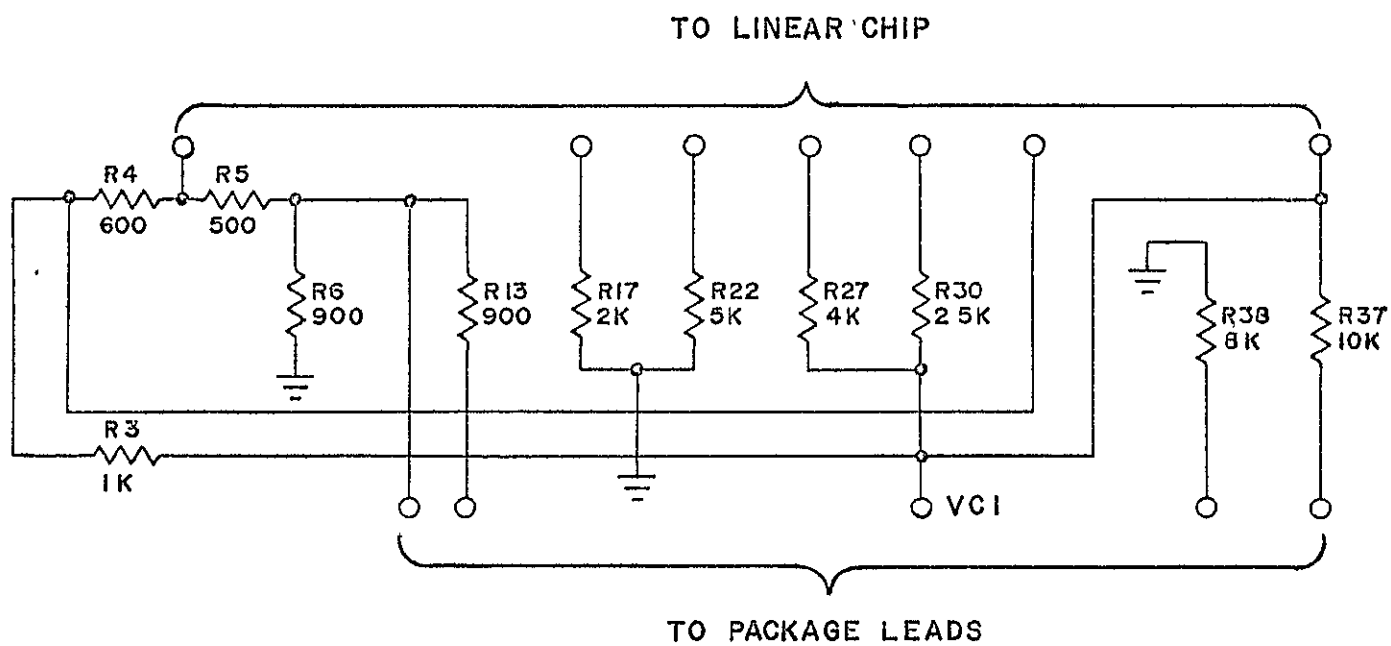


FIGURE 10 TAN RESISTOR CHIP SCHEMATIC

3.3 Integrated Circuit Chip Development

The following guidelines for the digital chip components were derived from the test results of the oscillator assembled with integrated components and proper performance of integrated, gold diffused, digital circuits.

- a. Transistor Structures: The following three device structures were used for all diodes and transistor used on the digital chip:
 - (1) single base-emitter collector, double-emitter and double collector. Double collector transistors were used for output transistors to provide low off-set voltages for different currents levels. Double emitter transistors were used where high current gain is required at higher currents.
- b. Transistor Parameters: The transistor design goals were:
 1. $h_{FE} = 20$ minimum at $I_c = 0.5$ to 10 mA.
 2. $V_{ceo} = 18$ volts minimum at $I_{co} = 100$ mA.
 3. $V_{beo} = 6$ volts minimum at $I_{bco} = 100$ mA.
 4. Switching and storage times: 10 nanoseconds.
- c. Diffused Resistors: Resistors were designed to dissipate up to a maximum of 10 mW from a nominal sheet resistance of 125 ohms/square. Resistance tolerance was set for $\pm 20\%$ and ratio tracking at $\pm 1\%$.

- d. "Stopper" Diode: The base-emitter (p+,n+) stopper diode structure was used for zener diodes and for the comparator-to-flip-flop coupling capacitor. A 6 volt breakdown voltage was the target value for the "stopper" diode.

A top view of the various device structures used on the digital and linear chips are shown on Figures 11 and 12.

3.4 Digital and Linear Chip Lay-Out

The digital chip was laid out on a 55 by 57 mil area. Aluminum conductors 0.5 mil wide were used for low current carrying lines. One mil aluminum conductors were used for high currents and up to 3 mil conductors for ground lines to minimize high voltage transients. Minimum wire bonding pad areas were set at 3 x 4 mils. A micro-photographic view of the finished digital chip is shown in Figure 13.

The area for the linear chip is approximately 77 x 80 mils and includes the timing capacitors. A photograph of the linear chip is illustrated in Figure 14.

3.5 Integrated Oscillator Interconnect Masks Design

The masks for the three oscillator chips were designed to reflect the characteristics of the discrete device bread-board and the integrated component oscillator test results. A number of interconnect mask options were incorporated in the three chips to allow for adjustments of the final circuit performance. The mask design options were the following:

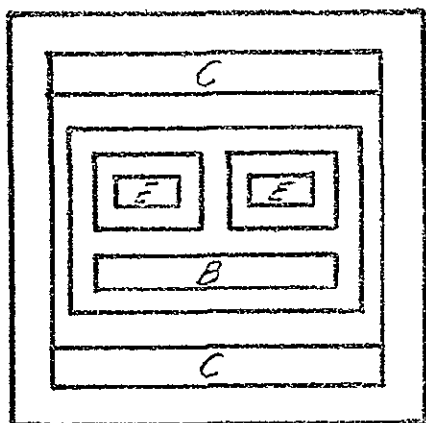


FIG. A
HIGH CURRENT, HIGH
GAIN OUTPUT NPN
TRANSISTOR
Q1, 2, 25, 26

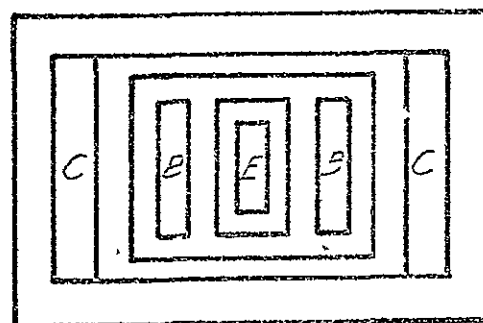


FIG. B
HIGH CURRENT GAIN
NPN TRANSISTOR
Q5, 8, 15, 18

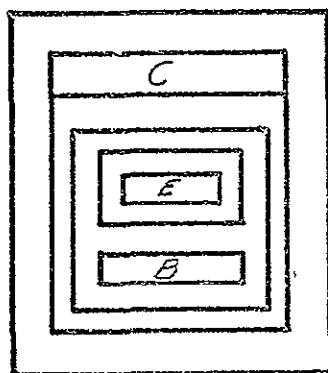


FIG. C
GENERAL PURPOSE
NPN TRANSISTOR
Q3, 6, 7, 19, 20, 28

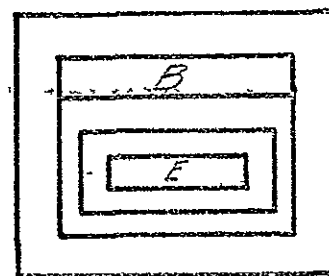


FIG. D
GENERAL PURPOSE
BASE-EMITTER DIODE
D1, 2, 3, 5, 11, 13, 14, 15, 16

FIGURE 11
SPECIAL TRANSISTOR & DIODE
STRUCTURES USED ON THE
DIGITAL CHIP

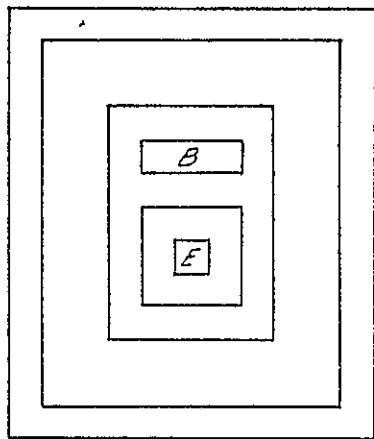


FIG. A
GENERAL PURPOSE DIODE
D8, 9, 12, 17

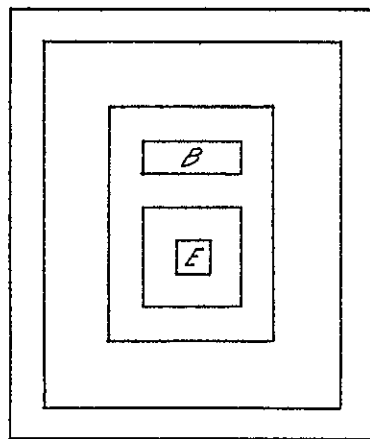


FIG. B
ZENER DIODE
D18, 19

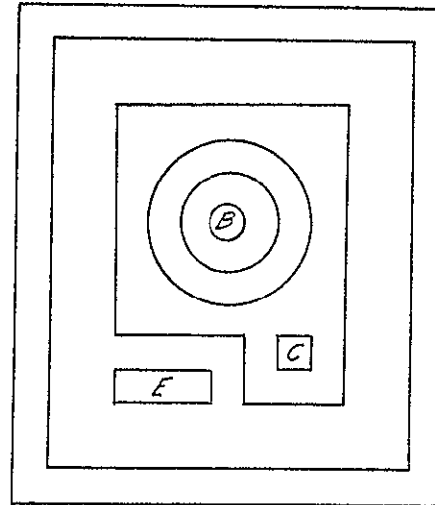


FIG. C
LATERAL PNP TRANSISTOR
Q11, 17, 23, 24

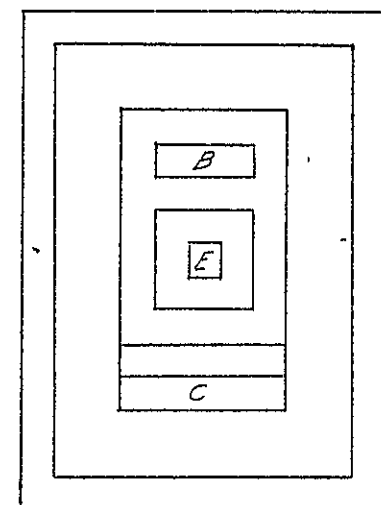


FIG. D
GEN. PURPOSE NPN TSTR
Q10, 12, 14, 22

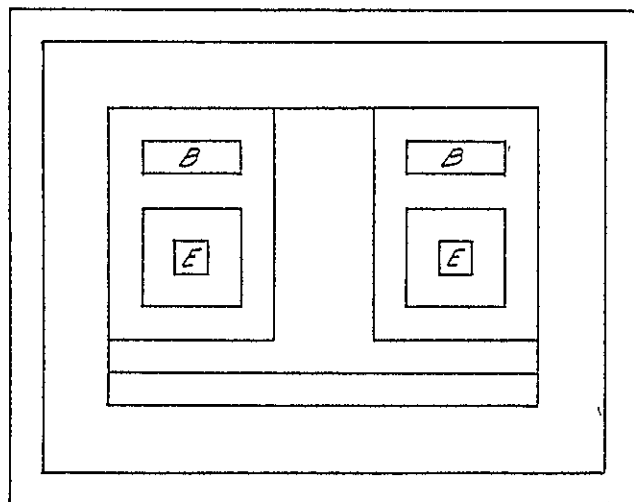


FIG. E
MATCHED NPN TRANSISTOR PAIR
Q13, 16

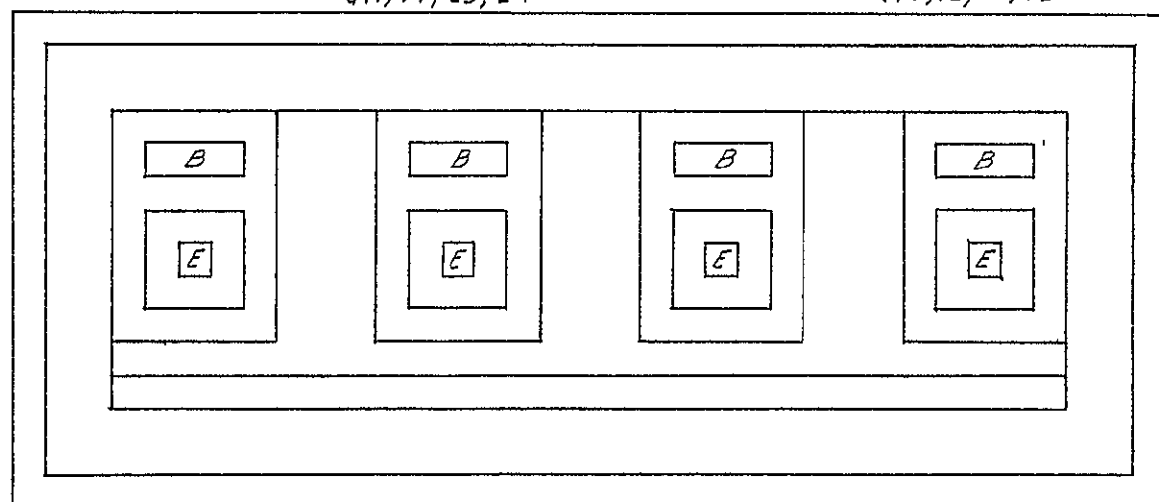


FIG. F
MATCHED NPN QUAD TRANSISTOR
Q4, 9, 21, 27

FIGURE 12
SPECIAL TRANSISTOR & DIODE STRUCTURES
USED ON LINEAR CHIP

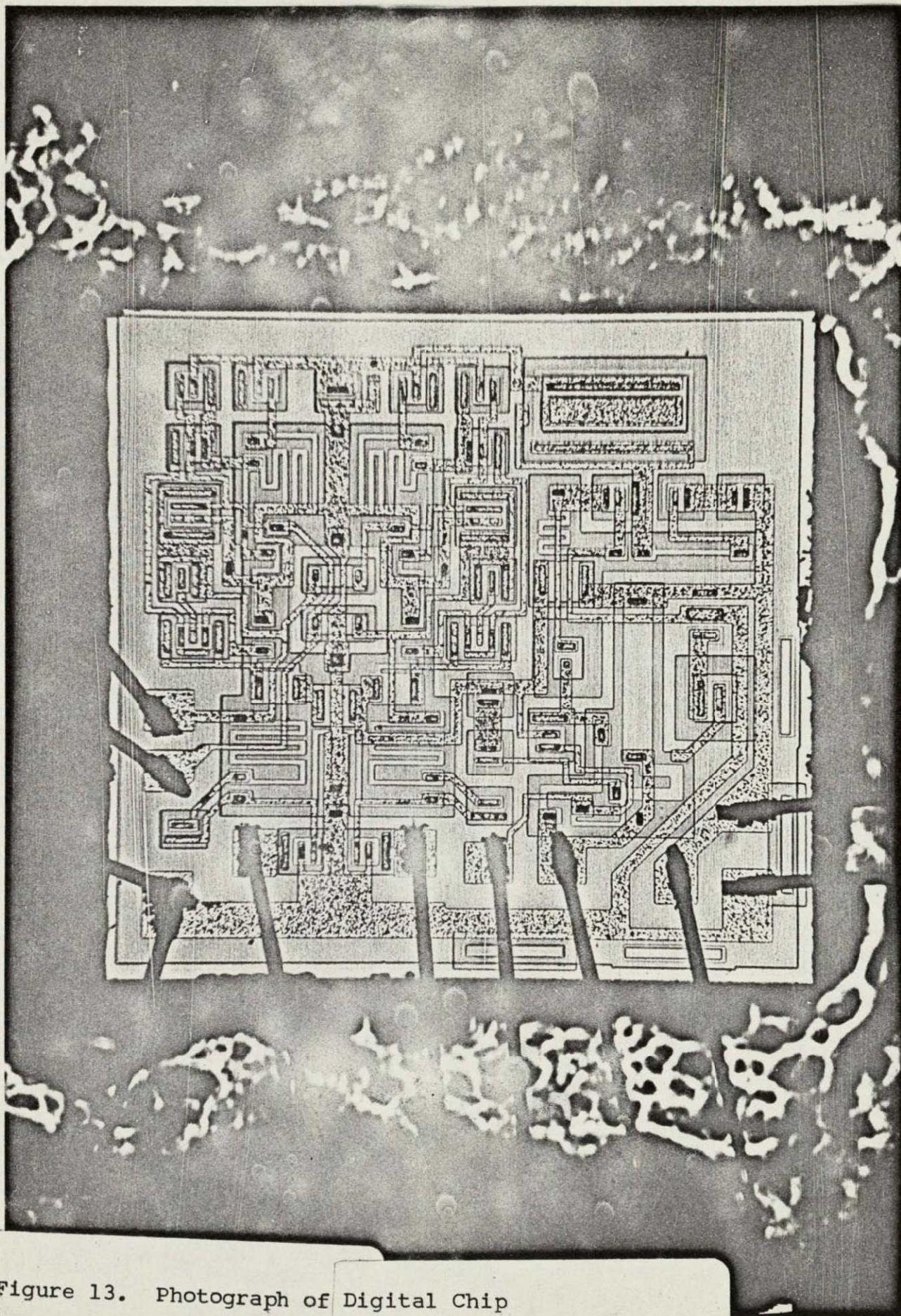


Figure 13. Photograph of Digital Chip

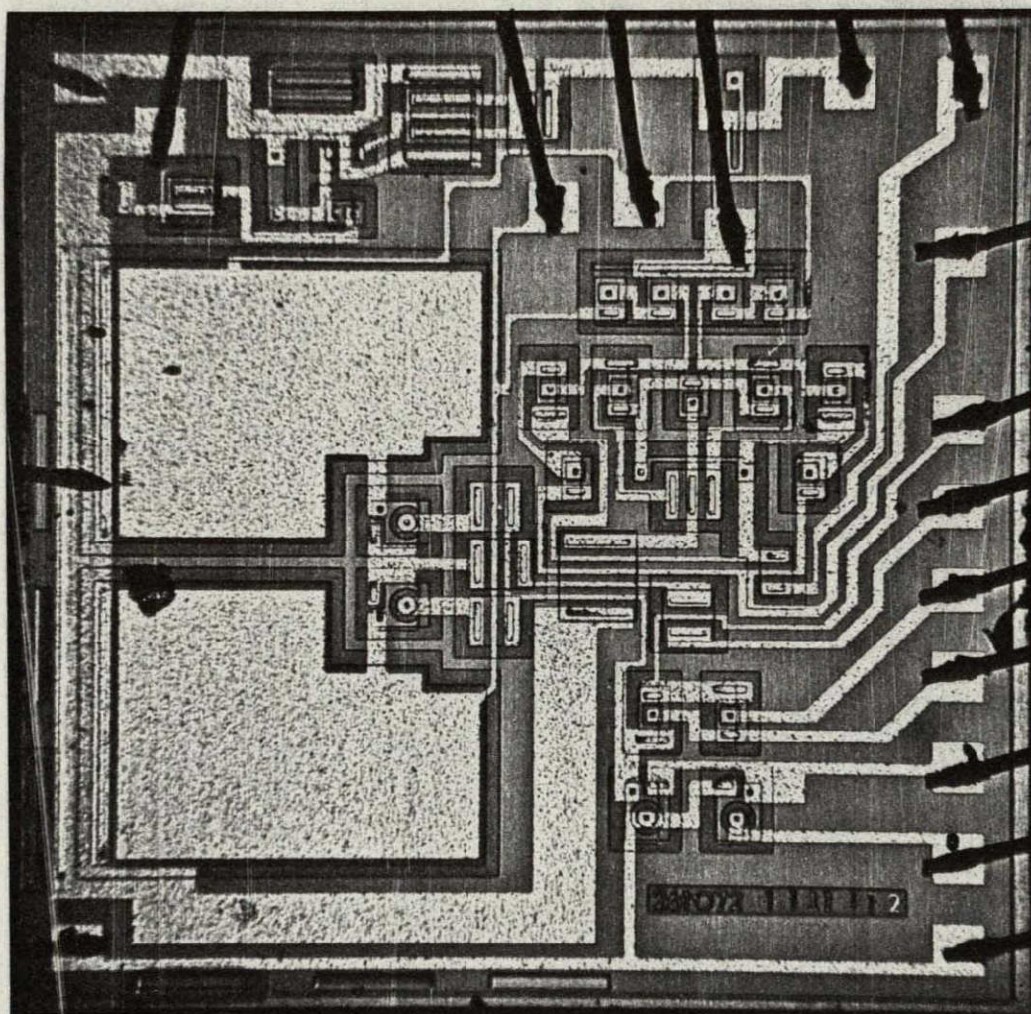


Figure 14. Photograph of Linear Chip

1. Comparator to Flip Flop Coupling Capacitor:

Provisions were made to use the top or side wall capacitance of the base-emitter stopper diode (CR_1O) structure. Each diode component contains approximately 30 pf of capacitance. The flip-flop switching speed is related to the comparator output voltage amplitude and the fall time.

2. Current Limiting Resistor and Supply Polarity Protection Diode:

Mask provisions were made to connect resistor R13 to limit the oscillator current to 17 mA. When $V_{cc} = +13$ volts is applied. A mask option was provided for using the oscillator protective diode CR6 for reverse supply voltage connections. The diode is not used in the final circuit due to excessive PNP parasitic leakage currents. The parasitic PNP transistor current could be minimized by adding a N+ subdiffusion under the diode.

3. Thin Film Resistor Chip:

The resistor chip has several resistor tap options for obtaining various resistor value combinations. The major resistor tap is used in the current sink temperature coefficient control resistor, R13. Actually, each resistor is made up of several thin film sections that can be used to increase resistor values.

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Because TaN resistors can only be increased in value by the oxidation trimming process, provisions for reducing a resistor can be accomplished by shorting sections of the resistor. It was determined during the integrated component oscillator evaluation test, that an oscillator could have either a positive or negative frequency temperature coefficient. Hence, the current supply I_k includes provisions for controlling positive or negative oscillator frequency changes.

4.0 Oscillator Test Results:

The first integrated circuit oscillator samples operated at lower frequencies than expected 1.0 KHz and had inadequate temperature stability. The low oscillator frequency and the poor temperature stability were attributed to the low PNP transistor current gains, h_{FE} and Alpha. Processing changes were made to increase the current gains of the PNP transistors without adversely reducing the NPN transistor current gains. The following compromises in current gains for the PNP and NPN transistors were made, even though the compromised values were below target values.

Current Gain	PNP	NPN
h_{FE}	10 minimum $I_c = 100 \mu A$	100 minimum $I_C = 100 \mu A$
α	0.80 $I_c = 100 \mu A$	0.98 $I_c = 100 \mu A$
V_{CEO}	20 Volts $I_{co} = \mu A$ max	20 Volts $I_{co} = \mu A$ max.

Table 2. Linear IC chip PNP and NPN Transistor Current Gain Specifications

It was also determined that transistor base to emitter voltage V_{be} matching and tracking varied approximately 20% across the diffused linear silicon wafer. These variations in current gains on the linear wafers required changes in the thin film resistor chip design in order to individually trim the resistors that controlled oscillator frequency. The major transistor parameter problem on the linear chip was non-linear V_{be} tracking over the required operating temperature range. Examples of NPN transistor V_{be} tracking are shown in Figure 15. The most critical aspect of V_{be} tracking is the non-linear changes in oscillator stability due to the non-linear V_{be} in the transistor⁶ is used in the comparator.

1.1 Integrated Circuit Analysis

The effective voltage used in the frequency defining function is determined by: (1) voltage across the timing capacitor (V_t); (2) comparator reference voltage (V_R); (3) the differential voltage at the comparator inputs. The effect of change in the effective timing voltage on frequency is determined from the formula given in equation 6. An example of oscillator frequency changes due to the differential changes in V_{be} over the operating temperature range, based on values shown on Figure 15, curve 3 illustrates the need for good V_{be} differential tracking. Since there are effectively four (4) base-emitters diodes in the comparator input circuit, the V_{be} off-set voltage is increased by a factor of 4.

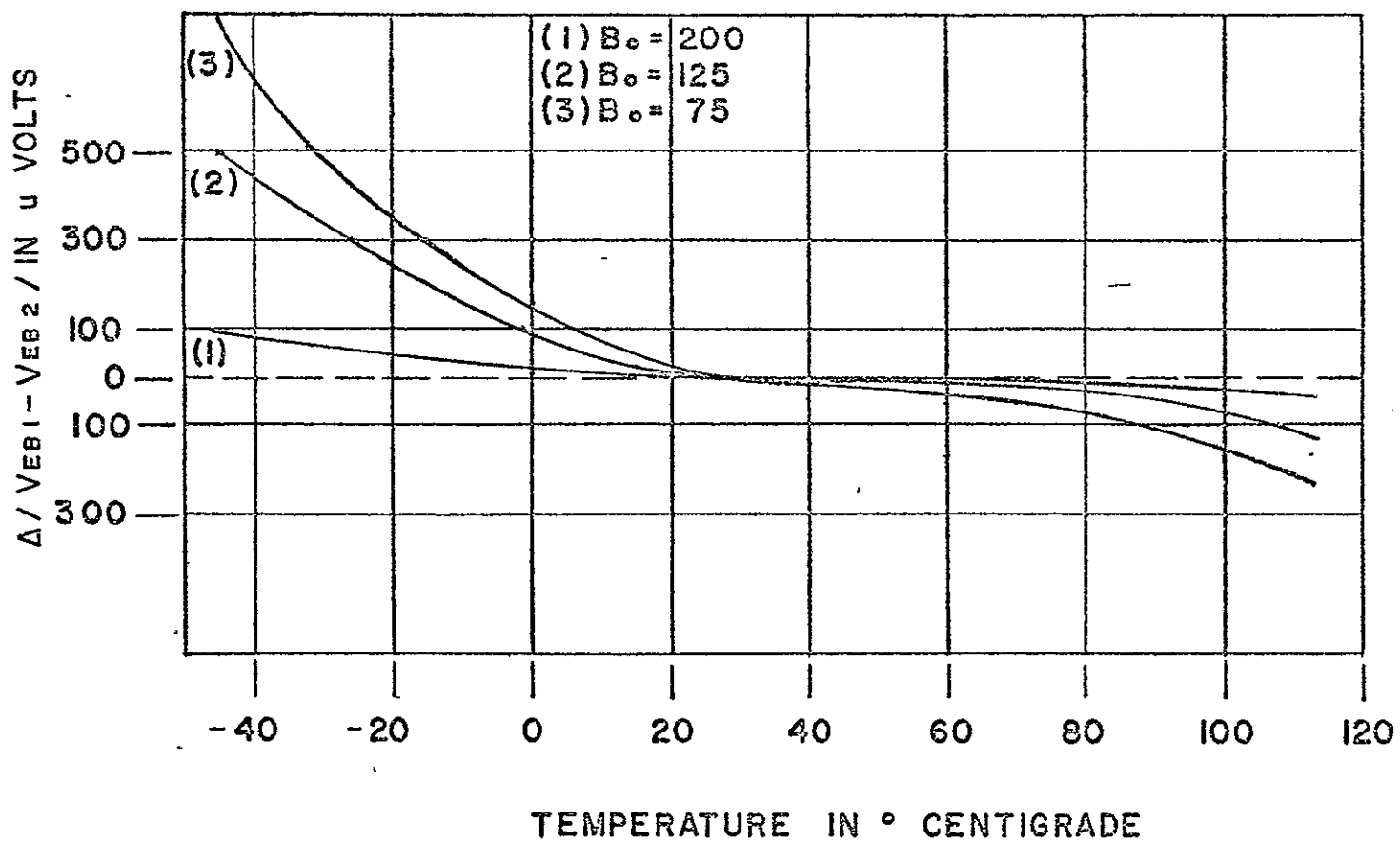


FIGURE 15 DIFFERENTIAL V_{BE} VS TEMPERATURE FOR MATCHED TRANSISTOR PAIRS.

Applying equation 9A for F ,

$$\Delta F = - \left[\frac{I_k}{2C_T V_T} \right] \left[\frac{\Delta V(t)}{V_T} \right] \text{ Hz}$$

$$\Delta F = - \left[\frac{50 \times 10^{-6}}{2 \times 120 \times 10^{-12} \times 2} \right] \times \left[\frac{4 \times 1000 \times 10^{-6}}{2} \right]$$

$$\Delta F = -227 \text{ Hz}$$

The current supply I_k had a small positive temperature coefficient, thus increasing the oscillator frequency deviation. The oscillator frequency deviation was improved as shown on Figure 16 B by adjusting the current supply I_k for a negative temperature coefficient. It can be observed, however, that the positive and negative frequency deviations below and above $+40^\circ\text{C}$ cannot be corrected by the current supply input. It can be seen from the analysis given that the ideal differential V_{be} curve shown in Figure 15 is curve 1. It was determined that the transistor gain for curve 1 had a h_{FE} of 160. The frequency deviation resulting from curve 1 of Figure 15 would be

$$\Delta F = - \left[\frac{50 \times 10^{-6}}{2 \times 1.2 \times 10^{-10} \times 2} \right] \times \left[\frac{4 \times 125 \times 10^{-6}}{2} \right] = 26 \text{ Hz}$$

The 26 Hz could be reduced approximately by one half by adjusting the current supply I_k for a negative temperature coefficient.

4.1.1 Common Mode Voltage

A second factor that contributes to the oscillator frequency deviation is the positive temperature coefficient associated with the reference zener diode CR4 (See Figure 10.) The voltage across the zener diode increases approximately $1.2 \text{ mV}/^\circ\text{C}$.

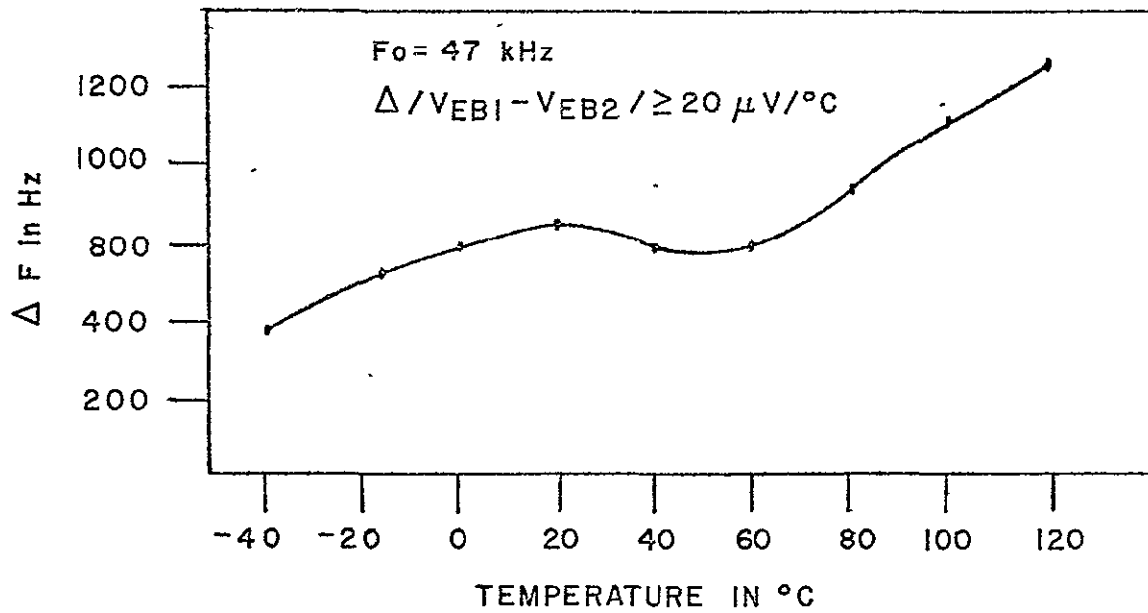


FIGURE 16A OSCILLATOR ADJUSTED FOR SMALL POSITIVE TEMPERATURE COEFFICIENT

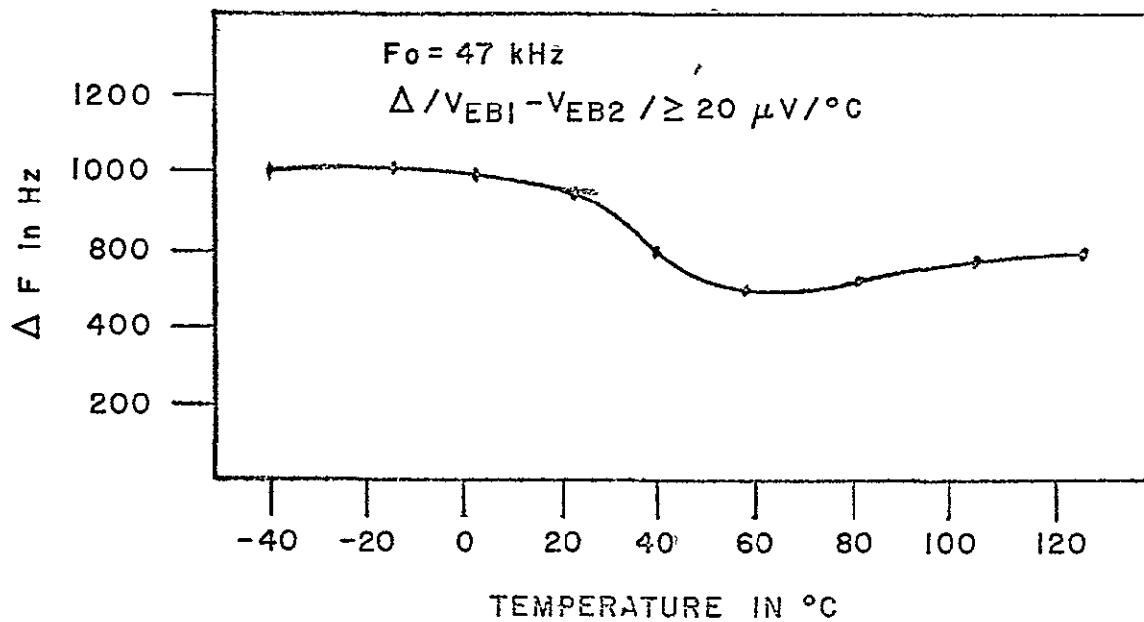


FIGURE 16B OSCILLATOR ADJUSTED FOR NEGATIVE TEMPERATURE COEFFICIENT

Resistor values selected for the current supply bias divider were not optimized to minimize the common mode voltage derived from the reference zener diode.

4.2.0 Oscillator Operation Versus Temperature

Several oscillators operated at low temperatures (-25°C) but not at $+110^{\circ}\text{C}$, while some oscillators operated at $+110^{\circ}\text{C}$ but not at -25°C .

4.2.1 Analysis

A comparator output slewing rate of 10^3 volts/ μsec is required to trigger the flip flop. The 1.0 mA current supply for the comparator section on the linear chip will provide a 2 volt/ μsec slewing rate if the NPN transistors have a β_0 of 60. The voltage gain of the two stage amplifier comparator section on the digital chip increases the final slewing rate to 10^3 volts/ μsec required to trigger the flip flop. Oscillator failures at high temperatures are due to the leakage current through the level shifting zener diode CR7 and the collector base leakage current I_{co} from Q15. The sum of leakage currents from CR7 and Q15 causes a voltage to be developed across resistor R20 sufficiently to partly turn on Q15. If Q15 is partly turned on, the required voltage gain cannot be obtained for the required 10^3 volt/ μsec slewing rate necessary to trigger the flip flop. Hence, the oscillator fails to operate. This problem could be corrected by decreasing the value of R20, or by adding a forward conducting diode in series with CR7, or by reducing the voltage across R15. To add the diode or decrease R20 requires a

complete change in the digital chip mask sets. A more practical correction is to decrease the 12 volts across R15 by reducing the input voltage and connecting an external resistor to the 6 volt reference diode CR4 to supply the required current for the oscillator. However, the oscillator frequency will change for changes in the supply voltage.

The decrease in npn current gain in the comparator section of the linear chip caused some oscillator circuits to stop operating at the low temperatures.

5.0 PACKAGING

The three silicon chips that make up the oscillator were mounted in a 3/8 by 3/8 inch hermetically sealed flat pack. A 3/8 by 1/4 inch flat pack has adequate area for the three oscillator chips but to minimize thermal problems at elevated temperatures a 3/8 by 3/8 inch flat pack was used. A photograph of assembled oscillator before lid attachment is shown on Figure 17.

5.1 Assembly

An assembly drawing of the three oscillator chips and wire bonding schedule is shown on Figure 18. Gold-silicon preforms were used for die bonding. An ultrasonic wire bonder was used to bond the one mil aluminum wires to the three chips and to the package leads.

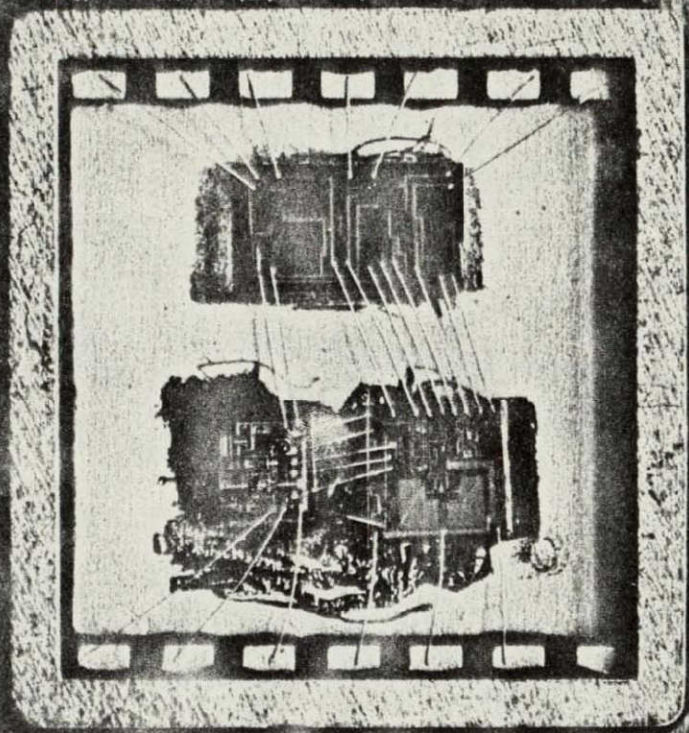
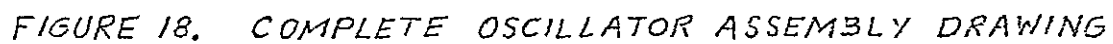


Figure 17. Photograph of Assembled Oscillator



5.2 Test

A typical assembled oscillator test set-up is shown in Figure 18. A list of package pin connections for oscillator operation is shown on Table 3.

<u>PIN NO.</u>	<u>SIGNAL</u>
1	Output-1
2	Output-2
3	Ground
4	Supply Voltage ($V_{cc} = 10 \pm 2$ volts)
5	Ground
6	No Connection Required
7	Unused
8	Internal Reference Voltage $V_{cc} = 5.5 \pm 0.2$ volts
9	No Connection Required
10-11	Connected Together
12-13-14	Connected Together

Table 3. Oscillator Package Pin Connections

5.2.1 Oscillator Frequency Range Adjustment

The oscillator frequency can be increased or decreased by connecting an external resistor as follows:

- a. To increase the oscillator frequency connect the external resistor from pins 12, 13 and 14 which are shorted together, to pin 3. The external resistor should have a minimum value of 10 K ohms and have a temperature stability of 20 ppm.

- b. To decrease the oscillator frequency, connect an external resistor from pins 12, 13 and 14 which are shorted together, to pin 8. The resistor should have a minimum value of 10K ohms and have a maximum temperature stability of 20 ppm.
- c. The oscillator frequency can be modulated by connecting an external voltage, (0 to + 5 volt) through a 10K ohm resistor. If the external voltage source is not a D.C. voltage, the frequency is limited to 4 KHz, for a normal center frequency of 20 KHz.

5.2.2 Oscillator Frequency Stability Adjustment

The oscillator frequency sensitivity to changes in temperature can be adjusted by connecting an external resistor as follows:

- a. Positive Temperature Coefficient Correction

Oscillators with a positive temperature, (increasing frequency changes for increasing temperature changes) coefficients can be adjusted to minimize frequency changes by connecting an external resistor from pins 9 to pins 10 and 11. The external resistor should have a minimum value of 1.0 K ohm and a temperature stability of 20 ppm.

b. Negative Temperature Coefficient Correction

Oscillators with negative temperature coefficients can be adjusted for minimum frequency changes by connecting an external resistor (initial jumper from pins 10 and 11 removed) from pin 10 to 11. The external resistor should have a maximum value of 1.0 K ohm and a temperature stability of 20 ppm.

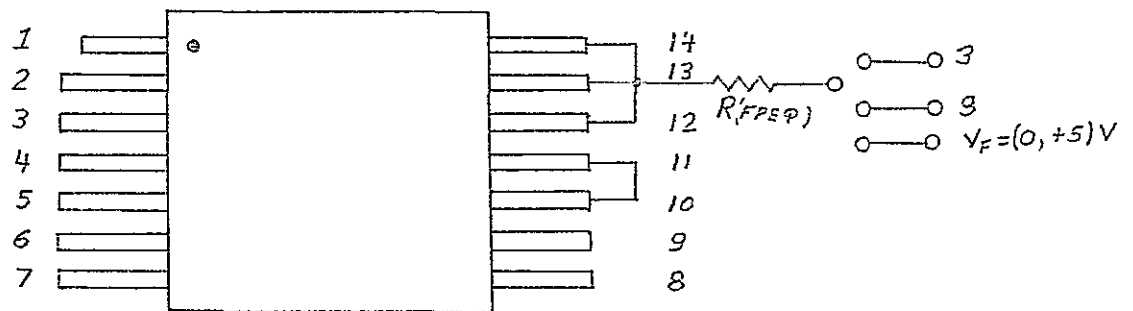


Figure 19a. Frequency Adjustment

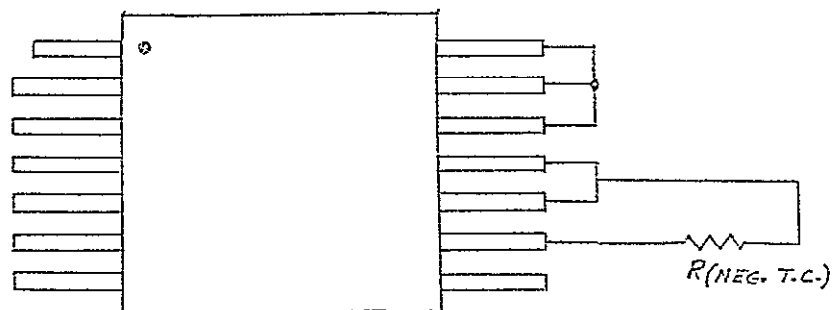


Figure 19b. Negative Temperature Coefficient Adjustment

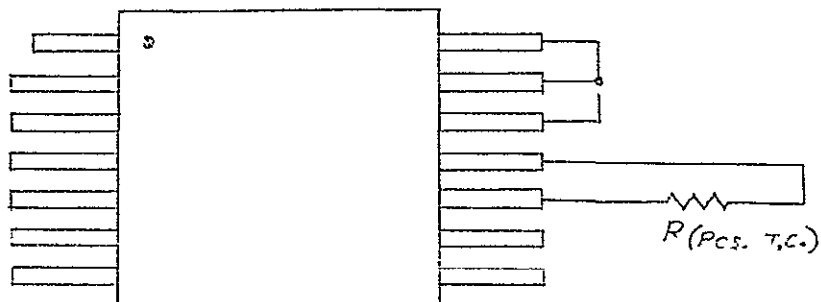


Figure 19c. Positive Temperature Coefficient Adjustment

Figure 19. Oscillator Test Set-up for Frequency, Positive and Negative Temperature Coefficient Adjustments.

6.0 CONCLUSIONS AND RECOMMENDATIONS

The oscillator developed during this program, using the integrated circuit and compatible thin film resistor techniques, establishes the basic circuitry and integrated circuit guidelines for an oscillator based on the concept of independent generation of oscillator parameters. The oscillator that was developed had a near zero temperature coefficient over a specific (80°C) temperature range. For example, on a 20 KHz oscillator, a change of 100 hertz over an 80°C temperature range was typical.

6.1 Mathematical Prediction Model

The integrated circuit oscillator test results indicates that 10% oscillator performance can be predicted based on individual frequency defining parameters. This approach eliminates many of the "cut-and-try design" techniques due to the inherent temperature coefficients, hard-to-predict parasitic capacitance effects, and non-linearities in the component elements.

6.2 Non-linear Voltage Parameter:

The nonlinearities in the oscillator was due primarily to the effective voltage parameter $V(t)$. Even though the constant current supply I_k and timing capacitor C_T maintained a nearly linear timing voltage ($V(t)$) the voltage comparator introduced a nonlinearity factor due to poor differential tracking ($\Delta / V_{be1} - V_{be2}$) at its inputs. This problem can be corrected by using either one or a combination of the two approaches listed as follows:

- a. Higher Gain Transistors: By using transistors in the comparator inputs with hFE of 200 or higher, the comparator input differential off-set voltage (ΔV_{be}) can be held to less than $5 \mu V/^{\circ}C$. As shown previously, when ΔV_{be} is approximately $5 \mu V/^{\circ}C$ the matched transistors will track linearly over a $125^{\circ}C$ temperature range.
- b. Operate Comparator Over Limited Temperature Range: As shown in Figure 16, the change in slope of ΔV_{be} tracking occurs at approximately $+30^{\circ}C$. Therefore, if the matched transistors are operated above $40^{\circ}C$ a 50 percent improvement in ΔV_{be} tracking is obtained. The adjustable temperature coefficient of the current supply I_k can be adjusted to optimize the remaining nonlinear effects on oscillator performance. An improvement of better than 50 percent is anticipated in the overall oscillator frequency stability characteristic.
- Critical areas in the comparator could be held above $+40^{\circ}C$ by using components that are temperature controlled. This approach would not require heating the three chips that make up the oscillator and save wasted operating power. This is one of the advantages of constructing the oscillator with independent parameter controls.

5.3 High-Low Temperature Problems:

The problems relating to the oscillator failure to operate at the high and low temperatures can be corrected by simply changing component values, and increasing transistor betas in the comparator.

a. High Temperature: By reducing the value of resistor R_{20} , the leakage currents from diode D_7 and transistor Q_{15} will insure reliable oscillator operation at $+110^{\circ}\text{C}$. A diode can be added in series with D_7 to provide an additional safety factor for excess leakage currents.

b. Low Temperatures: By increasing the betas of transistors on the comparator the oscillator will operate successfully over the low temperature range. A comparator output voltage slewing rate of $100\text{V}/\mu\text{S}$ is required to trigger the flip flop. This requires that transistors in the linear section of the comparator have a minimum B_o of 100 for reliable oscillator operation at -30°C .

5.4 Oscillator Start-Up

An automatic oscillator start-up circuit is shown in Figure 20. This circuit can be added internally or externally. The start-up circuit will require approximately 10 square mils of chip areas and consume approximately 20 mw of power.

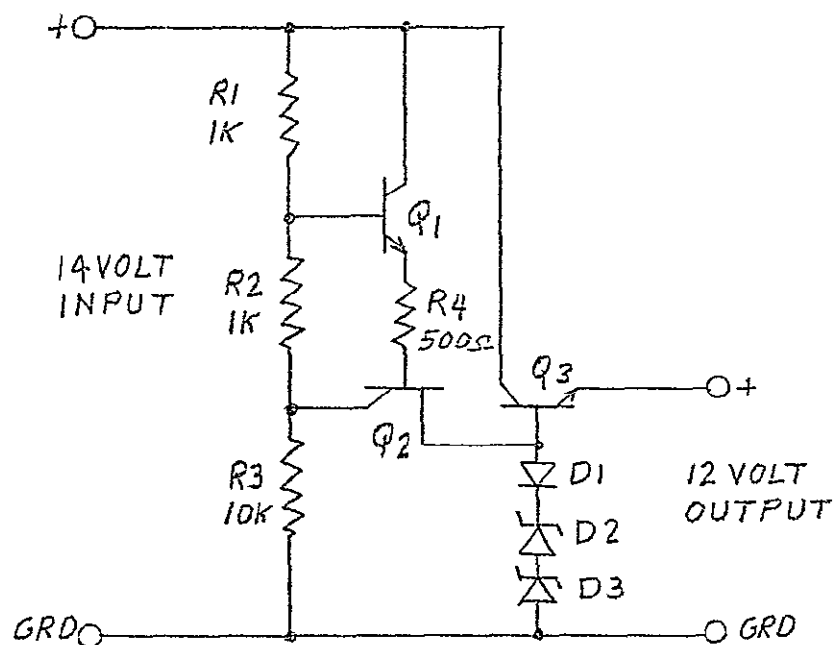


FIGURE 20 STARTER-REGULATOR CIRCUIT

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3. W. J. Stebbins, R. C. Gallagher, M. N. Giuliano, "Techniques for Temperature Stabilizing a Sure Starting Microelectronic Astable Multivibrator," Proceedings Fifth Annual Microelectronics Symposium, July 1966
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APPENDIX A

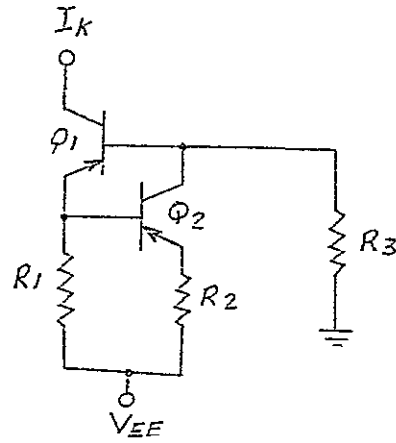


FIGURE 1. CONSTANT CURRENT SOURCE SCHEMATIC

A general solution, in closed form, for output current I_K is derived from the following generalizations:

$$\text{defining } V_{e1} = V_{ee} - (I_{e1} - I_{b2}) R_1 \quad (1)$$

$$I_{e1} = \frac{V_{ee} - V_{e1}}{R_1} + I_{b2} \quad (2)$$

$$V_{c2} = (\beta I_{e2} + I_{b1}) R_3 \quad (3)$$

$$V_{c2} = V_{e1} - V_{be1} \quad (4)$$

$$I_{e2} = \frac{V_{ee} - (V_{e1} + V_{be2})}{R_2} \quad (5)$$

after some algebra manipulations it is possible to show that,

$$\begin{aligned} I_{e1} = & \left[\frac{R_3 V_{ee}}{R_1 R_2 + \beta R_1 R_3} \right] + I_{b2} \left[\frac{(R_1 R_3 + R_1 R_2)}{R_1 R_2 + \beta R_1 R_3} \right] - \left[\frac{\beta I_{b1} R_2 R_3}{R_1 R_2 + \beta R_1 R_3} \right] \\ & + \left[\frac{2 R_2 V_{be2}}{R_1 R_2 + \beta R_1 R_3} \right] - \left[\frac{R_2 V_{be1}}{R_1 R_2 + \beta R_1 R_3} \right] \end{aligned} \quad (6)$$

A minimum solution to the inequality is to make

$$R_3 = K_3 R_2 \quad (21)$$

where $1 < K_3 < 2$

It is well to note that $I_{e1} \approx I_{e2}$ is required for good V_{be} tracking between Q_1 and Q_2 . Therefore, from (7) R_1 , R_2 and R_3 are required to be adjusted as the following:

$$I_{e1} = \frac{V_{ee}}{R_1} \left(\frac{1}{1 + \frac{2 R_2}{R_3}} \right) \quad (22)$$

$$\text{but } I_k = \angle I_{e1} = \frac{V_{ee}}{R_1} \left(\frac{2}{1 + \frac{2 R_2}{R_3}} \right) \quad (23)$$

and from (2) and (5) it can be shown that

$$R_1 = R_2 \left[\frac{1 + \frac{R_1 I_{b2}}{V_{be2}}}{1 - \frac{V_{be2}}{V_{ee} - V_{e1}}} \right] \approx \left(\frac{1}{1 - K_4 V_{be2}} \right) R_2 \quad (24)$$

Test data obtained from the circuit indicates that K_4 will vary between the limits,

$$1 < K_4 < 2 \quad (25)$$

The absolute values of resistors R_1 , R_2 and R_3 can be reduced, for a given output current I_k , by connecting R_3 to a positive voltage V_{bb} as shown in Figure 2. Resistor values can be reduced in proportion to the absolute difference voltage as the following:

$$R_n^1 \approx \frac{R_n}{V_{EE} - V_{BB}}$$

If it is desirable that I_k have a negative temperature coefficient, then from (16) the relationship between R_2 and R_3 can be redefined as

$$R_3^1 > R_2 > R_3 \quad (19)$$

since $R_3 = R_2$, we get the inversion,

$$\left| \frac{R_3^1}{R_2} - \frac{R_2}{R_3} \right| > \epsilon_4 \quad (20)$$

It should be recalled that the relationship $K_2 I_{b2}$ $K_1 I_{b1}$ gave rise to a positive temperature coefficient also.

Thus, ϵ_4 must be adjusted accordingly. If we refer to (18), an approximation can be derived for R_3' .

$$\text{since } \frac{R_2 + R_3}{R_2 + \angle R_3} \approx 1$$

$$\text{and } \left(\frac{R_2 R_3}{R_2 + R_3} - \frac{1}{R_1} \right) \geq \frac{R_3}{2 R_1} < 1/2 \quad (21)$$

but R_1 R_2 R_3 , to insure both transistors operate with approximately the same emitter current. Therefore, the net part of I_{b2} that flows through R_3 is at most

$$(I_{b2} - I_{b1}) \leq 1/2 I_{b2} \quad (22)$$

It was shown in (20) that a negative temperature coefficient would result with respect to the transistor's V_{be} 's,

if $R_3' > R_2 > \angle R_3$, then a first minimum approximation is,

$$\frac{(R_3 - R_2)}{R_2 - R_3} \geq \left(\frac{R_2 + R_3}{R_2 + \angle R_3} \right)$$

$$(R_3^2 - R_2^2) (R_2 + \angle R_3) (R_2 + R_3) R_2 R_3$$

$$\text{or } R_3^2 - R_2^2 > R_2 R_3$$

$$\text{and } R_3^2 - R_2^3 - R_2^2 \geq 1 \quad (23)$$

For the K_1, K_2 terms we have,

$$\left| \frac{R_2 + R_3}{R_2 + \alpha R_3} - \alpha \left(\frac{R_2 R_3}{R_2 + R_3} \right) \frac{1}{R_1} \right| < \epsilon_1 \quad (14)$$

and for the G_1, G_2 terms we have,

$$\left| R_1 + \frac{R_1 R_2}{2 R_3} - R_1 + \frac{\alpha R_1 R_3}{R_2} \right| < \epsilon_2 \quad (15)$$

normalizing ϵ_2 with respect to R_1 , we get,

$$\left| \frac{R_2}{2 R_3} - \frac{\alpha R_3}{R_2} \right| < \epsilon_3 \quad (16)$$

an ideal solution would be to make,

$$R_3 = \alpha R_2 \quad (17)$$

this will ensure ϵ_3 is positive for all values of α .

For the K_1, K_2 terms we have,

$$\frac{R_2 + R_3}{R_2 + \alpha R_3} > \alpha \left(\frac{R_2 R_3}{R_2 + R_3} \right) \frac{1}{R_1} \quad (18)$$

then for all possible values of R_1, R_2 and R_3 ,

$$K_2 I b_2 > K_1 \alpha I b_1$$

and to a first approximation, I_k will have a positive temperature coefficient, if $R_3 = \alpha R_2$.

$$\text{or } I_{e_1} = \frac{V_{ee}}{R_1} \left(\frac{1}{1 + \frac{2R_2}{R_3}} \right) + I_{b_2} \frac{R_2 + R_3}{R_2 + \beta R_3} - \beta I_{b_1} \left(\frac{R_2 R_3}{R_1 R_3 + R_1 R_2} \right) \\ + \left[+ \frac{\beta V_{be_2}}{\beta R_1 + \frac{R_1 R_2}{R_3}} \right] - \left[\frac{V_{be_1}}{R_1 + \frac{R_1 R_3}{R_2}} \right] \quad (7)$$

$$I_{e_1} = K_1 \frac{V_{ee}}{R_1} + K_2 I_{b_2} - K_3 \beta I_{b_1} + G_1 \beta V_{be_2} - G_2 V_{be_1} \quad (8)$$

for I_{e_1} to be independent of transistor parameters, it is necessary for the dependent terms to vanish and the term

$$I_e = K \left(\frac{V_{ee}}{R_1} \right) \quad (8)$$

$$\text{defines } I_k = I_{c_1} = \beta I_{e_1} \quad (9)$$

for the stability criteria for I_k and transistor dependent terms to vanish will require that,

$$\left| K_2 I_{b_2} - K_3 \beta I_{b_1} \right| < \epsilon_1 \quad (10)$$

$$\text{and } \left| G_1 \beta V_{be_2} - G_2 V_{be_1} \right| < \epsilon_2 \quad (11)$$

Then ϵ_1 , and ϵ_2 will determine system stability, to the extent that real values for the K's and G's can be realized and for matched transistor parameters,

$$\left| I_{b_1} - I_{b_2} \right| \epsilon_3 = 0 \text{ current} \quad (12)$$

$$\left| V_{be_1} - V_{be_2} \right| \epsilon_4 = 0 \text{ volts} \quad (13)$$

otherwise the various derived formulae will not be valid.

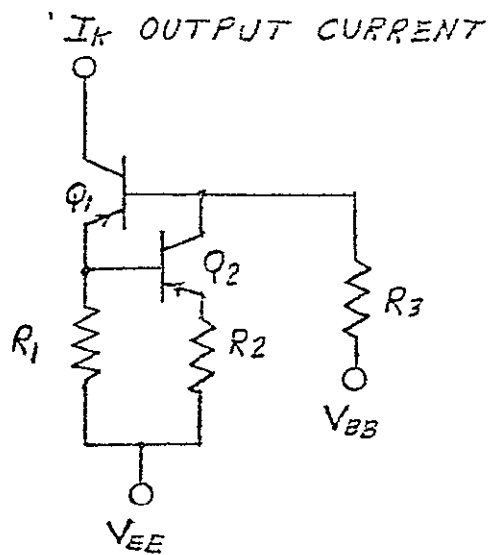


FIGURE 2 CONSTANT CURRENT SOURCE SCHEMATIC

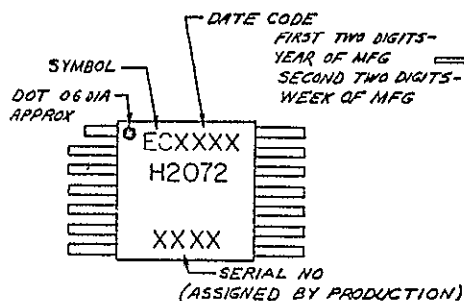
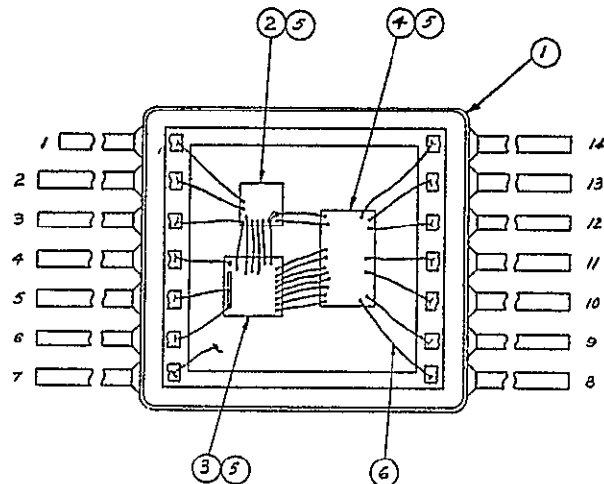
	$R_1 = 3.1k$ $R_2 = 2.5k$ $R_3 = 2.3k$ $V_E = 1.6V$ $V_B = 0$	$R_1 = 4.8k$ $R_2 = 4.1k$ $R_3 = 3.9k$ $V_E = 5.2V$ $V_B = 3.5V$	$R_1 = 4.8k$ $R_2 = 4.1k$ $R_3 = 2k$ $V_E = 5.2V$ $V_B = 3.5V$	$R_1 = 4.8k$ $R_2 = 4.1k$ $R_3 = 4.6k$ $V_E = 5.2V$ $V_B = 3.5k$
T_A $^{\circ}C$	$I_K \mu A$ ZERO T.C.	$I_K \mu A$ ZERO T.C.	$I_K \mu A$ + T.C.	$I_K \mu A$ - T.C.
-30	250.1	260.3	266.81	255.05
+30	250.25	260.43	267.11	254.10
+110	250.5	260.66	270.0	250.11

TABLE 1 CURRENT SOURCE TEST DATA; RESISTORS HAD 10PPM T.C.R., TRANSISTORS WERE MATCHED 2N3803's

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NOTES

- 1 SEE DOCUMENTS LISTED BELOW FOR PROCESSING, ASSEMBLY & TESTING.
A. PRODUCT FLOW CHART SPF
B. SCHEMATIC DIAGRAM DRAWING
NO ELE262826
- 2 PIN DESIGNATIONS ARE FOR REFERENCE ONLY



CHARACTERS TO BE 6 POINT NEWS GOTHIC CONDENSED, BLACK IN COLOR

BRANDING INFORMATION
SCALE NONE

NOTE: BRAND AS SHOWN ABOVE USING INK, ITEM 9

AR	9	BLK200241-003	INK, MARKING
1	8	BLK261602-000	PREFORM, LID
1	7	CAA261601-000	LID
AR	6	WRE260003-000	WIRE, GOLD, 30/10 DIA
AR	5	BLK260033-013	PREFORM 1
1	4		CHIP, RESISTOR RA-1071
1	3	CKA262160	CHIP, I.C. LINEAR
1	2	CAA262159	CHIP, I.C. DIGITAL
1	1	HAA260227	FLAT PACK

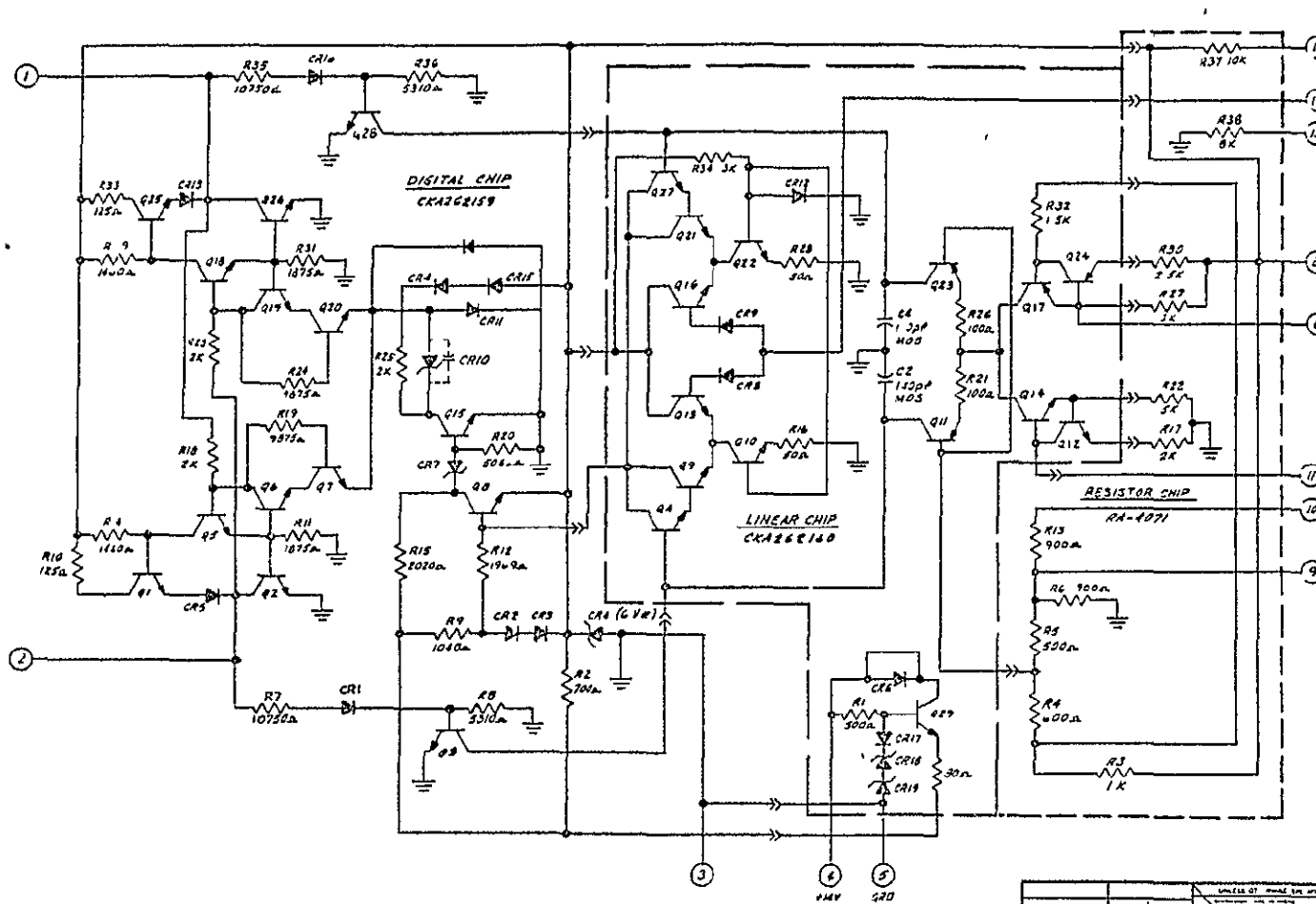
QTY ITEM PART NO DESCRIPTION
LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED		ECD APPROVAL		DATE		Electronic Components United Aircraft	
0 MARK ONE ARE		DRAWN		12 5 58		MONOLITHIC OSCILLATOR H2072	
1 TOLERANCES 0		CHECKED		12 5 58			
2 PLACE DIE MALLS		DESIGNER					
3 PLACE DIE 13 8		MECH ENG					
DO NOT SCALE THIS DRAWING		ELECT ENG				SHEET CODE IDENT NO. DRAWING NO. C 28572 ECH207200	
MATERIAL		Q.A. REL					
SEE L/M		PROD ENL					
FINISH		CONTRAST					
NONE		APPROVED				SCALE 10/1	
APPLICATION						SHEET OF	

ELE262225

REV	DATE	DESCRIPTION	BY	APPROVED
1				

NOTES
1 SYMBOL INDICATES AN INTER-CHIP CONNECTION (WIRE BOND) →



DESIGN OF MONOLITHIC CIRCUITS		CIRCUIT SYMBOL		DATE	
DESIGNER		CHECKED		DATE	
DRAWN		REVIEWED		DATE	
MATERIAL		APPROVED		DATE	
REVISIONS		DATE		DATE	
APPLICATION		DATE		DATE	
ELECTRONIC COMPONENTS		UNITED AIRCRAFT		DATE	
SYNTHETIC DIAPHRAGM		MONOLITHIC CALCULATOR		DATE	
D 28572		ELE262225		DATE	

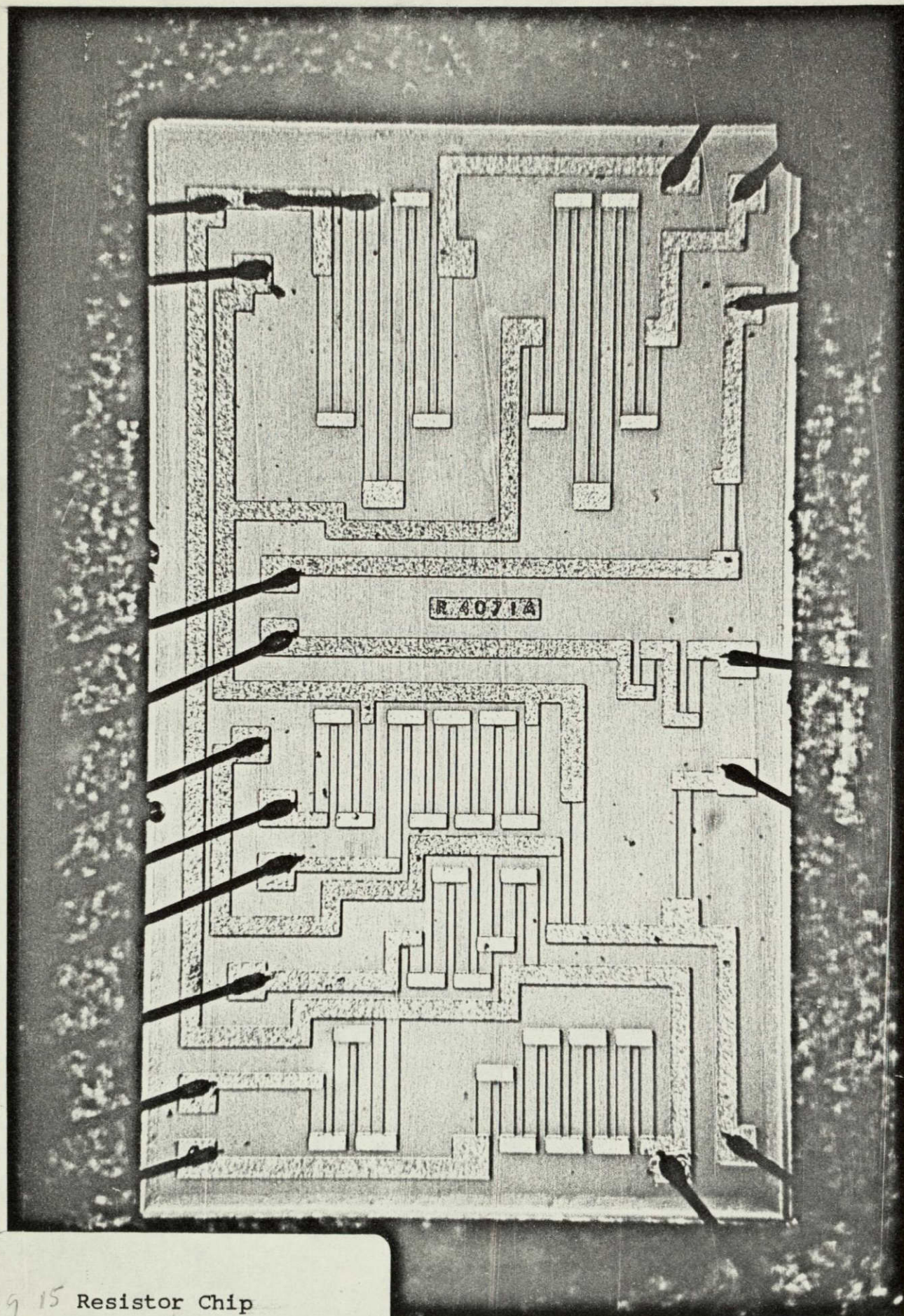


Fig 15 Resistor Chip