6294

PHASE COMPLETION REPORT
IN ACCORDANCE WITH PHASE III
OF NASA CONTRACT NAS-8-11916

Bendix Navigation & Control Division
Teterboro, New Jersey 07608

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N 70 18976

NASA CR 102453

PHASE COMPLETION REPORT IN ACCORDANCE
WITH PHASE III OF NASA CONTRACT NAS 8-11916

CASE FILE
COPY

Prepared by: B Friedman
B. Friedman

THE BENDIX CORPORATION
NAVIGATION AND CONTROL DIVISION
TETERBORO, NEW JERSEY

REVIEW OF PHASE I AND II ACCOMPLISHMENTS

Phase I

Phase I of the contract called for the design and development of microelectronic circuits for stabilization of a gas bearing gyro servo loop. During this phase a number of plausible designs for each stage of a microelectronic servo amplifier were investigated. Extensive evaluation testing enabled a selection of the design configurations best suited for the performance and miniaturization requirements specified. When circuit module breadboarding and testing were completed, closed loop system testing was performed. A recommended overall amplifier design was presented in MT-8161. The stress levels of the microelectronic servo loop components under worst case conditions were calculated and submitted in MT-8163. A worst case thermal analysis was conducted on the preamp active network, and PWM modules. The results were introduced in MT-8164. Further examination of circuit operation resulted in revisions of the overall amplifier design in an effort to improve performance. MT-8166 was written to describe these design revisions. MT-8168 was presented upon completion of a failure effect and reliability analysis on the microelectronic servo amplifier. Toward the conclusion of Phase I concept definition of the servo amplifier was manifested in a formal breadboard circuit which was thoroughly evaluated and shipped to NASA per contract instructions. MT-8170 provided a description of the characteristics and operation of the microelectronic servo amplifier breadboard and MT-8179 served to document the overall performance characteristics the servo amplifier.

Phase II

Phase II contract requirements essentially were: to fabricate, test, and institute final design corrections on Phase I circuitry, and to complete and deliver six operating servo loop electronics to the Marshall Space Flight Center. During the period of performance of Phase II, eight (8) preamp and detector modules, eight (8) low pass filter and stabilizing network modules, and eight (8) dual channel pulse width modulator modules were constructed and tested. Each of six (6) sets of these prototype units was assembled onto a motherboard (supplemented with a power supply module), tested as a complete servo amplifier, and shipped to MSFC. Another set of modules was potted, assembled on a motherboard, and subjected to a temperature and humidity environmental test program. The three modules of the remaining set were potted and individually subjected to acceleration, vibration, and shock environmental testing.

An outline of the evaluation and environmental test procedures for the microelectronic servo amplifier prototype modules was presented in MT-8172. The specific evaluation test procedures for the preamp and detector, low pass filter and stabilizing network, and PWM modules followed in MT's 8173, 8174 and 8175 respectively. MT-8176 covered the evaluation test procedure for the overall amplifier.

As evaluation testing on the prototype modules and amplifiers progressed, several problems were encountered and minor design corrections were made. MT-8180 updated the microelectronic servo amplifier schematic and evaluation test procedures prior to shipment of the first amplifier. Material, describing certain problem areas and possible component and circuitry improvements, was incorporated into MT's 8177 and 8240. Progress reports No. 6 thru No. 19 provided a running account of all the problems and developments that occurred during Phase II.

Included in the test program of prototype units was environmental testing. Reports on the mechanical environmental tests that were performed on the potted preamp and detector, low pass filter and stabilizing network, and PWM modules were presented in MT's 8241, 8242, and 8243 respectively. MT-8244 documented the extreme temperature and humidity environmental tests run on a potted prototype amplifier assembly.

A complete listing of all MT's generated under Phase I and Phase II follows.

INDEX OF PHASE I AND PHASE II MT'S

MT	TITLE	AUTHOR
8150	Analysis of a Low-Pass Notch Filter	V. Kiltenis
8151	Investigation of the Single Channel Pulse Width Modulator in Conjunction with NASA Contract NAS 8-11916	A. Esser
8152	Investigation of the Transformer Coupled Preamplifier and Detector in Conjunction with NASA Contract NAS 8-11916	A. Esser
8155	Additional Investigation on the Transformer Coupled Preamplifier, Detector and Filter Configuration Previously Described in MT-8152	A. Esser
8156	Investigation of the Microelectronic Servo Loop Demodulator Section in Conjunction with NASA Contract NAS 8-11916	A. Esser
8157	Investigation of the Dual Channel Pulse Width Modulator in Conjunction with NASA Contract NAS 8-11916	A. Esser
8160	Investigation of the Stabilizing Network for the Microelectronic Servo Loop in Conjunction with NASA Contract NAS 8-11916	A. Esser
8161	Recommended Overall Amplifier Design in Conjunction with NASA Contract NAS 8-11916	A. Esser R. Weiss
8162	Investigation of Dead Zone in Dual-Channel Pulse-Width Modulator	R. Weiss

MT	TITLE	AUTHOR
8163	Stress Analysis of the Microelectronic Servo Loop in Conjunction with NASA Contract NAS 8-11916	A. Esser
8164	Thermal Analysis of the Microelectronic Servo Loop in Conjunction with NASA Contract NAS 8-11916	A. Esser
8165	Additional Investigation of the Stabilizing Networks for the Microelectronic Servo Loop in Conjunction with NASA Contract NAS 8-11916	A. Esser
8166	Revisions of the Overall Microelectronic Servo Amplifier Design Previously Described in MT-8161	A. Esser
8167	Additional Investigation of the Dual Channel Pulse Width Modulator Previously Described In MT-8157	A. Esser
8168	Failure Effect and Reliability Analysis Micro-electronics Servo Loop Developed on Contract NAS 8-11916	W. Podolak
8169	Investigation of the Operation of a High Efficiency DC to DC Converter - Converter Type Power Supply in Conjunction with NASA Contract NAS 8-11916	I. Soller
8170	Description and Operation of Microelectronic Servo Amplifier Breadboard in Conjunction with NASA Contract NAS 8-11916	A. Esser

8171 Description and Test Evaluation of a DC to DC Converter Having Multiple Isolated Outputs in Conjunction with NASA Contract NAS 8-11916 — S. Weinstein

8172 An Outline of the Evaluation and Environmental Test Procedures for the Microelectronic Servo Amplifier Prototypes Developed Under NASA Contract NAS 8-11916 — A. Esser

8173 Test Procedure for Microelectronic Preamp and Detector Module in Conjunction with NASA Contract NAS 8-11916 — A. Esser

8174 Evaluation Test Procedure for Microelectronic Low Pass Filter and Stabilizing Network Prototype Modules in Conjunction with NASA Contract NAS 8-11916 — B. Osterloh

8175 Test Procedure for Microelectronic Pulse Width Modulator Module in Conjunction with NASA Contract NAS 8-11916 — A. Esser

8176 Test Procedure for Overall Microelectronics Servo Amplifier in Conjunction with NASA Contract NAS 8-11916 — A. Esser

8177 A Description of Certain Problem Areas and Some Possible Improvement on the Microelectronic Servo Amplifier in Conjunction with NAS Contract NAS 8-11916 — A. Esser

8179 Microelectronic Servo Amplifier Performance Characteristics (NASA Contract NAS 8-11916) — R. Weiss

MT	TITLE	AUTHOR
8180	Updating for Microelectronic Servo Amplifier Schematic and Evaluation Test Procedures Prior To Shipment of the First Microelectronic Servo Amplifier Prototype in Conjunction with NASA Contract NAS 8-11916	B. Osterloh
8240	Discussion of Possible Components and Circuitry Improvements for Microelectronic Servo Loops Developed under NASA Contract NAS 8-11916	A. Esser
8241	Mechanical Environmental Tests on a Potted Preamp and Detector Prototype Module in Accordance with NASA Contract NAS 8-11916	B. Osterloh W. Gorczycki
8242	Mechanical Environmental Tests on a Potted Low Pass Filter and Stabilizing Network Prototype Module in Accordance with NASA Contract NAS 8-11916	B. Osterloh
8243	Mechanical Environmental Tests on a Potted Dual Channel Pulse Width Modulator Prototype Module in Accordance with NASA Contract NAS 8-11916	B. Osterloh W. Gorczycki
8244	Temperature and Humidity Environmental Tests on a Potted Microelectronic Servo Amplifier Prototype Assembly in Accordance with NASA Contract NAS 8-11916	B. Osterloh W. Gorczycki

PHASE III CONCLUSIONS AND RECOMMENDATIONS

As a result of the program of evaluation and testing carried out under Phase III of NASA Contract NAS 8-11916, it can be concluded that the servo amplifier design is capable of performing its intended task. There are, however, certain recommendations which should be considered in an attempt to further improve the reliability and performance of the circuitry. The recommendation which contains the greatest impact on reliability is concerned with the custom integrated circuits used in the Pulse Width Modulated DC amplifier. These monolithic integrated circuits have been found defective on several instances, due entirely to improper quality assurance and inspection provisions at the vendor. It is therefore recommended that before additional units be purchased, a comprehensive and detailed purchase specification outlining quality and inspection criteria, along with complete electrical specifications, be generated.

It is also recommended that additional investigation of the triangle wave generator be undertaken to improve triangle wave linearity when used in low gain applications as suggested in MT-8254.

Another area that should be further studies is the unity gain operational amplifier used in the preamp. It has been found that in the event of a loss of the positive supply voltage this amplifier is exposed to the possibility of exceeding the common mode imput rating, which in turn causes a degradation in amplifier performance or even failure. It is recommended that diodes be incorporated in the input to preclude the possibility of a failure of this type, or that a operational amplifier incorporating input protection and a much greater differential input, such as the LM101, be used to replace the μA709 presently used.

INTRODUCTION

The purpose of Phase III of NASA contract NAS 8-11916 has been to build, test, and evaluate a servo amplifier designed for the stabilization of a Gas Bearing Gyro Servo Loop. The circuit contained in this servo amplifier have been designed using microelectronic components where-ever feasible in an effort to realize greater reliability along with volume and weight savings.

This report contains a review of the work carried out under this contract. Also contained is a description of the constituent circuits contained in the servo amplifier. All test data and evaluation is contained in MT form. Copies of the pertinent MT's are included with this report.

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1.0 REVIEW OF PHASE III CIRCUITS

1.1 PREAMPLIFIER AND DETECTOR

The preamplifier configuration evaluated under Phase III is shown below. This circuit differs from the preamp circuits of Phase I and Phase II primarily because of the use of differential input and output. Since a satisfactory operational amplifier utilizing differential input and output modes was not available when evaluation began, it was necessary to use two μA709 devices to accomplish the desired differential mode operation. The detector evaluated under Phase III uses integrated choppers to achieve demodulation.

Test data for the Preamp and Detector circuit is presented in MT-8249, and from these results it has been concluded that the circuitry presented below will satisfactorily perform its entended function in loop operation.

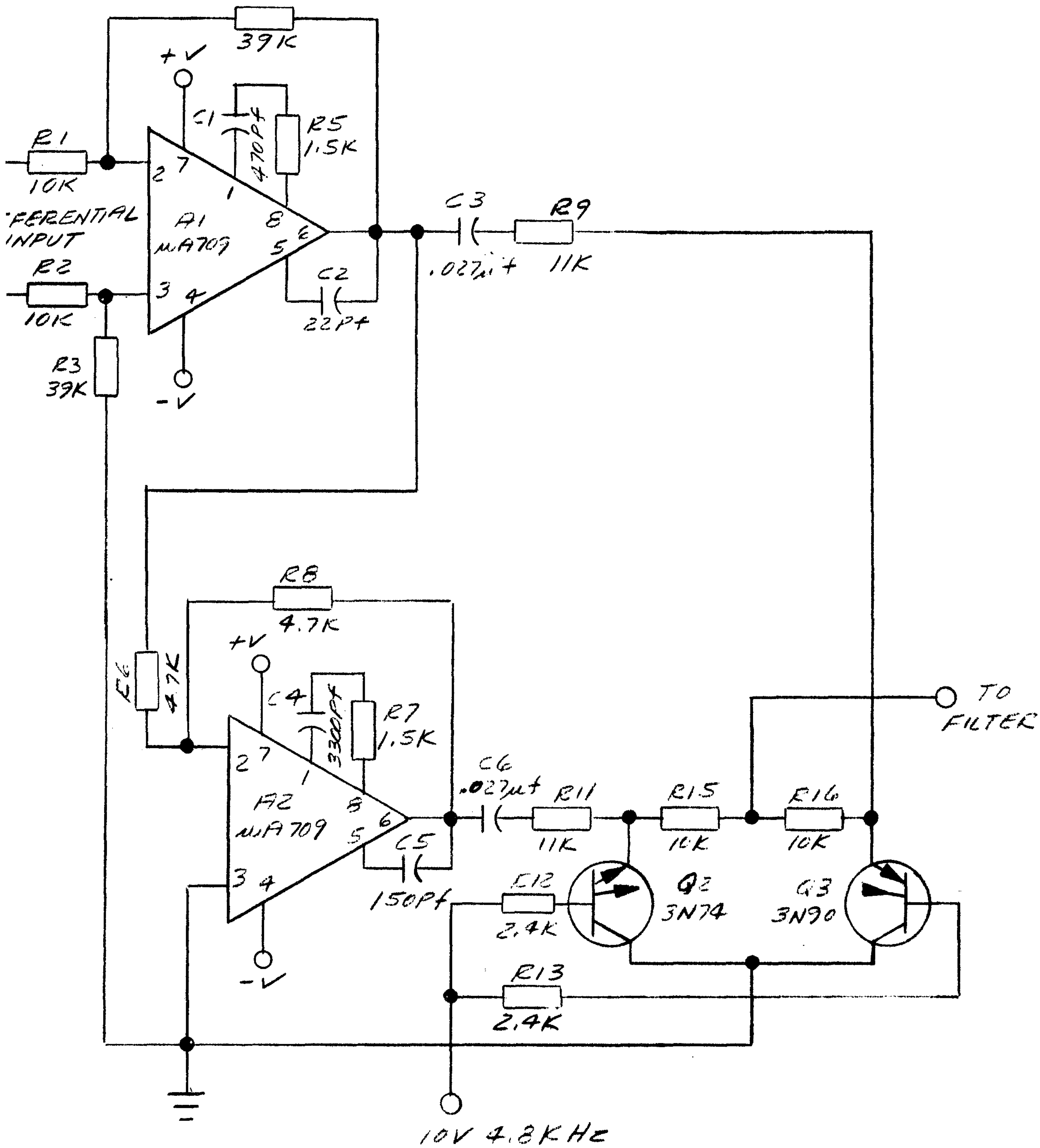

FIGURE 1

PREAMP-DETECTOR

1.2 LOW PASS FILTER

The low pass filter, shown below, has been changed from the passive configuration of Phase I and II to an active design. This circuit is described in MT-8252.

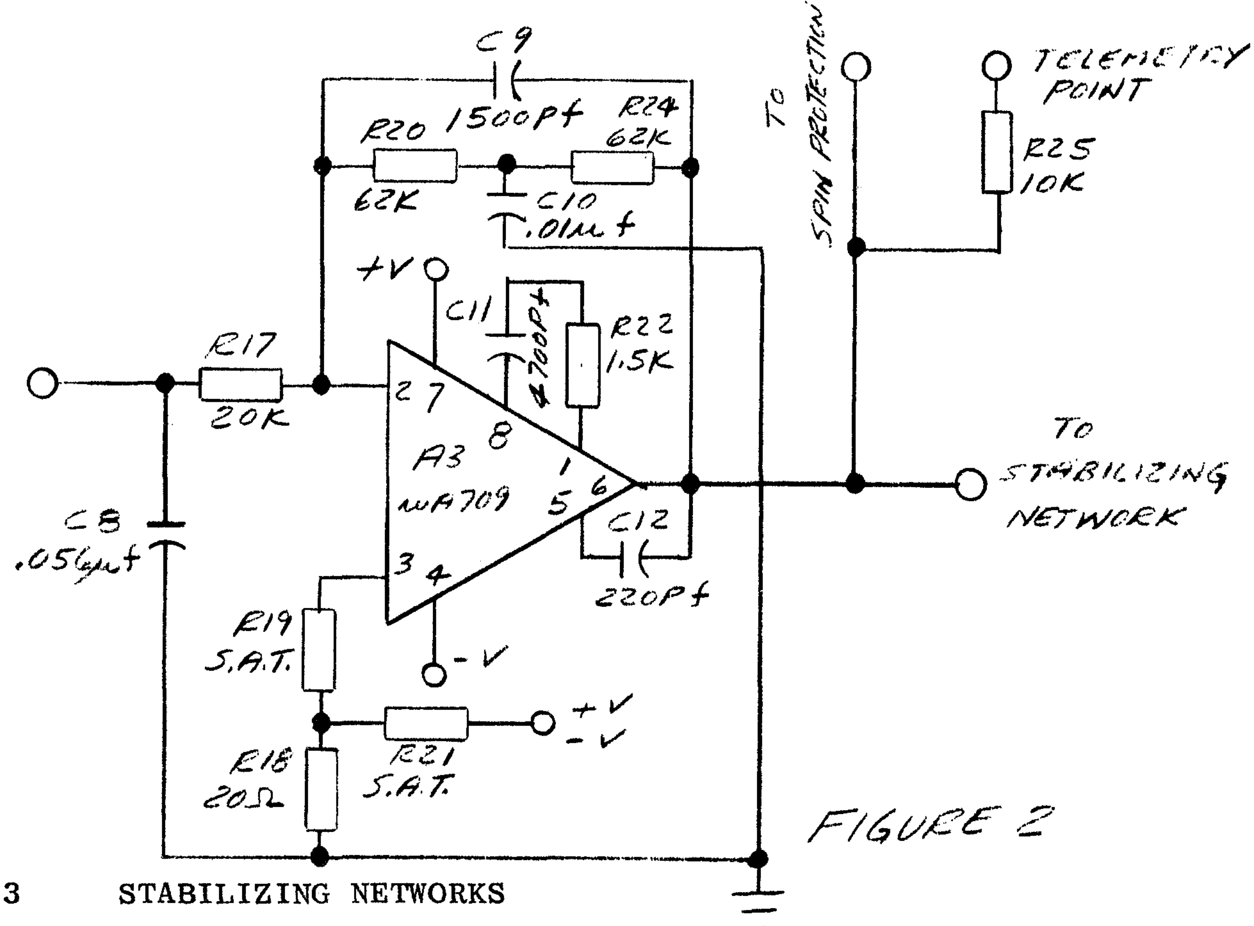

FIGURE 2

1.3 STABILIZING NETWORKS

The active network design shown in Figure generates the following transfer function.

$$\frac{(37\times10^{-6}s^{2} + 48.8\times10^{-4}s + 1)(1.345\times10^{-2}s^{2} + 119.3\times10^{-2}\,s + 1)}{(117\times10^{-2}s)(19.3\times10^{-8}s^{2} + 4.17\times10^{-4}s + 1)(20.7\times10^{-2}s + 1)}$$

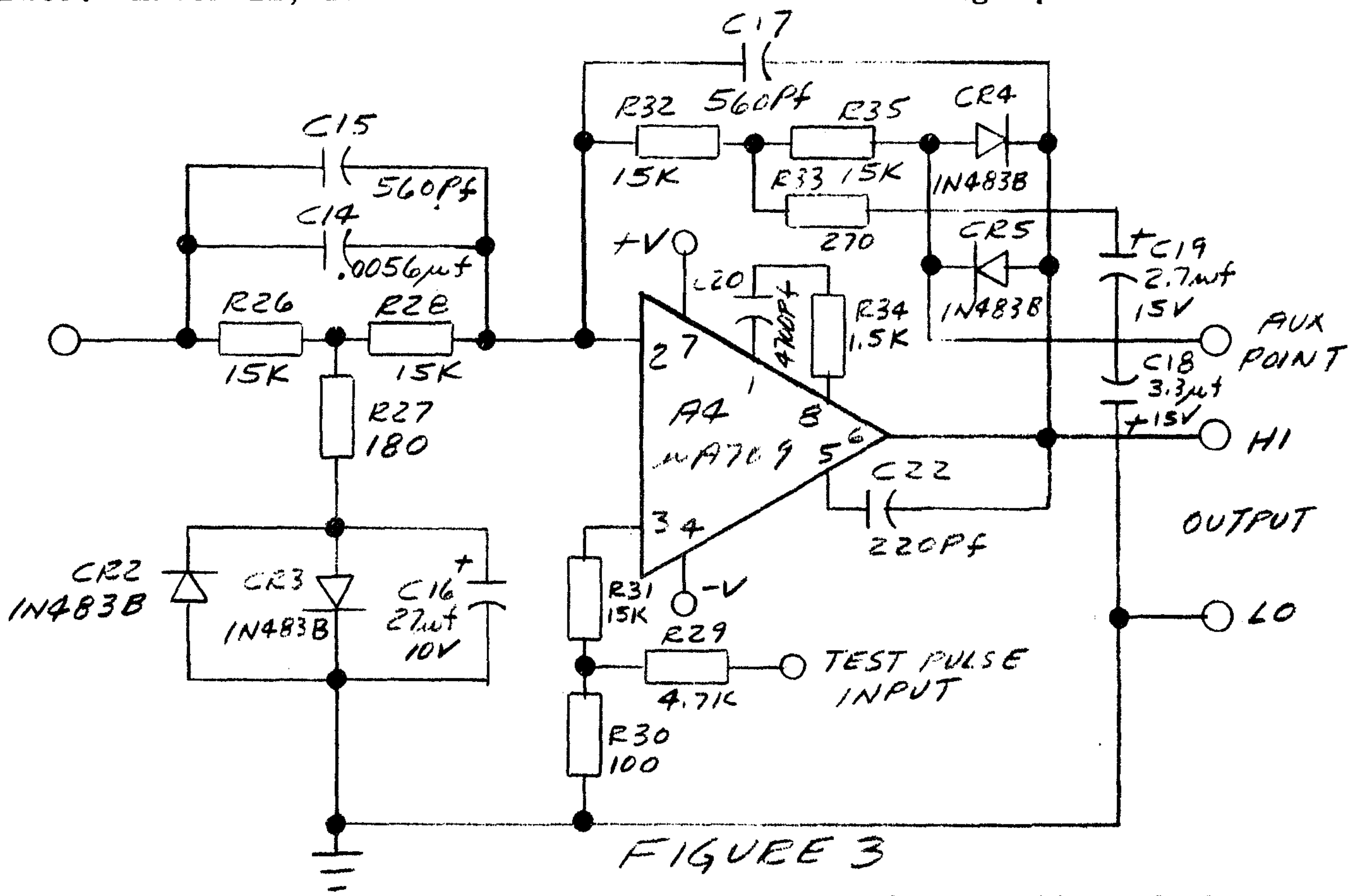

FIGURE 3

The difference in the form of the transfer function of the active network used in Phase III from the form of Phases I and II is due to the addition of a series feedback capacitor. As can be seen from the transfer function for Phase III, this feedback capacitor theoretically gives infinite d.c. gain, which in turn can be interpreted as theoretical infinite d.c. stiffness. A detailed description of the Stabilizing Networks can be found in MT's 8247 and 8250.

1.4 PWM POWER AMPLIFIER

Although the power amplifiers used in Phases I and II of NAS 8-11916 were also pulse width modulated, the power amplifier evaluated under Phase III is strikingly different.

The design philosophy on all previous PWM efforts had been to utilize standard microelectronic devices in an effort to achieve greater reliability and savings in weight and space. The philosophy used in Phase III was to attempt to integrate, using custom integrated circuits as much as possible, a discrete component PWM design. In order to implement the discrete component design shown in Figure 4 in integrated monolithic form, a breadboard type integrated circuit was employed. This particular I.C. is a device comprised of six NPN transistors and 33 resistors. Contact pads for all of the components are provided on the chip and by custom interconnection of the devices, circuit functions can be fabricated. An important aspect of this device which permits a design to be converted quite easily from discrete form to integrated is the fact that dielectric isolation is employed to separate each of the active devices from any other, and to isolate the resistor array. This process greatly reduces the parasitics and hidden components usually associated with monolithic integrated circuits. Figure 5 shows the circuit elements available on chip and also the connection pad layout. Figure 6 shows the die interconnection patterns generated to achieve the PWM configuration shown in Figure 7. The five chips thus produced represent four different circuit areas in the discrete component design. The four circuits integrated are shown in Figure 8 to 11.

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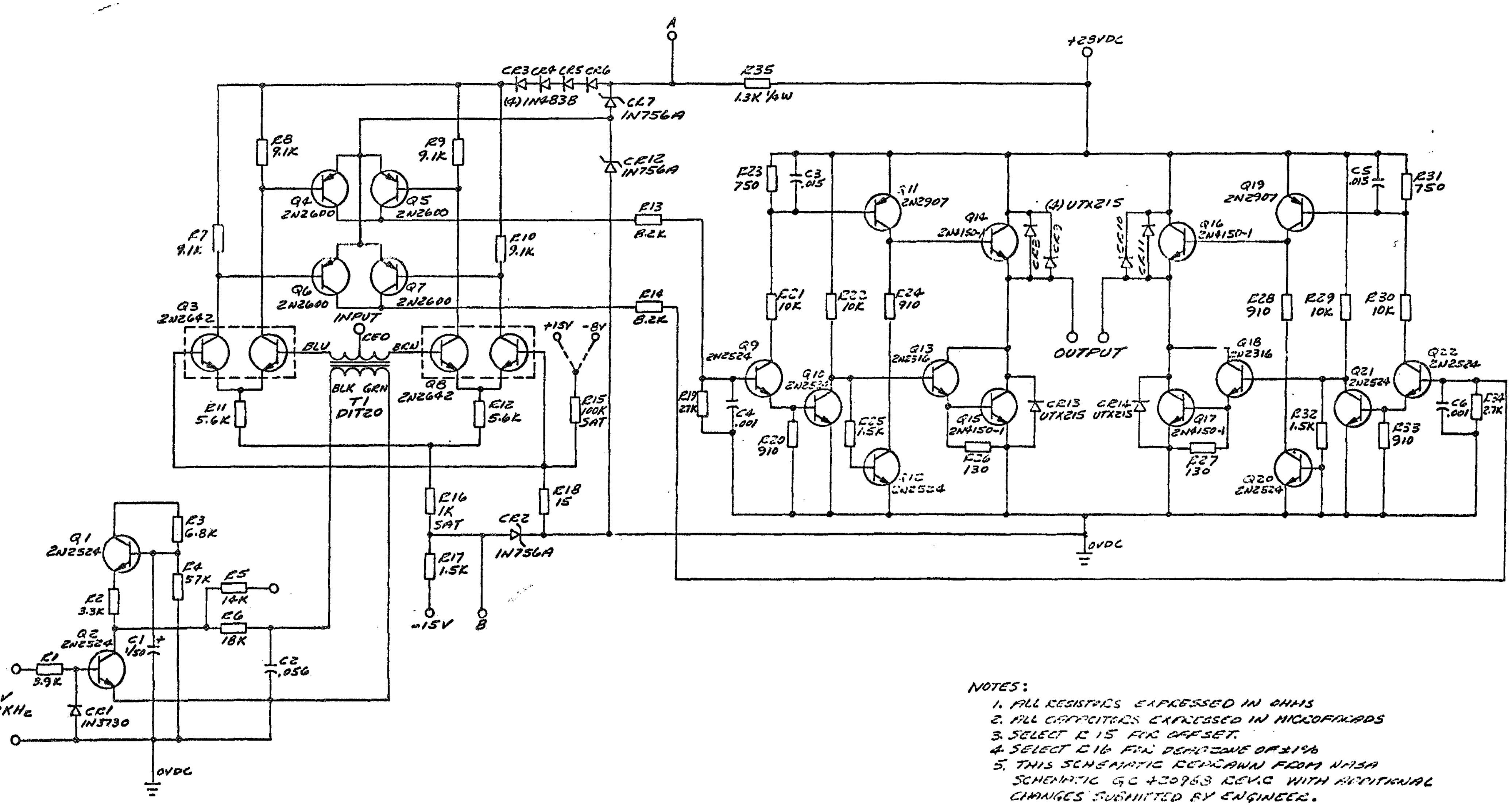

NOTES:

1. ALL RESISTORS EXPRESSED IN OHMS
2. ALL CAPACITORS EXPRESSED IN MICROFARADS
3. SELECT R 15 FOR OFFSET.
4. SELECT R 16 FOR DEADZONE OF ±1%
5. THIS SCHEMATIC REDRAWN FROM NASA SCHEMATIC GC 420963 REV.C WITH ADDITIONAL CHANGES SUBMITTED BY ENGINEER.

✱=INDICATES SUBASSEMBLY †=VENDOR ITEM – SEE SOURCE CONTROL OR SPECIFICATION CONTROL DRAWING	– LIMITS OF ACCEPTABLE WORKMANSHIP ARE DEFINED IN NAVIGATION & CONTROL STANDARDS DS-103	UNLESS OTHERWISE SPECIFIED – DIMENSIONS ARE IN INCHES – TOLERANCES ON DECIMALS 2 PLACE ±.03 3 PLACE ±.005 4 PLACE ±.0005	DR M. DICKSON CHK ENGR T. D. MET REL APPD	THE BENDIX CORPORATION NAVIGATION & CONTROL DIVISION TETERBORO, NEW JERSEY, U.S.A.
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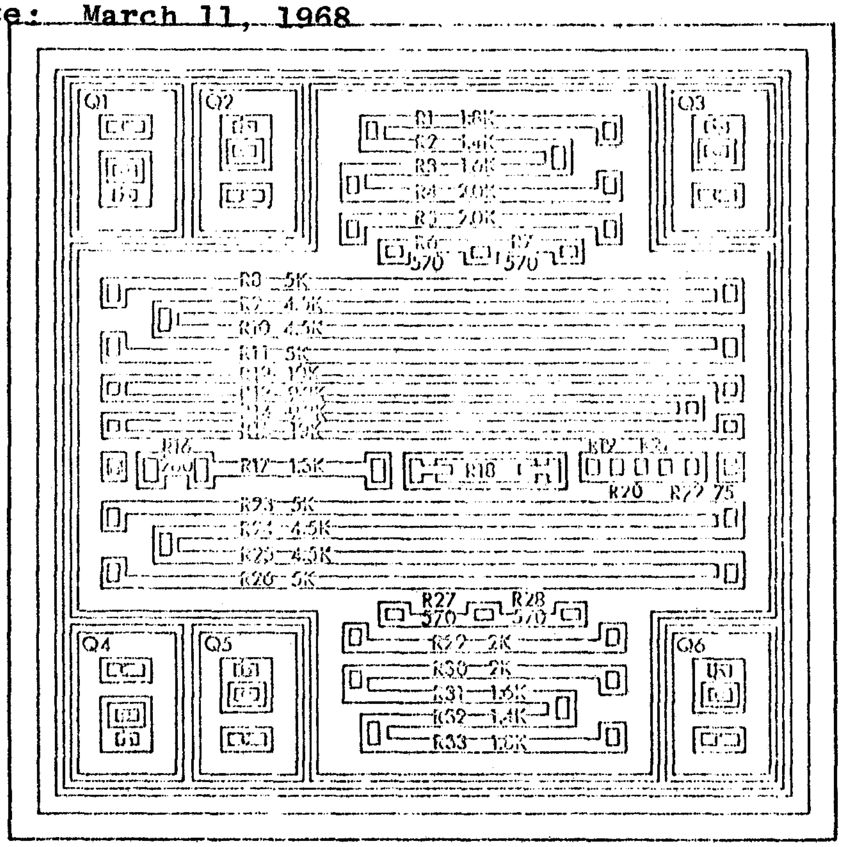
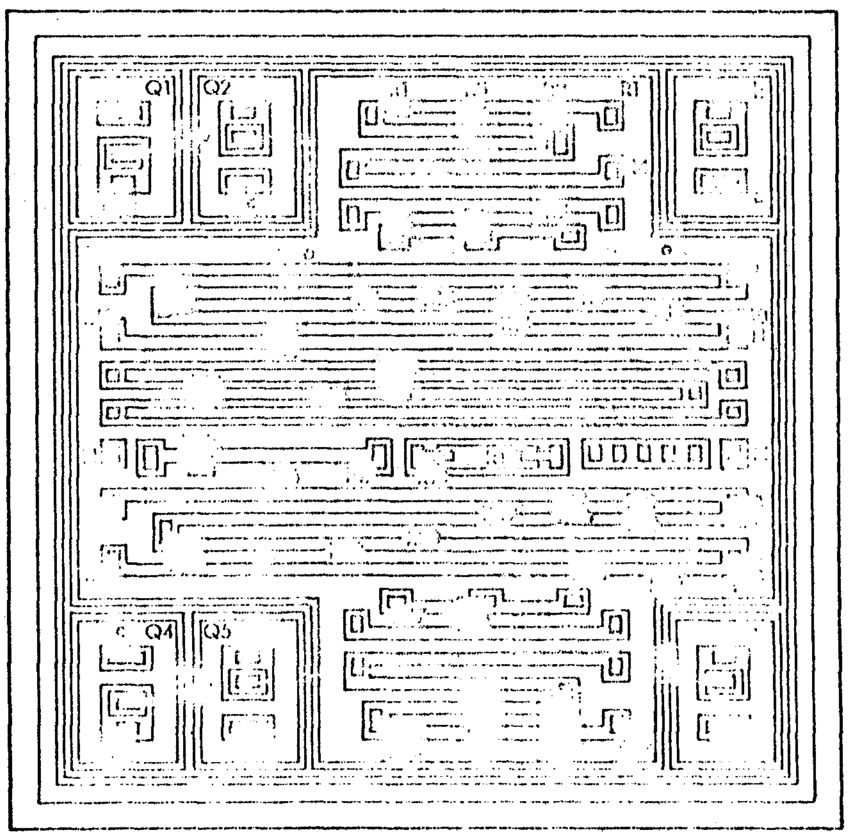
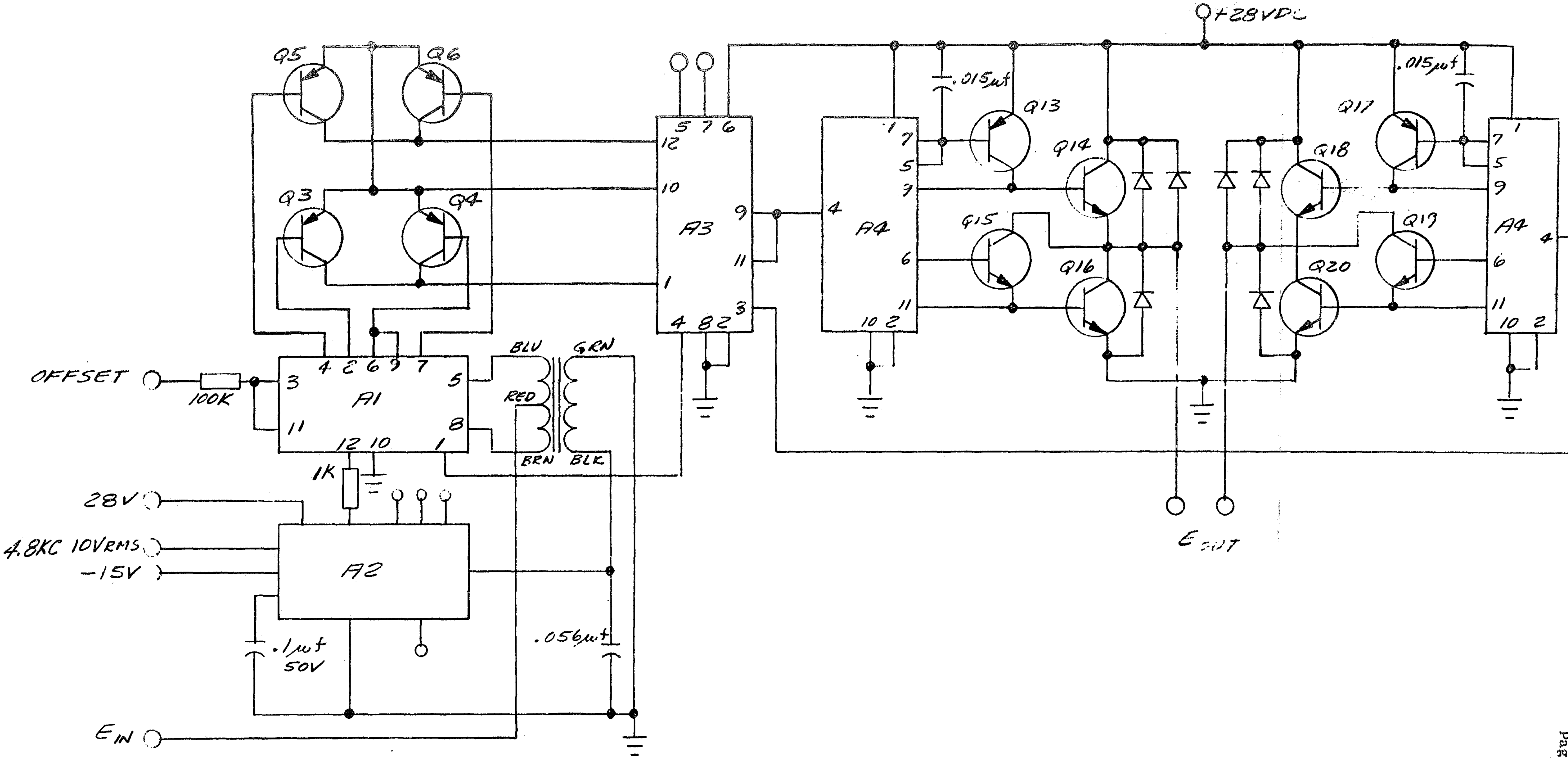


COMPONENT IDENTIFICATION



COMPONENT TERMINAL PAD LAYOUT

FIGURE 5



I.C. PWM SERVO AMP
(STITCHED VERSION)

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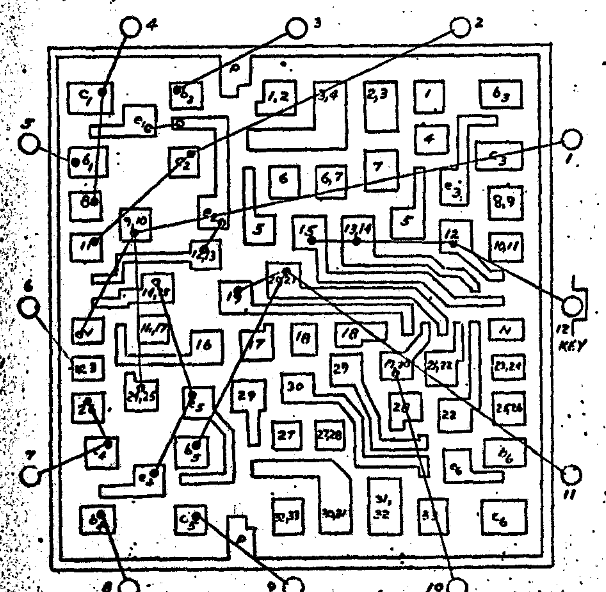
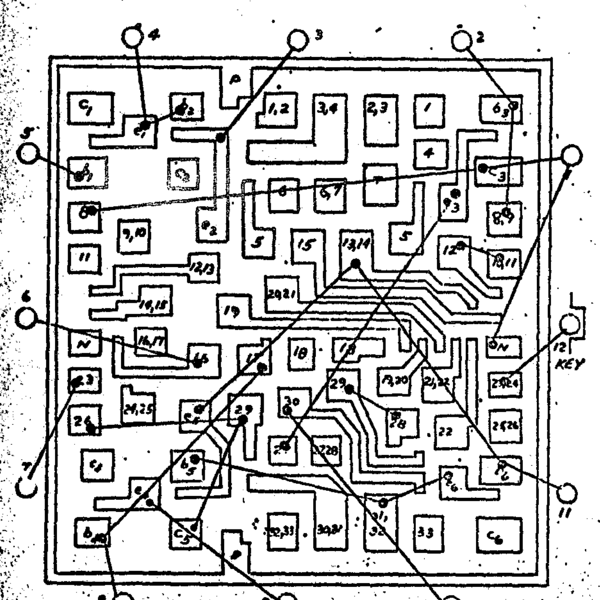
1001



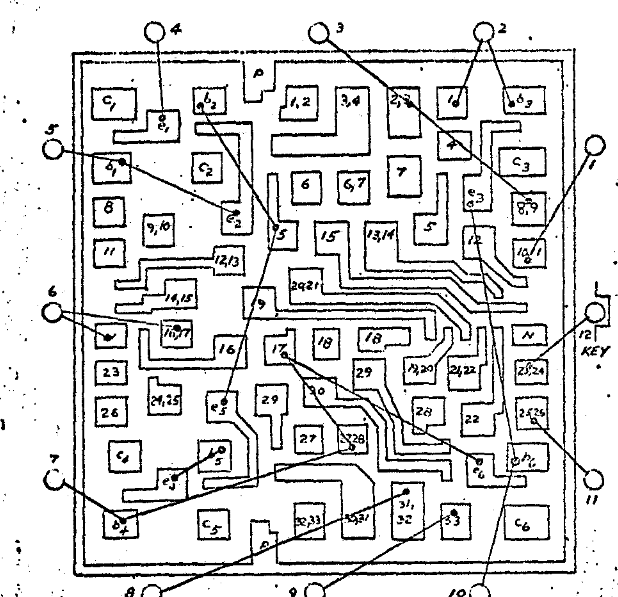
MASTER DICE BREADBOARD

1002



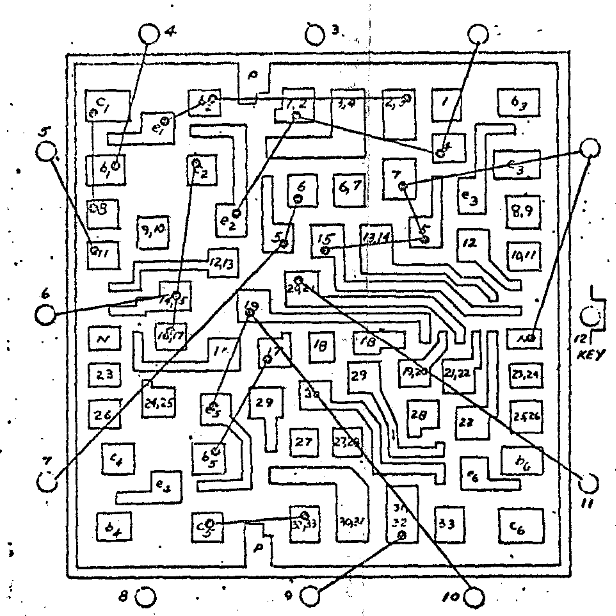
MASTER DICE BREADBOARD

1003



MASTER DICE BREADBOARD

1004



MASTER DICE BREADBOARD

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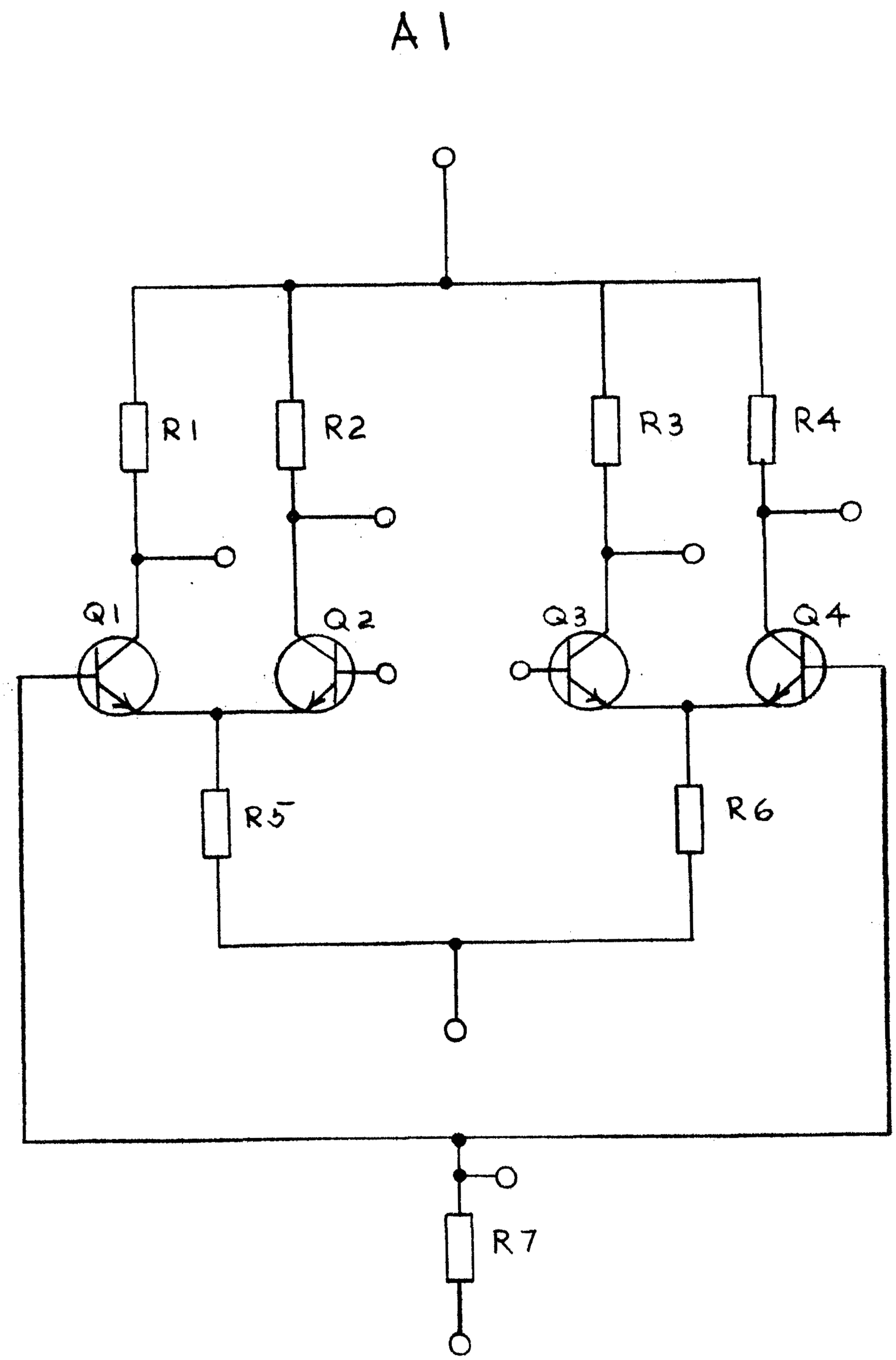

FIG. 8

A2

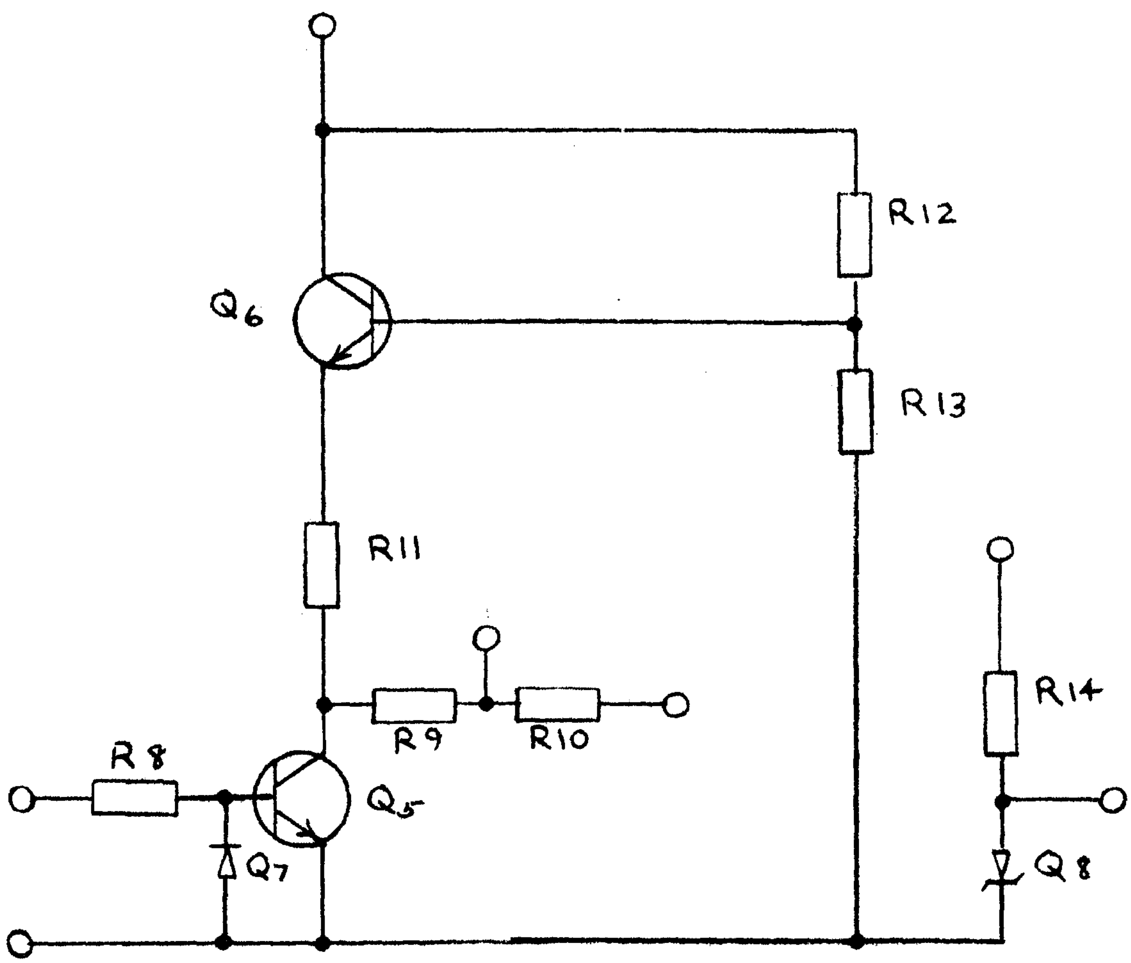

FIG 9

A3

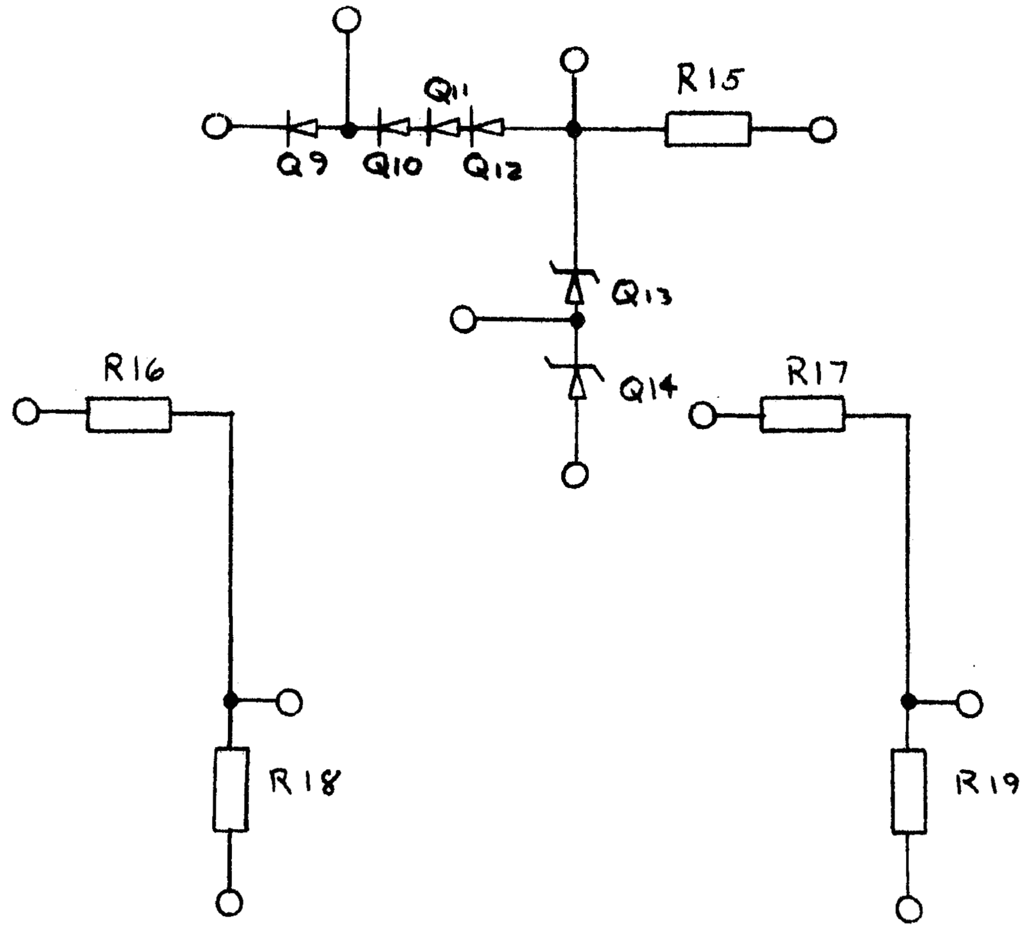

FIG. 10

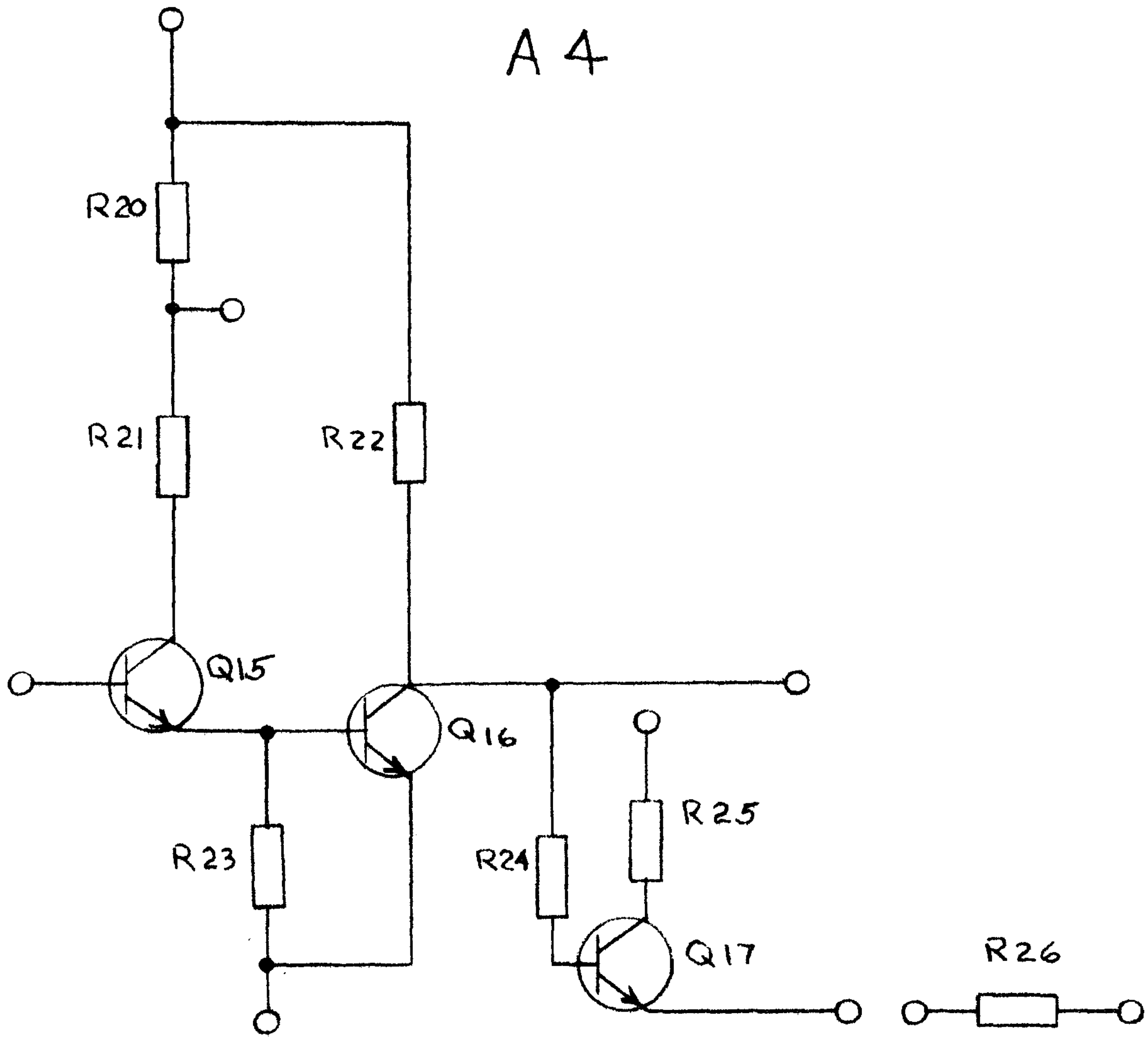

FIG. 11

After the circuit configuration for the four types of chips were found satisfactory, chips with custom metallization were made up to replace the ultrasonically bonded wire interconnects. It was decided to perform all circuit testing and evaluation with the metallized versions. The circuit configuration of Figure 12 uses the metallized chips namely the VI-1101, VI-1102, VI-1103, and VI-1104 made by Vector, Division of United Aircraft. MT-8254 deals with the PWM circuit shown in Figure 12 built to the assembly drawing of Figure 13. The results of the testing program carried out on the PWM circuit show that the circuitry is well suited to perform its intended loop functions.

5.1 PWM CHIPS

In addition to the 5 metallized chips received under NAS 8-11916 for PWM evaluation more identical devices were received from the vendor. Of the devices tested three failures were encountered that were directly attributable to improper manufacturing and testing short comings. These three failures are documented in MT's 8253 and 8255. Table 1 is a breakdown of the failures encountered from all causes. Meetings with the vendor at his facility, pointed out that these devices were manufactured as engineering prototype units, and as such were not subject to the normal quality assurance and reliability screening procedures. Visual inspection was minimal if at all, and the only testing performed was d.c. resistance measurement at the case pins. In order to reduce the number of failures of the type referenced in the aforementioned MT's, it is

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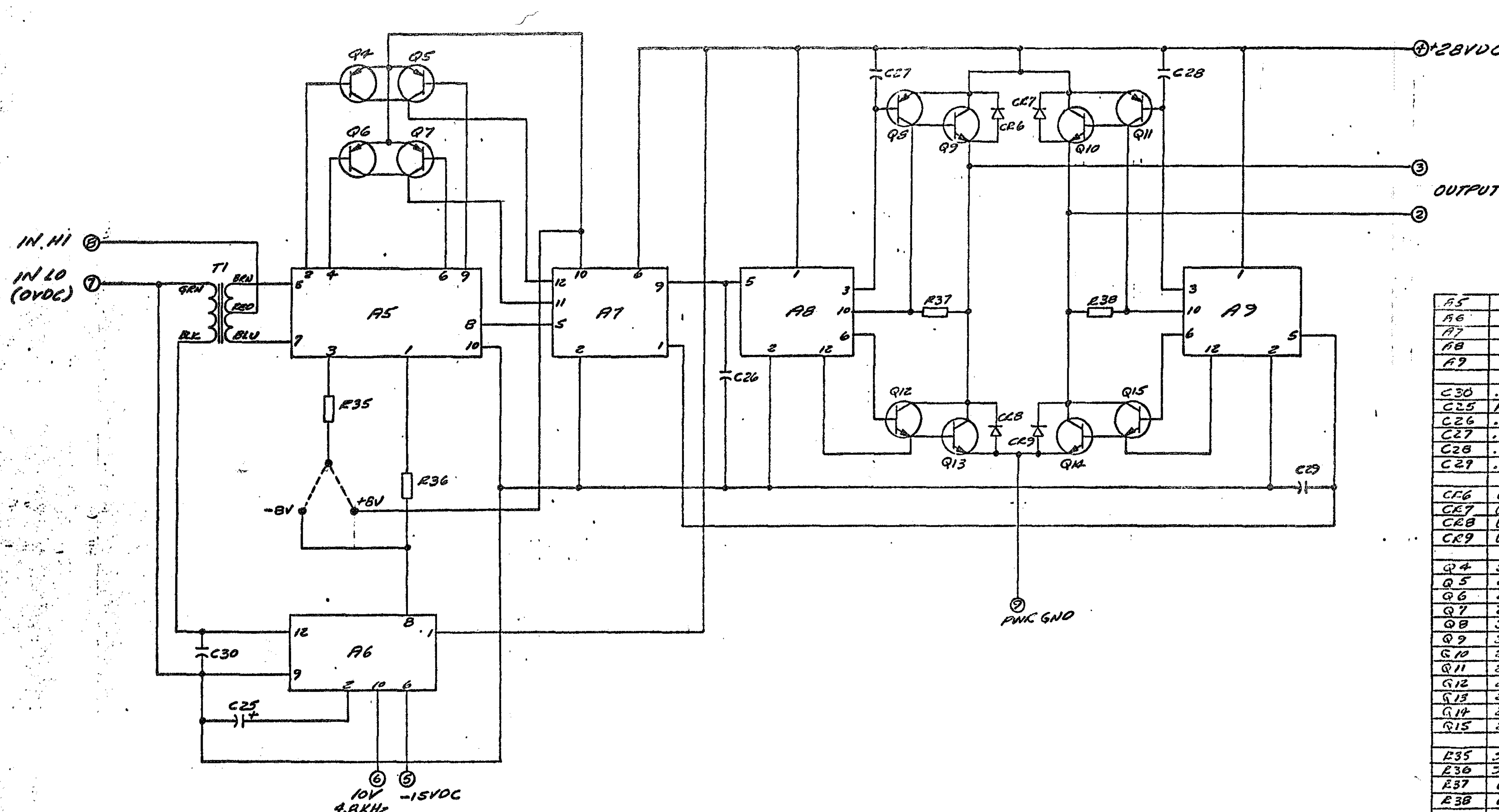

A5		V11101
A6		V11102
A7		V11103
A8		V11104
A9		V11104
C30	.1UF ±10% 50V	VK30BX104K
C25	1UF ±10% 35V	CS13BF105K
C26	.001UF ±10% 200V	CK05CW102K
C27	.015UF ±10% 50V	VK30BX153K
C28	.015UF ±10% 50V	VK30BX153K
C29	.001UF ±10% 200V	CK05CW102K
CR6	UTX210	
CR7	UTX210	
CR8	UTX210	
CR9	UTX210	
Q4	2N722	
Q5	2N722	
Q6	2N722	
Q7	2N722	
Q8	2N2907	
Q9	2N4150 (H.S.)	
Q10	2N4150 (H.S.)	
Q11	2N2907	
Q12	2N2316	
Q13	2N4150 (H.S.)	
Q14	2N4150 (H.S.)	
Q15	2N2316	
R35	S.A.T. 100K NOM ±5% 1/8W	RC05GF104J
R36	S.A.T. 1K NOM ±5% 1/8W	RC05GF102J
R37	680 ±5% 1/8W	RC05GF681J
R38	680 ±5% 1/8W	RC05GF681J
T1	DIT 20 (UTC)	

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+ — VENDOR ITEM — SEE SOURCE CONTROL OR SPECIFICATION CONTROL DRAWING

— LIMITS OF ACCEPTABLE WORKMANSHIP ARE DEFINED IN ECLIPSE-PIONEER STANDARDS DS-103

UNLESS OTHERWISE SPECIFIED
— DIMENSIONS ARE IN INCHES
— TOLERANCES ON DECIMALS
2 PLACE ±.03 3 PLACE ±.010 4 PLACE ±.0005

HARDNESS

FINISH

MATERIAL

DR N.D. 7-11-67
CHK
T.D.
MET.

CONTRACT NO.

APPROVAL

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PART REF

ORIGINALLY DESIGNED FOR

THE Bendix CORPORATION
ECLIPSE - PIONEER DIVISION
TETERBORO, NEW JERSEY, U.S.A.

SCHEMATIC
INTEGRATED POWER AMPLIFIER

SIZE	CODE IDENT NO.	
D	19315	X1849775

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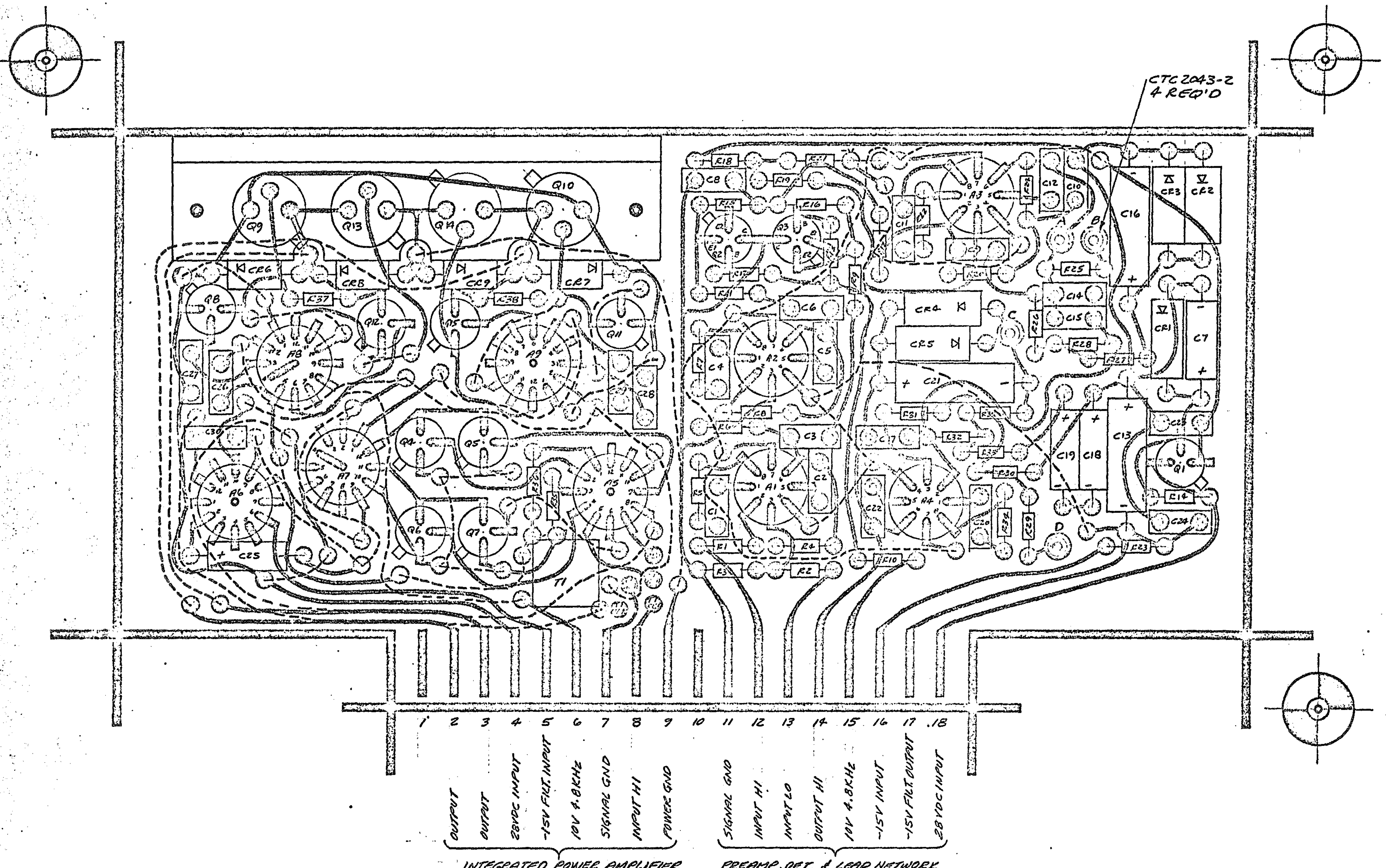
Device Type	No. Received	No. OK	Failed Due to Overstress	Failed Due to Manufacture
VI-1101	6	4	1	1
VI-1102	6	4	0	2
VI-1103	3	2	1	0
VI-1104	12	10	2	0

TABLE 1

suggested that arrangements be made to guarantee close visual inspection of all devices, along with process control and dynamic electrical testing.

1.5 OVERALL SERVO AMPLIFIER

The overall servo amplifier shown in Figure 14 and 15 is presently being constructed. Figure 16 shows the assembly drawing. This servo amplifier uses the circuits previously described in this report. When test and evaluation data becomes available, it will be forwarded in MT form.



UNLESS OTHERWISE SPECIFIED
—DIMENSIONS ARE IN INCHES
—TOLERANCES ON DECIMALS
2 PLACE ± .03 3 PLACE ± .005 4 PLACE ± .0005

MATERIAL

DR JV. 12. 1-11-68
CHK
T. D.
MET.

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APPROVAL

THE Bendix CORPORATION ECLIPSE - PIONEER DIVISION TETERBORO, NEW JERSEY, U.S.A.

ASSEMBLY
MICROELECTRONIC
SERVO AMPLIFIER

SIZE D CODE IDENT NO. 19315 1849964

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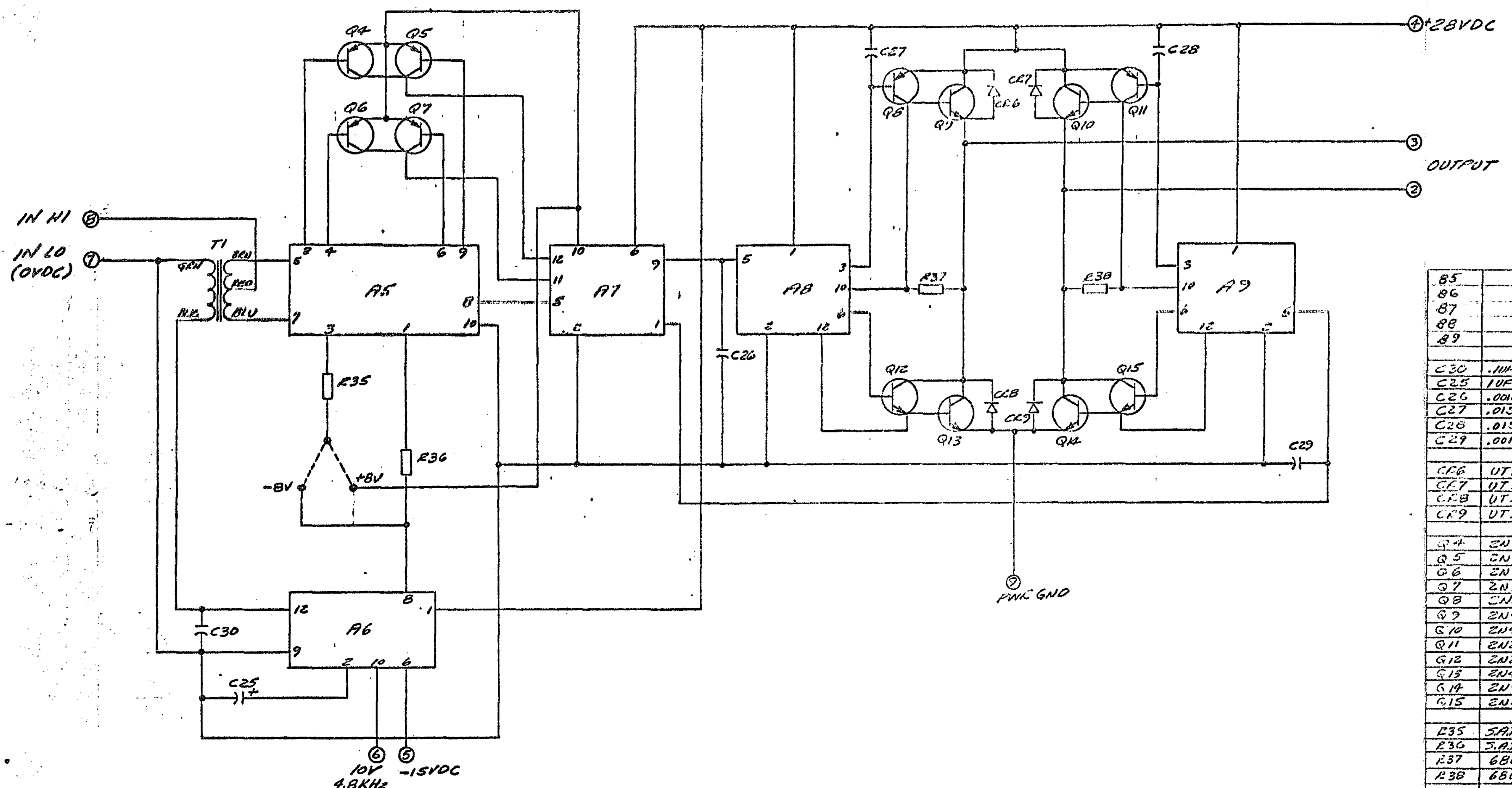

A5		V11101
A6		V11102
A7		V11103
A8		V11104
A9		V11104
C30	.1UF ±10% 50V	VK30BX104K
C25	1UF ±10% 35V	CS13BF105K
C26	.001UF ±10% 200V	CK05CW102K
C27	.015UF ±10% 50V	VK30BX153K
C28	.015UF ±10% 50V	VK30BX153K
C29	.001UF ±10% 200V	CK05CW102K
CR6	UTX210	
CR7	UTX210	
CR8	UTX210	
CR9	UTX210	
Q4	2N722	
Q5	2N722	
Q6	2N722	
Q7	2N722	
Q8	2N2907	
Q9	2N4150 (H.S.)	
Q10	2N4150 (H.S.)	
Q11	2N2907	
Q12	2N2316	
Q13	2N4150(H.S.)	
Q14	2N4150(H.S.)	
Q15	2N2316	
R35	S.A.T. 100K NOM ±5% 1/8W	RC05GF104J
R36	S.A.T. 1K NOM ±5% 1/8W	RC05GF102J
R37	680 ±5% 1/8W	RC05GF681J
R38	680 ±5% 1/8W	RC05GF681J
T1	DIT 20 (UTC)	

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FORM

* — INDICATES SUBASSEMBLY
† — VENDOR ITEM – SEE SOURCE CONTROL OR SPECIFICATION CONTROL DRAWING

— LIMITS OF ACCEPTABLE WORKMANSHIP ARE DEFINED IN ECLIPSE-PIONEER STANDARDS DS-103

HARDNESS

FINISH

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— TOLERANCES ON DECIMALS
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MATERIAL

DR W.D. 7-11-67
CHK
T.D.
MET.

CONTRACT NO.

APPROVAL

APPROVAL

THE Bendix CORPORATION
ECLIPSE-PIONEER DIVISION
TETERBORO, NEW JERSEY, U.S.A.

SCHEMATIC
INTEGRATED POWER
AMPLIFIER

SIZE D | CODE IDENT NO. 19315 | X1849773

SCALE | WT | SHEET

PART NO.

MF	REVISIONS				
	ZONE	LTR	DESCRIPTION	DATE	APPROVED

SYMBOL	DESCRIPTION	PART NO.		SYMBOL	DESCRIPTION	PART NO.
A1	μA 709			R1	10K 1/8W 5%	RC05GF103J
A2	μA 709			R2	10K	RC05GF103J
A3	μA 709			R3	39K	RC05GF393J
A4	μA 709			R4	39K	RC05GF393J
				R5	1.5K	RC05GF152J
C1	470pf 200V ±10%	CK05CW471K		R6	4.7K	RC05GF472J
C2	22pf 200V ±10%	CK05CW220K		R7	1.5K	RC05GF152J
C3	.027pf 50V ±10%	VK30BX273K		R8	4.7K	RC05GF472J
C4	3300pf 200V ±10%	CK06CW332K		R9	11K	RC05GF113J
C5	150pf 200V ±10%	CK05CW151K		R10	2.4K	RC05GF242J
C6	.027μf 50V ±10%	VK30BX273K		R11	11K	RC05GF113J
C7	1μf 35V ±10%	CS13BF105K		R12	2.4K	RC05GF242J
C8	.056μf 50V ±10%	VK30BX563K		R13	2.4K	RC05GF242J
C9	1500pf 200V ±10%	CK06CW152K		R14	5.6K	RC05GF562J
C10	.01μf 50V ±10%	VK30BX103K		R15	10K	RC05GF103J
C11	4700pf 200V ±10%	CK06CW4[illegible]2K		R16	10K	RC05GF103J
C12	220pf 200V ±10%	CK05CW221K		R17	20K	RC05GF203J
C13	6.8μf 35V ±10%	CS13BF685K		R18	20 1/8W 5%	RC05GF200J
C14	5600pf 200V ±10%	CK06CW562K		R19	S.O.T. SEE NOTE 4	RC05GF---J
C15	560pf 200V ±10%	CK05CW561K		R20	62K 1/8W 5%	RC05GF623J
C16	27μf 10V ±10%	CS13BC276K		R21	S.O.T. SEE NOTE 3	RC05GF---J
C17	560pf 200V ±10%	CK05CW561K		R22	1.5K 1/8W 5%	RC05GF152J
C18	3.3μf 15V ±10%	CS13BD335K		R23	11	RC05GF110J
C19	2.7μf 15V ±10%	CS13BD275K		R24	62K	RC05GF623J
C20	4700pf 200V ±10%	CK06CW472K		R25	10K	RC05GF103J
C21	39μf 10V ±10%	CS13BC396K		R26	15K	RC05GF153J
C22	220pf 200V ±10%	CK05CW221K		R27	180	RC05GF181J
C23	.027μf 50V ±10%	VK30BX273K		R28	15K	RC05GF153J
C24	.027μf 50V ±10%	VK30BX273K		R29	4.7K	RC05GF472J
				R30	100	RC05GF101J
CR1	1N966			R31	15K	RC05GF153J
CR2	1N483B			R32	15K	RC05GF153J
CR3	1N483B			R33	270	RC05GF271J
CR4	1N483B			R34	1.5K	RC05GF152J
CR5	1N483B			R35	15K 1/8W 5%	RC05GF153J
Q1	2N910					
Q2	3N74					
Q3	3N90					

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UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN INCHES
- TOLERANCES ON DECIMALS
2 PLACE ±.03 3 PLACE ±.005 4 PLACE ±.0005

HARDNESS

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MATERIAL

DR
CHK
ENGR
T.D.
MET
REL
APPD

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THE BENDIX CORPORATION NAVIGATION & CONTROL DIVISION TETERBORO, NEW JERSEY, U.S.A.

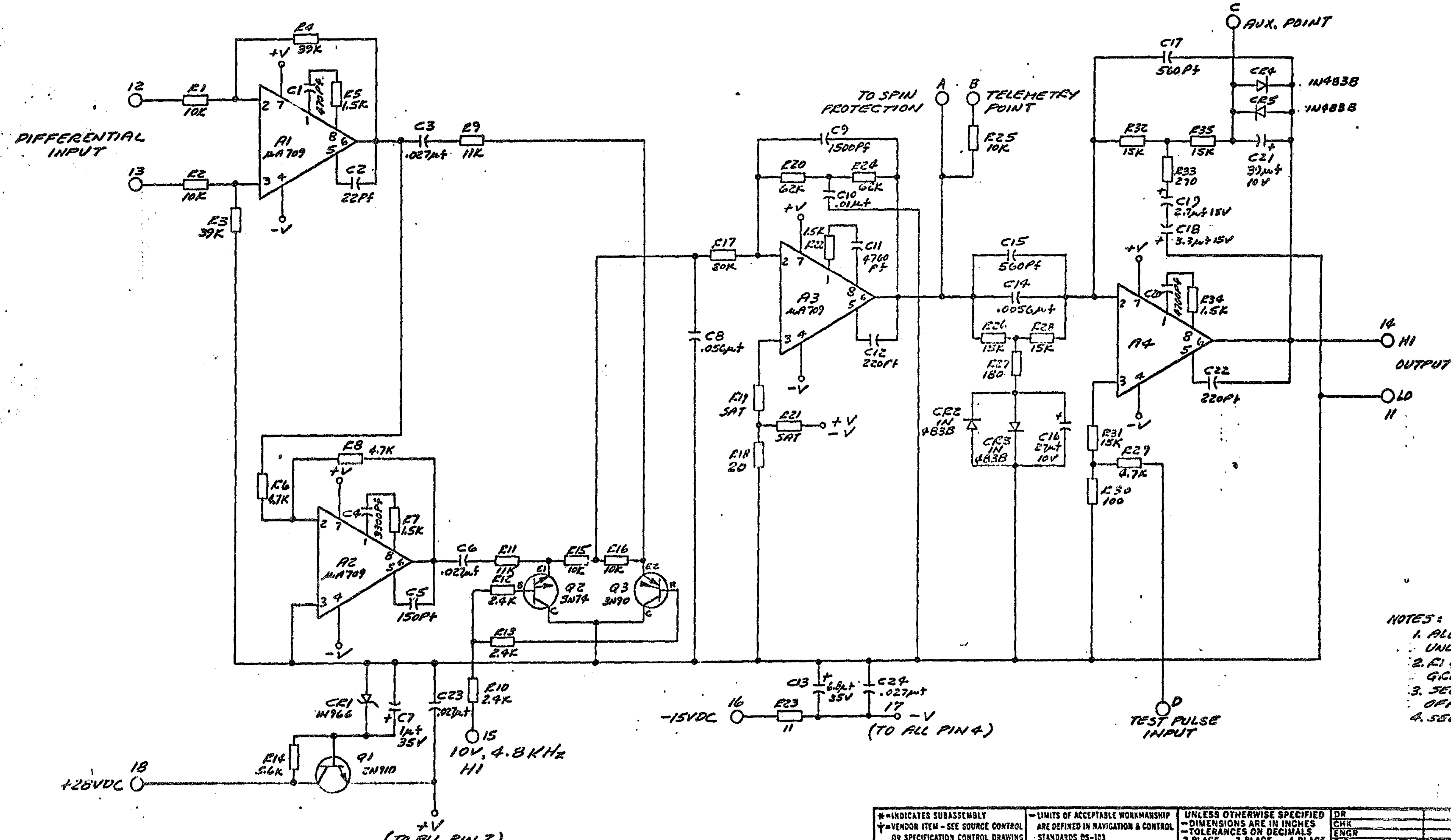
SIZE D CODE IDENT NO. 19315 1849953

SCALE

FORM 10412/1

PART NO.

MF	REVISIONS				
	ZONE	LTR	DESCRIPTION	DATE	APPROVED



NOTES:
1. ALL RESISTORS ARE 1/8W 5% RC05 UNLESS OTHERWISE SPECIFIED
2. R1 & R2 ARE TO BE USED FOR SETTING GRADIENT AT 2V/DEG.
3. SELECT R21 & POLARITY TO NULL OFFSET IN COMPLETE LOOP.
4. SELECT R19 FOR OPTIMUM DRIFT

*=INDICATES SUBASSEMBLY ✝=VENDOR ITEM - SEE SOURCE CONTROL OR SPECIFICATION CONTROL DRAWING	—LIMITS OF ACCEPTABLE WORKMANSHIP ARE DEFINED IN NAVIGATION & CONTROL STANDARDS DS-103	UNLESS OTHERWISE SPECIFIED —DIMENSIONS ARE IN INCHES —TOLERANCES ON DECIMALS 2 PLACE ±.03 3 PLACE ±.005 4 PLACE ±.0005	DR CHK ENGR T.D. MET REL APPD	THE BENDIX CORPORATION NAVIGATION & CONTROL DIVISION TETERBORO, NEW JERSEY, U.S.A.
HARDNESS		MATERIAL		SCHEMATIC PRE AMP - DETECTOR - LEAD NETWORK
FINISH			CONTRACT NO.	
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2.0 INDEX OF PHASE III MT'S

MT	TITLE	AUTHOR
8247	Theoretical Investigation of the Stabilizing Networks of the Micro-electronic Servo Loop in Conjunction with Phase III of NAS 8-11916	B. Friedman
8249	Preamp and Detector Test Results In with NAS 8-11916	B. Friedman
8250	Test Results on the Active Network in Conjunction with NAS 8-11916	B. Friedman
8252	Active Filter and Overall Preamp Detector Filter and Network Test Results in Conjunction with NAS 8-11916	B. Friedman
8253	Investigation of V1102 Microcircuit Failure in Conjunction with NAS 8-11916	B. Friedman
8254	Integrated Circuit Test Results in Conjunction with NAS 8-11916	B. Friedman
8255	Investigation of Additional Micro-circuit Failures in Conjunction with NAS 8-11916	B. Friedman

To: Engineering File - MT-8247

From: B. Friedman

Issue: Original

Date: 9 June 1967

Theoretical Investigation of the Stabilizing Networks of the Microelectronic Servo Loop in Conjunction with Phase III of NAS 8-11916

Prepared by: B. Friedman

B. Friedman

THE BENDIX CORPORATION
NAVIGATION-CONTROL DIVISION
TETERBORO, 07608 NEW JERSEY

1.0 SCOPE

The purpose of this report is to present a description of the frequency characteristics of the stabilizing networks for the Saturn Microelectronics Phase III.

2.0 CIRCUIT CONFIGURATION

Presented in Figure 1 is the schematic of the stabilizing network. This schematic was obtained from N.A.S.A., M.S.F.C., and has undergone no modification at this time. However, the diodes in the input and feedback networks have been omitted for this analysis.

3.0 CIRCUIT ANALYSIS

The input network is a standard form and its transfer impedance is

$$A\left[\frac{T_3S + 1}{T_1T_2S^2 + T_1S + 1}\right]$$

where:

$$A = 2R_1$$

$$T_1 = R_2C_1 + 2R_1C_2$$

$$T_2 = \frac{R_1(R_1 + 2R_2)C_1C_2}{R_2C_1 + 2R_1C_2}$$

$$T_3 = (R_2 + \frac{R_1}{2})\, C_1$$

The feedback network is not, however, a standard form and it is therefore necessary to desire it. The feedback circuit is shown again in Figure 2 and referring to that diagram, the following equation hold if it is assumed that $e_o = 0$ since it is terminated at the input to a operational amplifier.

(1) $i_o = i_4 + i_1$

(2) $i_1 = e_i C_1 S$

(3) $i_4 = e_4/R_1$

$$e_4 = e_i \; \frac{(R_3 + 1/C_3S)(R_1)}{(R_3 + R_1 + 1/C_3S)} \Bigg/ \left(\frac{(R_3 + 1/C_3S)R_1}{(R_3 + R_1 + 1/C_3S)} + Z_2\right)$$

$$e_4 = e_i \; \frac{R_3 + 1/C_3S)\ (R_1)}{(R_3 + 1/C_3S)(R_1) + Z_2(R_3 + 1/C_3S + R_1)}$$

$$i_4 = \frac{e_i\ (R_3 + 1/C_3S)}{(R_3 + 1/C_3S)(R_1) + R_2(R_3 + 1/C_3S + R_1)}$$

$$i_o = e_iC_iS + \frac{e_i\ (R_3 + 1/C_3S)}{(R_3 + 1/C_3S)(R_1) + Z_2(R_3 + 1/C_3S + R_1)}$$

$$\frac{e_i}{i_o} = \frac{R_3R_1 + R_1/C_3S + Z_2R_3 + Z_2/C_3S + R_1Z_2}{R_1R_3C_1S + R_1C_1S/C_3S + Z_2R_3C_1S + Z_2C_1S/C_3S + R_1Z_2C_1S + R_3 + 1/C_3S}$$

$$Z_2 = R_2 + 1/C_2S$$

$$R_2 = R_1 = R$$

$$\frac{e_i}{i_o} = \frac{R_3R + R/C_3S + RR_3 + R_3/C_2S + R/C_3S + 1/C_2C_3S^2 + R^2 + R/C_2S}{2RR_3C_1S + 2R\frac{C_1}{C_3} + \frac{C_1}{C_2}(R_3 + 1/C_3S + R) + R^2C_1S + R_3 + 1/C_3S}$$

Combining terms and simplifying

$$\frac{e_o}{i_i} = \frac{2R\,(R_3C_2C_3S^2 + C_2S + \frac{R}{2}C_2C_3S^2) + (C_3S\,(R_3 + R) + 1)}{S(C_2+C_1)\left[S^2(2R_3+R)\,RC_3\frac{C_1C_2}{C_2+C_1} + S((2R)\frac{C_1C_2}{C_2+C_1} + R_3C_3\frac{C_1}{C_2+C_1} + R_3\frac{C_3C_2}{C_2+C_1} + 1\right]}$$

if $C_2 \gg C_1$ $\qquad C_2 + C_1 = C_2$

$$\frac{e_o}{i_i} = \frac{C_2C_3(2RR_3+R^2)S^2 + \left[(2RC_2) + (R_3+R)C_3\right]S + 1}{SC_2\left[(2RR_3+R^2)(C_3C_1)S^2 + \left\{(R_3+R)\frac{(C_1C_3)}{C_2} + 2RC_1 + R_3C_3\right\}S + 1\right]}$$

As a proof of the validity of the above transfer impedance, it is only necessary to let C_2 approach infinity such that its impedance approaches zero and the transfer function should be the same form as the function of the input networks. This is the case and so the transfer impedance will be considered valid.

4.0 FREQUENCY RESPONSE

Using the transfer functions of the input and feedback networks, an overall transfer function for the stabilizing networks can be obtained. Substituting element values the transfer function is

$$\frac{(37X10^{-6}\ s^2 + 48.8X10^{-4}s + 1)(1.345X10^{-2}s^2 + 119.3X10^{-2}\ s + 1)}{(117X10^{-2}s)(19.3X10^{-8}\ s^2 + 4.17X10^{-4}\ s + 1)(20.7X10^{-2}\ s + 1)}$$

It is interesting to also look at the transfer function of the stabilizing networks without the series capacitor C_2 in the feedback path. This transfer function is,

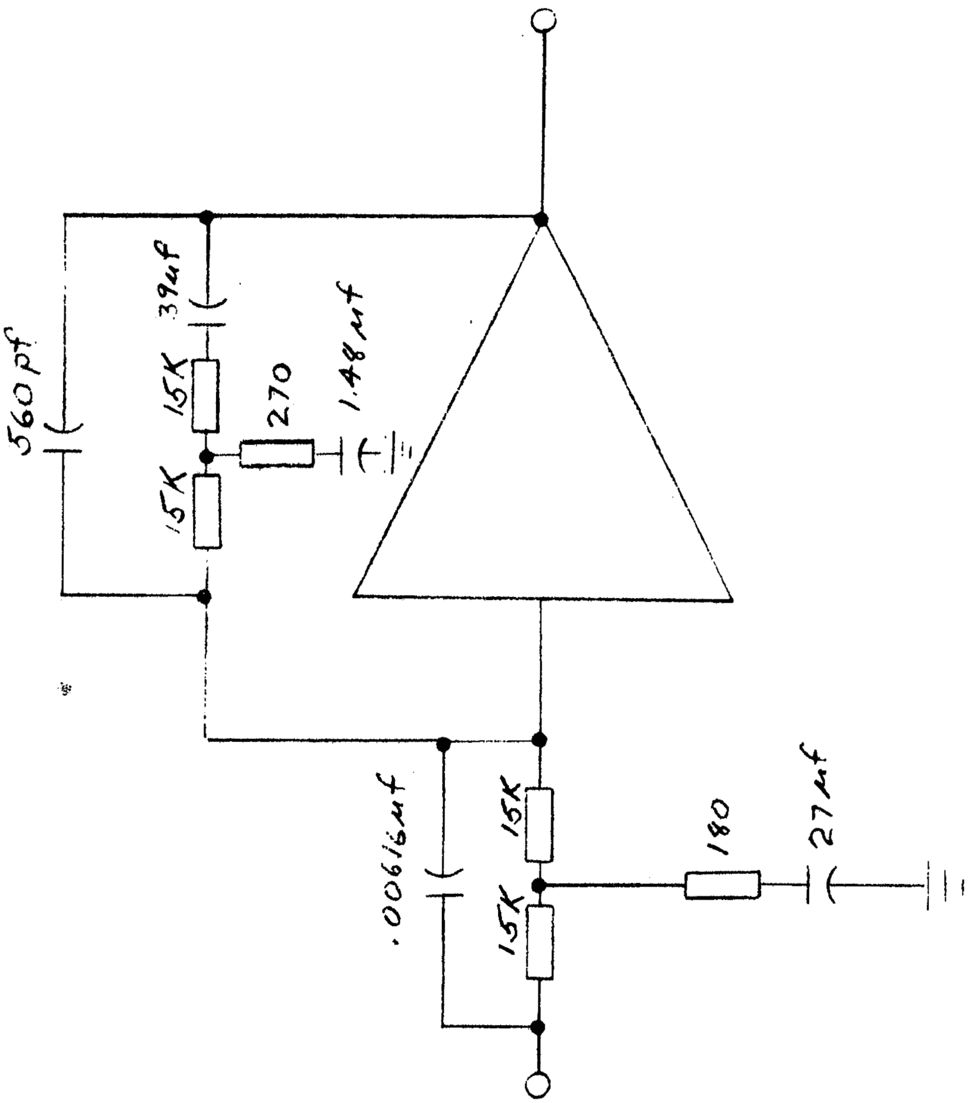
$$\frac{(11.5X10^{-3}\ s+1)(37X10^{-6}\ s^2 + 48.8X10^{-4}\ s+1)}{(20.7X10^{-2}\ s+1)(19.3X10^{-8}\ s^2 + 4.17X10^{-4}\ s+1)}$$

Tables 1 and 2 contain theoretical data for the frequency response of the networks with and without the series C_2 capacitor. Graphical response is shown in Figures 3 and 4.

5.0 CONCLUSION

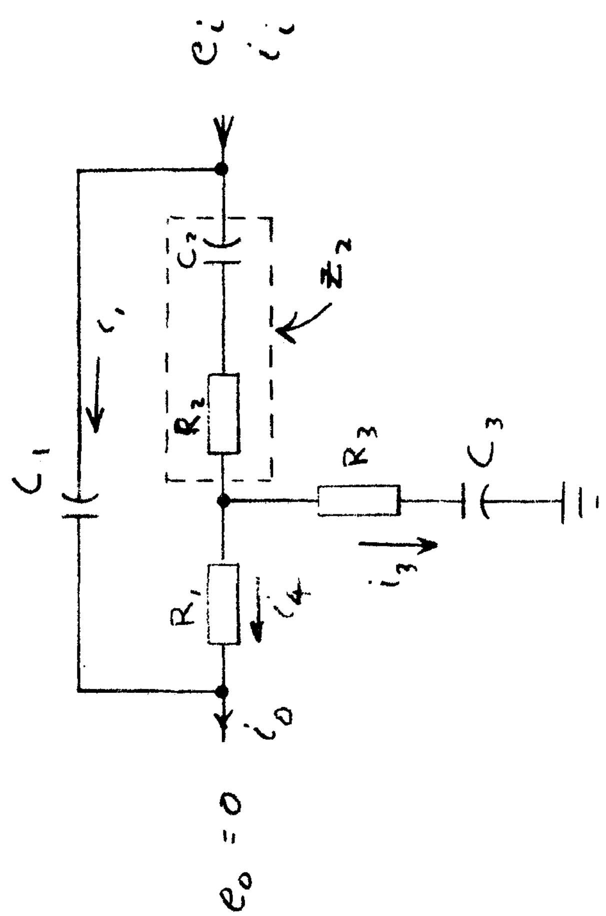
From the theoretical frequency response data it can be seen that the addition of a series capacitor in the d.c. feedback path gives a great increase in d.c. gain, (theoretically infinite). This in turn is equal to an infinite stiffness at d.c. This tremendous network gain is not practically possible and the maximum gain to be realized, assuming zero leakage through the capacitor at d.c.

is limited to the open loop gain of the operational amplifier being used (typically 45,000 for a µA709). It can also be readily seen from the theoretical data that this capacitor only exerts a noticeable influence on the circuit at d.c. and very low frequencies. At a later date experimental data will be presented and correlated to this theoretical data.



STABILIZING NETWORKS

fig 1



FEEDBACK NETWORK

fig. 2

Response With C_2

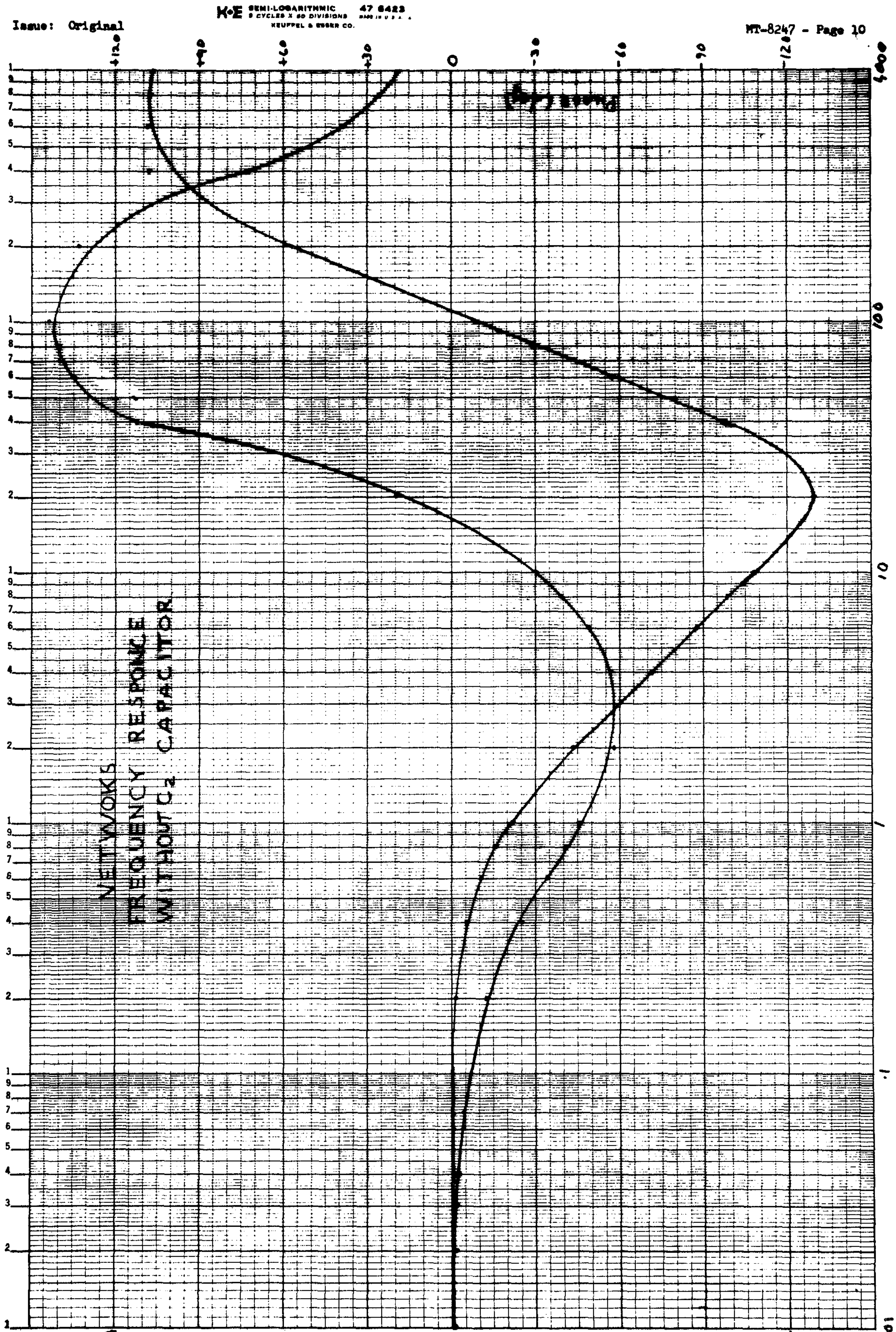
Freq Cps	Gain db	Gain v/v	Phase deg
.01	22.696	13.64	-86.442
.02	16.744	6.874	-82.930
.03	13.334	4.642	-79.507
.04	10.987	3.543	-76.210
.06	7.867	2.474	-70.109
.07	6.773	2.181	-67.342
.08	5.876	1.967	-64.776
.09	5.132	1.806	-62.413
.10	4.507	1.680	-60.249
.20	1.426	1.178	-47.399
.40	-0.486	.9456	-43.814
.60	-1.761	.8165	-47.198
.80	-2.970	.7104	-51.133
1.0	-4.123	.6221	-54.416
2.0	-8.743	.3655	-61.455
4.0	-14.186	.1953	-58.526
6.0	-17.402	.1349	-50.670
8.0	-19.611	.1046	-41.759
10.0	-21.269	.08641	-32.533
20.0	-25.977	.05025	19.716
40.0	-19.377	.1074	113.056
60.0	-11.422	.2685	134.941
80.0	-5.958	.5036	141.740
100.0	-1.782	.8145	143.871
200.0	11.348	3.693	133.081
400.0	21.652	12.09	73.264
600.0	21.889	12.43	38.767
800.0	21.419	11.77	25.941
1,000	21.131	11.39	19.627
2,000	20.698	10.84	9.096
4,000	20.583	10.69	4.462
6,000	20.561	10.67	2.964
8,000	20.554	10.66	2.220
10,000	20.550	10.65	1.775

Table I

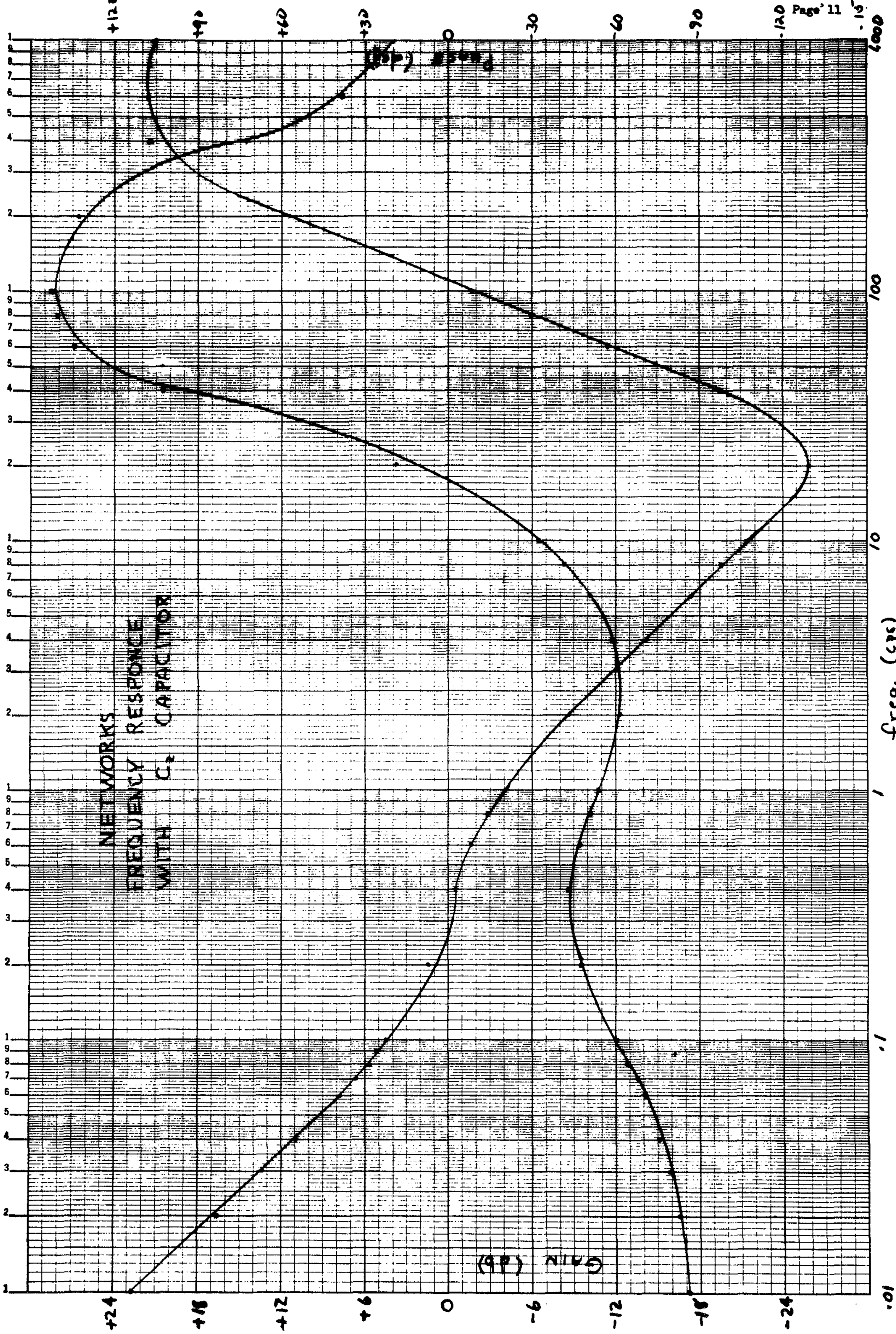
RESPONSE WITHOUT C_2 CAPACITOR

FREQ CPS	GAIN db	GAIN V/V	PHASE deg
.010	-.001	.9999	-.688
.020	-.003	.9997	-1.375
.030	-.007	.9992	-2.062
.040	-.012	.9987	-2.748
.060	-.026	.9970	-4.117
.070	-.036	.9959	-4.800
.080	-.047	.9946	-5.480
.090	-.059	.9932	-6.159
.10	-.073	.9917	-6.839
.20	-.284	.9679	-13.432
.40	-1.038	.8874	-25.187
.60	-2.060	.7888	-34.521
.80	-3.177	.6937	-41.542
1.0	-4.286	.6105	-46.703
2.0	-8.847	.3611	-57.519
4.0	-14.270	.1934	-56.441
6.0	-17.476	.1337	-49.171
8.0	-19.676	.1038	-40.540
10.0	-21.325	.08585	-31.503
20.0	-26.003	.05010	20.377
40.0	-19.383	.1074	113.431
60.0	-11.423	.2684	135.199
80.0	-5.958	.5036	141.735
100	-1.781	.8147	144.028
200	11.351	3.694	133.16
400	21.655	12.10	73.304
600	21.892	12.43	38.793
800	21.422	11.78	25.961
1,000	21.134	11.39	19.643
2,000	20.701	10.84	9.104
4,000	20.586	10.74	4.466
6,000	20.565	10.67	2.967
8,000	20.557	10.66	2.222
10,000	20.554	10.66	1.777

TABLE 2


NETWOKS
FREQUENCY RESPONCE
WITHOUT C2 CAPACITOR

K+E SEMI-LOGARITHMIC 5 CYCLES X 60 DIVISIONS 47 6423 MADE IN U.S.A. KEUFFEL & ESSER CO.



To: Engineering File - MT-8249 Issue: Original

From: Bruce Friedman Date: 2 October 1967

Preamp and Detector Test Results

In Conjunction with NAS 8-11916

Prepared by: B. Friedman

B. Friedman

THE BENDIX CORPORATION

NAVIGATION-CONTROL DIVISION

TETERBORO, 07608 NEW JERSEY

ABSTRACT

This report contains test results obtained on a breadboard model of the Preamp and Detector circuitry of the P.W.M. servo loop in conjunction with NAS 8-11916.

1.0 INTRODUCTION

Testing was performed on this circuitry to permit evaluation of this revised Preamp-Detector configuration as required by NAS 8-11916, Phase III.

2.0 CONCLUSION

From the testing performed it can be concluded that the revised Preamp Detector circuitry is well suited for its intended operation in the microelectronic servo loop.

3.0 SUMMARY OF RESULTS

3.1 Quiescent Current

Results of this test are presented in Table 1.

3.2 A.C. and D.C. Null

This data is presented in Table 2.

3.4 Frequency Response

Frequency Response data is shown in Table 4.

3.5 Decoupling

Decoupling data is presented in Table 5.

4.0 TESTING

4.1 Circuit Diagram

All testing was carried out on a breadboard model of the circuit shown in Figure 2.

4.2 Test Conditions

The Quiescent Current, AC and DC Null, and AC Gain and Linearity tests were performed at 25°C and 70°C. All other tests were performed only at 25°C.

QUIESCENT CURRENT

(input shorted)(no load)

BIAS SUPPLY	25°C	70°C
+15	10.5ma	10 ma
-15	9.5ma	9 ma

Table 1

AC & DC NULL

(input shorted)

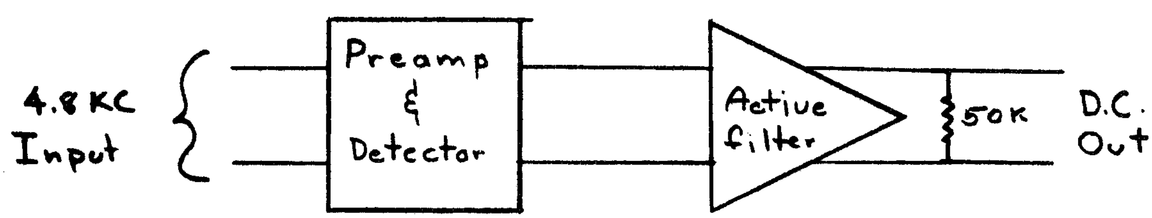
	25°C	70°C
DC mv	+1.1	-8.7
AC mv	6.0	3.5

Table 2

DC GAIN & LINEARITY

INPUT 4.8 KC mv RMS	V.D.C. OUT	
	25 °C	70 °C
0	+ 1.6 mv	- 8.7 mv
30	228 mv	+ 229 mv
50	330 mv	387 mv
100	758 mv	786 mv
200	1.515 V	1.583 V
400	3.028	3.171
600	4.539	4.758
700	5.292	5.547
800	6.044	6.333
900	6.323	6.249
1000	6.309	6.227
1100	6.299	6.217

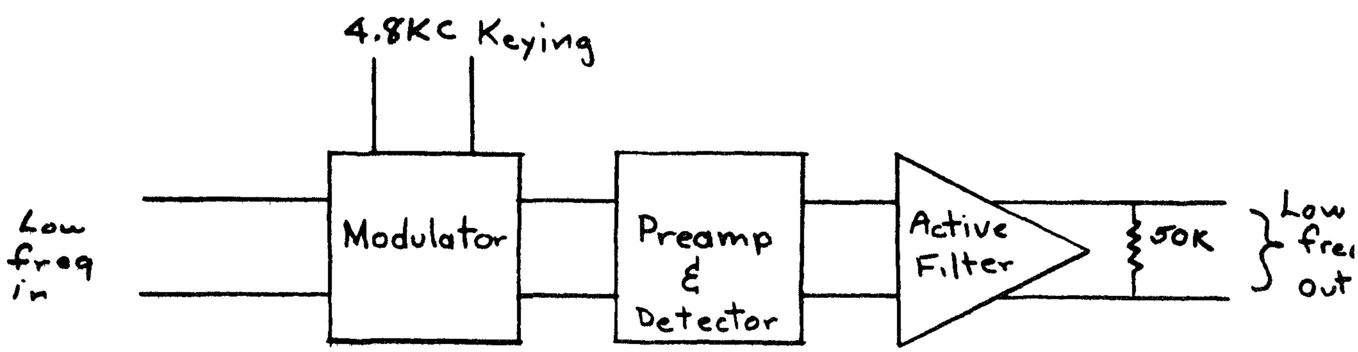
Table 3



Frequency Response

FREQ	INPUT	OUTPUT	Gain db	Phase deg.
1	1V PP	7V PP	16.9	0
5		12V PP	21.6	5°
10				5°
20				5°
50				7°
100				13°
200				25°
300				32°
400				42°
500				58°

Table 4

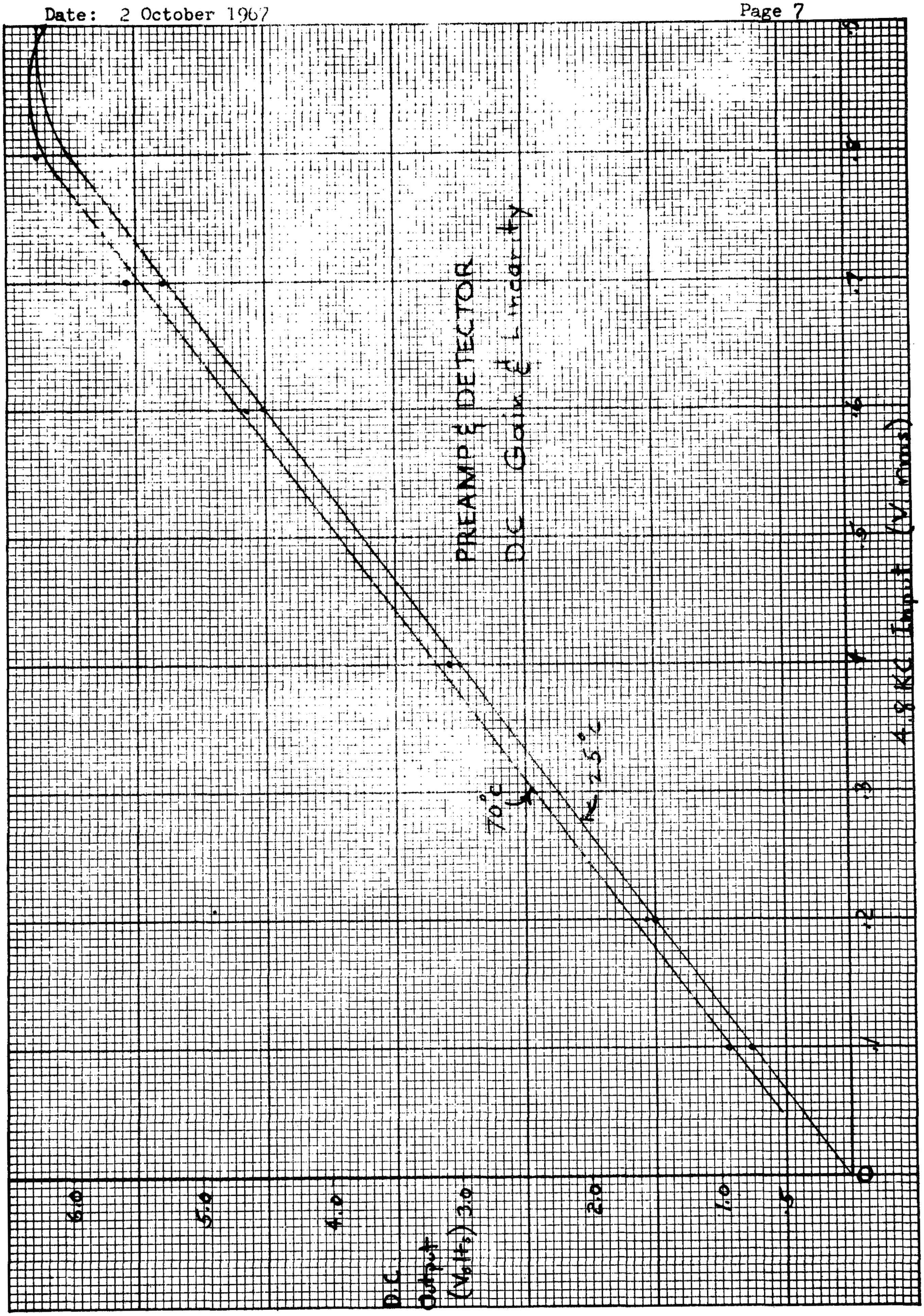


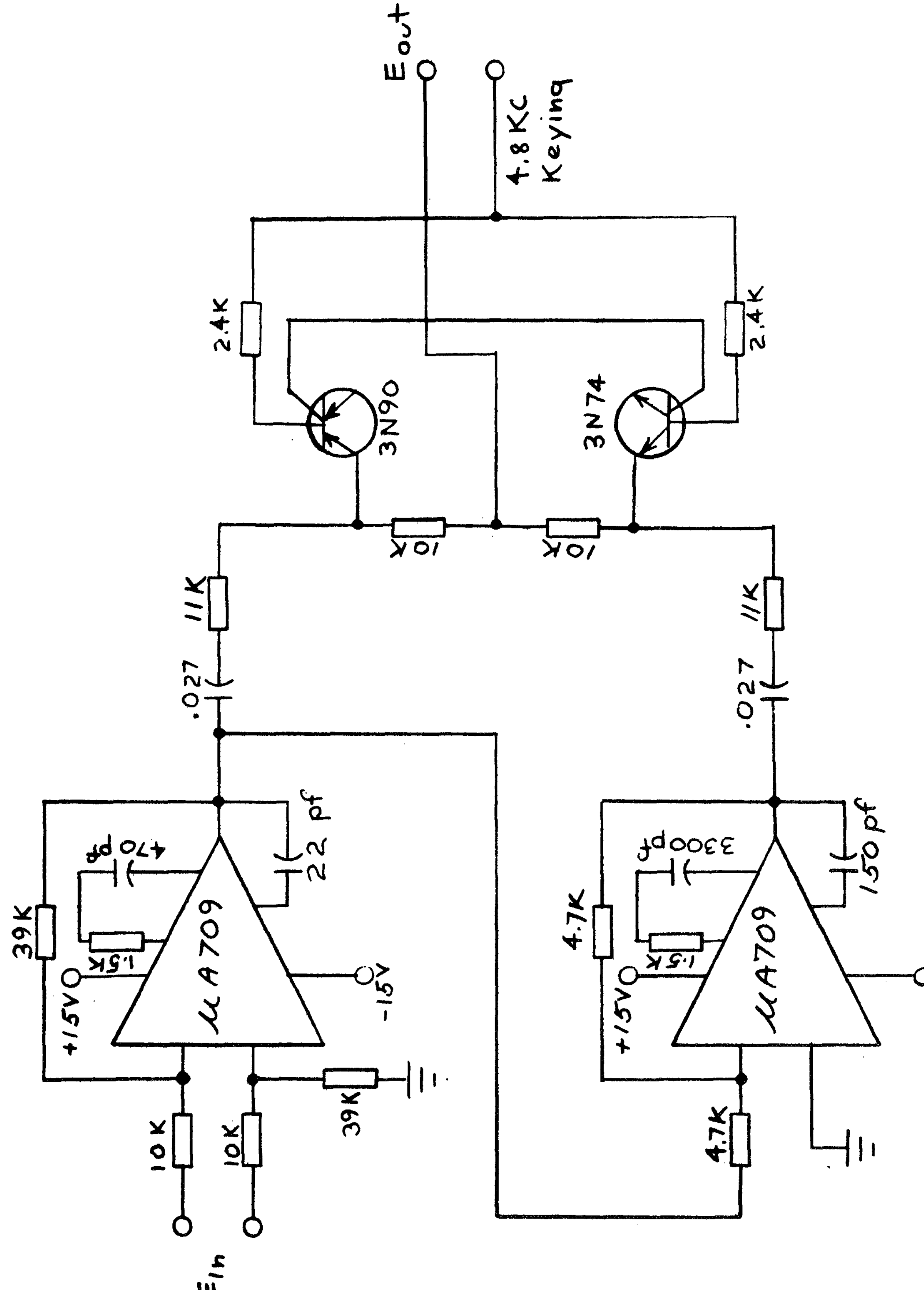
DECOUPLING

Input freq	+15 V Output (rms)	-15 V Output (rms)
60	1 mv	1 mv
120	8 mv	3 mv
400	8 mv	4.2 mv
800	16 mv	4.8 mv
2.4 KC	10.5 mv	4.8 mv
4.8 KC	10.5 mv	3.8 mv
9.6 KC	15.0 mv	6.0 mv

Table 5

1 V rms noise coupled to (+ & -) bias lines. Input shorted, output read across 50K active filter load.


PREAMP & DETECTOR
DC Gain & Linearity
70°C
25°C
4.8 KC Input (V. rms)
D.C. Output (Volts)
6.0
5.0
4.0
3.0
2.0
1.0
.5
0
.1
.2
.3
.4
.5
.6
.7
.8
.9



Preamp Detector

fig 2

To: Engineering File - MT-8250 Issue: Original

From: Bruce Friedman Date: 2 October 1967

Test Results on the Active

Network In Conjunction with

NAS 8-11916

Prepared by: B. Friedman

B. Friedman

THE BENDIX CORPORATION

NAVIGATION-CONTROL DIVISION

TETERBORO, 07608 NEW JERSEY

ABSTRACT

Contained in the document are the results of the testing carried out on the active networks of the microelectronic servo loop in conjunction with Phase III of contract NAS 8-11916. Also included is a comparison of the frequency response of the network with theoretical predictions.

1.0 INTRODUCTION

The testing and evaluation of this circuitry was carried out as per contractial requirements to ascertain the ability of the proposed networks to meet the theoretical requirements imposed upon it by design. It was also intended to bring to light any existing problem areas and to assure compatability with servo requirements.

2.0 CONCLUSIONS AND RECOMMENDATIONS

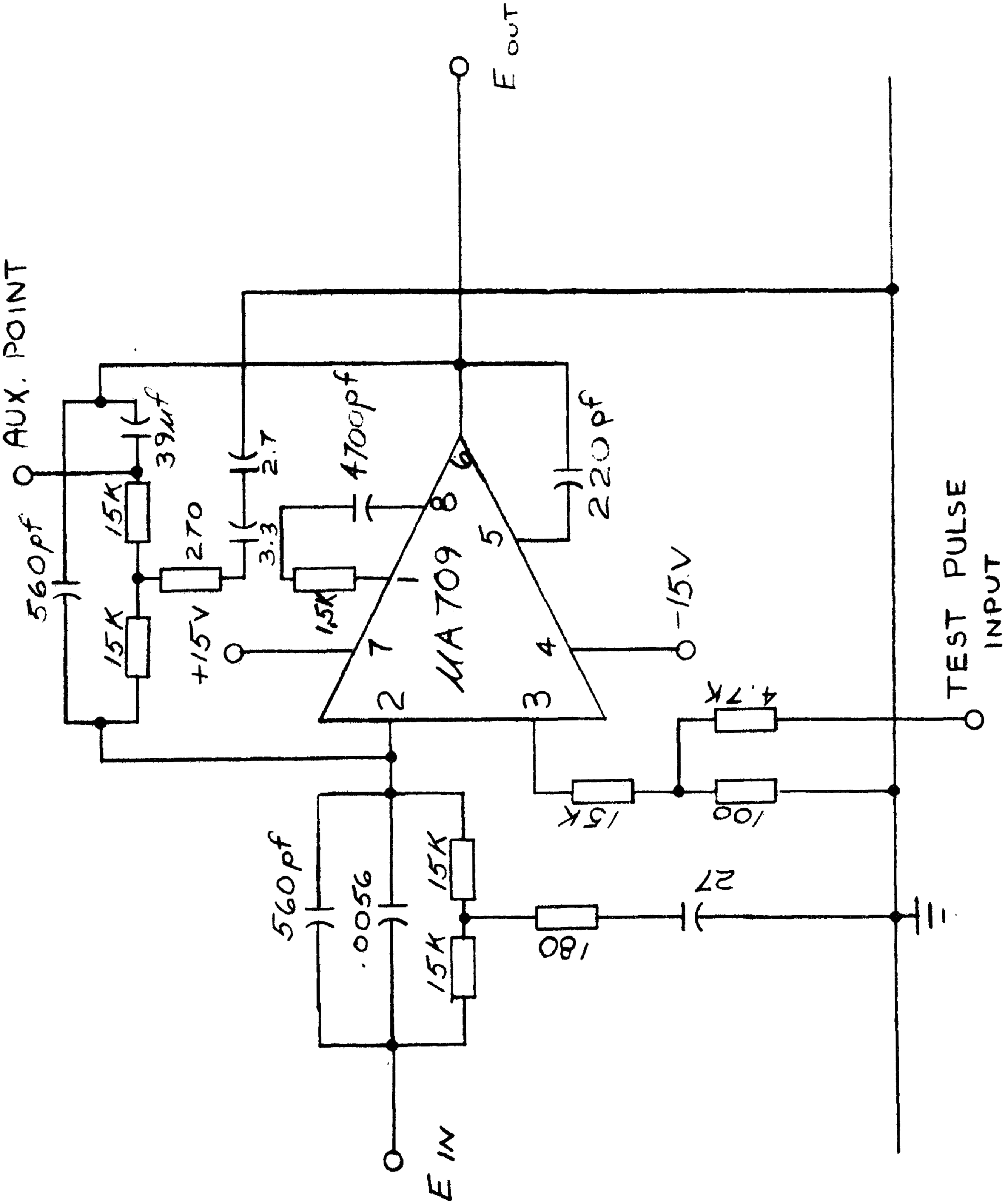
As a result of the testing and evaluation performed it can be concluded that the active network in question is capable of performing its assigned task in the microelectronic servo loop. The test data shows close agreement with the theoretically derived response requirements and the temperature testing could not show up and discrepancies in circuit performance.

3.0 SUMMARY OF RESULTS

Test and theoretical comparison data for the circuit of Fig. 1 with the 39µf capacitor shorted to facilitate testing is presented in Table 1 through 6.

4.0 TEST CONDITIONS

All testing carried out on the active networks was done with the 39µf capacitor bypassed by connecting the auxiliary point shown in Fig. 1 to the output terminal. This was necessitated by the fact that the charge stored by the capacitor and the leakage associated with this element prohibit valid testing open loop with the capacitor.


E OUT
AUX. POINT
39μf
2.7
4700pf
220pf
15K
270
3.3
560pf
15K
1.5K
+15V
-15V
μA709
TEST PULSE
INPUT
4.7K
15K
100
560pf
.0056
15K
15K
180
27
E IN

AC & DC NULL

(INPUT SHORTED, 10 K LOAD)

	E_{OUT} 25°C	E_{OUT} 70°C
DC mV	9.45	6.0
AC mV	1.45	3.3

QUIESCENT CURRENT

(INPUT SHORTED, 10K LOAD)

BIAS SUPPLY	25°C	70°C
+ 15V	4.4 ma	4.5 ma
− 15V	4.4 ma	4.5 ma

TABLE 1

Frequency Response @ 25 °C

Freq. Cps.	Input	Output	Gain V/V	Gain DB	Phase Deg
.01	.5V	.5V	1	0	-2°
.05	.5V	.5V	1	0	-4°
.1	.5V	.5V	1	0	-8°
.2	.1V	.1V	1	0	-18°
.5	.5V	.5V	1	0	-38°
1.0	1V	.5V	.5	-6.02	-45°
1.5		.4V	.4	-8.90	-55°
2.0		.35V	.35	-9.1	-58°
3.0		.30	.30	-10.9	-58°
5.0		.20	.20	-13.98	-47°
10.0		.12	.12	-18.40	-25°
15.0		.07	.07	-23.6	0°
20.0		.065	.065	-24.0	30°
25.0		.060	.060	-24.44	50°
30.0		.070	.070	-23.2	75°
33.0		.080	.080	-22.00	90°
35.0		.080	.080	-22.00	100°
40.0		.10	.10	-20.0	115°
50.0		.16	.16		130°
80.0		.50	.50	-6.02	145°
100		.80	.80	-1.94	135°
150		1.80	1.80	5.1	130°
200	.5V	1.90	3.80	11.6	125°
280		3.6	7.2	17.1	115°
300		4.2	8.4	18.48	105°
400		5.0	10.0	20.0	68°
500		5.2	10.4	20.32	45°
1KC		4.8	9.6	19.50	24°
4.8KC		4.8	9.6	19.50	0°
9.6KC		4.9	9.8	19.70	0°

TABLE 2

Frequency Response @ 70°C

Freq	Input	Output	Gain	Gain	Phase
Cps			V/V	db	Deg.
.01	.5V	.5V	1	0	-0°
.05	.5V	.5V	1	0	-2°
.1	.5V	.5V	1	0	-5°
.2	.1V	.1V	1	0	-6°
.5	.5V	.5V	1	0	-15°
1.0	1V	.7V	.7	-3.1	-45°
1.5		.5V	.5	-6.02	-57°
2.0		.35V	.35	-9.1	-61°
3.0		.24	.24	-12.4	-63°
5.0		.15	.15	-16.46	-51°
10.0		.12	.12	-18.40	-27°
15.0		.10	.10	-20.0	0°
20.0		.06	.06	-24.44	20°
25.0		.08	.08	-22.0	35°
30.0		.10	.10	-20.0	65°
33.0		.11	.11	-19.16	85°
35.0		.11	.11	-19.16	100°
40.0		.14	.14	-17.06	120°
50.0		.20	.20	-13.98	130°
80.0		.50	.50	-6.02	140°
100		.80	.80	-1.94	145°
150		1.80	1.80	5.1	140°
200	.5V	1.90	3.80	11.6	135°
280		3.70	7.40	17.4	110°
300		4.20	8.40	18.48	105°
400		5.60	11.20	21.0	70°
500		5.60	11.20	21.0	50°
1KC		5.40	10.80	20.68	20°
4.8KC		5.20	10.40	20.32	0°
9.6KC		5.20	10.40	20.32	3°

TABLE 3

Theoretical Frequency Response

	Gain	Gain	Phase
	DB	V/V	deg
.01	-.001	.999	-.68
.02	-.003	.999	-1.37
.03	-.007	.999	-2.06
.04	-.012	.998	-2.74
.06	-.026	.997	-4.11
.07	-.036	.995	-4.80
.08	-.047	.994	-5.48
.09	-.059	.993	-6.15
.10	-.073	.991	-6.83
.20	-.283	.967	-13.43
.40	-1.038	.887	-25.18
.60	-2.06	.788	-34.52
.80	-3.17	.693	-41.54
1.0	-4.28	.610	-46.70
2.0	-8.84	.361	-57.51
4.0	-14.2	.193	-56.44
6.0	-17.4	.133	-49.17
8.0	-19.6	.103	-40.54
10.0	-21.3	.085	-31.50
20.0	-26.0	.050	20.37
40.0	-19.3	.107	113.43
60.0	-11.4	.268	135.19
800	-5.95	.503	141.93
100.0	-1.78	.814	144.02
200.0	11.35	3.69	133.16
400	21.65	12.10	73.30
600	21.89	12.43	38.79
800	21.42	11.78	25.96
1000	21.13	11.39	19.64
2000	20.70	10.84	9.10
4000	20.58	10.70	4.46
6000	20.56	10.67	2.96
8000	20.55	10.66	2.22
10,000	20.55	10.66	1.77

TABLE 4

K+E SEMI-LOGARITHMIC 47 6423
3 CYCLES X 60 DIVISIONS
KEUFFEL & ESSER CO.

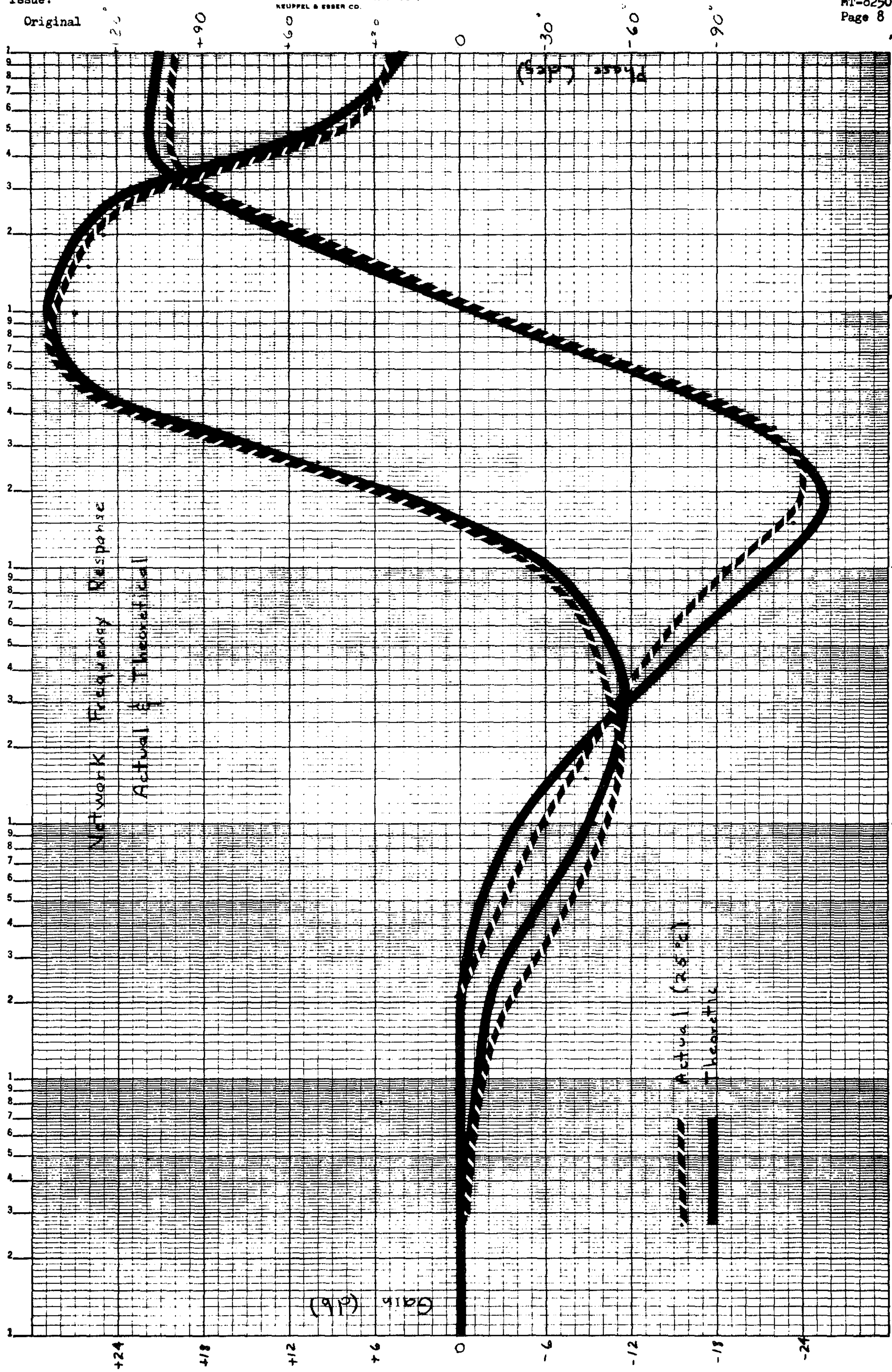


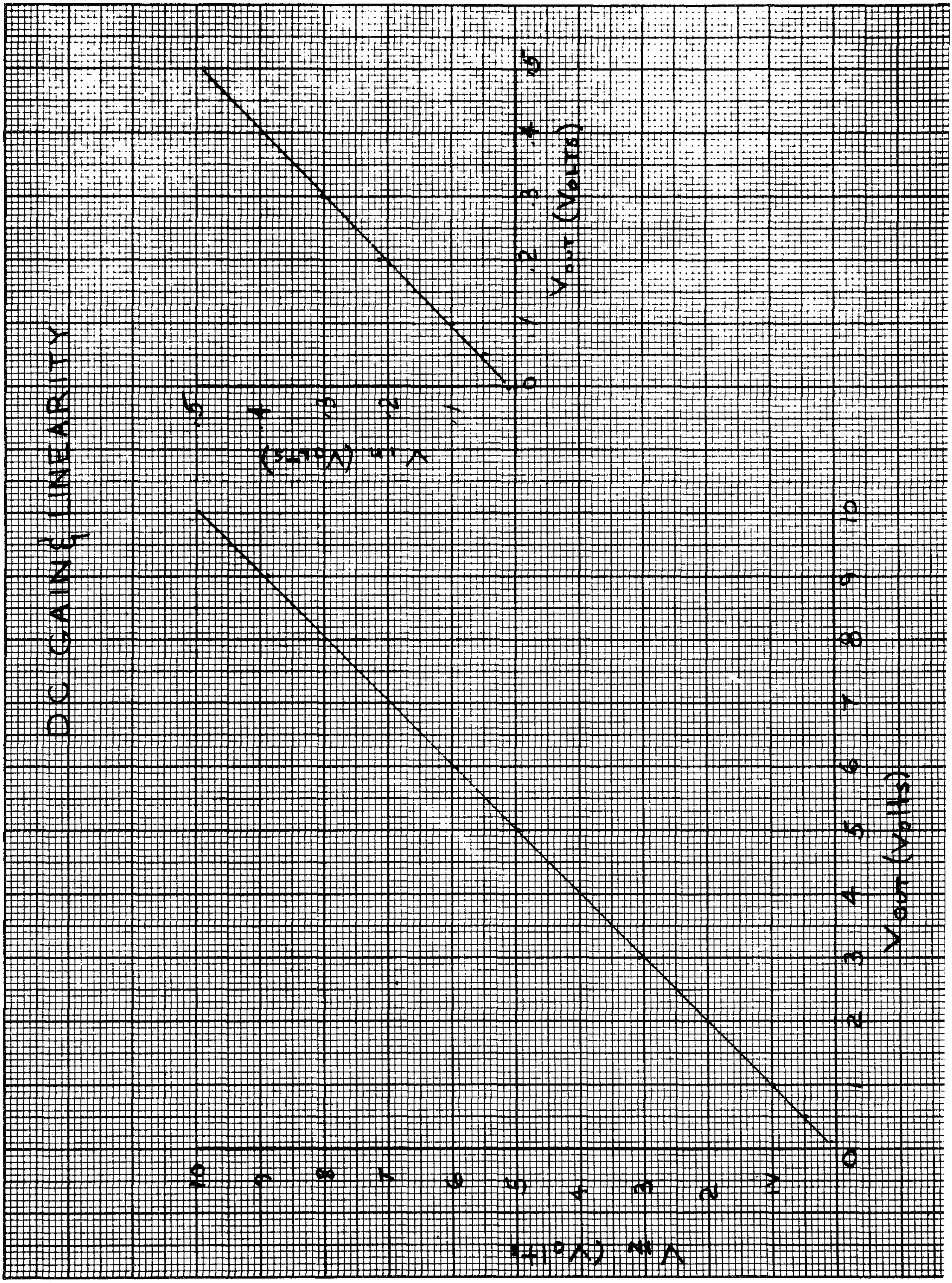
fig 2

DC GAIN & LINEARITY

(10K LOAD)

DC Input	OUTPUT 25°C	OUTPUT 70°C
0	+9.3mv	+5.0mV
1mv	+7.9	+4.2
2	+7.0	+3.4
3	+6.0	+2.4
5	+3.9	+.50mv
10	-1.2	-4.5
50	-44.4	-42.4
.1V	-98.4	-96.0
.2	-214	-195.0
.3	-301	-300.
.4	-398	-401
.5	-498	-498
1.0	-984	-.985V
3.0	-3.09V	-2.98
5.0	-4.97	-4.99
6.0	-5.91	-5.87
7.0	-6.92	-6.88
9.0	-8.89	-8.87
10.0	-9.94	-9.89

TABLE 5


DC GAIN & LINEARITY
V out (Volts)
0 .1 .2 .3 .4 .5
V in (Volts)
.1 .2 .3 .4 .5
V out (volts)
0 1 2 3 4 5 6 7 8 9 10
V in (Volts)
1 2 3 4 5 6 7 8 9 10

DECOUPLING

NOISE FREQ	OUTPUT mv rms	
	+15V	-15V
60	40	24
120	40	24
400	40	24
800	40	24
2400	40	27
4800	65	65
9600	110	120

(1 V rms noise coupled to bias supplies)

(INput SHORTED, No LOAD)

TABLE 6

To: Engineering File - MT-8252

From: B. Friedman

Issue: Original

Date: 16 October 1967

Active Filter and Overall Preamp

Detector Filter and Networks Test

Results in Conjunction with

NAS 8-11916

Prepared by: B. Friedman

B. Friedman

THE BENDIX CORPORATION

NAVIGATION-CONTROL DIVISION

TETERBORO, 07608 NEW JERSEY

ABSTRACT

This report contains test results obtained on a breadboard model of the Active Filter. Also presented are preliminary results of testing carried out on a Preamp-Detector Active Filter and Stabilizing Networks configuration.

1.0 INTRODUCTION

Testing was carried out on these circuits to permit evaluation as required by NAS 8-11916, Phase III, and to point out any shortcomings in the circuit performance.

2.0 CONCLUSION

As a result of the testing described in this report as well as that presented in MT's 8249 and 8250 it is reasonable to conclude that the loop circuitry including Preamp, Detector, Active Filter and Stabilizing Networks is well suited to perform its intended function in a microelectronic servo loop.

3.0 SUMMARY OF RESULTS

3.1 Active Filter

All tests were performed on a breadboard model of the circuit of Figure 1. The quiescent current data presented shows values of current with both the filter and networks energized.

3.1.1 Quiescent Current

(input shorted, no load)

Bias Supply	+25°C	+70°C
+15V	4.5 ma	4.3 ma
-15V	4.5 ma	4.3 ma

3.1.2 Null

Null	25°C	70°C
DC MV	2.3 mv	4.8 mv
AC MV	1.6 mv	3.5 mv

3.1.3 Frequency Response

Frequency response data is presented in Figures 2 and 3. Figure 4 is the results of a computer analysis of the frequency response and Figure 5 shows a graphical comparison of actual data versus theoretical predictions.

3.2 Preamp, Detector, Filter and Networks

3.2.1 Quiescent Current

(input shorted, no load)

Bias Supply	25°C	70°C
+15V	10.0 ma	10.0 ma
-15V	10.0 ma	10.0 ma

3.2.2 Null

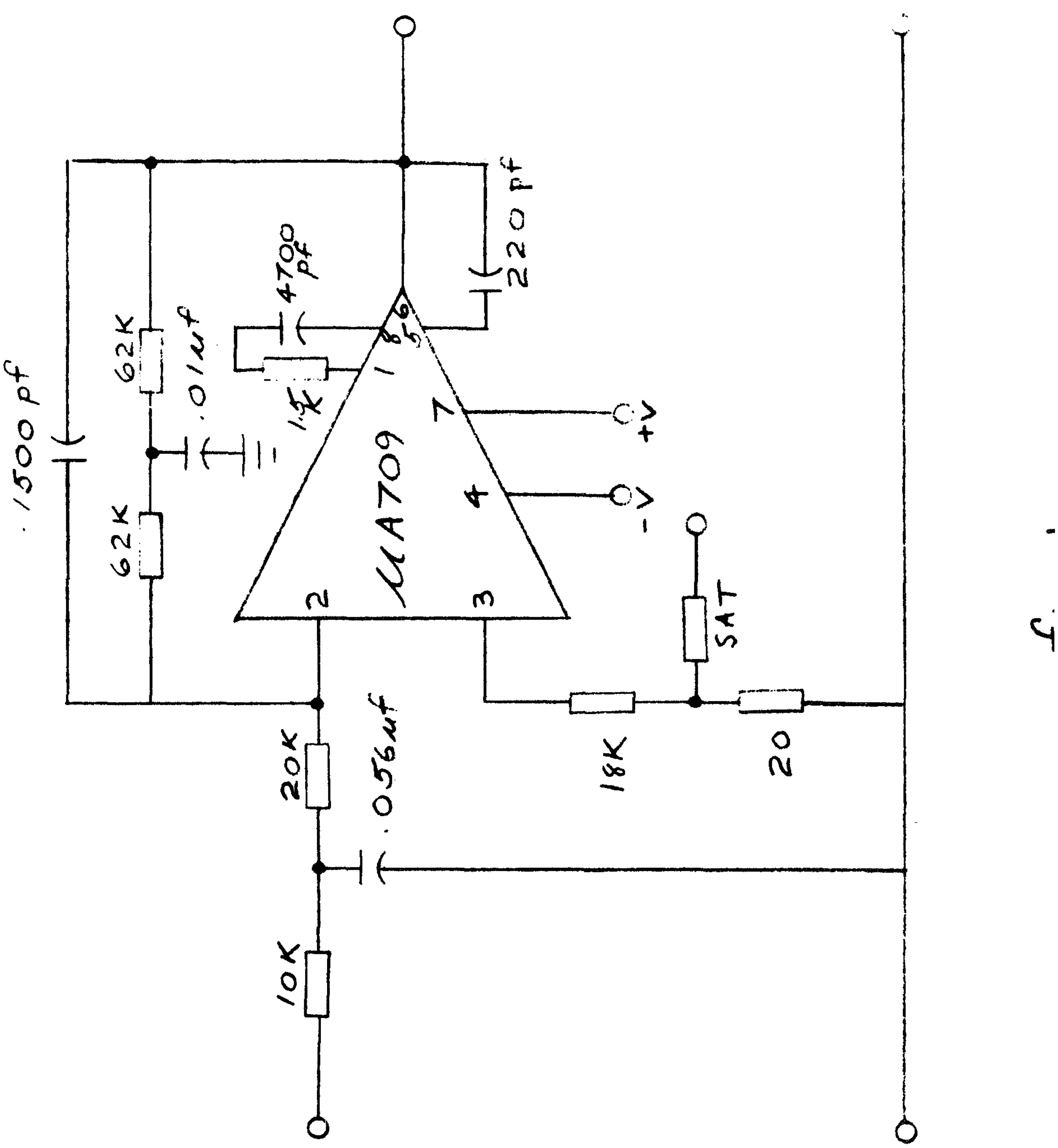
(input shorted, 10K load)

Null	25°C	70°C
AC MV	3.81 mv	5.00 mv
DC MV	6.80 mv	14.0 mv

3.2.3 Gain

Data for gain from 4.8KC preamp input to d.c. output across 10K load is presented in Fig. 6. Figure 7 is a graph of this data.

ACTIVE FILTER



FILTER FREQUENCY RESPONSE
25°C

Freq	INPUT	Output	Gain	Gain	Phase
CPS			V/V	db	deg (-)
1	.5 V pp	2.0 VPP	4.0	12.0	0°
10		2.2	4.4	12.8	4°
100		2.1	4.2	12.4	5°
200		2.1	4.2	12.4	8°
300		2.1	4.2	12.4	15°
400		2.2	4.4	12.8	38°
500		2.4	4.8	13.6	55°
600		2.4	4.8	13.6	78°
800		1.65	3.3	10.4	120°
1 Kc		.95	1.90	5.6	140°
1.2		.65	1.30	2.2	152°
1.5		.40	.80	-2.0	160°
2.0		.20	.40	-8.0	175°
5.0		.03	.06	-24.5	
7.0		.02	.04	-28.0	
8.0		.015	.03	-30.4	
9.0		.012	.024	-32.3	
9.6		.01	.02	-34.0	
10 Kc		.01	.02	-34.0	
20	160 mv. RMS	1.2 mv RMS	.0075	-42.5	
40 Kc	"	.9 mv RMS	.0056	-45.0	

fig. 2

FILTER FREQUENCY RESPONSE
70°C

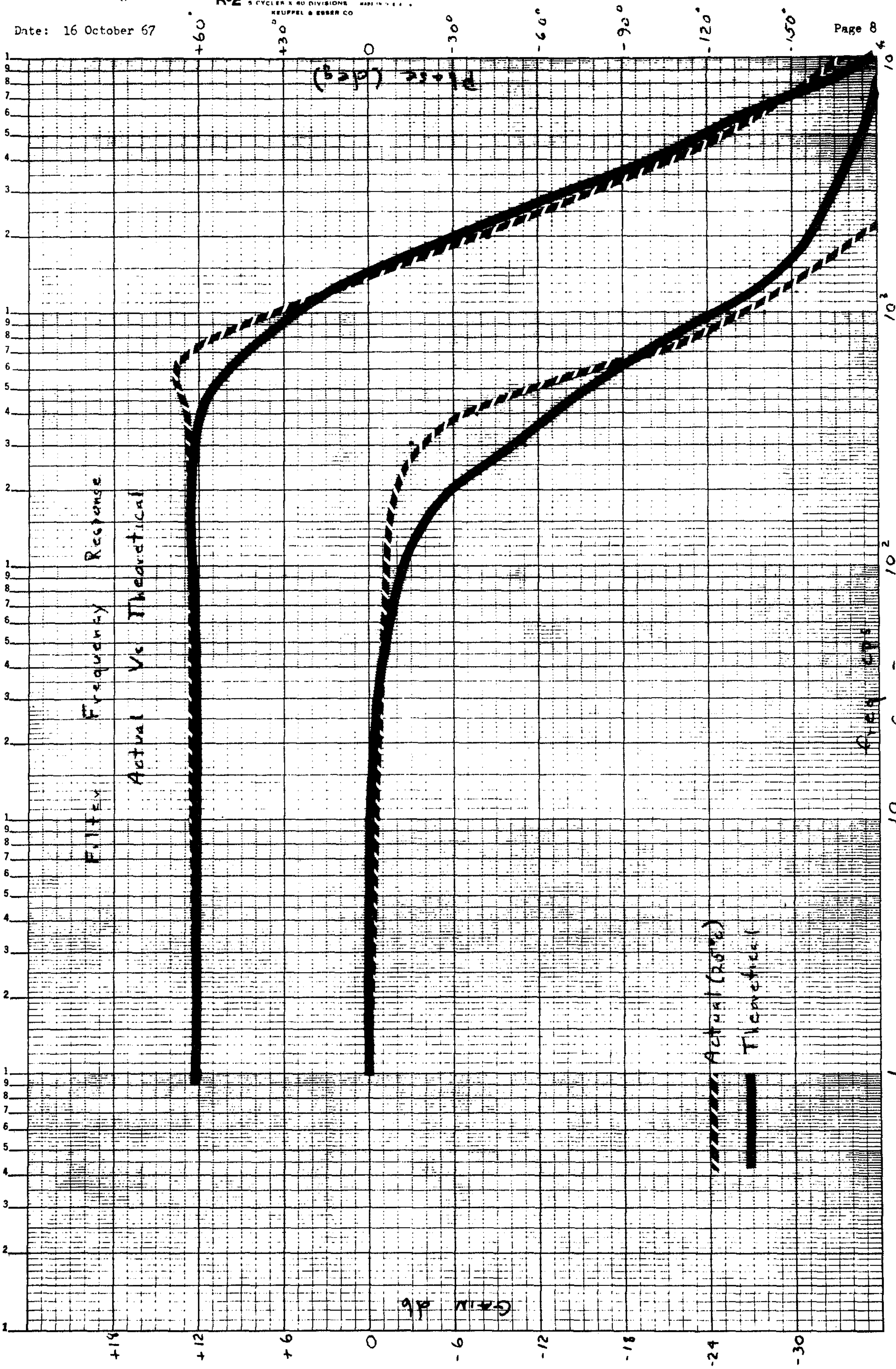
FREQ	INPUT	OUTPUT	Gain	Gain	Phase
CPS			V/V	db	DEG (-)
1	.5Vpp	2.0Vpp	4.0	12.0	0
10		2.2	4.4	12.8	8°
100		2.2	4.4	12.8	8°
200		2.3	4.6	13.2	16°
300		2.3	4.6	13.2	26°
400		2.3	4.6	13.2	39°
500		2.4	4.8	13.6	55°
600		2.4	4.8	13.6	79°
800		1.6	3.2	10.1	125°
1 KC		.9	1.8	5.08	135°
1.2		.6	1.2	1.60	160°
1.5		.35	.70	-3.1	178°
2.0		.19	.38	-8.5	
5.0		.033	.066	-23.7	
7.0		.025	.050	-26.0	
8.0		.020	.040	-28.0	
9.0		.015	.030	-30.5	
9.6		.015	.030	-30.5	
10KC	140mv rms	2.6mv rms	.0185	-34.8	
20KC		2.1mv rms	.0150	-36.5	
40KC		2.0mv rms	.0143	-36.8	

fig. 3

Theoretical Frequency
RESPONSE

Freq. cps	Gain V/v	Gain db	Phase deg(-)
1	4.14	12.34	.135
10	4.14	12.34	1.35
100	4.12	12.29	13.5
200	4.06	12.18	27.1
400	3.80	11.60	56.1
600	3.11	9.87	86.4
800	2.21	6.91	111.0
1KC	1.52	3.65	127.4
2 KC	.385	-8.28	156.7
4 KC	.0947	-20.46	168.4
6 KC	.0419	-27.5	172.6
8 KC	.0235	-32.5	174.5
10 KC	.0150	-36.4	175.6

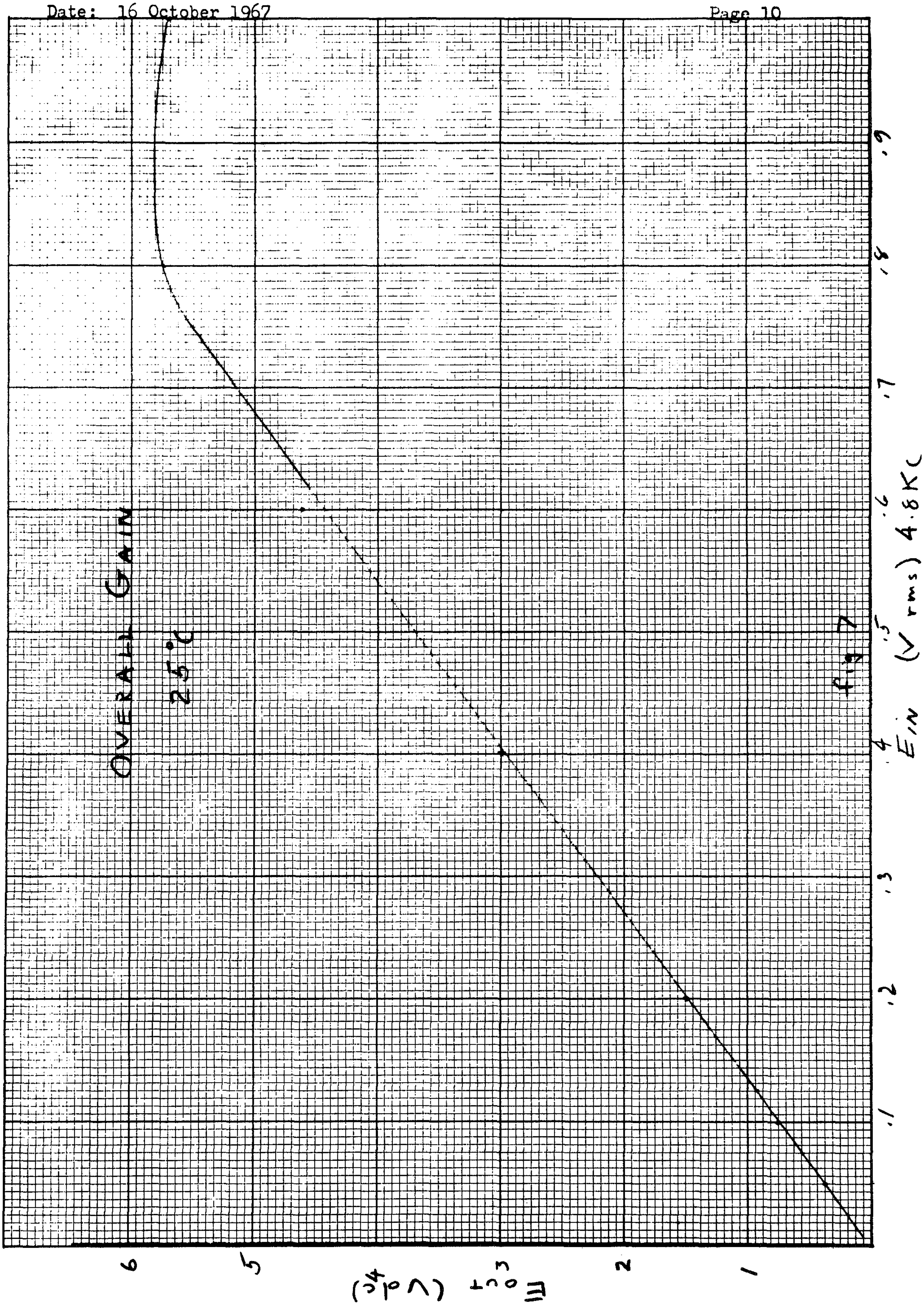
fig. 4


Filter Frequency Response
Actual Vs Theoretical
Phase (deg)
Gain db
Freq cps
Fig 5
Actual (20°C)
Theoretical

PREAMP, DETECTOR FILTOR & NETWORKS OVERALL GAIN

	25°C	70°C
Ein (rms) 4.8KC	D.C OUT	D.C. OUT
0	+6.8mv	+2.50mv
10 mv	-7.2 mv	-63.8mv
30 mv	-226 mv	-221.5mv
50 mv	-381 mv	-379mv
70 mv	-536mv	-536.5mv
100mv	-769mv	-777 mv
150mv	-1.155V	-1.168V
200mv	-1.546V	-1.554V
400mv	-3.098V	-3.123 V
600mv	-4.643V	-4.688V
800mv	-5.755V	-5.623V
1V	-5.734V	-5.600V

Fig. 6


OVERALL GAIN
25°C
fig 7
EIN (V rms) 4.8KC
.1
.2
.3
.4
.5
.6
.7
.8
.9
Eout (V dc)
1
2
3
5
6

To: Engineering File - MT-8253

From: B. Friedman

Issue: Original

Date: November 30, 1967

INVESTIGATION OF V1102 MICROCIRCUIT FAILURE IN CONJUNCTION WITH NAS 8-11916

Prepared by: B. Friedman

B. Friedman

THE BENDIX CORPORATION
NAVIGATION AND CONTROL DIVISION
TETERBORO, NEW JERSEY

ABSTRACT

This report contains a description of a malfunction discovered in a V1102 microcircuit presently being evaluated as part of NAS 8-11916. Also contained is a failure analysis performed on the device and a recommendation for closer vendor visual inspection and improved cleaning procedures to insure non-reoccurance of this type of failure.

1.0 INTRODUCTION

This report is presented to describe a failure encountered in a integrated circuit V1102. This particular device is used in the triangle wave generator of the microelectronic servo loop being evaluated under NAS 8-11916, as shown in N/C print X1849773. Any malfunction in this particular device would result in a degradation in the performance of the entire system and possibly a loss of entire loop operation.

2.0 CONCLUSION AND RECOMMENDATIONS

As a result of the failure analysis described in this document it can be concluded that the presence of a metallic particle in the device package can cause the failure by shorting two surface points on the chip and causing excessive current to the device and subsequent forward biasing of the isolation diodes. After conferring with the manufacturer it has been decided that closer visual inspection is required prior to sealing the device, along with improved cleaning procedures and personnel awareness.

3.0 DESCRIPTION

3.1 EVIDENCE OF MALFUNCTION

During testing of the integrated circuit P.W.M. configuration an operation discrepancy in the V1102 device was evidenced by a nonlinearity in the triangle wave, causing a resultant nonlinearity in P.W.M. characteristics, an excessive drift, and a dc level on the output of the triangle wave generator.

3.2 FAILURE ANALYSIS

Comparison of the device in question with a properly operating device yielded the results presented below in Table 1 with pin numbers being referenced to Figure 1. The dc level present at pins 11 and 12 is indicative of a leakage current flowing to the output. By substituting an external resistance from the collector to the SAT capacitor the malfunction was removed. At this point it was decided to remove the cap from the device and examine the device under a high power scope. Photo micrographs are presented in Figures 2 and 3. Under enlargement it is possible to see evidences of excessive current flow and the resultant opening in the metallization between B+ and the N type tub. Also visable is a conductor shorting the N type tub to the output pad. From the visable evidence it appears that a metallic conductor present before sealing, lodged itself in the position shown in the photos. Referring to Figure 1 it can be seen that if a short (such as shown in the pictures) was placed between the N type tub and the output pad, pin 12, the only resistance between B+ and ground would be the dc resistance of the external transformer. This would cause the heavy current flow in evidence in the photos and probably the open in the metallization between B+ and the N type tub. With this open condition and the short between the N type tub and the output, the distributed diodes associated with a P type resistor in a N type tub would be forward biased creating a leakage path to the output. Meetings with the manufacturer at his facility tend to establish this as the cause of failure. The vendor has concurred with the findings of N/C and has assured that much closer visual inspection would be carried out on all subsequent orders. The vendor has also promised to instruct personnel of the problem so that their inspection and cleaning procedures be improved.

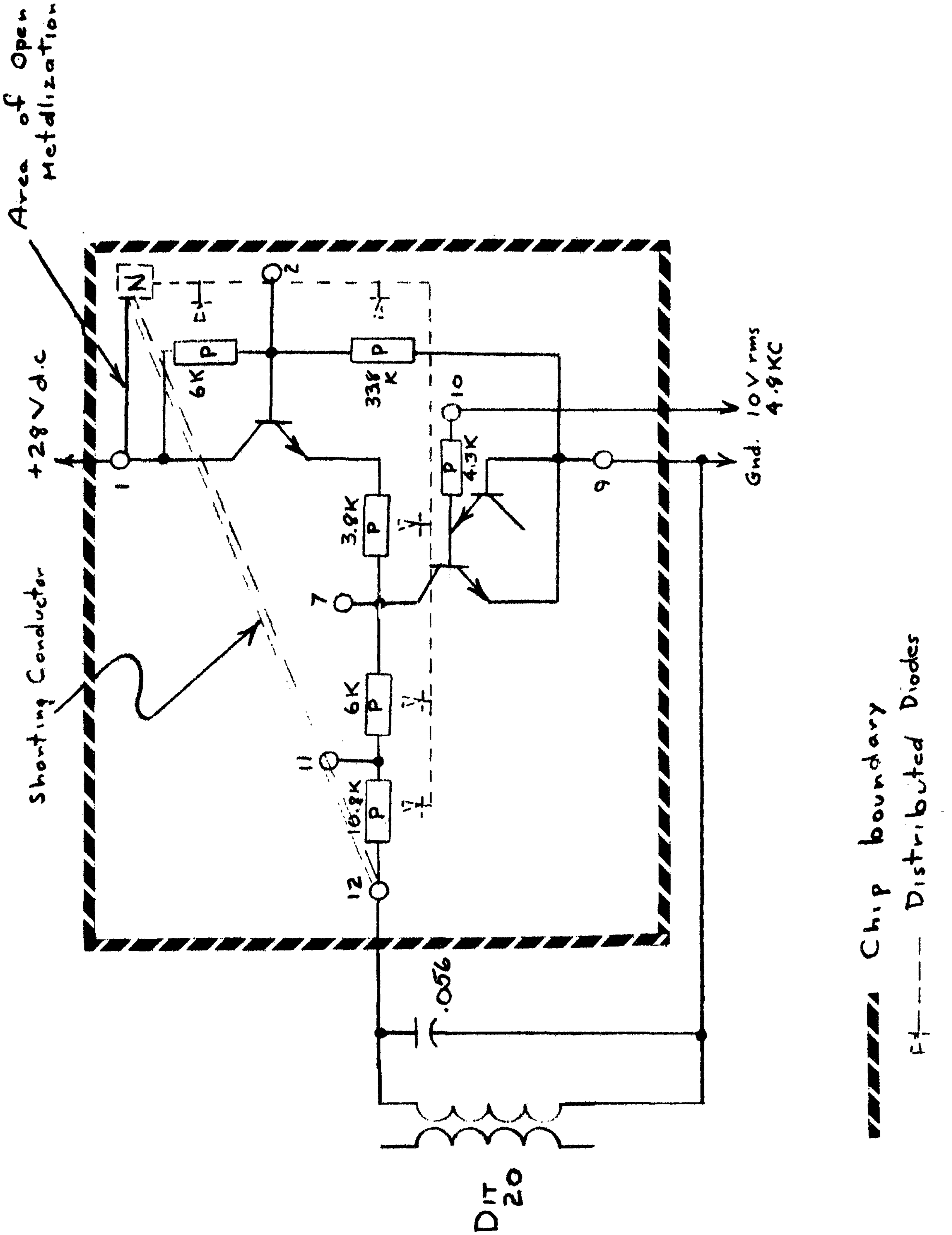

Area of Open Metallization
+28 V d.c
Shorting Conductor
6K
3.8K
6K
4.3K
10 V rms
4.9 KC
Gnd.
.056
Chip boundary
Distributed Diodes

fig 1

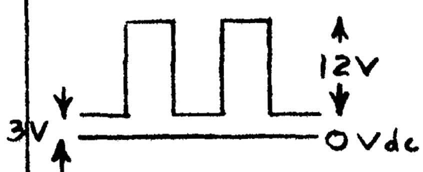
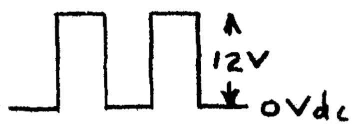
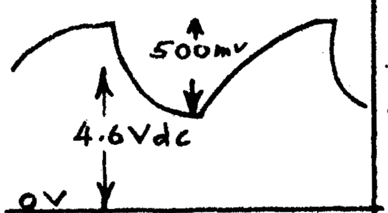
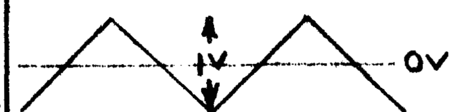
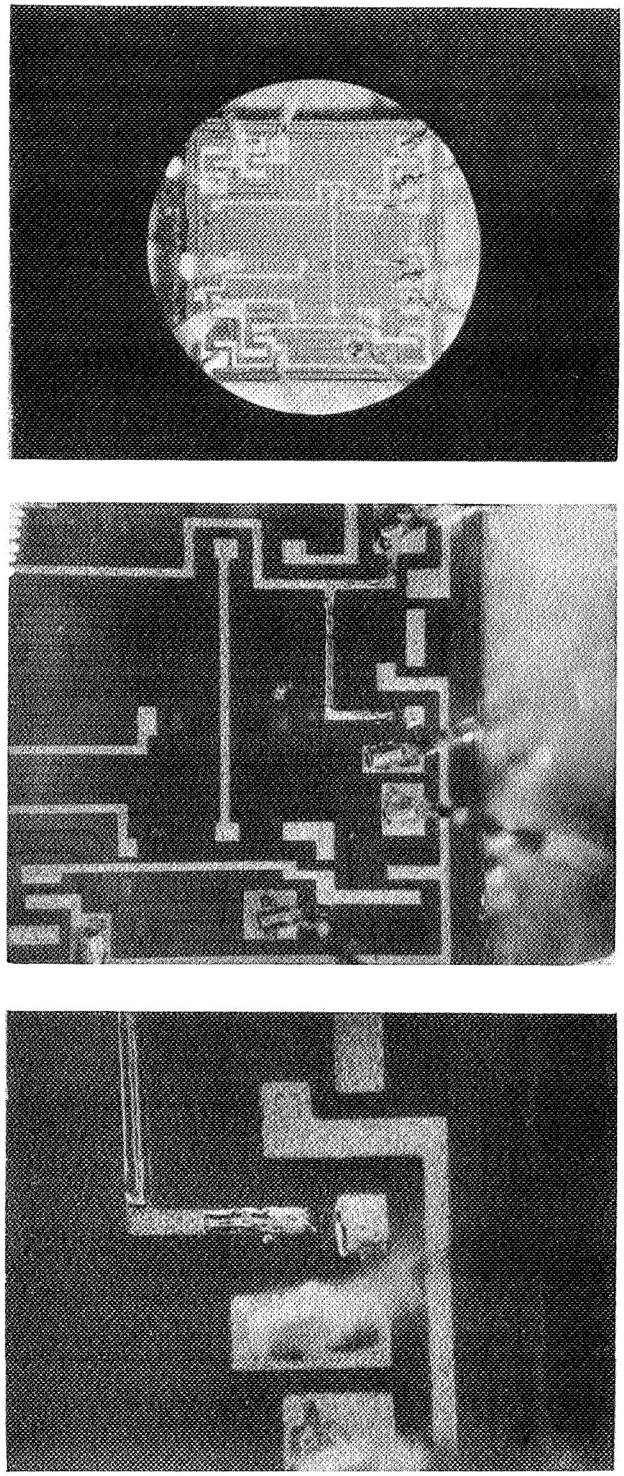
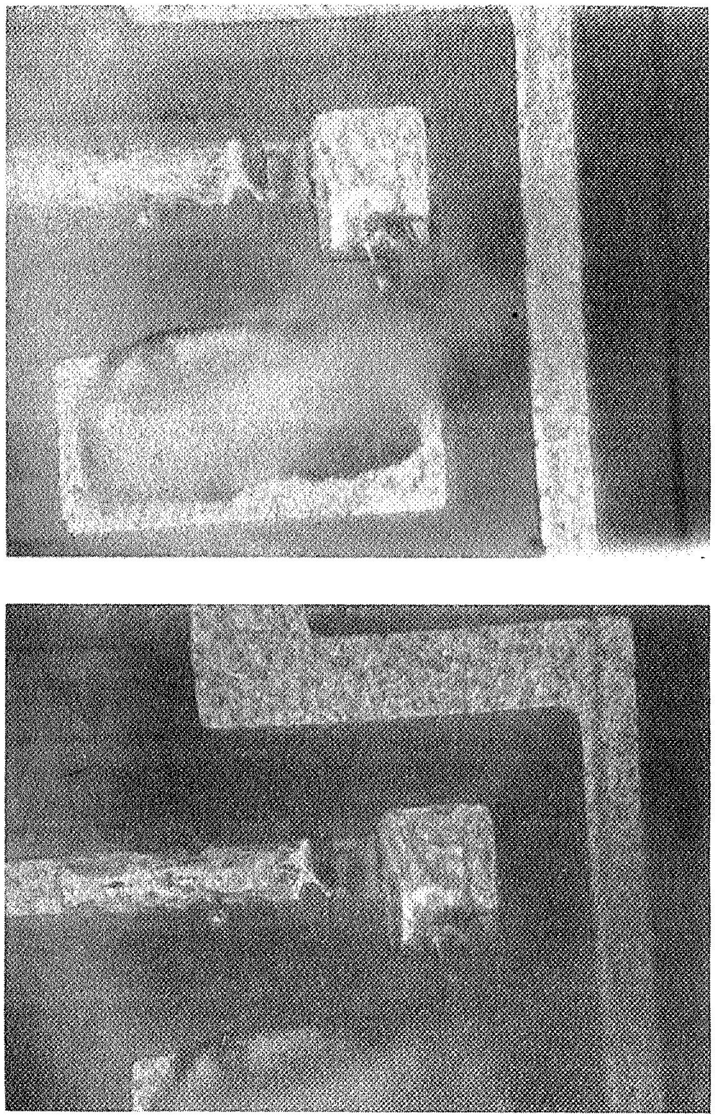
PIN	V1102 (Defective)	V1102 (Good)
1	+29Vdc	+29Vdc
2	+26Vdc	+24Vdc
7		
8	- 9.0 V	- 8.5V
9	0 Vdc	0Vdc
10	10V rms	10V rms
11		
12		

TABLE 1



HEAVY CURRENT AREA AND SHORTING CONDITION

FIGURE 2



SHORT BETWEEN B+ PAD AND N TYPE TUB

FIGURE 3

To: Engineering File - MT-8254 Issue: Original
From: B. Friedman Date: January 11, 1968

INTEGRATED CIRCUIT PWM
TEST RESULTS IN CONJUNCTION
WITH NAS 8-11916

Prepared by: B. Friedman
B. Friedman

THE BENDIX CORPORATION
NAVIGATION AND CONTROL DIVISION
TETERBORO, NEW JERSEY

ABSTRACT

This report describes the test results obtained on a Integrated Circuit Pulse Width Modulator being evaluated under NAS 8-11916. Included is data obtained for both room temperature and 70°C.

1.0 SCOPE

The testing described herein was undertaken in order to determine the performance of an Integrated Circuit PWM and to ascertain its ability to perform satisfactorily its intended servo loop function.

2.0 TEST CIRCUIT

All testing was performed on the circuit configuration shown in Figure 1. A unit was fabricated to the assembly drawing shown in Figure 2. All data was taken with a 28 Ω 54 mh torquer load.

3.0 CIRCUIT PERFORMANCE

The integrated circuit PWM operated adequately as shown by the data presented in this report. However, there are certain restrictions on circuit performance which may not be apparent in the data. When the circuit is used for low gain apllications, ie, the SAT capacitor is equal to .056µf with a 28 ohm load resulting in a gain of approximately 3.3, the triangle wave is not linear and there results a gain change when approaching saturation. This gain change is due to the non-linear widening of the triangle wave near its midpoint.

The higher the gain of the PWM, the less evident this problem becomes. This problem could possibly be eleviated by a modified triangular wave generator.

4.0 TEST RESULTS

4.1 GAIN

The amount of gain was determined for two C_g values. For a capacitor value of .056 µf the gain was found to be approximately 3.3 A/V, however, the non-linearity of the triangle wave was found to be very great at this setting. With the gain capacitor value of .12µf the gain was 10 A/V and the triangular wave became more linear.

$C_g = .056\mu f$

$E_{1N_1} = \underline{40mv} \quad I_{OUT_1} = \underline{118ma}$

$E_{1N_2} = \underline{80mv} \quad I_{OUT_2} = \underline{250ma}$

$$G = \frac{I_{OUT_2} - I_{OUT_1}}{E_{1N_2} - E_{1N_1}} = \frac{132}{40} = 3.3 \text{ A/V}$$

$C_g = .12\mu f$

E_{1N_1} = <u>30mv</u> I_{OUT_1} = <u>300</u>

E_{1N_2} = <u>50mv</u> I_{OUT_2} = <u>495</u>

$$G = \frac{I_{OUT_2} - I_{OUT_1}}{E_{1N_2} - E_{1N_1}} = \frac{195}{20} = 10 \text{ A/V}$$

4.2 NULL

With the input shorted a reading of .06 ma was recorded for the load current at 25°C. With the temperature elevated to 70°C the null remained the same.

(E_{1N} = 0)

I_L 25°C	I_L 70°C
.06 ma	.06 ma

4.3 QUIESCENT CURRENT

Quiescent current values for two temperatures are presented below.

(E_{1N} = 0)

Bias Supply	I_O 25°C	I_O 70°C
+28 VDC	19 ma	20 ma
-15 VDC	2.9 ma	3 ma

4.4 DEADZONE AND LINEARITY

This test was performed using a 28 ohm 54 mh torquer load. Test data is presented in Table 1 and results are shown graphically in Figures 1 and 2.

From these figures it should be noted that even though there was not apparent change in null, there was a marked increase in deadzone characteristics accompanied by an offset to the positive side.

4.5 GAIN VS. POWER SUPPLY VARIATION

The data for this test is presented in Table 2. A graphic representation of this table for the 25^{o}C test is shown in Figure 3.

5.0 CONCLUSION

From the test results presented in this report, it can be concluded that this circuit will adequately perform its intended loop requirements. It is recommended that the linearity of the triangle wave generator be further investigated, for this determines the circuit linearity.

During test of this PWM, two of the custom microelectronic devices were found to be defective. MT-8253 presents an investigation of the defective V1102 chip, and a later report will describe the V1101 chip.

DEADZONE & LINEARITY
$C_q = .12 \mu f$ 28Ω 54 mh TORQUER

	25°C		70°C	
E_{IN} mv	I_{OUT} + ma	I_{OUT} - ma	I_{OUT} +	I_{OUT} -
0	.06	.06	.06	.06
1	20	5	.06	.06
2	43	29	.06	.06
3	53	35	.06	37
4	63	45	.06	47
5	71	54	.06	55
6	81	75	.5	65
7	89	92	2.1	75
8	98	105	13	89
9	106	117	37	110
10	114	129	55	126
12	133	148	77	151
15	160	175	105	186
20	206	231	156	241
25	253	283	206	295
30	300	330	258	345
35	345	385	310	410
40	395	420	360	470
45	445	495	410	525
50	495	550	460	590
55	545	610	520	655
60	600	670	580	720
65	655	730	640	785
70	715	790	700	840
75	770	840	760	900
80	835	870	830	900
90	900	900	900	900

TABLE 1

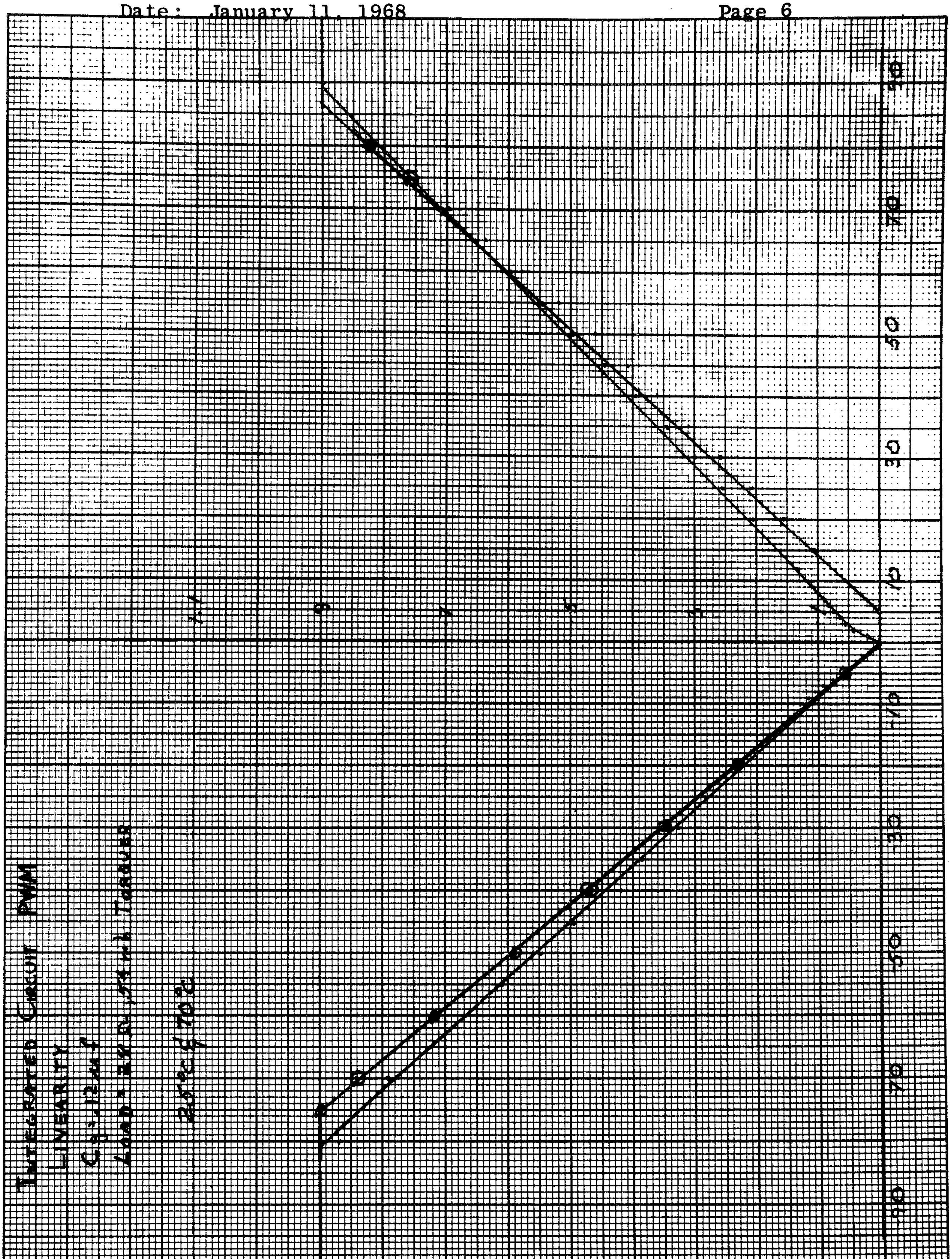

INTEGRATED CIRCUIT PWM
LINEARITY
Cg=.12µf
LOAD = 2K Ω, 54 mh TORQUER
25°C & 70°C
1.1
.9
.7
.5
.3
.1
90
70
50
30
10
10
30
50
70
90

fig. 3

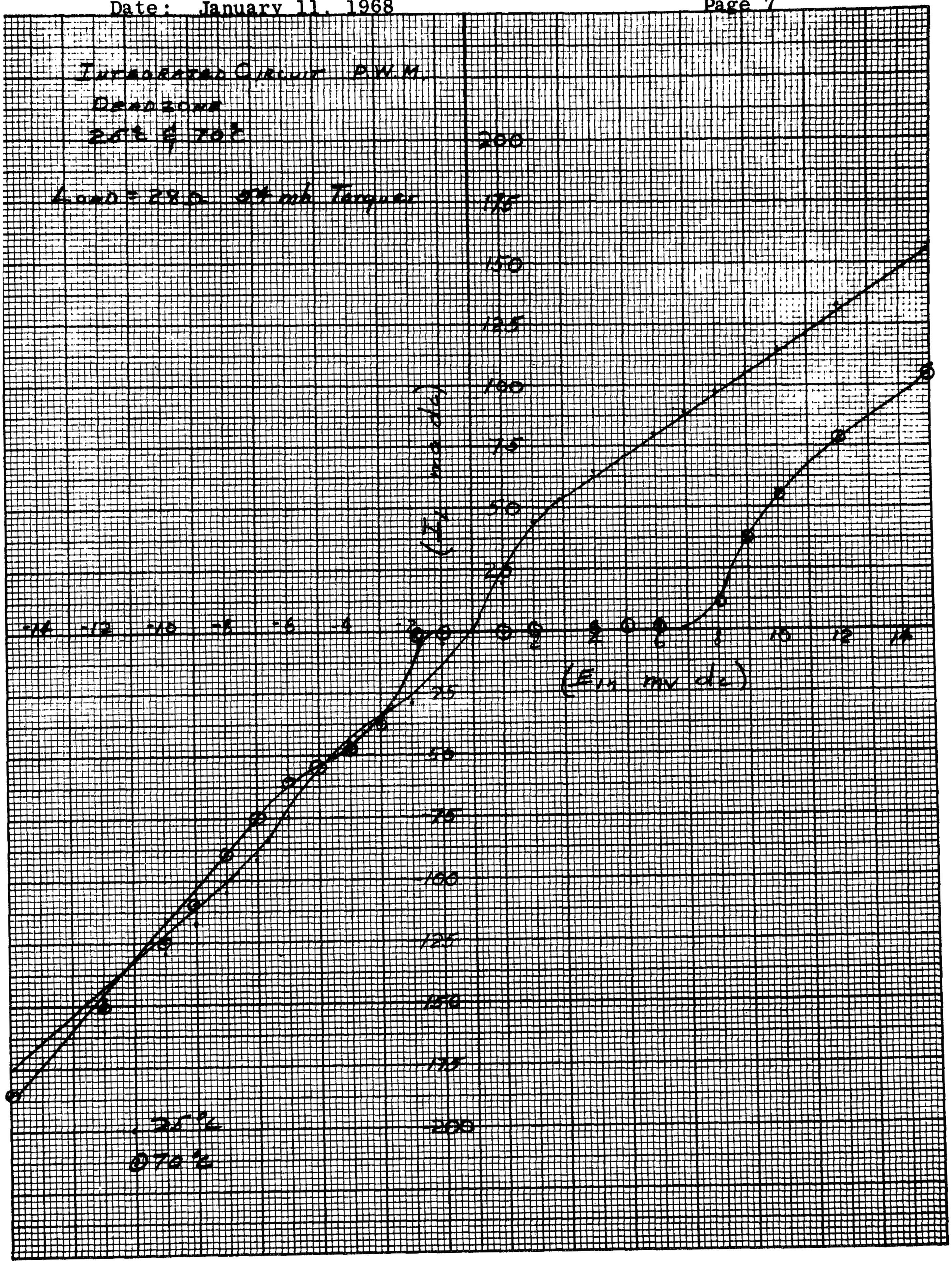

Integrated Circuit P.W.M.
Deadzone
25°C & 70°C
Load = 28 Ω 54 mh Torquer
(IL ma dc)
(Ein mv dc)
— 25°C
⊙ 70°C

Fig. 4

GAIN VS. POWER SUPPLY VARIATION

		$B^+=24V$	$B^+=28V$	$B^+=32V$
	E_{IN} mV	I_{OUT} ma	I_{OUT} ma	I_{OUT} ma
25°C	0	.26	.06	.30
	5	18	71	68
	10	70	114	110
	20	165	206	205
	40	350	395	390
	50	450	495	490
	60	550	600	590
	90	760	900	940
	-5	-36	-54	-84
	-10	-102	-129	-155
	-20	-200	-231	-265
	-40	-405	-420	-480
	-50	-515	-550	-590
	-60	-635	-670	-710
	-90	-760	-900	940
70°C	0	.10	.06	.01
	5	.10	.06	.06
	10	27	55	63
	20	133	156	165
	30	235	258	260
	50	440	460	470
	90	775	900	1.05A
	-5	-32	-55	-74
	-10	-100	-126	-150
	-20	-215	-241	-270
	-30	-320	-345	-380
	-50	-565	-590	-618
	-90	-770	-900	-1.05A

TABLE 2

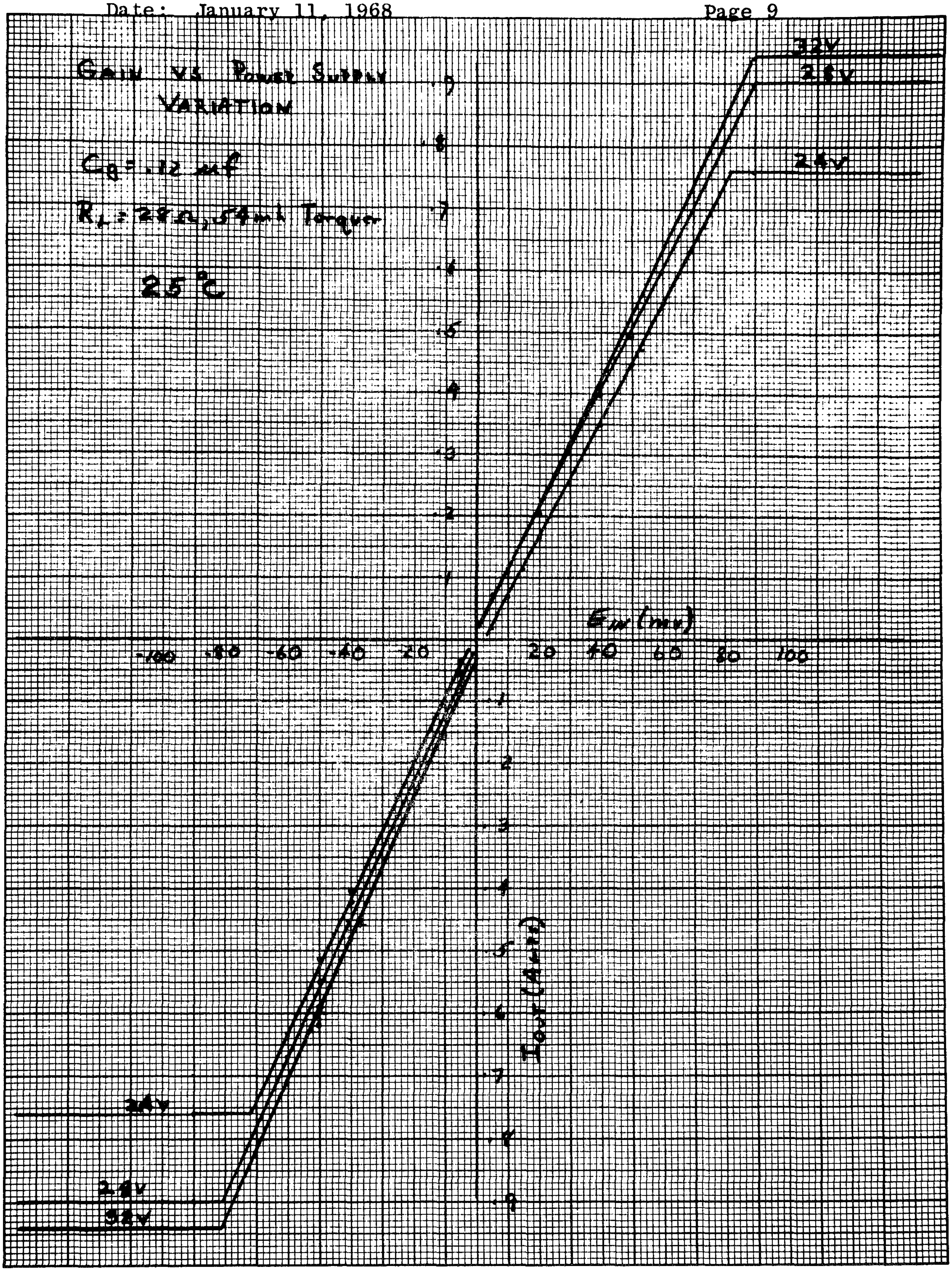
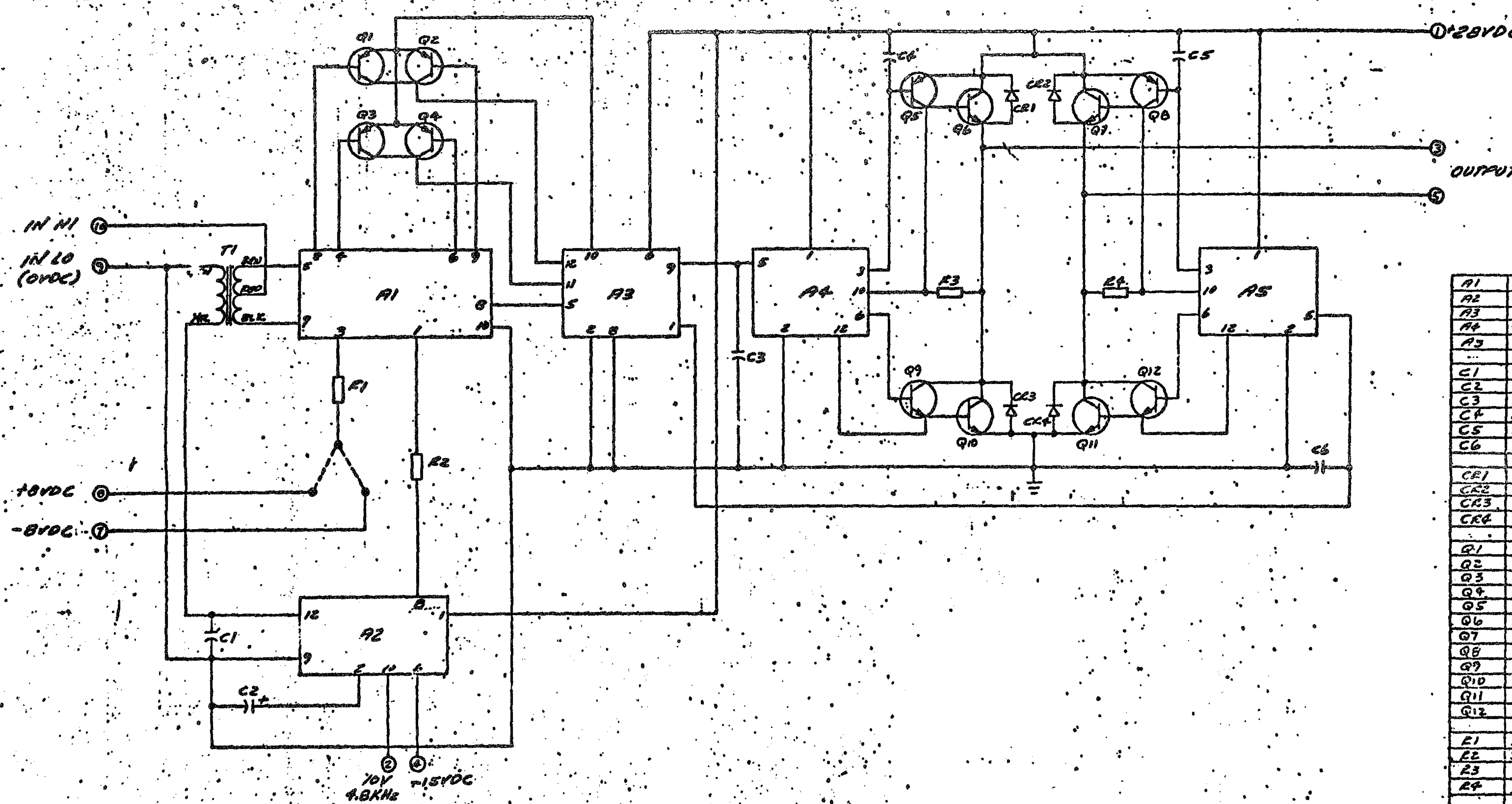

GAIN VS POWER SUPPLY VARIATION
C_Q = .12 μf
R_L = 28Ω, 54 mh Torquer
25°C
32V
28V
24V
E_{IN} (mv)
I_{OUT} (Amps)
-100
-80
-60
-40
-20
20
40
60
80
100

fig. 5

PART NO.

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPROVED



A1		V11101
A2		V11102
A3		V11103
A4		V11104
A5		V11104
C1	.1UF ±10% 50V	VK30BK104K
C2	1UF ±10% 35V	CS13BF105K
C3	.001UF ±10% 200V	CK05CW102K
C4	.015UF ±10% 50V	VK30BX153K
C5	.015UF ±10% 50V	VK30BX153K
C6	.001UF ±10% 200V	CK05CW102K
CR1	UTX210	
CR2	UTX210	
CR3	UTX210	
CR4	UTX210	
Q1	2N722	
Q2	2N722	
Q3	2N722	
Q4	2N722	
Q5	2N2907	
Q6	2N4150 (H.S.)	
Q7	2N4150 (H.S.)	
Q8	2N2907	
Q9	2N2316	
Q10	2N4150 (H.S.)	
Q11	2N4150 (H.S.)	
Q12	2N2316	
R1	S.A.T. 100K ohm ±5% 1/8W	RC05GF104J
R2	S.A.T. 1K ohm ±5% 1/8W	RC05GF102J
R3	680 ±5% 1/8W	RC05GF681J
R4	680 ±5% 1/8W	RC05GF681J
T1	DIT 20 (UTC)	

☐ DO NOT MARK PART NO.
☐ MARK PART NO. AS SPECIFIED

⊕ = INDICATES SUBASSEMBLY
⊕ = VENDOR ITEM – SEE SOURCE CONTROL OR SPECIFICATION CONTROL DRAWING

– LIMITS OF ACCEPTABLE WORKMANSHIP ARE DEFINED IN ECLIPSE-PIONEER STANDARDS DS-103.

UNLESS OTHERWISE SPECIFIED
– DIMENSIONS ARE IN INCHES
– TOLERANCES ON DECIMALS
2 PLACE ±.03 3 PLACE ±.010 4 PLACE ±.0005

HARDNESS

MATERIAL

FINISH

PART REF

ORIGINALLY DESIGNED FOR

DR W.D. 7-11-67
CH.
T.O.
MET.

CONTRACT NO.

APPROVAL

APPROVAL

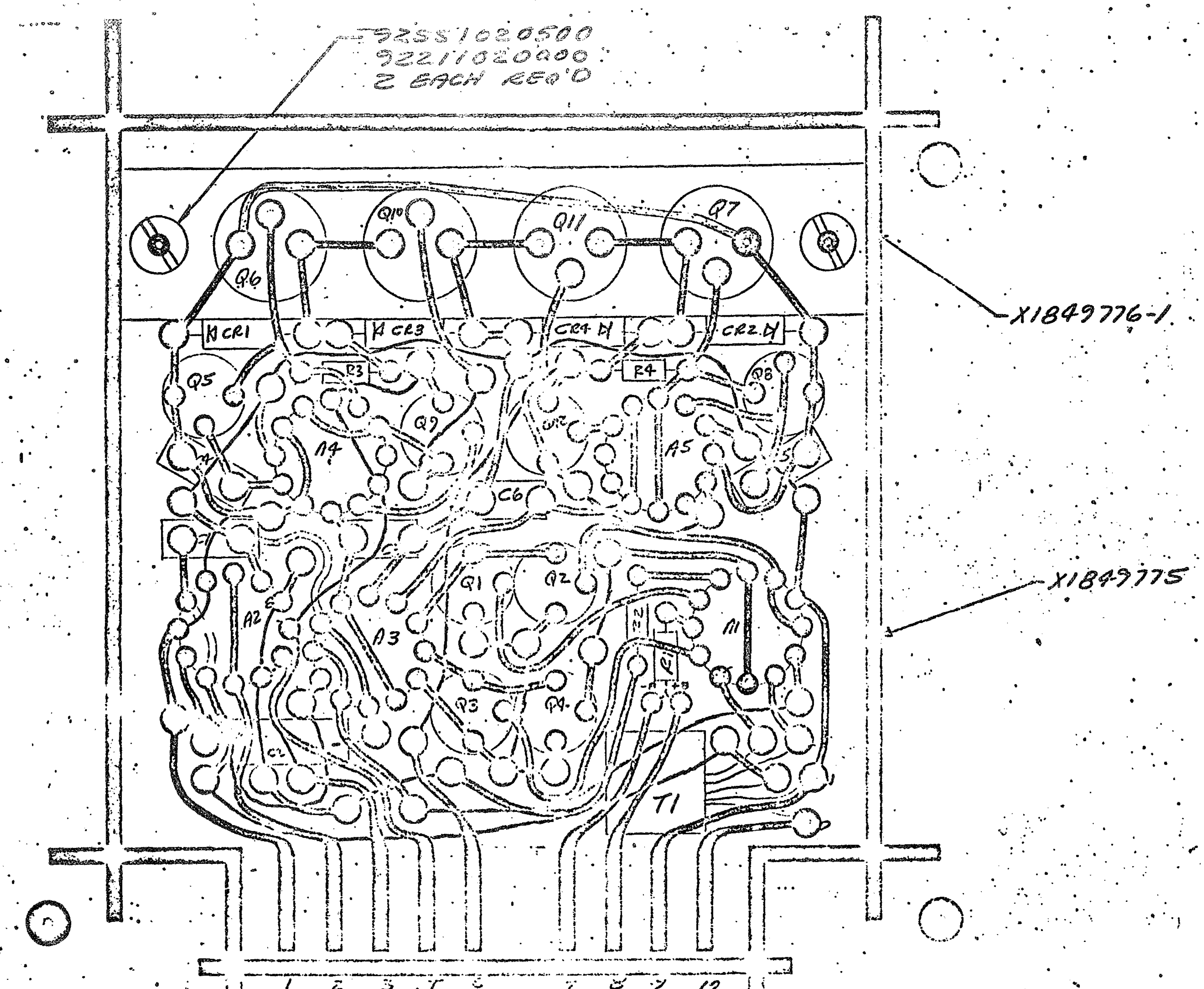
THE Bendix CORPORATION ECLIPSE-PIONEER DIVISION TETERBORO, NEW JERSEY, U.S.A.

SCHEMATIC
INTEGRATED POWER AMPLIFIER

SIZE D CODE IDENT NO. 19315 X1849773

SCALE WT SHEET

FIG. 1



+ = INDICATES SUBASSEMBLY ‡ = VENDOR ITEM - SEE SOURCE CONTROL OR SPECIFICATION CONTROL DRAWING	— LIMITS OF ACCEPTABLE WORKMANSHIP SPECIFIED IN ECLIPSE-PIONEER STANDARDS 05-103	UNLESS OTHERWISE SPECIFIED — DIMENSIONS ARE IN INCHES — TOLERANCES ON DECIMALS 2 PLACE ± .03 3 PLACE ± .005 4 PLACE ± .0005	DR W. D. 7-14-67 CHK T. D. MET.	THE Bendix CORPORATION ECLIPSE-PIONEER DIVISION TETERBORO, NEW JERSEY, U.S.A.
HARDNESS		MATERIAL		ASSEMBLY PRINTED CIRCUIT BOARD
FINISH			CONTRACT NO.	
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FIG. 2

To: Engineering File - MT-8255 Issue: Original
From: B. Friedman Date: January 19, 1968

INVESTIGATION OF ADDITIONAL MICROCIRCUIT FAILURES IN CONJUNCTION WITH NAS 8-11916

Prepared by: B. Friedman
B. Friedman

THE BENDIX CORPORATION
NAVIGATION AND CONTROL DIVISION
TETERBORO, NEW JERSEY

ABSTRACT

Contained in this report is a description of two improperly functioning microcircuits being evaluated as part of NAS 8-11916. Also contained are failure analysis performed on these devices which tend to establish that both microcircuits were defective due to manufacture and vendor inspection shortcomings.

1.0 INTRODUCTION

The purpose of this report is to ascertain the probable cause of failure of two custom microelectronic devices being evaluated for application under NAS 8-11916. The two microcircuits concerned are 1) V1101 (used in the mixing stage of the integrated circuit P.W.M.) and 2) V1102 (the triangle wave generator also used in the P.W.M.).

2.0 CONCLUSIONS AND RECOMMENDATIONS

From the evidence presented in this report it can be concluded that both devices were defective when shipped by the manufacturer. The malfunction of the V1101 was due to improper handling of the chip during manufacture evidenced by the scratched metalization. The V1102 failure can be attributed to improper process control by the manufacturer resulting in subsequent breakdown and leakage. Although both of these failures and the failure reported in MT-8253 were manufacturing problems, it should be noted that the manufacturer has stated that any of these devices "previously shipped or presently in stock were manufactured as prototypes under engineering laboratory conditions and with no intent to impose process, inspection or normal manufacturing controls. Secondly, these devices have not been subjected to simulated parameter testing that would be experienced in the using system. --- the probability for this happening again is relatively high since these are partially tested prototypes."

3.0 V1101 FAILURE

During a check of the resistor values on V1101 S/N 23 it was found that measurements between pins 7 and 1 did not exhibit a diode characteristic when pin 1 was at a higher potential than pin 7. These measurements indicated a base to emitter short. Further testing of the chip tended to strengthen the probability that a base to emitter short was in existence. After opening the case the chip surface was examined under a high power microscope. It was seen that the entire surface of the device had been scratched and the base emitter junction in question was physically shorted by scratched metallization. Photomicrographs showing these conditions are presented in Figure 2.

4.0 V1102 FAILURE

The microelectronic V1102 device passed all d.c. resistance tests, however, when the unit was placed in the circuit operating malfunctions were experienced. Table 1 presents a pin for pin comparison of the voltage waveshapes experienced on the defective S/N 35 chip and a properly operating device S/N 38. From this data it can be seen that a d.c. level exists at pin 11, also apparent is the distortion in the triangle wave at pin 11. Figure 3 shows the circuit used to obtain this data. Opening the microcircuit package and inspecting the device under high magnification revealed no evidence of surface irregularities. However, it was found that a decrease in the B+ voltage below 18.5 volts removed the d.c. level on pin 11. This fact indicated a breakdown was occuring in the device. By inserting the device in a curve tracer with pin 1 connected to the collector terminal and pin 11 connected to the emitter connection the voltage versus current characteristic presented in Figure 4 was obtained. From this figure it can be seen that a breakdown does occur at approximately 18.5 volts. Even though it is impossible to prove where this breakdown is occuring exactly, from the data it is reasonable to assume a diode breakdown between the N tub and the resistor region associated with the 6K on pin 11.

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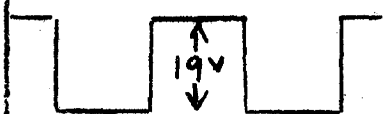
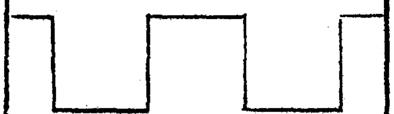
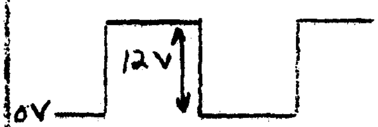
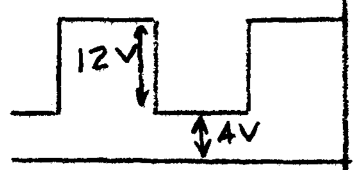
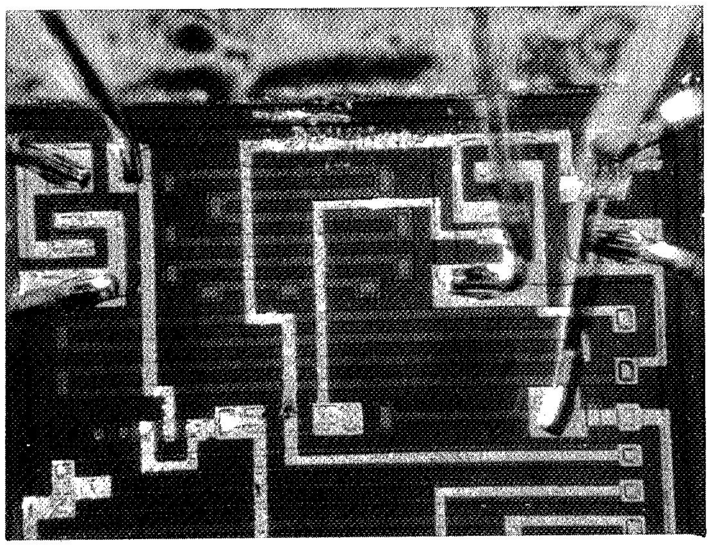
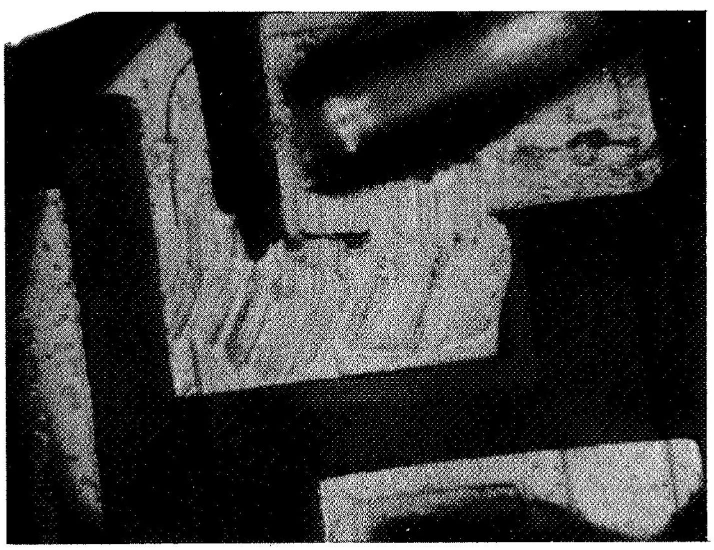
PIN	V1102 S/N 38	V1102 S/N 35
1	+28 Vdc	+28 Vdc
2	+24 Vdc	+24 Vdc
7	 19V	
8	-8 Vdc	-8 Vdc
9	0	0
10	10 V rms 4.8 Kc	10 V rms 4.8 Kc
11	 12V 0V	 12V 4V
12	 1V 40 mv offset	 400 mv 90 mv offset

TABLE I





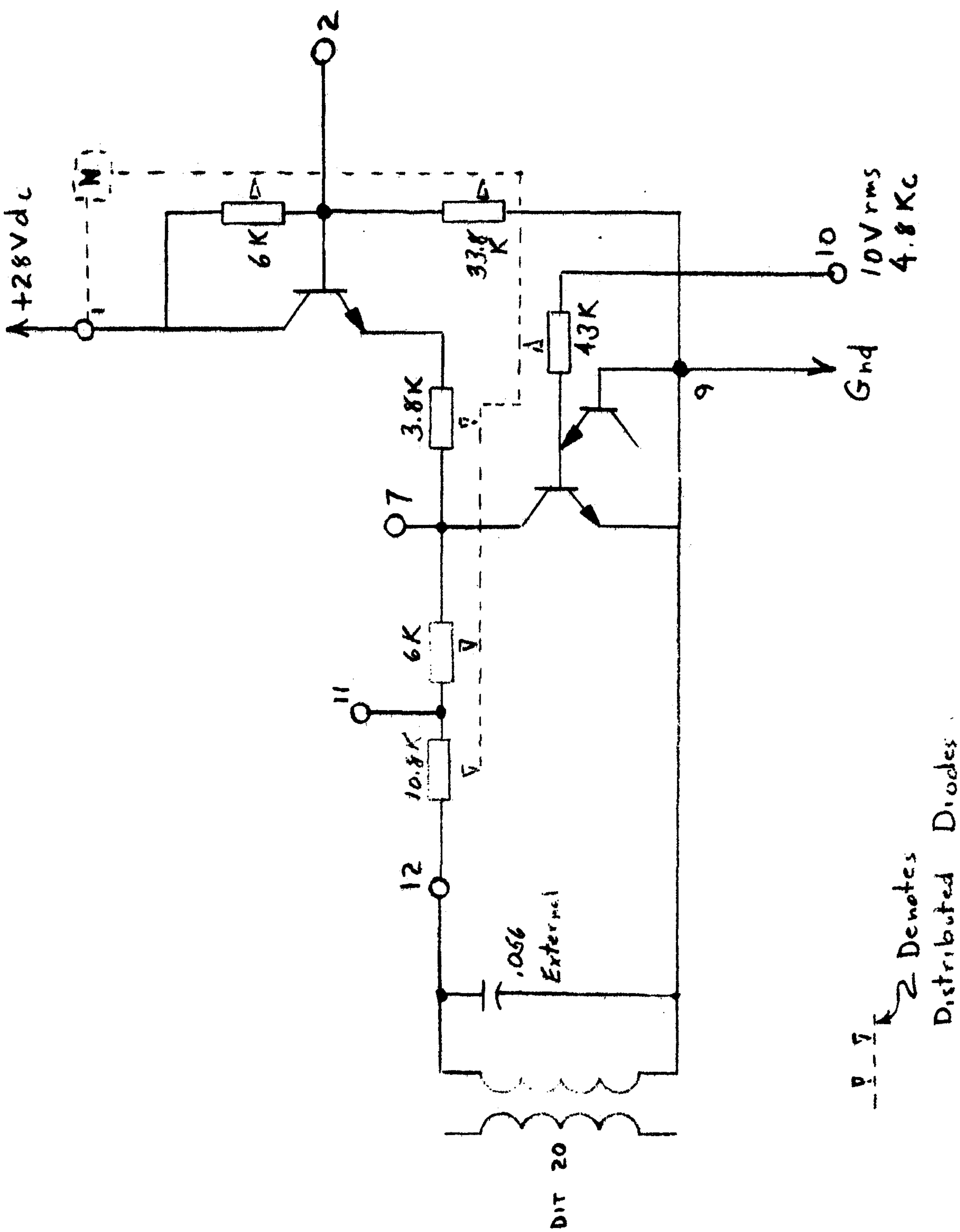

2
+28Vdc
1
6K
33.8K
10
10Vrms
4.8Kc
43K
Gnd
9
3.8K
7
6K
11
10.8K
12
.056
External
DIT 20
Denotes
Distributed Diodes

fig 3