Ref: 300-62

QUARTERLY PROGRESS REPORT
DIGITAL DATA SAMPLING MODULES

Contract No. NAS8-30003

Period of Performance
April 1 through June 30, 1969

Submitted to:

NASA
George C. Marshall Space Flight Center
Huntsville, Alabama

General Instrument Corporation
Microelectronic Division
Advanced Development Center
17 East Oakland Avenue
Salt Lake City, Utah 84115

INTRODUCTION

This is the fourth quarterly progress report to be submitted on Contract No. NAS8-30003 for the design, development, and fabrication of microminiature Digital Data Sampling Modules. The report covers the period from April 1 through June 30, 1969 and includes work performed during the last two months of the final design phase (Phase II) and the first month of the Fabrication Phase (Phase III) of the three phase program.

A Phase II Final Design Review was held with NASA at the Huntsville facility on June 5th and 6th and as a result a modification was suggested in the program to allow additional time to develop the low level amplifier portion of the system since this was the only portion of the system not completed and ready for final design review. As a result of the amplifier problem, General Instrument was asked to present a plan which would allow for the additional time for amplifier development while remaining within the presently allotted program funding. The following was proposed by General Instrument:

General Instrument will fabricate test and deliver fifty (50) high level modules rather than the 128 modules originally contracted. The funds which will be saved from this reduction will be used to facilitate the design and fabrication on two types of low level modules (two different amplifier types) and deliver the following types and quantities of low level modules by March 30, 1970.

Five (5) CIAM (μA 735 or equivalent) 30 mv full scale

Five (5) CIAM (μA 735 or equivalent) 50 mv full scale

Five (5) CMIA (RA-909 amplifier) 30 mv full scale

Five (5) CMIA (RA-909 amplifier) 50 mv full scale

In addition, General Instrument proposed to deliver one system controller, one set of cables, and one PDP-8 computer within the presently available program funds.

To date there has been no information received from NASA as to the acceptance or rejection of the above proposal and, therefore, General Instrument is proceeding under the assumption that the program will proceed as proposed. A schedule for the revised program as outlined above is shown in Figure 1.

A request for permission to purchase and deliver a PDP-8 computer as part of the program was submitted immediately following design review. No word on this request has been received to date. Since a purchase order cannot be placed until approval is received and since the delivery of a computer after placement of the purchase order is three to four months, it is imperative that permission be received very soon if the computer is to be of value during the testing phase of the program. During the past quarter, the final design of all other portions of the system has been completed and each of the various subsystems has been fabricated in integrated circuit form.

The subcontracts for the development of both a hybrid and integrated circuit voltage comparator has been completed and the subcontract for a hybrid voltage reference supply was completed.

A complete high level data module has been fabricated on two printed circuit boards as shown in Figures 2 and 3 and is operating with good results.

The mechanical design of the high level data module has been completed including the layout and photography of the individual ceramic substrates and printed circuit boards.

Meetings were held with three hybrid circuit manufacturers to discuss the manufacture of the low level amplifiers. A bid package for the fabrication and testing of the amplifier was completed by Analog Integrated Microsystem, (The amplifier design subcontractor) and has been mailed to the hybrid manufacturers for bid. The availability of a new amplifier developed by Raytheon has been investigated for use in the CIAM approach. Information received to date indicates that it should be available during the month of July.

A brief summary of the work completed during the past month is given below. This is followed by a detailed discussion of some of the various subsystems.

1. Completed final design review.
2. Completed development of the timing register.
3. Completed redesign of complementary circuits.
4. Completed redesign of multiplexer for differential operation.
5. Completed detailed tape-ups and photography on ceramics and printed circuit boards.
6. Completed fabrication of high level module on PC boards.
7. Continued testing and evaluation of subsystems and module.
8. Placed purchase orders for parts for prototype assembly.

INPUT CIRCUIT (COMPLEMENTARY)

The first complementary input circuit chip which was designed had a substrate back-bias problem and a power latch-up problem. It was found that these problems could be taken care of by the addition of two external resistors. This particular circuit with the two resistors is currently being used in the module with very good results; however, a redesign was initiated to overcome the requirement of both of these problems and eliminate the external resistors. The first wafers from this redesign have just been completed and one currently being tested. Initial test results indicate problem has been solved, however, until the circuit has been packaged and fully tested this cannot be positively known. It is felt at present that this problem will be solved prior to the requirement for chips for the prototype and as a backup, the first design is satisfactory with the addition of the external resistors. Complete information on the new design will be available by the end of the first week of July.

TIMING REGISTER

Fabrication and testing of the timing register subsystem was completed during the past month with satisfactory results. This circuit performs all functions as designed except that a single power supply provides more reliable operation than when using ground as one of the supplies. This has the effect of increasing the power dissipation of the timing register by approximately 10 mw but provides operation over a large variation in

either clock amplitude or supply voltage. Rather than redesign the register to provide the operation at the slight power reduction it appears desirable to use the circuit as is. The timing register operates very well in this mode and functions well in the module to frequencies of about 700 KHz. This chip now replaces the four 9 bit shift register chips which were originally used for the timing register.

OVERVOLTAGE PROTECTION CIRCUIT

The masks have been completed and the first wafers fabricated for this circuit. A separate chip is now used for the resistors and the zener diodes. The first wafers for the resistor chip resulted in lower than desired breakdown voltage (40-50 rather than 60-70), therefore, a slight modification in the diffusion process is now being implemented. The wafers for the zener diodes are now in process and will be evaluated during the following month. It is anticipated that all problems concerning this circuit will be solved and the chips ready for prototype fabrication during August.

OUTPUT DRIVER (COMPLEMENTARY)

The output driver circuit initial design had the same latch up problem as the input chip but again will operate satisfactorily with the addition of two external resistors and is presently operating in this manner in

the data module tests. A redesign to eliminate these external resistors was also completed and mask photography is currently underway. As with the input chip, this modification is expected to solve the latch-up problem and the chip is expected to be available in final form for prototype fabrication in August. The initial design with the external resistors is a back-up for the new design approach. Operation of the chip with the two external resistors is entirely satisfactory in the module operation.

MULTIPLEXER

The multiplexer chip for the high level module is completed and operating satisfactorily. The requirement for a low level differential multiplexer for the CMIA low level module resulted in a redesign of the metal mask of the high level multiplexer, however, in order to provide the differential switch capability. This redesign has been completed and the mask cutting and photography is currently underway. The new mask set for the low level mux will be identical to the high level mux except the change in the metal mask and the increased cnip size required to provide the additional pads for the differential switches.

As a preliminary to the low level mux design, the "on" resistance of the two switch pairs on the present high level mux was measured. The switch "on" resistance of the two differential switches match to within approximately 30 ohms over the expected input range.

The calibration multiplexer for the CIAM low level module was fabricated and tested during the past month. Although the yield on the circuit for

the first set of wafers was very poor, good chips were found at the wafer probe test which verifies the correctness of the circuit design and mask set. Further testing on this chip will be performed as soon as packages with sufficient pins are available (46 pins). These have been ordered from our New York facility. In addition, another lot of wafers are being fabricated for further testing and yield evaluation. These wafers will be available in early July.

A/D CONVERTER

The operational performance of the A/D converter breadboard is compatible with the requirements of the Digital Data Sampling System over the specified temperature range of -20°C to +85°C. The conversion accuracy of the A/D converter will be degraded when utilized in the low level application, however, due to the error contribution of the signal conditioning amplifiers.

The present A/D logic chip configuration is acceptable for both the high level (8-bit) and low level (9-bit) systems. A minor mask modification has been initiated to increase device yield by more nearly matching the ladder switch "on" resistance to the compensated ladder elements.

Previous testing of the bipolar comparators has shown this chip to be acceptable in the packaged (TO-5) condition. Additional comparator tests are presently being conducted to determine the amount of degradation--if any--in performance due to temperature levels required to attach the chip to the ceramic substrate.

Compensated ladder networks in chip form have been obtained from Solid State Scientific. A small number of networks are also being procured from Halex and Hybridyne for further evaluation. At present, the Solid State Scientific network has been selected for this application, primarily due to its small size.

Ceramic substrates should be available by mid-July. A prototype A/D converter will be fabricated at that time to evaluate the assembly technique and post-assembly performance of the converter.

LOW LEVEL AMPLIFIER

CIAM Approach

A visit was made to Beckman Instruments - Microcircuit Operations located in Buena Park, California, Aerojet General Microelectronic Department located in Azusa, California, and Halex Incorporated, located in Torrence, California on June 12 and 13. Mr. Marv Rudin was in attendance at Aerojet and Beckman.

The CIAM Hybrid Amplifier approach was discussed with each company and the information contained in the Status Report presented at the NASA Design Review meeting in June was conveyed to the vendors. Since the schematic in the status report did not contain provisions for initial offset adjustment, pin designations for the Raytheon RM 4132 amplifier, and the ceramic form factor, Mr. M. Rudin was to prepare a bid package with the updated information. Ceramic dimensions were specified at the above mentioned meetings. Also, suggested test specifications were to

be included in the bid package along with a suggested resistor adjustment procedure. The appendix contains the information mailed to the potential vendors on June 26. However, since General Instrument did not receive the information until June 30th, comments are not contained in this report.

In general, each vendor seemed to be aware of the magnitude of the low level amplifier assembly. Following is a brief table of technology and comments.

Manufacturer	Technology	Ohms/Square Max.	Remarks
Beckman	Thick film	400 K/Sq.	Can adjust with sand abraison and can meet specified tolerances.
Aerojet General	Thin film Mask-deposition	10K/Sq.	Can meet specified resistor range and tolerance.
Halex	Thin film	3K/A	Must use thick film chip resistors for the two 50 meg ohm resistors. All other specifications can be realized.

Of course, construction of the amplifiers depends on μA735 or RM 4132 availability. Latest dates are μA 735 - August, RM 4132 - by the end of the first week in July.

An order was placed for RM 4132 samples with Raytheon on the 9th of June with delivery promised on July 14th.

CMIA Approach

Five RA909A devices were purchased from Radiation Incorporated and a breadboard was constructed. Appendix y contains some results of the measured parameters.

In general, the CMIA configuration will apparently handle the low level multiplexer switching transients as simulated in the test set. However, no exact settling time was measured. One problem area became evident immediately - that of a limited output voltage swing within 2 volts of the supply voltages. This in effect limits the allowable common mode voltages at the input with ±7.5 volt supplies to -4.2 and +4.5 volts in the presence of a 30 millivolt differential input signal. Also, the measured common mode rejection was quite low, however, this is due in part to the resistor mismatch and would be improved with the specified resistor tolerances as noted in June Design Review Status Report.

REFERENCE SUPPLY

The appendix contains the temperature performance results of the reference supply prototypes assembled by Hallex. Also, a thin film layout of the reference supply is presented along with the specification and temperature data of a breadboard version.

The results indicate that the zener voltage does not remain within its specified 0.001%/^{o}C temperature coefficient particularly for hot temperatures greater than ≈ +50^{o}C. The results of the breadboard version indicated that this could happen, however, it was felt that the actual

thin film resistor network in conjunction with the circuit would be necessary to verify the above conclusion. Since the breadboard measured zener current remained essentially constant over the temperature range and that both breadboard version and prototypes exhibit the same results the zener's temperature coefficient is not sufficient to produce the desired 0.1 percent reference supply accuracy.

Therefore, on subsequent units the zener's temperature coefficient will be specified to be 0.0005%/^{o}C.

SYSTEM CONTROLLER

The Command line driver circuitry has been redesigned to generate a faster rise and fall time signal and a larger amplitude signal. The redesigned circuit drives the line with a much improved signal.

Approximately 80 percent of the logic is checked out. The System Controller has been in use for checking out Data Modules that final checkout of the breadboard System Controller has been slowed up. For this reason a Command line generator is being fabricated to test modules.

The logic design of the PDP-8 interface has not been started since we have not received final approval to purcnase the PDP-8L.

FABRICATE, TEST AND DELIVER 200 DIGITAL DATA SAMPLING MODULES (PHASE III)

DATE	June	July	Aug.	Sept.	Oct.	Nov.	Dec.	Jan.	Feb.	Mar.
Design Review	△									
Design Approval	△									
Complete High Level Module Design	△									
Purchase PDP-8		△								
Complete Breadboard Evaluation		△								
Complete Layouts		△								
Procure Material			△							
Fabricate Ceramics				△						
Fabricate Beam Lead Wafers				△						
Fabricate Ceramics (Prototype)			△							
Fab. Prototype Module (High Level)				△						
Test Prototypes				△						
Fabricate Ceramics (High Level)					△					
Fabricate Modules (High Level) (50)						△				
Test Modules						△				
Fab. & Test System Control #1					△					
Fab. & Test System Control #2						△				
Test System (High Level)						△				
Deliver H.L. Modules							△			
Evaluate L.L. Amp. Bids			△							
Select Design Approach				△						
Complete L.L. Module Design					△					
Procure Amps.						△				
Fab. Prototypes (6) (3 each type)							△			
Test Prototypes								△		
Fabricate Modules (20 modules)									△	

Figure 1.

FABRICATE, TEST AND DELIVER 200 DIGITAL DATA SAMPLING MODULES (PHASE III)

DATE	June	July	Aug.	Sept.	Oct.	Nov.	Dec.	Jan.	Feb.	Mar.				
Test Modules														
Training Program														
Final Report														
Deliver Remaining Portion of System														

Figure 1 (Continued)

APPENDIX

CIAM AMPLIFIER BID PACKAGE

General

This is a set of specifications delineating the essential requirements for a hybrid micropower data amplifier required by General Instruments under a NASA R and D contract. Because this is a general state-of-the-art development program, not intended for a specific flight program, reliability tests are not required.

Circuit Schematic

Two alternate circuits I and II are given. I is for the use of the Fairchild μA735 micropower op amp, and II for the preferred op amp, the RM 4132. They are both given because neither is yet available. The RM 4132 is expected to be ready in small quantities the first week in July and the μA735 will be ready in August.

Component Values

Values and tolerances for the component parts of the CIAM are given in Attachments I and II, for each schematic. Specifications for the op amps are attached on separate sheets labeled RM 4132-AS1 and AS2, and μA735-AS1 and AS2.

Performance Specifications

Attachment III gives the performance specification for the CIAM amplifier, independent of which micropower op amp is employed.

Test Specifications

Attachment IV gives test specifications for the overall CIAM amplifier, and some suggested tests for use on the DA and OA subcircuits comprising the CIAM amplifier.

Resistor Adjustment Procedures

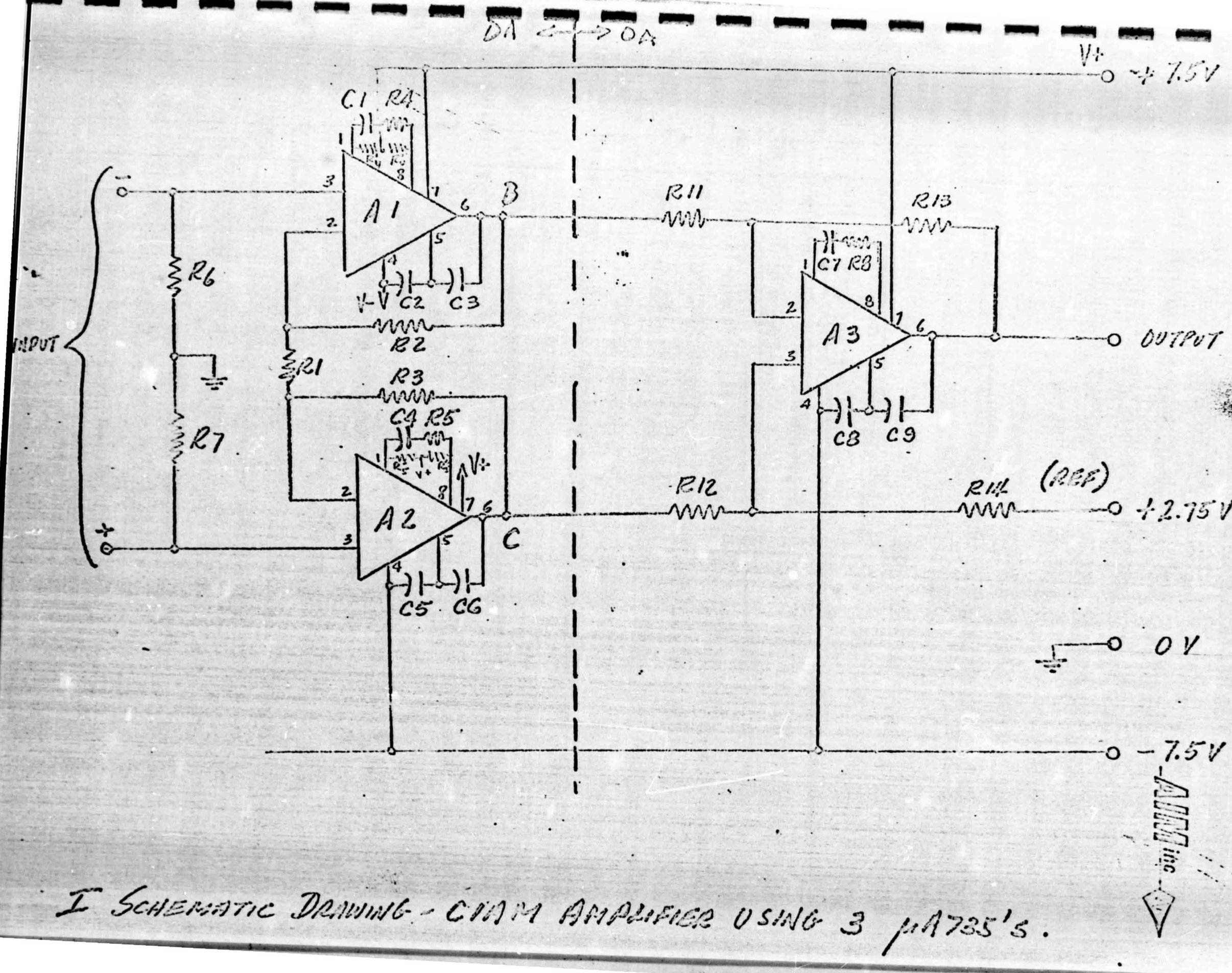
Attachment V gives suggested resistor adjustment procedures in building the CIAM amplifier.

Requirements

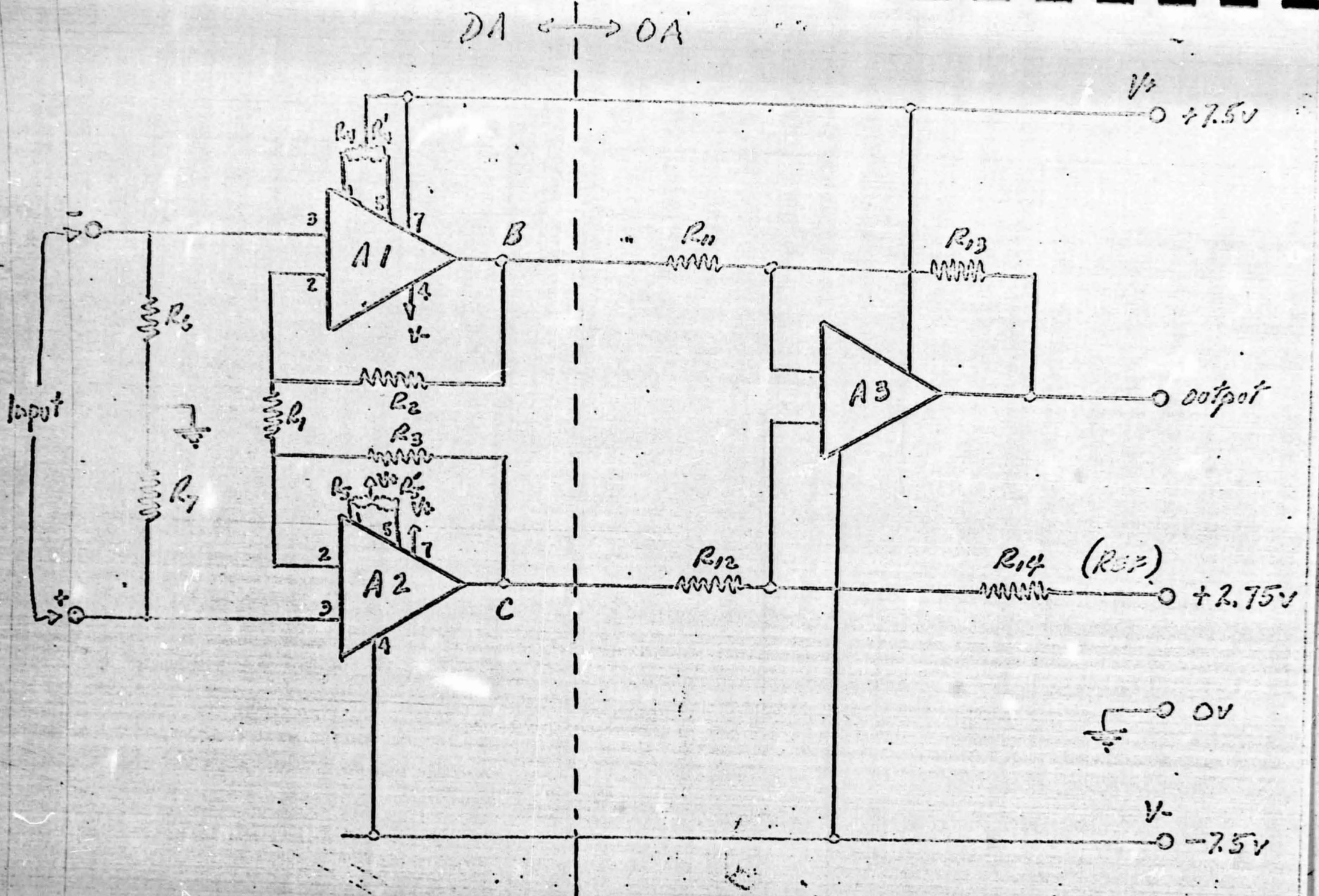
The substrate and terminal numbers to be used will be supplied by R. Nelson of General Instruments, Advanced Microelectronic Center, Salt Lake City, Utah. It is preferred that the op amp chips experience no more than 300°C temperature during hybrid assembly and package sealing, and if the temperature reaches 400°C, that it do so for less than 5 minutes.

Bid Conditions

Business aspects of this bid, such as time to bid, time to deliver, quantities required, etc. will be governed by Mr. R. Nelson or Mr. J. Mathis of General Instrument. It is presently our understanding that bids should be based on quantities of 10 and 500 CIAM amplifiers.



I SCHEMATIC DRAWING - CMM AMPLIFIER USING 3 μA735's.



II Schematic Drawing - Gain Amplifier using 3 RM4132's.

Attachment I

Parts List- Single Amplifier, CIAM System

Operating temperature ragne: -20° to +85°C

A1, A2 μA 735 selected per spec 735-AS1

A3 μA 735 selected per spec 735-AS2

Capacitors*

C1, C4, C7	0.022μF	± 20%	25WVDC
C2, C5, C8	0.0022μF	± 20%	25WVDC
C3, C6, C9	180pF	± 20%	25WVDC

Resistors

R1	2KΩ ± 20%	
R2, R3	15.7KΩ ± 20%, matched to 5%	
(R2 + R3)/R1	15.67 ± 1%	
R4, R5, R8 (comp)	22KΩ ± 10%	$R_4'=R_4''=R_5'=R_5''$= 4 MΩ ± 20% (adjust R_4' and R_5' for zero offset of A1 and A2 respectively)
R6, R7	50MΩ ± 20%, matched to 6%	
R9, R10	not used	
R11, R12	50KΩ ± 20%	
R13, R14	250KΩ ± 20%	
R14/R12, R13/R11	5.00 ± 1%, matched to 0.1%	

*Insulation resistance>100MΩ

735-AS1 AMPLIFIER SPECIFICATION Input Amplifier
3-6-69 4-7-69* GH&W/sow

Absolute Maximum Ratings

Supply Voltage		15	V
Input Voltage	Either Input	V+/V-	V
	Between Inputs	7	V
Internal Power Dissipation		300	mW
Storage Temperature Range		-65 to +150	°C
Operating Temperature Range		-20 to +85	°C

Electrical Characteristics

(At T_A=-20°to+85°C, V_+= +7.5V, V_-= -7.5V, *R_L= 14.8kΩ, unless otherwise specified.)
* +referred to +1.7V, not ground.

		Min	Typ	Max	Units
Open-Loop Response					
*Small Signal	DC Gain	15K	—	—	--
	Unity-Gain Bandwidth				MHz
	Gain at ____ MHz				--
*Large Signal	Full-output dc gain	40K	—	—	--
(Full output = ±5.3 V)	Max. Freq. for full output				MHz
	Max. Slewing Rate				V/μs
Undesired Signal Rejection (r.t.i.)					
	CMRR (CM Input Range=±5.1 V)	—	—	10	μV/V
	Power Supply Rejection (±0.5V)	—	—	25	μV/V
Input Impedance					
Between Inputs	R				MΩ
	Parallel C				pF
Common Mode	R				MΩ
	Parallel C	—	—	2.5	pF
Input Offset Voltage					
Without external trim		—	—	1	mV
Temperature coefficient, average					μV/°C
Drift (per ____)					μV
Input Current					
Either ~~Input~~ Average, both inputs		—	—	20	nA
Offset		—	—	10	nA
Temperature coefficient, ave.	Either Input				nA/°C
	Offset				nA/°C
Drift (per ____)	Either Input				nA
	Offset				nA
Input Noise					
f_o= ____Hz; Δf= ____Hz.	Voltage, rms				nV
	Current, rms				pA
f_o= ____Hz; Δf= ____Hz.	Voltage, rms				nV
	Current, rms				pA
f_o= ____Hz; Δf= ____Hz.	Voltage, rms				nV
	Current, rms				pA
Output					
*Voltage, peak			+5.3 V (sourcing 250μA)		V
*Current, peak			-5.3 V (sinking 475μA)		mA
Impedance, l.f.					Ω
Power Requirements (At rated supply voltage = ±7.5V)					
Power Dissipation, Quiescent		—	1	3	mW
Current from positive supply	Quiescent	—	0.07	0.2	mA
	Full Load				mA
Current from negative supply	Quiescent	—	0.07	0.2	mA
	Full Load				mA

Note: Two 735-AS1's required for each 735-AS2

735-A52 AMPLIFIER SPECIFICATION (Output Amplifier)

3-6-69 4-7-69* GH Wilson

Absolute Maximum Ratings

Supply Voltage		15	V
Input Voltage	Either Input	V_+ / V_-	V
	Between Inputs	7	V
Internal Power Dissipation		300	mW
Storage Temperature Range		-65 to +150	°C
Operating Temperature Range		-20 to +85	°C

Electrical Characteristics

(At T_A = -20° to +85°C, V_+ = +7.5V, V_- = -7.5V, R_L = 8.2kΩ†, unless otherwise specified.)

* †returned to +1.8V, not ground

		Min	Typ	Max	Units
Open-loop Response					
Small Signal	DC Gain				--
	Unity-Gain Bandwidth				MHz
	Gain at ____ MHz				--
Large Signal (Full output = 0 to +5.5V)	Full-output dc gain	15K	-	-	--
	Max. Freq. for full output				MHz
	Max. Slewing Rate				V/μs
Undesired Signal Rejection (r.t.i.)					
	CMRR (CM Input Range = ±4.0V / +4.7V)	-	-	100	μV/V
	Power Supply Rejection (±0.5V)	-	-	200	μV/V
Input Impedance					
Between Inputs	R				MΩ
	Parallel C				pF
Common Mode	R				MΩ
	Parallel C				pF
Input Offset Voltage					
Without external trim		-	-	6	mV
Temperature coefficient, average					μV/°C
Drift (per ____)					μV
Input Current					
~~Either Input~~ Average, both inputs		-	-	100	nA
Offset		-	-	50	nA
Temperature coefficient, ave.	Either Input				nA/°C
	Offset				nA/°C
Drift (per ____)	Either Input				nA
	Offset				nA
Input Noise					
f_o = ____ Hz; Δf = ____ Hz.	Voltage, rms				nV
	Current, rms				pA
f_o = ____ Hz; Δf = ____ Hz.	Voltage, rms				nV
	Current, rms				pA
f_o = ____ Hz; Δf = ____ Hz.	Voltage, rms				nV
	Current, rms				pA
Output					
*Voltage, peak			+5.5V (sourcing 450μA)		V
*Current, peak			0V (sinking 225μA)		mA
Impedance, l.f.					Ω
Power Requirements (At rated supply voltage = ±7.5V)					
Power Dissipation, Quiescent		-	1	3	mW
Current from positive supply	Quiescent	-	0.07	0.2	mA
	Full Load				mA
Current from negative supply	Quiescent	-	0.07	0.2	mA
	Full Load				mA

Note: One 735-A52 required for each 735-A51

Attachment II

Parts List-Single Amplifier, CIAM System

Operating temperature range: -20° to +85°C

A1, A2 RM 4132 selected per spec RM 4132-AS1
A3 RM 4132 selected per spec RM 4132-AS2

Capacitors*

None

Resistors

R1	2K ± 20%
R2, R3	15.7K ± 20%, matched to 5%
(R2 ÷ R3)/R1	15.67 ± 1%

$R_4 = R_4' = R_5 = R_5' =$ KΩ (adjust R_4 and R_5 for zero offset of A1 and A2 respectively).

R6, R7	50MΩ ± 20%, matched to 6%
R9, R10	not used
R11, R12	50KΩ ± 20%
R13, R14	250KΩ ± 20%
R14/R12, R13/R11	5.00 ± 1%, matched to 0.1%

* Insulation resistance >100MΩ

AM-1132-AS1 AMPLIFIER SPECIFICATION

Absolute Maximum Ratings (minimum values)

Supply Voltage		15	V
Input Voltage	Either Input	V+/V-	V
	Between Inputs		V
Internal Power Dissipation		300	mW
Storage Temperature Range		-65 to +150	°C
Operating Temperature Range		-20 to +85	°C

Electrical Characteristics

(At T_A= -20°C to +85°C, V_+= +7.5V, V_-= -7.5V, R_L= 1MΩ, unless otherwise specified.)
Returned to +1.7V, not ground.

		Min	Typ	Max	Units
Open-Loop Response					
Small Signal	DC Gain	15K	—	—	--
	Unity-Gain Bandwidth				MHz
	Gain at _____ MHz				--
Large Signal	Full-output dc gain	40K	—	—	--
(Full output = ±5.3V)	Max. Freq. for full output				MHz
	Max. Slewing Rate				V/μs
Undesired Signal Rejection (r.t.i.)					
	CMRR (CM Input Range= ±5.1V)	—	—	10	μV/V
	Power Supply Rejection (±0.5V)	—	—	25	μV/V
Input Impedance					
Between Inputs	R				MΩ
	Parallel C				pF
Common Mode	R				MΩ
	Parallel C	—	—	2.5	pF
Input Offset Voltage					
Without external trim		—	—	1	mV
Temperature coefficient, average					μV/°C
Drift (per _____)					μV
Input Current					
~~Either Input~~ Average, both inputs		—	—	20	nA
Offset		—	—	10	nA
Temperature coefficient, ave.	Either Input				nA/°C
	Offset				nA/°C
Drift (per _____)	Either Input				nA
	Offset				nA
Input Noise					
f_o= _____Hz; Δf= _____Hz.	Voltage, rms				nV
	Current, rms				pA
f_o= _____Hz; Δf= _____Hz.	Voltage, rms				nV
	Current, rms				pA
f_o= _____Hz; Δf= _____Hz.	Voltage, rms				nV
	Current, rms				pA
Output					
Voltage, peak }	(Sourcing 250μA)	+5.3			V
Current, peak }	(Sinking ~~Sourcing~~ 475μA)	-5.3			mA
Impedance, l.f.					Ω
Power Requirements (At rated supply voltage = ±7.5V)					
Power Dissipation, Quiescent				1	mW
Current from positive supply	Quiescent			0.7	mA
	Full Load				mA
Current from negative supply	Quiescent			0.7	mA
	Full Load				mA

Note: Two AS1's are required for each AS2.

AMPLIFIER SPECIFICATION

Absolute Maximum Ratings (minimum values)

Supply Voltage		15	V
Input Voltage	Either Input	V+/V-	V
	Between Inputs	7	V
Internal Power Dissipation		300	mW
Storage Temperature Range		-65 to +150	°C
Operating Temperature Range		-20 to +85	°C

Electrical Characteristics

(At T_A=-20°to+85°C, V_+= _____, V_-= _____, R_L= 2.2kΩ, unless otherwise specified.)
Y returned to +1.2 V, not ground

			Min	Typ	Max	Units
Open-Loop Response						
Small Signal	DC Gain		—	—	—	--
	Unity-Gain Bandwidth		—	—	—	MHz
	Gain at _____ MHz		—	—	—	--
Large Signal	Full-output dc gain		15K	—	—	--
(Full output = _____)	Max. Freq. for full output		—	—	—	MHz
	Max. Slewing Rate		—	—	—	V/μs
Undesired Signal Rejection (r.t.)		+4V				
	CMRR (CM Input Range= -4.0V)		—	—	100	μV/V
	Power Supply Rejection (±0.5V)		—	—	200	μV/V
Input Impedance						
Between Inputs	R		—	—	—	MΩ
	Parallel C		—	—	—	pF
Common Mode	R		—	—	—	MΩ
	Parallel C		—	—	—	pF
Input Offset Voltage						
Without external trim			—	—	6	mV
Temperature coefficient, average			—	—	—	μV/°C
Drift (per _____)			—	—	—	μV
Input Current						
~~Either Input~~ Average, both inputs			—	—	100	nA
Offset			—	—	50	nA
Temperature coefficient, ave.	Either Input		—	—	—	nA/°C
	Offset		—	—	—	nA/°C
Drift (per _____)	Either Input		—	—	—	nA
	Offset		—	—	—	nA
Input Noise						
f_o= _____Hz; Δf= _____Hz.	Voltage, rms		—	—	—	nV
	Current, rms		—	—	—	pA
f_o= _____Hz; Δf= _____Hz.	Voltage, rms		—	—	—	nV
	Current, rms		—	—	—	pA
f_o= _____Hz; Δf= _____Hz.	Voltage, rms		—	—	—	nV
	Current, rms		—	—	—	pA
Output						
Voltage, peak	(sourcing 450μA)		+5.5V	—	—	V
Current, peak	(sinking 225μA)		0 V	—	—	mA
Impedance, l.f.			—	—	—	Ω
Power Requirements (At rated supply voltage = _____)						
Power Dissipation, Quiescent			—	—	1	mW
Current from positive supply	Quiescent		—	—	0.07	mA
	Full Load		—	—	—	mA
Current from negative supply	Quiescent		—	—	0.07	mA
	Full Load		—	—	—	mA

Attachment III

CIAM PERFORMANCE SPECIFICATIONS

AIM inc

INTENDED OPERATING CONDITIONS	Config. A	Config. B
Supply Voltage	± 7.5V	± 7.5V
Power Dissipation	13 mW	4 mW
Differential Source Resistance	5kΩ	5kΩ
Differential Source Resistance Unbalance	± 1kΩ	± 1kΩ
Temperature Range	-20°C≤T≤+85°C	-20°C≤T≤+85°C
Output Loading	10-200 pf $R_{dc} \gtrsim \infty$	10-200 pf $R_{dc} \gtrsim \infty$

ELECTRICAL PERFORMANCE CHARACTERISTICS

Parameter			Typical
Differential Input Resistance			100 MΩ
Common-Mode Input Resistance			25 MΩ
Output Resistance			.2Ω
Power Dissipation			4mW
Gain			166.6± 1%
Small Signal Bandwidth			6kHz
Slew Rate			20V/msec
Common-Mode Rejection Ratio			461μV/5V
Components:	Pre amp	CM-1 100μv/5v	
		CM-1a 125μv	
		CM-2 120μv	
		CM-3 36μv	
	Post amp	CM-1 30μv	
		CM-2 50μv	
Power Supply Rejection Ratio			32μV/5v
Input Offset Voltage (including TCVos)			2.4mV
TC Input Voltage			6μV/°C
Input Bias Current (common mode)			10nA to (0V Common mode) .00 nA (± 5V Common mode)
Input Offset Voltage Due to Input Offset Current			1?9μV
Noise (6kHz bandwidth)			4μV rms
Total Error			24μV p-p

Attachment IV

Test Procedures - CIAM Amplifier (Using μA735 or RM 4132)

Overall CIAM Amplifier (Mandatory Tests)

Note: Unless otherwise specified, V+ = +7.5V, V- = -7.5V, T=25°C and the CIAM output is assumed unloaded and referenced to ground. Refer to Fig. 1 for terminal identification numbers.

1. Differential Input Resistance (Refer to Fig. 2)

With full scale input of 120 mV p-p at a frequency ≤60 Hz applied, vary the balanced source resistance between 0 and 1MΩ and observe output voltage variation. It must be 1% of full scale i.e.≤| ±50 mV| . Insure that common mode voltage is less than 0.5V at terminals 1 and 2. Measure at 1 and 2 with HiZ AC VT VM, with input signal generator set to 0V out, and .5MΩ resistors shorted.

2. Common-Mode Input Resistance (Refer to Fig. 3)

Apply a convenient low frequency AC signal, say 10V p-p @ 60 Hz in series with a large capacitor, say 0.1μF, and a 1MΩ resistor to the shorted-across inputs of the CIAM amplifier and observe the voltage across the 1MΩ resistor. It must be ≤400 mV p-p.

3. Output Resistance (Refer to Fig. 4)

With input at an amplitude sufficient to drive output to 0.2 mV referenced with the output reference tied to ground, vary output load from $R_L = 0.2\Omega$ to $R_L = \infty$, (by opening it) keeping input constant. Observe change in output voltage. It must be <0.1mV.

4. Power Dissipation (Refer to Fig. 5)

a. Measure the currents flowing between the amplifier and the V+ and V- supplies at ± 7.5V, with the inputs shorted together and floating and the output floating. They will be equal and must be less than 135 μA.

b. Apply a differential input voltage of ± 30 mV, with the amplifier unloaded. The sum of the currents from the V+ and V- supplies must not exceed 200 μA.

5. Gain and Gain Linearity (Refer to Fig. 6)

Apply differential input voltages of ±30 mV ± 60 mV and observe the output. It must be within 1% of ± 2.5V and ± 5V (respectively).

6. Small Signal Bandwidth (Refer to Fig. 7)

Apply a differential input voltage of ± 1.0 mV p-p, first at 60 HZ and thence at 6KHZ, while measuring the output voltage referenced from ground. The output amplitude must not vary more than 3 db.

7. Slew Rate (Refer to Fig. 8)

With an input differential signal applied producing ± 5V peak output into a 50 KΩ load at a low frequency, say 60 Hz, advance the frequency until the amplitude drops to ± 4V. This frequency must be greater than 700 HZ. Alternately, a square wave input can be applied, driving the output to ± 5V, and the rise rate after switching measured on an oscilloscope. It must be 20V/m Sec.

8. Linear Output Voltage Swing (Refer to Fig. 9)

With a 100 kΩ load resistor, apply ± 66 mV (either p-p AC or DC voltage) and observe output voltage of the amplifier. It must be $\geq$ |.990 [gain (measured with 5V out in test 5) x ± 66 mV]|.

9. Common Mode Rejection Ratio (Refer to Fig. 10)

With a source imbalance of 1KΩ, apply a convenient low frequency, say 60 Hz, signal of 5V p-p referenced to ground to the amplifier inputs. Measure the output amplitude. The output amplitude must be $\leq$ 38.5mV.

10. Power Supply Rejection Ratio (Refer to Fig. 11)

Increase |V+| by 0.5V and decrease |V-| by 0.5V, with input shorted. Observe change in output voltage. It must not exceed 2.1 mV. Repeat, varying V+ and V- in opposite direction.

11. Input Offset Voltage, Including TC VOS (Refer to Fig. 12)

Measure output voltage with input shorted at -20°C, + 25°C and +85°C. The output voltage must not exceed ± 192 mV, referenced to ground.

12. Input Bias Current (Refer to Fig. 13)

With one input grounded through a 100kΩ resistor and the other shorted to the ground, measure the output voltage with the two inputs differential input shorted and unshorted. The variation in output voltage must be ± 166 mV. Repeat, reversing the inputs.

13. Input Offset Current (Refer to Fig. 14)

With 100kΩ to ground from each input, first short and then unshort across the input terminals, observing the output voltage variation. It must be ≤ 83 mV.

14. Noise (Refer to Fig. 15)

With an RC filter on the output as shown, observe the p-p noise on an oscilloscope. It must be ≤ 300 mV p-p.

15. Output Offset by +2.75V

With the output reference terminal connected to + 2.75V vary the differential signal input from + 30 mV to -30 mV and read output voltage referenced to ground. It must be + 5.0V and 0V respectively within ± 50 mV.

CIAM Subcircuits (Optional Tests)

I. DA (For definition of DA see CIAM Schematics I and II)

1. A-1 and A-2 Offsets Short terminals 2-3 on each op amp and measure their output voltages at nodes B and C. They must each be 0 ± 1V.

2. DA Gain With ± 30 mV differentially applied to DA inputs, observe differential voltage between nodes B and C. V_{BC} should be within 1% of 500 mV.

II. OA (For definition of OA see CIAM Schematics I and II)

1. Common mode Rejection Ratio Apply ± 5V to nodes B and C (OA input) with nodes B and C shorted together. Observe the output voltage with the reference terminal grounded. It must be $\leq$ 5 mV.

2. Gain Apply ± 500 mV to the input of the OA (to terminals B and C) and observe the output with reference terminal grounded. It must be ± 2.5V within 1%.

Attachment V

Suggested Procedures for Resistor Adjustment

In implementing the resistors in the CIAM amplifier there is a choice between passive and active adjustment. The resistors can be adjusted for the required nominal values and ratio match before the op amp chips are bonded in--i.e. "passive"adjustment --or they can be adjusted with the op amps active, to force such parameters as offset voltage, offset current and common mode ratio very close to their ideal value--zero. When the latter is done, performance may drift faster as the temperature moves away from the temperature existing during adjustment, but still the performance is closer to ideal at most temperatures. Therefore, active adjustment is recommended for most of the ratios, while passive adjustment is usually restricted to those cases where it is necessary to achieve the nominal values specified--generally to a 20% tolerance.

Four resistor ratios will probably require adjustment:

(1) The input bias resistors

(2) The voltage offset balancing resistors

(3) The DA gain determining resistors

(4) The OA gain determining resistors.

It is recommended that the voltage offset balancing resistors be adjusted first by shorting across the input to each op amp and adjusting for a minimum voltage out using the test set up in Attachment IV. Then the input bias resistors can be adjusted

either for minimum offset current or minimum common mode rejection ratio (in μv/v rti).

The best approach is to adjust the bias resistors for minimum error with a maximum common mode voltage (± 5V), and the maximum source resistance (5KΩ), and also if possible to adjust the nominal values of the two resistors, for 0V at the input at room temperature. But if the latter procedure is too complex, then it is recommended that CMRR be minimized, by adjusting the bias resistors for minimum AC out of the CIAM amplifier while applying a 5V AC common mode signal.

The third adjustment should then be to set the DA gain determining resistors for the target differential gain--16 2/3. This is best done by adjusting the center resistor, R_1 while applying an AC differential input and observing the DA output at BC.

Finally, it is necessary to adjust OA gain to 1% and CMRR to 0.1% with R_{11} through R_{14}. It is recommended that R_{13} and R_{14} be adjusted passively (before the op amp is bonded) for the required 1% ratios. Then one of the set of four resistors, R_{11} through R_{14}, should be actively adjusted to minimize the CMRR.

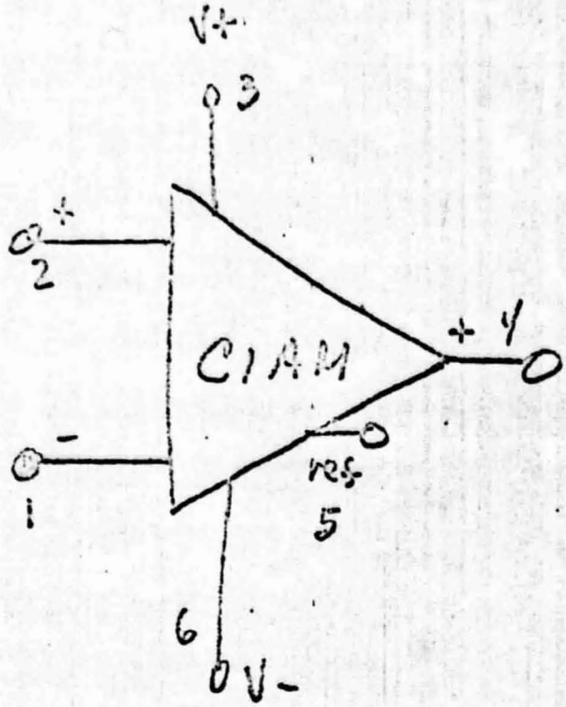


Fig. 1 CIAM Terminal Identification.

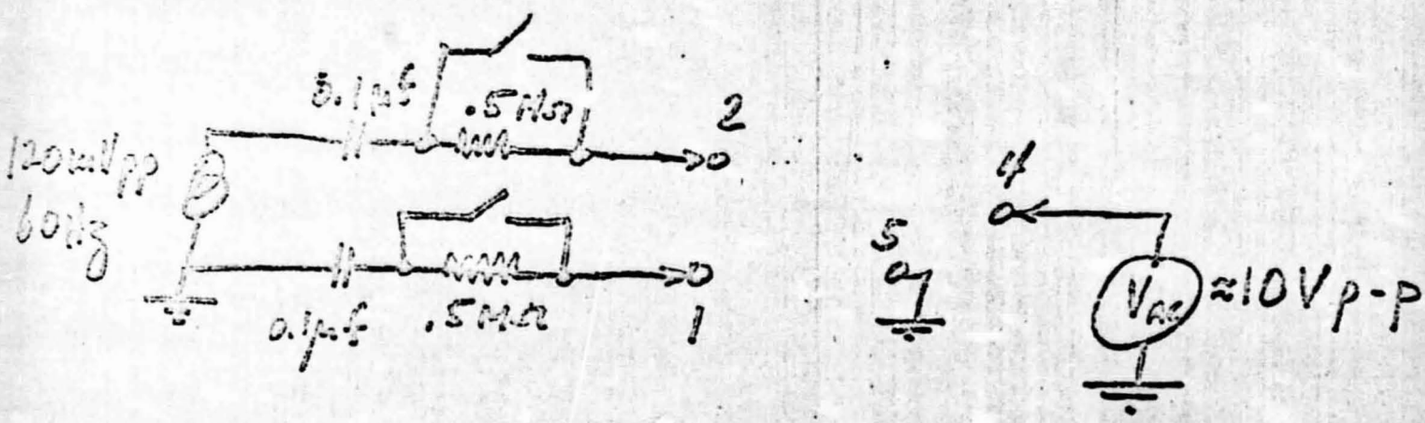


Fig. 2 Differential Input Resistance.

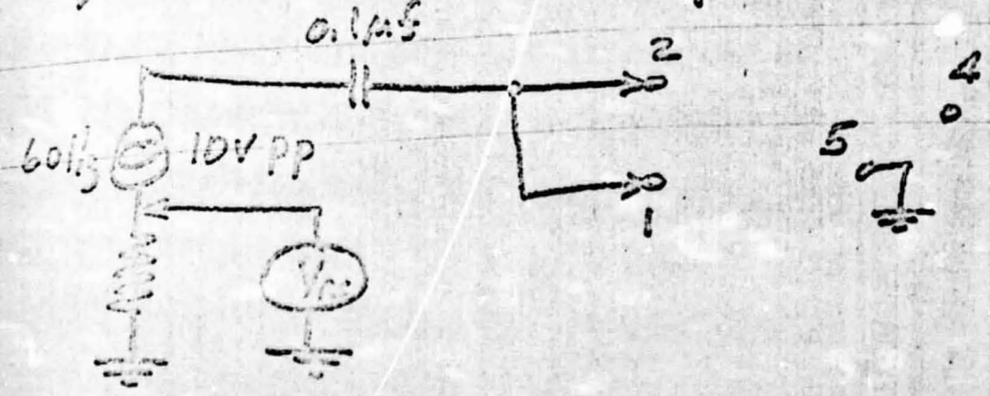


Fig. 3 Common Mode Input Resistance.

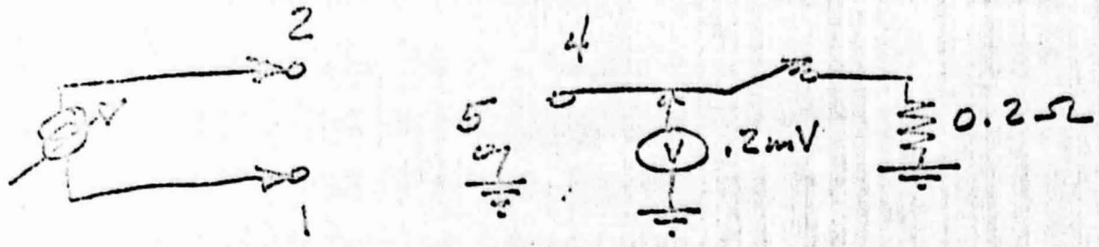


Fig. 4 Output resistance

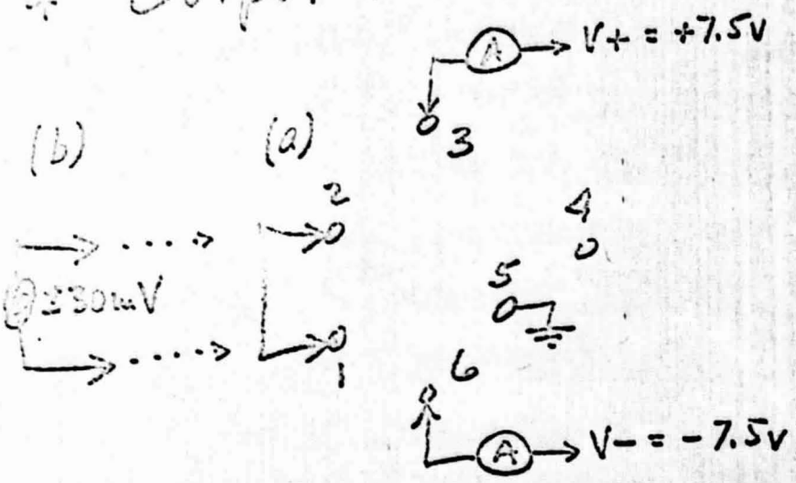


Fig. 5 Power Dissipation

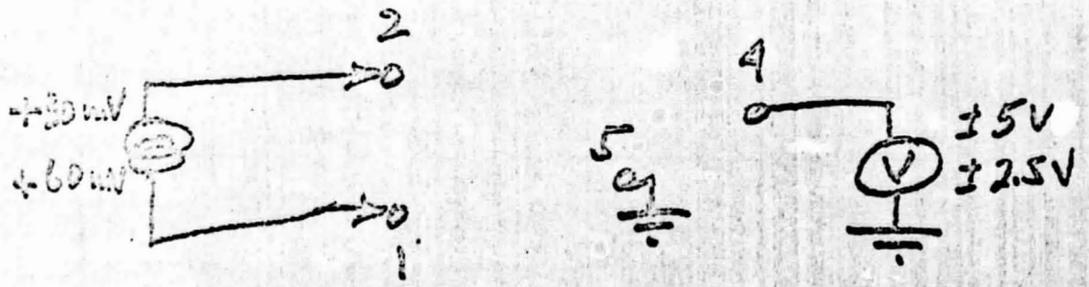
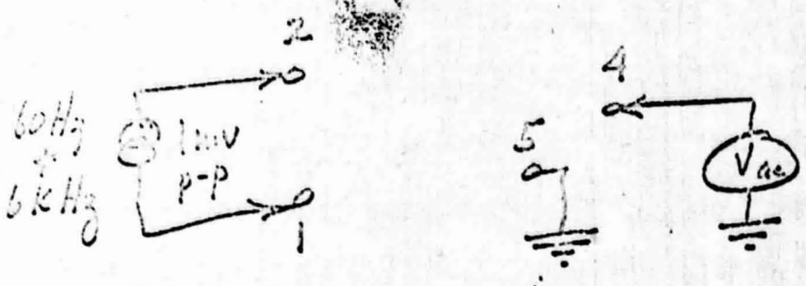
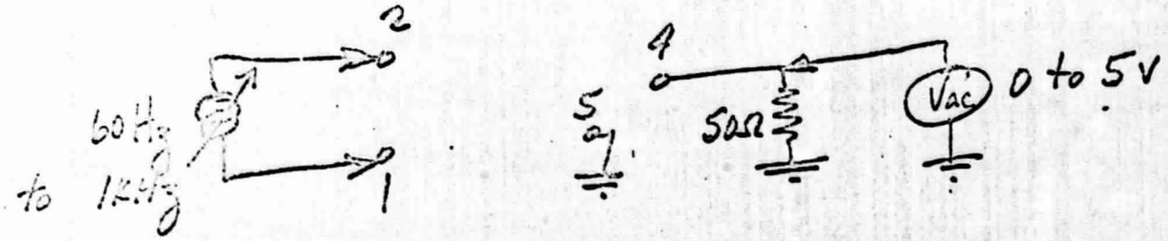


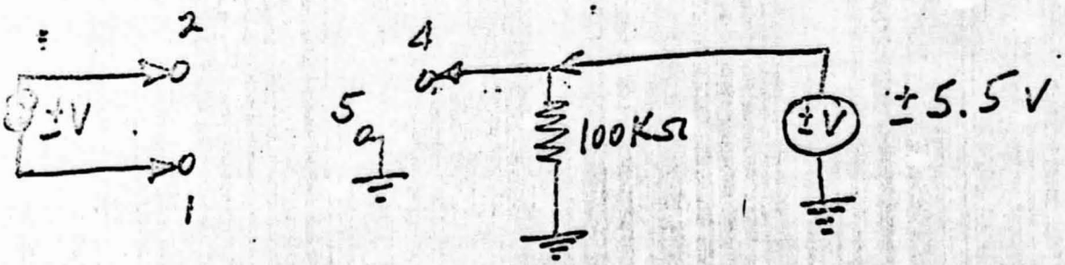
Fig. 6 Gain



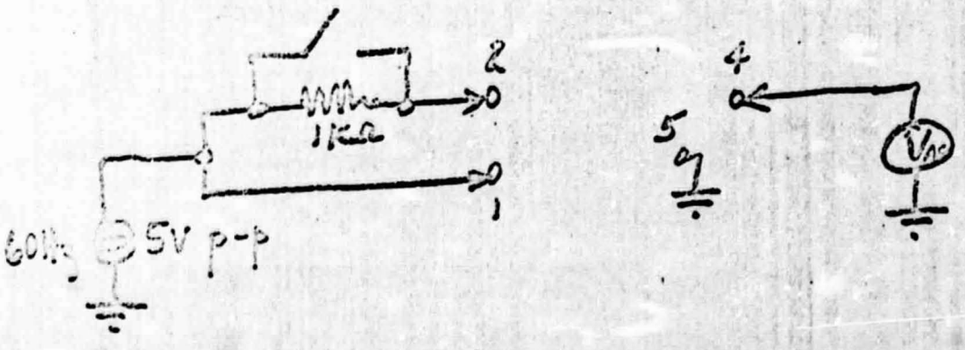
7. Small Signal Bandwidth



8. Slew Rate

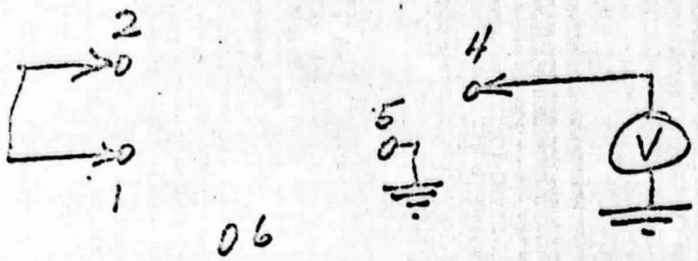


9. Output Voltage Swing



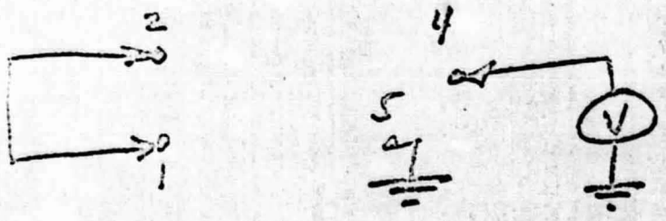
10. Common Mode Rejection Ratio

+7.5±.5V
03



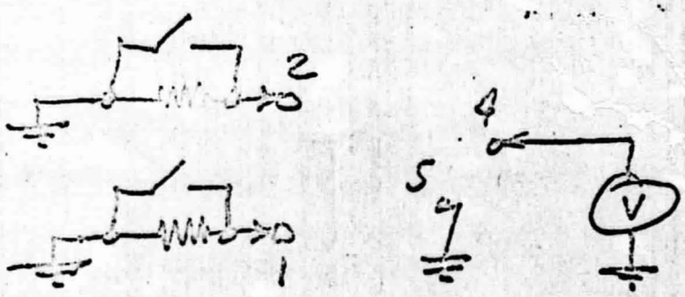
06
-7.5±.5V

11. Power Supply Rejection Ratio

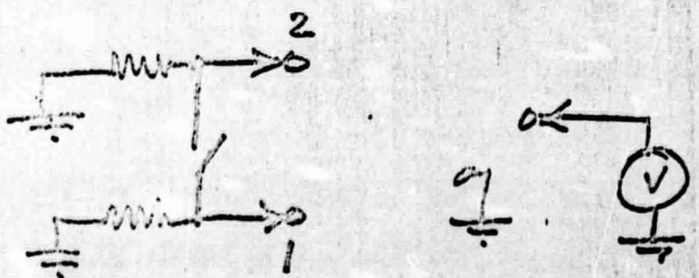


T = -20°C
T = 25°C
T = 85°C

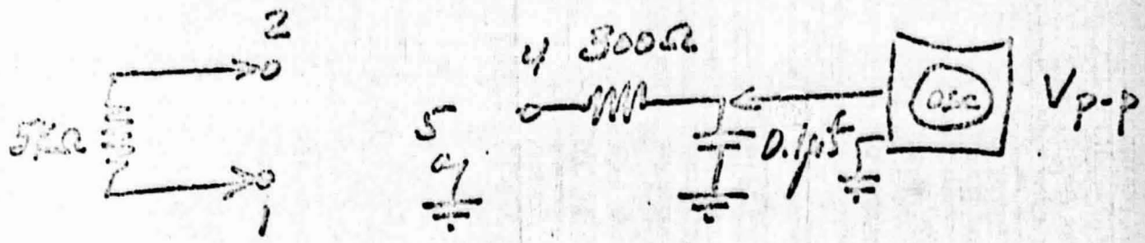
12. Input Voltage Offset



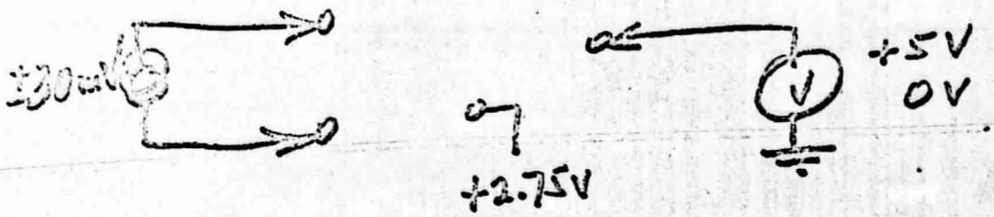
13. Input Bias Current



14. Input Offset Current



15. NOISE



16. OUTPUT OFFSET

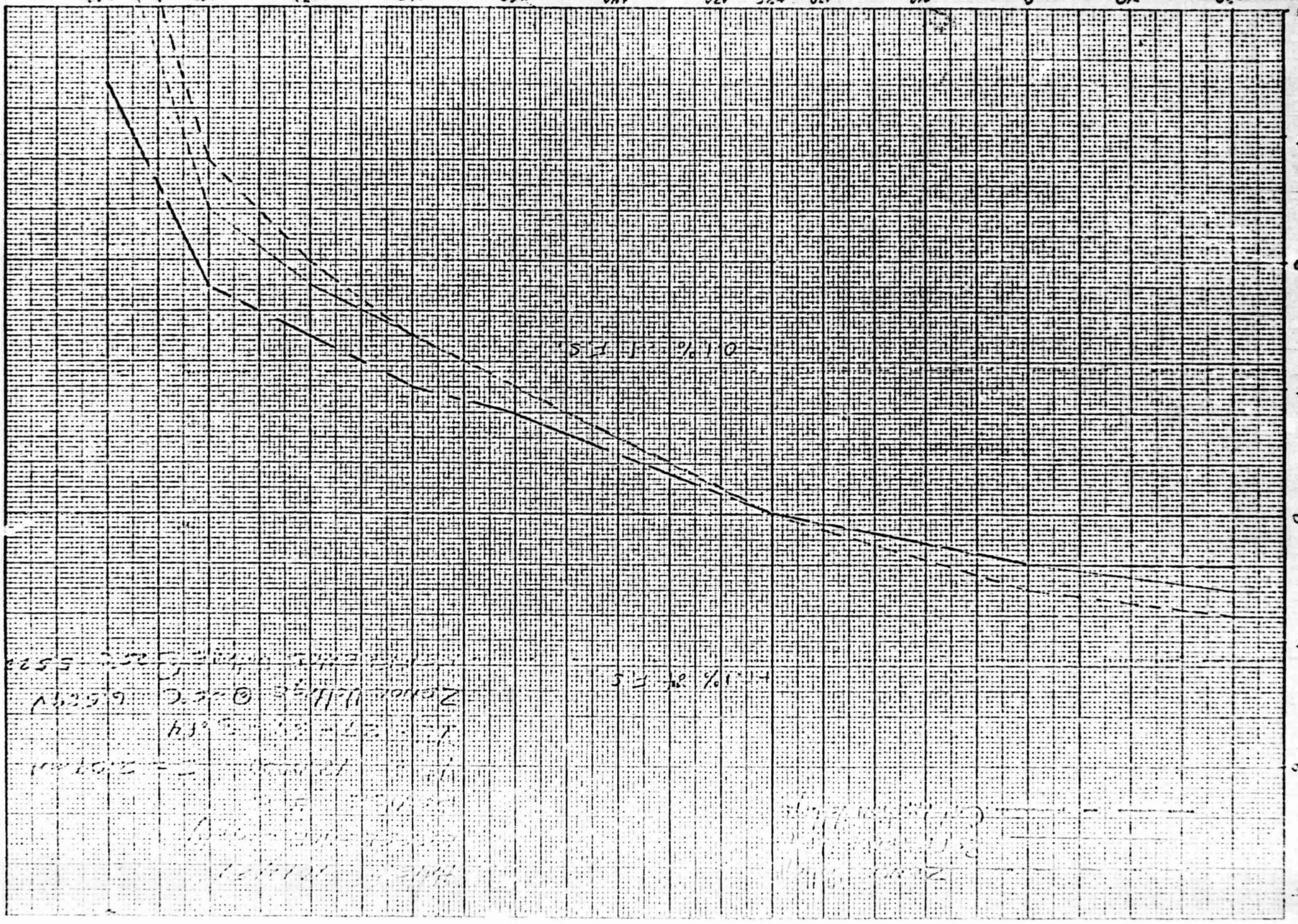
REFERENCE SUPPLY

RS-1

HALEX

PERFORMANCE TESTS

Temperature in °Centigrade



Temperature IN °Centigrade

-20 -10 0 10 20 30 40 50 60 70 80 90

50

10

5

0

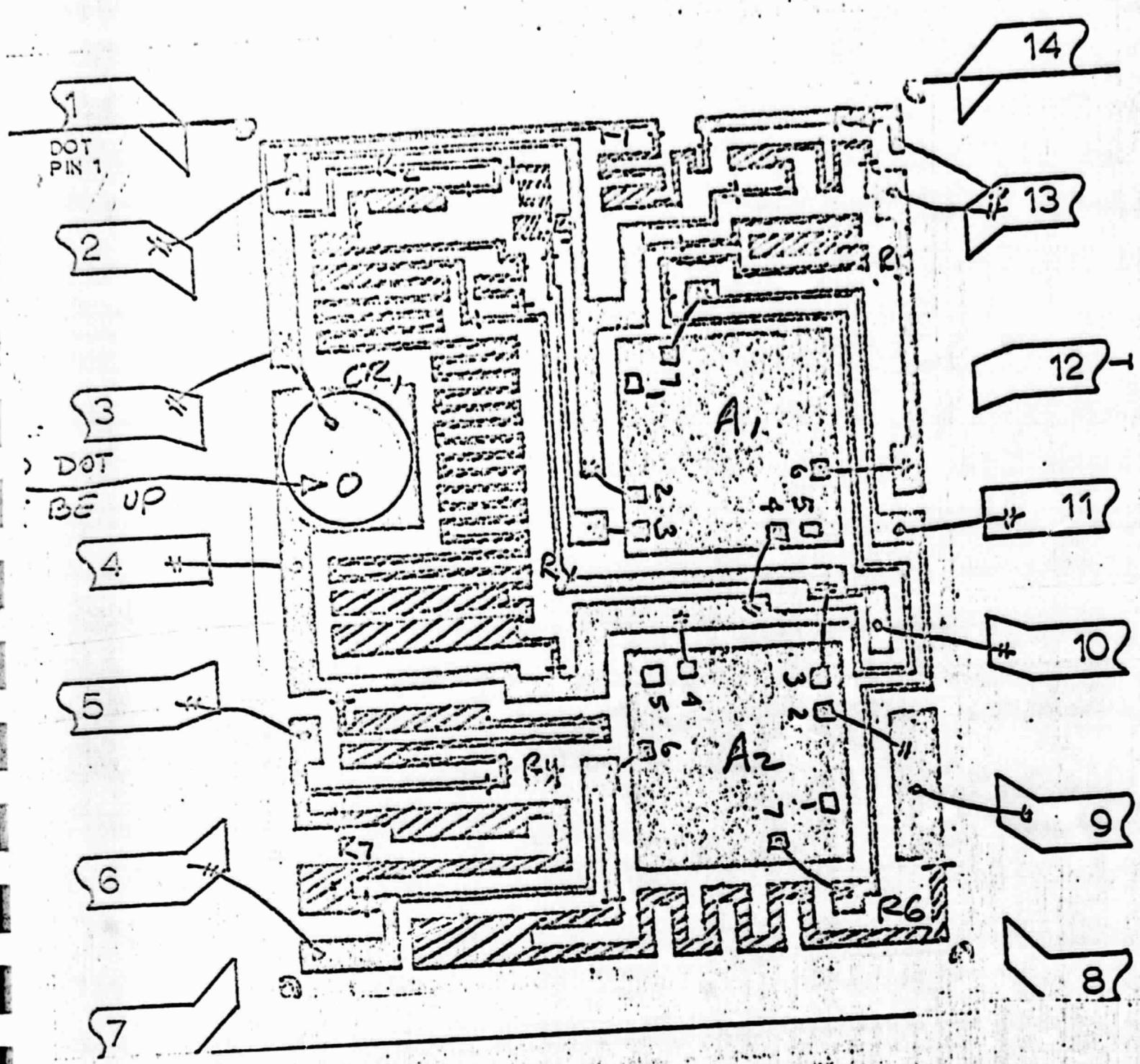
-5

TEMPERATURE IN °CENTIGRADE

ERROR FROM 25°C READING IN MV.

Temperature in °Centigrade

Error from 25°C Reading in mv.



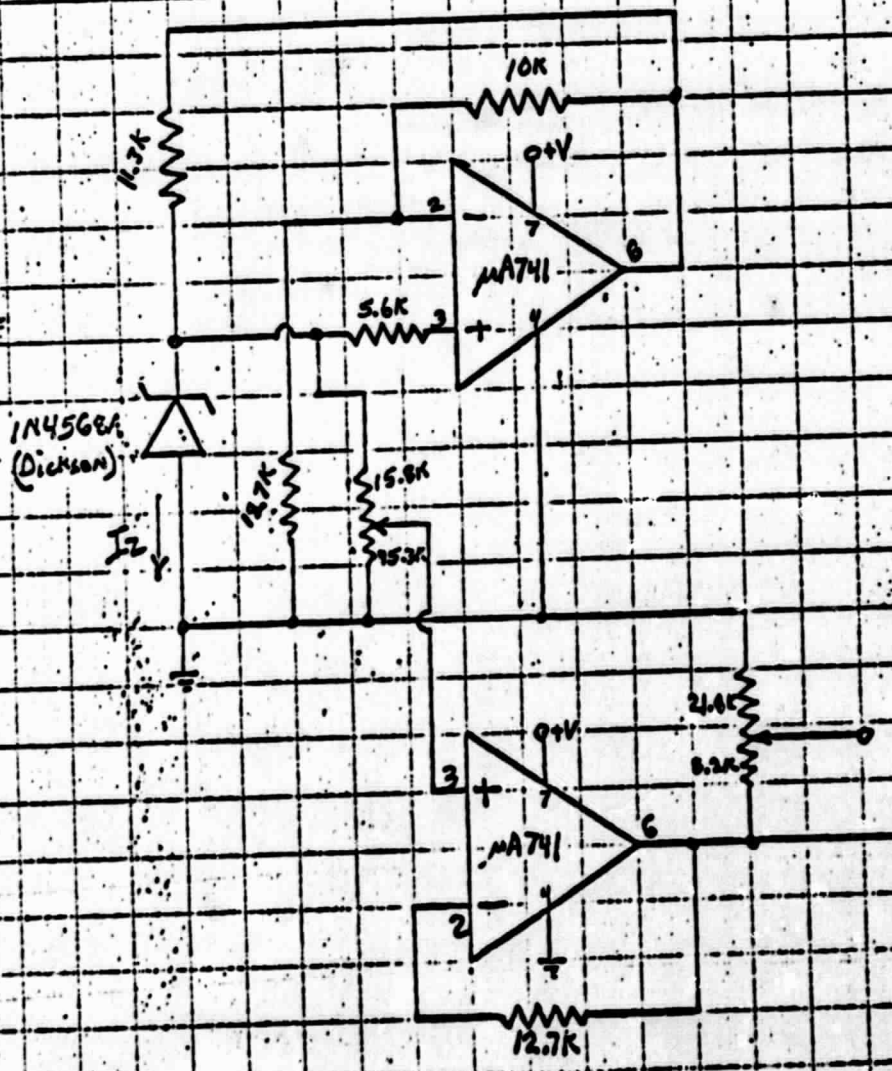
RS-1

Reference Supply

20X

Power Supply Currents were measured under conditions described on page 81 :

Device	$I_{V^+(5V)}$	I_{V^+}	$I_{V^-(5V)}$	I_{V^-}	I_{GND}
1					
2					
3					
4					



Precision Calibration and Reference Supply

Performance of circuit shown on facing page.

	V^+ (v)	I_Z (μa)	E_{OUT} (v)	e_{noise} (rms, μv)
T = -20°C	11.00	242	5.503	1.17
	11.50	242	5.503	1.40
	12.00	242	5.503	1.45
	12.50	242	5.503	1.35
	13.00	242	5.503	1.35
T = 0°C	11.00	242	5.503	1.25
	11.50	242	5.503	1.23
	12.00	242	5.503	1.20
	12.50	242	5.503	1.21
	13.00	242	5.503	1.24
T = 25°C	11.00	242	5.502	1.10
	11.50	242	5.502	1.14
	12.00	242	5.502	1.15
	12.50	242	5.502	1.07
	13.00	242	5.502	1.08
T = 50°C	11.00	242	5.499	1.15
	11.50	242	5.499	1.13
	12.00	242	5.499	1.10
	12.50	242	5.499	1.10
	13.00	242	5.499	1.10
T = 85°C	11.00	241	5.486	0.93
	11.50	241	5.485	0.88
	12.00	241	5.485	1.02
	12.50	241	5.485	1.12
	13.00	241	5.485	1.04

Power consumption @ 25°C & V^+ @ +12.00v = 13.80 mw

CALIBRATION REFERENCE SUPPLY

ΔEo vs. TEMPERATURE for Vt = 12.00V

BREAD BOARD VERSION

0.19% of F.S.

15
10
5
0
5
10
15
20

-20 -10 0 +10 +20 +25 +30 +40 +50 +60 +70 +80 +85 +90

SPECIFICATION RS-1

REFERENCE SUPPLY
&
PRECISION CALIBRATION ASSEMBLY
HIGH LEVEL

April 16, 1969

1.0 CONSTRUCTION

Hybrid circuit consisting of two μA741 monolithic operational amplifer chips, one ME1Z4568A precision reference zener chip, and one precision resistor network assembled on a glazed alumina substrate and adjusted for specified precision voltage outputs.

2.0 PACKAGE

As required--However, a 1/4" X 1/4" X 0.070 inch - 10 lead flat pack ceramic case would be perferrable.

3.0 TEMPERATURE

Operating: -20°C to + 85°C
Storage: -55°C to + 100°C

4.0 SCHEMATIC

See Figure 1.

5.0 COMPONENTS

5.1 OPERATIONAL AMPLIFIERS

2- μA741 -Full military specification. (Manufactured by Fairchild Semiconductor)

5.2 DIODES

1-ME1Z4568A-Low current, low temperature coefficient precision reference zener diode. (Manufactured by Dickson Inc)

5.3 RESISTORS

R_1 : 11.3K ± 5%, TC $\leq$ 50ppm/°C,
R_2 : 113K ± 5%, TC $\leq$ 50ppm/°C
R_3 : 5.6K ± 5%, TC $\leq$ 50ppm/°C
R_4 : 10.0K ± 5%,
R_5 : 18.7K ± 5%
$\frac{R_4}{R_5}$: matched to $\leq$ 1% of 0.54
$\frac{R_4}{R_5}$: TC tracking $\leq$ 10ppm/°C

R_6: 13.7K ± 5%, TC ≤ 50ppm/°C

Defining $\beta = \frac{R_x}{R_2}$ where R_x is a fraction of R_2 initially adjusted to yield 5.510 ± 0.0005 volts DC at output number 1 (see schematic) at room temperature and V^+ = 12.00 ± 0.10 volts DC. Hence β:TC tracking ≤ 10ppm/°C

R_7 : 30K ± 5%, TC ≤ 50ppm/°C.

Defining $\alpha = \frac{R_y}{R_7}$ where R_y is a fraction of R_7 initially adjusted to yield 4.000 ± 0.0005 volts DC at output number 2.
At room temperature, V^+ = 12.00 ± 0.10 volts DC, and the voltage at output #1 adjusted at 5.510 ± 0.0005 volts DC. Hence,
α :TC tracking ≤ 10ppm/°C

6.0 ELECTRICAL FUNCTIONAL TEST

6.1 INITIAL ADJUSTMENT 1.

After all parts have been assembled set up circuit as shown in Figure 2. Adjust the tap on R_2 until output #1 is 5.510 ± 0.0005 volts DC.

6.2 INITIAL ADJUSTMENT 2

After performing initial adjustment #1, adjust the tap or R_7 until output #2 is 4.000 ± 0.0005 volts DC.

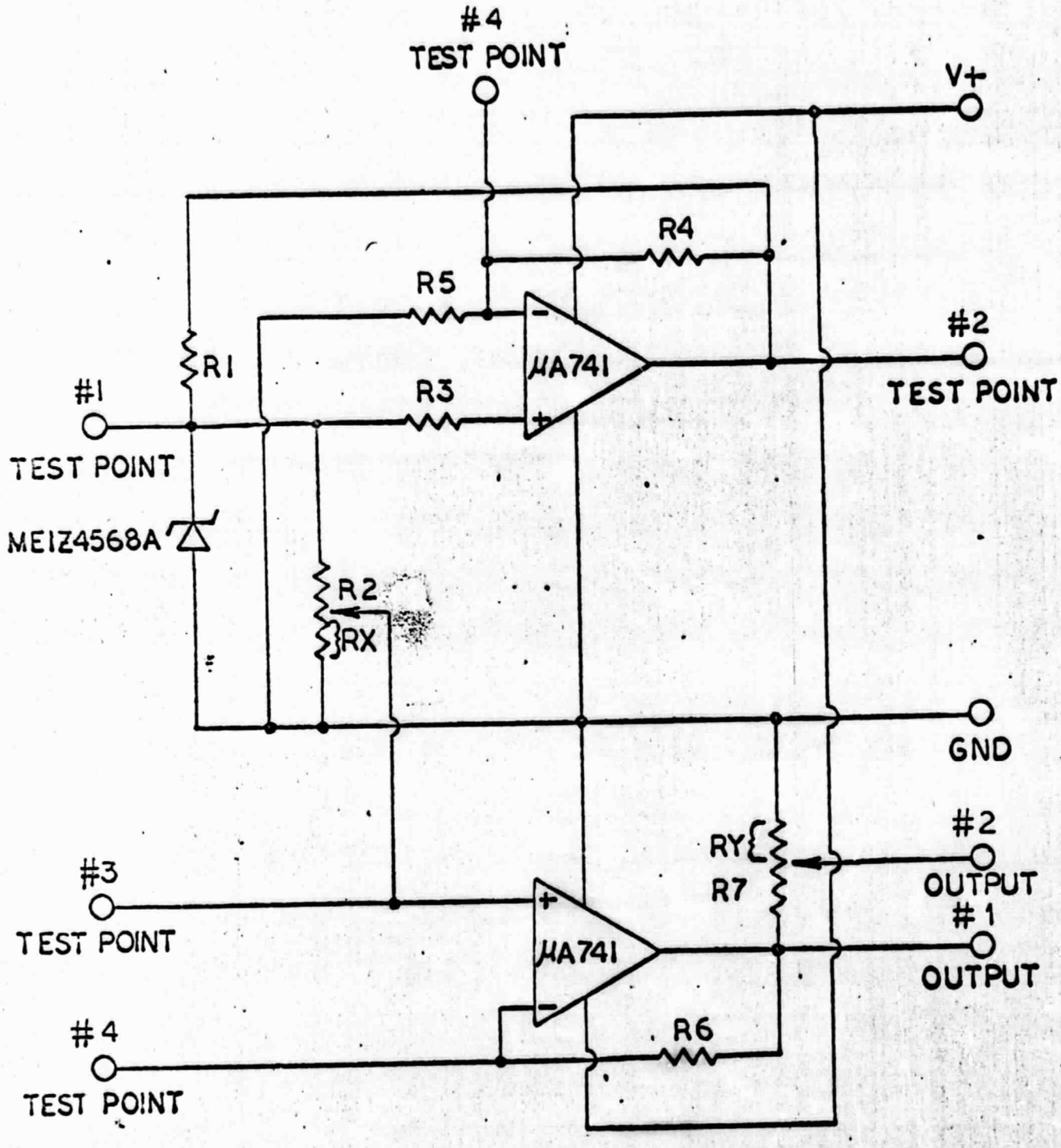


FIGURE 1 : PRECISION CALIBRATION AND REFERENCE SUPPLY.

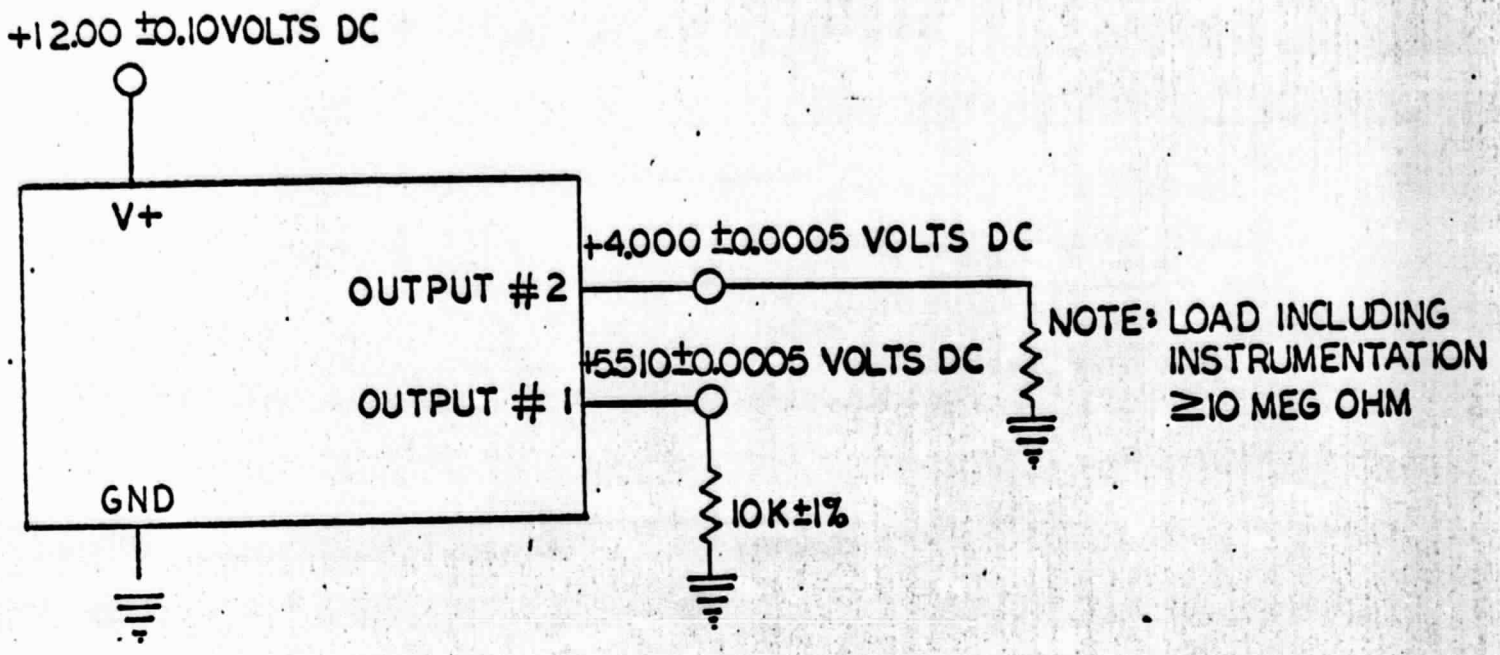


FIGURE 2 : FUNCTIONAL TEST SET UP.

Radiation Instruments

RA-909-A

Operational Amplifier:

Performance in The Triple Amplifier Configuration

6/27/69

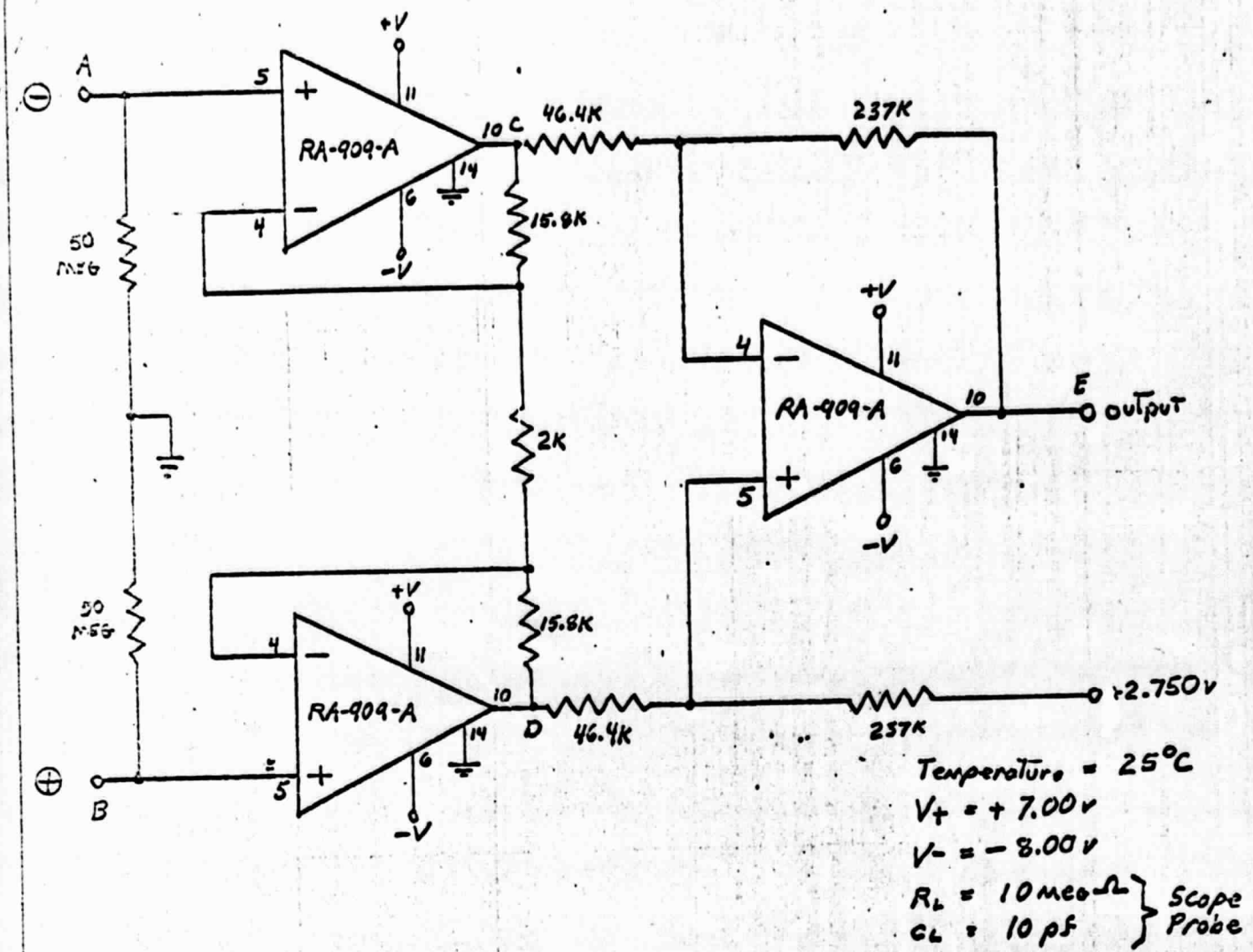


Figure 1

Triple Amplifier Configuration

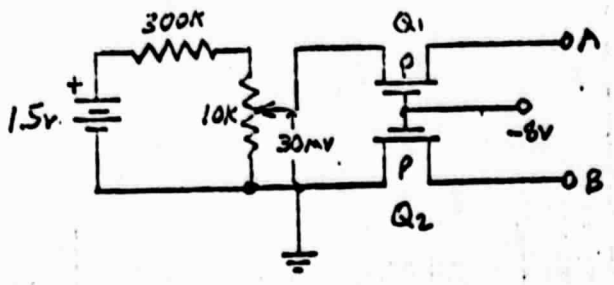
I. A 5KΩ resistor was Tied across points A, B and the D.C. voltages at the lettered points were measured:

pt.	voltage
A	-0.758v
B	-0.759v
C	-2.640v
D	-2.580v
E	+2.870v

I_{V+} = 2.944 ma
I_{V-} = 2.603 ma

$P_D = (15v)(5.547ma) = 83.2 mw$

II The following circuit was connected to points A, B of Fig. 1: (5K removed)
$Q_1, Q_2 \rightarrow$ 10 mil



Again the D.C. voltages at the lettered points of Figure 1 were measured:

pt	voltage
A	+0.030v
B	0v
C	+0.246v
D	-0.195v
E	+0.275v

$I_{V^+} = 2.670$ ma
$I_{V^-} = 2.646$ ma

$P_D = (15.0v)(5.316\,ma) = 79.74$ mw

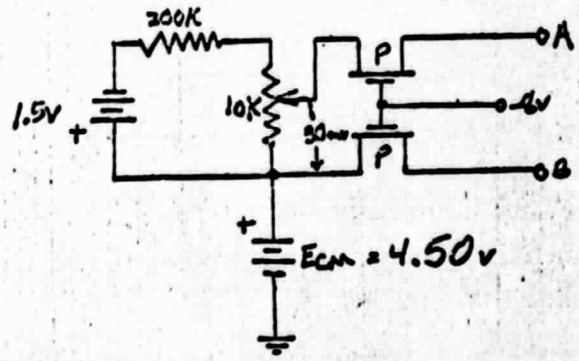
III As per II above except the polarity of the 30mv. signal was reversed:

pt	voltage
A	-0.030v
B	0v
C	-0.301v
D	+0.289v
E	+5.320v

$I_{V^+} = 2.653$ ma
$I_{V^-} = 2.607$ ma

$P_D = (15.0v)(5.260\,ma) = 78.90$ mw

IV The following circuit was connected to points A, B of Fig. 1:



Voltages at lettered points of Figure 1:

pt	voltage
A	+4.47v
B	+4.50v
C	+4.21v
D	+4.76v
E	+5.30v

$I_{V^+} = 2.640$ ma
$I_{V^-} = 2.605$ ma

$P_D = (15.0v)(5.245\,ma) = 78.68$ mw

V. As per IV above except polarity of E_{CM} was reversed and changed to -4.20v:

pt	voltage
A	-4.23v
B	-4.20v
C	-4.48v
D	-3.94v
E	+5.35v

$I_{V+} = 2.650\,ma$
$I_{V-} = 2.600\,ma$

$P_D = (15.0v)(5.250ma) = 78.75mw$

VI. From II and III above, differential voltage gain may be calculated:

$$A_V = \frac{\Delta E_O}{\Delta E_{in}} = \frac{5.320v - 0.275v}{0.060v} = 84.08$$

VII. Output offset voltage reffered to the input (E_{OSI}) may be determined from I and VI:

$$E_{OSI} = \frac{2.870v - 2.750v}{84.08} = \frac{0.120v}{84.08} = 1.41mv$$

VIII. The inputs were allowed to float (5K shunt was removed from A, B). The output went hard against the V^- supply

IX CMRR a 2KΩ resistor was connected to pt. A and a 3KΩ resistor was connected to pt B, of circuit of Figure 1. The other ends were tied together to a common-mode voltage, E_{CM}.

E_{CM}	E_{OUT} (pt E)
0v	+2.860v
+4.00v	+2.843v
-4.00v	+2.870v

$$CMR = \frac{\Delta E_{CM}}{\Delta E_{OUT}} \cdot A_V$$

$$= \frac{8.00v}{0.027v} \cdot 84.08$$

$$= 24,888$$

$$CMRR = 20 \log CMR$$

$$= 20 \log 24,888$$

$$= 87.92db$$

X Frequency Response

Two MOSFETS were connected as per II, a signal generator being substituted for the 30 mv signal:

Frequency	e_{in}	e_{out}
1 KC	0db	38.4 db
2 KC		38.4 db
4 KC		38.4 db
8 KC		38.4 db
10 KC		38.4 db
20 KC		38.4 db
40 KC		38.4 db
60 KC		38.4 db
100 KC		38.4 db
200 KC		38.2 db
400 KC		37.5 db
600 KC		32.3 db
1000 KC		26.2 db
2000 KC		17.6 db
4000 KC		14.3 db
6000 KC		14.2 db
10000 KC		14.1 db

The above data is graphed on the following page. The decreasing slope of the line above 1 MC is believed to be due to noise pickup by the circuit and hence the measurements are NOT accurate above this frequency.

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FREQUENCY RESPONSE RADIAN TRIPLE AMPLIFIER CONFIGURATION

40
38
36
34
32
30
28
26
24
22
20
18
16
14

10KC 100KC 1MC 10MC

→ Frequency

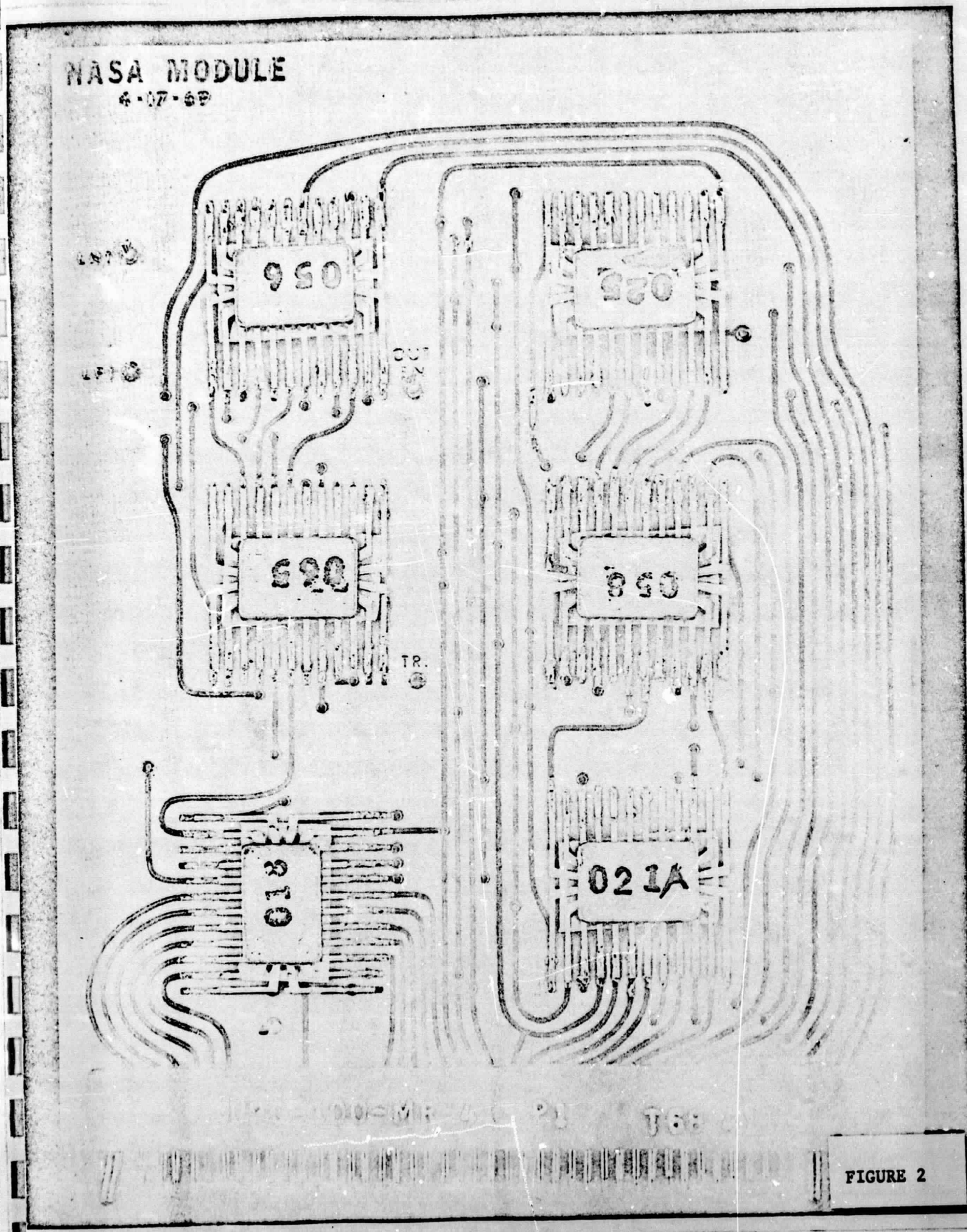

FIGURE 2

GENERAL INSTRUMENT

A/D CONVERTER GI 1001

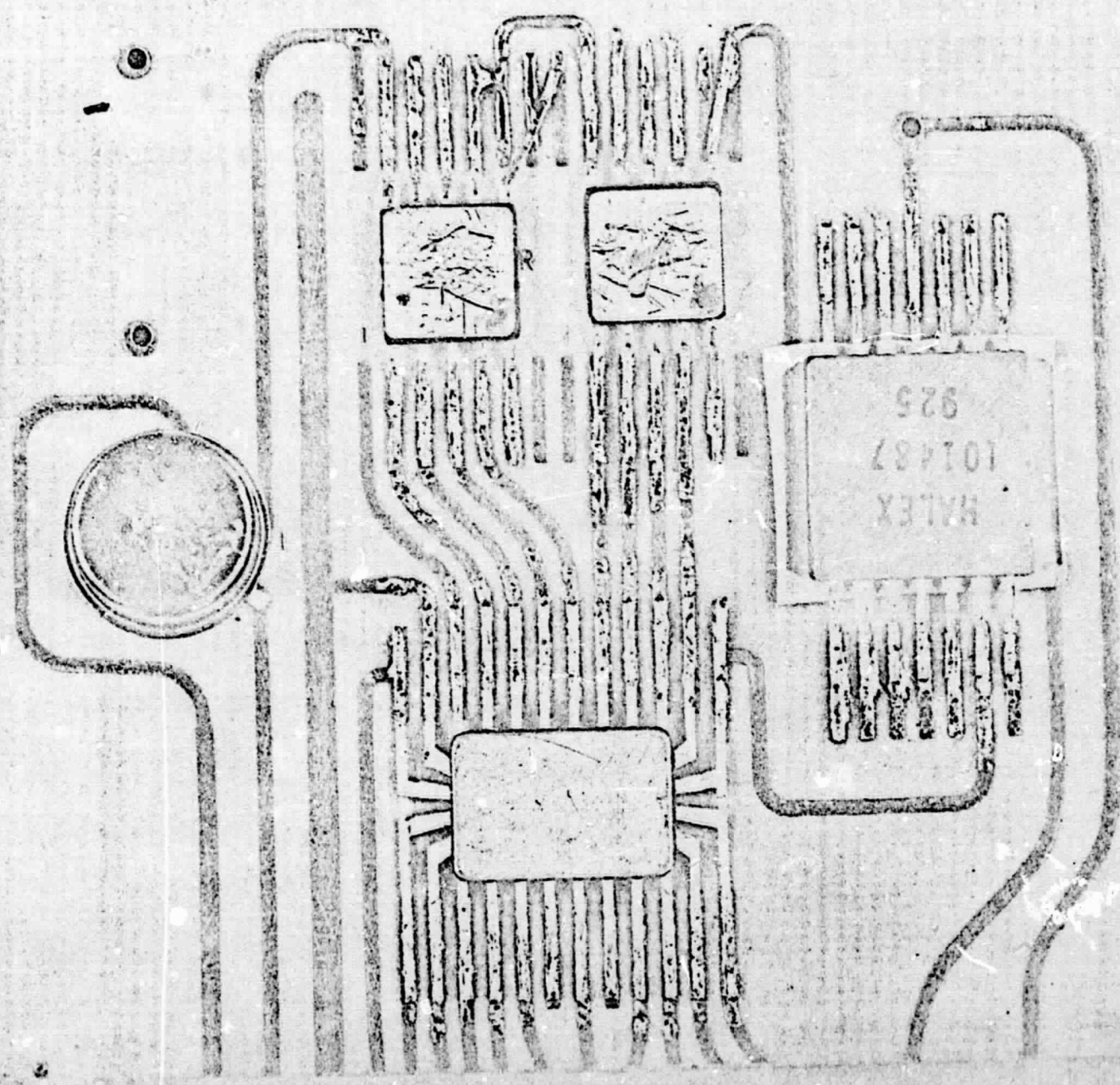

FIGURE 3