JPL CONTRACT 952592
(SUBCONTRACT UNDER
NASA CONTRACT NAS7-100)

SECTION II

INTERIM TECHNICAL REPORT

CUSTOM METALLIZED MULTIGATE ARRAY

FOR

CALIFORNIA INSTITUTE OF TECHNOLOGY
JET PROPULSION LABORATORY
4800 OAK GROVE DRIVE
PASADENA, CALIFORNIA 91103

JANUARY 26, 1970

RADIATION INCORPORATED
MICROELECTRONICS DIVISION
MELBOURNE, FLORIDA

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This work was performed for the Jet Propulsion Laboratory, California Institute of Technology, as sponsored by the National Aeronautics and Space Administration under Contract NAS7-100.

RADIATION INCORPORATED
Microelectronics Division
Melbourne, Florida

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APPENDICES

Appendix I References

1.0 INTRODUCTION AND SUMMARY

This report covers the Phase I study of alternate reliability concepts for a Custom Metallized Multi-gate Array (CMMA). Since the 10-year lifetime goals for the product make conventional screening and burn-in procedures unacceptable, unconventional avenues must be explored.

The study included a literature search to prevent redundant or useless effort. Most of the useful material was supplied by JPL. Findings from the literature search were analyzed for usefulness to this program and process. Brainstorming sessions with device and circuit engineering were held to uncover and screen any new ideas.

Those concepts deemed most useful or worthy of further investigation are detailed in section 2.3. The basic idea is to use test patterns as process quality evaluation tools. These patterns used in conjunction with revised inspection procedures seem to offer adequate means to accomplish the goals.

2.0 STUDY FINDINGS AND RESULTS

The Reliability study findings and results are documented in three sections; 1) Standard Product Assurance; 2) Additions to Standard Product Assurance; 3) Reliability Control Plan unique to CMMA.

Sections 2.1 and 2.2 are not a required part of this phase but represent advance thinking.

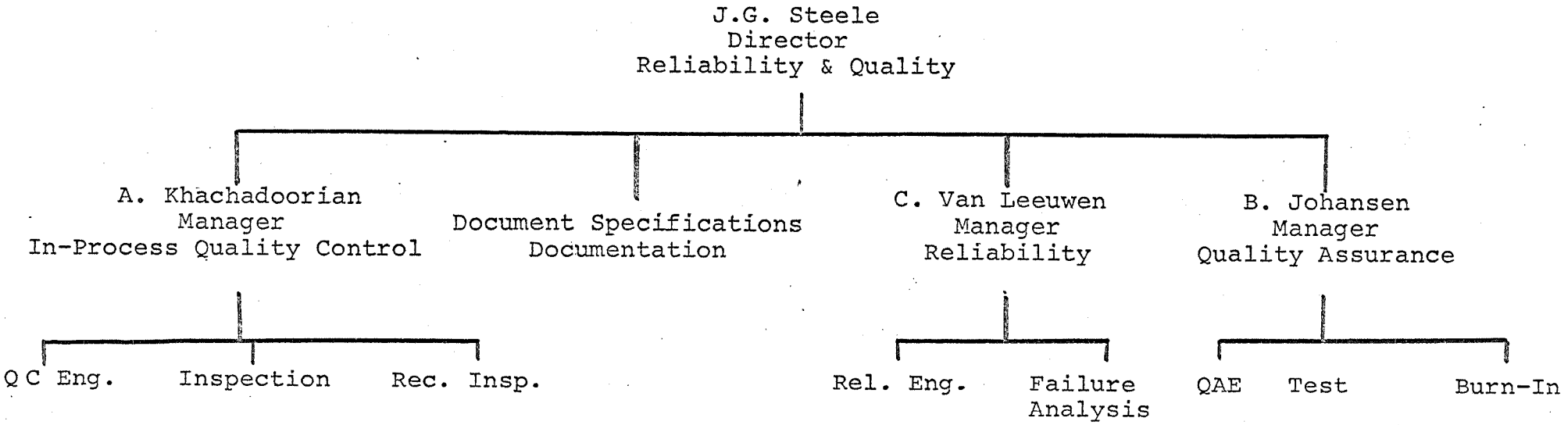
2.1 Standard Product Assurance Plan

2.1.1 Reliability and Quality Organization. The Reliability and Quality organization as shown in Figure 2.1-1 reports directly to the Vice President and General Manager of the Division. This concept assures a direct and unimpeded access to top management.

2.1.2 Design Review Participation

2.1.2.1 Review Definitions: The following reviews are defined in connection with the development of a new product:

a. Concept Review: This review examines basic concepts of design, outlines basic fabrication techniques and provides an estimate of design/fabrication costs as related to customer requirements.


J.G. Steele
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C. Van Leeuwen
Manager
Reliability
B. Johansen
Manager
Quality Assurance
Q C Eng.
Inspection
Rec. Insp.
Rel. Eng.
Failure
Analysis
QAE
Test
Burn-In

Figure 2.1-1

b. Design Review: This review examines detail aspects of the circuit and device designs and their relationship to customer requirements before commitment to actual circuit layout.

c. Layout Review: This review examines the layout composite to determine correctness, compatibility with processing area capabilities and potential reliability.

d. Test Review: This review examines wafer probe and final test requirements to insure proper preparation for these tests.

e. Life Test Review: This review examines life test results to verify new product reliability.

2.1.2.2 Reliability Engineering Participation: Reliability Engineering has the following responsibilities as concerns the foregoing reviews of new product.

a. Concept Review: Reliability Engineering uses this review to gain initial familiarization with proposed new product and is made aware of delivery schedules. This will generate a schedule for all proposed reliability support activities.

b. Design Review: Following this review a detailed plan of reliability evaluation is prepared, which includes details of evaluation of finished goods and discrete test vehicles and/or patterns. These in essence are designs, methods or devices which are expected to have a potential impact on reliability enabling ultimate evaluation.

c. Layout Review: Prior to this review, an extensive study is made by Reliability Engineering using an advance copy of the layout with layout rules. Reliability will sign off the proposed layout upon completion of the review.

d. Test Review: Reliability Engineering determines any special reliability testing procedures which may be required in preparation for this review.

e. Life Test Review: At this review, Reliability Engineering presents detailed results of life tests performed on the new product.

2.1.3 Failure Analysis: An extensive failure analysis policy procedure is used as an essential aid to effectively diagnose failed devices. These are generated as a result of reliability testing, in-house life testing, lot qualifications, field returns, etc. It also serves the purpose of analyzing fallout at the various processing steps, e.g. pre and post burn-in, wafer sort, etc. to improve yields.

2.1.4 Process Quality Control: The purpose is to establish and maintain effective controls for monitoring manufacturing processes and equipments, to provide rapid feedback of information concerning the state of control and to initiate, design, and develop statistical controlled experiments to further improve quality and reliability.

2.1.4.1 Responsibility: The primary responsibility of Process Quality Control Department is to establish and maintain effective controls for monitoring manufacturing processes and equipments, to provide rapid feedback of information concerning the state of control and to initiate, design and develop statistical controlled experiments to further improve reliability and quality. The Department's responsibility is to communicate the status of process controls to the Reliability Department, Quality Assurance, Program Management, Engineering and Manufacturing. During each critical manufacturing operation, the Process Quality Control Department monitors processes and product quality by means of random sampling of product at specified frequencies. Process Control Charts are maintained on processes and workmanship characteristics during all phases of manufacturing. The inspection results which indicate process status are posted at all critical production stations for immediate feedback of information to the foreman and operator. Out of control situations result in immediate line stoppage until corrective action is implemented and/or other quality ruling established. Summary reports are issued periodically on information concerning trends and defect levels.

Process Audits are performed to verify conformance of operating procedures. These audit reports review all manufacturing and quality control procedures on a random unannounced basis. Discrepant items are corrected and are formally documented by means of a Request for Corrective Action (RCA) procedure. Failure to respond to audit reports results in immediate shut-down and loss of Line Qualification.

2.1.4.2 Process Flow: At designated intermediate steps of the manufacturing process, in-line evaluations are performed on a sample or 100 per cent basis in accordance with operator instructions or quality specifications. These evaluations include measurements of electrical and physical parameters. The economic and quality considerations for in-line evaluation and control are to detect and report when any manufacturing operation is not in control, to detect and remove units which do not comply with workmanship quality standards and to remove units whose electrical characteristics indicate a low probability of passing final product electrical parameter specifications.

2.1.4.3 Process Control Data: Process Control Data is recorded on an attribute or variable basis as required and P-Charts or $\bar{X}R$ Charts are maintained daily. The rapid feedback of information concerning process yield

fluctuations provided by this technique and strengthened by the weekly highlight reports supports a valuable aid to insure that out-of-control processes are quickly identified and brought back into control.

2.1.4.4 Inspection:

2.1.4.4.1 Quality Control inspectors assigned to manufacturing lines perform sample testing and inspection of product to verify product quality, and in addition, monitor process conditions and equipment settings against specified operating instructions.

a. Typical examples of process control consists of sampling electrical tests or physical examination of units at a specified processing stage, examination of sample units after welding operations, radiographic examination of the internal construction and measured values of device geometries.

2.1.4.4.2 The sample inspections and the acceptance criteria used by Quality Control inspectors are defined and documented in quality specifications applicable to the manufacturing line or area.

a. Operating instructions applicable to the manufacturing line are used by manufacturing personnel as the working documents at each operation. These operating instructions are frequently reviewed and audited against formal specifications for compliance.

b. When a sample, taken by the inspector, fails or when he observes a process condition that is contrary to the Operating Instructions, the inspector notifies the manufacturing foreman and the quality engineer. This procedure requires the issuance of a Request for Corrective Action to initiate appropriate corrective action.

c. The results obtained from the Process Quality Control inspections are recorded on Quality Control Audit Reports and sent to the quality engineer for evaluation and appropriate corrective action. At stations designated by the Quality Control Specifications, control charts are prepared and maintained from data obtained either from in-line evaluation stations. The charts either comprise of attribute or variables control charts.

d. In some cases, material which has been rejected at in-line evaluation stations is reworked to produce acceptable product providing rework or reinspection is non-destructive. The standard procedure is for Quality Control to return the devices with a Discrepant Material Report to Manufacturing requesting a 100 per cent rework or reinspection. After reworking, the devices are inspected at the Process Control station at which they were rejected previously. If found acceptable, the units are then processed through the remaining manufacturing operations. Product again failing to meet requirements is returned to Manufacturing with a new Defective

Material Report, indicating the number of units returned and the cause for rejection.

2.1.4.5 Traceability: Lot identity is maintained from diffusion through all manufacturing and testing stages. Lot identity is marked externally on each finished device and is therefore traceable at any time from diffusion to shipment. Lot travelers move through the line with the product and provide traceability at all points in the operation.

2.1.4.6 Process Controls:

2.1.4.6.1 Material Product Control:

a. The material area is considered a proprietary area. This area receives and processes wafers prior to integrated circuit diffusion processing. Primary processing is oriented to the Radiation Incorporated proprietary dielectric isolation and other unique processes.

b. The processes controlled in this area consist of:

Epitaxy

Resist Removal

Moat Etch

Oxide Strip

Poly Thickness

Oxide Integrity

c. Data obtained from inspections associated with these foregoing processes is recorded on $\bar{X}R$ charts. In addition, weekly reports are published stating the total wafers

submitted for inspections, number of wafers sampled, total number of lots rejected and a total of each reject category. These reports are distributed to both Manufacturing and Quality management.

2.1.4.6.2 Wafer Fabrication Control:

a. The Wafer Fabrication area is considered a proprietary area. Dielectrically isolated wafers are processed in this area through masking, diffusion and thin film steps.

b. Quality inspections in this area consist of:

Diffusion encompassing:

Visual

Resistivity

Junction Depth, as monitored by means of angle lap, staining and/or plating using $\bar{X}R$ chart monitor recording techniques. This also includes monitoring of spectrographic analysis of all dopant substances in terms of contamination with potentially mobile ions.

Photo Chemistry encompassing:

Visual

Geometry Measurements

This also includes monitoring of photo resist control in terms of controlled viscosity, particle contamination and shelf life.

Thin Film encompassing:

Visual

Film Thickness Measurements

Resistivity

Passivation encompassing

Thickness Control

c. Data obtained from the above inspections is recorded on $\bar{X}R$ Charts or P Charts. Weekly reports are issued to management stating the total number of wafers submitted at each inspection point, number rejected, and the total for each reject category.

2.1.4.6.3 Assembly: The processes controlled in this area are:

a. Dice Inspection: Following 100 per cent inspection by Manufacturing, Quality Control sample inspects each dice lot to MIL-STD-883, Method 2010 criteria with data being maintained on both run folders and P Charts. In addition, all reject dice are recorded by failure mechanism as shown on the back of each P Chart.

b. Package Inspection: Following 100 per cent manufacturing inspection, Quality Control sample inspects each package lot for visual defects. This inspection is in addition to the Quality Receiving inspection where all lots are sample inspected to both visual and electromechanical criteria as specified by the respective procurement specifications. Data obtained from this inspection is recorded on P Charts and the Weekly Summary Report. In addition, lot qualification procedures call for a complete environmental package qualification.

c. Die Mount Inspection: This is a continuous inspection of the die mount operation per MIL-STD-883. Visual inspection is performed hourly on each die mounting machine with data being maintained on both P Charts and the Weekly Summary Report. All rejects are categorized according to failure mechanism as shown on the back of each P Chart. In addition, periodic samples are subjected during each shift to an X-Ray examination. In case the sample fails this examination, all product die attached during the last acceptable sample is screened by Manufacturing through 100 per cent X-Ray.

d. Wire Bond Inspection: This is a continuous inspection to MIL-STD-883 visual inspection complemented by a periodic wire pull test during each shift with the visual inspection results being maintained on P Charts and the wire pull test results maintained on $\bar{X}R$ Charts. All visual rejects are categorized by failure mechanism on the back of each P Chart, Visual inspection results are also reported on the Weekly Summary Report.

e. Pre-Seal Inspection: This is a lot by lot visual inspection to MIL-STD-883 criteria. Inspection results are maintained on P Charts with all rejects being categorized according to the failure mechanism on back of each P Chart. Inspection results are also reported on the Weekly Summary Report.

f. Seal Inspection: Continuous monitoring of the sealing operation is performed by inspecting each sample visually for the following defects:

Seal

Misalignment of parts

Plating

Lead frame damage

Package damage

In addition to visual inspection, a sample of units is taken periodically during each shift and subjected to the Fine Leak Test. Test results are maintained on P Charts and summarized on the Weekly Summary Report.

g. Final Inspection: Lot by lot visual inspection to the seal inspection criteria and the package visual inspection criteria. Inspection results are maintained on P Charts and summarized on the Weekly Summary Report.

2.1.4.7 Environmental Monitoring: Environmental monitoring is performed by In-Process Quality Control and consists of:

a. Deionized Water Resistivity Monitor - This check is performed once per shift.

b. Deionized Water Silica Content Monitor - A warning is given whenever Silica content reads greater than specified and a shut-down will result when it reads greater than 2 x the specified limit. This function is performed twice weekly.

c. Deionized Water Bacteria Level Monitor - This monitoring is performed once a week.

d. Monitoring of Room Temperature, Room Humidity, Coating Operation Temperature, and Coating Operation Humidity with particular attention to cooling slices down to ambient temperature.

e. Deionized Water PH Monitoring - This monitoring is performed once per shift.

f. Particle Count, Airborne, Monitor - This monitoring is performed twice weekly.

g. Monitoring of the dryness control over all gases used in oxidation steps, with particular attention being paid to the nitrogen used in oxide densification steps.

2.1.5 Incoming Material Control

2.1.5.1 Purpose: The purpose of this section is to evaluate incoming material to meet appropriate quality standards and specifications and to implement effective controls to assure that defective material is not used. To continuously receive acceptable incoming material, a program of vendor selection and appraisal with vendor corrective action for unsatisfactory performance is instituted.

A representative sample of each incoming shipment is inspected to the specifications for that material by the Vendor Quality Control and Receiving Inspection personnel. Depending on the material, the specifications may call for inspection of physical, dimensional, electrical,

analytical, or environmental characteristics.

An Inspection Plan is prepared for each type of material by the Quality Engineer for use by inspection personnel. This information indicates the criticality of the parameters to be inspected and specifies sample sizes and acceptance criteria for each material. The selection of sampling plans is based on the relative importance of specific parameters in the manufacture of the product and the cost to perform the evaluation. Generally, MIL-STD-105D is invoked on all lot submissions.

2.1.5.2 Flow of Materials:

2.1.5.2.1 Each shipment is held in the receiving area pending satisfactory completion of all the specified evaluations on a first-in-first-out inventory basis. When a material lot is rejected, a Vendor Corrective Action Report is prepared showing the results of the inspection. A red "stop" identification sticker, initialed and dated, is attached to each container holding the rejected material. The lot is then transferred to the stockroom area and held in a rejected material inventory pending notification of the vendor by Purchasing and subsequent return of the material to the vendor or screening of the lot at the vendor's expense.

The acceptance of non-conforming material for use in the manufacturing line requires the approval of the Quality

Control Department and the pertinent Product Department. The procedures for evaluation of non-conforming material manufactured within the plant are the same as for material purchased from a vendor except that a Material Rejection Notice is prepared when a lot is rejected in plant.

2.1.5.2.2 Identification stickers are attached to: a) accepted material, b) material awaiting analytical or environmental evaluation, and c) material upon rejection. Stickers attached to accepted and rejected material are initialed and dated by the inspector. Accepted material may then be transferred to the stockroom. Rejected material is held in a segregated inventory under the control of Vendor Quality Control pending MRB action or return to vendor.

Lot identity is maintained for certain critical material in the stockroom and through designated steps of processing. Photomasks from the Radiation Incorporated mask-making facility are inspected on a sample basis to Quality Control. The acceptance testing criteria includes the aspect of damage caused by usage on previous product. Every lot of masks is sampled to a 1 per cent AQL for visual defects and to a 2.5 per cent AQL for dimensional measurements. The dimensional inspections are made at 400X magnification. Visual defect inspections are made at 50X magnification employing back lighting for such defects as scratches, emulsion flaws, foreign material, opaqueness and edge definition.

2.2 Additions to Standard Product Assurance Plan

This section covers proposed additions to the Standard Product Assurance Plan which are proposed for, but not necessarily unique to, the JPL Phase II and III efforts. In general, these additions are necessitated by the LSI construction of the CMMA; as such, they apply to other LSI device types now under development by Radiation Inc. The majority of these additions are now under consideration by Radiation Inc. as a part of various LSI development programs now in progress. Topics covered in this section are grouped roughly by process step as follows:

a) Materials

b) Masks

c) Oxidation

d) Diffusion

e) Thin Film

f) Isolation Oxide

g) Assembly and Packaging

2.2.1 Materials

2.2.1.1 Additional controls on epitaxial layer thickness will be developed using pilot slice evaluation techniques. This technique will also provide close control over epi resistivity. The procedure consists of running pilot slices at critical spots in the epi reactor and then evaluating these pilot slices for the needed parameters.

2.2.2 Masks

2.2.2.1 In the area of masking techniques, a "double exposure" technique is expected to be a virtual necessity. Two techniques have been used for this purpose:

a) A masking procedure consisting of aligning and exposing the mask and slice, moving the mask over one circuit pattern and repeating the procedure. If a flaw exists in the mask, the probability of the same flaw existing in the same area on the next circuit pattern is practically nil. Hence, the double exposure will eliminate potential oxide pinholes.

b) A procedure which repeats photoresist application following the first masking/exposing operation and then masks/exposes the second photoresist layer using a second mask. This technique provides additional assurance against pinholes but requires an extra photoresist operation.

2.2.2.2 An improvement in mask inspection technique is afforded by the use of an optical microdensitometer. This instrument provides a quantitative measure of opagueness, edge acuity, stepping tolerances and line widths. In addition, optical comparison techniques have been proposed which inspect a mask by comparison to an extensively inspected, known good mask.

2.2.2.3 A technique which has been considered but which will not be attempted is electronic scanning of masks by TV camera. The resulting video signal is then processed through pattern recognition techniques. This technique could possibly eliminate such simple mask defects as voids and contamination. The requirements in terms of equipment are beyond the scope of the JPL Phase II and III programs.

2.2.3 Oxidation

2.2.3.1 Periodic qualification of chemicals, glassware, handling procedures and oxidation furnace tubes in terms of freedom of ionic contamination is considered essential to high-yield LSI processing. This qualification procedure will be implemented by running pilot silicon slices through the various processing steps and obtaining a measure of oxide stability through MOS C-V analysis.[14,18,19] Oxide stability will then be a direct indicator of mobile ion contamination level.

2.2.3.2 Control over purity, contamination level and dryness of gases used in oxidation steps by C-V methods similar to those outlined above.[19]

2.2.3.3 Control over oxide stability of individual runs by sampling in terms of C-V response of the oxide. This step can be implemented by MOS analysis of the product or pilot slices and will give a quantitative measure

of oxide contamination level.[13]

2.2.3.4 Controls over oxide step by sampling inspection of slices using a scanning electron microscope. Correlation studies are proposed for the Phase II and III efforts to provide an effective inspection procedure and possible processes for altering oxide step profiles by suitable etching steps.

2.2.4 Diffusion

2.2.4.1 Additional visual inspection criteria will be generated to provide adequate inspection of LSI circuitry in terms of diffusion spacings, tolerances and other criteria influenced by high density design.

2.2.5 Thin Film

2.2.5.1 Improved controls over aluminum film thickness are required to provide assurance against electromigration effects.[3,5] This control is particularly critical in avoiding excessive thinning of metallization at oxide steps. Proposed is further development of a technique of controlling the total amount of metal deposited by control of the total mass of metal introduced into the evaporator source.

2.2.5.2 Additional visual inspection criteria will be required to cover the second level metallization. Some of the criteria which will be developed to include poor edge

definition, shorts and opens, voids, scratches, via contact alignment, incomplete alloying and metal undercutting. Again, it is the intent to use a scanning electron microscope to inspect slices on a sample basis where feasible. In the event a 100% probe testing of gate cells is implemented, visual inspection criteria will be generated defining acceptable limits of probe damage.

2.2.6 Isolation Oxide

2.2.6.1 A control over isolation oxide thickness will be required to provide adequate oxide between first and second level metals.[11,12]

2.2.6.2 Additional visual inspection criteria will be generated to enable proper inspection after isolation oxide aperture etch. These criteria will define such items as incomplete oxide removal in vias, oxide cracking, pinholes and other oxide flaws, undercutting, contamination and alignment. The development of advanced inspection methods are proposed, such as infrared scanning to detect pinholes, cracks and voids, which are expected to have a major impact on yield at this level. Similar criteria will be generated to enable inspection of the passivation oxide layer.

2.2.7 Assembly and Packaging

2.2.7.1 The package for the CMMA is not defined at the present.

Depending on the final package and the die attach method to be used, a method will be developed which will enable inspection of die attach integrity. In the case of the aluminum/germanium die attach used by Radiation Inc. in previous radiation resistant packages, an X-Ray inspection will not show up the die attach since the constituents of the Al/Ge alloy are radiographically transparent. Proposed areas of evaluation will include fillet inspection at the edge of the die to detect incomplete wetting; infrared scanning techniques to detect hot spots caused by incomplete die attach on account of voids. Gold die attach will be evaluated using conventional X-ray techniques.

2.2.7.2 A problem which applies to all visual inspection of high complexity dice is that of operator fatigue. Procedures for systematic scanning of dice, slices and masks will be developed which are expected to minimize this problem. This item will also become part of the Training and Motivation proposal which is scheduled for Phase II.

2.2.7.3 A preseal vacuum bake to enhance device stability will be investigated.

2.2.7.4 An equipment manufactured by the Navan division of North American Rockwell has been procured by Radiation

Inc. This equipment will perform 100% nondestructive bond pull testing. Development of operating procedures for this tester will take place during Phase II of the JPL program.

2.2.7.5 A bonder operator qualification program, similar to those currently employed on several hi-rel programs, will be instituted on the JPL program and extended to all other LSI efforts now under development.

2.2.7.6 A "closed loop" bonding system is now under development by Radiation Inc. This system is a departure from the usual ultrasonic bonding apparatus in that the total energy applied to each bond is kept constant irrespective of the amount of friction between bonding wire, metallization and bonding tip. This bonding system will be further developed concurrent with the Phase II and III efforts.

2.2.7.7 In conjunction with the development during Phase II of revised preseal visual inspection criteria to cover the package used, correlation studies are proposed to correlate bond wire deformation to other bond characteristics.[1]

2.2.7.8 The possibility of 100% inspections by Quality Control at dice inspection and pre-seal visual inspection will be investigated. The present procedure consists of a

100% inspection by Manufacturing followed by a sampling QC inspector.

2.3 Reliability Control Plan Unique to CMMA Design

2.3.1 Introduction

The problem of predicting and demonstrating low failure rates on LSI devices is a formidable one indeed. In a program such as this, the economics and time required to demonstrate the low failure rates required dictate that the classical approach to reliability demonstration is impractical and prohibitive. As a result, an approach which calls for the design and use of test vehicles was chosen.

The idea of using test vehicles as aids in controlling and predicting reliability is not a new concept.[15,17,22] It is felt that the use of test vehicles will enable the correlation of reliability to process variations such that product capable of meeting the reliability goals of this program can be produced and screened. In general, the approach is one of using test vehicles as tools to control and indicate (or screen) those failure mechanisms which are considered most pertinent to this product. It should be noted that the series of test vehicles and the various methods of evaluation mentioned in the balance of this report are proposals and require additional evaluation before being implemented into a hardware program. Extensive evaluation of all vehicles described is planned during Phase II, with the objective of arriving at a test vehicle which takes a minimum of space and provides all necessary

information. Additionally, the Phase II effort will determine information needed to insure long-term CMMA stability and also the distribution of test vehicles/ elements over the slice.

2.3.2 Definitions

For the purposes of this report, the following definitions apply:

Test Vehicle - A test vehicle is defined as a die identical in size to a standard CMMA die which consists of test elements and test circuits. The test vehicles will be strategically located on each and every wafer and will be processed in an identical fashion as the standard CMMA circuits.

Test Elements - A test element is defined as a structure designed into the test vehicle which enables specific physical and electrical process oriented properties of the structure to be easily monitored so that they can be used to provide information about specific potential failure mechanisms. A key concept is that of true acceleration; the test elements to be used in the CMMA program will be specifically designed to accelerate the failure mode which they are designed to detect. This concept is basic to the philosophy of highly accelerated testing of test elements and will be covered at length for each pertinent failure mode in the balance of this section.

Test Circuits - A test circuit is defined as a structure

designed into the test vehicle which will allow the electrical characteristics of both the Driver Gate and Standard Gate to be easily monitored. It should be noted, however, that in contrast to the test elements as defined above these structures are not designed to accelerate basic failure modes. Rather, they are exact duplicates of the driver and standard gates and are designed to provide long-term and/or high stress testing data on the individual gate cell.

2.3.3 Applications

The test vehicles defined above will be used for four major purposes in assuring long-term stability of the CMMA:

a) Process Verification

b) In-Process Quality Control

c) 100% Screening

d) Life Test/Longevity/Environmental Evaluations

Listing of Proposed Test Elements

a) Metallization Crossover Test Element

b) Surface Conductivity Test Element

c) Electromigration Test Element

d) Via Contact Test Element

e) Control NPN Transistor

f) Emitter-Base Field Plate NPN Transistor

g) Emitter-Base and Collector-Base Field Plate NPN transistor

h) MOS Capacitor

2.3.3.1 Process Verification

The emphasis on this category will be on the use of test elements to investigate a series of processing tradeoffs affecting reliability. These will be determined by high-stress testing of the applicable test elements; this will enable timely decisions to be made regarding tradeoffs. Discussed below are the principal tradeoffs, the specific test elements designed to investigate them and the proposed test methods to be employed in the Phase II and III evaluations.

2.3.3.1.1 Isolation Oxide For Two-Layer Metallization

This oxide layer is critical from a yield-reliability viewpoint. Pinholes, oxide flaws, cracks and ion migration in the oxide are generally expected to be significant failure modes. The oxide thickness is an important parameter; a minimum thickness is required for adequate dielectric integrity between metallization layers, with a maximum being imposed by constraints on the oxide step height/metallization thickness ratio. Specific test elements to be used here include the following:

a) A metallization crossover test element to be used in oxide integrity studies. This test element consists of a series of multiple crossovers generated by a pattern

of each metallization layer at right angles to each other. It should be noted that this test element has already been used successfully in our earlier 2-layer metallization development work. This element enables measurement of oxide conductivity, incidence of pinholes and ultimate dielectric strength. Stresses which will be used in testing include high-temperature voltage step stress and constant-voltage, high-temperature long term testing. The element will be used initially to evaluate various permutations in the 2-layer interconnect process. It is anticipated that the present test element will not be used in the final test vehicle because of its complexity and large size. The final test element is visualized as a capacitor-like structure of small geometry.

b) A surface conductivity test element to be used in measuring this parameter directly. This element consists of two adjacent, interlocking "comb" type metallizations with required bonding pads and will be used to study single interface effects. Elements will be located at the interface of thermally grown oxide/isolation oxide and on top of the final passivation oxide (oxide/package ambient interface). These structures will allow measurement of surface conductivity, migration of surface ions, surface breakdown potential and the effects of temperature on these parameters. Again, stress methods will consist of combinations of temperature and voltage, with electrical

measurements being made both at ambient and elevated temperatures.

2.3.3.1.2 Metallization Thickness

This parameter is constrained by considerations of metal step height and electromigration susceptibility. Basically, electromigration is a phenomenon in which transport of mass in metals takes place when metals are stressed at high current densities. It has been found that at high current densities the rate of momentum exchange between conducting electrons and the metal (aluminum) ions is large enough to exert a force on the ions in the direction of electron flow.[2,5] This action creates vacancies at the negative end of a conductor and whiskers/hillocks at the positive end. Eventually sufficient vacancies are formed to create a void across the aluminum conductor resulting in an open circuit or intermittent condition. For long thin aluminum stripes, J. R. Black[5] of Motorola has established a relationship between MTBF, current density, and temperature. The equation is of the form

$$\frac{1}{MTBF} = A J^2 \exp(-\phi/kT)$$

where

MTBF = mean time between failure (hours)

A = constant involving cross sectional area and other physical properties

J = current density (amps/cm^2)

ϕ = activation energy (electron-volts)

k = Boltzman's constant

T = temperature (degrees Kelvin)

The value of ϕ (activation energy) was found to vary from .48 electron-volts to 1.2 electron-volts because of differences in the structure of the aluminum film. The aluminum films used in the fabrication of the CMMA will be well ordered, large grained aluminum films and therefore will have activation energies in the range of .84 electron-volts to 1.2 electron-volts. Using a current density of 10^5 amps/cm^2 as a design maximum, the work of Black shows that MTBF's far in excess of 10 years are to be expected at an ambient of +125^{o}C. Since the CMMA will be operating at much lower temperatures than this, it is the opinion that the 10^5 amp/cm^2 design maximum is very conservative. Since the work of Black was performed on long thin aluminum stripes, the equation for MTBF is optimistic because it does not take into consideration the effect of aluminum over oxide steps. It has been shown that considerable reduction in cross sectional area can take place at oxide steps if the relationship of oxide thickness to aluminum thickness is not properly controlled. Figure 2.3-1 shows this relationship. Since the design goal for the 2-layer metallization system is to have a 1.2 to 1.3 ratio of aluminum thickness to oxide thickness,[29] reduction of lifetime due to electromigration of aluminum at oxide steps is, therefore, not considered a problem.

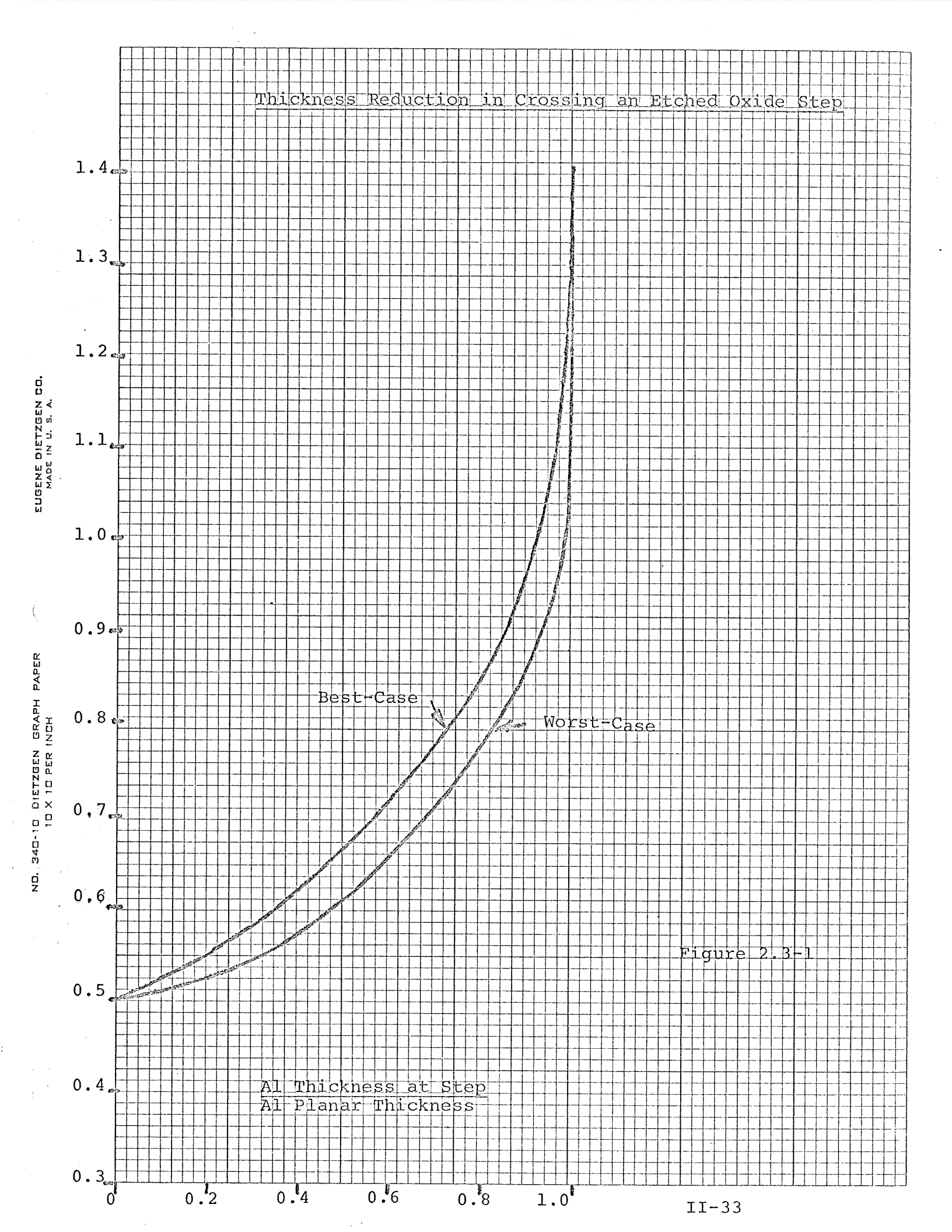

Thickness Reduction in Crossing an Etched Oxide Step
1.4
1.3
1.2
1.1
1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0
0.2
0.4
0.6
0.8
1.0
Best-Case
Worst-Case
Al Thickness at Step
Al Planar Thickness
EUGENE DIETZGEN CO.
MADE IN U. S. A.
NO. 340-10 DIETZGEN GRAPH PAPER
10 X 10 PER INCH

Figure 2.3-1

A sample calculation for worst-case MTBF for the CMMA is shown below;

Assume worst-case parameters: $T_a = +125^{\circ}C$

$P_d = 88$ mW

$\Theta_{ja} = 90^{\circ}C/watt$

Hence, $T_j = T_a + P_d \cdot \Theta_{ja} = 125^{\circ}C + (.088)\ (90) = 133^{\circ}C = 406^{\circ}K$

Using expression by J. R. Black[5] for MTBF by electromigration

$$MTBF = \frac{A \exp\ (\phi/kT)}{K\ J^2}$$

in which A = cross sectional area of conductor

ϕ = Activation energy

k = Boltzmann's constant

T = Temperature, $^{\circ}K$

K = constant

J = current density

and $A = 6.45 \times 10^{-7}$ cm^2 (2 mils x 50 u")

$\phi = 1.2$ eV

$k = 8.62 \times 10^{-5}$ $eV/^{\circ}K$

$T = 406^{\circ}K$

$K = 8.5 \times 10^{-10}$ for large crystallite, glassed Al films

$J = 5.8 \times 10^4$ A/cm^2

we obtain:

$$\text{MTBF} = \frac{(6.45 \times 10^{-7})\ (e^{1.2/8.62 \times 10^{-5} \times 4.06 \times 10^{2}})}{(8.5 \times 10^{-10})\ 33.5 \times 10^{8}}$$

or MTBF = 13×10^{7} hours = $\underline{1.5 \times 10^{4}\ \text{years}}$

Note this represents a worst-case temperature of +125°C. The CMMA is expected to remain at a maximum temperature of + 25°C during the 10 - year mission, which will result in several orders of magnitude improvement in MTBF.

The following test elements will be investigated during the Phase II effort to provide experimental verification of the above conclusion.

a) Narrow Al interconnect stripes at both first and second level metal. This is the classical electromigration study element which has been used by most investigators in the field.[5] The main area of interest is the effects of external factors such as SiO_2 over-coat/dielectric layers and proximity of Si/Al contacts on the mass transport rate in these conductors. They are intended to be stressed using a current/temperature combination and will be analyzed by the extensive use of the scanning electron microscope.

b) A dual purpose test element consisting of a metal run over oxide steps and through contact apertures

between metallization layers (via contacts). This element will explore the electromigration aspects of worst-case metallization situations over oxide steps, as well as via contact-related usage which will be expanded upon later. The worst-case oxide step exists at the point where the isolation oxide passes over a step in the first-layer metallization. The test element described will contain this worst-case situation. Again, a temperature/current stress will be used in evaluating this element, with emphasis being placed on SEM analysis of rejects.

2.3.3.1.3 Via Resistance

The process used to form reliable, low resistance via contacts will be the subject of process sensitivity studies during Phase II. Some of the factors entering into this process include via size, via etch procedures, metallurgical considerations at the Al/Al interface and contact alloying procedures. The test element used for this will consist of a metallization pattern on alternate layers running through a series of via contacts. This structure is also used for oxide step investigations (see above). A temperature/current stress will be used to accelerate possible failure mechanisms.

2.3.3.1.4 Surface Stability

The long-term stability requirements on the CMMA

necessitate that particular attention be paid to the production of a stable surface system. The process for the CMMA is specifically designed to minimize the effects of surface instability on device/circuit characteristics. The purpose of the added process steps proposed is to enhance the acceptor impurity concentration at the surface of the base region and the regions between adjacent collectors. In addition, test elements will be used to investigate the effects of phosphorus doping in the various layers of the SiO_2 system. An extensive series of test elements is outlined below, together with their applicable testing methods and the surface-related parameters they are designed to measure. In many cases the element will also be investigated for possible use in new in-process control steps.

a) Control NPN transistor. This device is a standard geometry NPN transistor as used in the gate cells. Its purpose is to provide a control device to be used with the field-plate transistors outlined below.

b) NPN transistor with emitter-base field plate. This device is designed to determine the susceptibility of the emitter-base junction to surface-induced inversion problems. The Al "field plate" electrode covers a large area of the emitter-base periphery. By varying the potential on this electrode the surface potential field can be locally varied and a measure of the extent can be measured of resistance to inversion. This test

element will be used to investigate process variations and for electrical measurements after High Temperature Reverse Bias stressing of the device.

c) NPN transistor with field plate over both emitter-base and collector-base junctions. This device will be used in a manner analogous to the NPN transistor discussed above. The field plate will enable measurement of inversion tendencies of both device junctions.

d) MOS Capacitor. From an In-Process Quality Control viewpoint, this is the most important test element in so far as surface stability is concerned. This element will provide Capacitance-Voltage (C-V) plots which in turn provide a comprehensive measure of oxide stability. The MOS capacitor will provide quantitative evaluations of the effects of metallization and oxide depositions by use in pilot slices run ahead of product. Following deposition, the capacitors will be analyzed using C-V response techniques and hot-stage drift screens using a temperature/voltage stress combination. This test element will also be used in all long-term stability evaluations.

2.3.3.2 In-Process Quality Control

Test elements will be used to implement an IPQC control which will be unique to the JPL program within Radiation Inc. This section will discuss the applications and process steps which will be investigated during the Phase II effort. Process categories covered are:

a) Oxidation

b) Thin Film

c) Isolation Oxide

2.3.3.2.1 Oxidation

As discussed before, all oxidation steps will be very closely controlled because of their major impact on device stability. In general, oxides will be evaluated using gold ball probe MOS capacitor techniques at all steps before metallization and by C-V analysis of the MOS capacitor after metallization steps. Test elements will be used in qualifying each slice at various steps in the process. MOS capacitors will also be fabricated on pilot slices in order to characterize all apparatus used for oxidation in terms of mobile ion contamination.

2.3.3.2.2 Thin Film

Deposition of aluminum layers frequently introduces uncontrolled mobile ion contamination into the Al/SiO_2 system.

The C-V analysis of the MOS capacitor test vehicles will provide a sensitive indicator of this type of contamination. In addition, the use of metallization test vehicles such as the via contact series and narrow interconnect types to provide information about metal coverage at oxide steps will be investigated. This test element will also provide an in-process control

on via resistance and silicon-aluminum contact resistance. The use of a scanning electron microscope as an in-process sampling visual inspection tool will be investigated in connection with the metallization test elements discussed above.

2.3.3.2.3 Isolation Oxide

Both the proposed cross-over test element and surface conductivity elements will be investigated for use in in-process control procedures. These two elements will provide data on oxide conductivity, incidence of pinholes, ion migration and surface conductivity.

2.3.3.3 100% Screening

Test element-oriented evaluation techniques will be used extensively in 100% Hi-Rel processing of CMMA product. During the Phase II development work procedures as outlined below will determine feasibility and usefulness of this approach.

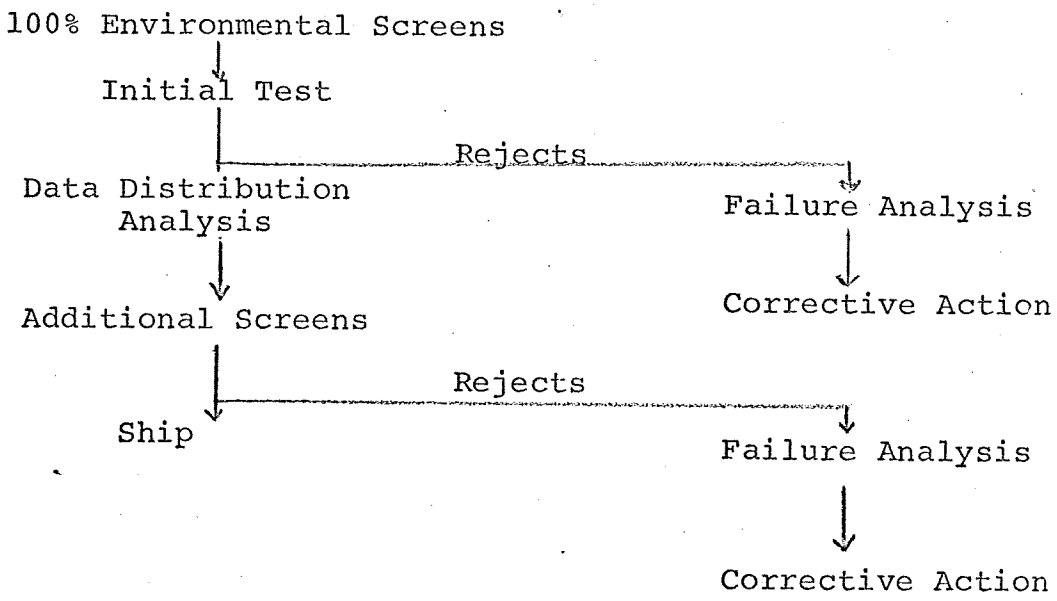
2.3.3.3.1 Test Vehicle Oriented Screens

It is proposed that the test vehicles from each slice be assembled and subjected to highly accelerated drift screening in order to determine if the use of these test vehicles as in-process control tools has really been successful. In addition, the results of this drift screening will also allow the product under test to be compared to the results of the experimentation

outlined in the Process Verification section 2.3.3.1. The drift screening conditions will be derived from results of the Product Improvement section. In this way, the expected performance of the product of these slices/runs can be projected on these particular failure mechanisms which were investigated. - It should be pointed out that the use of drift screening of test vehicles is not in itself a complete screen. It is intended to csmplement and in some cases dictate the screens to be used on the finished CMMA. Note also that these screens are aimed at providing sufficient sensitivity to expose and identify failure mechanisms which are considered to be of prime importance at this time. In addition, these screens are aimed at weeding out failure mechanisms associated with the die. Failure analysis will be performed on failed devices in order that corrective action can be implemented back into the process line. In addition to performing the above screens on test vehicles, it is proposed to test all vehicles of a diffusion run and to compile distributions of the data acquired. In so doing the data may provide information about potential anomalies. Units which appear to be abnormal will be failure analyzed in order to determine the underlying cause. This information will be fed back into the process area for corrective action.

2.3.3.3.2 CMMA Product Screens

The proposed sequence of screening is outlined below. It should be noted that these screens are an adaptation of standard hi-rel processing currently being performed at Radiation Inc.



In order to determine what 100% environmental screens to implement, a complete evaluation of the final CMMA package is proposed. The intent here is to submit the package to an extensive qualification, determine the shortcomings of the package, if any, and then stress the package to failure using applicable techniques similar to those in MIL-STD-883. It should be noted that the CMMA package is not yet determined. The initial CMMA product will be packaged in an interim package and no qualification of this package will be attempted. All failures will be failure analyzed in

order that corrective action can be implemented.

All units which fail initial testing will be data-logged in order that failure modes can be identified. Sufficient failure analysis is proposed to determine the failure mechanism and cause in order that corrective action can be implemented. A statistically significant sample will then be selected from all electrically good units. The intent here is to perform a distributional analysis of the various parameters of the devices in order to determine if the distributions are normal or marginal in relationship to the existing limit specifications and to determine the existence of any outliers. An investigation into whether the outliers are reliability risks or not will be instituted.

The additional screens that will be recommended will be screens that will be determined by the results of the investigations of section 2.3.3.1 and the results of the test vehicle screens. The following items will be given consideration in the determination of these screens:

s) 100% burn-in

b) Delta cull post burn-in

c) The need of lot acceptance testing where a qualification similar to method T5005 of Mil-Std-883 is required.

Failure analysis will be performed on a sufficient amount of fallout to determine the major failure modes/mechanisms. This analysis will be of sufficient depth to determine the failure mechanism and associated cause so that corrective action can be implemented into the process.

2.3.3.4 Life Test/Longevity/Environmental Qualifications

The concept of generating failure distributions on a per failure mode/mechanism basis by the use of high-stress testing of test vehicles is proposed to provide correlation between test results and failure rate per failure mechanism. The actual generation of numerical failure rates, both for individual mechanisms and the CMMA as a whole, will not be attempted. Rather, the relative effectiveness of the use of test patterns for process verification, in-process QC and 100% screening investigations with relationship to each failure mechanism will be explored.

2.3.3.4.1 Life Test/Longevity Qualifications

Meaningful accelerated stressing is proposed to verify the effectiveness of the test patterns. This will include stress evaluation of various test vehicles and test patterns, other than the actual CMMA, as discussed in the foregoing reliability assurance plan.

Failure distributions will be generated at stress levels

of three or more discrete magnitudes to study the occurrence of a particular failure mechanism by suitable employment of the test vehicles. This will enable us to evaluate the reliability integrity of a particular process step and as a means to extrapolate to lower actual in-use stress levels on a per-failure-mechanism basis.

The foregoing development of stress-time domains for each failure mechanism, as it relates to a particular process aspect, may prove valuable in determining suitable screens in an attempt to reduce the failure rate per failure mechanism per process step.

The failure mechanism occurrences which are being anticipated will be essentially associated with cross-overs of dual metallization systems,multiple dielectric layers, surface passivation, aluminum metallization, through-holes (vias), interconnects, package and others which are unique to large scale array devices of the proposed circuit and process CMMA design.

To evaluate the reliability performance of the CMMA under simulated in-use conditions, it is proposed to submit fifty units to a dynamic long-term life test at maximum fanout at 25^{o}C ambient employing a switching speed comparable to the operating mode of the system

in which the CMMA will be absorbed. To achieve valid acceleration, an additional lot size of devices will be stressed in accordance with the same life test configuration but at another ambient condition as to be determined during Phase II. The intended duration for both longevity tests would be 2 years. The intent of these tests is to develop history on the completed CMMA in order to determine if there are any failure modes/ mechanisms peculiar to the CMMA.

To estimate the rate of occurrence of individual failure mechanisms, it is proposed to generate accelerated stress-time domains on the following process and design related test vehicles.

Failure Mechanism(s) Related To:	Applied Stress Combinations
a) Cross-overs of dual metallization, multiple dielectrics, through-holes (vias)	Voltage and temperature
b) Aluminum metallization, interconnects	Current and temperature
c) Surface Passivation	Voltage and temperature

Stress domains a), b) and c) will be specifically explored in this study as a basis from which to predict the incidence of individual failure mechanisms applicable to the CMMA.

In order to arrive at meaningful in-use failure occurrence

on a per-failure-mechanism basis, it is proposed to generate a minimum of three failure distributions. It is intended to apply stress of increasing magnitude and hopefully to relate the frequency of failure with time resulting in a time dependent extrapolation. The three time dependent stress levels will be chosen in such a manner that the same predominant failure mode of interest will prevail throughout the stress-time domain so that for each of the three anticipated major failure mechanism categories, an in-use time occurrence relationship can be extrapolated. (See Figure 2.3-2).

From the foregoing approach log-normal or Weibull cumulative failure plots can be generated which will enable us to show a need for screening early failures. This is best illustrated in Figure 2.3-3 where an initial part of the cumulative failure distribution deviates from the intrinsic life distribution. By performing an effective burn-in, the apparent deviation can be eliminated resulting in a true intrinsic life distribution, i.e. free of possible infant mortality.

Each failure mechanism, if found to be time dependent, must exhibit a time dependent rate of incidence. This will be useful in establishing effective screens and to correlate process stability.

The approach of extrapolating to in-use operating conditions has proven to be a valid method as corroborated by the Bell Telephone Laboratories who started to initiate many step stress and accelerated extrapolated tests in the early 1960's with great success. Their experience has been backed up by current results of long-term life testing semiconductor devices both in the field (e.g. Telstar and the like) and in their laboratories.[25]

2.3.3.4.2 Environmental Qualifications

The package and wire bonding system of the CMMA will be subjected to Radiation's standard environmental testing procedures, based on Mil-Std-883. Additional qualification steps will be performed in areas of die attach and bond strength evaluations. Since the package for the CMMA is not defined at this time, no specific stress levels will be discussed.

The complexity and relative cost of the basic CMMA die renders it a difficult vehicle for environmental qualifications. All package qualifications run during the Phase II and III efforts will use the standard test vehicle pattern developed for the CMMA. This procedure has the following advantages:

a) The test vehicle is specifically designed to monitor

all dominant failure modes and will therefore be a more sensitive indicator than the proposed CMMA die.

b) The die size is identical to the CMMA die, providing a valid basis for comparison.

c) Electrical testing is greatly simplified, as is failure analysis of reject units.

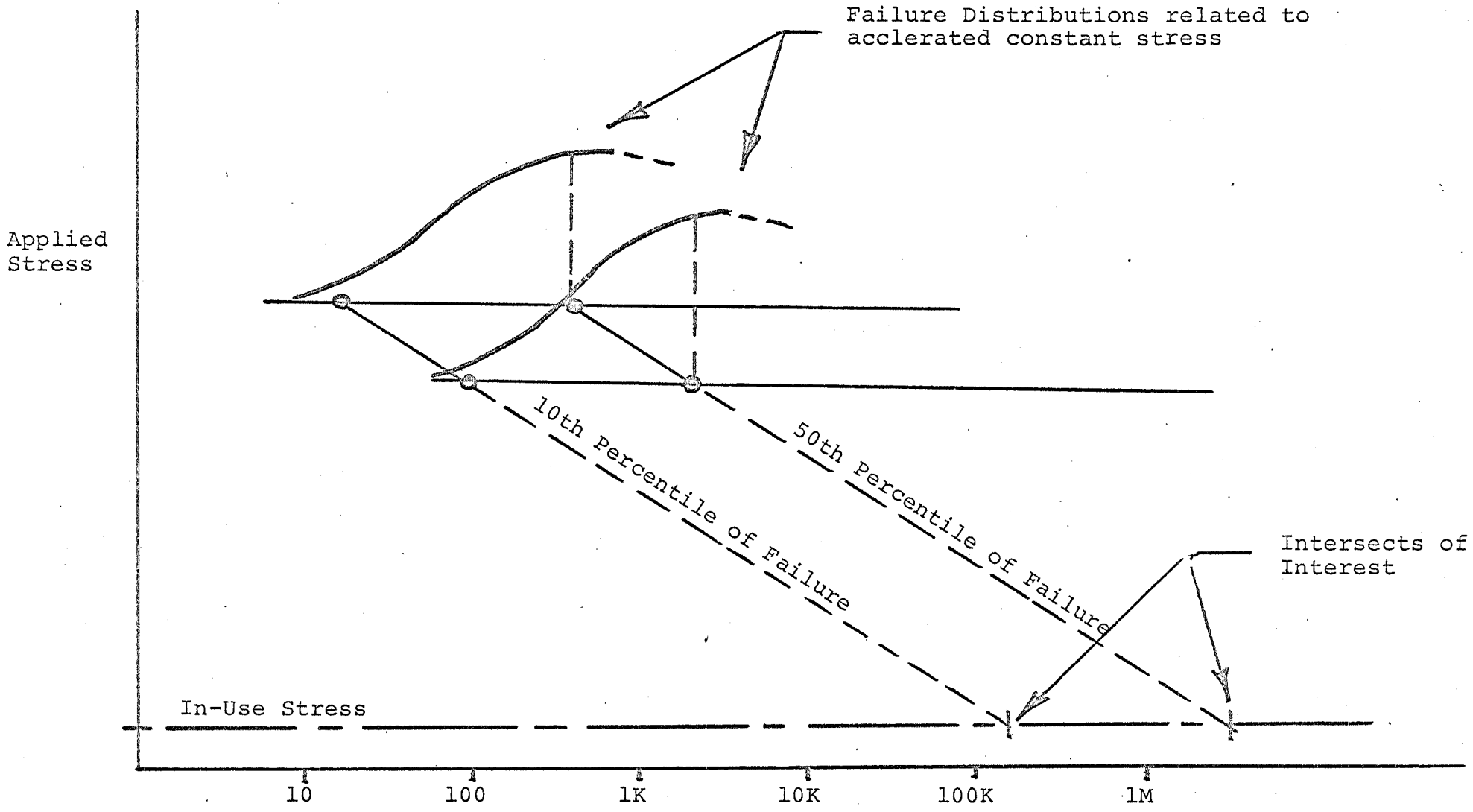

Failure Distributions related to acclerated constant stress
Applied Stress
10th Percentile of Failure
50th Percentile of Failure
Intersects of Interest
In-Use Stress
10
100
1K
10K
100K
1M
Log of Aging Time (in hours)

Figure 2.3-2

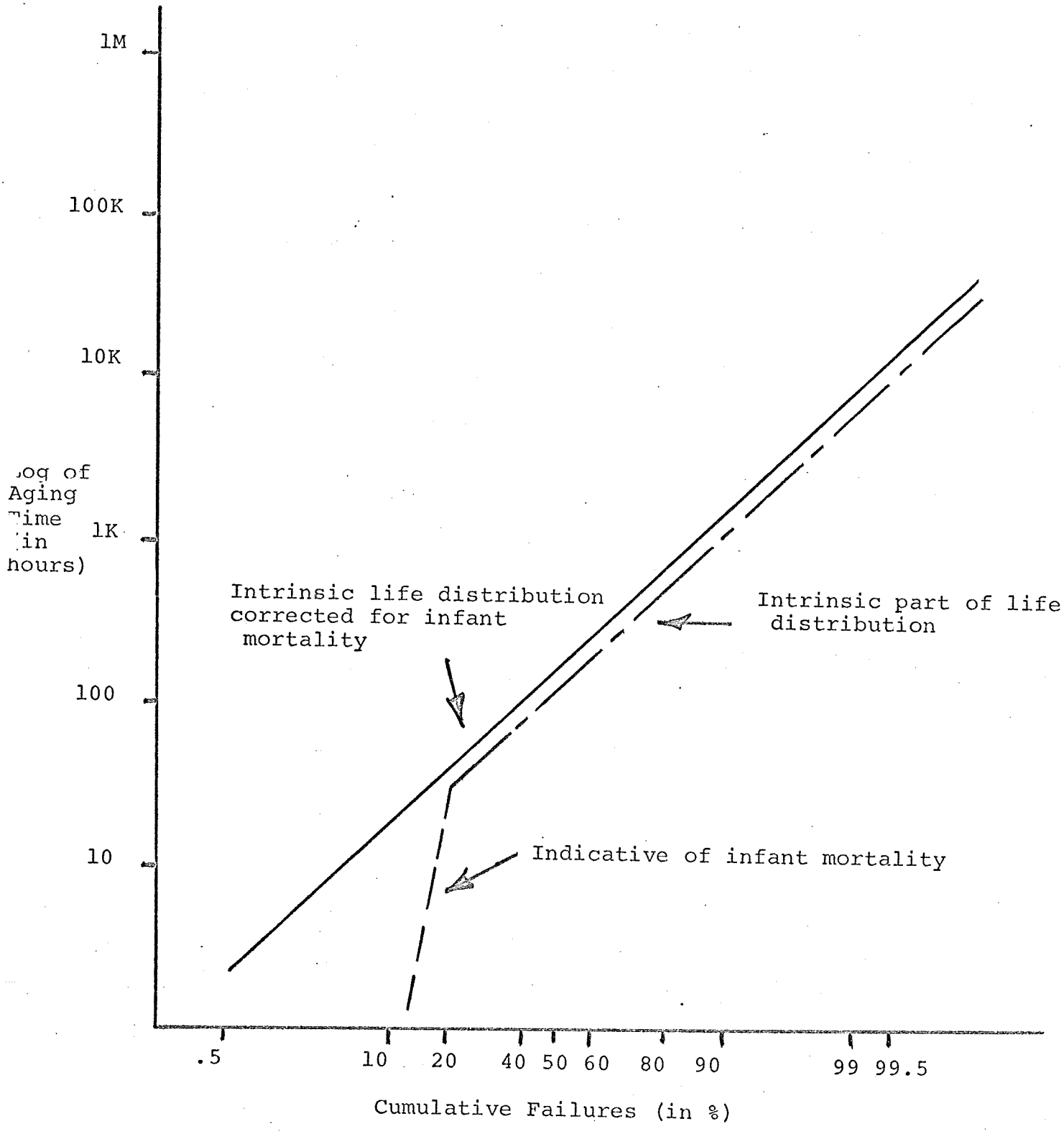

1M
100K
10K
Log of Aging Time (in hours)
1K
100
10
Intrinsic life distribution corrected for infant mortality
Intrinsic part of life distribution
Indicative of infant mortality
.5
10
20
40
50
60
80
90
99
99.5
Cumulative Failures (in %)

Figure 2.3-3

3.0 RECOMMENDATIONS AND CONCLUSIONS

The CMMA will require unconventional techniques for determing inherent quality. The test patterns described in Section 2.3 apparently provide some of these. During Phase II, the value of these patterns should be established as part of the development of the detailed Product Assurance plan.

Further work is needed to provide justification for whether individual gate testing is needed.

Since this program will use the epitaxial base structure, visual inspection standards must be revised. An attempt will be made to correlate visual criteria to device and circuit performance to determine if cell testing is needed or visual inspection and environmental testing will suffice.

APPENDIX 1

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