JPL CONTRACT 952592
(SUBCONTRACT UNDER
NASA CONTRACT NAS7-100)

SECTION I

INTERIM TECHNICAL REPORT

CUSTOM METALLIZED MULTIGATE ARRAY

FOR

CALIFORNIA INSTITUTE OF TECHNOLOGY
JET PROPULSION LABORATORY
4800 OAK GROVE DRIVE
PASADENA, CALIFORNIA 91103

JANUARY 26, 1970

RADIATION INCORPORATED
MICROELECTRONICS DIVISION
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RADIATION INCORPORATED
Microelectronics Division
Melbourne, Florida

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APPENDICES

1.0 INTRODUCTION AND SUMMARY

Section I of this interim report documents the Phase I design study effort for development of a Custom Metallized Multigate Array. Major areas of design investigation during this study were:

(1) Fabrication techniques and process design;

(2) Circuit design and analysis;

(3) Die organization and topological studies;

(4) Multi-level interconnect system studies;

(5) Radiation effects analyses; and

(6) Development of test concepts and general test philosophy.

Each of the above investigations were constrained by and related to the prime program development objective of reliability. The Phase I reliability study effort is documented as Section II of this interim report. Reliability aspects of the proposed design approach documented in Section I of this report are considered in detail in Section II.

The proposed design approach to the CMMA involves the following major aspects: (1) Fabrication of an array of 92 three-input, open-collector NAND gates; 24 three-input, active pull-up NAND gates; and 24 three-input extender and resistor pull-up cells. Die size of this array is approximately 104 mils by 134 mils. (2) Fabrication of this array through a minimum complexity, high packing density epitaxial base process. The proposed wafer

fabrication process requires three selective and one non-selective diffusions and one epitaxial deposition. (3) Component interconnection and custom gate interconnection through use of a two-level aluminum-silicon dioxide-aluminum metallization system and a diffused power and ground distribution system. Intra-cell wiring and second level cross-unders are accomplished with a fixed first level metallization; Inter-cell wiring to realize a specific custom logic function is accomplished with a custom second level metallization pattern.

Principal accomplishments and results of the Phase I Design Study include the following: (1) Optimization of the epitaxial base process for the CMMA application and fabrication and characterization of devices suitable for application in the Multigate Array. (2) Design and analysis of circuit structures required for mechanization of the proposed Multigate Array; (3) Performance of process verification and reliability studies on the two-level metallization system; (4) Analysis of device degradation effects after exposure to the specified radiation environment; (5) Development of a proposed die organization; and (6) Study and definition of alternate CMMA test concepts at probe and package level.

Major problem and/or trade-off areas which have been defined as a result of the Phase I design study include:

(1) Power-speed objectives have not simultaneously been achieved. Further study and a probable trade-off will be required in this area. (2) Noise margin objectives are not met at high temperature (125^{o}C) and low voltage (3.6V). A probable relaxation will be required in this area. (3) Breakdown voltages which can be repeatedly achieved without degradation in reliability, yield, and performance are less than the specified absolute maximum rating of 8 volts. A relaxation will be required in this area. (4) Oxide and metal thicknesses for the two-level interconnect system have not been optimized for yield and reliability. Further study is required. (5) Definition of test methods to optimize reliability assurance which are technically and economically feasible has not been accomplished. Further investigation and trade-off studies are required.

2.0 RECOMMENDATIONS

The following recommendations are submitted:

1) Continue the effort as outlined in the work statement for Phase II of the contract except as modified herein.

2) Adopt the design approach described in this report with additional consideration in the following areas.

3) Continue circuit mechanization and analysis to determine optimum power/speed and noise margin performance. Included in this effort should be consideration of alternate circuit mechanizations.

4) Perform post radiation performance analysis based on calculated device degradation for the herein proposed epitaxial base process. If possible perform radiation device testing to verify calculated degradation factors.

5) Continue investigation of test methods and techniques including the question of individual gate probe testing.

6) Adopt the programmable tester concept as described in Section 3.7 of this report. This tester concept is recommended in lieu of the custom tester concept outlined in the statement of work.

3.0 CMMA PHASE I DESIGN SUMMARY

3.1 Design Requirements and Objectives

3.1.1 Primary Objectives

The primary objectives shall be the design and fabrication of a low power bi-polar monolithic integrated circuit whose function can be determined by varying the interconnect metallization pattern(s). The design shall be governed by the following considerations, listed in order of decreasing importance.

3.1.1.1 Reliability: Reliability shall be considered to be of prime importance and shall influence all phases of design and fabrication.

3.1.1.2 Process simplicity: The number of discrete fabrication processes shall be kept to a minimum. All processes shall be within the state-of-the-art and within fabrication capability of more than one manufacturer, but need not reflect current manufacturing techniques where this could lead to possible early obsolescence.

3.1.1.3 Power consumption: Refer to Section 3.1.3.5

3.1.1.4 Functional flexibility: Refer to Section 3.1.3.6

3.1.1.5 Noise immunity: Refer to Section 3.1.3.7

3.1.1.6 Frequency of operation: Refer to Section 3.1.3.8

3.1.2 Functional requirements

The MA shall be designed for functional flexibility. A minimum requirement shall be the capability of performing a variety of logic functions by defining variations in the metallization interconnect pattern(s) without modification to the circuitry on the die. The MA shall be composed of the functional organization and shall operate according to the electrical and environmental requirements specified herein.

3.1.3 Electrical requirements

3.1.3.1 Logic levels:

a. Logic "1": +2.4 to +5.5 volts

b. Logic "0": 0.0 to +0.4 volt

3.1.3.2 Interfaces: All inputs and outputs shall be compatible with a TTL or DTL logic interface. All standard gate outputs shall be open collector, grounded emitter transistors.

3.1.3.3 Power supply: One power supply voltage shall be allowed. The voltage operating range shall be +3.6 to +5.5 volts.

3.1.3.4 Overvoltage: The design shall require that the MA with any metallization pattern shall not be damaged by application of +8.0 volts to the power supply node of any gate or application of +5.5 volts to any other input or output node of any gate, with the exception of the fan-in extension nodes.

3.1.3.5 Power consumption: The following information shall be considered design goals, rather than design requirements. Improvements in these goals will be given favorable consideration.

a. Standard gate output "1" power consumption: The power consumption of any standard gate of the MA shall not exceed 0.20 milliwatt (mw) under the following test conditions:

a. Temperature: +25°C.

b. Supply voltage: +5.0 vdc.

c. Gate inputs: Logic "0".

d. Gate outputs: No connection.

b. Standard gate output "0" power consumption: The power consumption of any standard gate of the MA shall not exceed 0.50 mw under the following test conditions:

a. Temperature: +25°C.

b. Supply voltage: +5.0 vdc.

c. Gate inputs: Logic "1".

d. Gate outputs: No connection.

c. Driver gate output "1" power consumption: The power consumption of any driver gate of the MA shall not exceed 0.80 mw under the following test conditions:

a. Temperature: +25°C.

b. Supply voltage: +5.0 vdc.

c. Gate inputs: Logic "0".

d. Gate outputs: No connection.

d. Driver gate output "0" power consumption: The power consumption of any driver gate of the MA shall not exceed 2.0 mw under the following test conditions:

a. Temperature: +25°C.

b. Supply voltage: +5.0vdc.

c. Gate inputs: Logic "1".

d. Gate outputs: No connection.

3.1.3.6 Functional flexibility: The MA shall be designed with sufficient flexibility to enable the fabrication of a wide variety of logic functions by employing JPL specified interconnect metallization pattern(s). The MA shall include, but not necessarily be limited to, the following functional capabilities.

a. Interconnection crossover capability: The MA with any metallization pattern(s) shall have the capability of employing a minimum of 200 electrical crossovers.

b. Standard gate fan-out: The MA shall include a minimum of 75 gates capable of driving a load equal to a minimum of 12 standard gates with no output pull-up or a minimum of 11 standard gates with an output pull-up after being subjected to specified radiation environment (see 3.5).

c. Driver gate fan-out: The MA shall include a minimum of 25 gates capable of driving a load equal to a minimum of 50 standard gates with no output pull-up or a minimum of 49 standard gates with an output pull-up after being subjected to specified radiation environment (see 3.5).

d. Gate fan-in: All gates of the MA shall have a fan-in capability of three with the additional capability of fan-in extention.

e. Fan-in extention: The MA shall have the capability to expand the fan-in of any gate to a minimum of 12 by the use of fan-in extenders located in the MA and connected to the expanded gate by means of the interconnect metallization pattern(s). A minimum of 24 extenders with a fan-in of three each shall be available for this function.

f. Gate output pull-up: The MA shall include the capability to connect passive pull-up to any gate by the use of pull-up resistors located in the MA and connected to the gate by means of the interconnect metallization pattern(s). A minimum of 48 pull-up resistors shall be available for this function, 24 of which shall equal a load of one standard gate and 24 of which shall equal a load of 10 standard gates.

g. Supply voltage interconnect: The MA shall have the capability to avoid applying power to a large portion of those gates not necessary to implement the required logic function.

h. Logic flip-flop capability: The MA shall have the capability to employ gates to implement the logic function of a R-S flip-flop.

3.1.3.7 Noise immunity: The MA shall not malfunction when subjected to any of the following noise conditions at any temperature within the operating temperature range.

a. Power supply noise: Voltage spikes on the power and ground lines having a maximum amplitude of 0.2 volt peak-to-peak and having a width from 10 nanoseconds (nsec) to 20 microseconds (μsec). The frequency of the spikes shall not exceed 100 kilocycles (kc).

b. Signal noise: Voltage spikes on the signal lines having a maximum amplitude of $\pm$ 0.40 volt and having a width from 10nsec to 20μsec. The frequency of the spikes shall not exceed 100 kc.

c. Power supply turn-on: The gate outputs of the MA shall reach their required output logic levels, as determined by their input logic levels, without an excessive power supply current drain when power is applied in the following manner:

Application of a step voltage with a rise time 100 nsec and amplitude of +5.0 volts, through a R-C filter with a resistance of 10 ohms and a capacitance of 1.0 microfarad (μf), to the power supply node of the gate.

d. Power supply turn-off: The gate outputs of the MA shall reach 0.0 volt without an excessive power supply current drain when power is removed in the following manner:

Decrease of power supply voltage from +5.0 to 0.0 volts, with a fall time of 100 nsec, through a R-C filter with a resistance of 10 ohms and a capacitance of 1.0 (μf), to the power supply node of the gate.

3.1.3.8 Frequency of operation: The following information shall be considered design goals rather than design requirements. Improvements in these goals will be given favorable consideration.

a. Standard gate propagation delay: The propagation delay of any standard gate of the MA shall not exceed the values specified in Table I when measured as specified on Figure 3.1-1.

Table I. Propagation Delay of Standard Gates

R_1 (ohms)	C_1 (pf)	Maximum t_{pd1} (nsec)	Maximum t_{pd0} (nsec)
R R/N	10+C 20+NC	50	20 50

R = 1 standard load.

C = 1 standard load.

N = standard gate fan-out.

b. Driver gate propagation delay: The propagation delay of any driver gate of the MA shall not exceed the values specified in Table II when measured as specified on Figure 3.1.-2.

Table II. Propagation Delay of Driver Gates

R_1 (ohms)	C_1 (pf)	Maximum t_{pd1} (nsec	Maximum t_{pd0} (nsec)
R R/M	10 + C 20 + MC	50	10 50

R = 1 standard load.

C = 1 standard load.

M = driver gate fan-out.

3.1.4 Environmental requirements

3.1.4.1 Operating temperature: The MA shall operate with case temperatures from -55 to +125°C.

3.1.4.2 Storage temperature: The MA shall be submitted to high temperature storage per MIL-STD-883, Method 1008, Test Condition C (72 hours at 150°C).

3.1.4.3 Thermal shock: The MA shall be subjected to thermal shock per MIL-STD-883, Method 1011, Test Condition A (Tmin = 0°C, Tmax = 100°C, 5 minutes at each extreme, transfer time less than 10 seconds, 5 cycles).

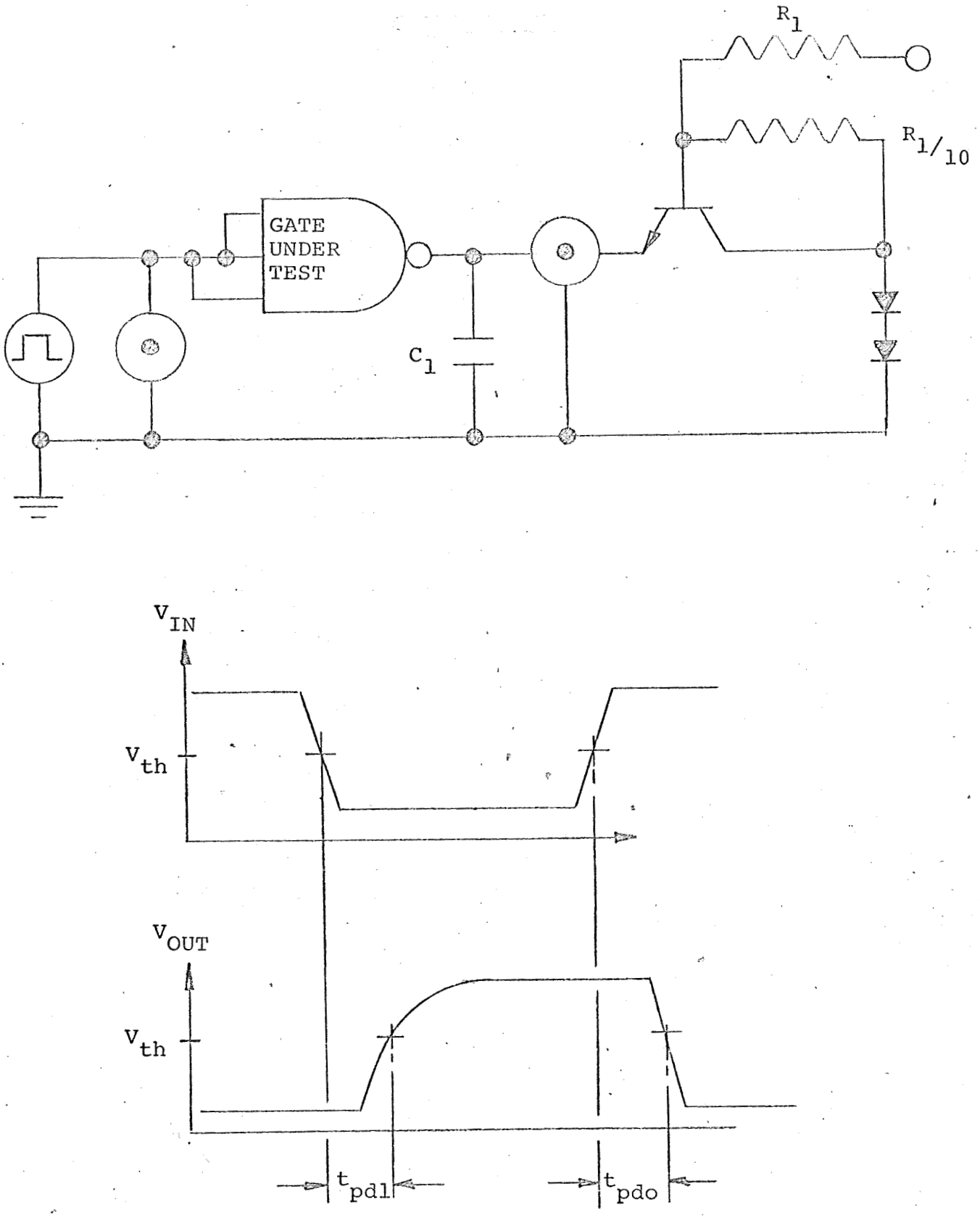
3.1.4.4 Centrifuge: The MA shall be subjected to centrifuge testing per MIL-STD-883, Method 2001, Test Condition E, Y_1 axis only (30,000 g's for 1 minute).

3.1.4.5 Hermeticity: The MA shall be subjected to a gross hermeticity test at the conclusion of the environmental tests. This test shall be per MIL-STD-883, Method 1014, Test Condition D (penetrant dye - fluorescein).

3.1.4.6 Radiation: The MA shall operate properly while being subjected to the radiation environment specified in Section 3.5 of this report.

3.1.4.7 Sterilization: The performance of the MA shall not be degraded below required performance levels when subjected to the following sterilization environment:

Dry heat: nonoperational exposure to 6 heat cycles at a maximum temperature of 135°C for 92 hours per cycle in a nitrogen atmosphere.



PROPAGATION DELAY TEST SET UP

FIGURE 3.1-1

3.2 DIE ORGANIZATION

The implementation of the Multigate Array circuit functions require concepts which afford maximum flexibility while maintaining a high packing density. The concepts utilized include; 1) A diffused power and ground bus system which frees the metal layers for intra-gate and inter-gate wiring. 2) A two level metal system, the second of which is varied to realize a specific logic function, and 3) positioning of the different cell types in a manner to provide for their most efficient usage.

3.2.1 Cell Matrix Pattern

The die is organized in a dual matrix pattern as shown in Figure 3.2-1 with the left side of die a mirror image of the right. A strip in the center of the die is utilized for metal ground and V_{cc} lines. Each matrix is a 6 x 12 array with the vertical dimension of each cell type constrained to be alike. Since their maximum usage will be as output interface devices, the driver gates shown in Figures 3.2-4 and 3.2-8 are arranged in columns along the outside edge of the die. For maximum flexibility, the extender cells, shown in Figures 3.2-5 and 3.2-9 are centrally located with respect to the other cells - a column in each half of the die. The remaining 4 columns in each die half consist of standard gate cells, two variations of which are shown in Figures 3.2-2, 3.2-6, 3.2-3 and 3.2-7, plus 2 positions per side to accommodate special test structures. This organization gives the added advantages of more efficient use of die area,

since differing cells need only be constrained in one dimension.

Total gate count is then:

24 Driver Gates

92 Standard Gates

24 Extender/Resistor pull-ups

4 Test structure cells

3.2.2 Power and Ground Bus System

The bus system for power and ground on the die consists of aluminum mains on the second level of interconnect located down the center of the die and a distribution system of diffused lines which leaves the metal layers free for signal wiring as shown in Figure 3.2-10. The location of the main buses minimizes the length of the diffused buses and makes it possible to split the V_{cc} line in dual logic functions so that each half may be separately energized. Additionally, if individual gate probe is to be accomplished, gates may still be energized in small numbers; that is, in groups of 5.

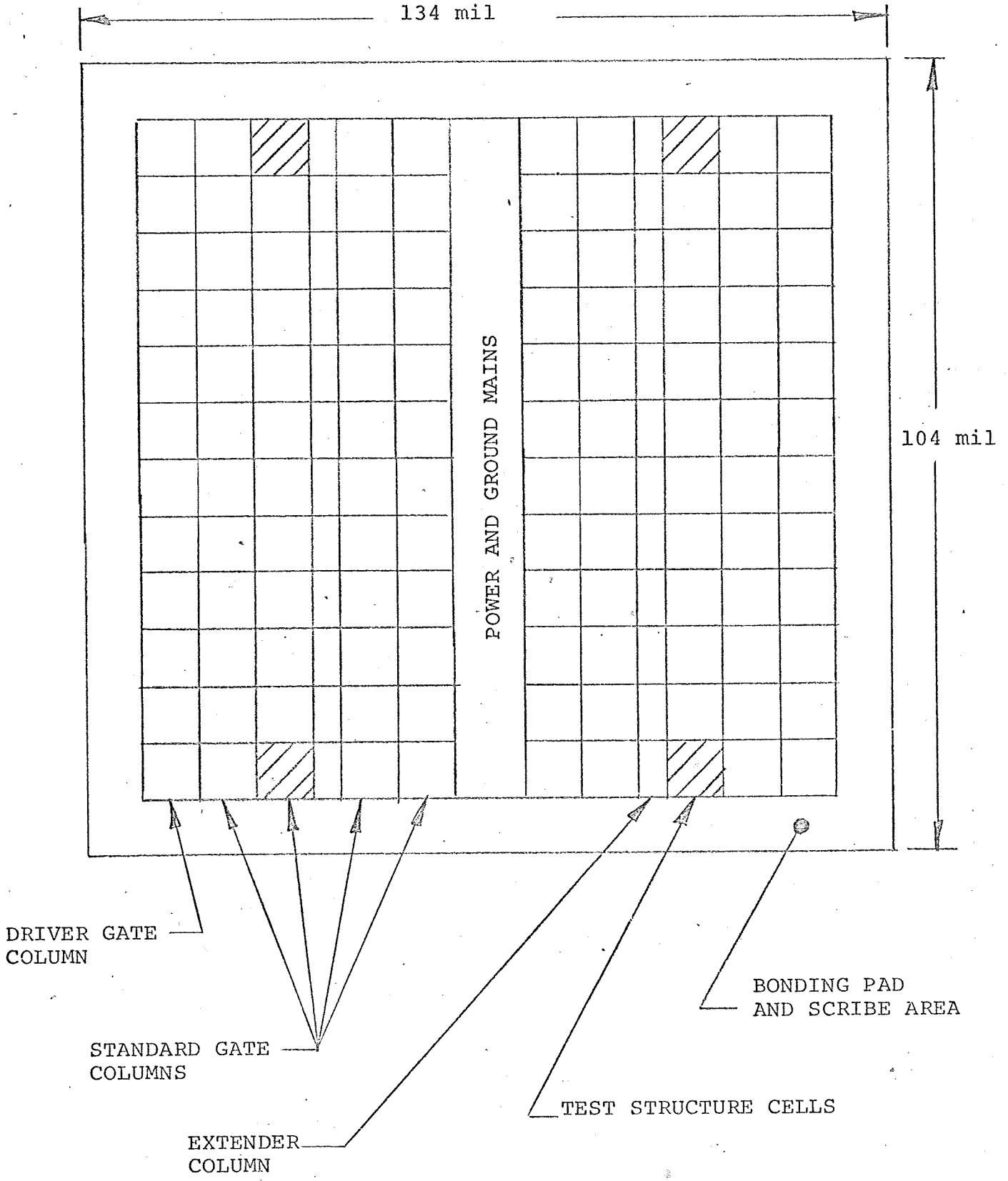
The V_{cc} distribution line is provided by the diffusions which delineate the resistors in the epi-base structure. This distribution bus then adds no area to the die. The ground distribution system is similarly formed by overlapping the N-type emitter, collector, and isolation diffusions. If a three mil wide bus is used, the maximum total resistance of any of the buses is less than 20 ohms. The additional area required for the ground

distribution bus is then available at first level metal for providing cross under tabs to assure interconnection flexibility.

3.2.3 Two Level Interconnect System

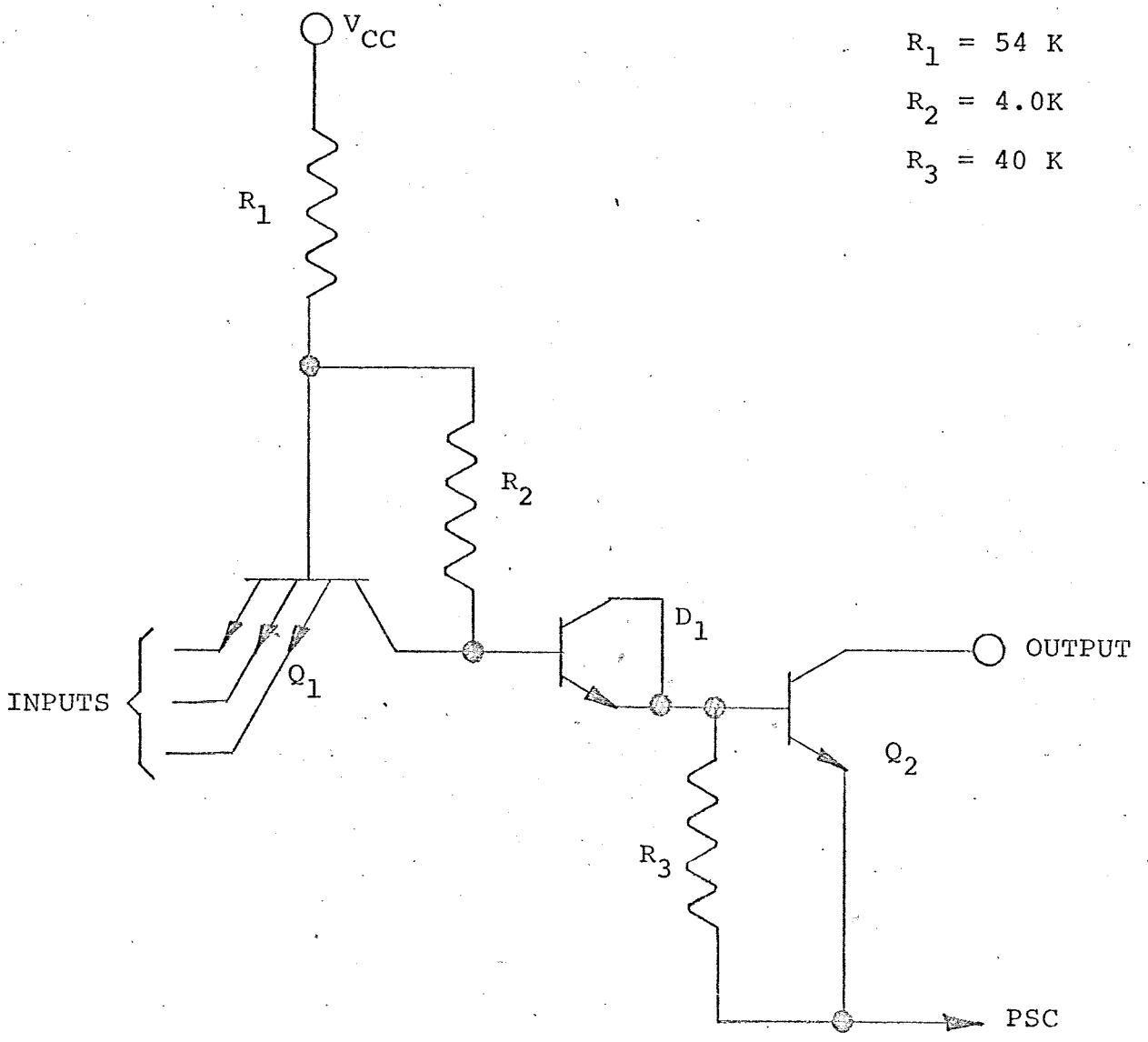
The metal-oxide-metal system defined in Section 3.6 of this report provides a method for generating low impedance, low capacitance circuit wiring with a high degree of flexibility. The first level consists of all intragate wiring and sufficient tabs to provide crossunders that may be necessary to interconnect gates to realize a desired logic function at second level interconnect. Studies indicate that relatively few crossunder tabs will be required to realize the specific functions required by this program. The type D flip-flop originally proposed, for instance, may be wired up at second level without using any crossunder tabs. The most complex of the logic functions specified may be realized with less than 50 crossunders. There will be at least 2 crossunder tabs available per cell on the die with a total of over 300, thus assuring a high degree of interconnection flexibility.

The second level of interconnect, of course, provides the custom metallization. Variations in this level alone need be made to build a specific logic function. If individual gate probe is not implemented, the connection of gates to the ground bus will be made at this level, thus no unused gates will be energized.



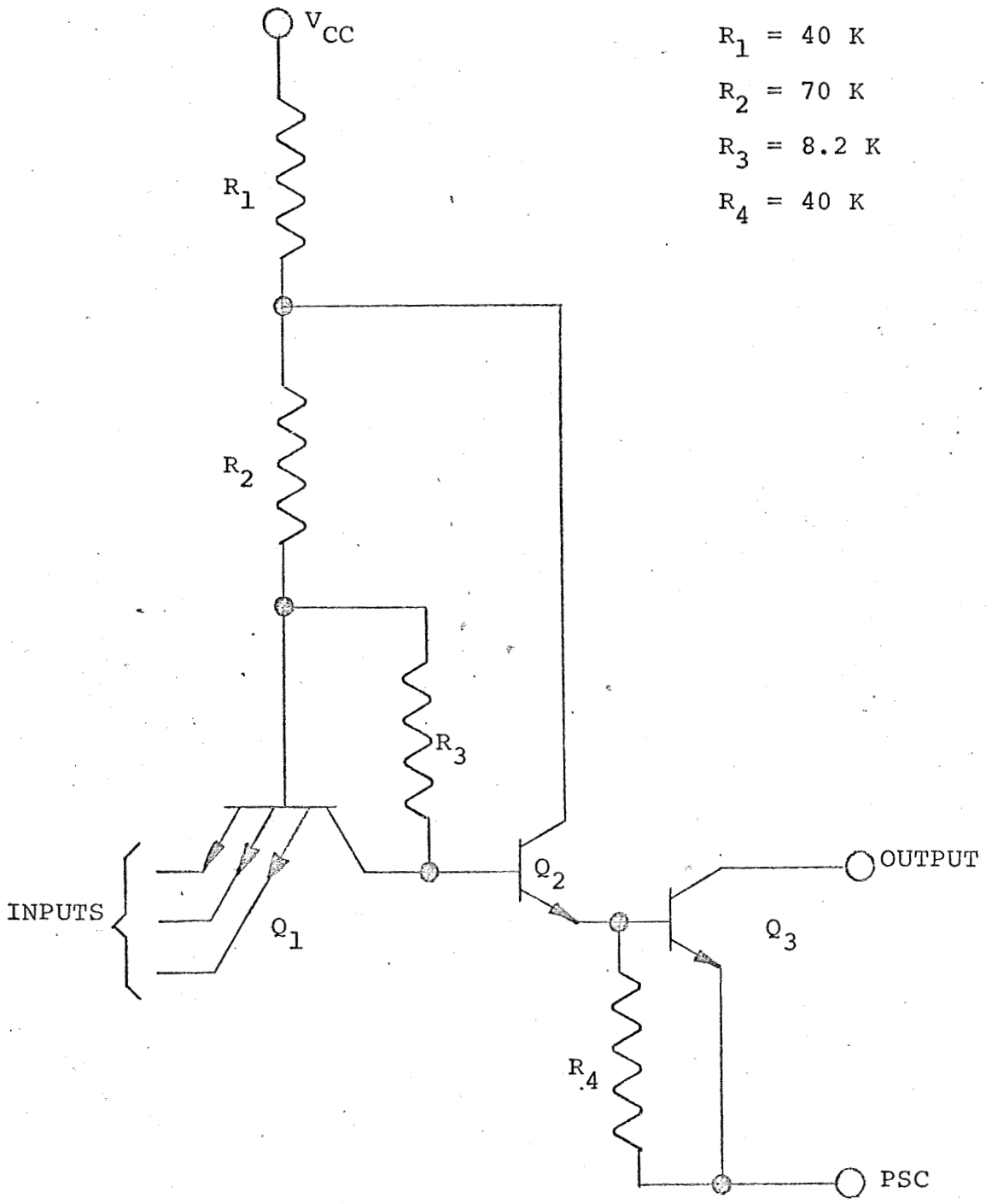
MULTIGATE ARRAY DIE ORGANIZATION

FIGURE 3.2-1



STANDARD GATE 1 SCHEMATIC

FIGURE 3.2-2



STANDARD GATE 2 SCHEMATIC

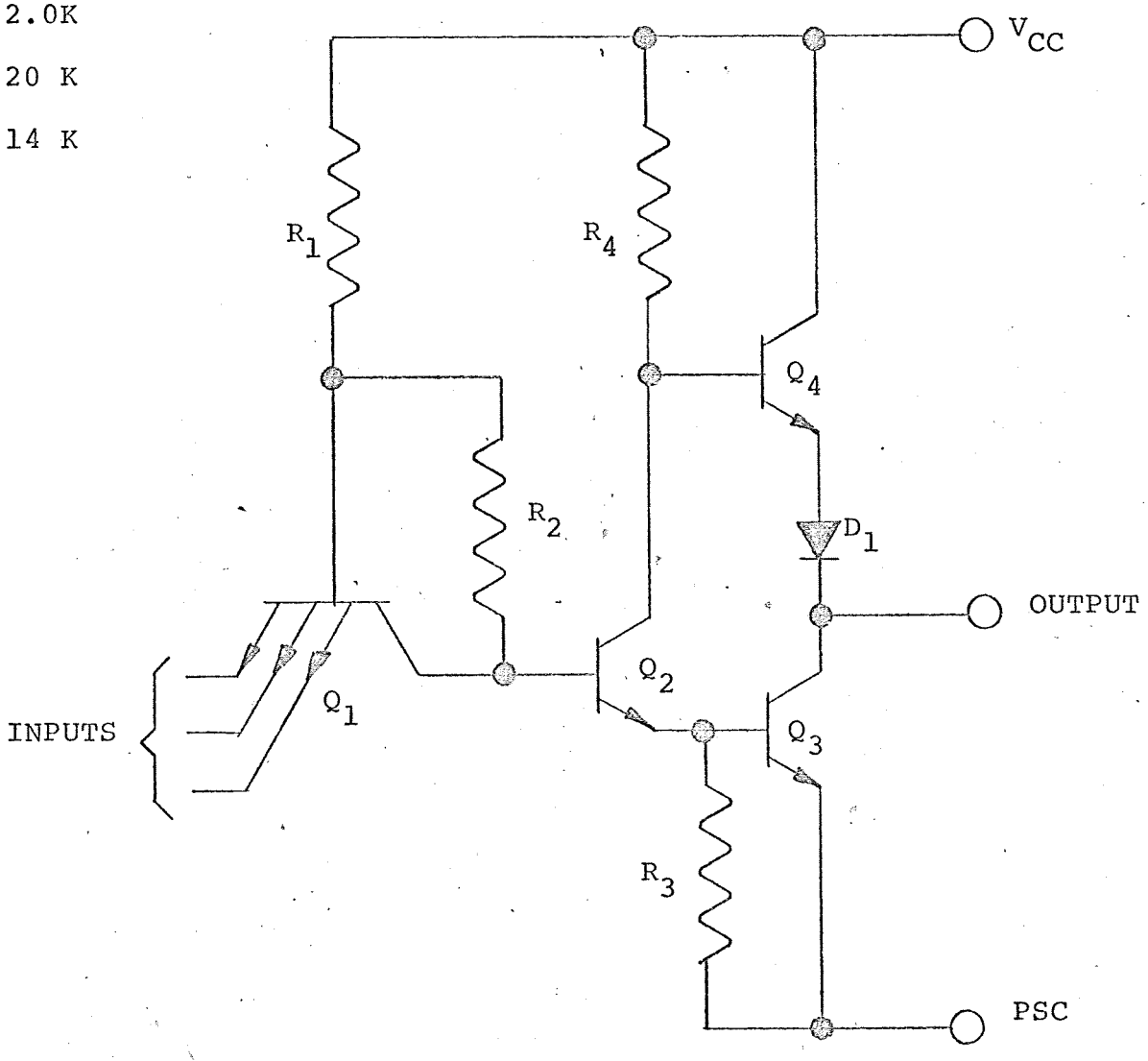
FIGURE 3.2-3

R_1 = 27 K

R_2 = 2.0K

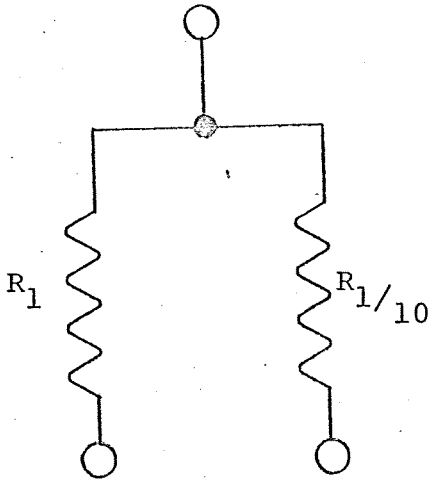
R_3 = 20 K

R_4 = 14 K



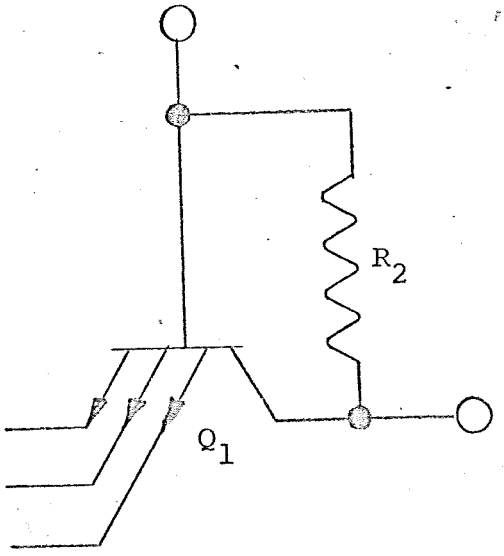
DRIVER GATE SCHEMATIC

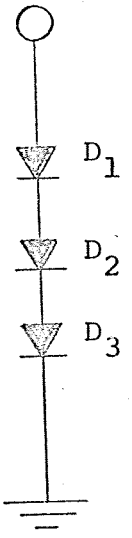
FIGURE 3.2-4



R_1 = 110 K

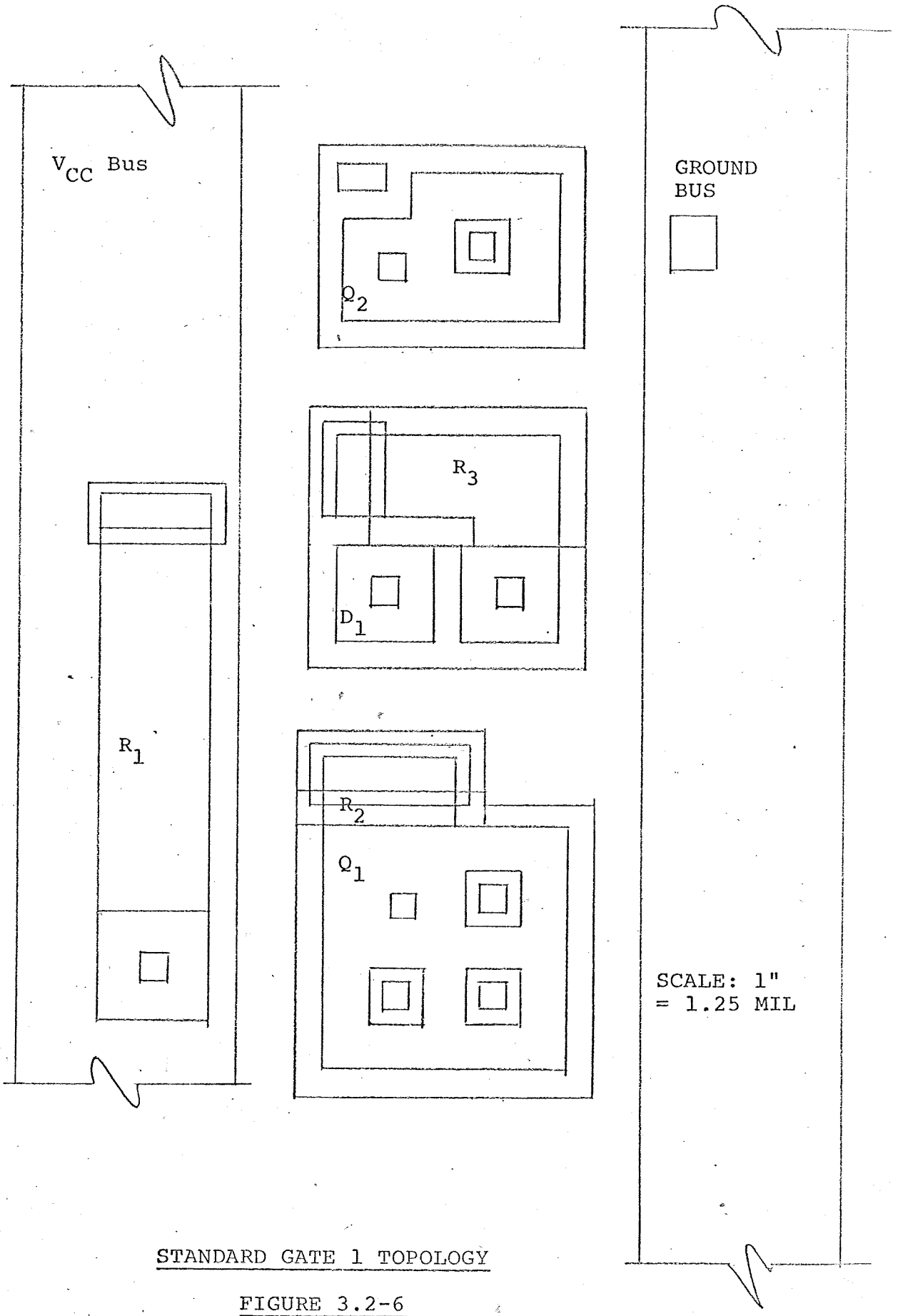
R_2 = 8.2 K





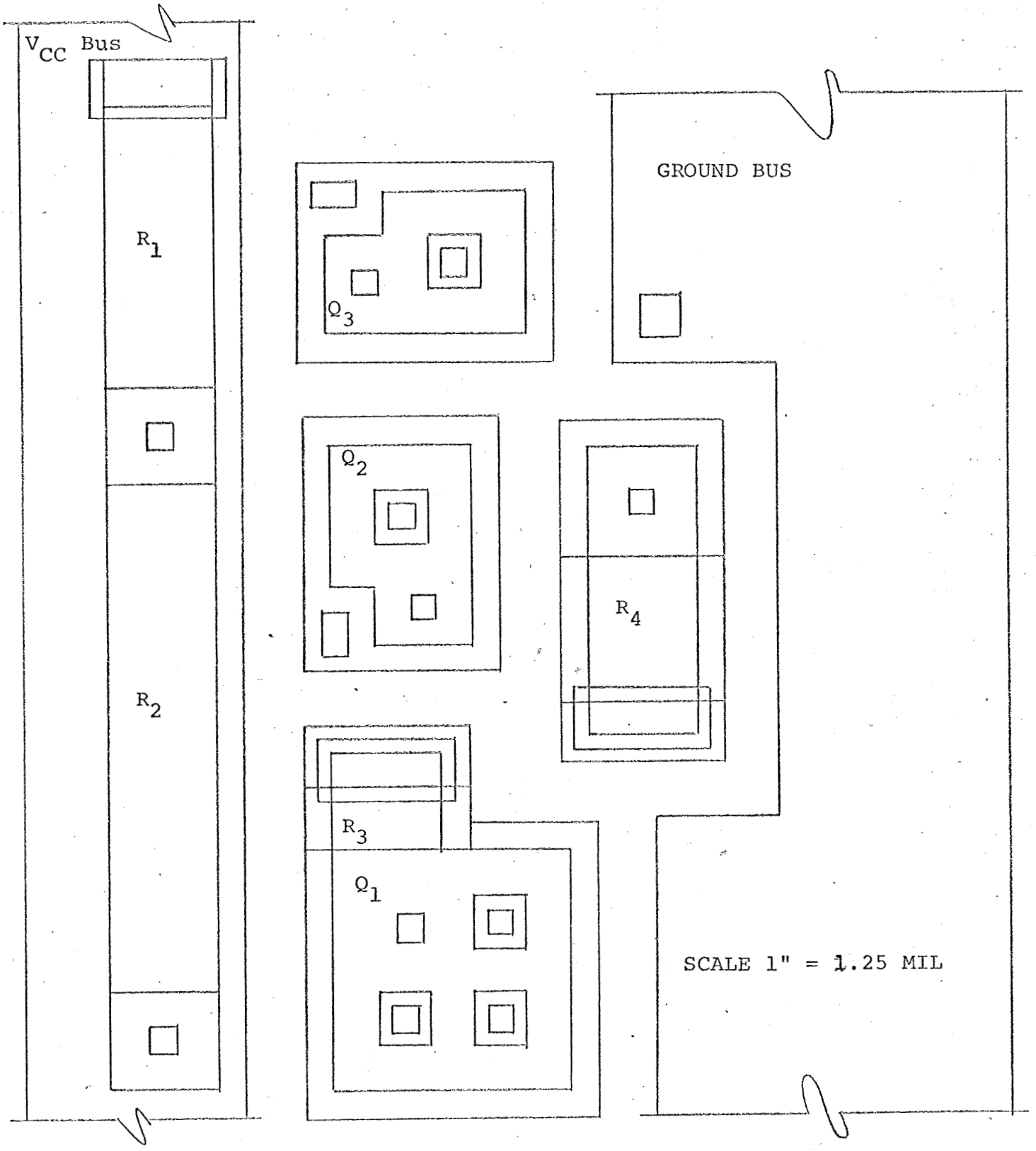
EXTENDER/PULL UP CELL

FIGURE 3.2-5



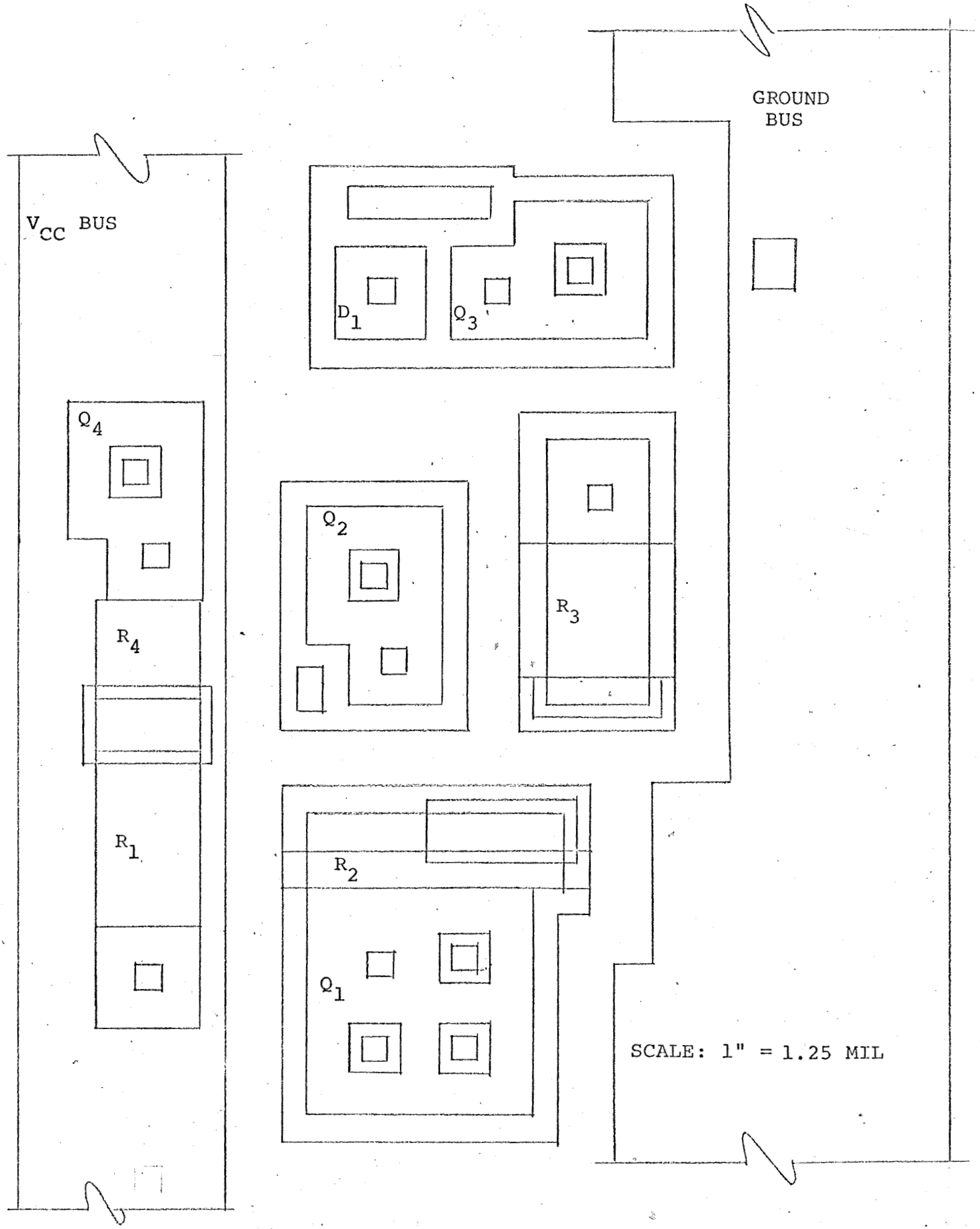
STANDARD GATE 1 TOPOLOGY

FIGURE 3.2-6



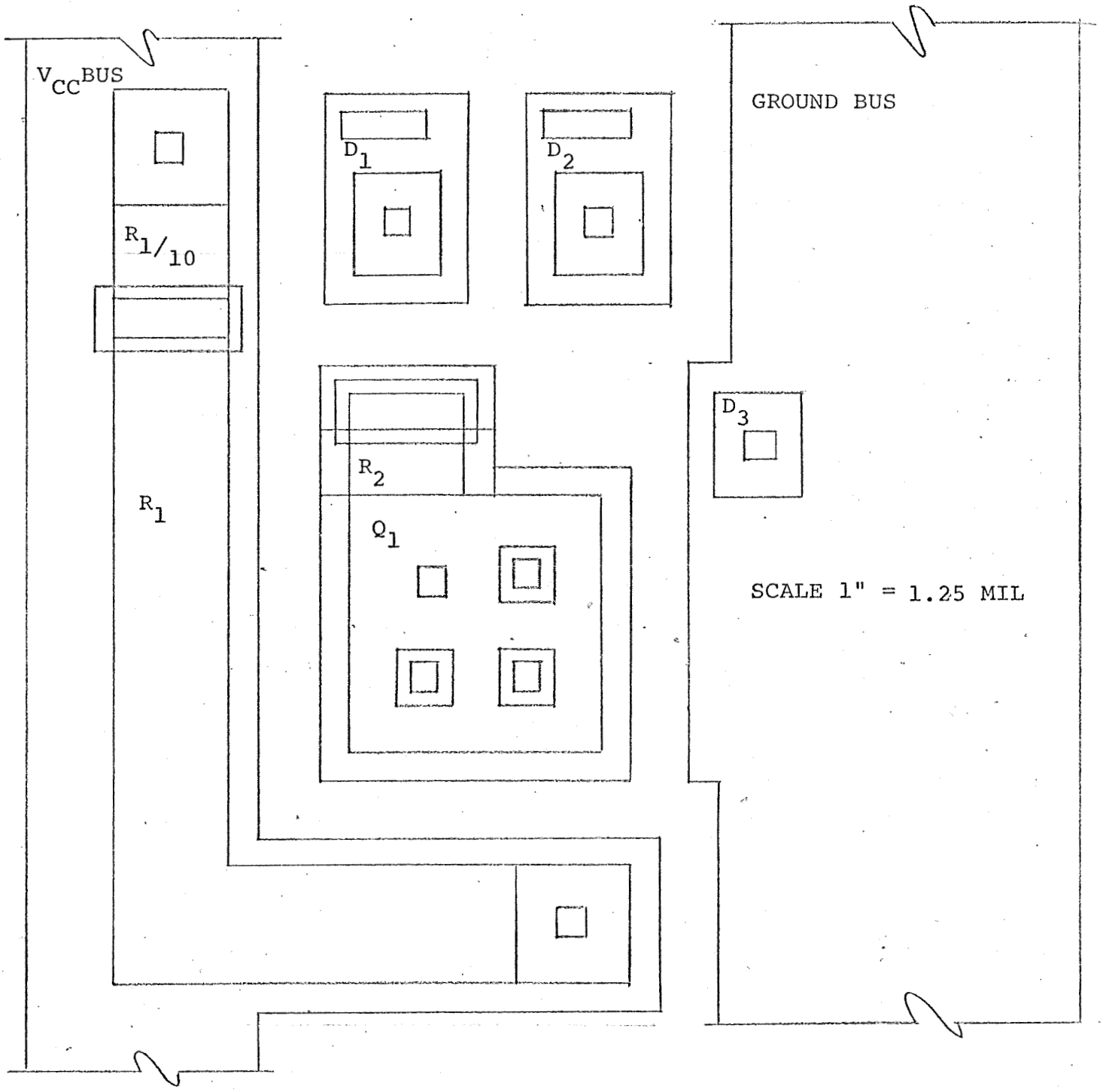
STANDARD GATE 2 TOPOLOGY

FIGURE 3.2-7



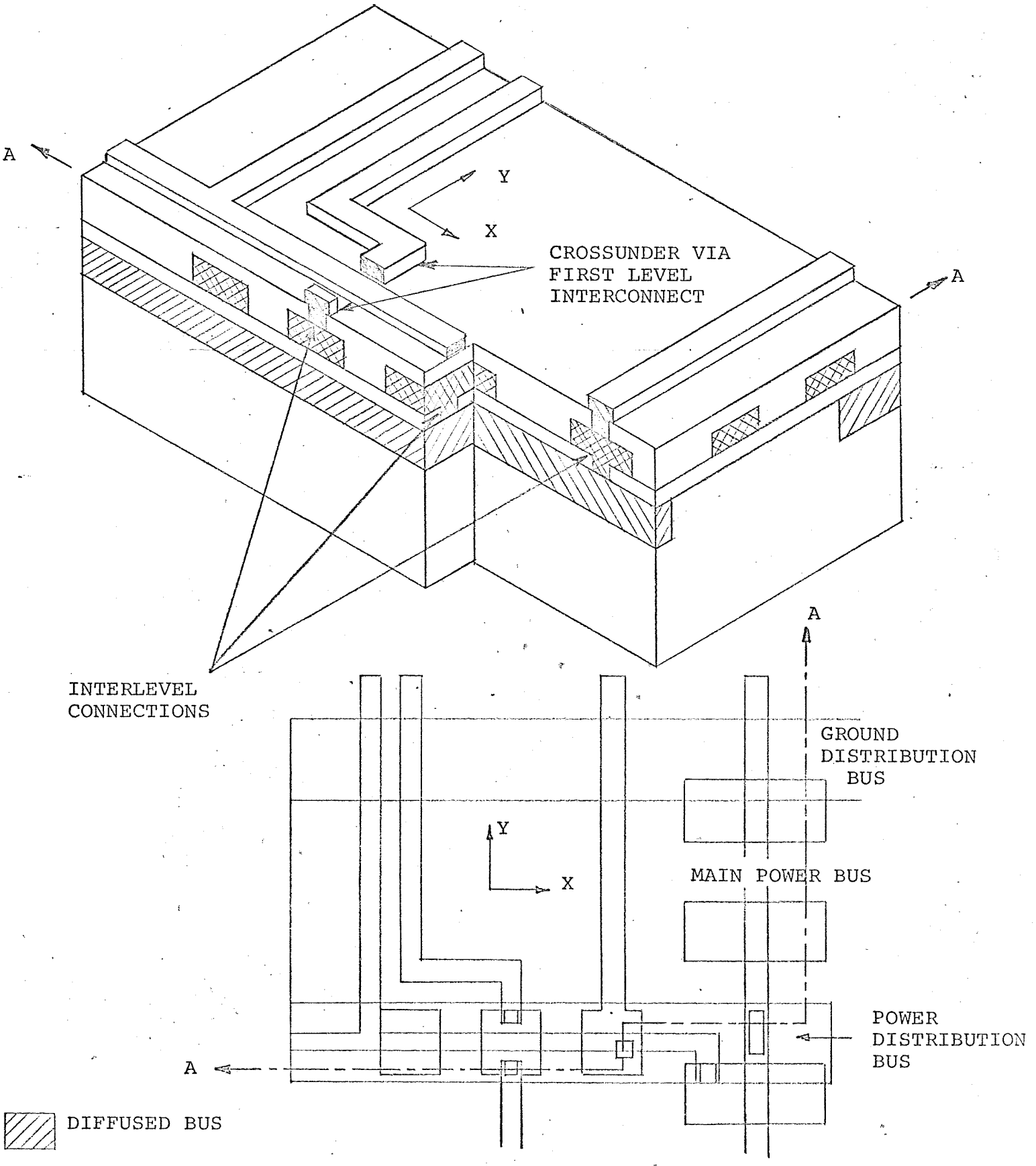
DRIVER GATE TOPOLOGY

FIGURE 3.2-8



EXTENDER/PULL-UP TOPOLOGY

FIGURE 3.2-9



POWER/SIGNAL DISTRIBUTION SYSTEM

FIGURE 3.2-10

3.2.4 Die Size

The individual cell sizes assuming no gate probe are:

Standard gate - 7 x 9 1/2 mils

Driver gate - 7 x 10 mils

Extender/pull up - 7 x 6 mils

Total die size for this approach then is 104 x 134 mils.

If allowance is made for individual gate probe, as discussed in Section 3.7, the total die size would be 134 x 142 mils, or a 36 percent increase in die area.

3.3 Gate Design for the Multigate Array

3.3.1 Circuit Mechanization

Interface requirements for TTL/DTL compatibility and the power supply requirement of a single positive supply with a voltage range of 3.6V to 5.5V immediately restricts possible circuit approaches to a configuration similar to conventional DTL or TTL structures. A TTL approach has in the past been shown to have a speed and die area advantage over a comparable DTL Gate. On this basis TTL structures were selected for the Multigate Array.

In defining a specific logic function, the factors of function per unit area and logic flexibility were considered. An efficient gate topology is realized with a three input gate and, probably more importantly, a Type D Flip-Flop is realizable with 6 such three input gates with no crossunders. A three input TTL NAND Gate was then selected as the MA logic function. A Three Input Extender employing the triple emitter gate input device

along with pull-up resistors and clamp diodes form the Extender/Pull-Up Cell as shown in Figures 3.2-5 and 3.2-9. The clamp diodes are included to provide optimum propagation delay in certain applications of the Standard Gate as described in Section 3.3.3 below.

The circuit configuration for the Driver Gate as shown in Figures 3.2-4 and 3.2-8 is a conventional TTL active pull-up circuit with the exception of the input collector-base clamp resistor, R2. This resistor must be added to effectively eliminate input emitter-to-input emitter gain resultant from the high inverse current gain characteristic of the epitaxial base process. The collector-base clamp resistor reduces the collector-base forward bias, and reduces the effective emitter-to-emitter gain as a function of the ratio of R1 to R2. Addition of this resistor has the negative effect of reducing noise margin as a result of the reduced collector-base forward voltage of the input transistor. An R1/R2 ratio of 13.5 was selected to reduce the reverse input current by a factor of approximately 100 at worst-case conditions of T = 125^{o}C and V^{+} = 5.5V, while reducing noise margin by approximately 120mV. Reverse input current as a function of supply voltage is shown in Figure 3.3-18.

Two circuit configurations for the Standard Gate have been analyzed: Standard Gate 1 shown in Figures 3.2-2 and 3.2-6 and Standard Gate 2 shown in Figures 3.2-3 and

3.2-7. A major trade-off exists between these gate configurations in terms of low-temperature, low-voltage fan-out and propagation delay as described in Section 3.3.3 of this report. Further consideration of this trade-off as well as consideration of a DTL input approach is necessary before a Standard Gate configuration can be selected. Consideration of reverse input current also necessitates use of the input collector-base clamp resistor for the Standard Gate as described above.

3.3.2 Epitaxial Base Device Characteristics

3.3.2.1 General Device Considerations

Transistor, diode, and resistor devices fabricated by the epitaxial base process have been electrically characterized over the full temperature range and applicable current and voltage conditions. This data was employed to develop model parameters for the proposed devices for each of the various MA circuits. The resultant models were then employed in the computer simulations of circuit performance described in the following sections. All model parameters were derived from empirical data except junction capacitance. The devices employed were fabricated with the process proposed for the MA as described in section 3.4 of this report. The transistor and diode models employed are essentially standard Ebers-Moll models. Model parameters were computed from empirical device measurements via mathematical relationships derived from the Ebers-Moll model.

Junction capacitance was calculated using a one-sided step junction approximation based on the base layer resistivity and the applicable junction area. That is,

$$C_j = \frac{C_1 A_j}{(Vj - V_B)^{\frac{1}{2}}}$$

Where

C_1 = capacitance/mil^2, at $V_j - V_B$ = 1V, = 0.4 pf/mil^2

V_B = junction barrier voltage = 0.7V

V_j = applied reverse junction voltage

A_j = junction area (mil^2)

This approximation is conservative in that it results in a maximum capacitance per unit area. Transistor and diode reverse leakage currents were not included in the models since measured values were of negligible magnitude. At T = 125°C for a typical MA device, measured leakages were on the order of:

I_{EBO} = 3nA

I_{CBO} = 40nA

I_{CEO} = 300nA

Test data for the proposed epitaxial base devices is presented in the following section.

3.3.2.2 Device Characteristic Data

TITLE	FIGURE
I_E VS V_{BE}	3.3-1
V_{bc} VS I_C	3.3-2
h_{FE} VS I_C (Small geometry device)	3.3-3
h_{FE} VS I_C (Medium geometry device)	3.3-4

TITLE	FIGURE
h_{FE} VS I_C (Triple emitter device)	3.3-5
V_{CE} (sat) VS I_C $\frac{I_C}{I_B}$ = 1 T = 25°C	3.3-6
V_{CE} (sat) VS I_C $\frac{I_C}{I_B}$ = 10 T = 125°C	3.3-7
V_{CE} (sat) VS I_C $\frac{I_C}{I_b}$ = 1 T = +125°C	3.3-8
V_{CE} (sat) VS I_C $\frac{I_C}{I_B}$ = 10 T = +125°C	33.-9
V_{CE} (sat) VS I_C $\frac{I_C}{I_B}$ = 1 T = -55°C	3.3-10
V_{CE} (sat) VS I_C $\frac{I_C}{I_B}$ = 10 T = -55°C	3.3-11
αI VS I_B	3.3-12
f_t VS I_C	3.3-13
Storage Time VS I_C/I_B	3.3-14
Breakdown Voltages VS Temperature	3.3-15
Resistance VS Resistor Voltage	3.3-16
Resistance VS Temperature	3.3-17

3.3.3 Multigate Array Performance

3.3.3.1 Performance Analysis

Performance of the proposed Driver and Standard Gate configurations has been computer simulated using the SCEPTRE nonlinear circuit analysis program. Breadboard testing has been performed to verify 25°C static simulations. Temperature extreme and transient response

FIGURE 3.3-1

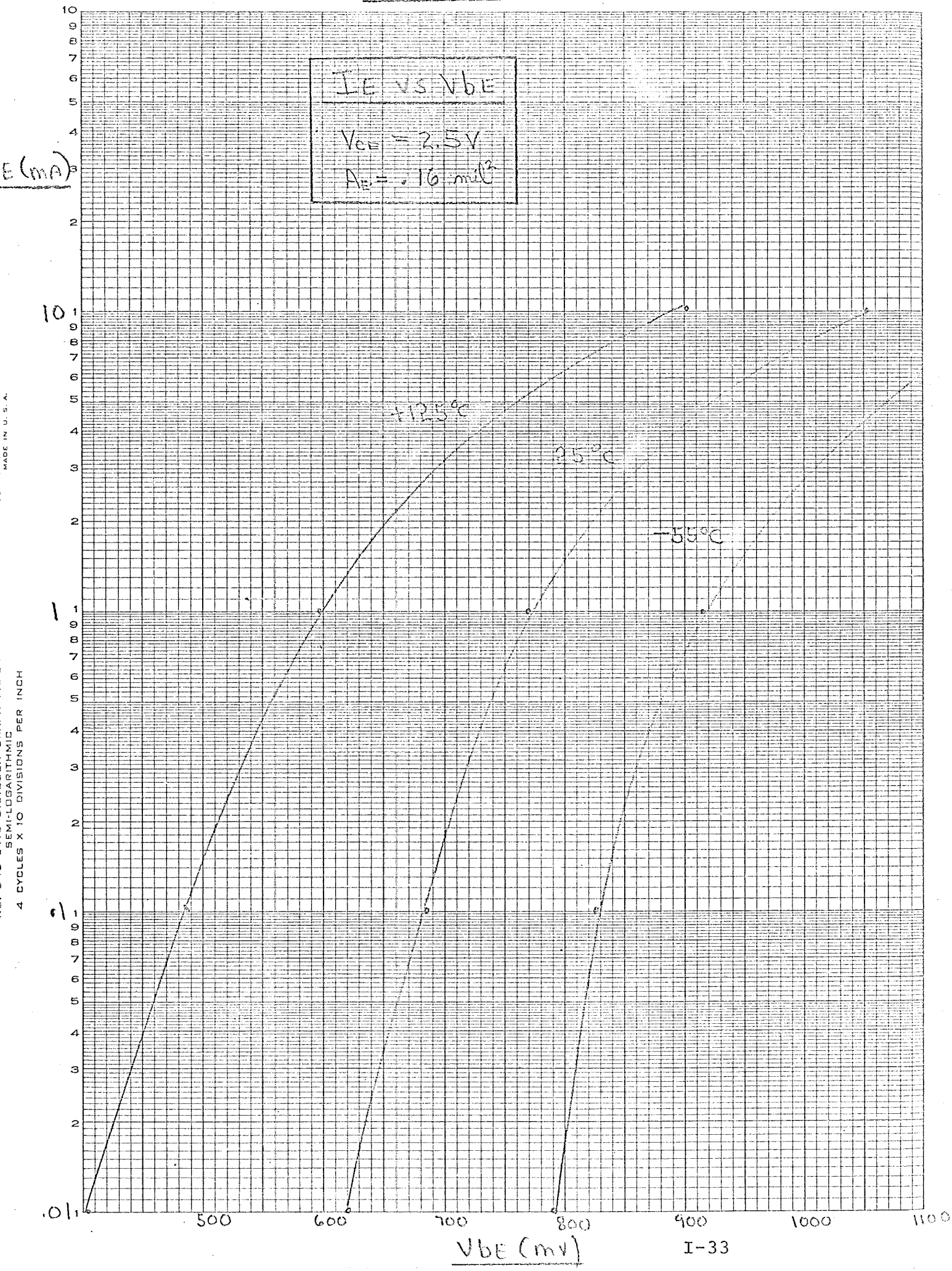

IE vs VbE
VCE = 2.5V
AE = .16 mil²
IE (mA)
+125°C
25°C
-55°C
VbE (mV)
500
600
700
800
900
1000
1100
10
1
.01
MADE IN U.S.A.
SEMI-LOGARITHMIC
4 CYCLES X 10 DIVISIONS PER INCH

FIGURE 5.5-2

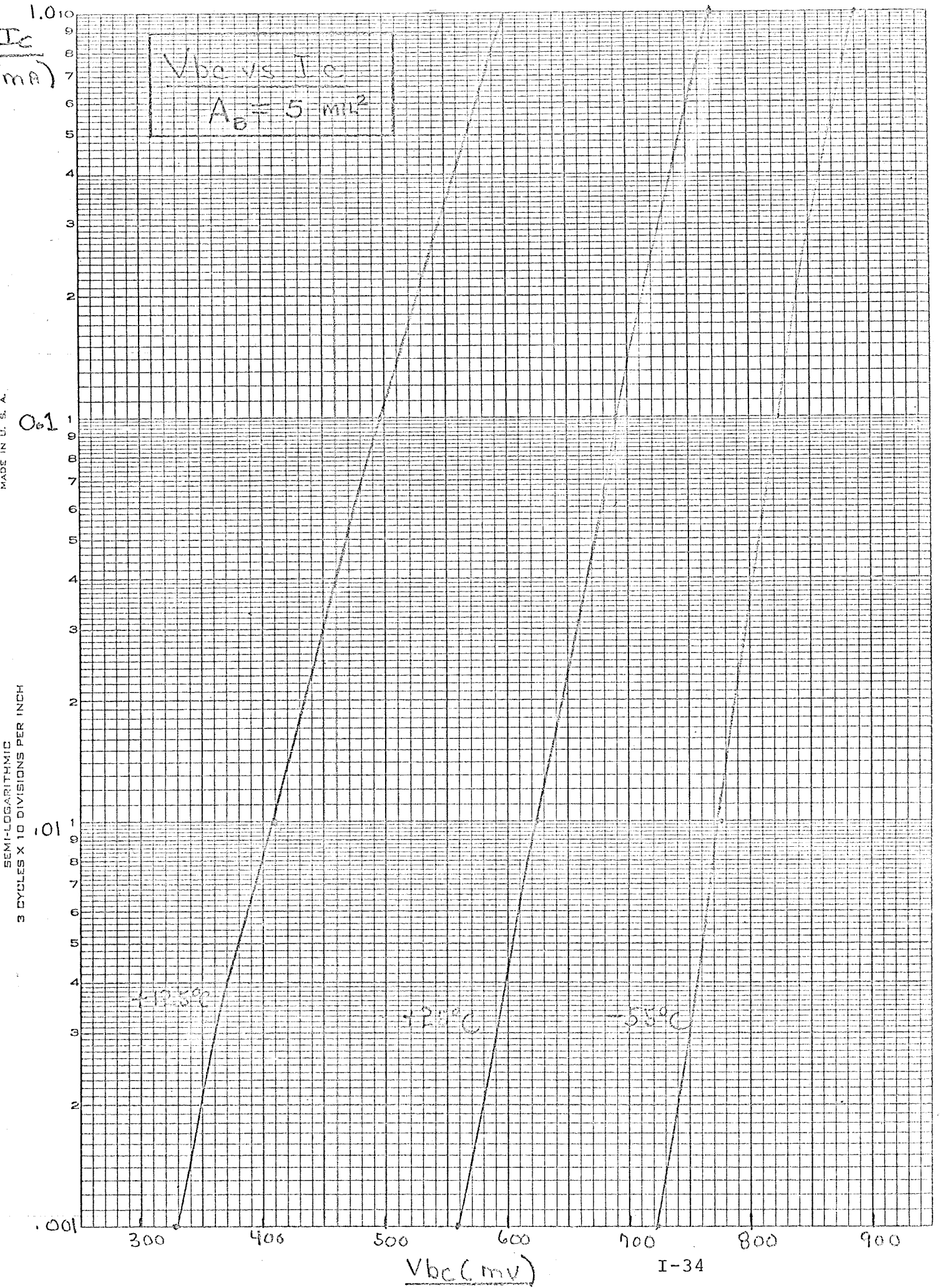
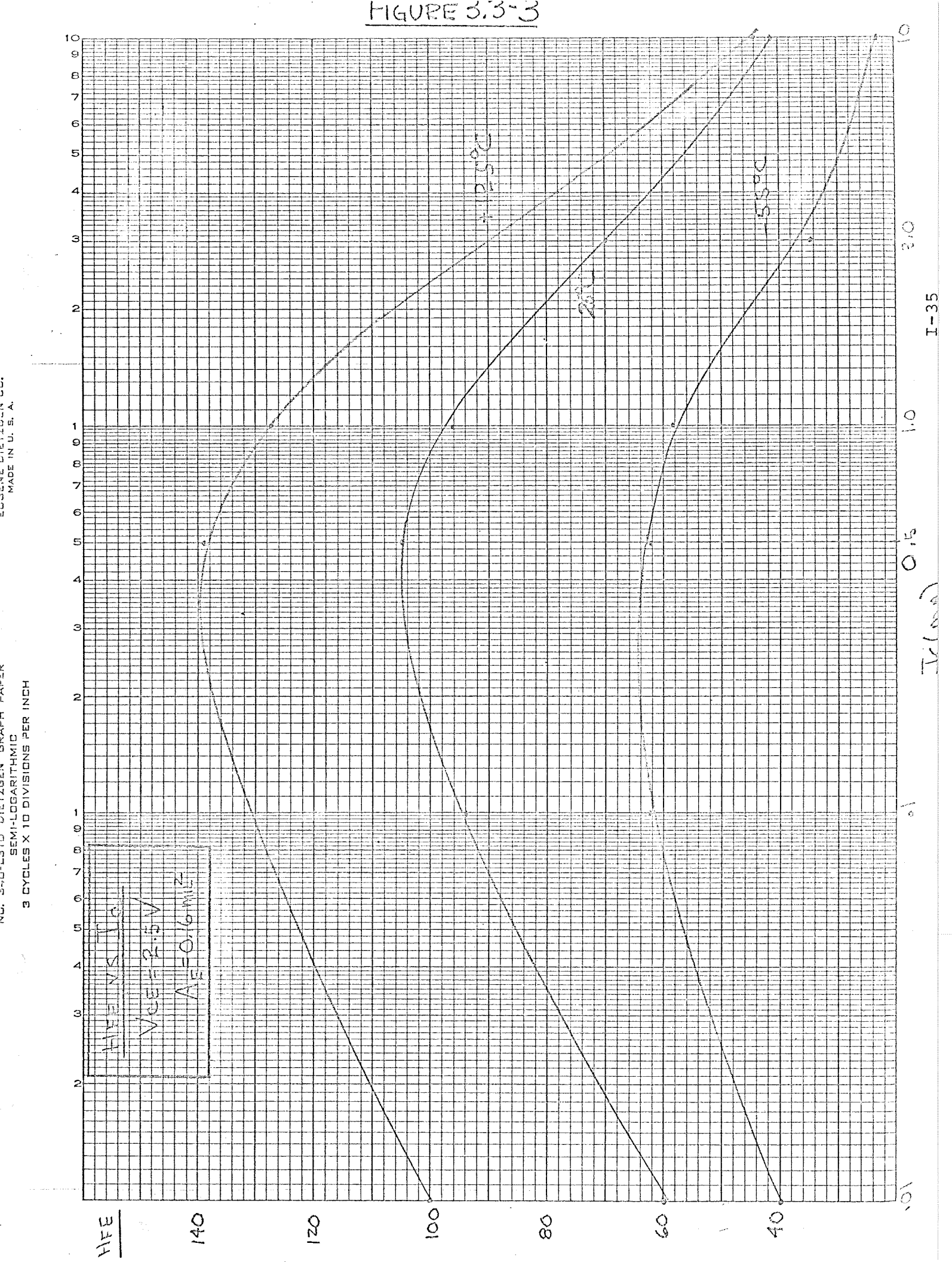
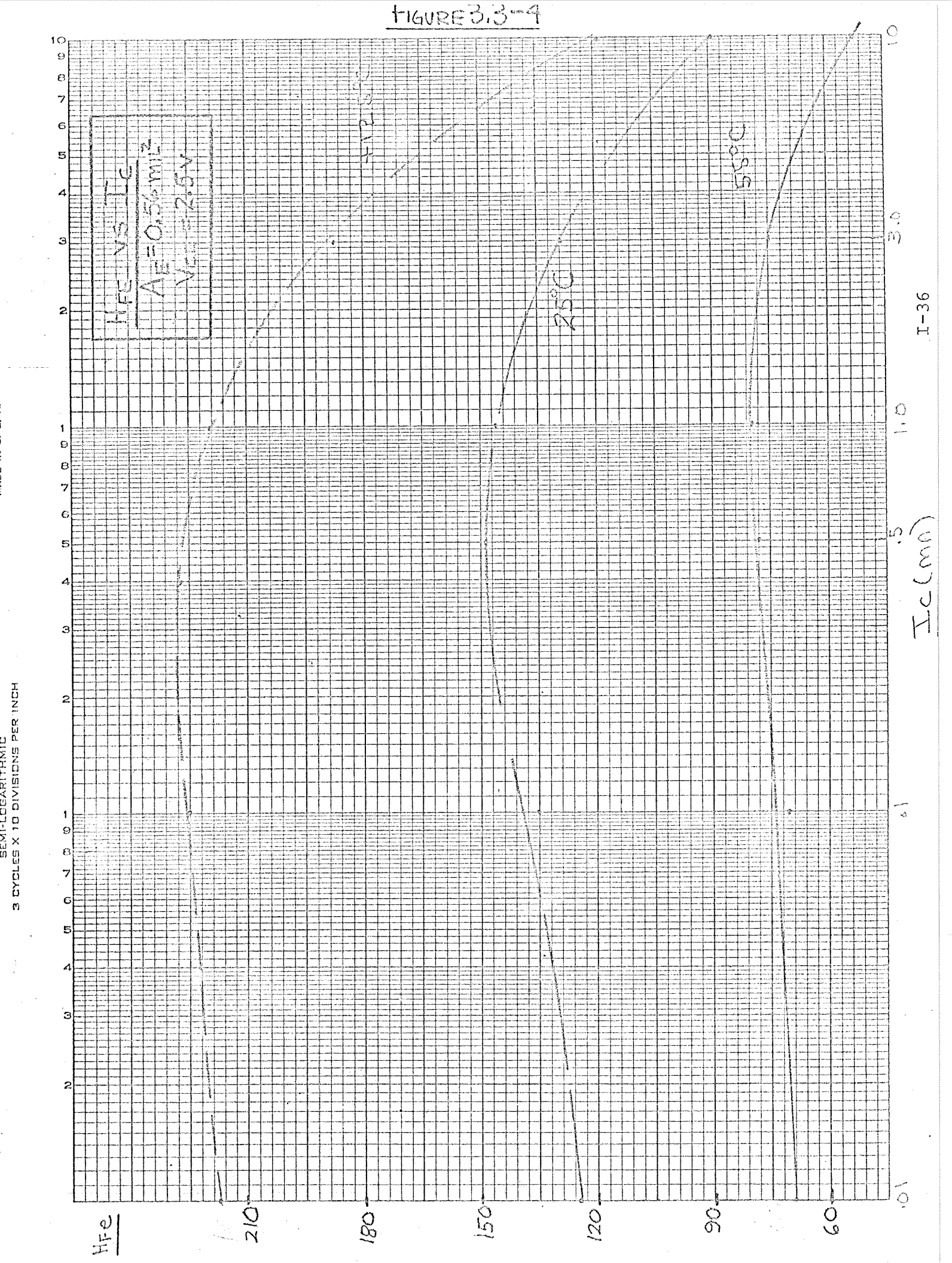

Vbc vs Ic
$A_E = 5$ mil^2
Ic (mA)
1.0
0.1
.01
.001
300
400
500
600
700
800
900
Vbc (mv)
-125°C
+25°C
-55°C
MADE IN U. S. A.
SEMI-LOGARITHMIC
3 CYCLES X 10 DIVISIONS PER INCH

FIGURE 3.3-3



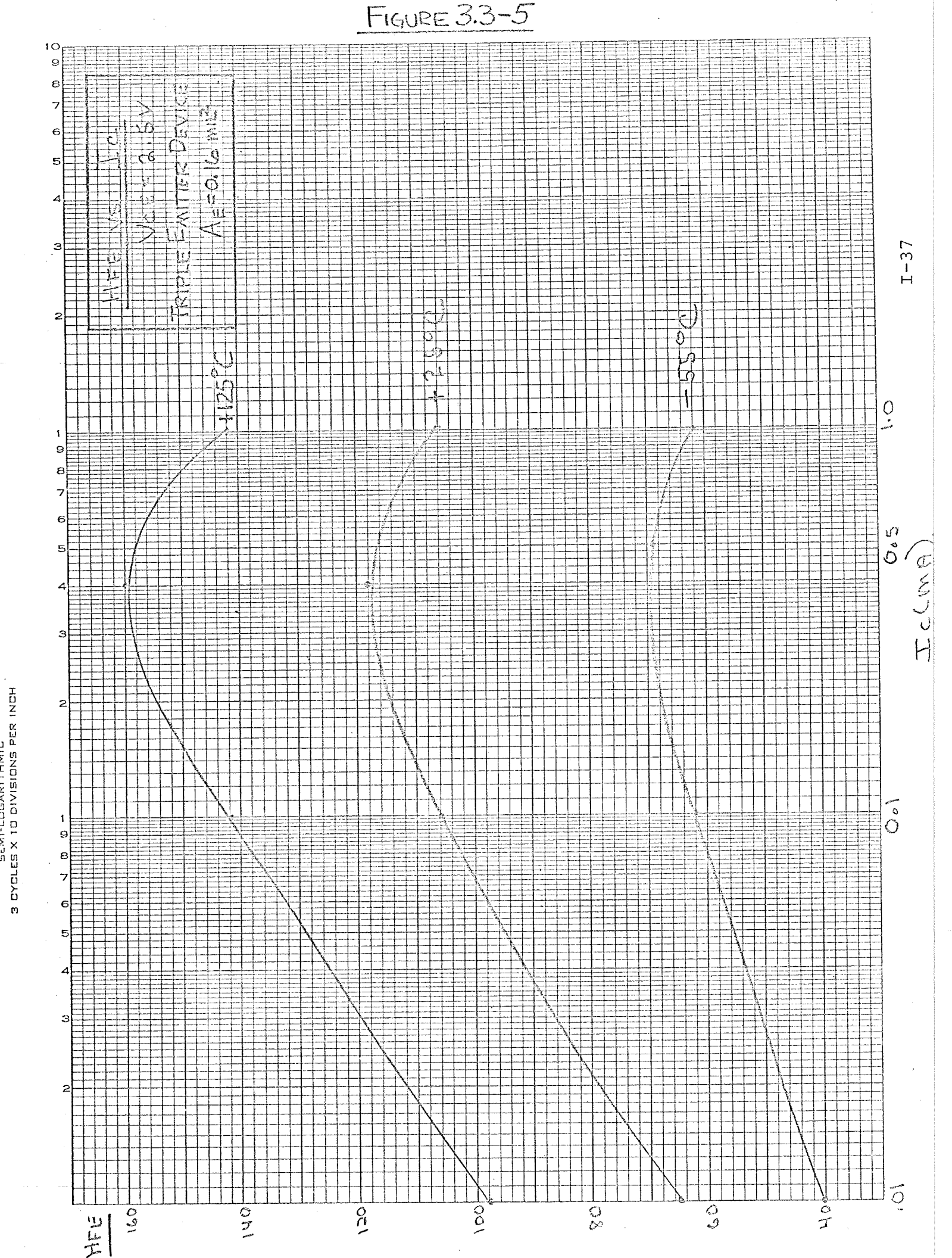
I-35

FIGURE 3.3-4



SEMI-LOGARITHMIC
3 CYCLES X 10 DIVISIONS PER INCH

FIGURE 3.3-5



SEMI-LOGARITHMIC
3 CYCLES X 10 DIVISIONS PER INCH

SEMI-LOGARITHMIC
3 CYCLES X 10 DIVISIONS PER INCH

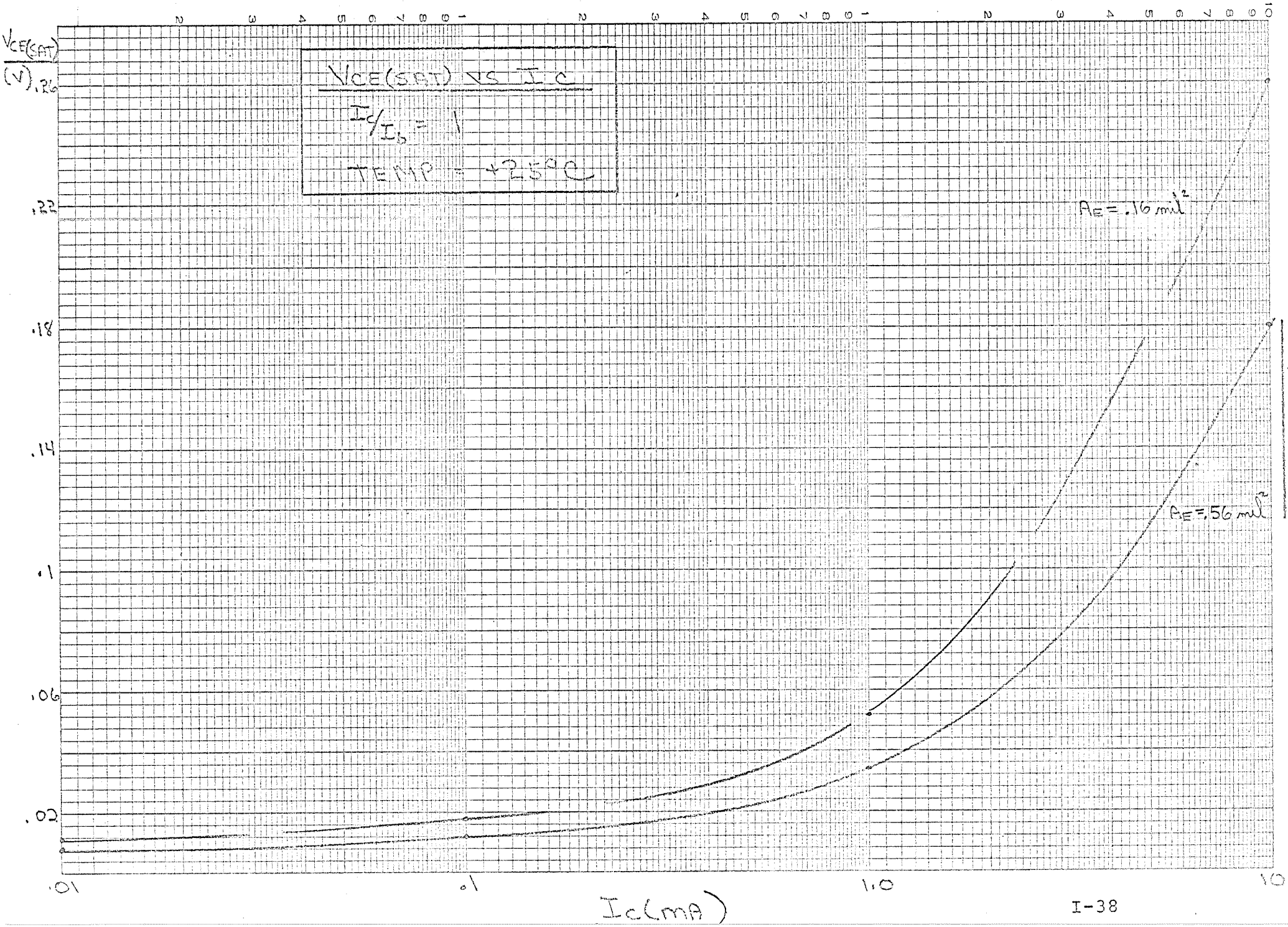
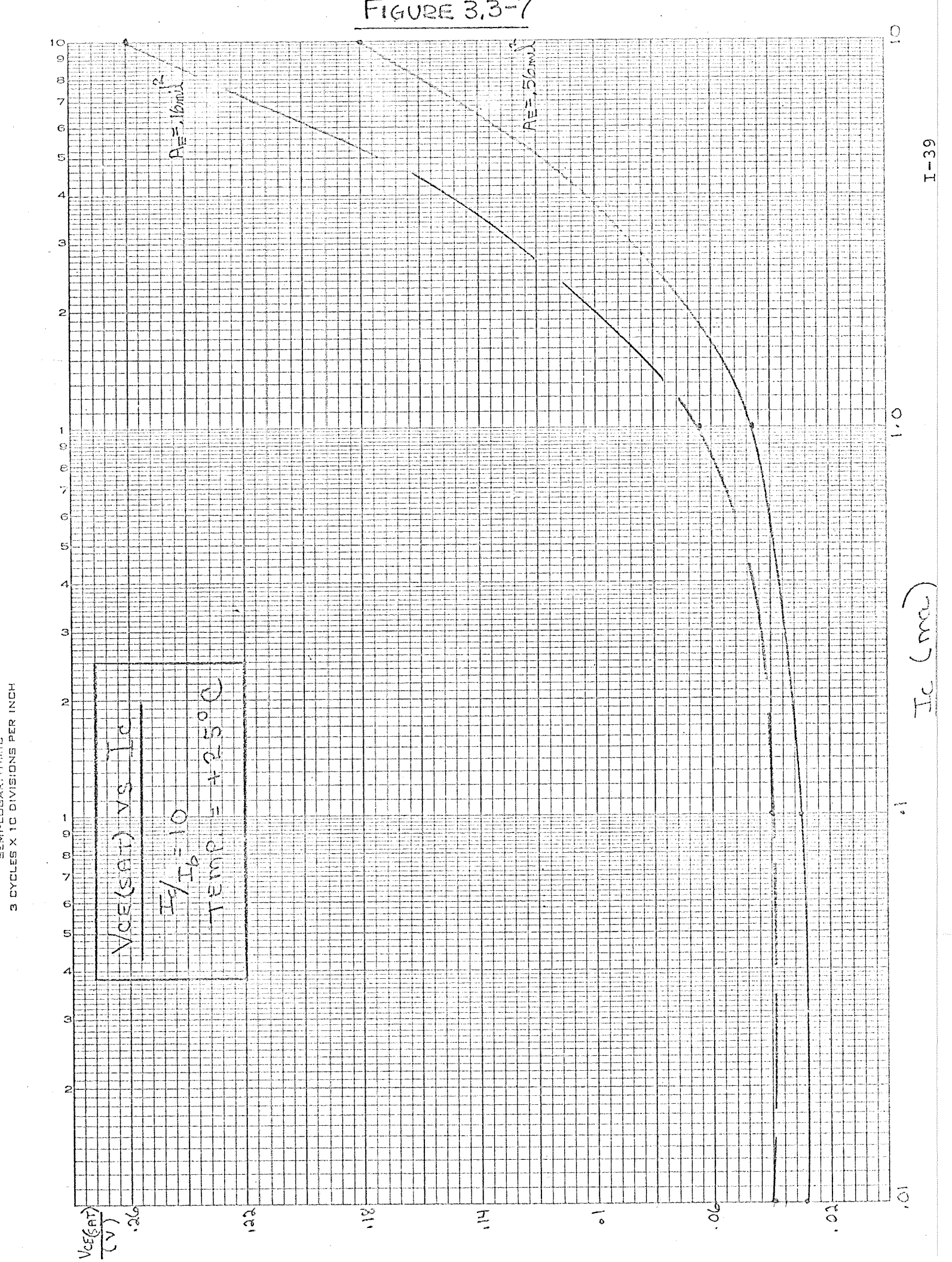
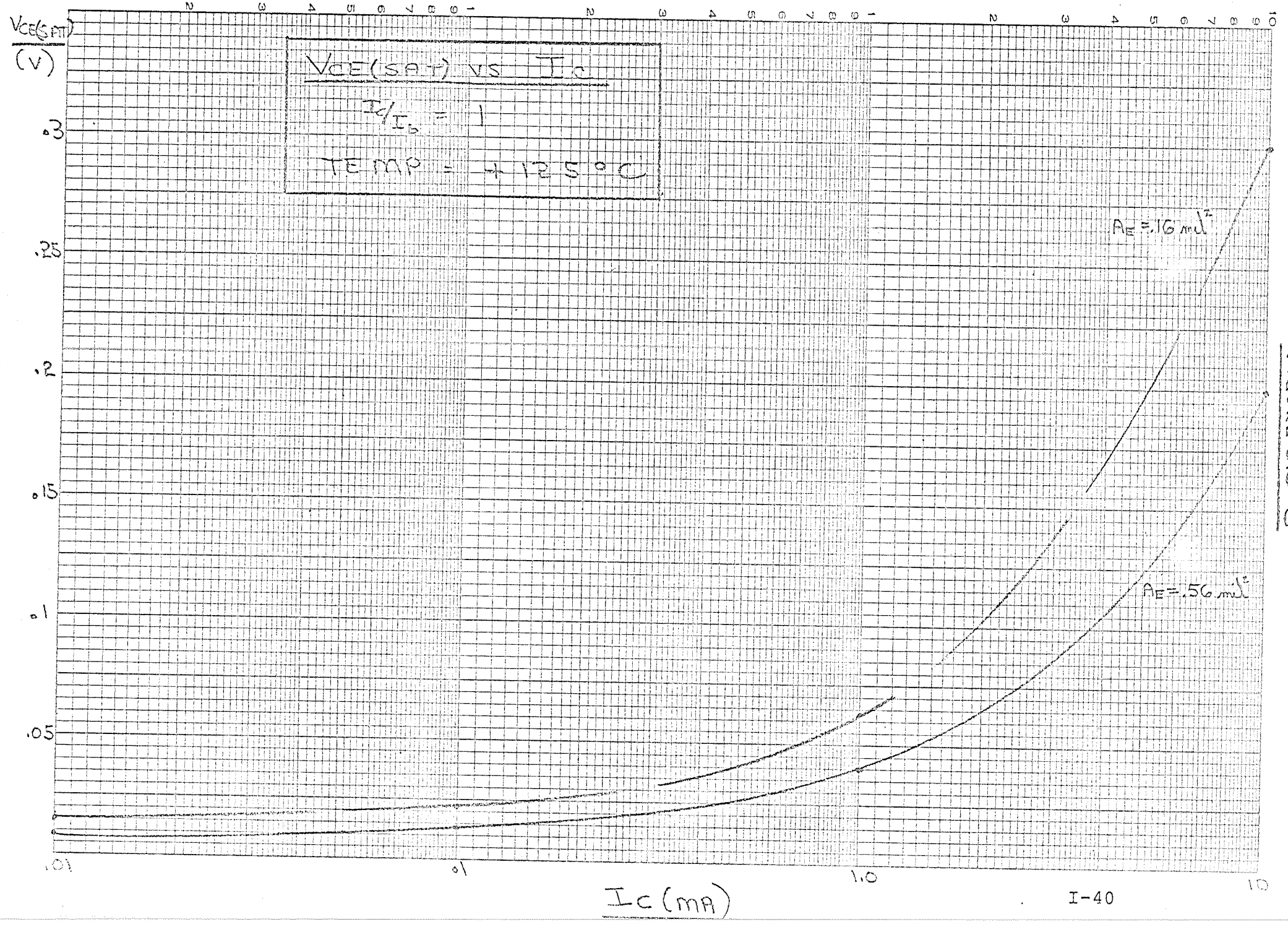


FIGURE 3.3-6

FIGURE 3.3-7


$V_{CE(SAT)}$ vs I_C
$I_C/I_b = 10$
Temp. = +25°C
$A_E = .16 mil^2$
$A_E = .56 mil^2$
$V_{CE(SAT)}$ (V)
.26
.22
.18
.14
.1
.06
.02
.01
.1
1.0
10
I_C (mA)
SEMILOGARITHMIC
3 CYCLES X 10 DIVISIONS PER INCH

3 CYCLES X 10 DIVISIONS PER INCH



3 CYCLES X 10 DIVISIONS PER INCH

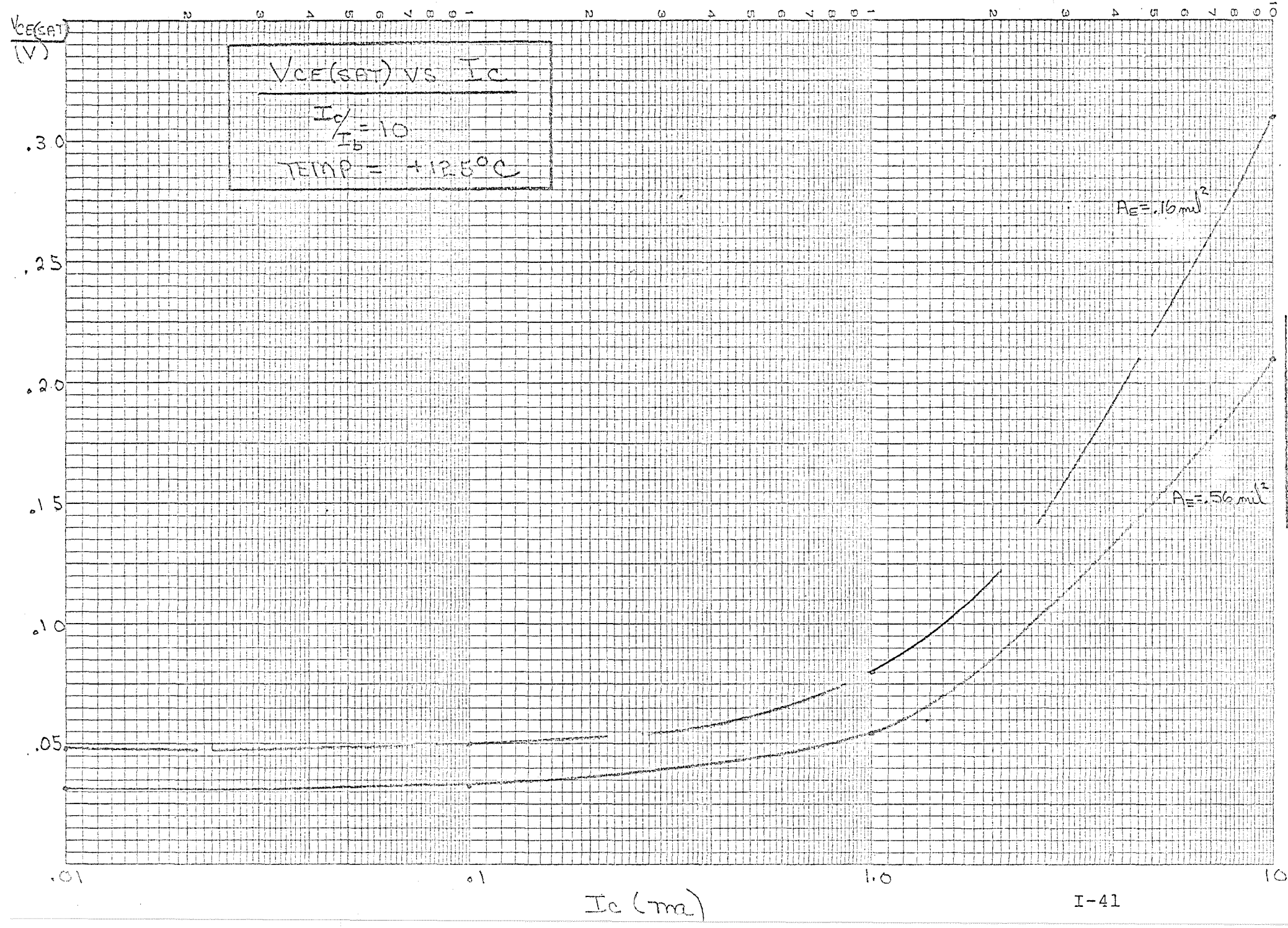
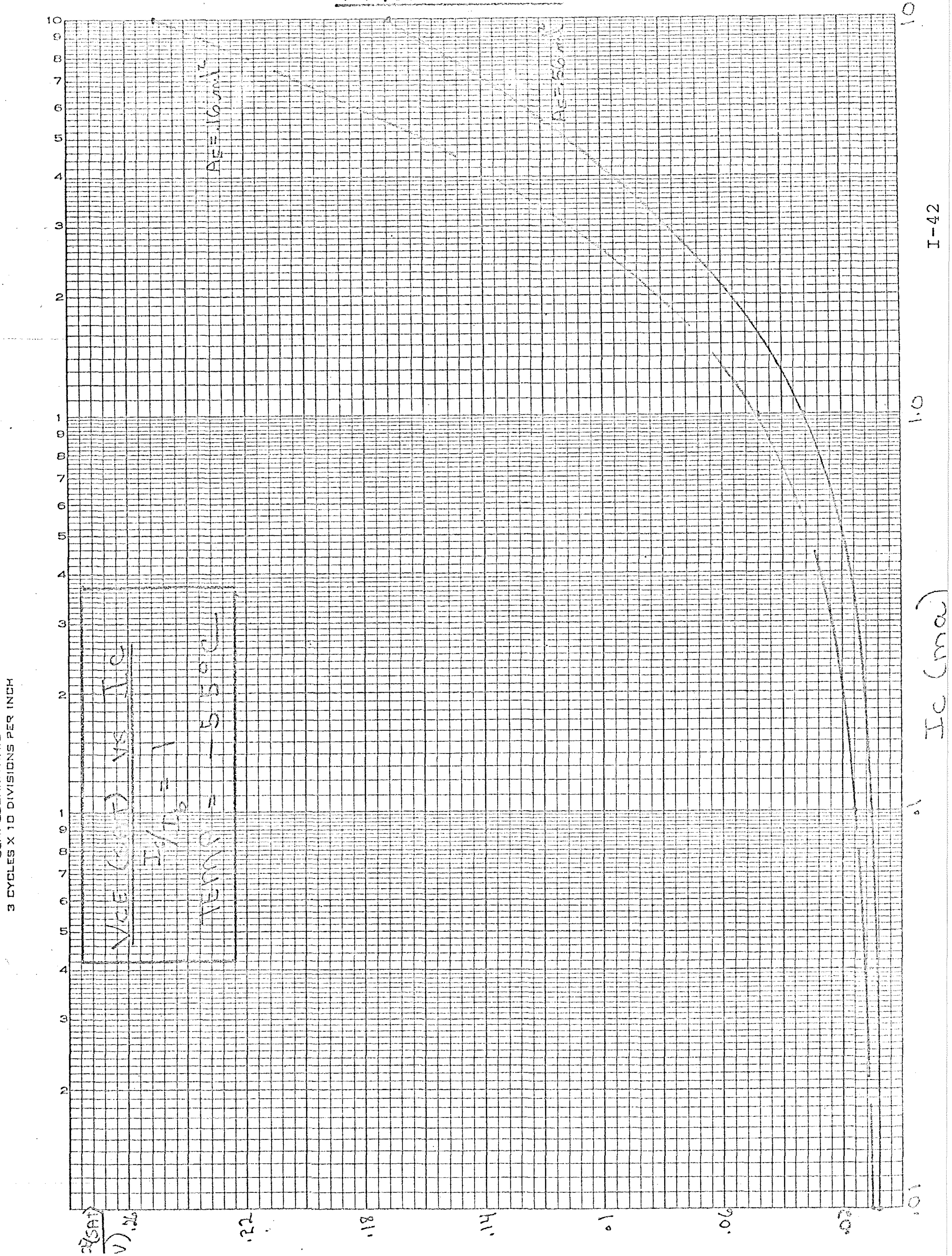


FIGURE 2.3-6

FIGURE 3.3-10



Vce (sat) vs Ic
TEMP = -55°C
Ic (ma)
.01
.1
1.0
10
.02
.06
.1
.14
.18
.22
.26
SEMI-LOGARITHMIC
3 CYCLES X 10 DIVISIONS PER INCH
MADE IN U. S. A.

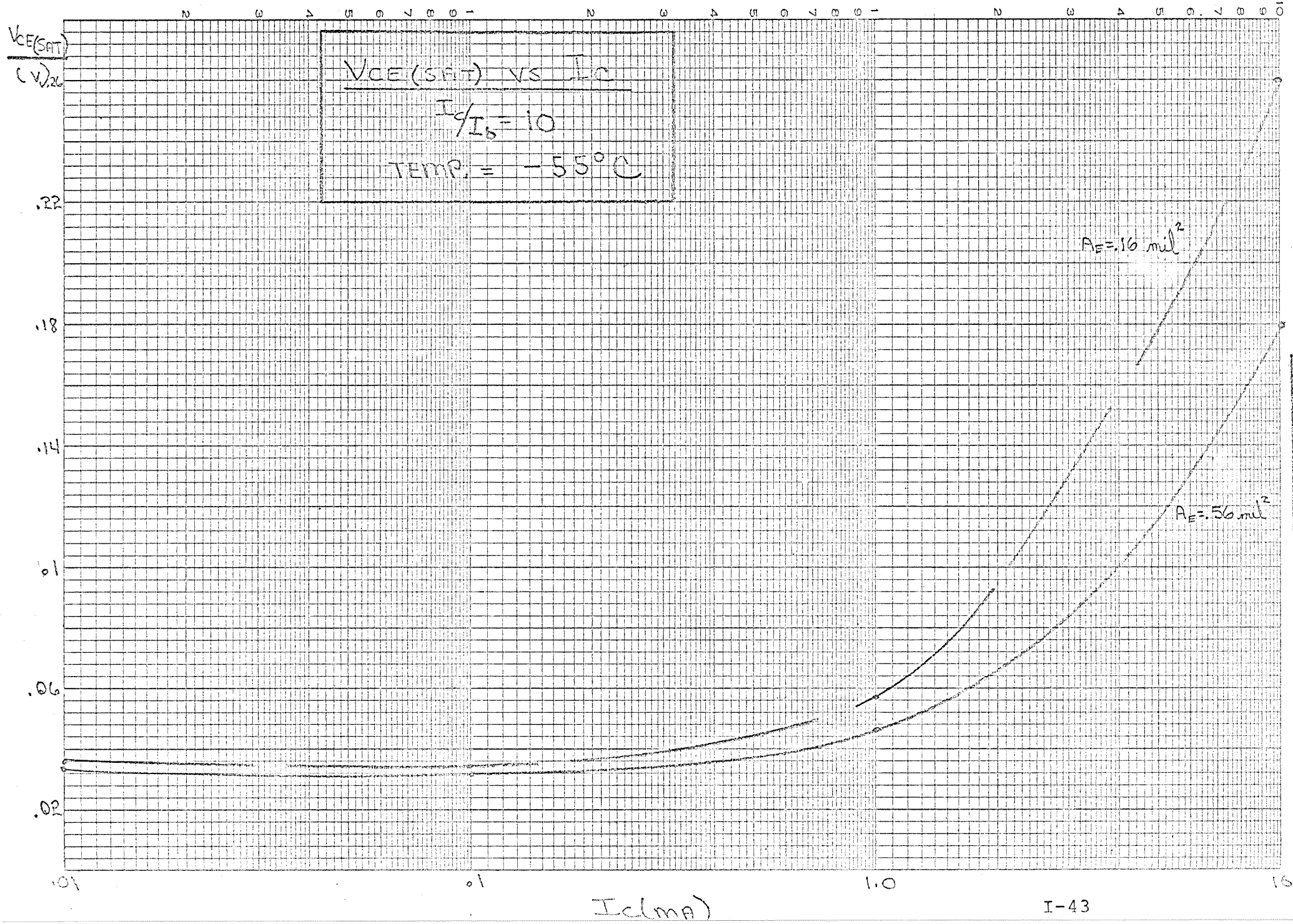


FIGURE 3.3-11

FIGURE 3.3-12

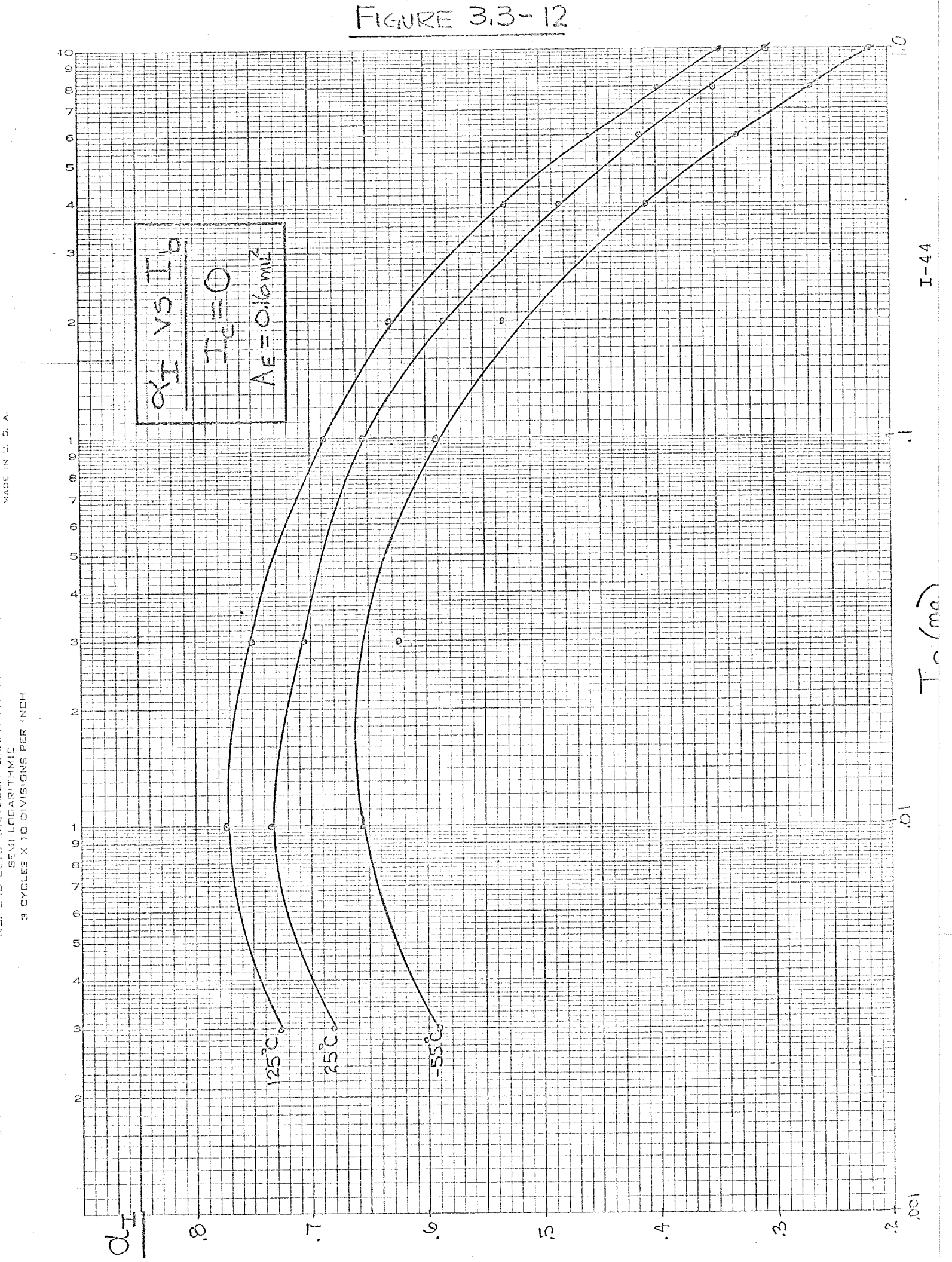
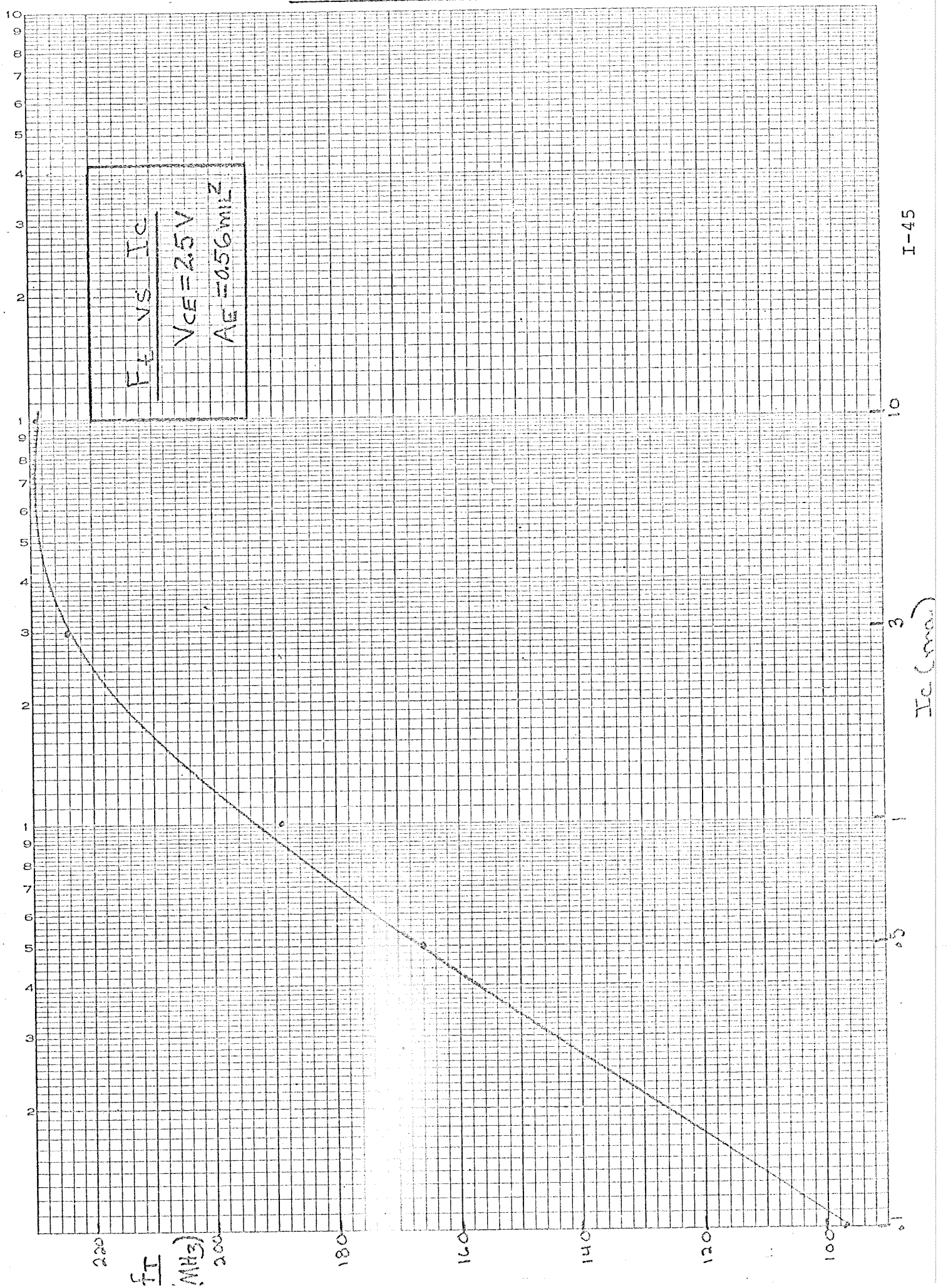

α_T vs t_b
T_C = 0
A_E = 0.16 mil^2
125°C
25°C
-55°C
α_T
.8
.7
.6
.5
.4
.3
.2
.1
.01
.001
T_b (ms)
MADE IN U. S. A.
SEMI-LOGARITHMIC
3 CYCLES X 10 DIVISIONS PER INCH

FIGURE 3.3-13


ft VS Ic
VCE = 2.5 V
AE = 0.56 mil²
SEMI-LOGARITHMIC
3 CYCLES X 10 DIVISIONS PER INCH
ft (MHz)
Ic (mA)
220
200
180
160
140
120
100
10
3
1
.5
.1

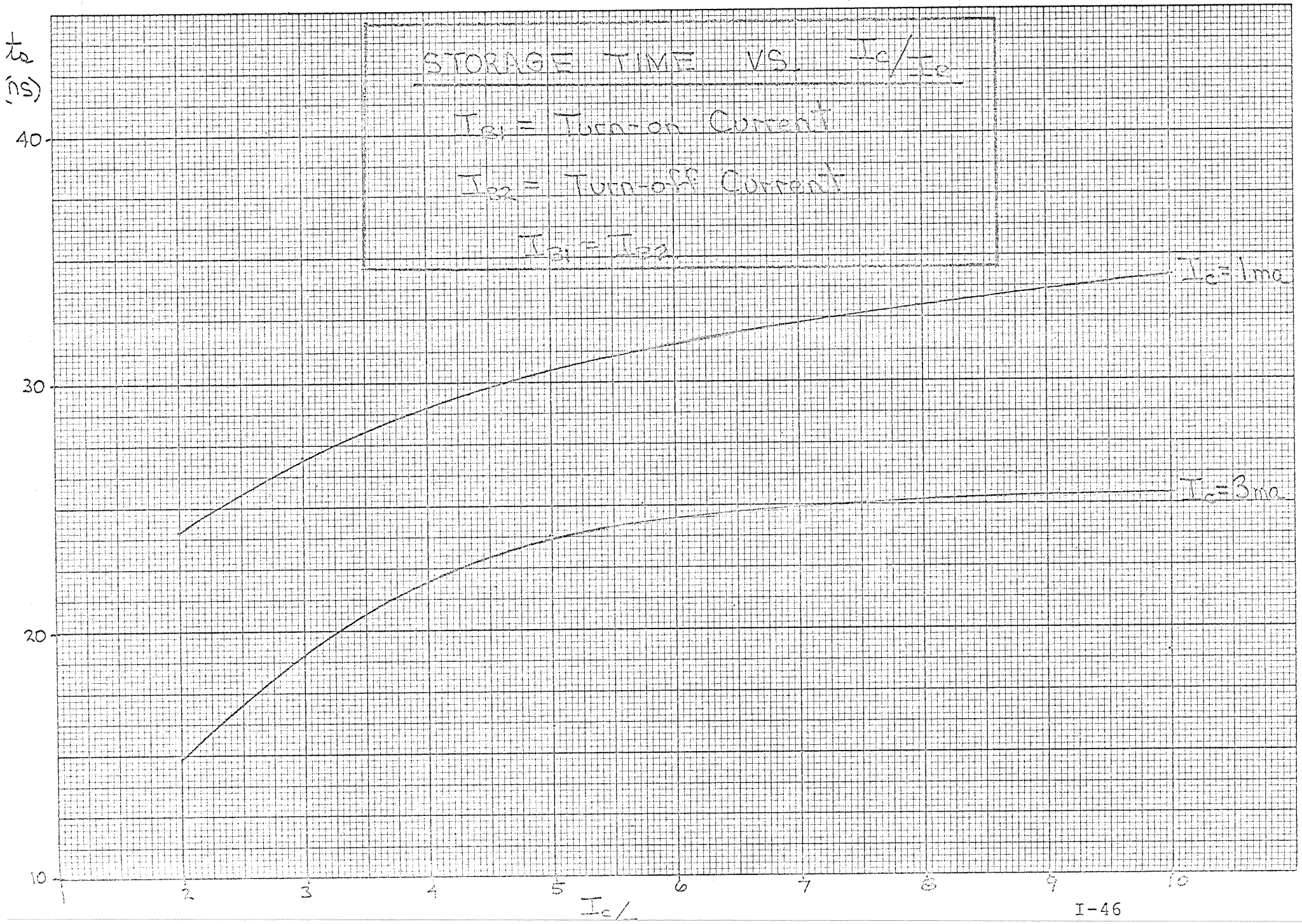


FIGURE 3.3-14

FIGURE 3.3-15

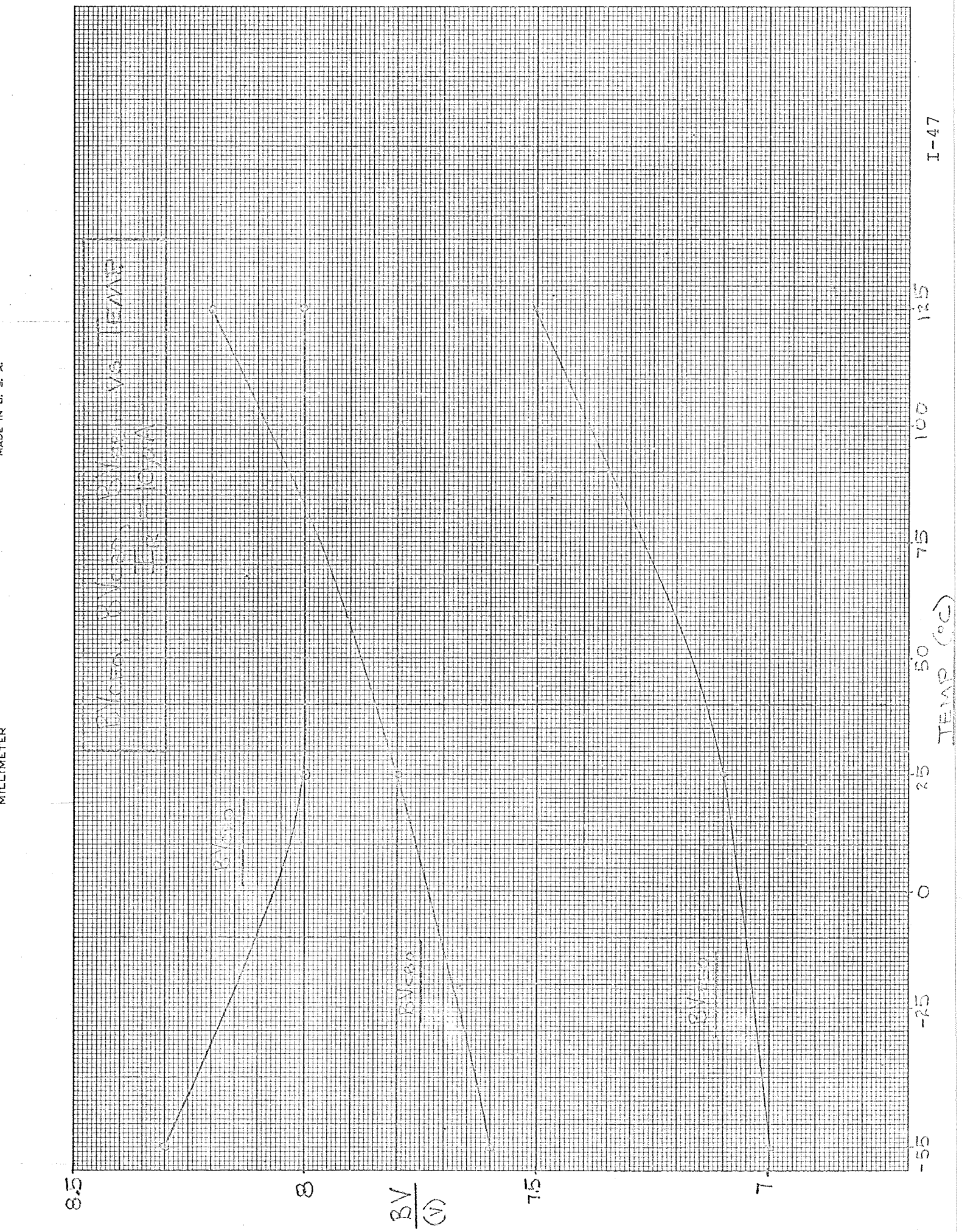
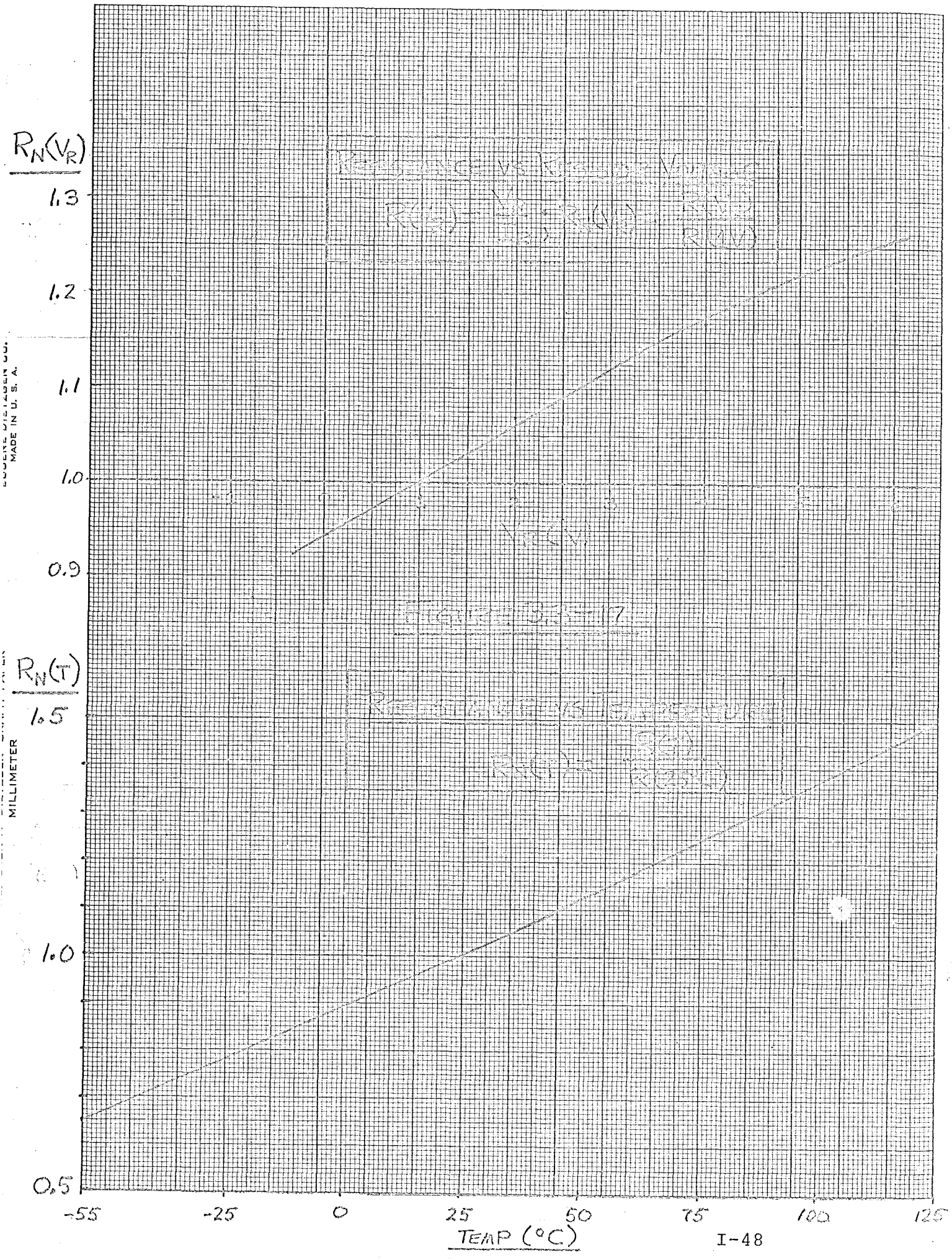


FIGURE 3.3 -16



breadboard verifications have not been performed. Circuit simulations performed include: (1) V_{in} vs V_{out} response at all combinations of nominal and extreme temperature, power supply voltage, and fan-out. (Figures 3.3-19 through 3.3-36) (2) Output low voltage (V_{ol}) vs output low current (I_{ol}) for all combinations of nominal and extreme temperature for nominal and extreme power supply voltage (Figures 3.3-46 and 3.3-51). (4) Propagation delay at maximum fan-out and nominal supply voltage for +25°C, -55°C, and +125°C (Figures 3.3-52 through 3.3-60).

Driver gate characteristics which are defined by these simulations include: (1) Input threshold voltage and noise margin; (2) Fan-out and logical "0" output level; (3) "0" and "1" state supply current and power dissipation; and (4) propagation delay.

3.3.3.2 Standard Gate Performance

The standard gate circuit configurations were constrained to satisfy the prime electrical design objective of power consumption at $V^+ = 5.0V$ and T = 25°C. The design objective and resultant nominal performance were as follows:

	Design Objective	Standard Gate 1	Standard Gate 2
P_D (0)	0.50mW	0.30mW	0.43mW
P_D (1)	0.20mW	0.38mW	0.19mW
P_D (avg)	0.35mW	0.34mW	0.31mW

Both gate configurations then satisfy the design objective average power dissipation while Standard Gate 2 more

closely satisfies the P_D (0) and P_D (1) objective. The division of power between "0" and "1" states was selected to optimize other performance parameters.

Noise immunity requirements in effect constrain the "0" and "1" worst-case input logic levels to 0.8V and 2.0V respectively. From V_{in} vs V_{out} data, these requirements may be evaluated by considering the maximum "0" input level V_{IL} (max) resulting in a minimum output "1" level of 2.4V. (This condition is more severe than the converse case of minimum "1" input level and maximum "0" output level). This data for the two standard gate configurations at worst-case fan-out = 1 is summarized below.

	V^+=5.5V			V^+=5.0V			V^+=3.6V		
	-55°C	25°C	+125°C	-55°C	25°C	+125°V	-55°C	25°C	+125°V
Std Gate 1									
V_{IL}(max) (V)	1.05	0.93	0.74	1.03	0.88	0.68	0.94	0.82	0.62
Std Gate 1									
V_{IL}(max) (V)	1.02	0.89	0.70	1.00	0.85	0.67	0.87	0.75	0.56

As is apparent both gates are sub-marginal at +125°C and have a small margin under all conditions. Standard gate 2 is also sub-marginal at V^+ = 3.6V.

Fan-out requirement is a fan-out of 12 standard loads. From V_{in} vs V_{out} data, both gates meet the fan-out requirements under all conditions except standard gate 1 at V+ = 3.6V and T = -55°C. To define a fan-out margin,

V_{OL} vs I_{OL} data is compared to the required fan-out current for each gate under the appropriate conditions. Specifically, the required maximum fan-out current I_{FO} (max) is compared to the output current I_{OL} (max) for which the output voltage is V_{OL} (max) = 0.4V.

	V^+=5.5V			V^+=5.0V			V^+=3.6V		
	-55°C	25°C	+125°C	-55°C	25°C	+125°C	-55°C	+25°C	+125°C
Std Gate 1									
I_{FO} (max) (mA)	1.46	1.02	0.72	1.32	0.91	0.62	0.86	0.60	0.42
I_{OL} (max) (mA)	>2	>3	3.7	>2	1.70	2.90	0.57	0.57	1.45
Std Gate 2									
I_{FO} (max) (mA)	0.86	0.51	0.35	0.68	0.46	0.30	0.67	0.33	0.22
I_{OL} (max) (mA)	>3	>5	>5	>3	>4	>5	>1	>2	>3

In most cases the computer simulations were terminated prior to V_{OL} = 0.4V, but in these instances it is apparent that an adequate fan-out margin exists. The only fan-out problem noted is for Standard gate 1 at V^+ = 3.6V and 25°C $\leq$ T $\leq$ -55°C. In all cases it is noted that Standard Gate 2 has superior fan-out capability to Standard Gate 1.

Considering propagation delay for the Standard Gates, the question of operating conditions for optimum performance immediately arises. If a pull-up resistor is employed which pulls the output up to the positive supply, propagation delays are completely unsatisfactory as a result of the delay time required to pull the output down from the positive supply to the threshold level. In multiple fan-out cases however, a pull-up resistor will be required to charge load capacitance under worst-case logic condi-

tions. Considering these two factors, the recommended approach is a clamped pull-up resistor in the Extender/ Pull-Up Cell as described previously and as shown in Figures 3.2-5 and 3.2-9. This technique of clamping the pull-up at three forward diode voltages can be employed to optimize internal propagation delays. If desired of course the clamp diodes need not be employed, to provide a high level external interface for example.

With this approach, however, the problem of defining and specifying Standard Gate propagation delay arises. This question cannot be resolved at this time, but for purposes of this report the following approach was employed. Propagation delays were simulated using the test configuration of Figure 3.1-1 with maximum fan-out. Propagation delays were determined from the computer simulations as the time interval between initiation of the input pulse and transition of the output to the output level necessary to produce a maximum "0" output level (0.4V) or minimum "1" output level (2.4V) when this level is applied to an identical gate. The required voltage levels were determined from V_{in} vs V_{out} data. This propagation delay definition is obviously arbitrary but is a measure of Standard Gate transient response. With this definition and under conditions of maximum fan-out, $V^+ = 5V$, simulated Standard Gate propagation delays (in nanoseconds) are as summarized below.

	-55°C		+25°C		+125°C	
	t_{pdl}	t_{pdo}	t_{pdl}	t_{pdo}	t_{pdl}	t_{pdo}
Std. Gate 1	67	35	70	50	58	39
Std. Gate 2	105	45	165	55	260	46

As is apparent from this data, Standard Gate 1, while slower than the objective specification for t_{pdl}, is significantly superior to Standard Gate 2 for both t_{pdl} and t_{pdo}.

3.3.3.3 Driver Gate Performance

The Driver Gate circuit configuration was also constrained to satisfy the prime electrical design objective of power consumption at $V^+ = 5.0V$ and $T = 25^oC$. Design objective and resultant nominal performance are as follows:

	Design Objective	Driver Gate
$P_D(0)$ (mW)	2.0	2.08
$P_D(1)$ (mW)	0.80	0.76
$P_D(avg)$ (mW)	1.40	1.41

Thus Driver Gate nominal power dissipation is in accord with design objectives.

Noise immunity requirements for the Driver Gate lead to similar considerations as for the Standard Gate for worst-case input logic levels of 0.8V and 2.0V for "0" and "1" levels respectively. From V_{in} vs V_{out} data, worst-case condition is again the maximum "0" input level, V_{IL} (max), resulting in a minimum "1" output level of 2.4V. This

data is summarized below for the worst-case condition of fan-out = 1.

	$V^+ = 5.5V$			$V^+ = 5.0V$			$V^+ = 3.6V$		
	-55^oC	$+25^oC$	$+125^oC$	-55^oC	$+25^oC$	$+125^oC$	-55^oC	$+25^oC$	$+125^oC$
Driver Gate									
V_{IL}(max) (V)	1.12	1.01	0.94	1.06	0.97	0.81	0.91	0.78	0.60

From this data, it is seen that a small margin exists for $V^+ \geq 5,0V$ while performance at $V^+ = 3.6V$ is sub-marginal at high-temperature.

Fan-out requirement for the Driver Gate is 50 standard loads. Assuming Standard Gate 1 defines fan-out requirements which is worst-case, the required fan-out current, I_{FO}(max), can be compared to the available output low current, I_{OL}(max), for which the output voltage is V_{OL} (max) = 0.4V.

	$V^+ = 5.5V$			$V^+ = 5.0V$			$V^+ = 3.6V$		
	-55^oC	$+25^oC$	$+125^oC$	-55^oC	$+25^oC$	$+125^oC$	-55^oC	$+25^oC$	$+125^oC$
Driver Gate									
I_{FO}(max) (mA)	6.09	4.25	3.00	5.50	3.79	2.59	3.59	2.50	1.75
I_{OL}(max) (mA)	>10	>10	>10	>10	>10	>10	>10	>10	>10

The V_{OL} vs I_{OL} computer simulations were terminated at I_{OL} = 10mA, but it is apparent that adequate fan-out margin exists for all conditions.

Considering propagation delay, a similar problem exists for the Driver Gate as for the Standard Gate in terms of

specifying and defining propagation delay. Since a principal application of the Driver Gate will be to provide an external interface with conventional TTL devices, a conventional definition will be employed in this report. Propagation delay is defined as the time interval between initiation of the input pulse and transition of the Driver Gate output to a defined threshold voltage. The defined threshold voltages are assigned as V_{TH} = 1.6V (-55°C), V_{TH} = 1.3V (25°C), and V_{TH} = 1.0V (+125°C) to approximately account for the shift in threshold with temperature. This data (in nanoseconds) is obtained from the propagation delay simulations under conditions of maximum fan-out and V^+ = 5.0V and is summarized below.

	-55°C		+25°C		+125°V	
	t_{pdl}	t_{pdo}	t_{pdl}	t_{pdo}	t_{pdl}	t_{pdo}
Driver Gate	52	35	74	40	100	45

From this data, it is seen that t_{pdl} objectives are not met and that t_{pdo} objectives are exceeded.

3.3.3.4 Post-Radiation Performance

Computer simulations of circuit performance with post-radiation parameters has not yet been performed. Before this work can be performed, post-radiation device characteristics must be calculated and inserted into final circuit configurations. Post-radiation performance analysis will be performed during Phase II of this contract.

FIGURE 3.3-18

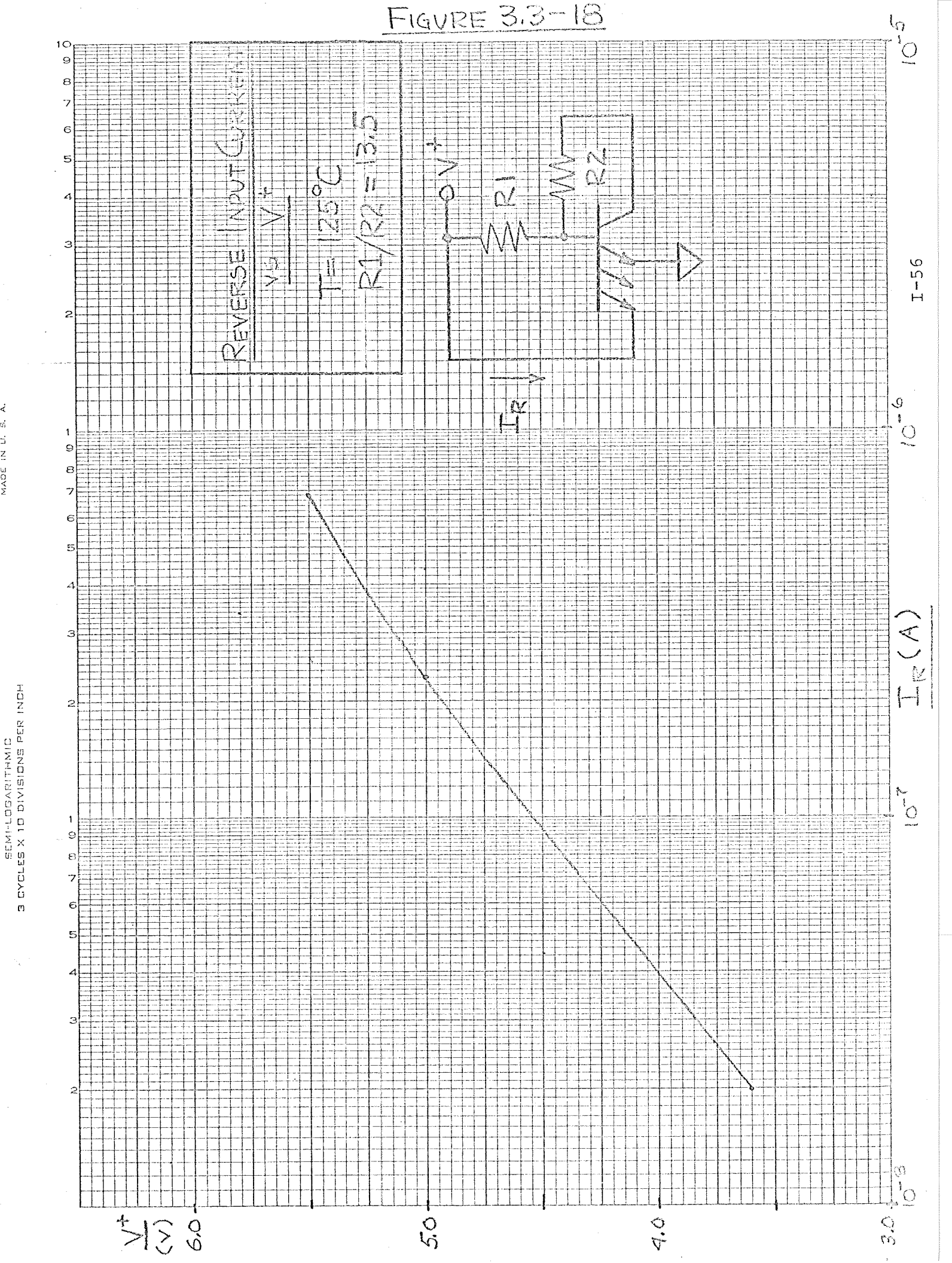

REVERSE INPUT CURRENT
VIR
V+
TE 125°C
R1/R2 = 13.5
9 V+
R1
R2
VIR
IR
10-5
10-6
10-7
10-8
IR (A)
V+ (V)
6.0
5.0
4.0
3.0
I-56
MADE IN U. S. A.
SEMI-LOGARITHMIC
3 CYCLES X 10 DIVISIONS PER INCH

FIGURE 3.3-19

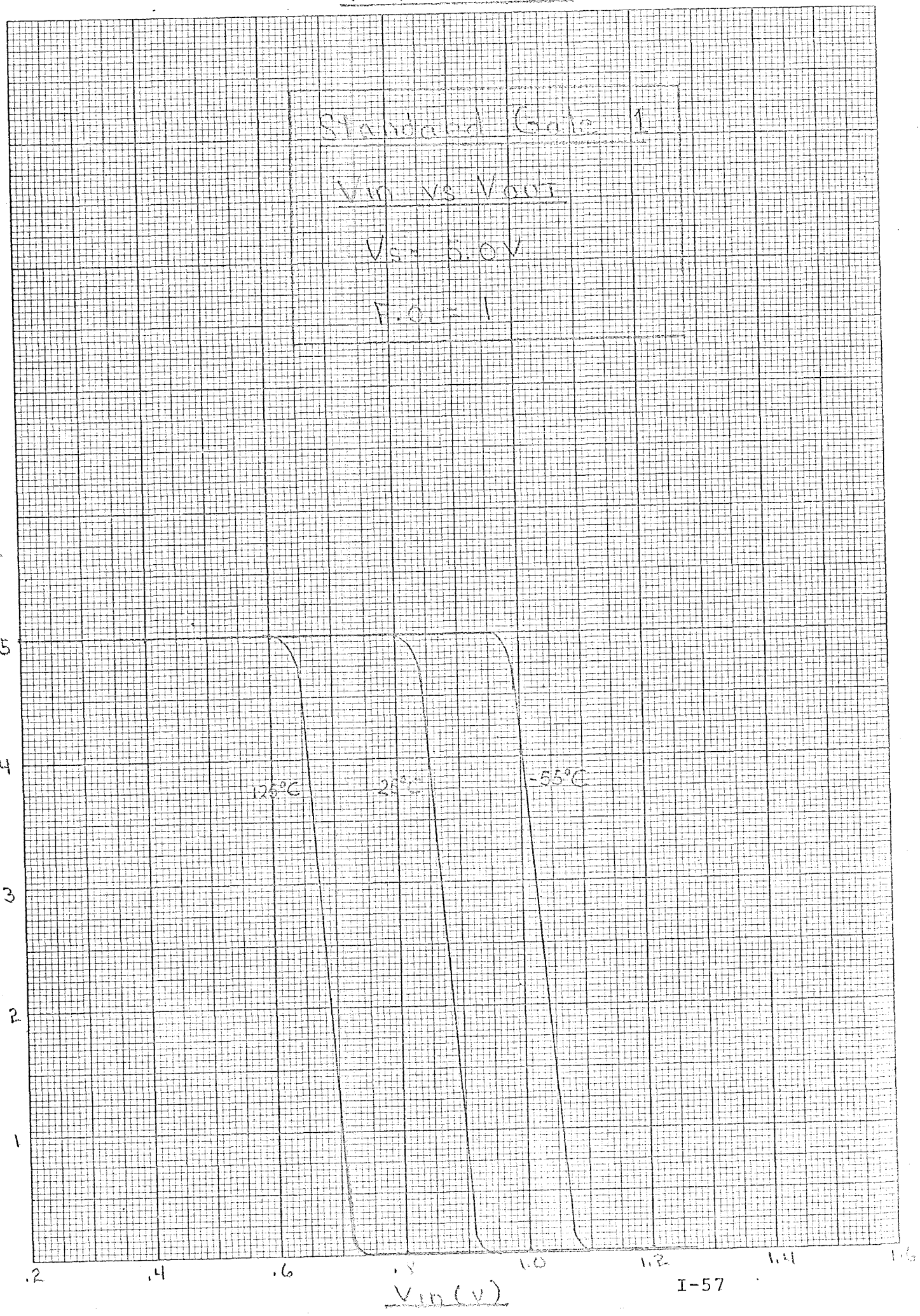

Standard Gate 1
Vin vs Vout
Vs = 5.0V
P.C. 1
Vout (V)
5
4
3
2
1
125°C
25°C
-55°C
.2
.4
.6
.8
1.0
1.2
1.4
1.6
Vin (V)

FIGURE 3.3-20

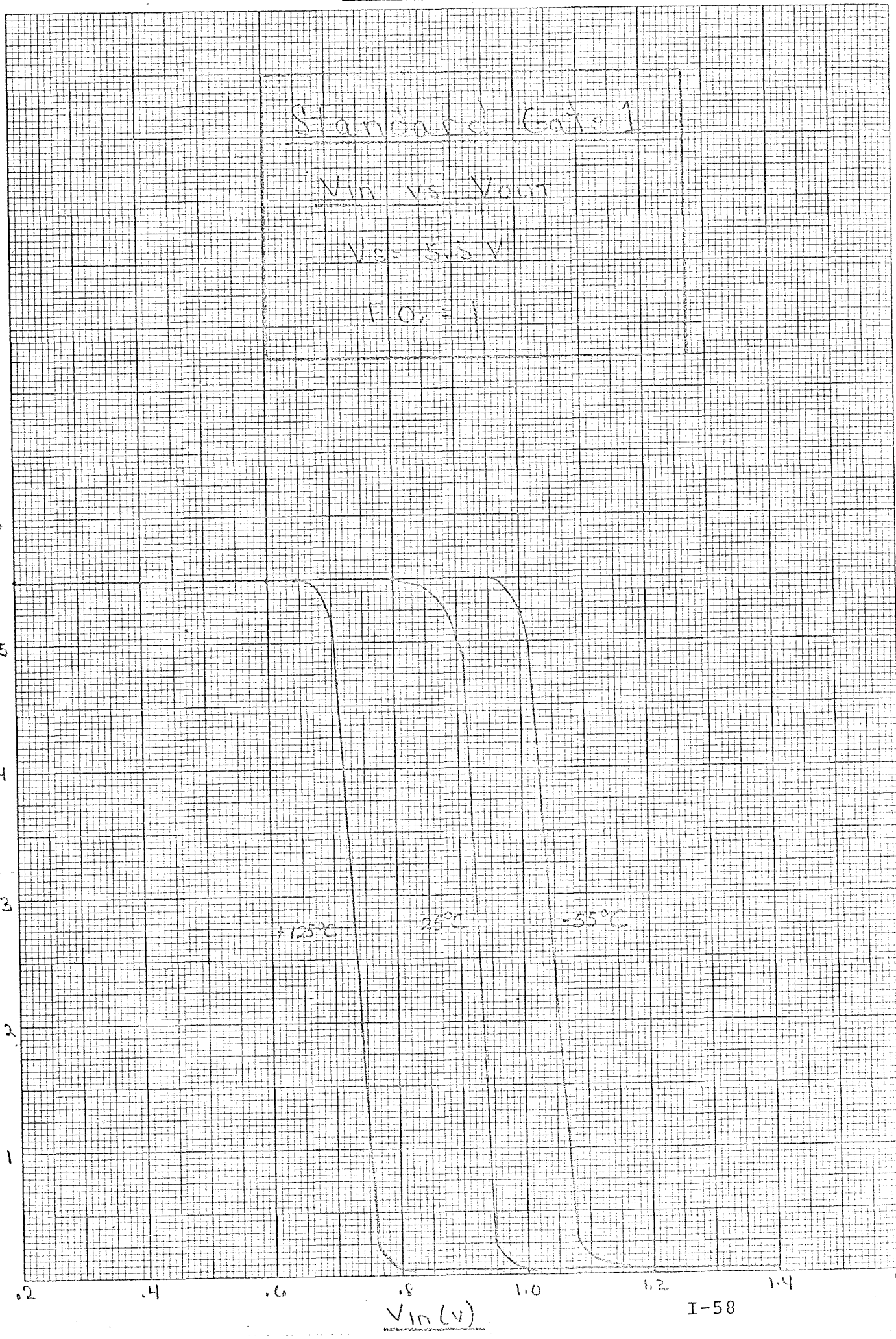


FIGURE 3.3-21

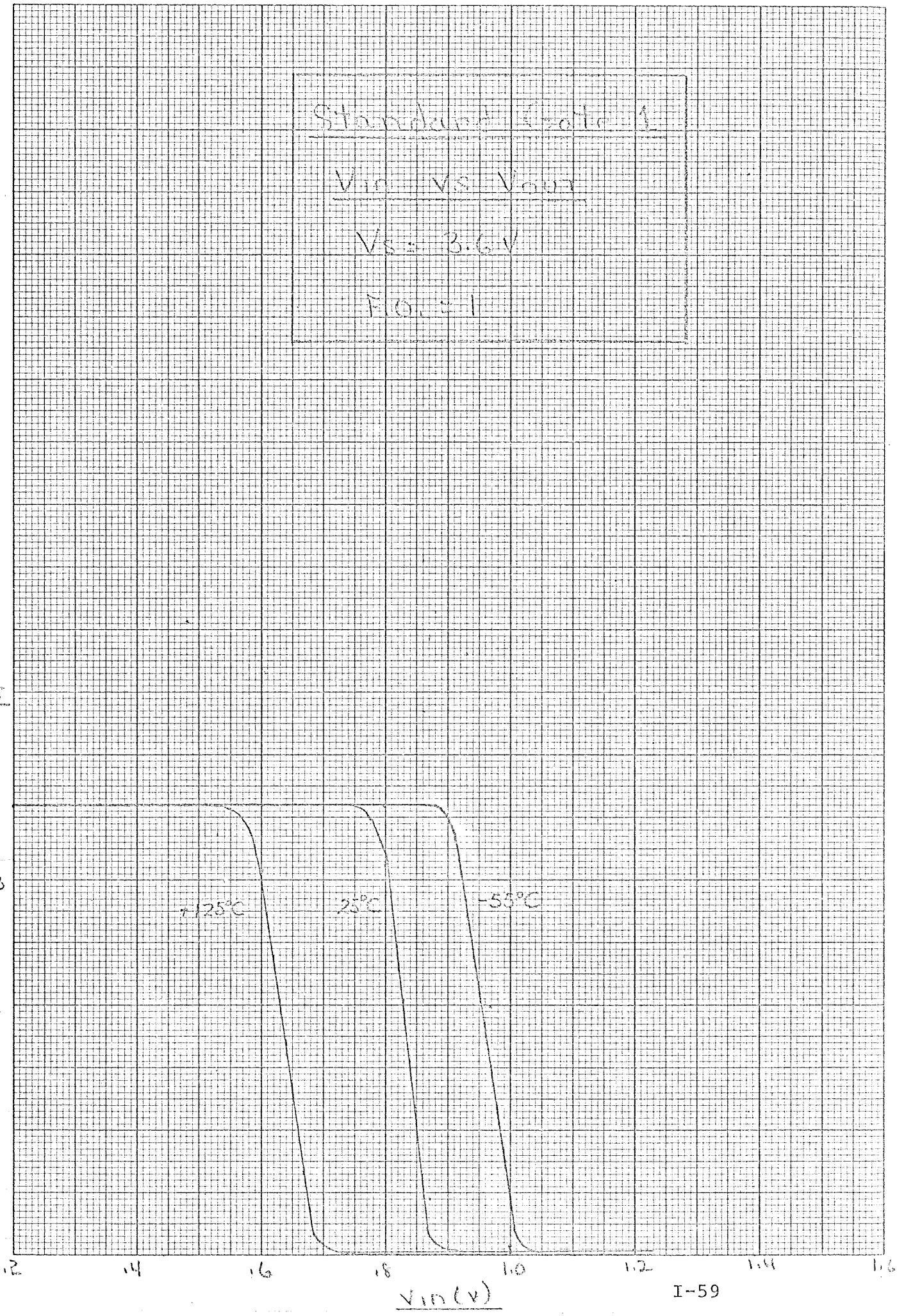


FIGURE 3.3-22

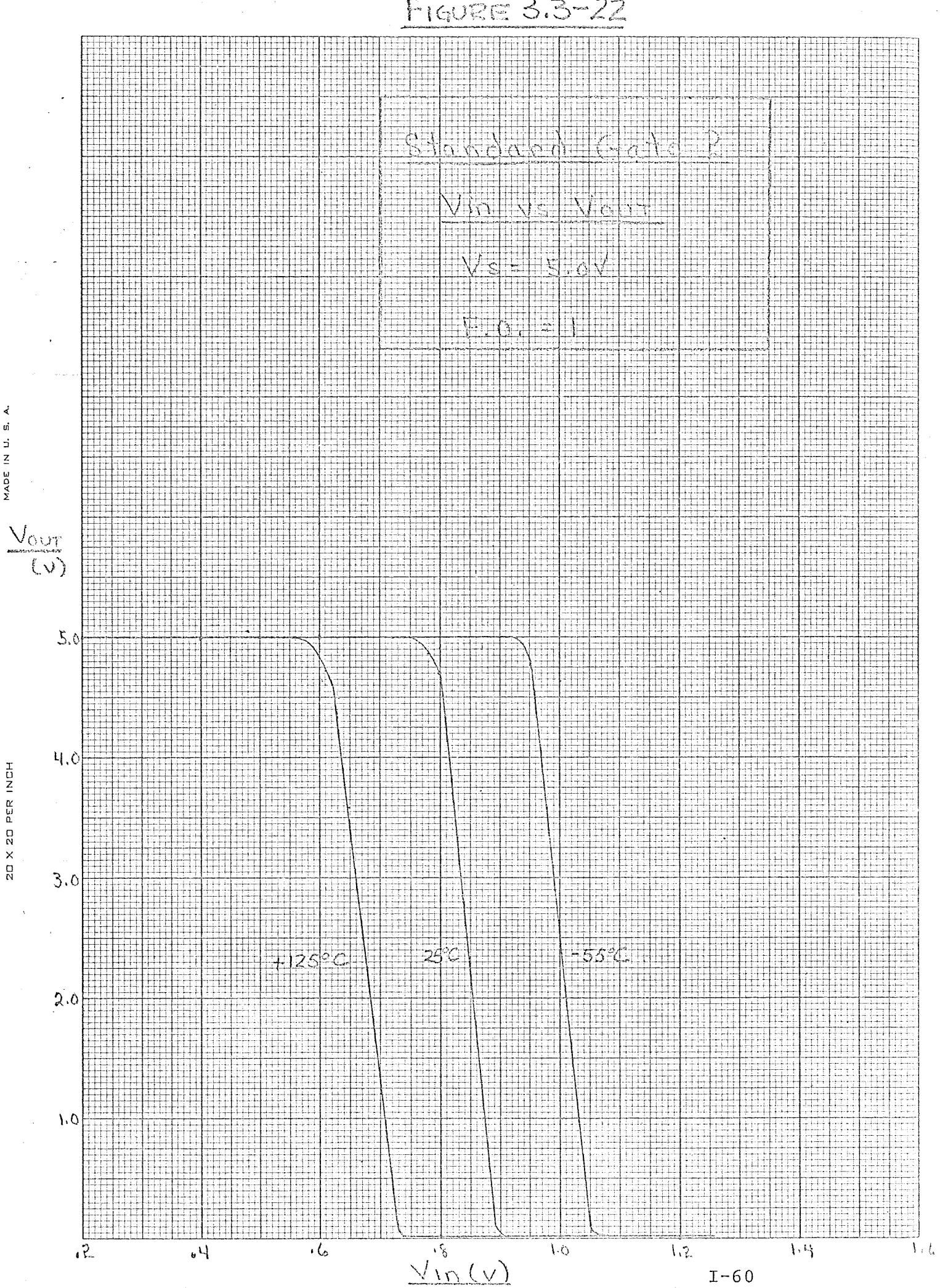

Standard Gate P
Vin vs Vout
Vs = 5.0V
E.R. = 1
Vout (v)
5.0
4.0
3.0
2.0
1.0
+125°C
25°C
-55°C
.2
.4
.6
.8
1.0
1.2
1.4
1.6
Vin (v)
MADE IN U. S. A.
20 X 20 PER INCH

FIGURE 3.3-23

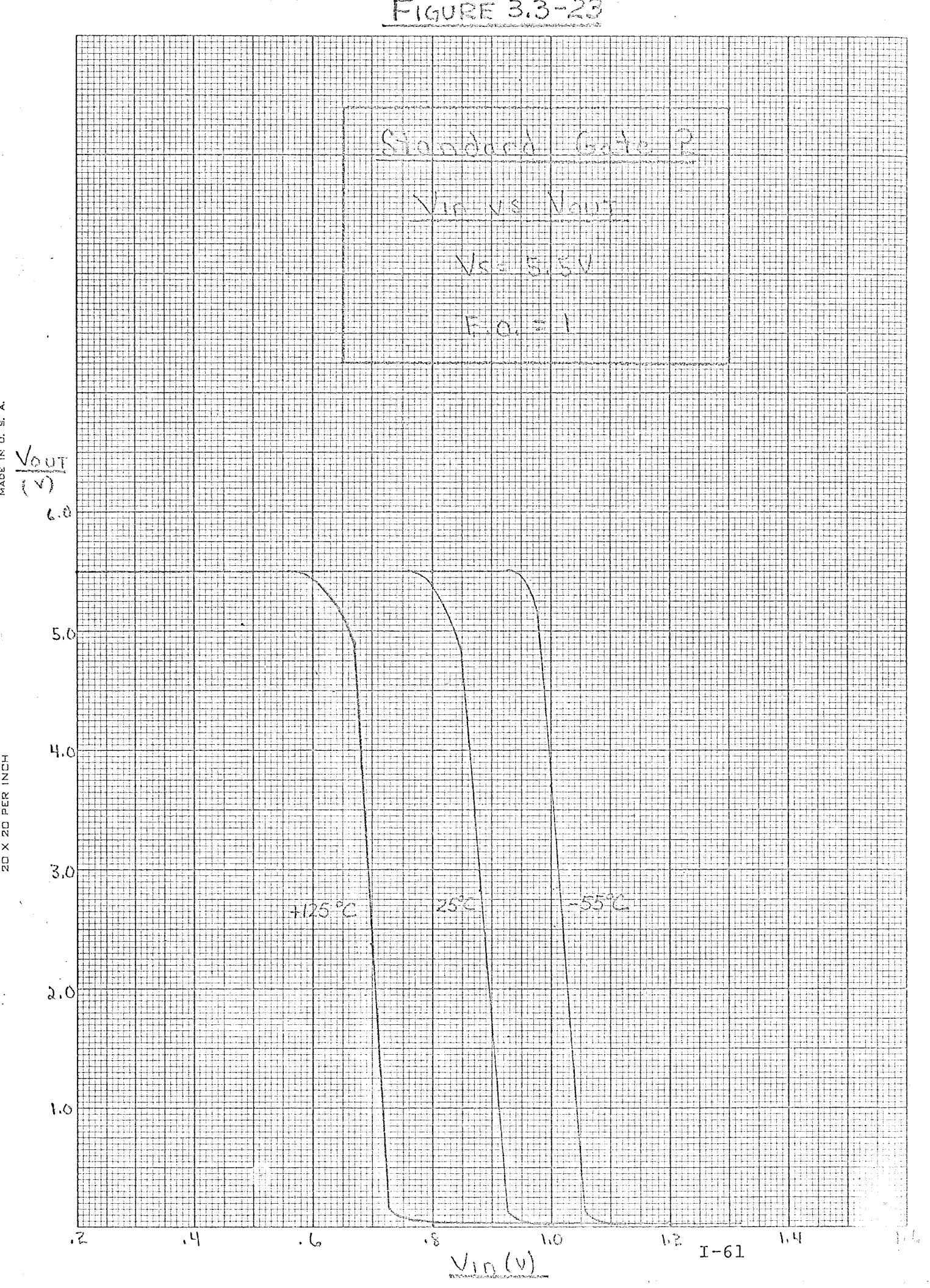


FIGURE 3.3-29

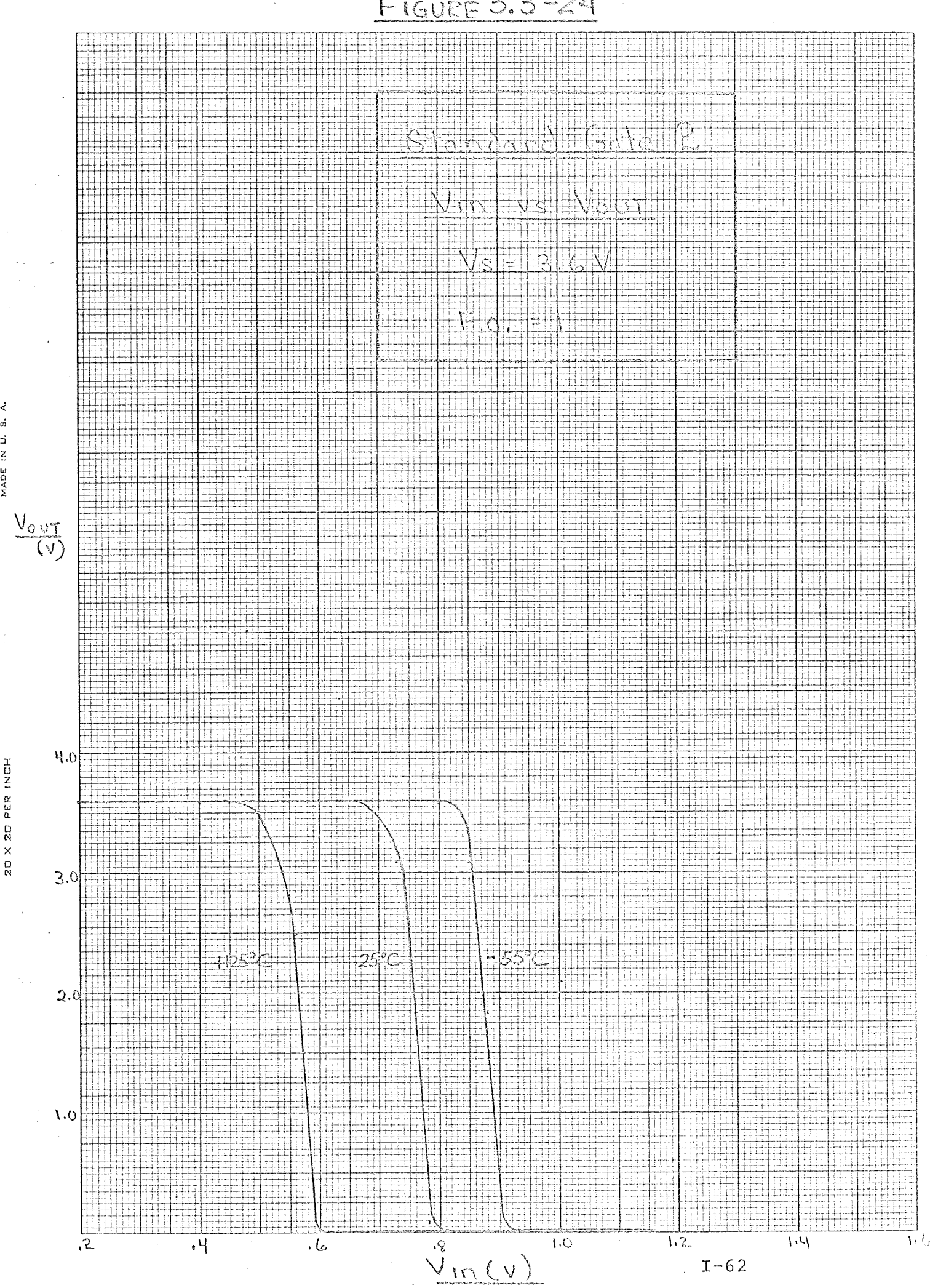

Standard Gate P.
V_{in} vs V_{out}
V_S = 3.6 V
F.O. = 1
V_{OUT} (V)
4.0
3.0
2.0
1.0
+125°C
25°C
-55°C
.2
.4
.6
.8
1.0
1.2
1.4
1.6
V_{in} (V)
MADE IN U. S. A.
20 X 20 PER INCH

FIGURE 3.3-25

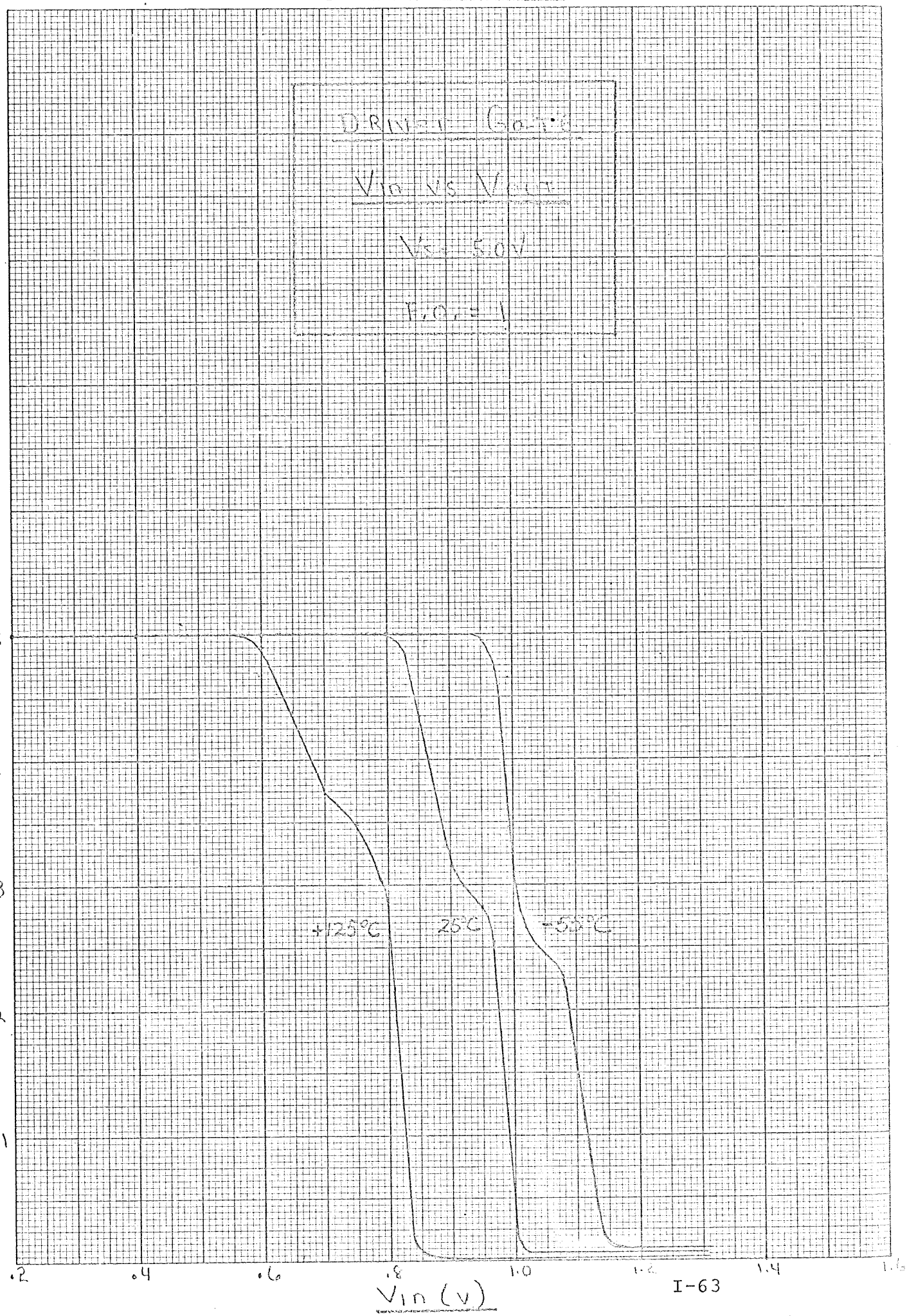


FIGURE 3.3-26

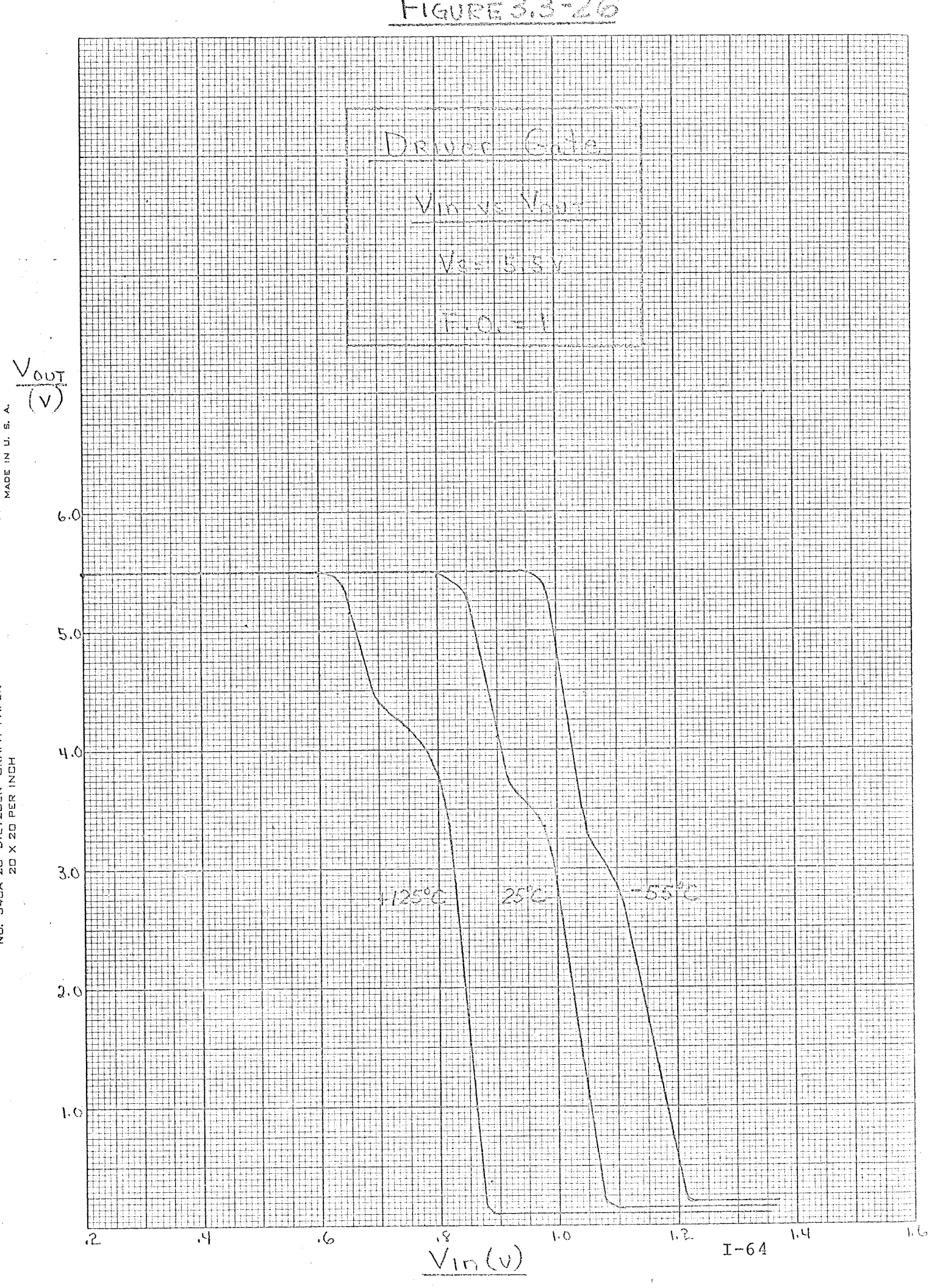


FIGURE 3.3-27

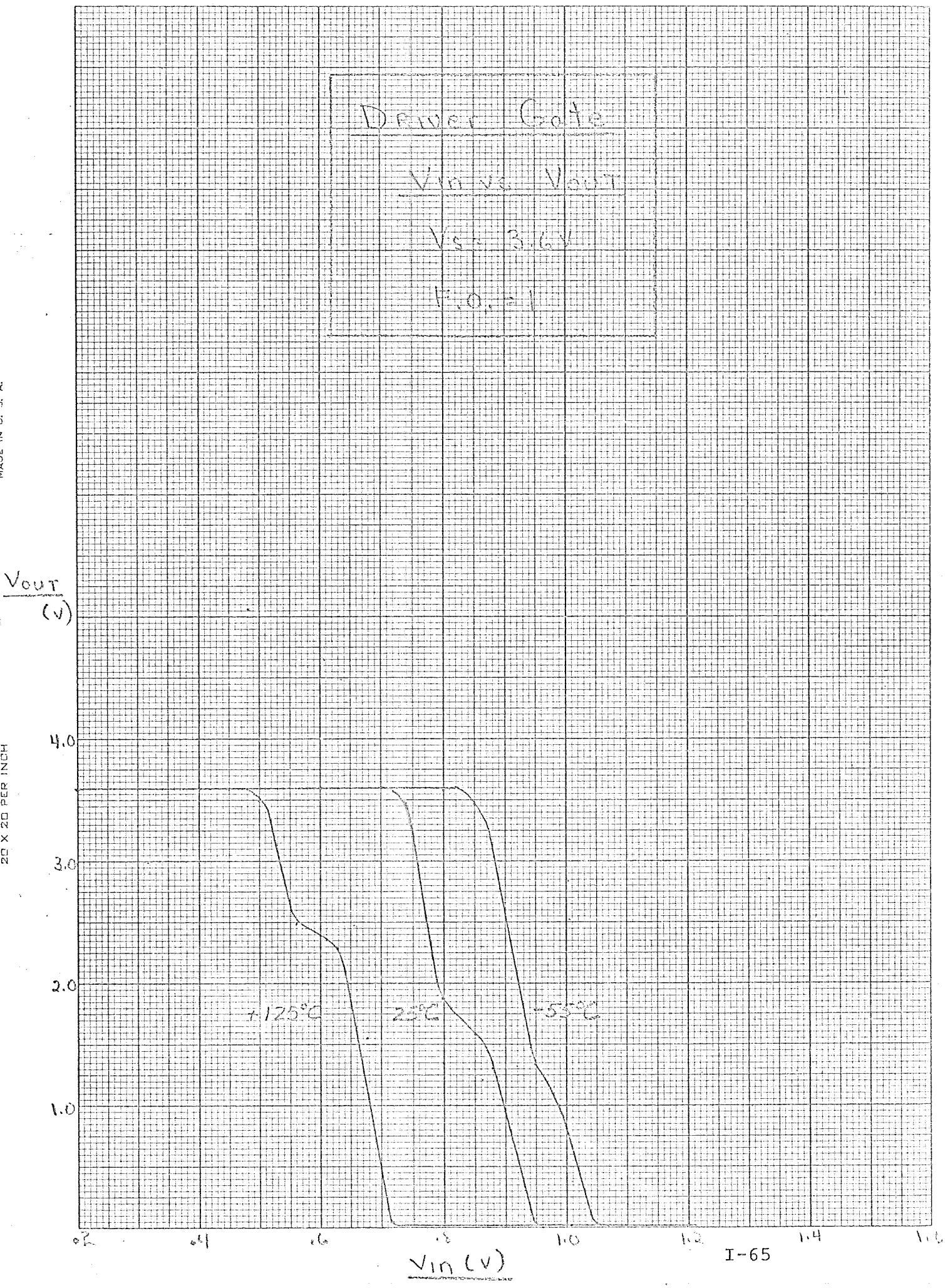

Driver Code
Vin vs Vout
Vs = 3.6V
T = 0, +1
Vout (v)
4.0
3.0
2.0
1.0
+125°C
25°C
-55°C
.2
.4
.6
.8
1.0
1.2
1.4
1.6
Vin (v)

FIGURE 3.3-28

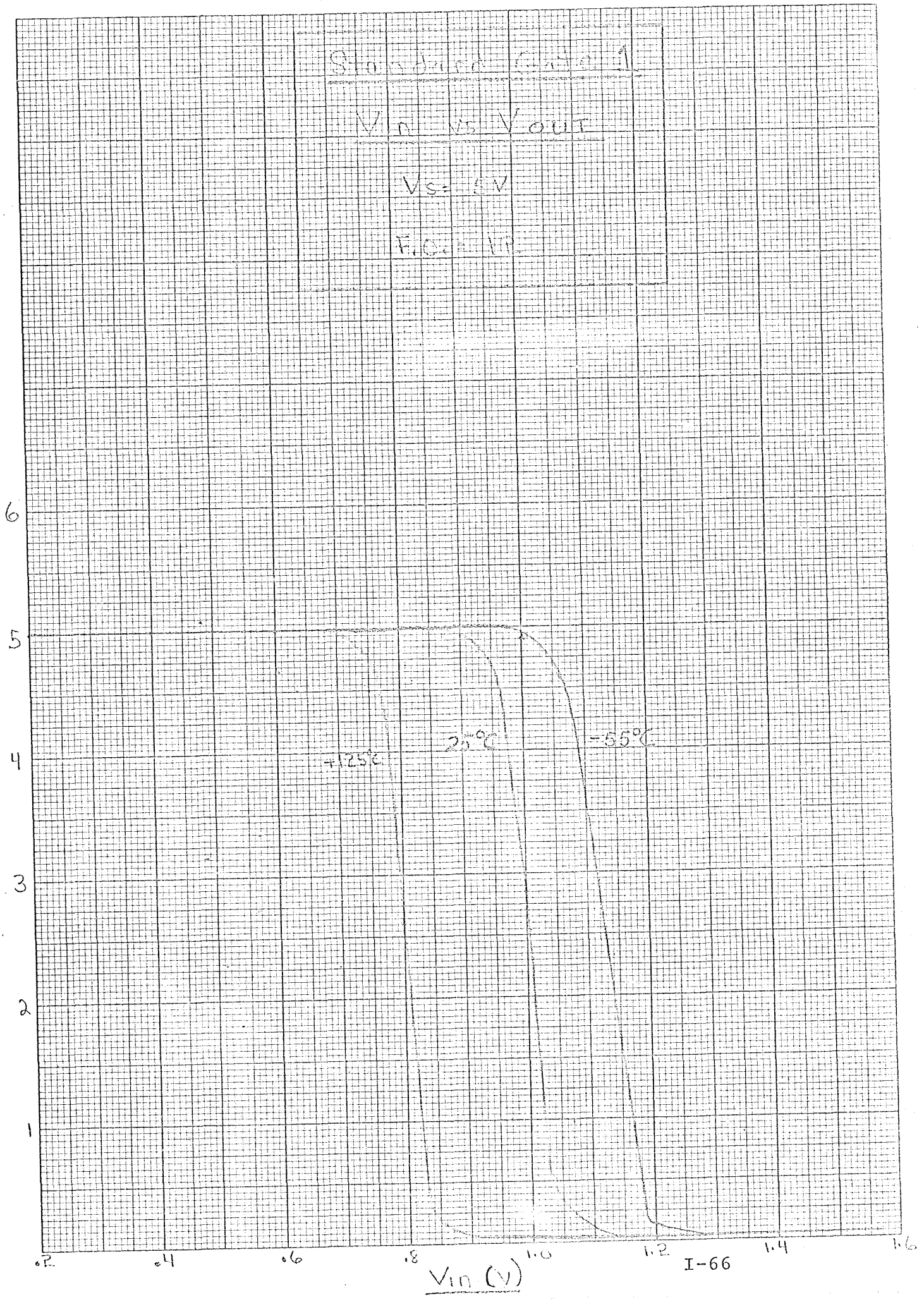

SHORT CIRCUIT CURRENT
VIN VS VOUT
VS = 5V
F.C. = 1P
+125°C
25°C
-55°C
6
5
4
3
2
1
IOUT (mA)
.2
.4
.6
.8
1.0
1.2
1.4
1.6
VIN (V)

FIGURE 3.3-25

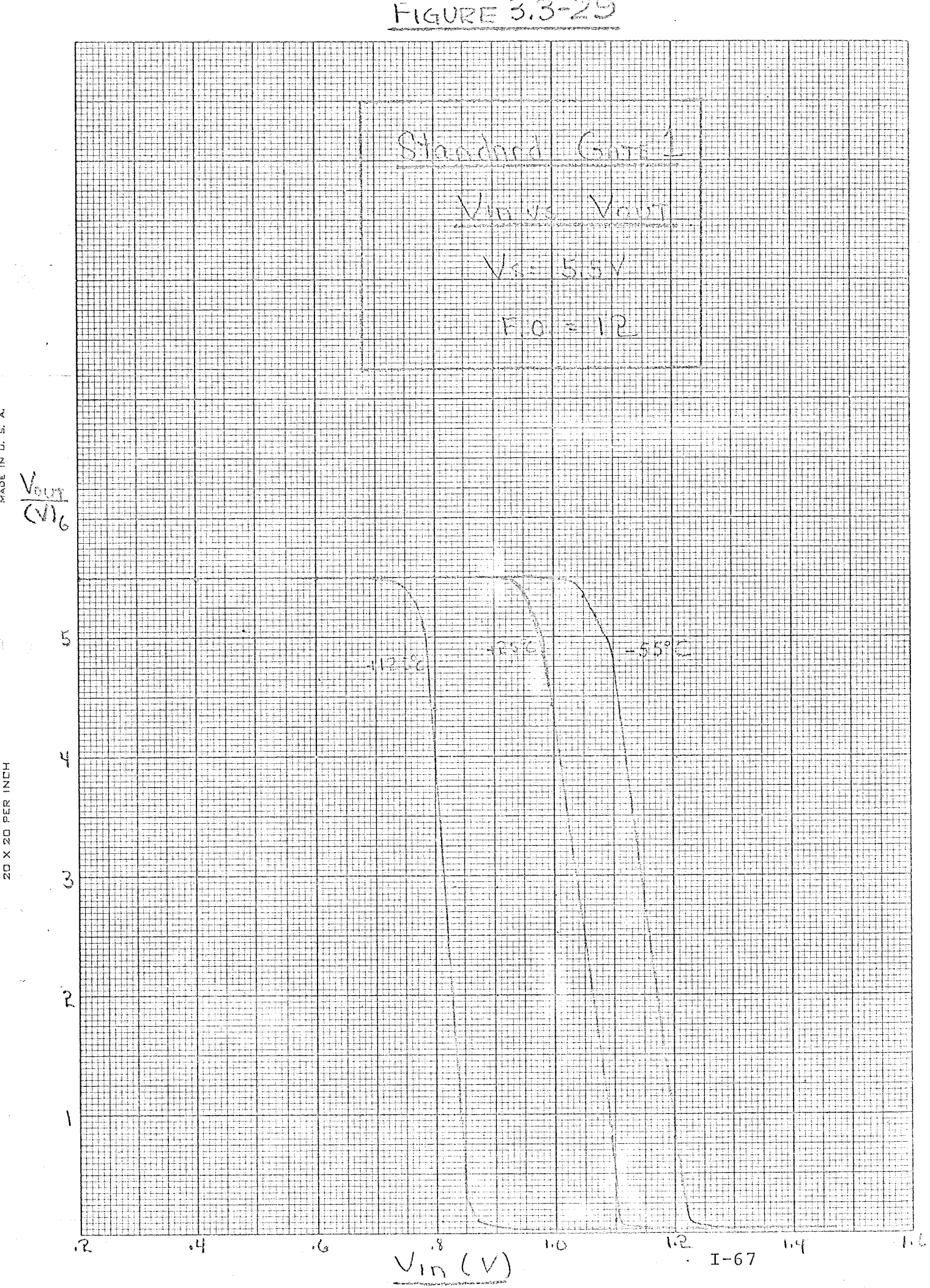


FIGURE 3.3-30

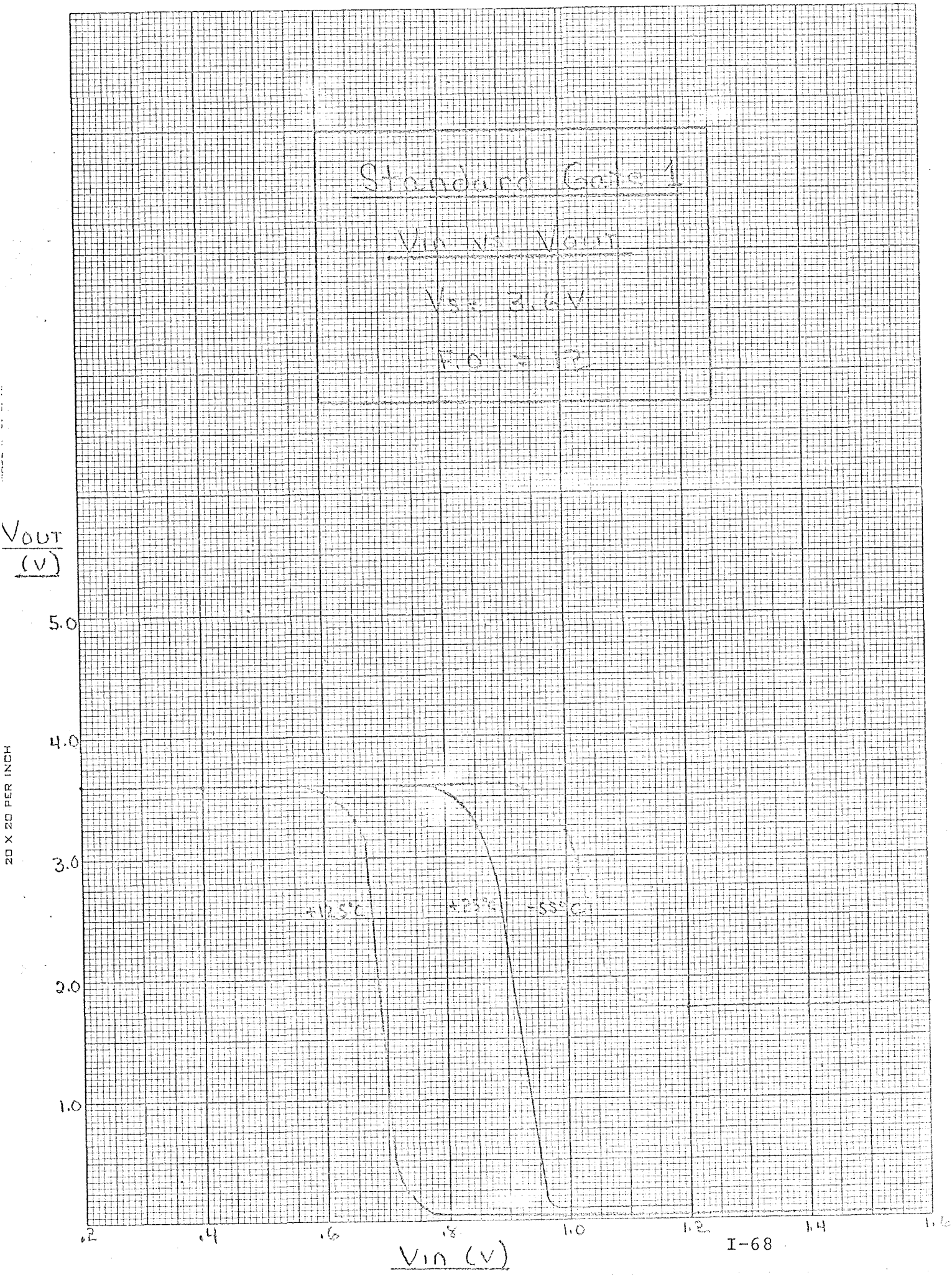

Standard Cell 1
VIN vs. VOUT
VBE = 3.6 V
RL = 1 kΩ
VOUT (V)
5.0
4.0
3.0
2.0
1.0
+125°C
+25°C
-55°C
.2
.4
.6
.8
1.0
1.2
1.4
1.6
VIN (V)
20 X 20 PER INCH

FIGURE 3.3-31

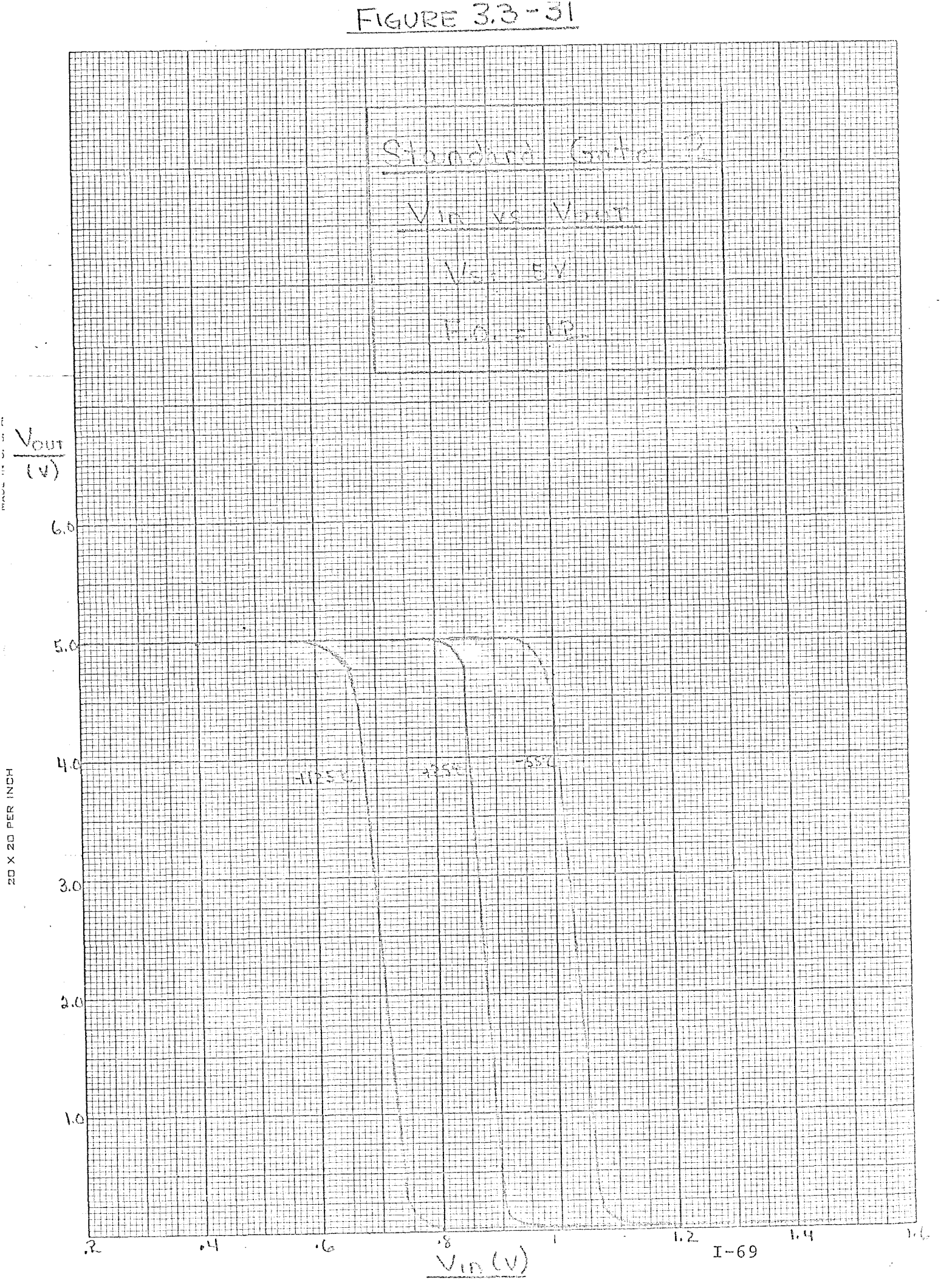

Standard Cmos
Vin vs Vout
Vcc = 5 V
T.C. = MP
Vout (V)
6.0
5.0
4.0
3.0
2.0
1.0
+125°C
+25°C
-55°C
.2
.4
.6
.8
1
1.2
1.4
Vin (V)
20 X 20 PER INCH

FIGURE 3.3-32

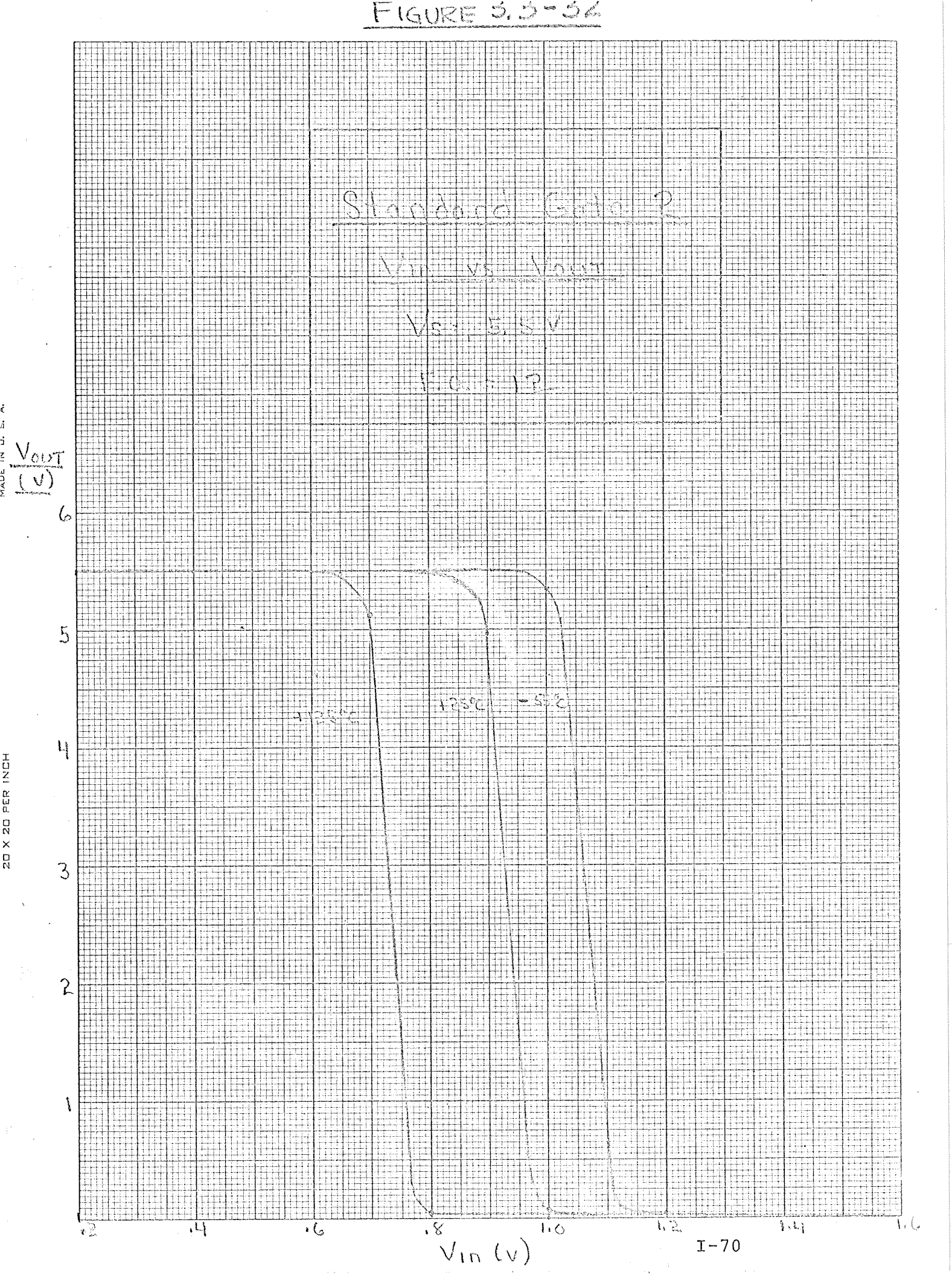


FIGURE 3.3-33

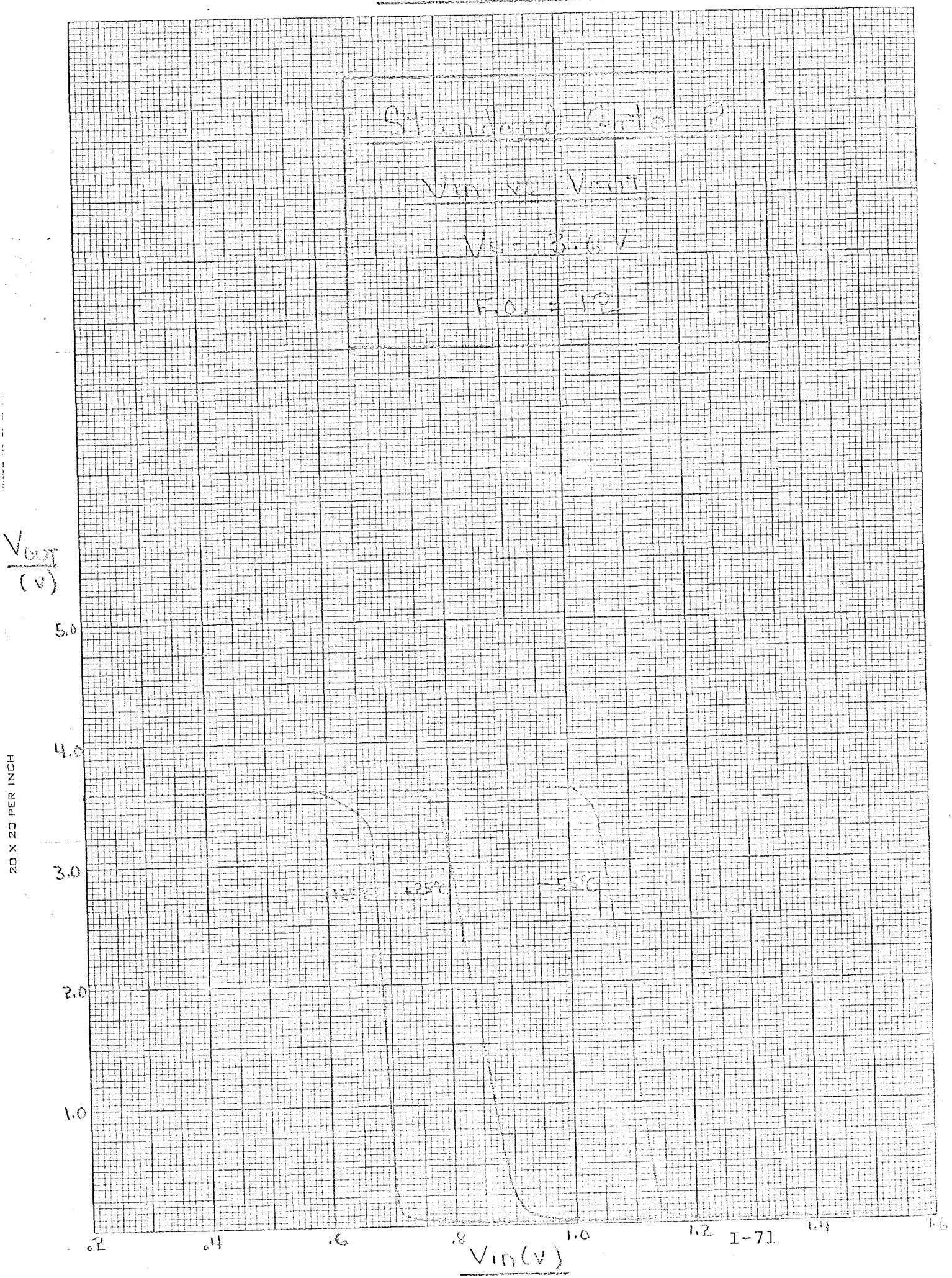

Simulated Data
Vin vs. Vout
Vs = 3.6 V
F.O. = 12
Vout (V)
5.0
4.0
3.0
2.0
1.0
-125°C - +25°C
-55°C
.2
.4
.6
.8
1.0
1.2
1.4
1.6
Vin(V)
20 X 20 PER INCH

FIGURE 3.3-34

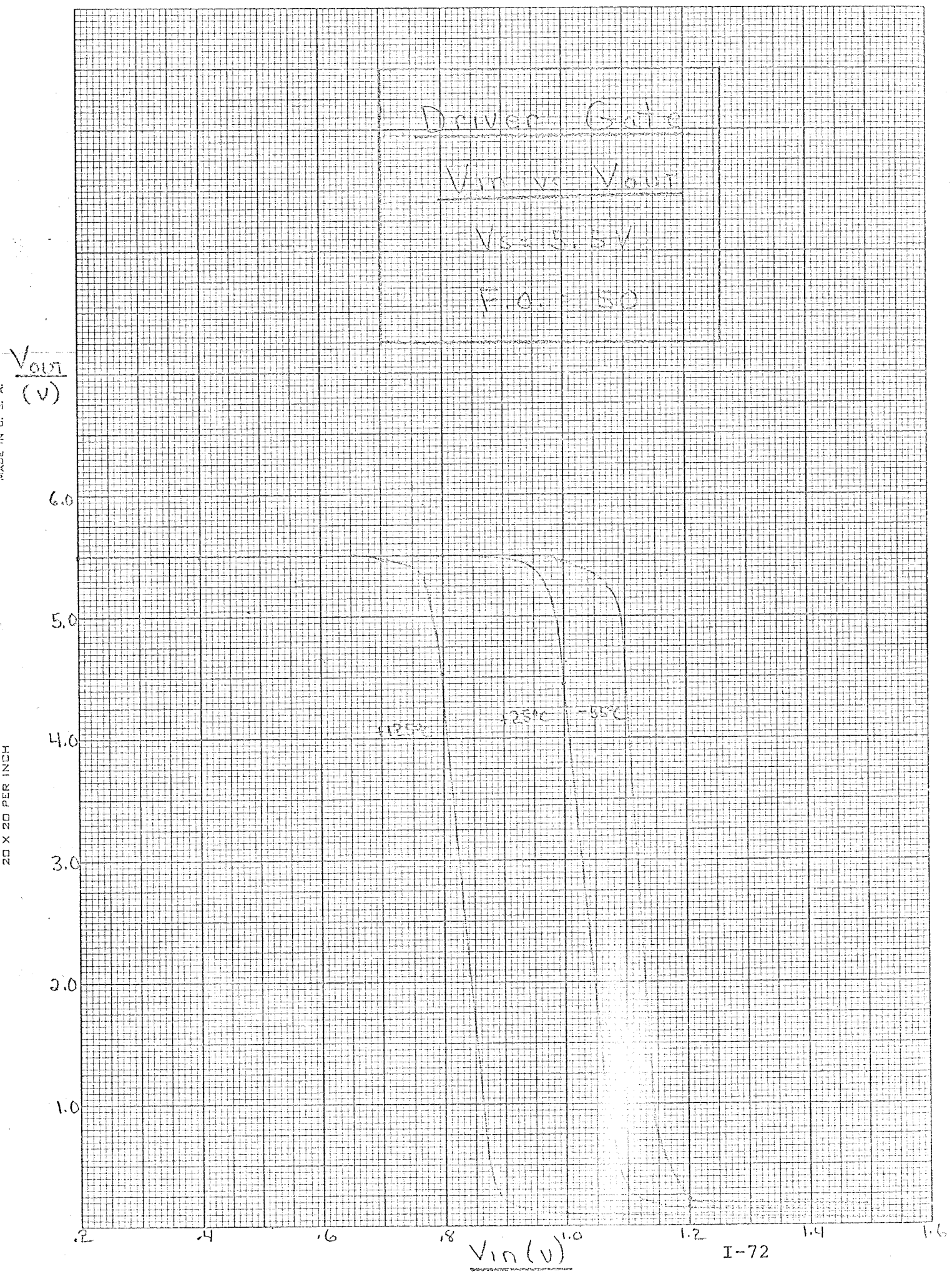

Driver Gate
Vin vs Vout
Vcc = 5.5V
F.O. = 50
Vout (v)
6.0
5.0
4.0
3.0
2.0
1.0
+125°C
+25°C
-55°C
.2
.4
.6
.8
1.0
1.2
1.4
1.6
Vin (v)

FIGURE 3.3-3

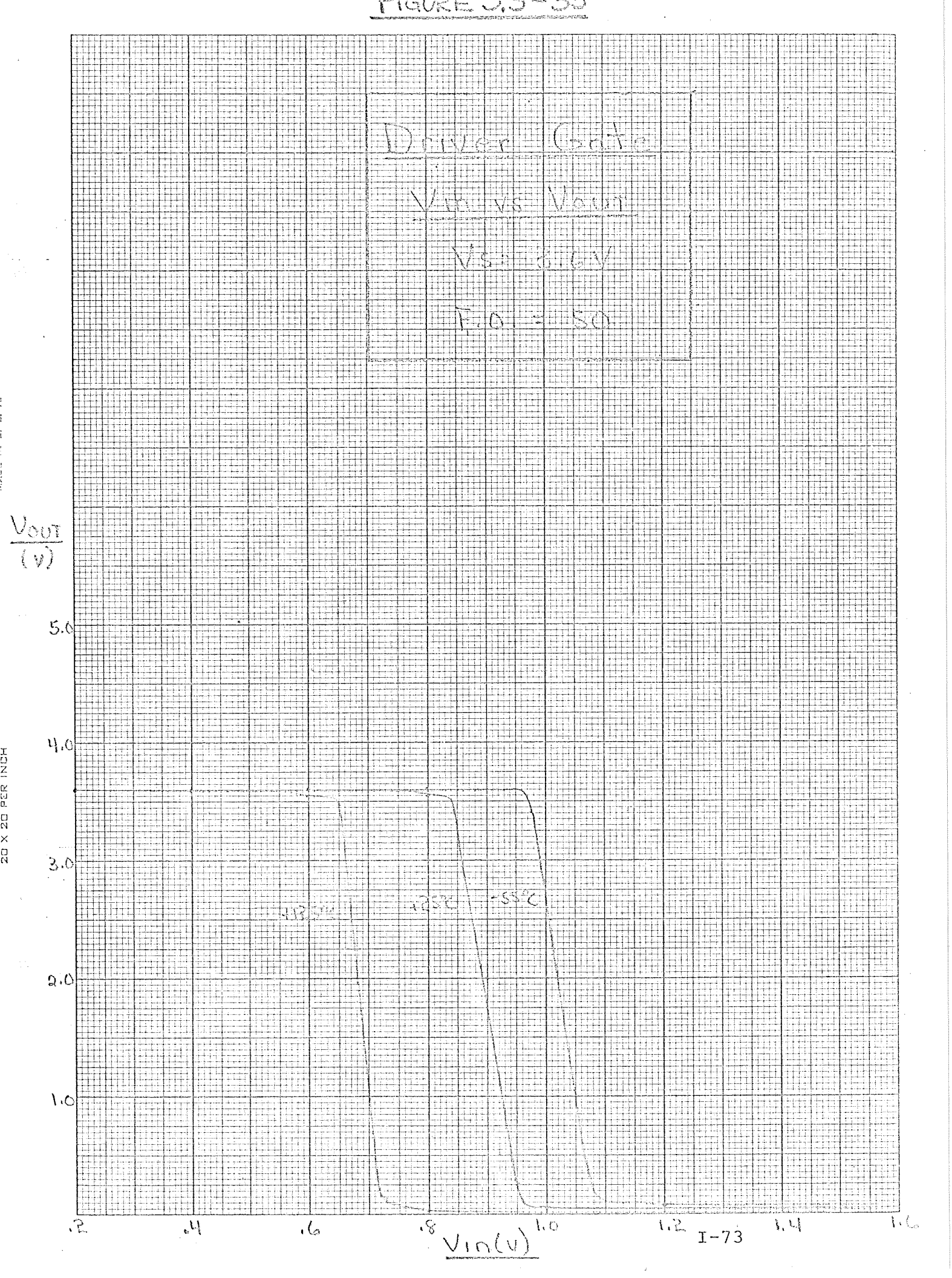
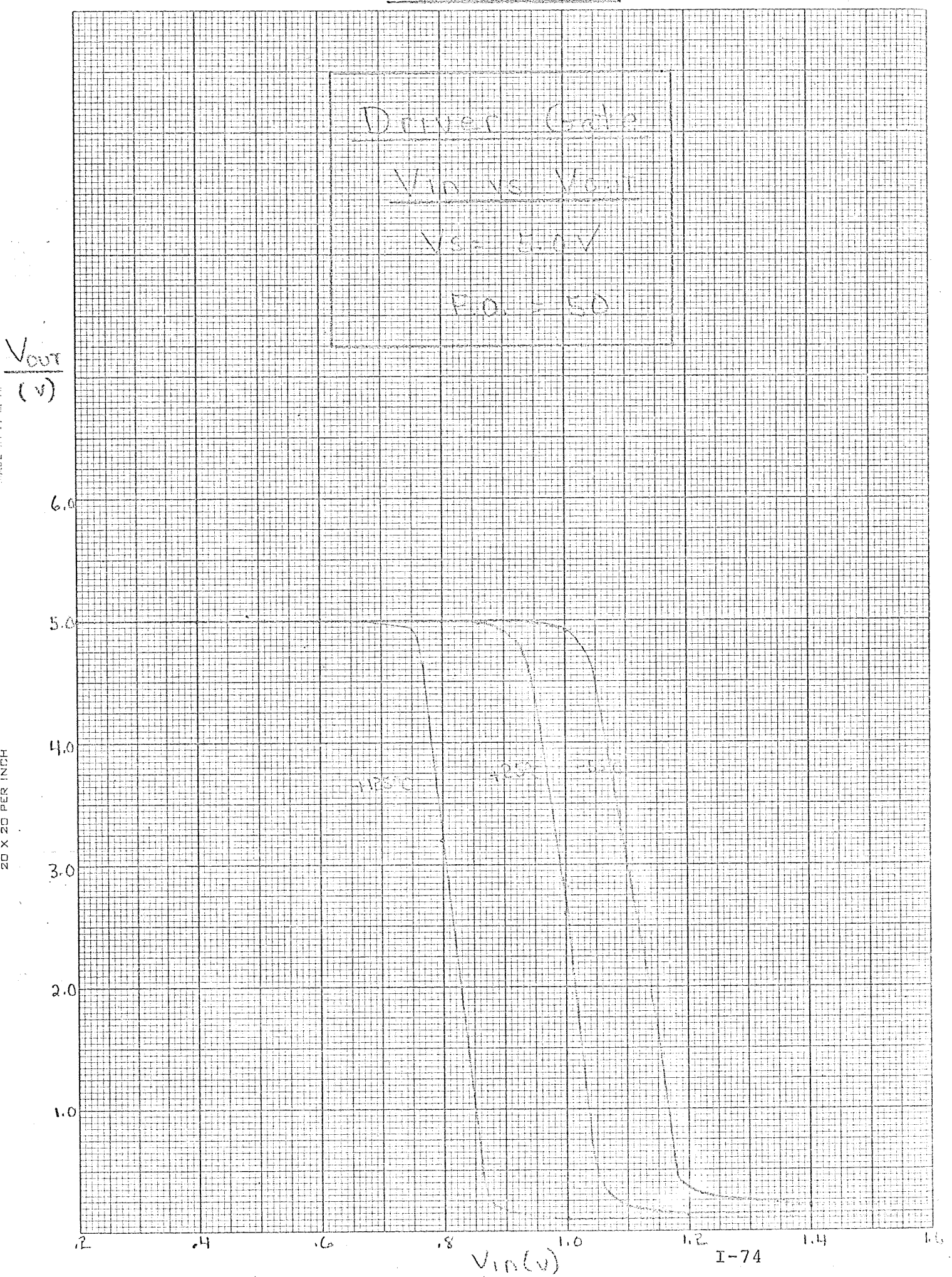

Driver Gate
Vin vs Vout
Vs. 5.0V
F.O. = 50
Vout (V)
5.0
4.0
3.0
2.0
1.0
+25°C
-55°C
.2
.4
.6
.8
1.0
1.2
1.4
1.6
Vin(V)
20 X 20 PER INCH

FIGURE 3.3-36

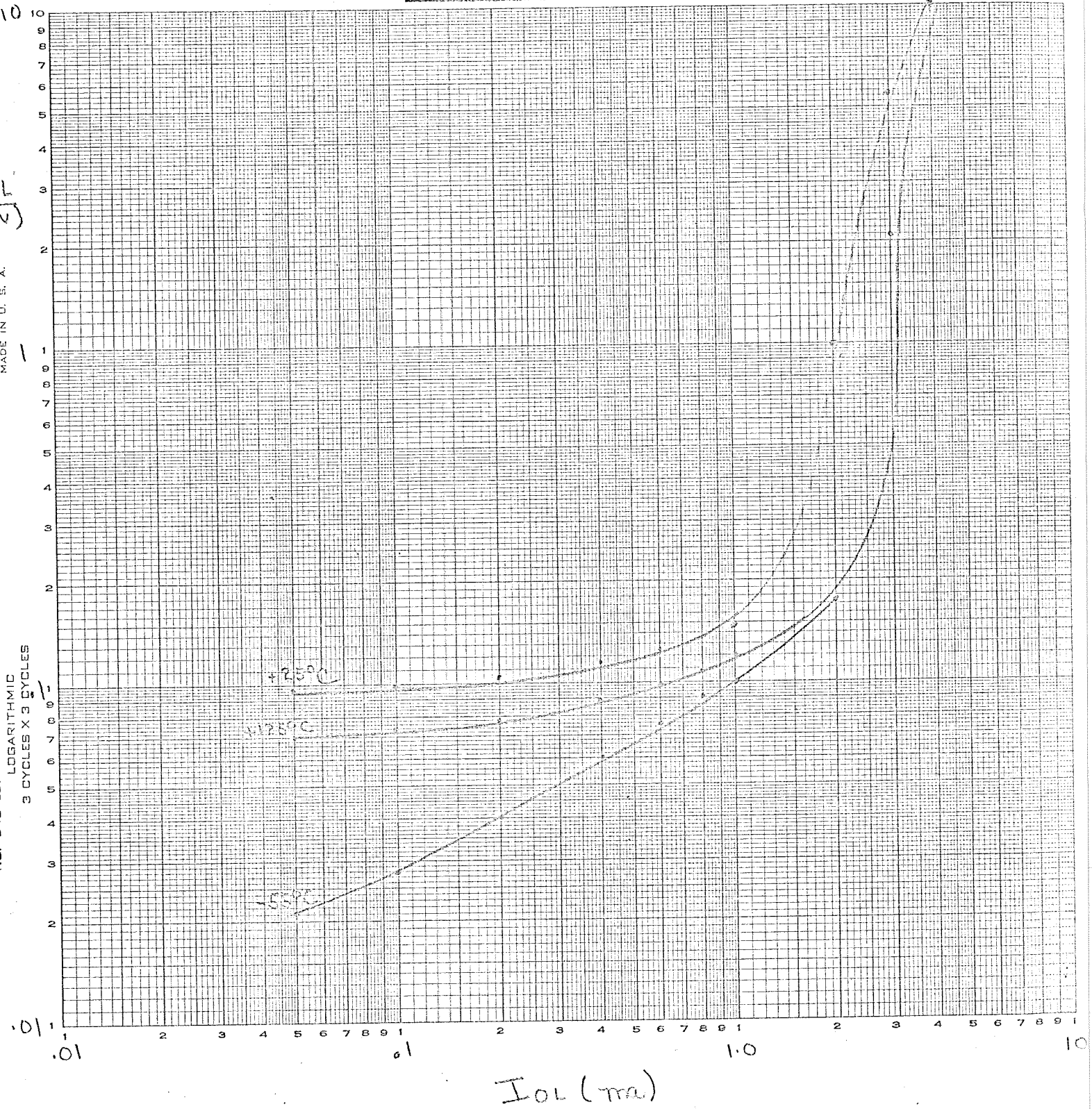

DRIVER (CMOS)
VIN vs VOUT
VSS = 0.0 V
P.O. = 5.0
VOUT (V)
6.0
5.0
4.0
3.0
2.0
1.0
.2
.4
.6
.8
1.0
1.2
1.4
1.6
VIN (V)
HIP5C
+25
-5
20 X 20 PER INCH

Standard Gate 1

V_{OL} vs I_{OL}

$V_S = 5.0V$

FIGURE 3.3-37

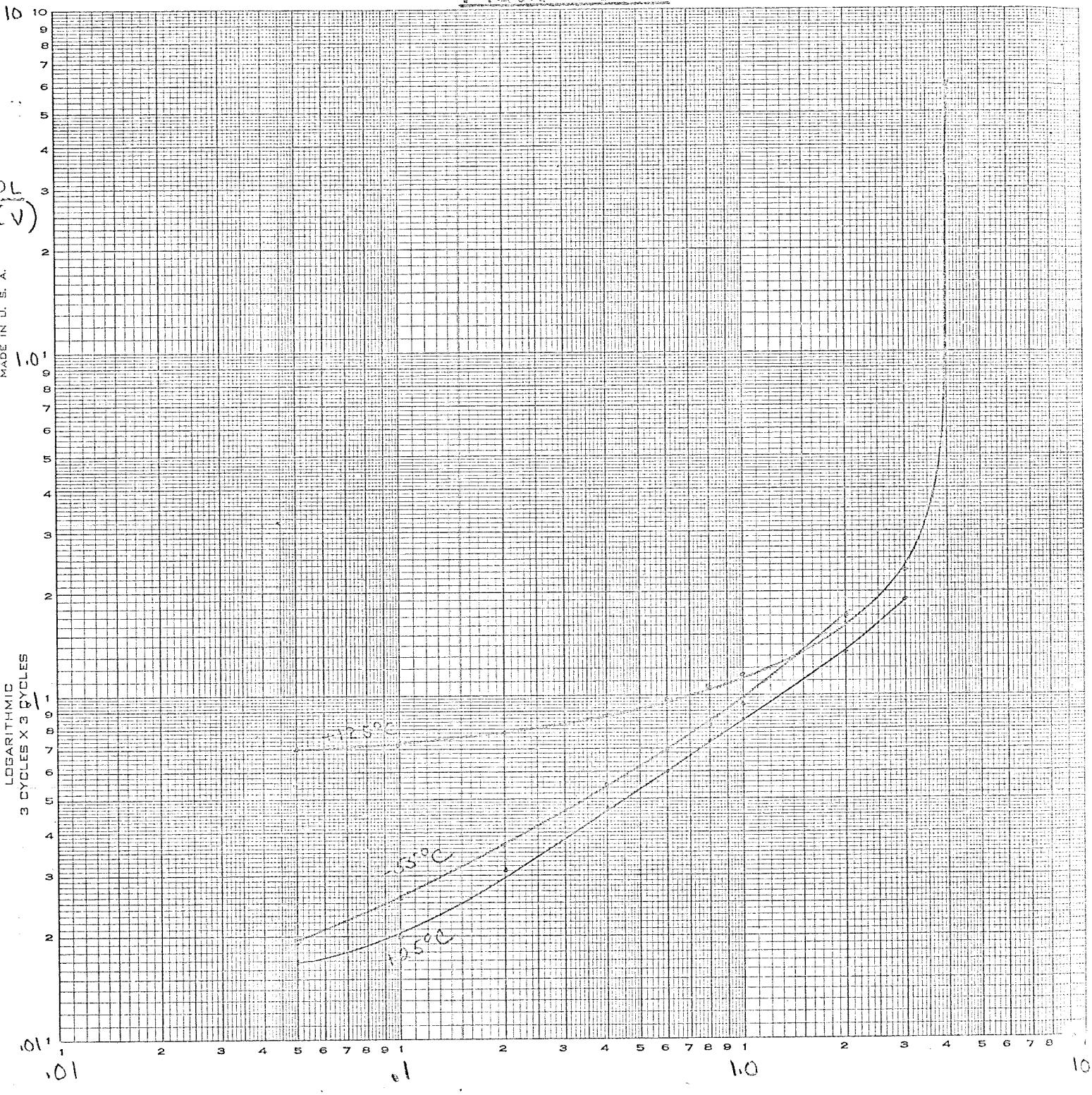


Standard Gate 1

V_{OL} vs I_{OL}

$V_S = 5.5V$

FIGURE 3.3-38



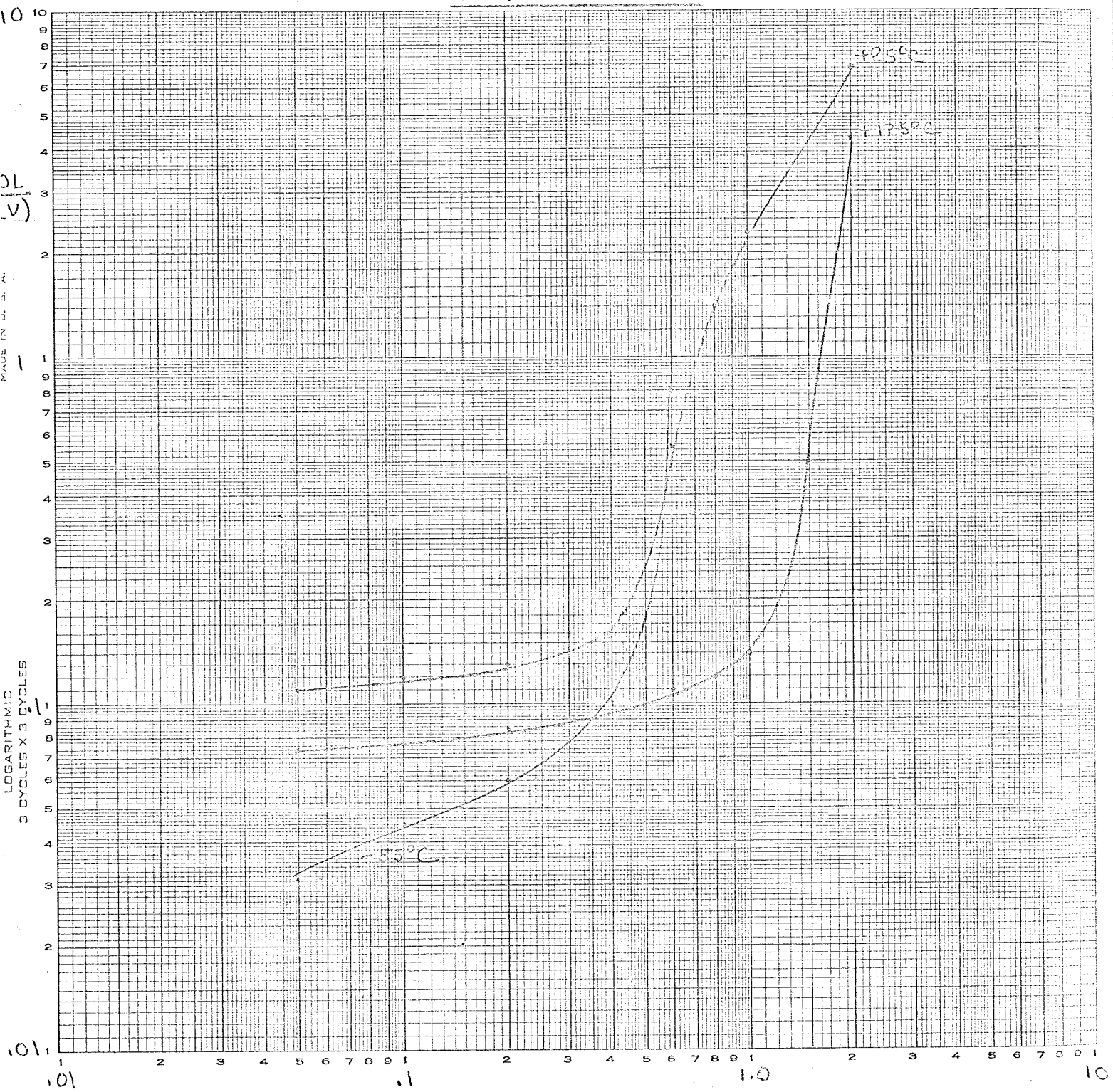
I_{OL} (ma)

Standard Gate 1

V_{OL} vs I_{OL}

$V_S = 3.6V$

FIGURE 3.3-39

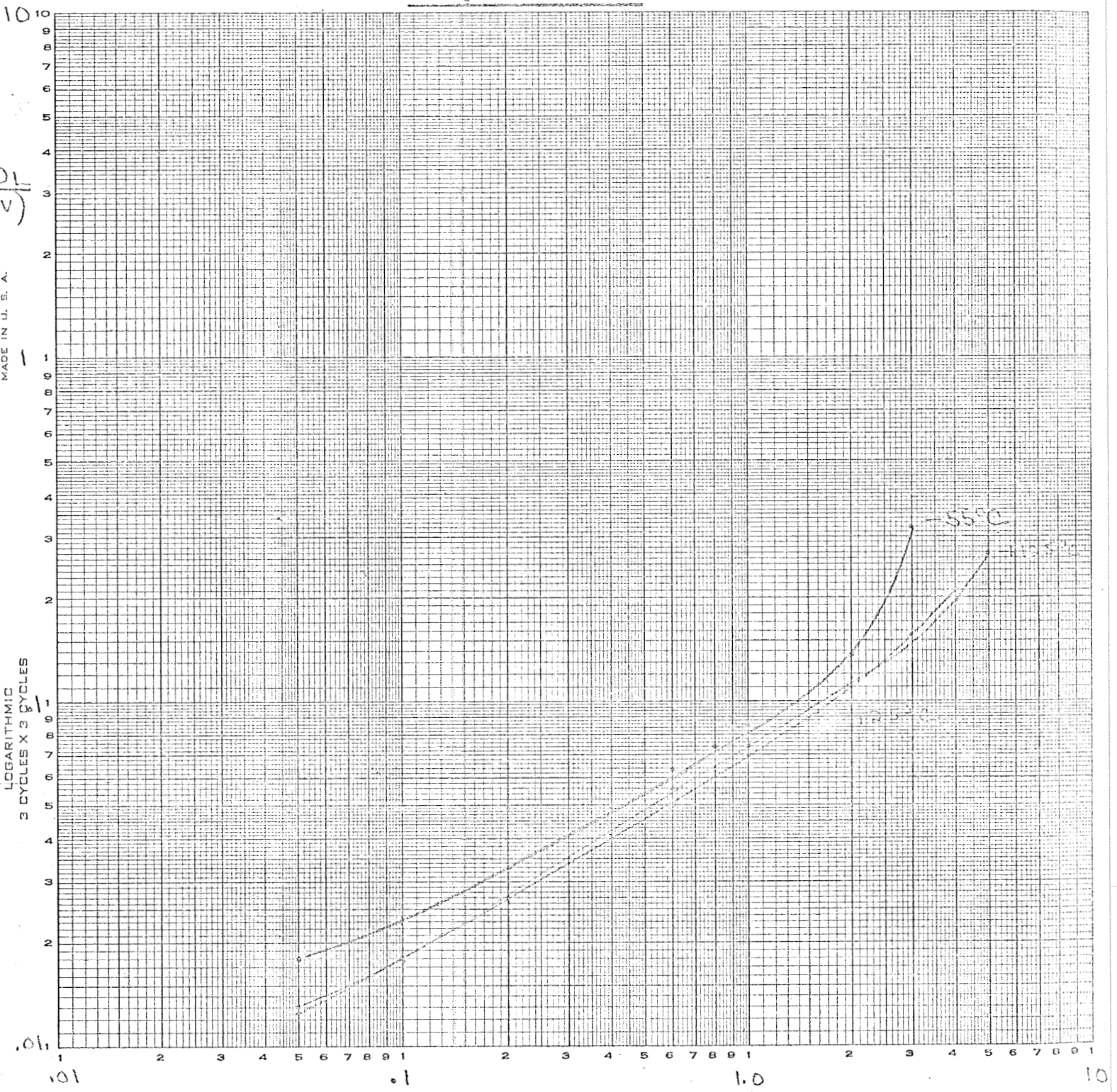


Standard Gate 2

V_{OL} vs I_{OL}

V_S = 5V

FIGURE 3.3-40



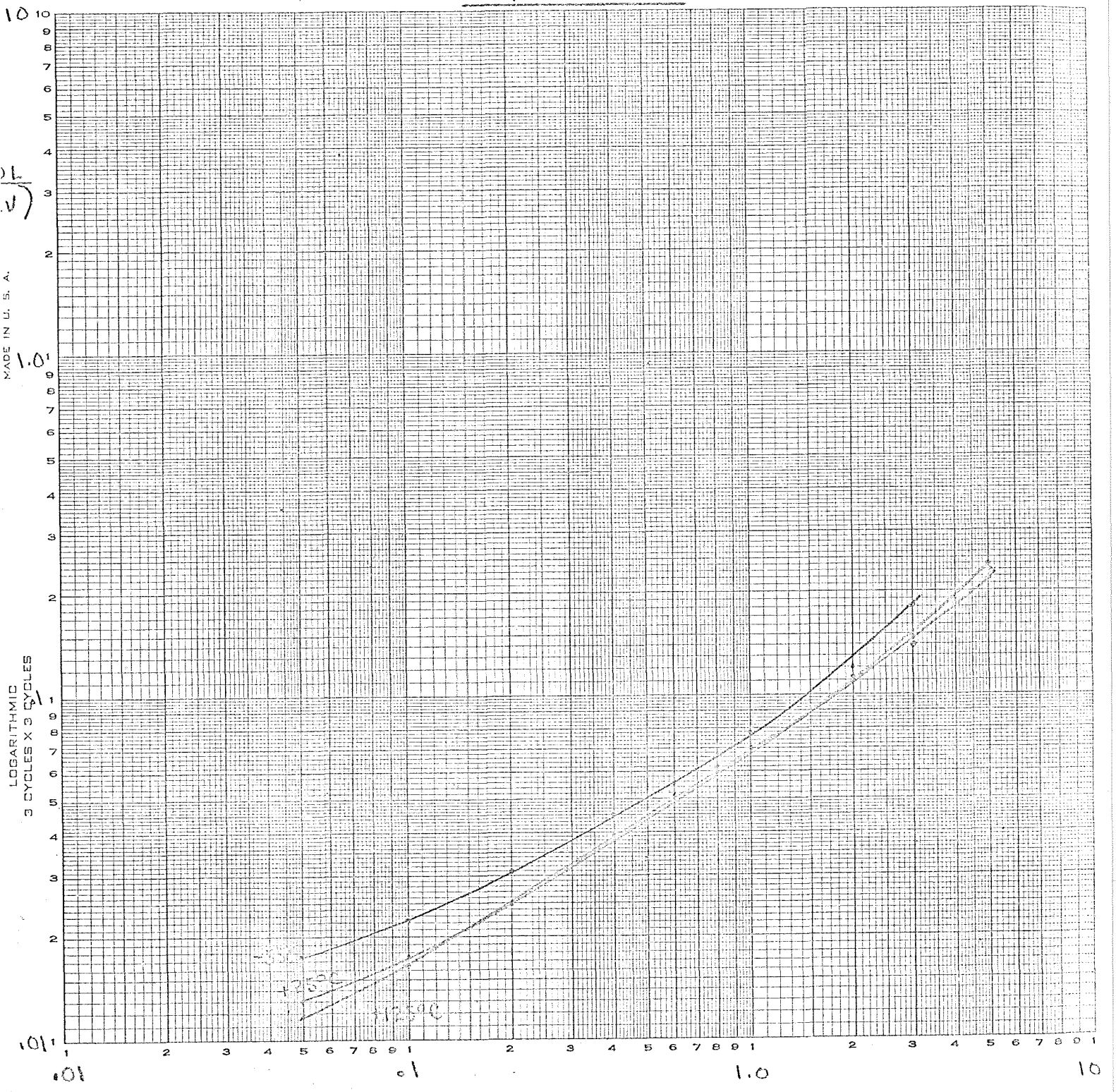
I_{OL} (ma)

Standard Gate 2

V_{OL} vs I_{OL}

V_S = 5.5 V

FIGURE 3.3-41



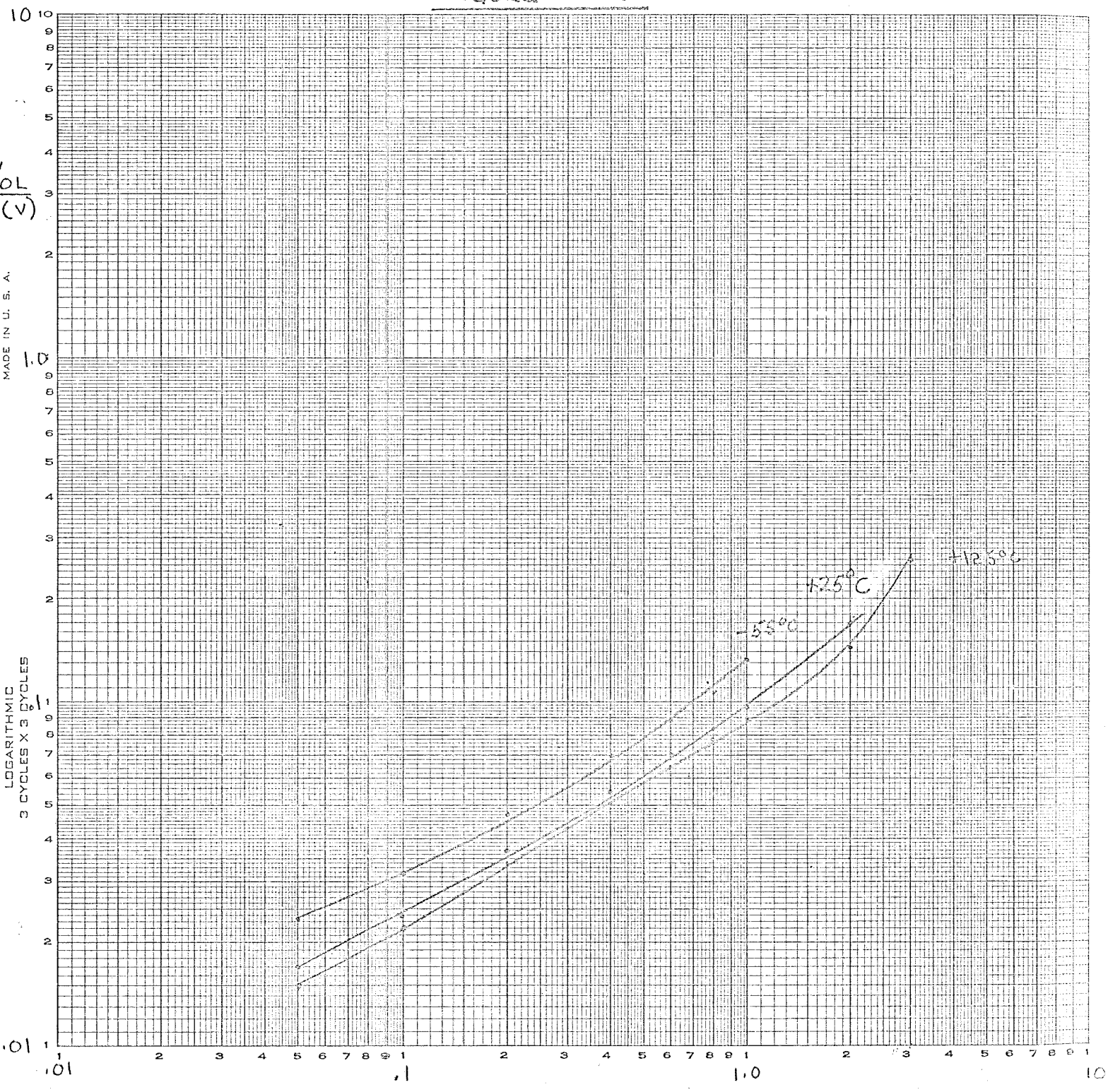
I_{OL} (ma)

STANDARD GATE 2

V_{OL} vs I_{OL}

$V_S = 3.6\,V$

FIGURE 33-42



V_{OL} (V)

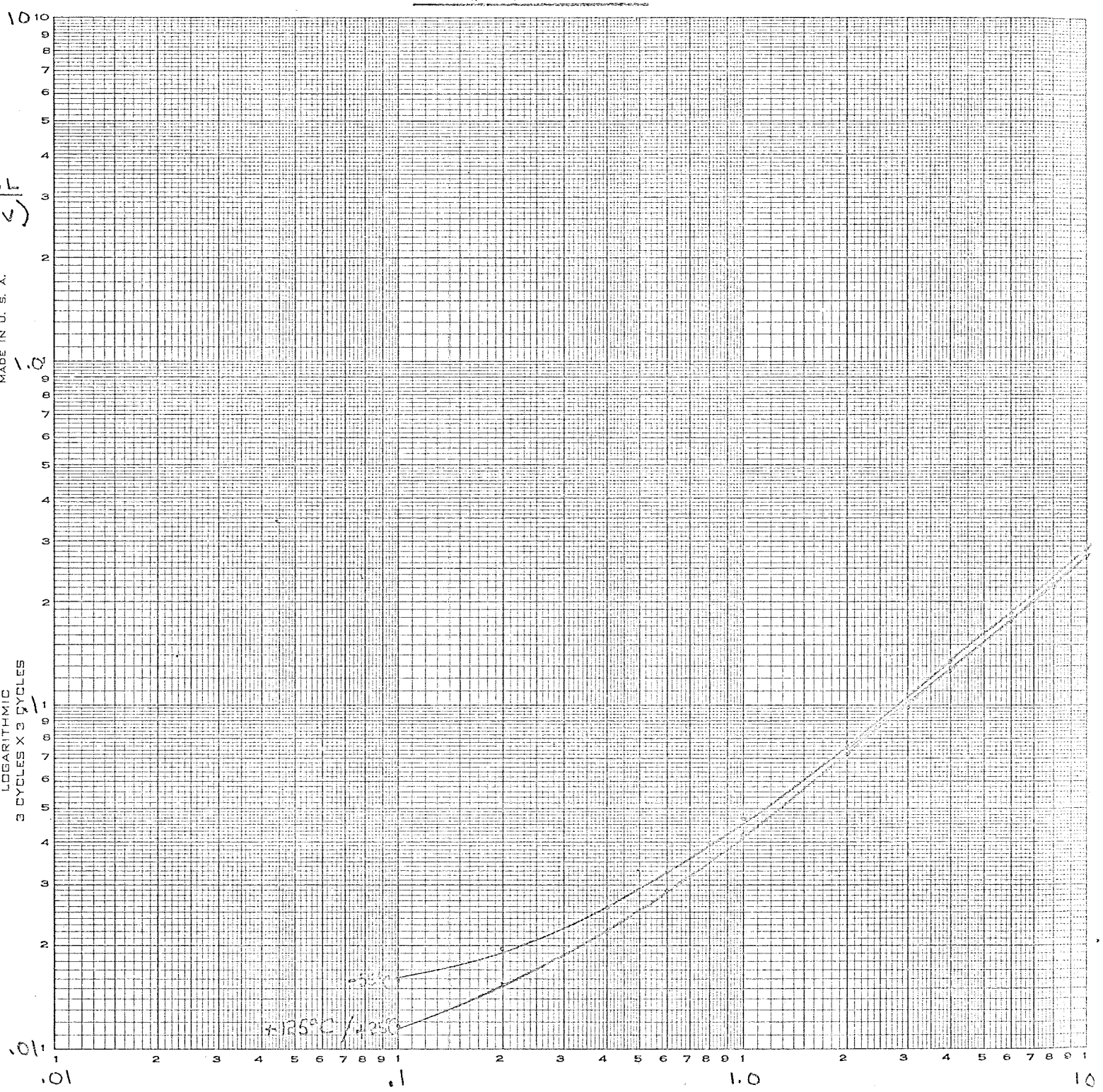
I_{OL} (ma)

DRIVER Gate

V_{OL} vs I_{OL}

V_S = 5.0V

FIGURE 3.3-43

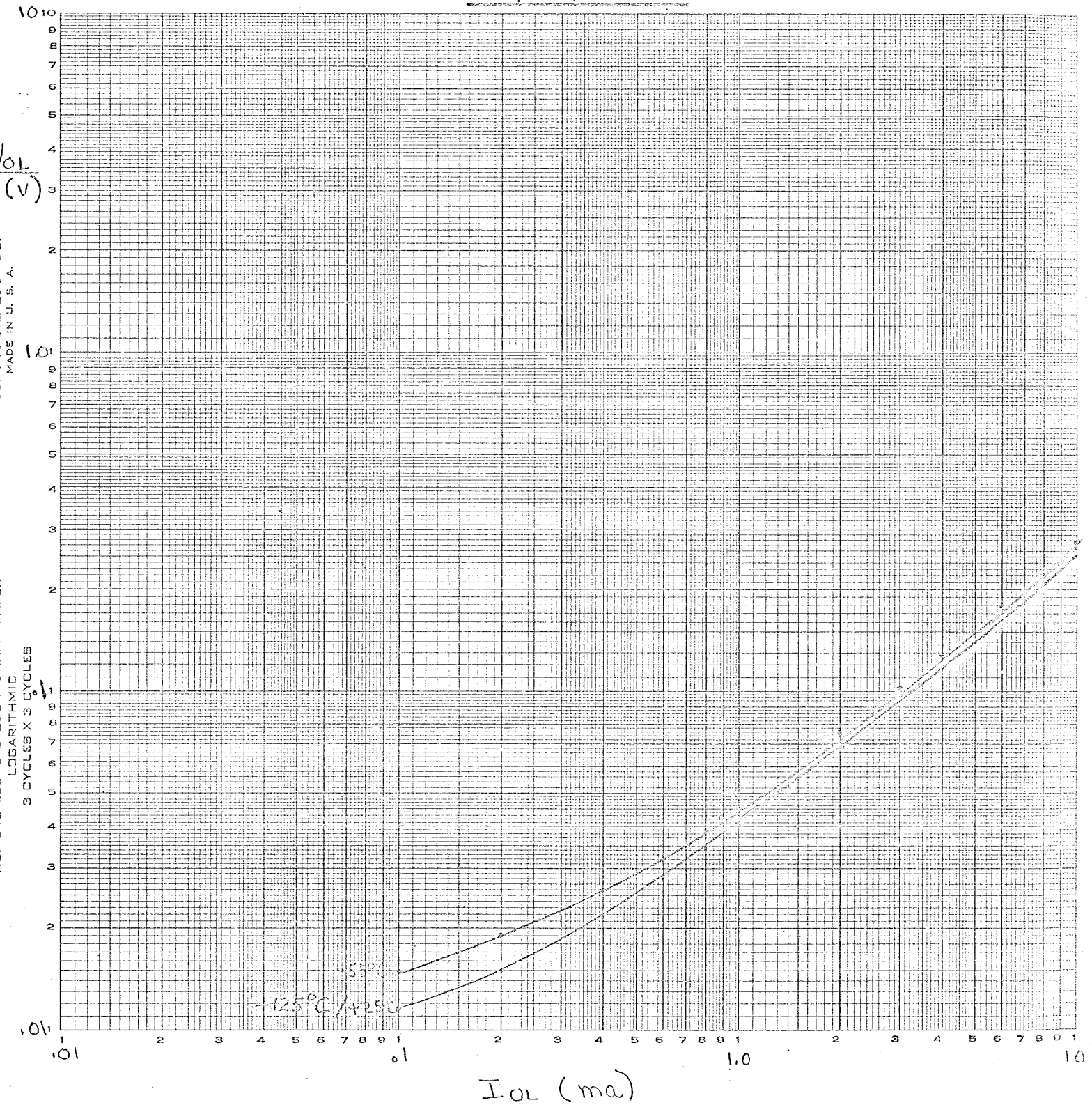


DRIVER GATE

V_{OL} vs I_{OL}

$V_S = 5.5V$

FIGURE 3.3-44



DRIVER Gate

VOL VS IOL

VS: 3.6V

FIGURE 3.3-45

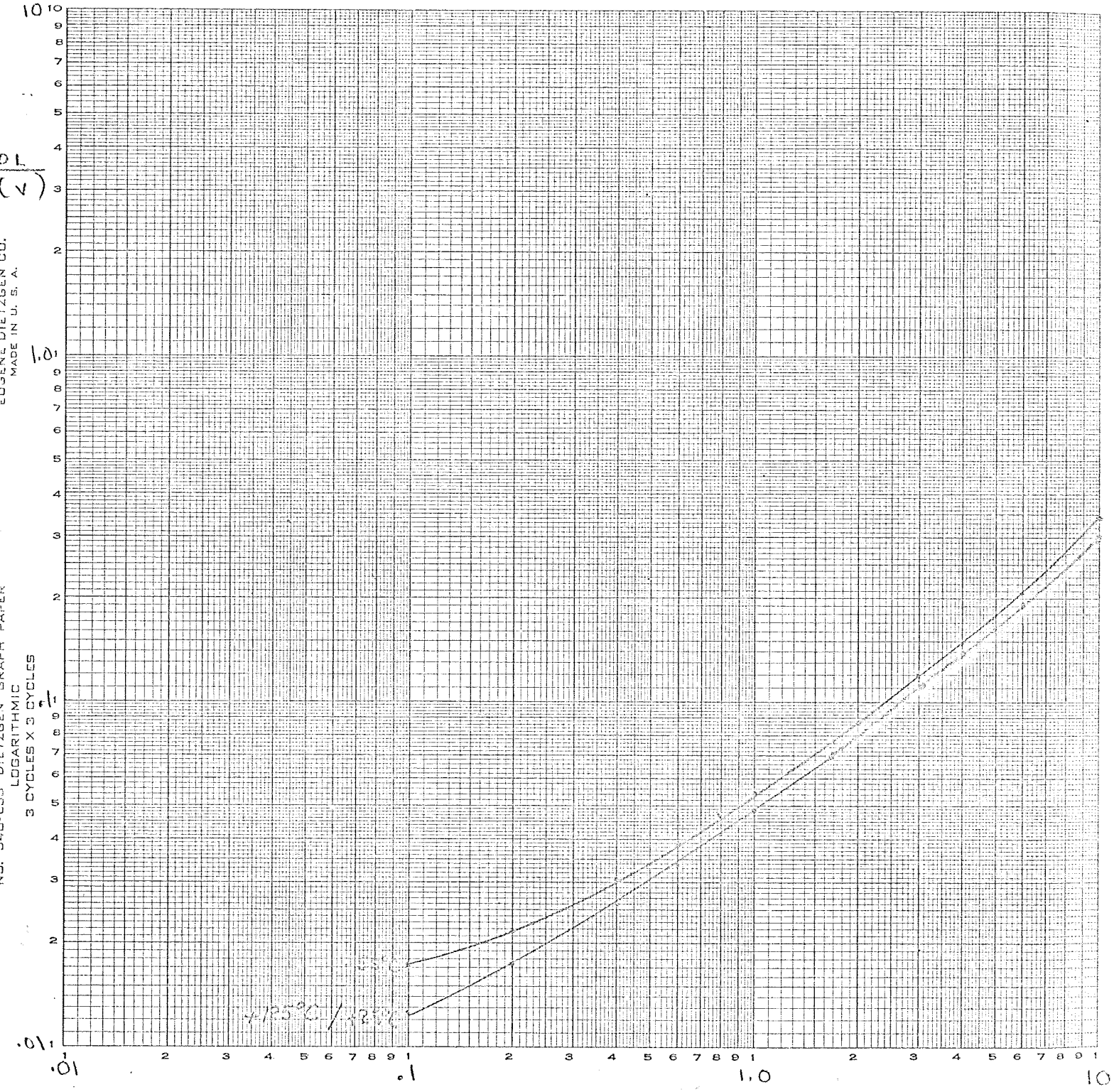


FIGURE 3.5-16

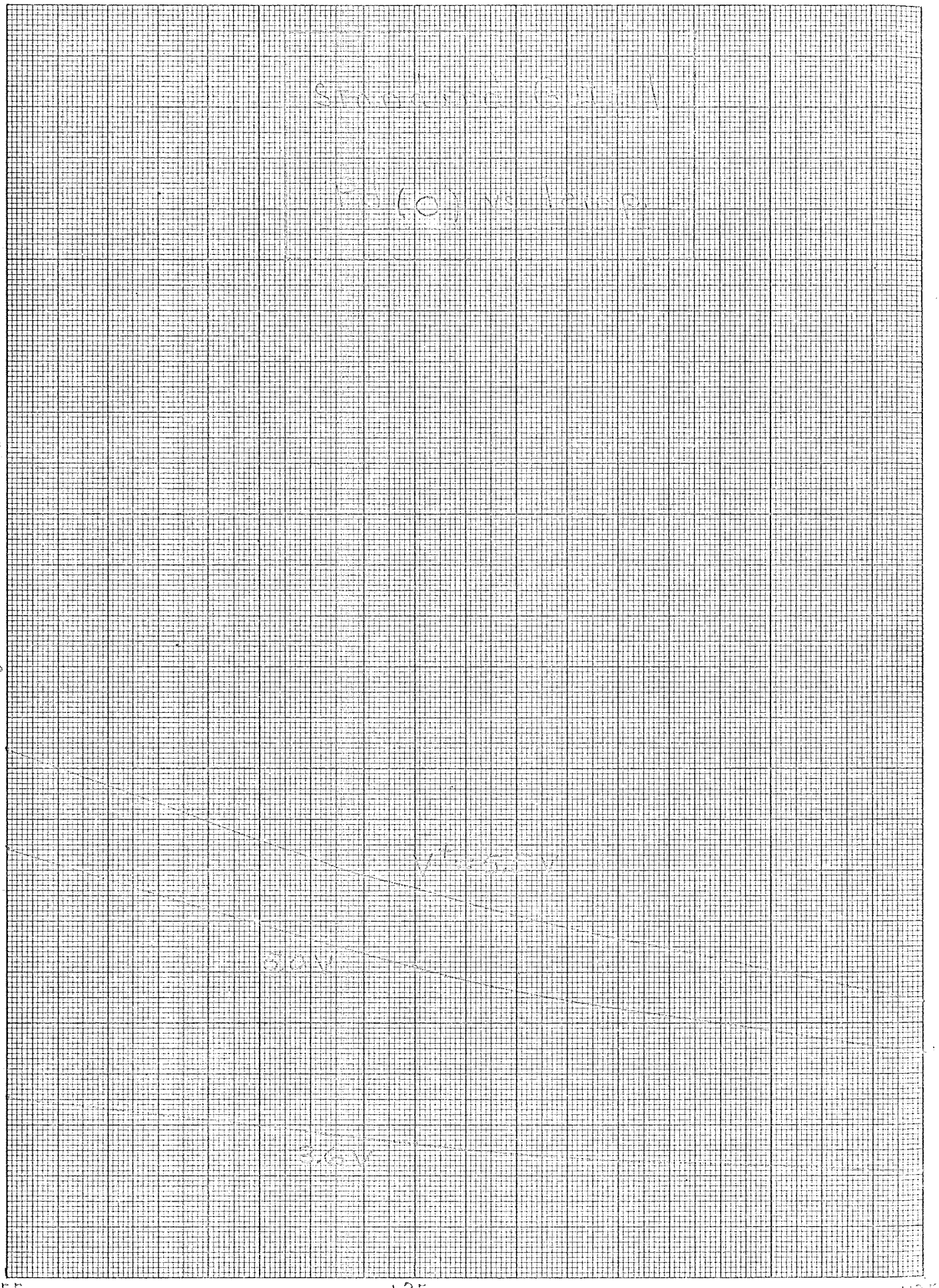


FIGURE 3.3-47

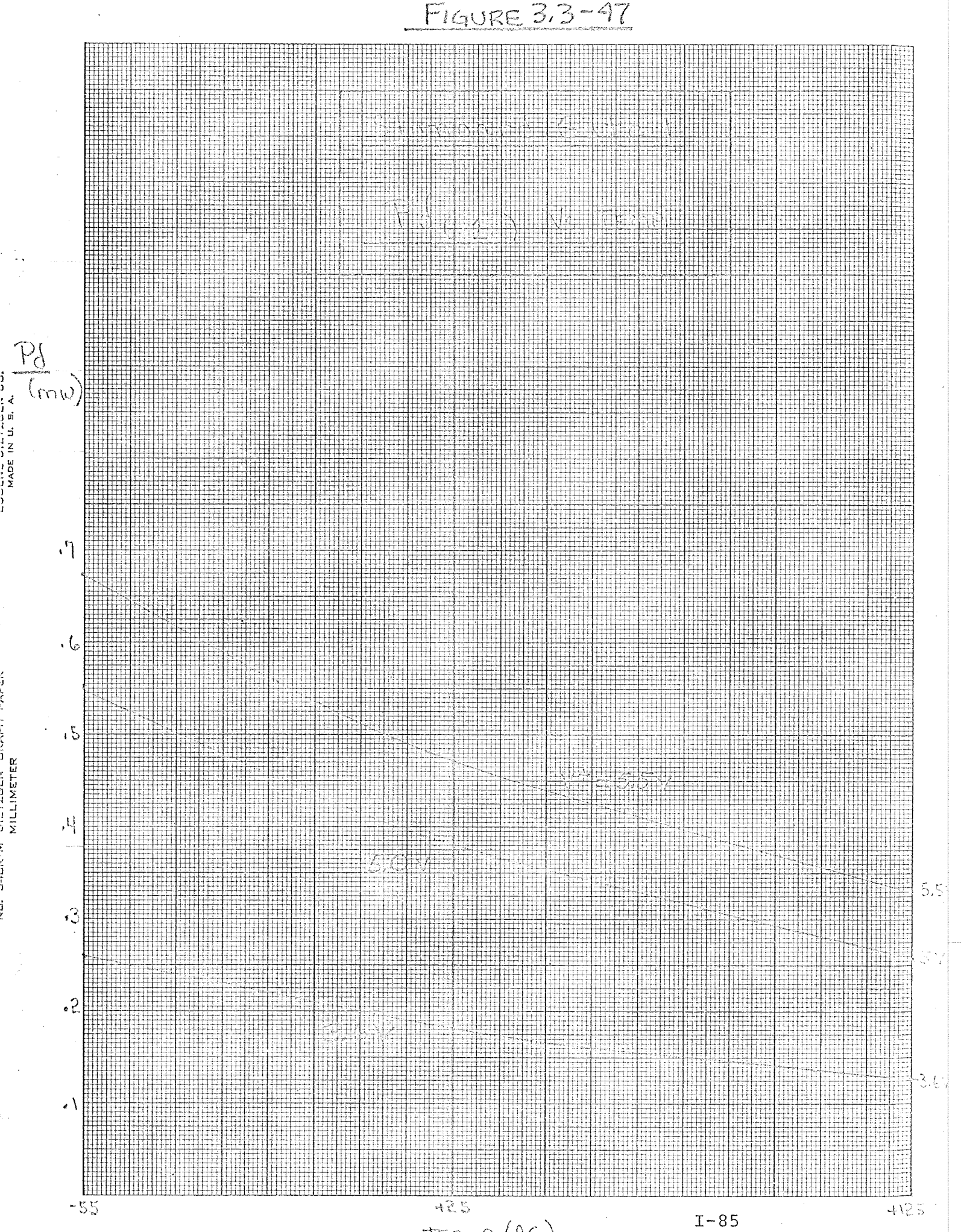
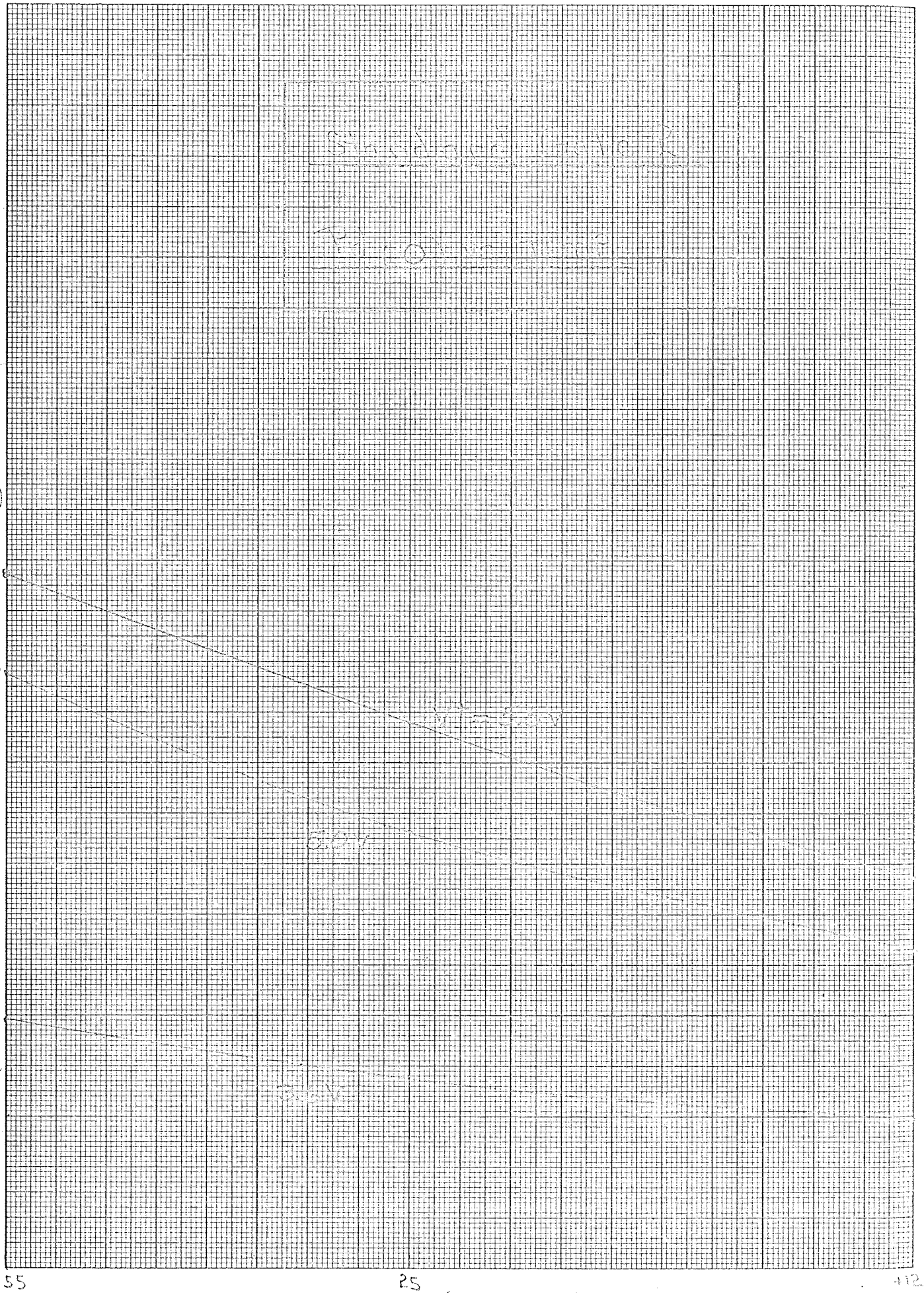


FIGURE 3.3-48



EUGENE DIETZGEN CO. MADE IN U. S. A.

NO. 340R-M DIETZGEN GRAPH PAPER MILLIMETER

FIGURE 3.3-49

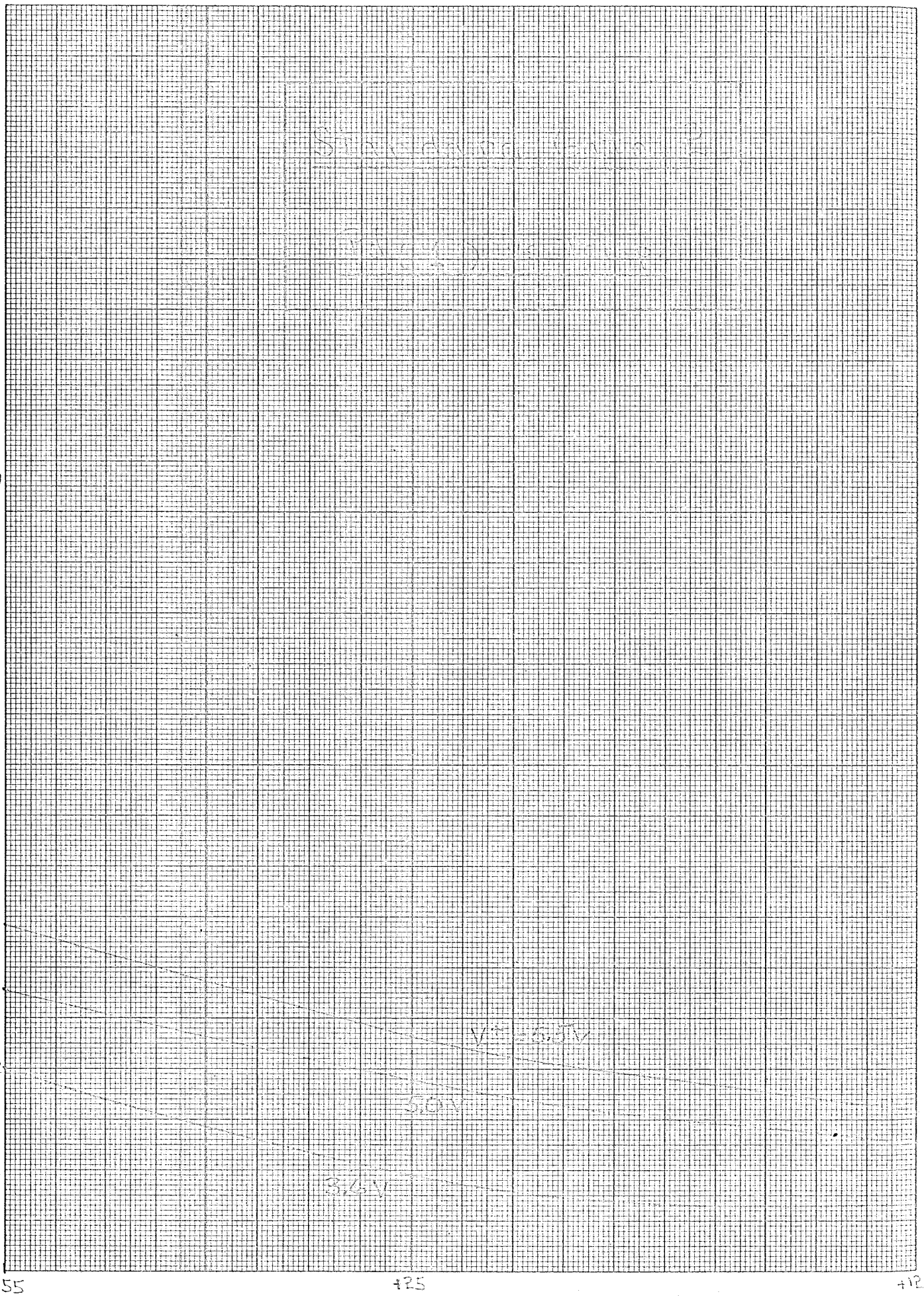


FIGURE 3.3-50

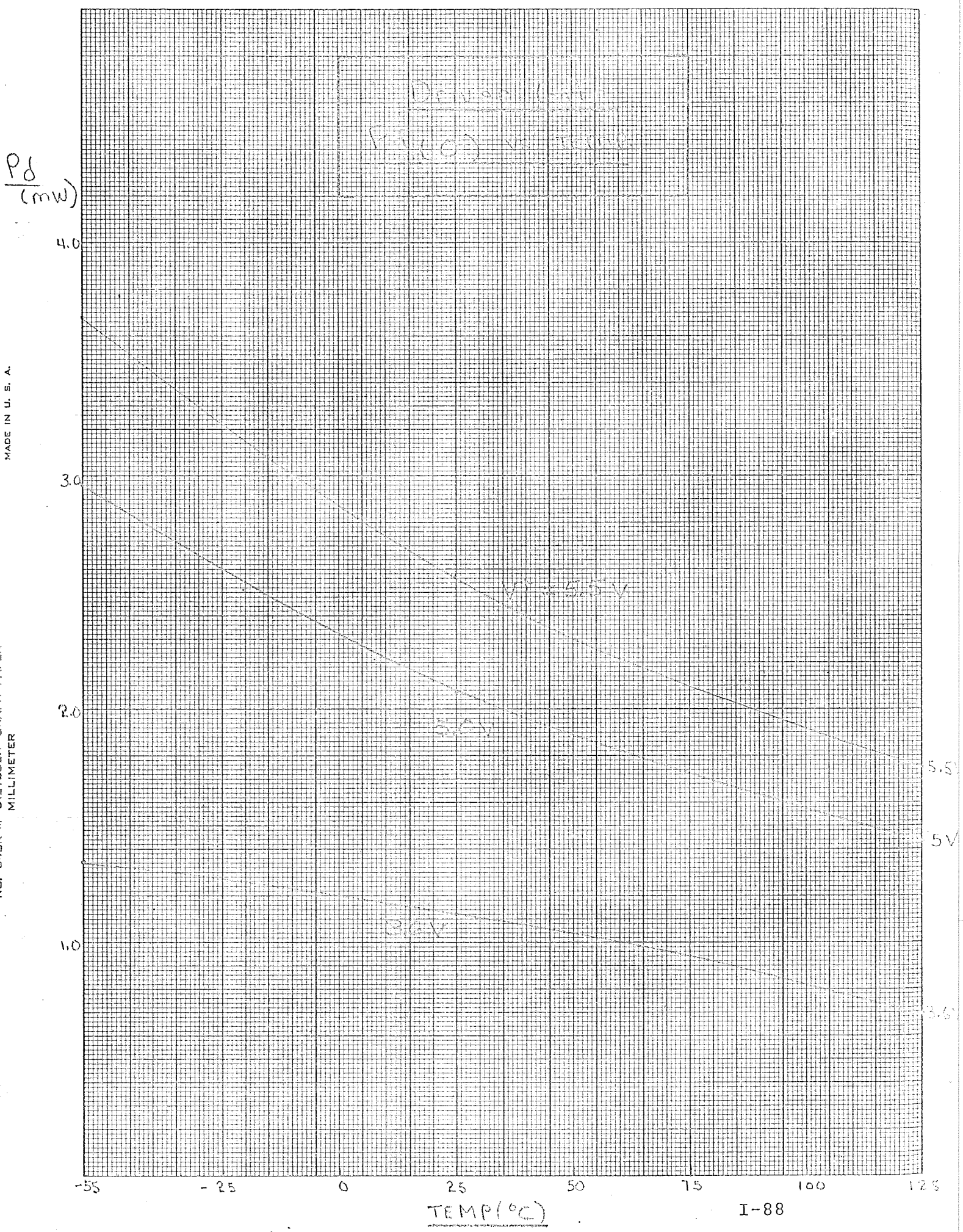
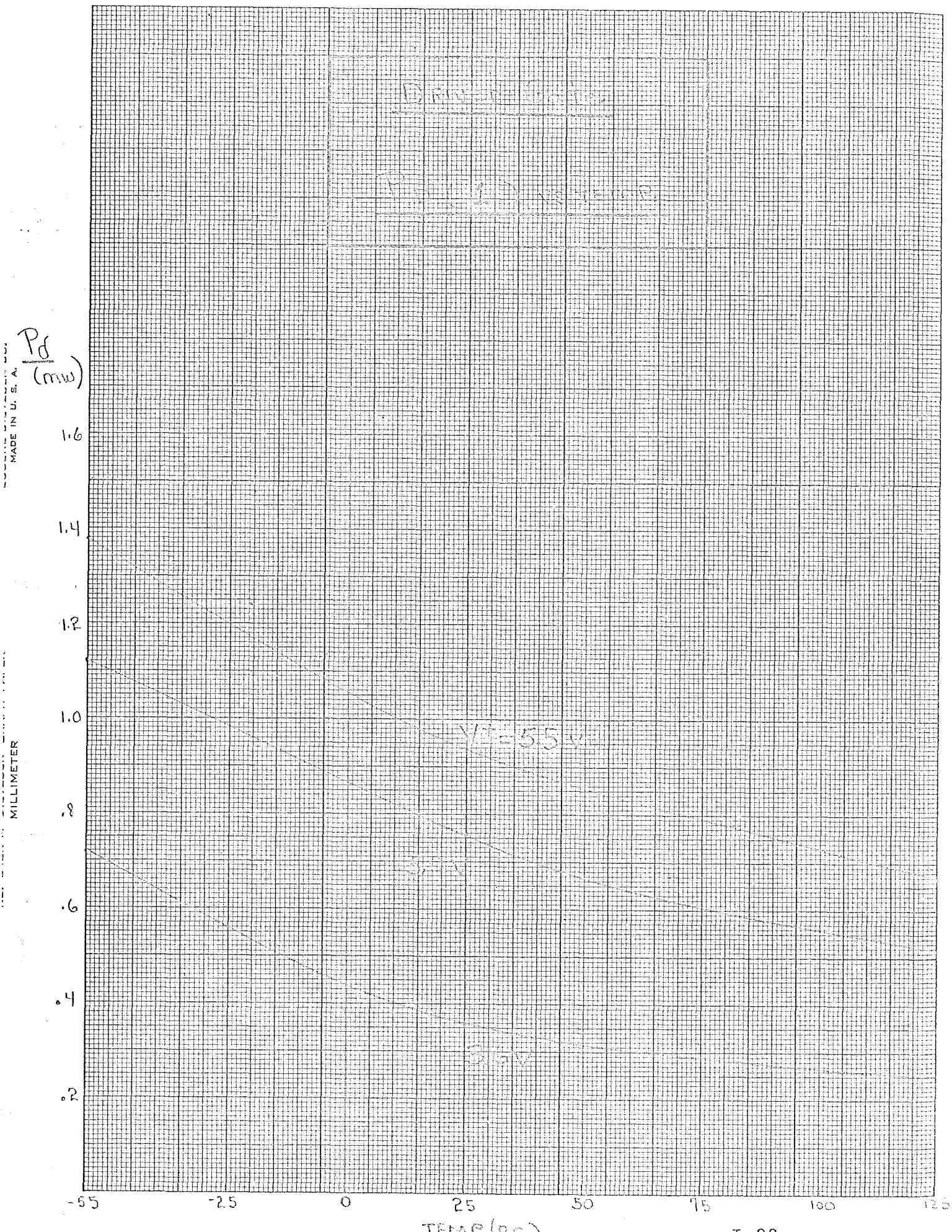


FIGURE 3.3-51


Pd (mw)
1.6
1.4
1.2
1.0
.8
.6
.4
.2
-55
-25
0
25
50
75
100
125
TEMP. (°C)
MILLIMETER
MADE IN U. S. A.

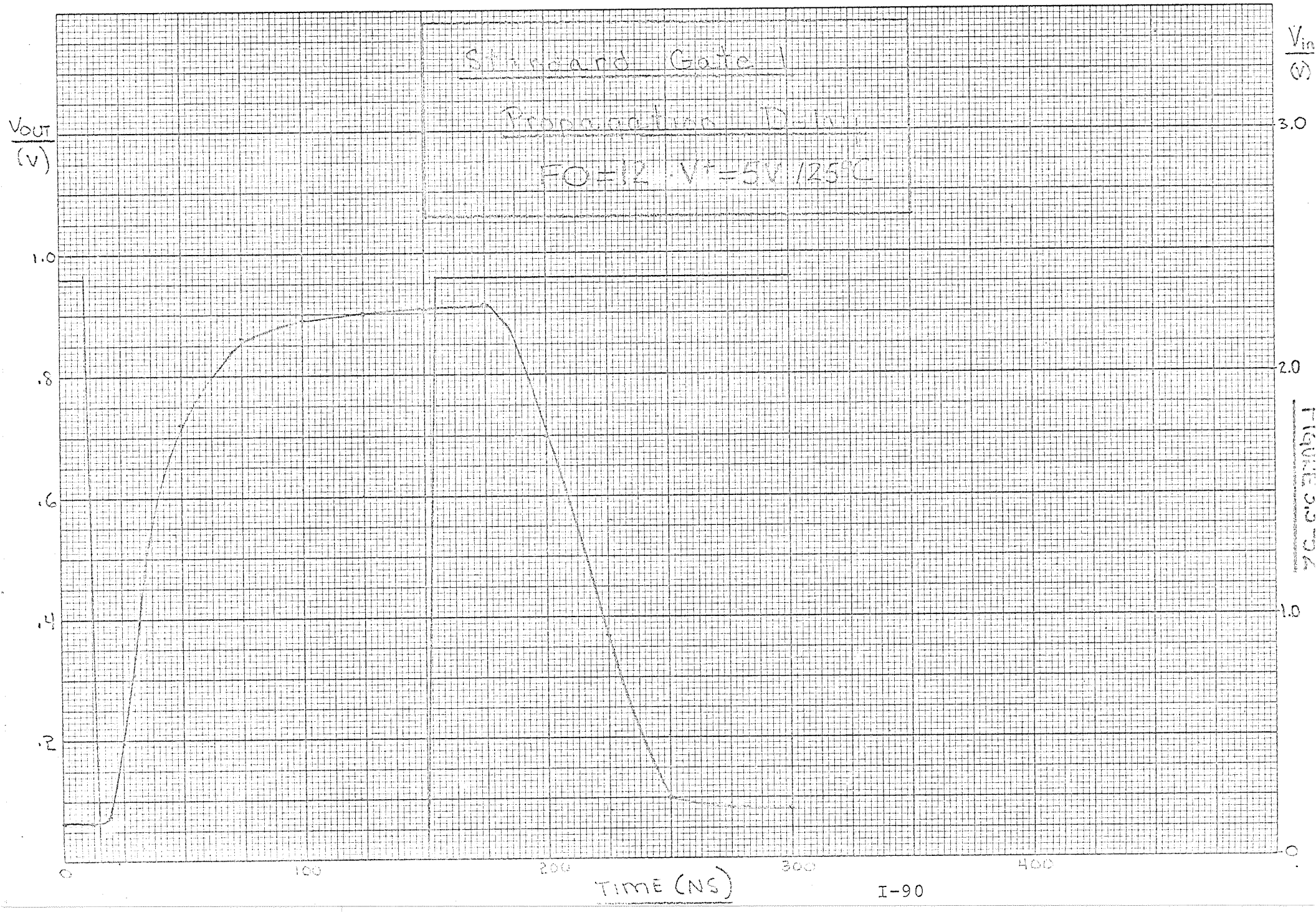


FIGURE 23-57

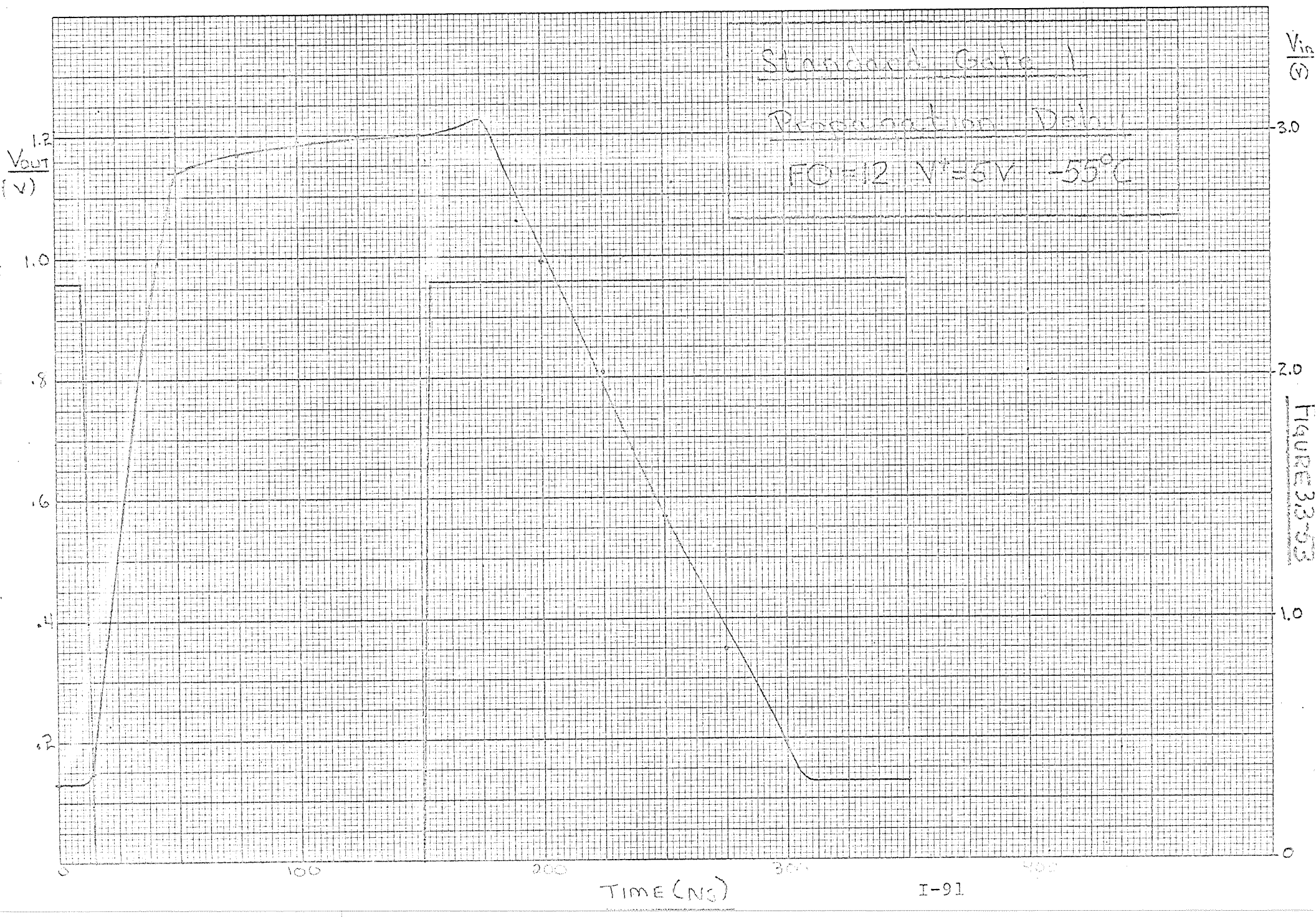
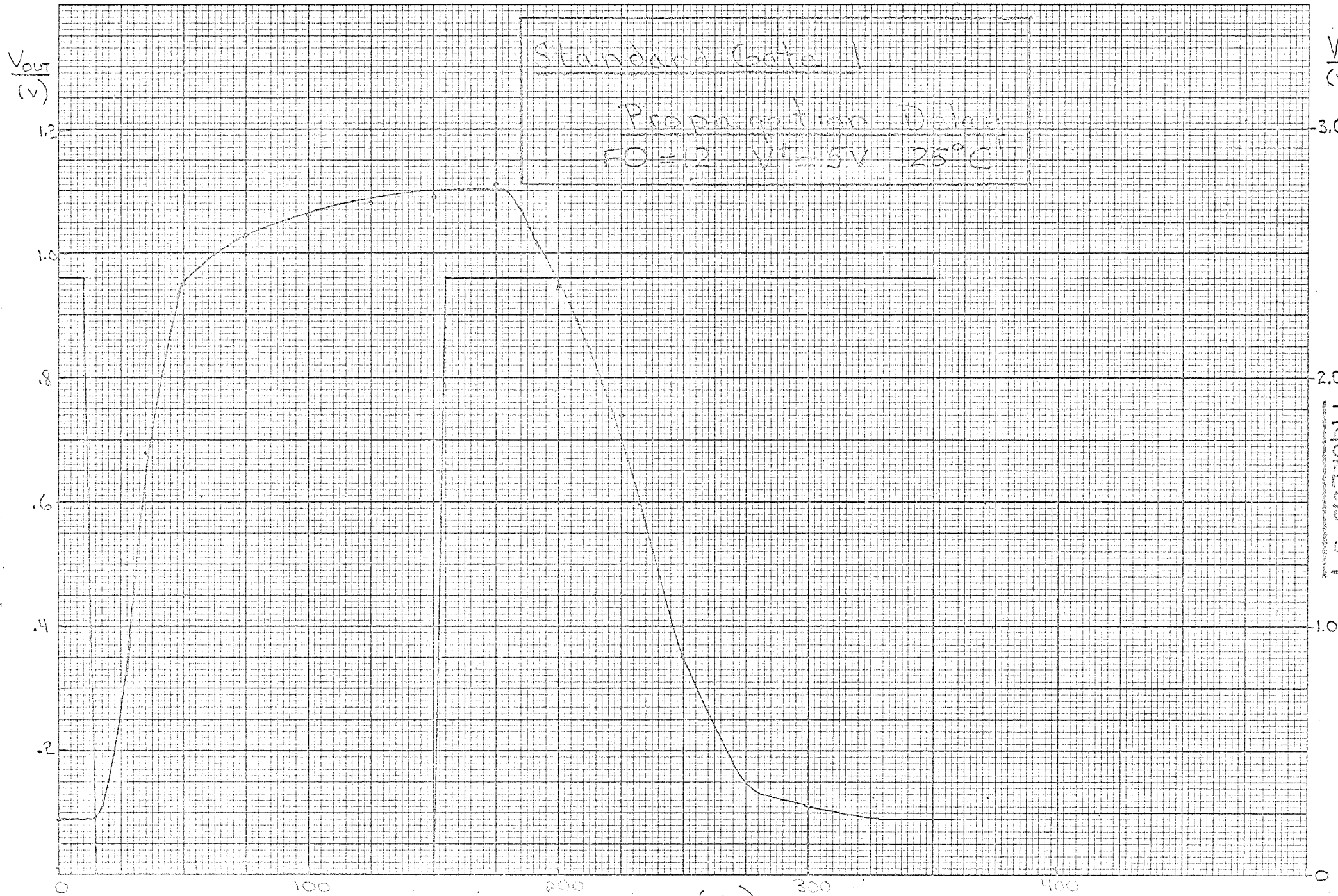


FIGURE 3333



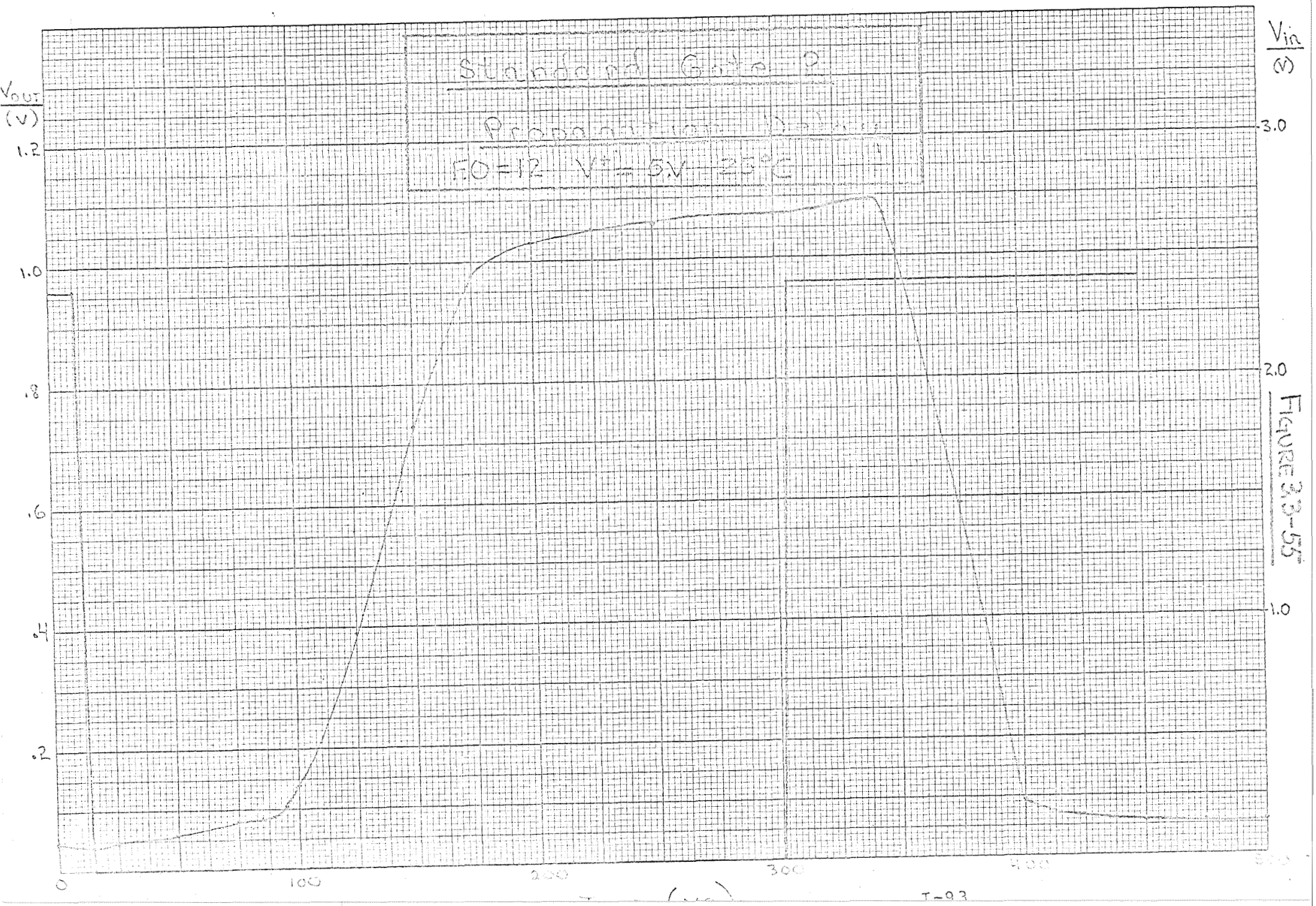


FIGURE 3.3-56

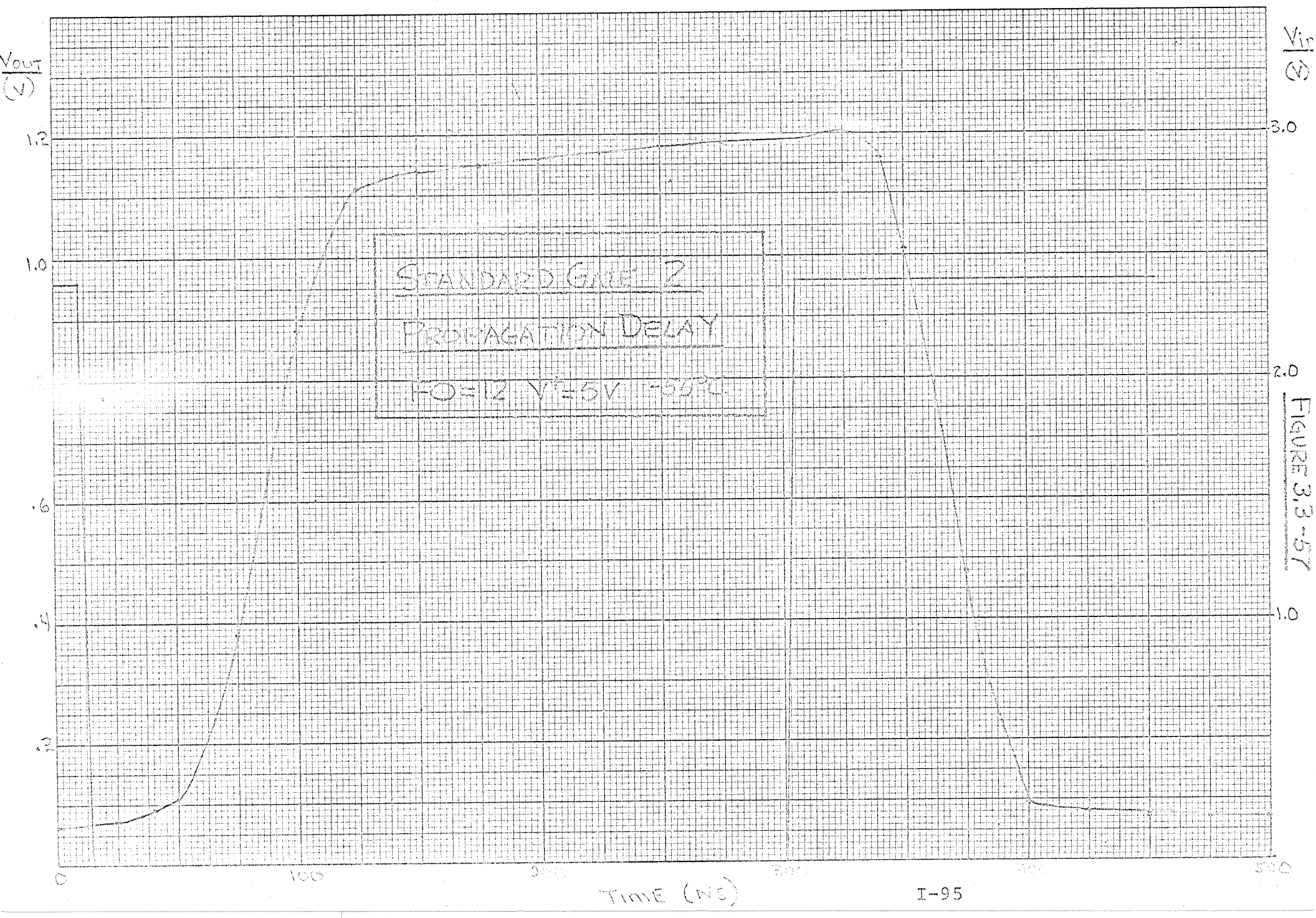


FIGURE 3.3-67

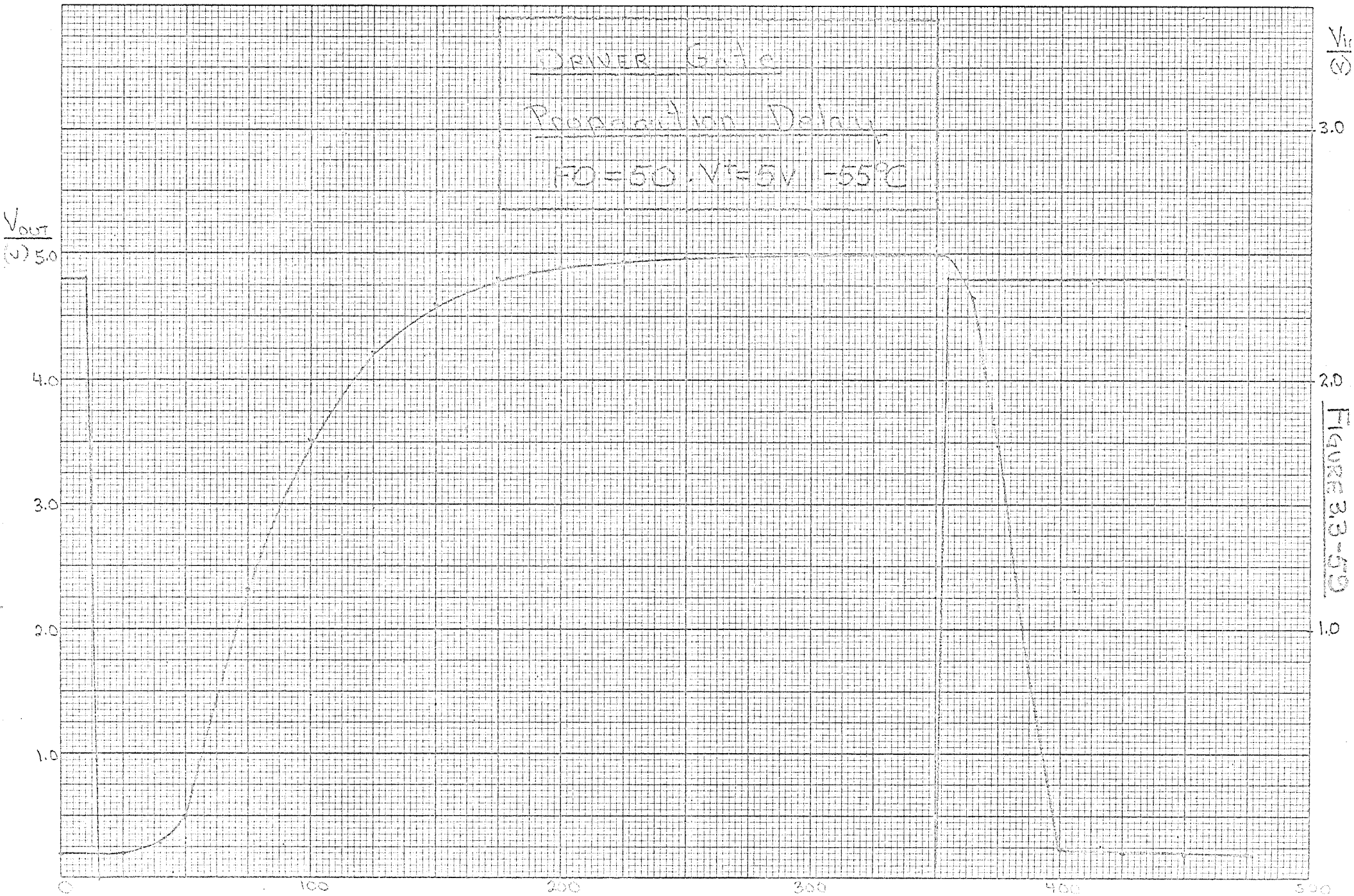


FIGURE 3.3-65

FIGURE 3.3-58

FIGURE 3.3-60

3.4 The Epitaxial Base Process

The epitaxial base process method as it relates to the structure of the devices and resistors and the predicted characteristics of these devices and resistors will be discussed in this section. The trade-offs required to obtain the necessary device characteristics and the actual mechanization of the process will also be discussed. The concluding part of this section will be devoted to the reliability aspects which relate to the specific design and process method used.

3.4.1 Device and Resistor Structures

The basic device layer structure for the epi-base transistor is shown in Figure 3.4-1. The layer structure for the pinch resistor is shown in Figure 3.4-2. The pertinent layers of the structure are the substrate, buried layer, collector, and emitter. It should be mentioned that all of the junctions of concern can be treated as abrupt junctions, since the donor concentrations in the buried layer, collector and emitter are much greater than the acceptor concentration in the base epitaxial layer.

3.4.1.1 The substrate or starting material is p-type silicon. The resistivity is 11-15Ω-cm with an acceptor concentration of $8 \times 10^{14}/cm^3$ to $1.3 \times 10^{15}/cm^3$. This results in a high resistance leakage path through the substrate and low junction capacitance to the substrate.

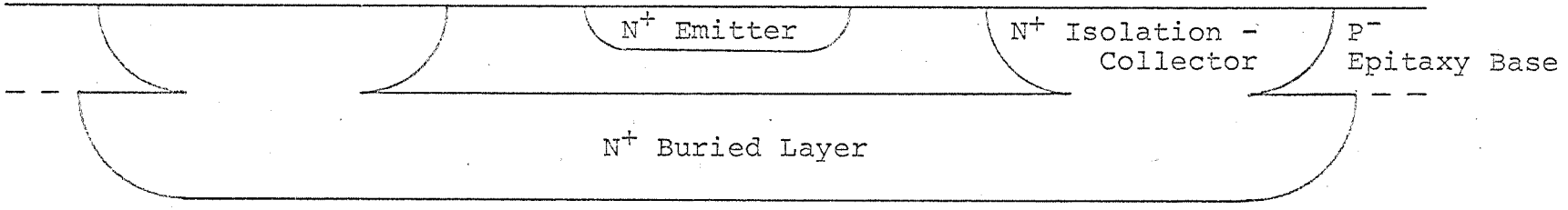


Figure 3.4-1 Epitaxial Base Transistor

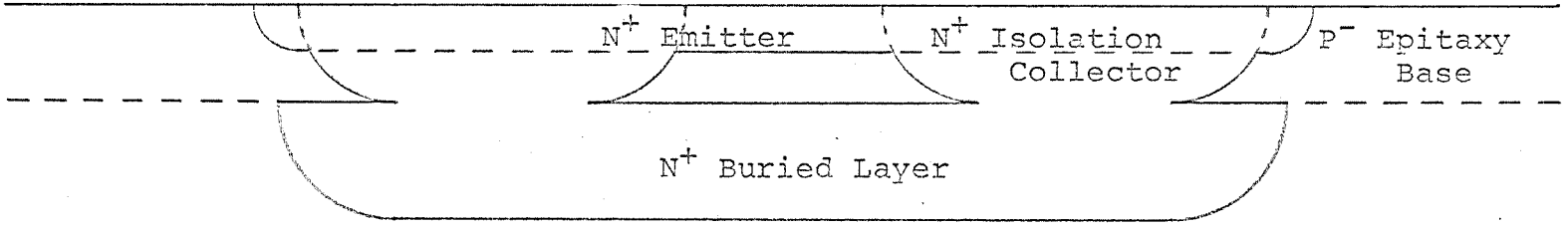


Figure 3.4-2 Epitaxial Base Pinch Resistor

The structure starts with a selective N^+ diffusion into the substrate. This diffusion is used to isolate the bottom of the structures to be built and to provide a low resistivity layer which will become the active collector of the transistors. The sheet resistivity of this layer (which will eventually form the buried layer) is approximately 40 to 45Ω/□ at a depth of 3.8 to 4.2 microns resulting in a surface donor concentration of about $2 \times 10^{19}/cm^3$.

3.4.1.2 The next layer is the base layer. This layer is epitaxially grown using boron as a doping species. The epitaxial P layer resistivity is 0.45 to 0.55Ω-cm with an acceptor concentration of about 3 to 4 x 10^{16}/□ cm^3 and is 2.3 to 2.6 micron thick.

3.4.1.3 The collector or isolation diffusion makes contact with the buried layer and hence completely isolates an island of epitaxial material. This is typically a 2 to 3Ω/□ diffusion of 2.6 micron depth and a surface donor concentration of $2.5 \times 10^{21}/cm^3$.

3.4.1.4 The transistor structure is then completed with an N type diffusion in the isolated island to form the emitter. The characteristics of the layer are similar to the collector-isolation except for the depth. It should be mentioned that the depth of this diffusion and the thickness of the epitaxial layer are extremely

critical since they fix the base width of the transistor. Transistors have been fabricated with base widths from 0.6 to 1.2 microns.

3.4.1.5 The method used to fabricate the resistors is compatable with the above mentioned structure. The only feature different is that the emitter N-type diffusion overlaps the isolation diffusion to form a layer of buried epitaxial P-type material. Again, the epitaxial thickness and the emitter diffusion are critical since this also fixes the thickness of the pinched resistor and hence determines the value of pinched sheet resistivity.

3.4.2 Epitaxial Base Layer Resistivity

The reverse bias breakdown voltage is controlled by the resistivity of the high resistivity side of all junctions. Hence, for all junctions except the substrate-buried layer junction, the base epitaxial resistivity controls the main junction characteristics.

3.4.2.1 Junction Characteristics

Since the base layer is uniformly doped, it also has a low surface donor concentration and hence is subject to surface inversion. This problem and a corrective measure will be discussed in more detail in Section 3.4.3. The junction characteristics for the junctions involved are given in Table 3.4-1.

TABLE 3.4-1

JUNCTION	DEPLETION WIDTH MICRONS	BREAKDOWN VOLTAGE VOLTS	CAPACITANCE pF/cm^2
Substrate - Buried layer	20	> 100	5×10^2
Buried layer- Epi base	0.3	25	4×10^4
Isolation- Epi base	0.4	30	2.5×10^4
Emitter-	0.35	25-30	3×10^4

The depletion layer width and the capacitance are given for a junction voltage of 2.5 volts reverse bias.

3.4.2.2 BV_{CEO} For Epitaxial Base

Note in Table 3.4-1 that the calculated breakdown voltage of the buried layer and isolation junctions are not equal; however, since the two junctions are connected, the collector-base breakdown will occur at the lower value. This is an important consideration in selecting the base resistivity since the value of the collector-emitter breakdown voltage is related to the collector-base breakdown and the current gain of the transistor through the equation.

$$BV_{CEO} = \frac{BV_{CBO}}{n\sqrt{H_{FE}}}, \text{ where } n = 3.75 \text{ to } 4.0.$$

If a lower resistivity is used for the base, then BV_{CBO} is reduced and for a given H_{FE}, the requirement on BV_{CEO} can not be satisfied. A high resistivity base means a lower acceptor concentration in the base and hence, enhances the possibility of surface inversion.

3.4.3 Trade Offs

One experimental run was made to establish the basic process parameters. The results of this run strongly indicated that surface inversion was indeed occurring over the base region.

3.4.3.1 Base Deposition

In order to eliminate the base surface inversion problem, it is necessary to increase the base surface concentration.

There are two approaches to this problem, (1) a selective guard-ring boron deposition-diffusion or (2) a non-selective boron deposition-diffusion.

3.4.3.2 Selective or Non-Selective Base Deposition

The first approach would require larger geometries over the entire circuit area, since guard rings would be necessary not only between emitter and collector in a given transistor but also between transistors. This approach would remove the main advantage of using the epitaxial base method, since it would add a photo resist step and also increase the geometry.

3.4.3.3 Reason for Non-Selective Base Deposition

The second approach was therefore considered the most desirable for both process and size considerations. The non-selective boron deposition is made over the entire surface of the slice. During this process step, the boron remains at the surface of the slice and hence does not reduce the lifetime of the minority carriers in the active base region or the injection efficiency of the active emitter area. There is an added feature here since the lateral injection of the emitter is reduced and hence the lateral current gain between two emitters is reduced.

3.4.3.4 BV_{CEO} Versus BV_{CEOS}

The increase in base surface concentration reduces the

value of the reverse bias breakdown voltage between collector and base. This breakdown voltage is denoted as BV_{CBOS} in contract to BV_{CBO} under the active emitter area. This is an important consideration since BV_{CBOS} may occur before the active transistor goes into the avalanche condition.

$$\text{If } BV_{CBOS} < \frac{BV_{CBO}}{(H_{FE})1/n}, \text{ then}$$

$$BV_{CEOS} = BV_{CBOS} + V_F$$

where V_F is the forward potential of the emitter base junction. This is summarized in Figure 3.4-3 and Figure 3.4-4. Figure 3.4-3 is a plot of BV_{CEO} versus H_{FE} for a given BV_{CBO}. Figure 3.4-4 is a plot of BV_{CEOS} versus the base surface concentration. A plot of surface state density required for onset of inversion is also included in Figure 3.4-4.

For a surface carrier concentration of $4 \times 10^{16}/cm^3$, a surface state density of $4.3 \times 10^{11}/cm^2$ will cause surface inversion. Normal processing may result in surface state densities as high as $10^{12}/cm$ with surface inversion for P-type material occurring at a surface carrier concentration of $2 \times 10^{17}/cm^3$. The minimum surface concentration in the base region to assure that surface inversion does not occur is between

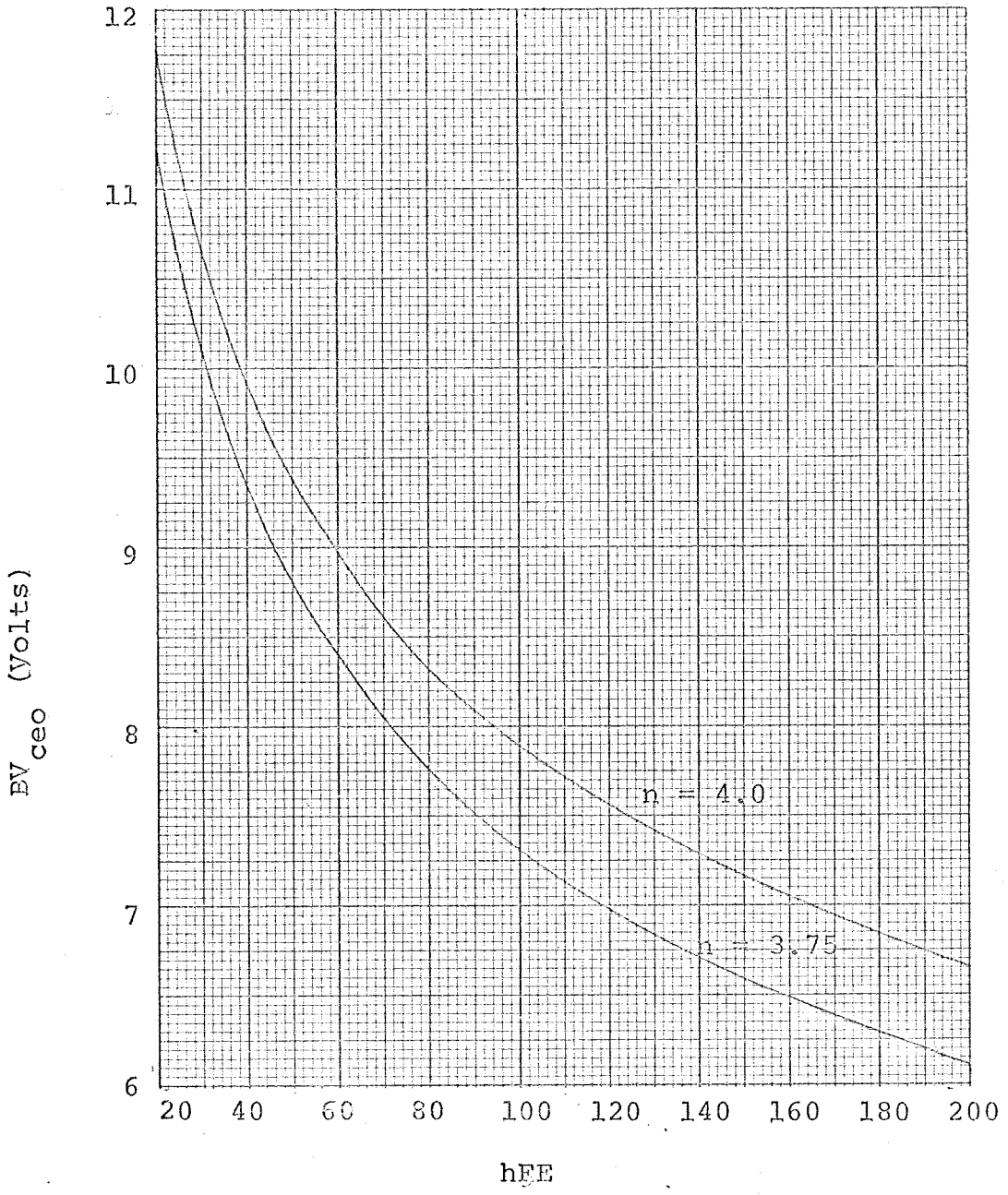


Figure 3.4-3 BV_{ceo} versus hFE

$$BV_{ceo} = \frac{BV_{cbo}}{\sqrt[n]{hFE}}, \quad BV_{cbo} = 25 \text{ volts}$$

n = 4 and 3.75

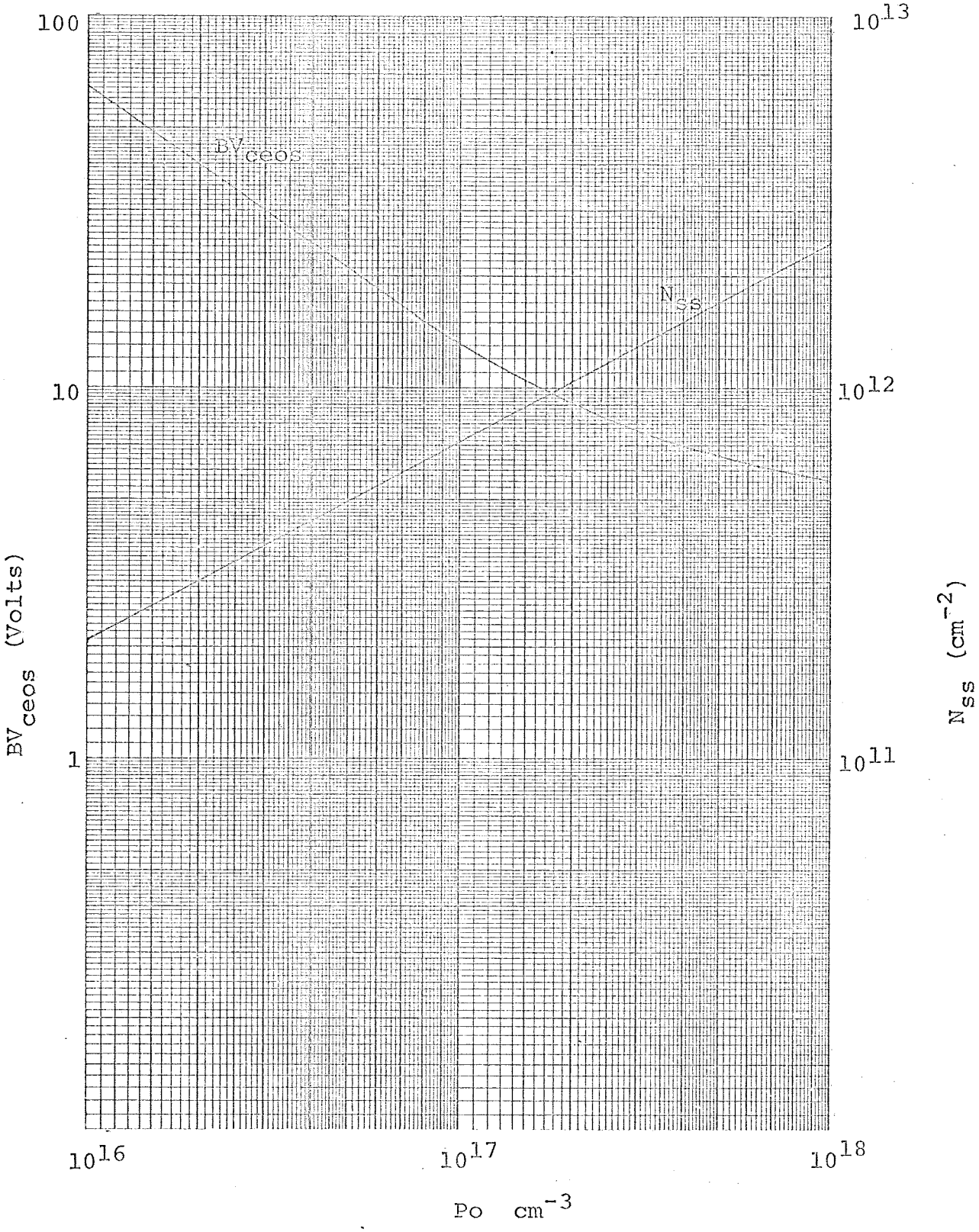


Figure 3.4-4 BV_{ceos} and critical inversion surface density for various base concentrations

2 and 3 x $10^{17}/cm^3$. From Figure 3.4-4, BV_{CEOS} is found to be 7.6 and 9.1 volts. The above mentioned considerations have not included any effect of a positively biased metal line.

3.4.3.5 Recommendations

The preceeding considerations can now be summarized. The surface concentration in the epitaxy base material must be greater than 2 x 10^{17} to eliminate inversion. This results in a BV_{CEOS} controlled by the base surface breakdown voltage and not by the active base avalanche condition of the transistor. The maximum obtainable BV_{CEO} is 9.1 volts. Any increase in surface state density due to slight variations in processing or the effects of radiation would be a potential inversion condition using this upper limit. The most acceptable condition would be to have a base surface concentration of a least 4 x $10^{17}/cm^3$ with a resulting BV_{CEOS} of 7 volts as a maximum.

3.4.4 Fabrication

The main steps in the epitaxial process for the CMMA are given below.

3.4.4.1 Process

1) Oxidation
2) Photo resist for buried layers
3) Buried layer N diffusion

4) Oxide removal

5) Epitaxial deposition

6) Oxidation

7) Photo resist for isolation-collector

8) Isolation-collector N diffusion

9) Oxide removal

10) Non-selective base P deposition

11) Oxidation

12) Photo resist for emitter

13) Emitter N^+ diffusion

14) Oxidation

15) Photo resist for contacts

16) Aluminum evaporation

17) Photo resist for aluminum interconnect

18) Insulating oxide deposition

19) Photo resist for via etch

20) Aluminum evaporation

21) Photo resist for second layer interconnect

22) Contact and stablization bakes

3.4.4.2 In Process Controls

There are several checks made to assure that the process results are as expected. After each diffusion, the resistivity of the layer is checked by four-point probe measurements and the layer thickness is measured by lap and stain methods. The collector base breakdown is checked after the collector isolation diffusion and after the non-selective base deposition and

subsequent oxidation. The parameters of the transistors are checked after the N^+ emitter diffusion. The sheet resistivity of the pinched resistors is checked at this point also. These in process checks are designed to allow maximum control of the process parameters and to monitor the device parameters at each process step.

3.4.4.3 Device Data

Device characteristics from several devices are shown in detail in another section of this report; however, the results of two groups of devices are presented along with the life test data obtained from these devices after fixed periods of time at 4 volt reverse bias at 150°C. The devices used in this life test were fabricated with a non-selective base deposition. Devices fabricated without the non-selective base deposition were not acceptable for life test consideration since the room temperature leakage currents were so high. In fact it was not possible to obtain beta curves on these devices due to the leakage between collector-emitter.

Initial Room Temperature Data

Run EB - 4B1; Test Group BB16

H_{FE}	BV_{CEO}@10μA	BV_{CBO}@10μA	BV_{EBO}@10μA
1mA@ 2.5V	Volts	Volts	Volts
36	8.5	10.7	7.0
33	10.0	11.0	7.2
29	8.1	11.6	7.0
37	10.2	11.0	6.9
33	9.0	10.8	7.5
42	9.7	9.8	7.1
30	8.2	11.5	6.6
31	10.5	10.8	6.9
30	10.5	11.6	7.0
31	9.5	11.6	7.2
46	8.0	11.3	7.1
31	7.5	10.8	7.2
33	8.0	11.2	7.2

The non-selective P base deposition for this run resulted in a base surface concentration of 1 to 1.5 x $10^{17}/cm^3$. This is considered the lower limit of the base surface concentration to prevent inversion.

Reverse Bias Leakage Data

Run EB-4B1 Test Group BB16

V_{BC} = -4 volts T = 150°C 13 units

Hours of Test	I_{EBO}@5V nA	I_{CEO}@4V nA	I_{CBO}@5V nA
0	0.5 - 7.0	8 - 32	1 - 18
48	0.3 - 6.0	1 - 7.6	1 - 17
96	0.1 - 6.0	1 - 8.2	1 - 16
168	0.1 - 5.2	1 - 8.0	1 - 16
500	1 - 7.6	1 - 8.1	3.6 - 20

Devices from another run are now also on reverse bias. The non-selective base deposition for this run resulted in a base surface concentration of $3 \times 10^{17}/cm^3$.

Initial Room Temperature Data

Run EB - 6C Test Group BB45

H_{FE} 1mA@ 2.5V	BV_{CEO}@10μA Volts	BV_{CBO}@10μA Volts	BV_{EBO}@10μA Volts
98	7.9	7.5	7.1
110	7.8	7.4	7.0
96	8.0	7.6	7.1
138	8.2	7.7	6.9
132	8.9	8.0	7.2
128	7.8	7.5	7.1
134	7.9	7.4	7.1
172	7.7	7.9	7.2
108	8.0	7.4	7.0

H_{FE}	BV_{CEO}@10μA	BV_{CBO}@10μA	BV_{EBO}@10μA
1mA@ 2.5V	Volts	Volts	Volts
134	7.8	7.7	6.9
138	7.8	7.2	6.8
200	8.2	7.7	6.7
105	8.0	7.4	7.1
125	7.6	7.3	6.7
120	7.8	7.3	6.6
152	8.0	7.4	6.6

Reverse Bias Leakage Data

Run EB-6C — Test Group BB45

V_{CE} - 4 volts — T = 150°C 16 units

Hours of Test	I_{EBO}@ 5V nA	I_{CEO}@ 4V nA	I_{CBO}@ 5V nA
0	<1	<2	<1
48	<1	<1.8	<1

3.4.4.4 Pinch Resistors

Pinch resistors have also been fabricated using the same process method as for transistors. In the resistor pattern presently being used, the emitter diffusion overlaps the isolation-collector diffusion and hence the voltage restriction on the resistors is BV_{EBOS}.

For the base width used in the transistors and using the resistivity of the epitaxial layer, the resistors have a calculated pinch-off voltage of about 7 volts. This agrees with the measured values of 6 to 7 volts.

The sheet resistance of the pinch resistors is of the order of 10 to 12 $K\Omega/\square$ for a base width of 1 micron. This is in agreement with the calculated value if the 0 bias depletion width of both top and bottom junctions is taken into consideration.

In calculating the value of the pinch-off voltage and the sheet resistance, the physical measurement of the base width is needed. The accuracy of this measurement is $\pm$ 1/2 sodium line or approximately $\pm$ 0.15 microns. For this reason, the emitter diffusion process is controlled and checked by measuring the resistance of the pinch resistors.

3.4.5 Reliability Considerations

A most important consideration of the total program is the long term reliability of the product. There are of course several potential failure modes in all devices; however, one of the primary concern is the surface inversion problem.

3.4.5.1 Necessity for Base Deposition

The importance of a high base surface concentration has been presented. The data obtained from the run without the non-selective P base deposition indicated inversion. The data presented from run EB-4B1 indicated that for a base surface concentration of $1 \times 10^{17}/cm^3$ the surface inversion problem did not exist. There is data to support the evidence of an increase in surface state density after irradiation. On metal - nitride - oxide - silicon structure, there were indicated increases of 3 to 4 in the surface state density on N-type silicon. This data may not be directly applicable to the structure used for the epitaxial base process; however, it does indicate qualitative increases in surface state density and should be a major consideration in the reliability of the product. This is especially important for the consideration of the BV_{CEO} required and in turn the base surface concentration.

3.4.5.2 New Test Structures

The above mentioned problem and other related surface problems will be investigated further in Phase II. Test structures are now in process to evaluate the specific surface state density of the process and to correlate this data with device leakage currents.

The new test structures will include:

1) A standard geometry control transistor.
2) A standard geometry transistor with field plates over collector-base and emitter-base junctions.
3) A standard geometry transistor with a field plate over the base surface from emitter to collector.
4) An MOS large area capacitor.
5) An MOM large area capacitor.
6) An inter-laced metal pattern for SiO_2 surface conductance.

These test structures will be on a die with the cell configurations such that any electrical characteristic changes in cell performance can be related to measured parameters on the test structure.

3.4.6 Process Control

The two critical process steps are epitaxial deposition and emitter diffusion. Both of these process steps determine the base width of the transistor and the pinch sheet resistance. In-process checks on resistivity and thickness of the epitaxial layer on control wafers which have an unmasked buried layer diffusion are now being used. In-process checks on the emitter diffusion are performed by measuring the resistance of the pinch resistors. These two in-process checks should eliminate one main problem, repeatability of devices and resistors from run to run.

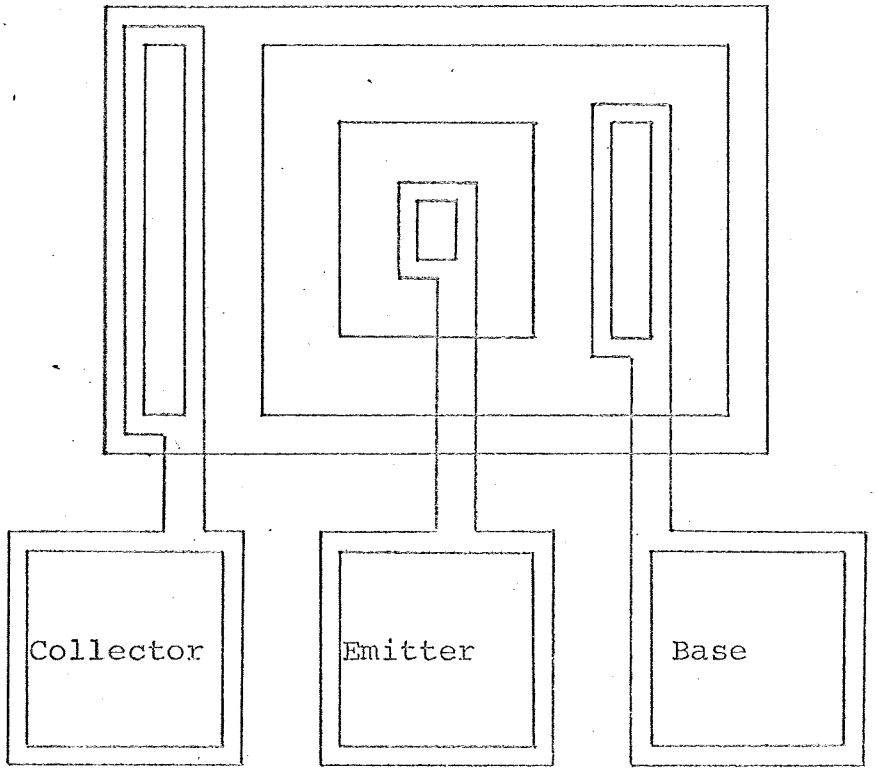


Figure 3.4-5 Standard Test Transistor

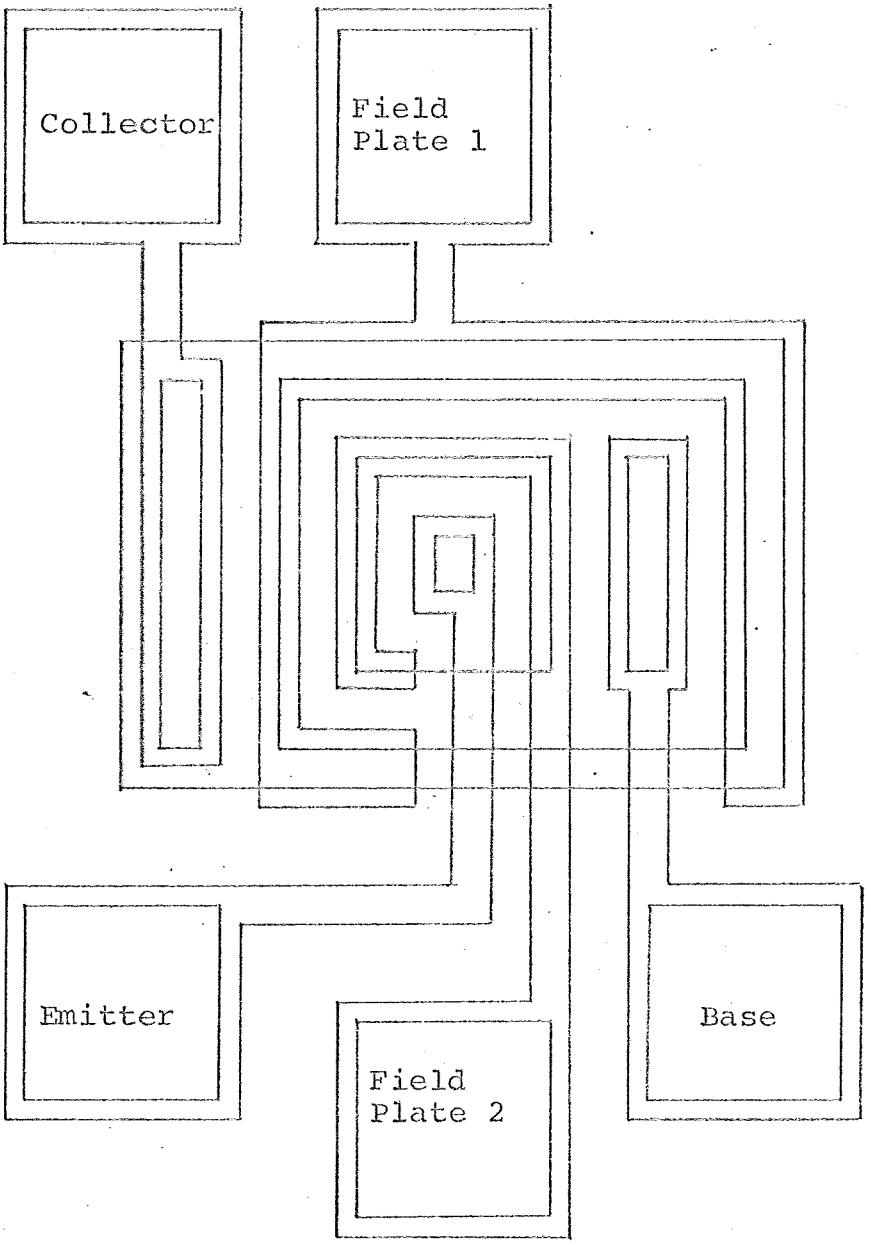


Figure 3.4-6 Standard Test Transistor with C-B and E-B Field Plates

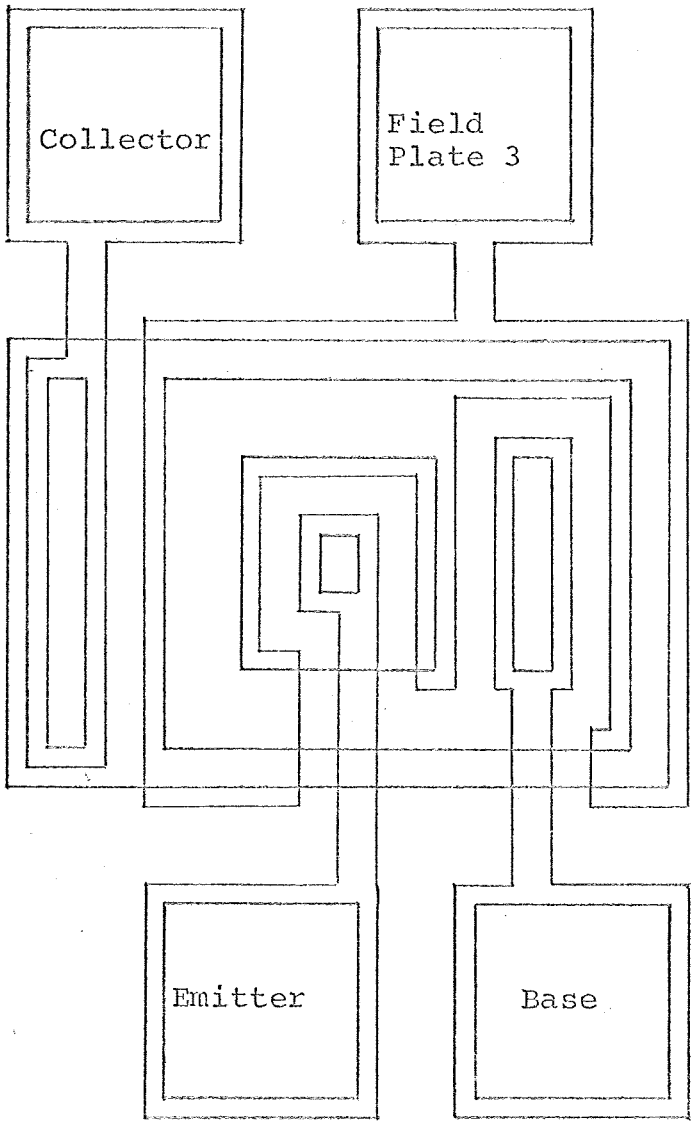


Figure 3.4-7 Standard Test Transistor with C-E Field Plate

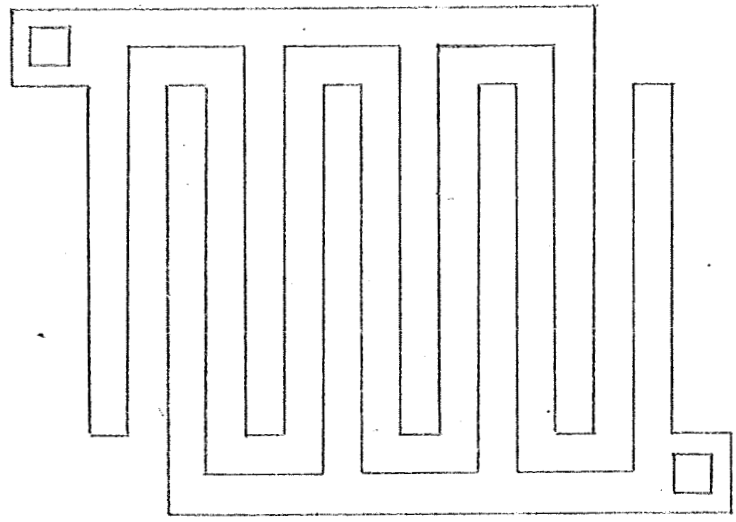


Figure 3.4-8 Test Structure for Oxide Surface Conductance

3.5 Radiation Effects

The effects of the radiation are considered to be displacement and ionizing. Chemical effects are not considered since there are very few mobile ions in the material which can exchange charge. Two typical species which are associated with chemical effects are N^+ and O_2 to form NO^+. Surface effects were considered to be negligible since a non-selective extrinsic base diffusion is performed to increase the base surface concentration and hence reduce base inversion. The two major effects, displacement and ionization are considered in the following text. The approach is to reduce all displacement damage effects to an effective neutron dosage and all ionizing effects to an effective gamma dosage.

The energies given are assumed to be monoenergetic levels resulting from a particle average over an energy interval. The spectrum is given in Table 3.5-1 as an aid in illustrating the relative energy levels of the different particles.

3.5.1 Ionizing Effect

In order to determine the ionizing effect of the electron and proton dosages, it was necessary to determine the stopping power of the particles in silicon. The stopping power or energy loss per unit path length $(^{-de}/_{\rho dx})$ was assumed to be the result of inelastic collisions. The

TABLE 3.5-1 Radiation Levels

Radiation Type	Energy Level (mev)	Flux Rate (particles/cm^2/sec)	Integrated Flux (particles/cm^2)
Electrons	1.0	1.0×10^{10}	2.0×10^{13}
	3.0	1.5×10^{10}	3.0×10^{13}
	10.0	1.5×10^{9}	3.0×10^{12}
	25.0	3.0×10^{8}	6.0×10^{11}
Protons	10.0	1.5×10^{9}	3.0×10^{12}
	30.0	5.0×10^{8}	1.0×10^{12}
	100.0	1.5×10^{7}	3.0×10^{10}
Neutrons	Energy Spectrum		
	Energy Interval (mev) / Percent	Flux Rate (neutrons/cm^2/sec)	Integrated Flux (neutrons/cm^2)
	<0.5 — 10.5	2.8×10^{3}	1.0×10^{12}
	0.5-1.5 — 25.4		
	1.5-2.5 — 35.3		
	>2.5 — 2.4		
	73.5 — 4.4		
Gamma	Energy Spectrum		
	Energy Interval (mev) / Percent	Dose Rate (rads/hr)	Integrated Dose (rads)
	<0.2 — 0.0	1.0×10^{-1}	1.0×10^{4}
	0.2-0.5 — 7.3		
	0.5-1.0 — 24.1		
	1.0-2.0 — 16.7		
	2.0-3.0 — 50.		
	>3.0 — 1.9		

stopping power for silicon was determined by using the experimental data for aluminum and making the proper conversion for the atomic number and atomic mass of silicon. Points on the stopping power curves for silicon as determined by the above method were checked against data for 10 and 100 MEV protons given in reference I and were found to be in good agreement. The stopping power curve for electrons was determined from points given in this reference also. These points were checked against calculated points. The equations used to check the curves are essentially the energy loss equations as derived from Rutherford scattering as given in reference 2 or reference 3. The resulting stopping power of electrons and protons in silicon is given in Figure 3.5-1.

The energy deposited per sec per gram of silicon is given by,

$$\frac{dE}{\rho dx} N \quad \text{in} \quad \frac{\text{MEV}}{\text{gm - sec.}}$$

where $\frac{dE}{\rho dx}$ = stopping power from Figure 3.5-1

N = flux rate

Using the fact that 1 Rad (Si) = [illegible] ergs/gm, we can find the number of Rads resulting from a given energy level of electrons or protons. This is,

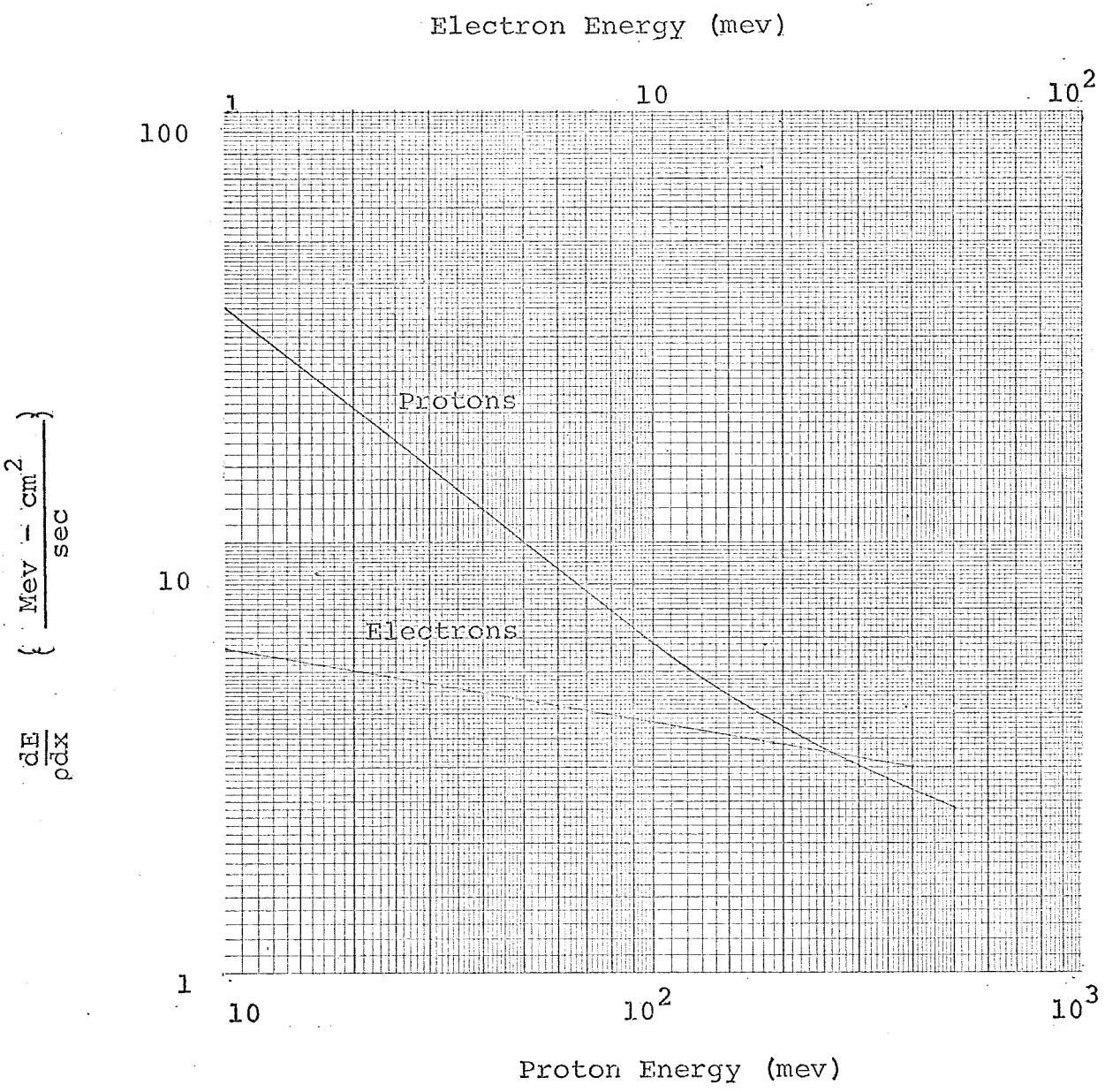


Figure 3.5-1 Average Energy Loss Per Unit Path Length for Electrons and Protons

$$\left(\frac{\text{Rads}}{\text{sec}}\right)_{\text{part.}} = \left(\frac{\text{NdE}}{\rho dx}\right)_{\text{part.}} \frac{\text{MEV}}{\text{gm-sec}} \left(1.6\times10^{-8} \frac{\text{Rads-gm}}{\text{MEV}}\right)$$

The effective dosage of a fission spectrum of neutrons is made using,

$$1 \ ^{n}/_{cm^2}\text{-sec} = 4.2 \times 10^{-11} \ \text{Rads}/_{\text{sec}}.$$

The resulting dose rate is then,

$$\dot{\gamma} \text{ Total} = \sum_i \dot{\gamma}_i$$

Where i sums over the particles and gamma rays. The resulting effective dose rate for all particles and gamma rays is,

$$\dot{\gamma} \text{ Total} = 3.2 \times 10^{3} \ \text{Rads}/_{\text{sec}}.$$

Using the collector-substrate junction as worst-case, a maximum photo current of 200×10^{-9} amps is determined.

3.5.2 Displacement Damage

The degradation effect on beta was determined for the protons from data found experimentally on solar cells operated in the Van Allen belt. This information is given in reference 4, 5 and 6. The damage constant for protons and electrons is given in Figure 3.5-2. A damage constant K_τ of 1.25×10^{-6} cm^2/n-sec. was used for neutron damage. The degradation due to electrons is found to be very small as compared to that for

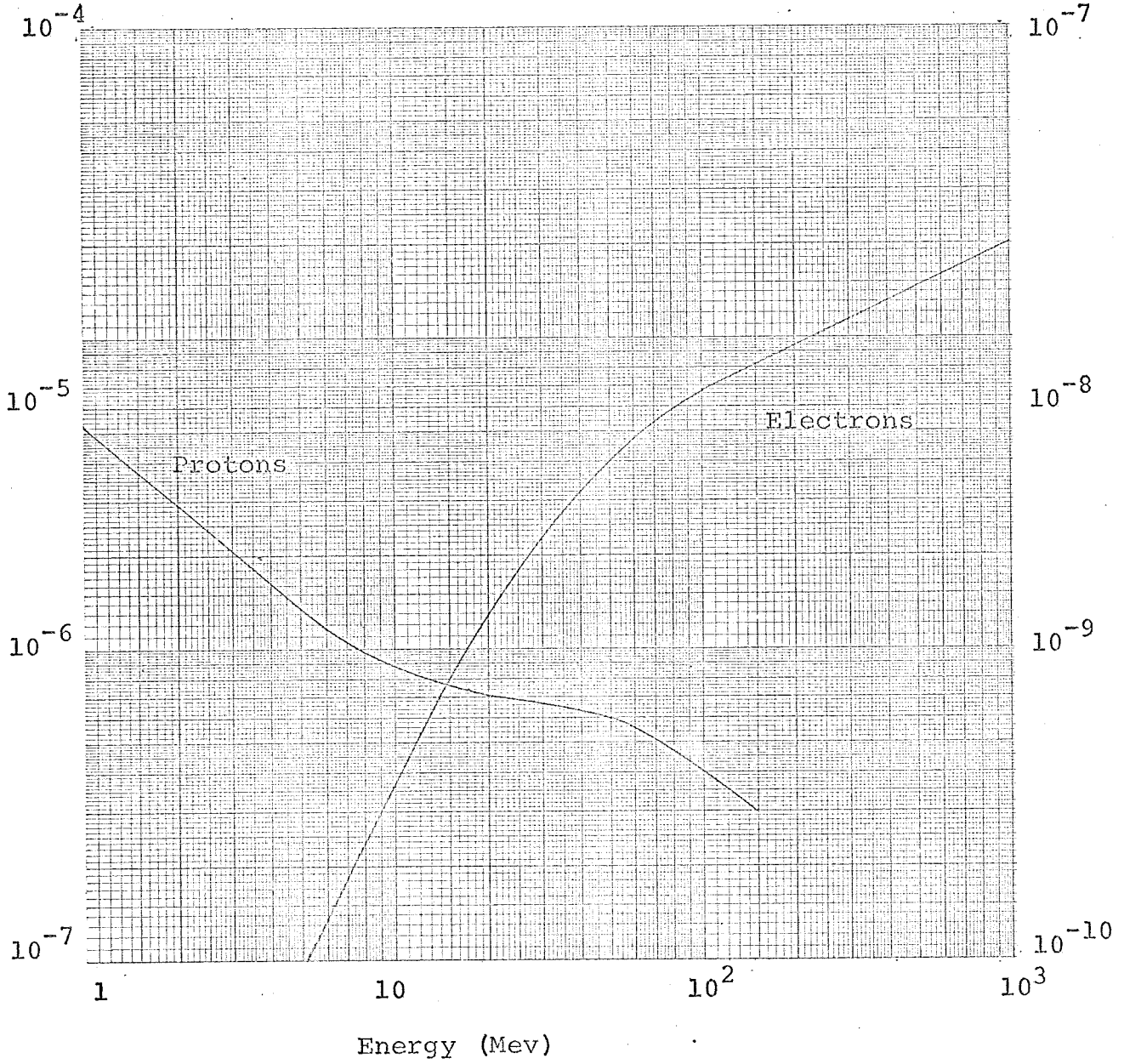


Figure 3.5-2 Diffusion Length Damage Constants For Protons and Electrons

protons and neutrons. The resulting $K_\tau\phi$ terms are shown below for the respective particles.

Electrons	ϕ (Particles/cm^2)	$K_\tau\phi$ (sec^{-1})
1	2×10^{13}	0.050×10^6
3	3×10^{13}	0.075×10^6
10	3×10^{12}	0.026×10^6
25	6×10^{11}	0.025×10
		0.176×10^6
Protons		
10	3×10^{12}	67.5×10^6
30	1×10^{12}	16.2×10^6
100	3×10^{10}	0.3×10^6
		84.1×10^6
Neutrons		
-	1×10^{12}	1.25×10^6
		1.25×10^6
Total		85.52×10^6

Using the equation for beta degradation

$$\frac{1}{\beta\phi} = \frac{1}{\beta o} + \frac{W^2}{2\ Deb} K_\tau\phi$$

$$\Delta\left(\frac{1}{\beta}\right) = \frac{W^2}{2\ Deb} K_\tau\phi = 2 \times 10^{-10} K_\tau\phi$$

With a 1 micron base width and Deb = 25 cm^2/sec, the change in beta is found.

$$\Delta\left(\frac{1}{\beta}\right) = .02$$

$$\beta_o = 40$$

$$\beta\phi = 22.5$$

3.5.3 Shielding Considerations

After consideration of aluminum as a shield and considering the reduced fluence of the 10 MEV protons, the new levels were calculated. Since the range of the 30 and 100 MEV protons is so large in aluminum, 0.438 and 3.70 cm respectively, only the shielding of the 10 MEV protons was considered. It was assumed that the fluence of the 30 MEV and 100 MEV protons were not reduced. An aluminum thickness of three path lengths (0.063cm) was used with a 10 MEV proton fluence reduction of 1/8. The new levels of radiation with shielding are given below

Electrons	ϕ (Particles/cm^2)	$K_T\phi$ (sec^{-1})
1 MEV	1×10^{13}	0.050×10^6
3	3×10^{13}	0.075×10^6
10	3×10^{12}	0.026×10^6
25	6×10^{11}	0.025×10^6
		0.176×10^6
Protons		
10 MEV	3.75×10^{11}	8.45×10^6
30	1×10^{12}	16.20×10^6
100	3×10^{10}	0.30×10^6
		24.95×10^6

Neutrons

-	1×10^{12}	1.25×10^{6}
		1.25×10^{6}
Total		26.25×10^{6}

$$\Delta \left(\frac{1}{\beta}\right) = .006$$

$$\beta_o = 40$$

$$\beta\phi \simeq 33$$

3.5.4 Summary

In summary, the investigation indicates that for the largest generation volumn, $I_{pp} \simeq 200$ nano-amp, and consequently not a serious problem. The beta degradation for the radiation levels given result in post-radiation beta of greater than 20 with no shielding. If the shielding is considered, the post-radiation beta is greater than 30. These results are quoted for a pre-radiation beta of 40 which is considered acceptable for the process method being used.

3.6 Two Layer Metallization

Two layer metallization development was well in an advanced stage prior to receipt of the CMMA contract. When the contract was received, development status and results were included as part of the CMMA program reporting activity.

3.6.1 Metallization Design

The processes for interconnecting Si devices with thin film aluminum metallization have been developed such that the electrical quality and reliability of such interconnections is commonly quite high at most facilities. As part of Phase I, the reliability of aluminum interconnect was re-examined in light of a projected 10 year mission. It has been known for some time that aluminum metallization subjected to current/heat fails in a fairly predictable manner due to electromigration. This failure mode is generally very long term, but was considered worthy of consideration for Phase I. Two of the latest technical reviews on electromigration are: (1) "Procedural Guidelines for Reliability Assessment of Large-Scale Integrated Circuits", RADC-TR-69-220, August 1969. (2) "A Brief Review of the State of the Art and Some Recent Results on Electromigration in Integrated Circuit Aluminum Metallization", S. Spitzer and S. Schwartz, J. Electrochem. Soc., 116, 1368, October 1969.

After reviewing several sources, the following conclusions

were reached:

A) No satisfactory theory has been postulated to explain electromigration, but several empirical descriptions have been given. Most results can be described in the form:

$$MTBF = \frac{A\ e^{(\emptyset/kT)}}{J^n}$$

where

MTBF = Mean Time Before Failure

A = Constant for a given film

$\emptyset$ = Effective activation energy

k = Boltzmann's constant

T = Absolute Temperature

n = Constant between 2 and 3

J = Current density (current per unit cross-sectional area)

B) Due to the extreme slowness of the phenomenon at normal stress levels all investigations have been at high stress levels. The results of different investigators do not agree as to the values of the constants relating MTBF, J, and T in the relation above.

C) It is found, however, that the "exact" values of the constants become relatively unimportant as the data is extrapolated from high stress levels to normal stress levels. For temperatures less than about $100^{\circ}C$ and current densities less than about 10^5 amps/cm^2, MTBF is extrapolated to be greater than 10^5 hours (10 years) regardless of disagreements between reported results at high stresses.

From the above, it is obvious that to obviate the effect of electromigration, the current density and/or operating temperature must not be allowed in a high stress condition. Information from JPL indicates that temperature during the mission will be well below 100°C. The current density level is subjected to design control. With the desired low level density in mind, proposed CMMA circuit designs call for:

A) 5.8×10^4 Amp/cm^2 maximum in the top level aluminum buss leading to either V_{cc} or Ground Bonding Pad. (35mA/2 mils x 50μ")

B) 1.5×10^4 Amp/cm^2 maximum in the bottom level aluminum buss lines. (6mA/2 mil x 35μ")

C) 4.1×10^4 Amp/cm^2 maximum in the smallest aluminum leads to Silicon contact apertures. (2.5mA/½ mil x 35μ")

The effectiveness of the proposed design will naturally be subject to reliability testing in later phases.

3.6.2 Deposited Dielectric Design

The multi-level requirement of the CMMA necessitates fabrication of two layers of aluminum separated by a dielectric.

During early development work it had been found that SiO_2 had the most desirable dielectric characteristics for satisfying this electrical isolation function. These characteristics are:

A) Low Dielectric Constant - about 4.0

B) High Dielectric Strength - 2 to 6 x 10^6 V/cm Break-

down Field

C) High Resistivity - 10^{16} - 10^{18} ohm - cm

D) High Stability - Inert to most thermo-chemical degradation modes.

Additionally, thin film Al-SiO_2 -Al geometries have been reported to be simple to fabricate and to be free of thin film effects which occur in some other dielectrics.

The two main techniques for depositing SiO_2 films - chemical vapor deposition and radio frequency sputtering - had been reported to produce films of similar characteristics. To obtain first hand comparison of the two techniques, a comparison of sputtered oxide versus silane oxide versus combination sputtered and silane oxide was performed on Al-SiO_2-Al test geometries fabricated in-house. Though the initial performance of all samples were comparable, the silane oxide samples had superior yield characteristics to post-fabrication high temperature stress.

The process design specification necessary to fulfill CMMA Phase I requirements was therefore designed around the chemical vapor deposition technique. Since our projections of JPL Phase II requirements were coincident with some of our in-house multi-level plans, some separately funded effort which would be applicable to Phase II is already in progress.

3.6.3 Processing

In order to test our capability in the multi-level metallization area, a test mask series was generated. These masks allow the fabrication of multi-level structures containing 200, 100, 50, 40, 30, 25, and 10 crossover points of 1 square mil each. Five runs were processed using the test masks to demonstrate that we could successfully fabricate multi-level structures.

The quality of these multi-level structures was excellent. Most slices had visually perfect oxide. On the few slices that did have oxide damage, electrical testing verified the poor quality of the oxide.

Runs 3, 4, and 5 were electrically tested (on slice) and found to be of excellent quality. Typically, less than 10% failure rates were observed for stress levels between 5 and 100 volts. (Failure criterion was leakage greater than 5μA).

However, the self-repairing tendency of failures in this structure made a conclusive Quality Analysis extremely difficult.

Three subsequent runs, 6, 7, and 8 were processed to provide test vehicles for a reliability study. The processing of these runs was considered an improvement over the processing for earlier runs. Film thicknesses for these runs conformed to circuit requirements. These runs

incorporated eleven process variations. Some visually good circuits from these runs have been packaged. Electrical testing, and the reliability study, will ultimately determine the quality of these structures and the processing steps used.

3.6.4 Testing

Electrical testing of multi-level structures can be broken down into two categories.

1) Characterization of good/bad structures
(maximum allowable leakage current criteria)
On-slice or in package.
6 volt/room temperature is considered non-destructive.

2) Temperature/Voltage Stressing

Testing in category II is covered in detail in the reliability report.

The following good/bad characterizations have been done:

A. 176 packaged units from run 4 were tested good/bad (criterion: 5μA of leakage) at 6 volts. The failure rate for these units was 81%. This was considered to be due to two factors:

a) processing steps were not considered to be near-optimum.

b) film thicknesses were considered to be deleterious to structure quality.

Considering these two points, the high rate of failures was not considered significant.

B. 1100 Packaged units from runs 6, 7, and 8 are currently being tested good/bad (criterion: 5μA leakage) at 6 volts. As previously mentioned, both the processing steps and the film thicknesses for these runs are considered improvements from earlier work. No yield data is currently available.

It should be noted that all units that tested good performed up to the capabilities of the bulk material. That is, good units demonstrated electrical breakdown at the dielectric breakdown strength of amorphous SiO_2 ($2\text{-}6 \times 10^6$ V/cm). No materials oriented problems have been observed.

Preliminary indications from experimental runs now in process are that we have made progress towards further improving our multi-level process.

3.7 Test Philsophy

Sufficient testing of the metallized Multigate Array must be performed to insure the functional and parametric integrity of the packaged array, with adequate performance margins such that continued operation may be assured in its operating environment, particularly the post radiation environment.

This section contains then a discussion of test methods which may be used to assure these characteristics. Methods discussed include programmable functional testing which can be used to test the packaged logic function at the voltage and temperature extremes required, probing individual gate cells, and wafer and die qualification through the use of test devices on the die.

3.7.1 Functional and Parametric Testing

Functional and parametric testing of the metallized array will be performed with the use of a programmable tester which will accept test programs to exercise all functions and thereby assure the integrity of the array. At package level, the array may be tested at both temperature and voltages extremes with this system.

A simplified block diagram of the tester to be built

as part of this contract is shown in Figure 3.7-1. The tester consists of input shift registers which will be loaded by a tape reader interface. Once the registers are loaded, the metallized array is exercised and its outputs compared with the correct output in the comparator block.

Such a tester will be highly flexible, since the designation of shift register outputs to either the inputs of the metallized array or to the comparator block is totally arbitrary. Therefore, the limitations on test capability is total pin count rather than a specific number of inputs and outputs. One tester then can be programmed to test any logic function built with the array. The use of a tape reader to load the input shift registers allows the direct use of a computer output which may be used to generate and/or verify the validity of a test program. Once a test program is loaded, the tester may be automatically or manually sequenced through the test program to test any number of units of a given type. It may be feasible to include in this tester the capability to test the transient characteristics of the metallized array even though the operation of the shift registers may be rather slow. The outputs of the shift register can be buffered with a high speed Flip-Flop. Application of a given set of test

inputs to the array and to the comparator can thus be simultaneously initiated. A variable delay strobe of the comparator block will then provide an indication of the minimum delay time of the unit under test.

3.7.2 Environmental Testing

Temperature testing is expected to be performed with the use of a calibrated thermoelectric probe placed in contact with the case of the unit under test. This has the advantages of eliminating the requirement for cabling into a temperature chamber with attendant problems. A case temperature controlled test is more repeatable than an ambient air temperature measurement since this depends on such variables as the amount of air flow and the length of time that power is applied to the unit.

The packaged unit may therefore be tested at both temperature and voltage extremes with variable loads placed on the outputs to ensure adequate fanout safety margins on the array output. This gives the capability of assuring operating safety margins by testing the unit at worst case conditions. For the problem of post radiation function, low voltage, low temperature testing can be employed.

Since the principle radiation effect is beta degradation as discussed in Section 3.5 and the minimum beta

requirement is the most stringent at low temperature, low voltage extremes, functional integrity under these conditions would ensure worst-case minimum current gain. With this minimum pre-radiation beta, knowledge of beta and resistor temperature coefficients, and the beta degradation factor, a post radiation minimum temperature and voltage operating point can be calculated. This approach may be as valuable as individual gate probe in assuring post radiation function. In addition, it is the least expensive in terms of additional hardware and software requirements, additional processing steps, handling, and die area.

3.7.3 Individual Gate Probe

An alternative method to ensure adequate operating safety margins is to implement a probe level test of the individual gates. With this approach room temperature, D.C., characteristics of fanout current, "O" input currents, and thresholds may be tested. Measurement of leakage currents at typical levels expected (less than 1 nA) is not feasible at probe since the presence of light on the die and of electromagnetic radiation from other equipment would totally mask measurements of such low magnitude.

The probe approach most likely to result in a reliability advantage is to probe at a point in the process beyond which the least processing remains, and which adds the

least additional steps in the process. The recommended approach is probe after the dielectric layer between metal layers has been applied and via's opened. This requires over-size via's to accomodate the probe tip. The minimum via size and spacing that may be used with the probe methods studied is 2 1/2 mil square via's with 6 mil spacing. To probe each input and output would more than double the die area. Alternatively, to probe one input plus the output requires an increase of 36%. The most preferable probe system studied is a fixed point probe system which utilizes a probe with a gold ball tip. The fixed point approach has the advantage that set up time and probe alignment accuracy are improved. Since the probe pattern is fixed and may be accurately matched to the die pattern, there is reduced danger of probes not striking the pads. The gold tip will be rather soft and the contact will not be a sharp point, thus the danger of fracturing the oxide under the probe pad is reduced. Factors that have yet to be determined and which can only be determined by actual testing of the system, are: 1) Difficulty in visually aligning the probe card on a die such that the probes strike the pads without touching the oxide around the pad; 2) If the probe does strike the oxide, what will be the extent of the cracking; that is, can it be localized to the area at the edge of the pad, or will cracks propagate into areas which will have second level

metallization over them.

The parameters that can be verified directly at probe and not after metallization and packaging are fanout currents and input thresholds of internal gates. Input pullup resistor values may also be measured at probe.

Resistor values may be inferred at package level from a measure of total power dissipation. Input thresholds are most strongly dependent on forward diode voltages and resistor ratios, which are not primarily affected by radiation levels. This leaves fanout current and therefore a measure of initial beta as the most significant parameter that can be verified with an individual gate probe.

The disadvantages that must be considered in making a decision to implement individual gate probe are the costs in terms of die area, software and hardware necessary to implement the probe, accounting problems in maintaining identity of units tested, and increased power dissipation. The maximum value for a given increase in die area can be gained by probing one input and the output of each gate. Cell energizing would be accomplished on a row by row basis to minimize the number of probe pads for this purpose. This would enable gate testing to be accomplished on this same row by row basis.

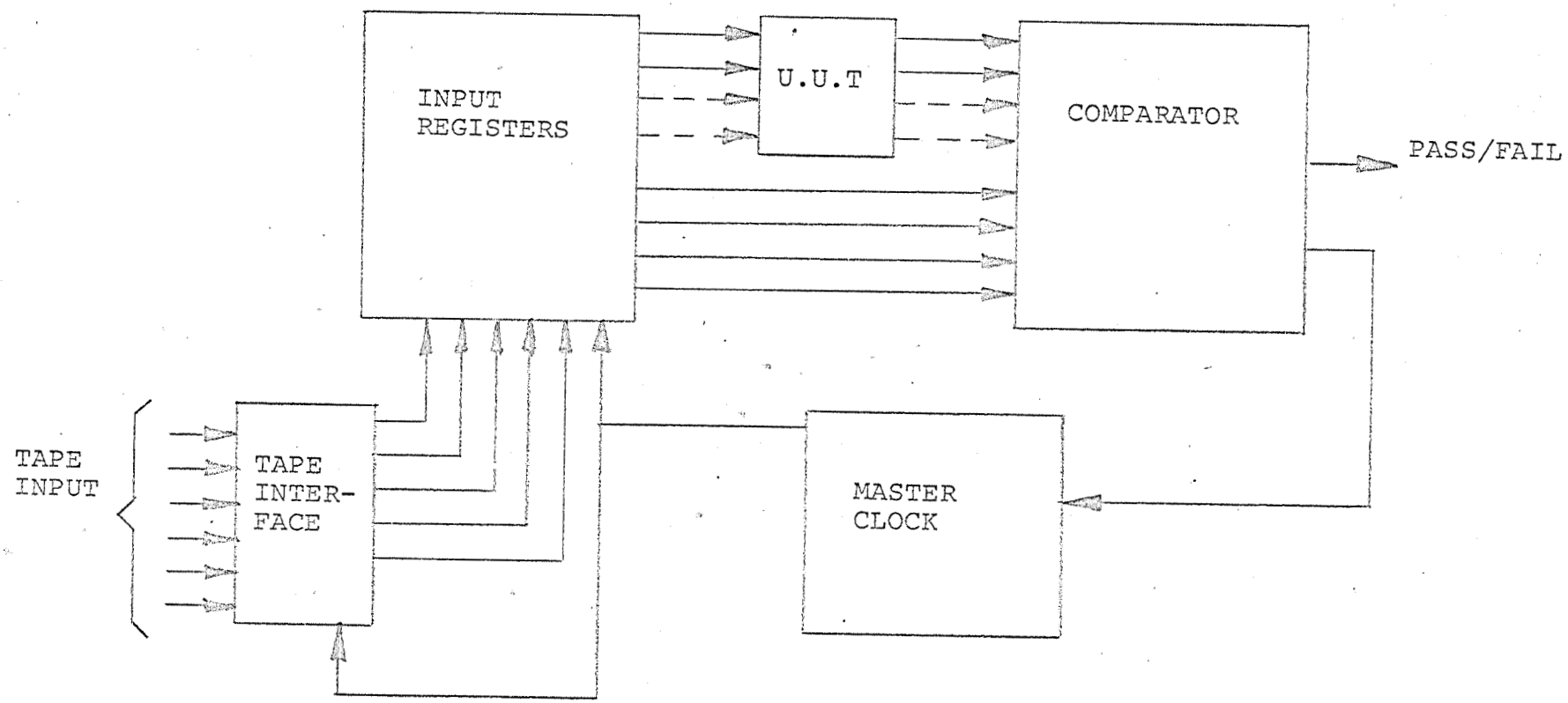
Increase in die area for this approach is 36%. The cell energizing scheme would increase total power of the metallized array by a maximum of 10%.

3.7.4 Special Test Structures

Included in the die organization discussed in section 3.2 is provision for special test cells. In addition, some positions on each wafer may be committed to test structures by varying one or both levels of metallization from the circuit pattern.

The test cells on each die may be committed to gates or individual devices. These cells may then be used to qualify the die at functional probe level or may be bonded out in the package for more exhaustive testing. Locating one of these cells in each quadrant of the die as shown in figure 3.2-1 will give an indication of the parameter uniformity across the complete die.

The wafer test positions will be used for test structures to qualify each wafer through more thorough testing than is feasible at the die test pattern level.



MULTIGATE ARRAY PROGRAMMABLE TESTER

FIGURE 3.7-1

APPENDIX I

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