IV. Development and Implementation

A. DSIF Development

1. Antenna-Mechanical Subsystem Field Instrumentation–Modular Concept, *J. A. Carpenter*

a. Introduction. During erection of the antenna-mechanical subsystem, instrumentation (including strain gauges, accelerometers, fluid and gas-pressure-sensing devices, recording anemometers, force gauges, thermocouples, and extensometers) is needed for installation, alignment, and performance evaluation.

During the early days of antenna installation, due to a lack of field housing facilities, instrumentation trailers were designed and built which housed not only the recording instrumentation needed in association with the above listed sensing devices, but also work and storage space. The subsequent history of utilization showed that the trailers spent from 40 to 75% of their life in transit and involved excessive handling, maintenance, and customs processing.

b. Design criteria. A re-evaluation of the utilization of this type of field instrumentation developed the following criteria:

(1) An instrumentation trailer embodying storage and work space was not needed, due to the on-location availability of such facilities.

(2) The instrumentation assemblies configuration should be as light and compact as reasonable and should lend itself to any mode of transport—air, sea, or land.

(3) The instrumentation assembly should be configured in discrete modules to support specific needs and avoid shipment of equipment not required for a specific task.

(4) The modular concept should allow for easy expansion of the assembly to the complexity required.

(5) The design of the instrumentation assembly should be simple enough to be able to be used at any skill level and to require minimum maintenance.

c. Final configuration. A modular instrumentation assembly concept was developed which affords the following:

(1) The basic equipment is resolved into two subunits: (a) an analog recording configuration with a strip

recorder for quick field looks and analyses; and (b) a parallelable analog tape recording unit (Fig. 1) for storing data from the strip recorder for later more complex analysis or digital processing.

(2) The two instrumentation subunits are mounted permanently in shock-proof shipping containers.

(3) These containers are weatherproof for shipping and field housing.

(4) The shipping and housing containers are of dimensions acceptable for commercial air shipment, when necessary.

2. Damage Prevention System for 85-ft Antenna,

J. Carlucci

a. Introduction. As a result of operational experience and an analysis of the safety needs of the DSIF antennas, a system has been designed which will allow the servo operator to monitor the antenna and surrounding area, and to control or prevent vehicles, equipment, and personnel intrusion. Due to the layout of the servo console, windows, hydromechanics building, cable trays and associated antenna hardware, it is presently impossible for the servo operator to perform control and monitoring functions continuously.

b. Problem. The general problem was reduced to two categories:

(1) Development of a barrier-alarm system that would not only prevent movement of hardware or equipment on and off the antenna pad without the servo operator's knowledge, but would have some reasonable form of interaction with the antennas drive system operation, and an alarm arrangement.

(2) Development of a surveillance system that would give an acceptable picture both day and night, for monitoring the antenna and surrounding area.

c. Solution.

Barrier-alarm system. Figure 2 shows a conceptual layout of the proposed barrier and safety alarm system (and the surveillance system) at DSS 11. This concept will be the basic one for all DSS alarm systems.

This system consists of a sectionalized chain link fence around the circumference of the antenna at a 260-ft diameter, with two 20-ft gates with locks and two 3-ft gates for personnel. An integrity cable runs around the top of the fence. The fence and integrity cable are made up in 10-ft sections and are removable, if required, by unbolting. The integrity cable is connected to the safety alarm arrangement. The purpose of the integrity cable is to provide the servo operator with an alarm indication when the barrier is broken or all 20-ft gates are not closed. The sectionalized chain link barrier acts as a personnel-control element.

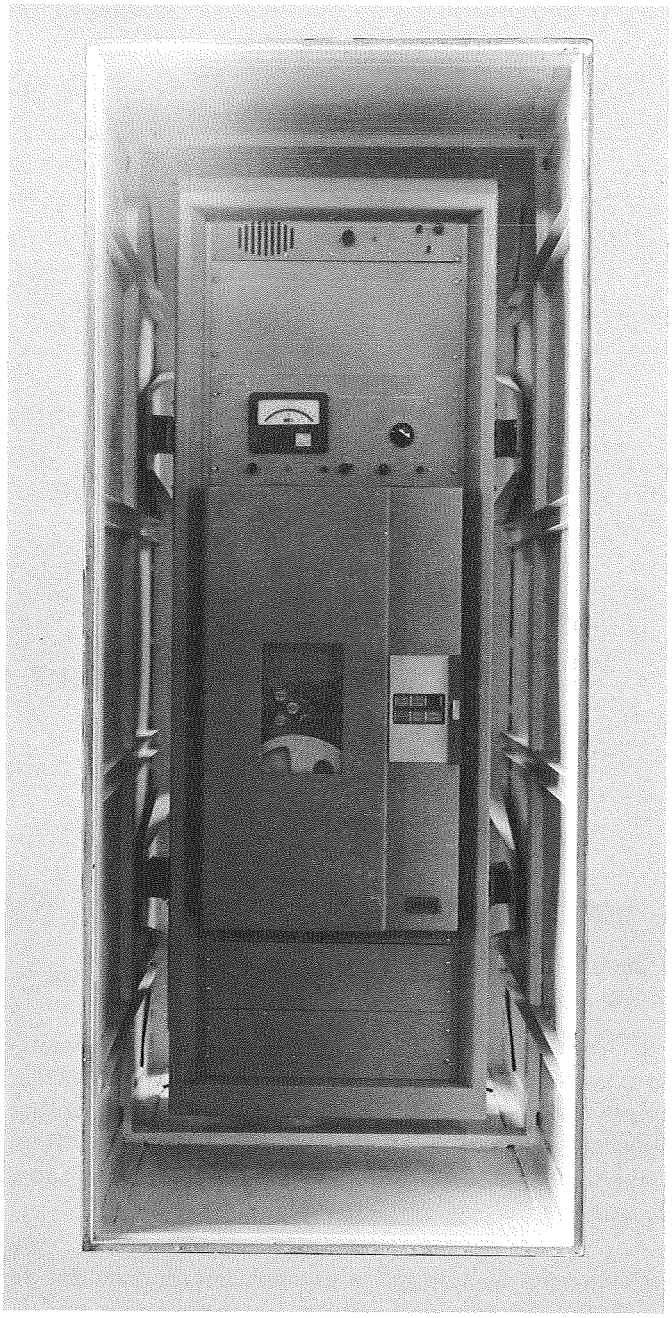


Fig. 1. Magnetic tape recording subunit in shipping container

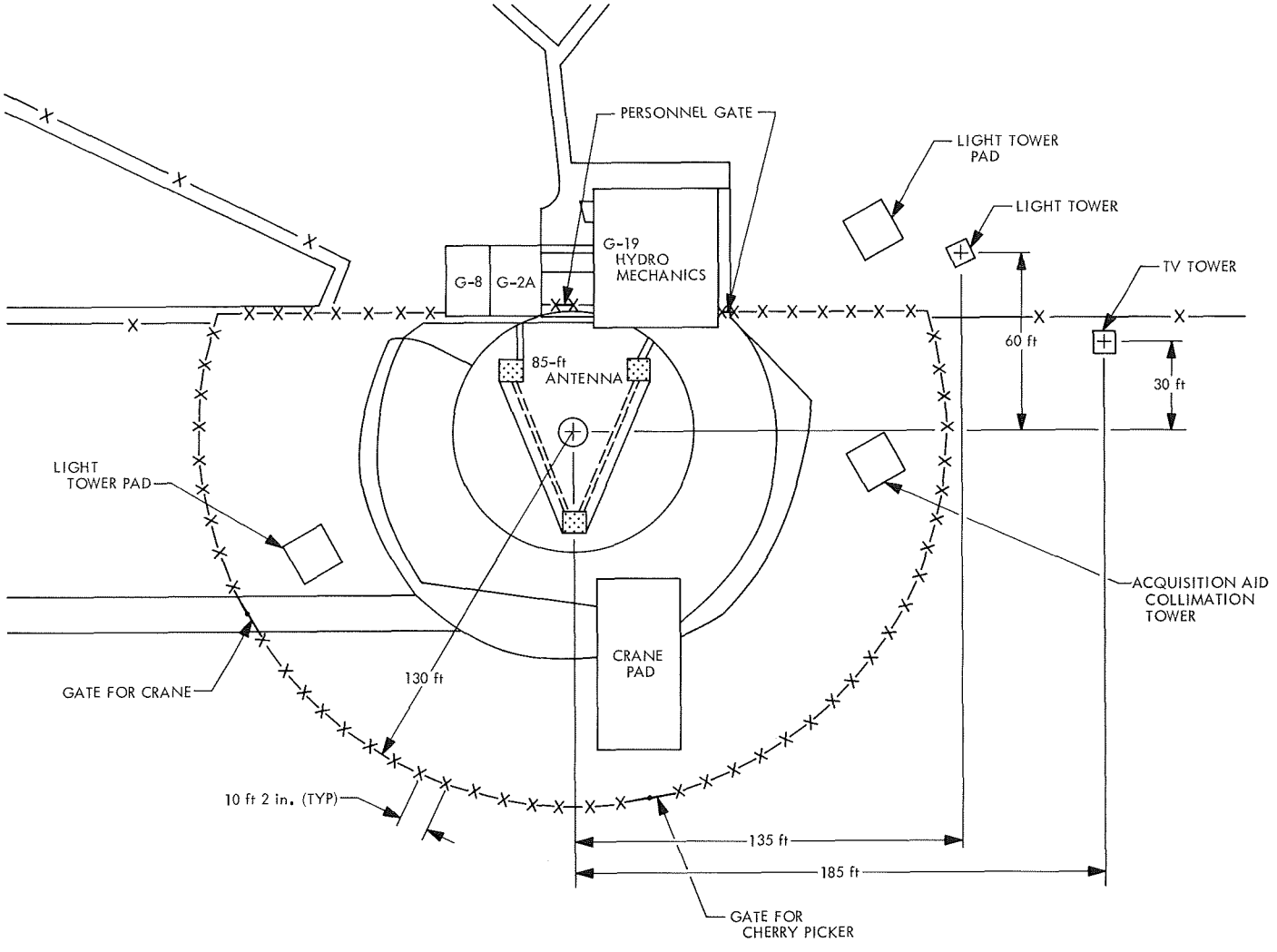


Fig. 2. Proposed barrier and safety alarm system

The safety alarm arrangement is a visual configuration which has a light bank reading "Hardware on Pad" when gates or fence sections are opened. In order to open the access gates a key must be removed from the servo console, which subsequently shuts down the servo. The shift supervisor also has a key which allows access to the antenna pad, on an emergency basis without disabling the servo, obtainable only with his approval.

Included in this system is a time delay which requires that the access key be in the switch and the TV system be operational for 5 min prior to servo power coming on. This is to make sure the servo operator surveys the antenna and area before operating the drive system.

Surveillance system. The resolved surveillance system is a TV system manufactured by Cohu Electronics, Inc., operating at 525 lines horizontal resolution with a 10,000/1 effective range for intensity variation. This range will produce a usable picture with light levels as low as 0.1 ft-cd on the face of the vidicon tube. The camera has a 10:1 zoom lens, mounted in an all-weather housing that is hermetically sealed, and all circuits are solid state.

Measurements made at DSS 11 indicated that existing area lighting was not sufficient to produce an acceptable picture at night. Therefore, the following requirements were adopted: the general scene area lighting, as measured at the TV camera, should be at least 0.1 ft-cd (preferably 1.0 ft-cd); the total distance from light source to antenna should be 140 ft and from antenna to camera 130 ft; for an emperically resolved actual reflection coefficient of about 0.20, there should be at least 1500-W

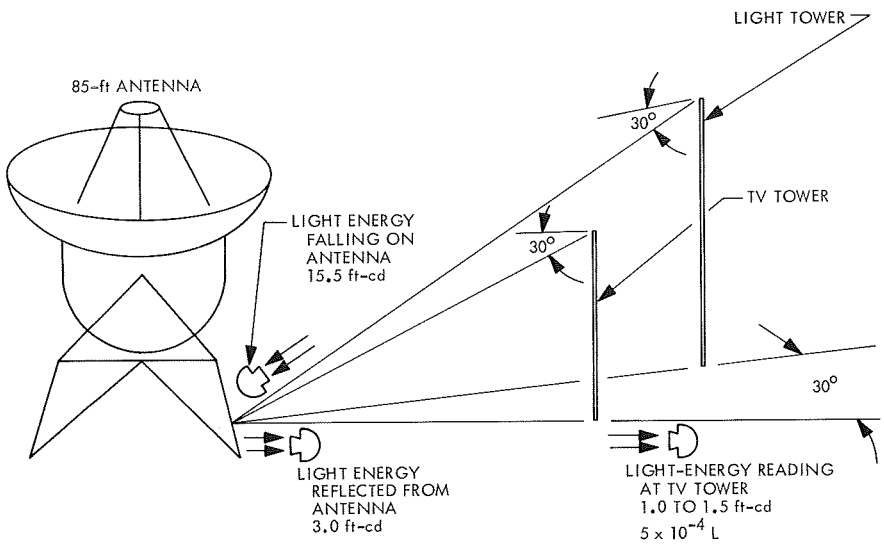


Fig. 3. Field test of surveillance system

lamps in banks of twelve, located on one of the present emergency light towers and directed at the center of the antenna with a maximum deviation from the normal of 30 deg or less, and having an initial rating of 33,000 lumens each.

Field test (Fig. 3) light readings at DSS 11 made at the base of the antenna, utilizing the θ and ϕ values of 30 deg each, confirmed the use of the 1500-W lamps. The results were:

Actual	Calculated
1 to 1.5 ft-cd	1.09 ft-cd
5×10^{-4} ft-L	5.55×10^{-4} ft-L

The number of lumens per unit area squared

$$E = \frac{I}{r^2} \cos\theta \cos\phi \text{ ft-cd}$$

where

I = light intensity, cd

r^2 = distance from light source, ft

θ = angle of incidence (zenith plane) to camera relative to reflecting surface

ϕ = angle of incidence (vertical plane) to camera relative to reflecting surface

3. ×3 Frequency Multiplier and Phase Modulator for Block IIIC S-Band Receiver–Exciter, C. E. Johns

a. Introduction. A new type of exciter phase modulator was developed to provide improved performance and the capability of setting modulation indices more precisely. The phase modulator presently used in the Block III C S-band receiver/exciter subsystem has a specified modulation linearity of ±5% over the range of indices from 0 to 2.4 rad at S-band. System measurements confirm that this is close to the limit of the capability of the present modulator design.

The present modulator design utilizes voltage-variable capacitors within a low-Q resonant circuit to achieve phase modulation. Due to the inherent nonlinear characteristic of capacitance variation versus applied voltage, voltage-variable capacitors are not suitable in a design requiring better than 5% linearity over large modulation indices. The design performance requirement of the new modulator is that the linearity be maintained within 1% for indices up to 2.4 rad at S-band.

b. Modulator design (ideal). A block diagram of the phase modulator module is shown in Fig. 4. The module being developed also contains a ×3 frequency multiplier ahead of the modulator. The 22-MHz input signal is amplified and amplitude-limited by amplifiers A1 and A2 and coupled to a wideband diode ×3 frequency multiplier. The multiplier output is filtered by a commercial filter centered at 66 MHz. The 66 MHz is then amplified (A3 and A4) and coupled to a 90-deg hybrid which provides two output ports, one having an in-phase signal

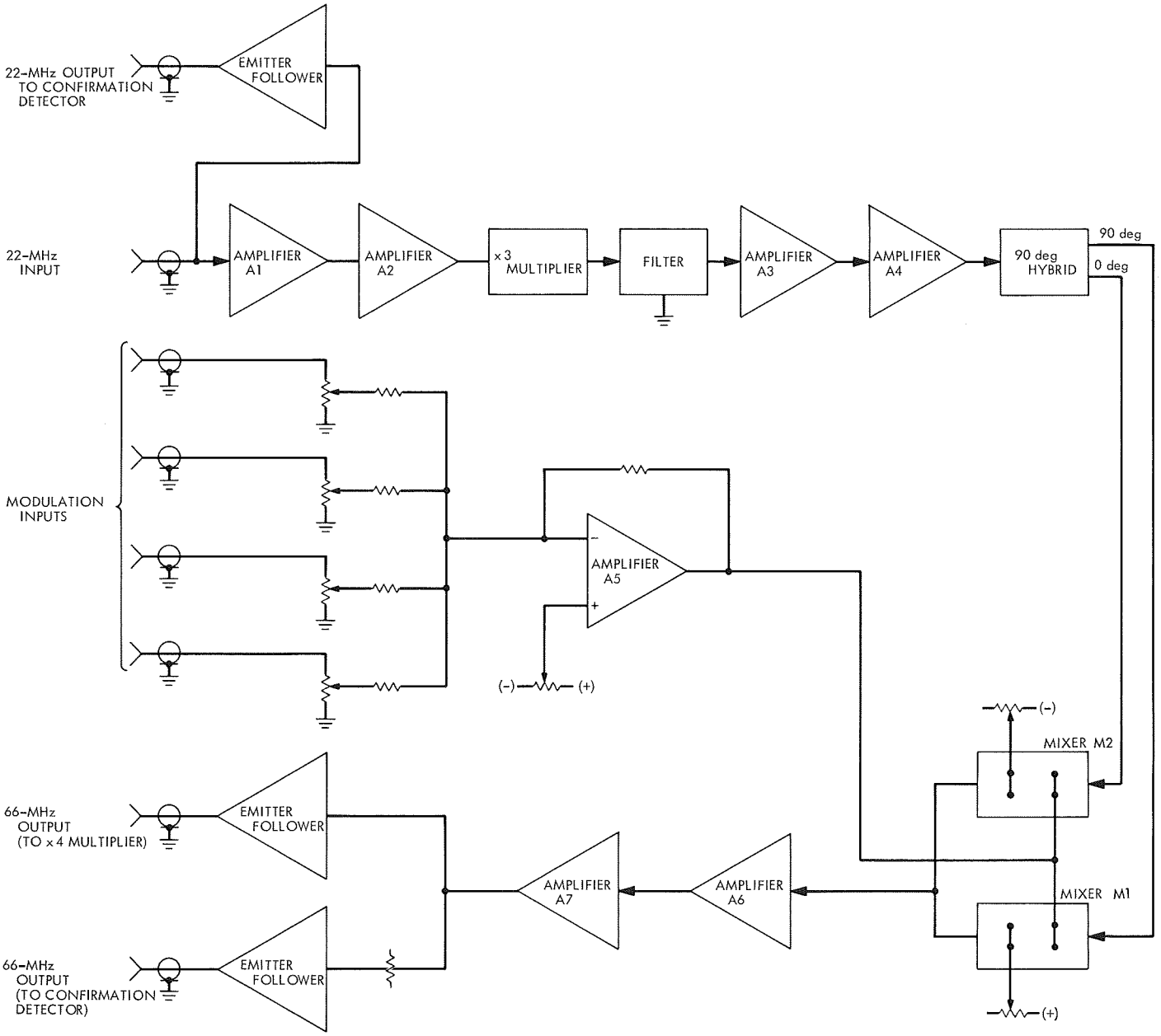


Fig. 4. × 3 frequency multiplier and phase modulator

and the second a quadrature signal. Each output port is then coupled to a commercial balanced mixer (M1 and M2) which is used as a voltage-variable attenuator. The control voltage on these mixers is the difference between the bias voltage and the voltage of the input modulation signal from the broadband video driver amplifier A5. Since the bias voltage on mixer M1 is positive and on mixer M2 is negative, the modulation signal will create control voltages that cause the attenuation of one mixer to increase while the attenuation of the other mixer decreases. These amplitude-modulated signals are then combined to produce a phase-modulated signal (discussed in more detail later). The combined carriers are subsequently amplified (A6 and A7) and applied to two isolated outputs through emitter followers.

The process of generating a phase-modulated carrier from amplitude modulation is not a new concept, but it was considered because of its capability of linear modulation over a large range of indices. The modulation process is best described in Fig. 5. Without the presence of modulation (assuming equal RF levels from each modulator, M1 and M2) the carrier vectors add as shown. When a positive modulating voltage is applied, the RF output amplitude of M1 increases linearly by the factor m and the output of M2 decreases linearly by m; a resultant carrier phase displacement (ϕ) occurs. Conversely, a negative modulation voltage results in a negative phase ($-\phi$) deviation. Figure 5 illustrates, then, an ideal situation where the unmodulated outputs of M1 and M2 are identical, and their output levels vary linearly with modulation voltage.

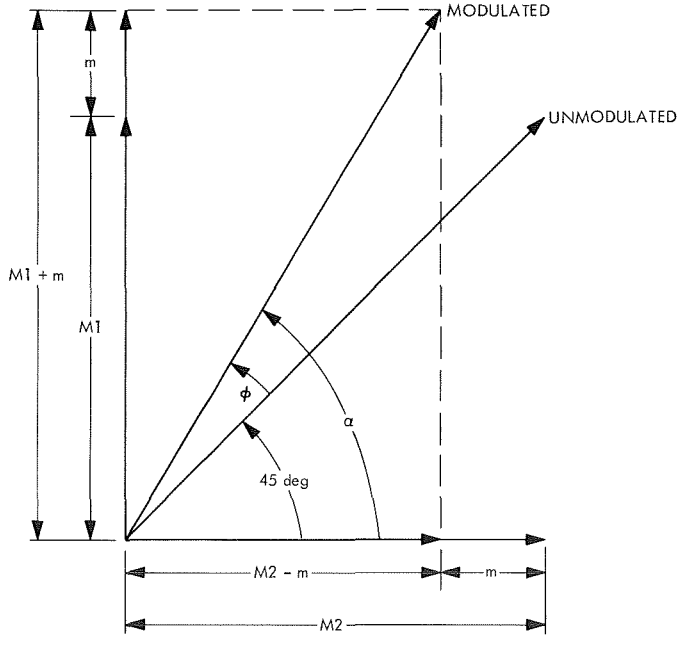


Fig. 5. Carrier vectors

Assuming the ideal case and that M1 and M2 are normalized to a value of 1, then the maximum linear ($\pm 1\%$) range of modulation can be determined from Fig. 5, as follows:

$$\alpha = \tan^{-1}\frac{1+m}{1-m} \tag{1}$$

and the phase deviation is

$$\phi = \alpha - 45\,\text{deg} = \tan^{-1}\frac{1+m}{1-m} - 45\,\text{deg} \tag{2}$$

To obtain the modulation sensitivity for very low indices

$$S_0 = \left.\frac{d\phi}{dm}\right|_{m=0} = \left.\frac{d}{dm}\left[\tan^{-1}\frac{1+m}{1-m} - 45\,\text{deg}\right]\right|_{m=0}$$

$$= \left.\frac{1}{1+m^2}\right|_{m=0}$$

$$S_0 = 1\ \text{rad/modulation unit (peak)} \tag{3}$$

Since the specified maximum modulation nonlinearity is 1%, then the sensitivity at the extreme of this linear range is

$$S_1 = S_0 - \frac{S_0}{100} = 1 - 0.01 = 0.99\ \text{rad/modulation unit (max)} \tag{4}$$

From Eqs. (3) and (4)

$$m_{\max} = \left(\frac{1-S_1}{S_1}\right)^{1/2} = \left(\frac{1}{99}\right)^{1/2} = 0.10053\ (\text{max}) \tag{5}$$

From Eq. (2)

$$\phi_{\max} = \tan^{-1}\frac{1+m_{\max}}{1-m_{\max}} - 45\,\text{deg}$$

$$= \tan^{-1}\frac{1+0.100503}{1-0.100503} - 45\,\text{deg} = 5.7399\,\text{deg (peak)} \tag{6}$$

For an ideal modulator, linearity within 1% can be attained to a peak phase deviation of ± 5.74 deg.

In the S-band exciter subsystem a 5.74-deg phase deviation at the modulator output, due to subsequent frequency multiplication, corresponds to 32×5.74 or 183.7 deg at S-band. This is approximately 33% greater than is required for carrier suppression using a sine-wave modulation signal, and is more than twice that required with square waves.

The amplitude variation for the ideal case over the linear range of phase modulation index is less than 0.1 dB. However, any amplitude variation is removed by subsequent limiters in the multiplier chain.

c. Modulator design (actual). There are several factors that cause the actual design to deviate from the ideal case, such as:

(1) The modulator diodes may be biased at a point that does not provide linear level changes.

(2) RF delay changes occur in the modulator as a function of the modulation voltage.

(3) A pair of modulators may be unbalanced, causing unequal changes in level.

Consider first the bias of the modulators. Figure 6 shows a typical signal level versus modulation voltage for the amplitude modulator. Point A on the curve indicates the bias for linear modulation as described in the ideal case. B and C represent bias points that produce nonlinear amplitude variation with modulation voltage. Assume the modulators are biased at point B and that the modulation voltage increases the RF outputs of M1 and M2 by 1.1 but decreases them by only 0.9, causing a 10% amplitude linearity distortion. From Eq. (2)

$$\phi = \tan^{-1}\frac{1 + 1.1\,m}{1 - 0.9\,m} - 45 \text{ deg} \tag{7}$$

$$S_0 = \left.\frac{d\phi}{dm}\right|_{m=0} = \left.\frac{0.99009}{m^2 + 0.19802\,m + 0.99009}\right|_{m=0} = 1 \text{ rad/modulation unit} \tag{8}$$

$$S_1 = S_0 - \frac{S_0}{100} = 0.99 \text{ rad/modulation unit at 1\% nonlinearity} \tag{9}$$

Then from Eqs. (8) and (9)

$$m_{max} = 0.0417131 \text{ modulation units} \tag{10}$$

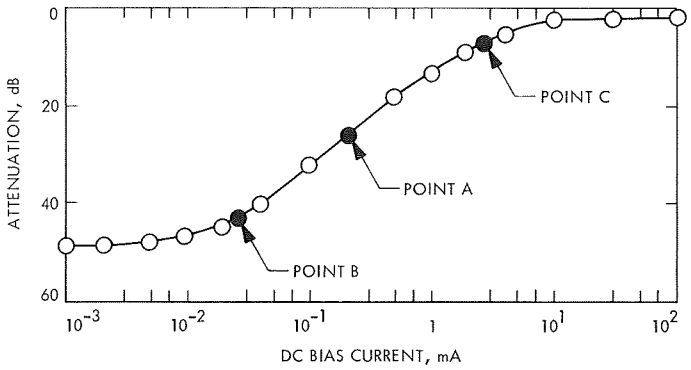


Fig. 6. Characteristics of amplitude modulator

and from Eqs. (7) and (10)

$$\phi_{max} = \tan^{-1}\frac{1 + 1.1\,m}{1 - 0.9\,m} - 45 \text{ deg} = 2.38131 \text{ deg} \tag{11}$$

Thus, biasing at point B on the curve shown in Fig. 6 greatly reduces the linear phase range.

If, on the other hand, the amplitude modulators are biased at point C of Fig. 6 where the modulation voltage increases the RF output by 0.9 but decreases them by 1.1, then

$$\phi = \tan^{-1}\frac{1 + 0.9\,m}{1 - 1.1\,m} - 45 \text{ deg} \tag{12}$$

$$S_0 = \left.\frac{d\phi}{dm}\right|_{m=0} = \left.\frac{0.990099}{m^2 - 0.19802\,m + 0.990099}\right|_{m=0} = 1 \text{ rad/modulation unit} \tag{13}$$

$$S_1 = S_0 - \frac{S_0}{100} = 0.99 \text{ rad/modulation unit} \tag{14}$$

at 1% nonlinearity. Then from Eqs. (13) and (14)

$$m_{max} = 0.198025 \text{ modulation units} \tag{15}$$

and from Eqs. (12) and (15)

$$\phi_{max} = \tan^{-1}\frac{1 + 0.9\,m}{1 - 1.1\,m} - 45 \text{ deg} = 11.4215 \text{ deg} \tag{16}$$

at the negative 1% distortion point.

The region between the zero modulation and the negative 1% point was investigated. It was found that the phase slope is not monotonic; however, at no point in this region does the nonlinearity exceed ±1%. It can be shown that the same $(-\phi)$ linearity is obtained when a negative modulation voltage is applied.

Selecting a nonlinear bias point C has increased the linear range over the ideal case. This is a result of compensating the nonlinear arctan function with the nonlinear characteristics of the amplitude modulation.

Another contributing factor to nonideal performance is the carrier phase delay change versus attenuation of each amplitude modulator, which constitutes approximately 15% of the total desired phase deviation. This phase shift is relatively linear over the operating amplitude range of the modulators of ±1 dB and does not contribute significantly to nonlinearity. The alignment procedure assures that both the phase delay characteristics and the differences between the characteristics of the modulators are compensated by selection of the proper bias.

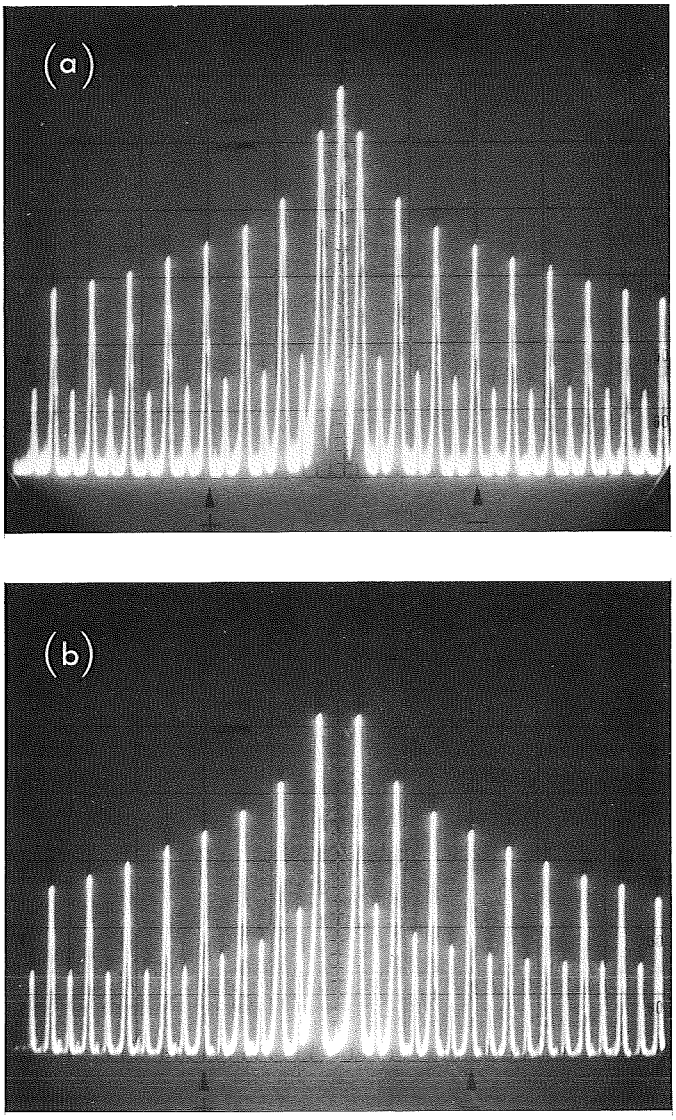


Fig. 7. S-band modulation spectra: (a) ~ 2 dB carrier suppression; (b) carrier suppressed

The photographs in Fig. 7 show S-band phase-modulation spectra (2110 MHz) using the new phase modulator. In Fig. 7a the carrier has been suppressed approximately 2 dB, and in Fig. 7b the carrier has been nulled. In both cases the modulation signal was a 100-KHz square wave with a rise and decay time of 10 ns. The existence of even-order harmonics is partly due to the rise time of the modulating signal. To obtain the photographs, the 66-MHz output from the modulator module was frequency-multiplied ×32 using standard Block III C S-band exciter subassemblies.

d. Conclusion. The use of amplitude modulation techniques to obtain a linear phase modulator has been demonstrated. Nonlinearities of less than 1% up to an index of 2.4 rad at S-band have been attained. The modulator itself has a bandwidth greater than ±10 MHz and can handle square-wave modulation signals up to 1 MHz. However, in the present Block III C exciter, the bandwidth is limited by the frequency multiplier chain following the modulator.

4. 400-kW Transmitter Controls, *R. L. Leu*

a. Introduction. The size and complexity of the 400-kW transmitter system demands a larger and more reliable control system. The new system uses solid-state discrete logic and monitor circuits. The new control system for the DSN 400-kW transmitter is under test at DSS 13 and is being static-tested in the laboratory. Preliminary testing of these circuits at DSS 13 proved them to be very satisfactory.

b. Control system. The control system is made up of a master control and four auxiliary controls as shown in Fig. 8. The system controls, monitors, and protects the klystron amplifier. (The motor-generator controls are part of the 1-MW motor-generator and are not discussed in this article.)

c. Local control console. The local control console is the master control of the system. All system interlock,

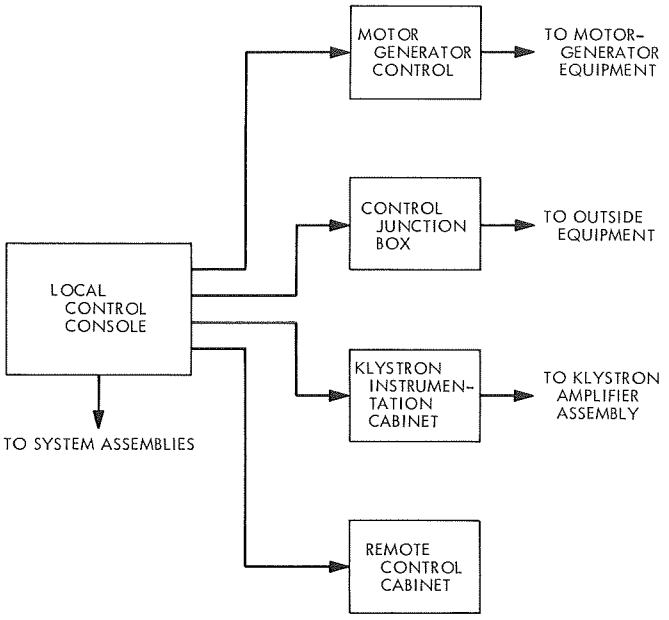


Fig. 8. 400-kW transmitter control system

monitor, and control functions are available on the terminal boards. This has been done to prepare for future computer control and monitor of the 400-kW transmitter. However, for complete computer control, additional functions will be required, and the termination bay is designed for the addition of more terminals.

To improve the system reliability and performance, solid-state logic has been designed for the interlock, control, and monitor functions. The relay interlock logic presently used in transmitter systems is being replaced by digital *and*-gate circuitry. The relay function used to illuminate fault and status lamps is being replaced by *lamp drivers*. The *on-off* control functions are being replaced by bistable circuitry. The logic units are designed to operate on an input signal between 15 and 30 Vdc. There are several additional advantages to using solid-state logic as opposed to relay logic. The size of the total logic chassis is about 1/10 the size of the existing relay assembly; power to energize the logic is 1/20 that required for relays; and the logic is more accessible for maintenance and trouble shooting.

Monitoring circuits to drive meters at remote locations have been designed, utilizing integrated differential amplifiers. These circuits are being used in the 450-kW transmitter at DSS 13 and have operated without failure or problems for the past 4 mo. The new design gives more reliable meter readings at the remote locations, decreased drift with temperature changes, and can be disconnected from the driving source without changing the local monitoring meter calibration.

d. Control junction box. This unit is located in the transformer/rectifier building north of the antenna. The control J-box is used as a control distribution and interlock status accumulation center for all outside equipment on the ground. The J-box contains a small logic chassis with summing logic, lamp driver, and bistable circuits. Interlock faults are summed into major fault categories and sent to the local control. The J-box has fault display lamps to indicate the precise fault of the local equipment. The lamp drivers are used for turning on and off the outside equipment on commands sent from the local control console.

e. Klystron instrumentation. The instrumentation cabinet will be located in the tri-cone with the klystron amplifier. This assembly is used for control and monitor of the 400-kW klystron amplifier. The control and interlock functions are: filament power, RF drive input, coolant flow, vacuum power, detection of waveguide arcs, and excessive reflected power. The instrumentation assembly monitors the klystron RF output power, RF reflected power, RF input power, and coolant flow.

f. Remote control. This unit is a transmitter system remote monitor with limited control. To operate the transmitter from the remote control requires that all auxiliary power supplies and motor–generators have been previously energized. The remote control design is such that it can be completely disconnected from the system without affecting the operation, with one exception: for safety purposes a *safe-run* key interlock is in series with the *beam voltage on* circuitry. The remote control is a self-contained unit and has a control logic assembly consisting of 15 lamp drivers, one bistable circuit, and a separate dc control power supply. This design then allows the remote cabinet to be placed several thousand feet from the local control and still function properly.

This unit has been tested at DSS 13 for 30 days in the R&D 450-kW transmitter system. Only two failures occurred during this period: one failure was not a design problem and the other failure was caused by the inductive kick of a relay in the old system with which it interfaced. The problem was corrected by adding damping diodes.

The local control console and the klystron instrumentation cabinet will be tested at DSS 13 prior to installation at DSS 14. Static tests only will be conducted on the

control J-box, and preliminary testing of the motor–generator controls will be started.

5. Installation of High-Voltage Power Supply and Cooling System at DSS 14, *J. R. Paluka*

a. High-voltage power supply components. The major components of the high-voltage power supply and cooling system for the Mark III 400-kW DSN transmitter have been placed on their various pads and in the vault room. In addition, the mechanical alignment and shimming of all the rotating machinery has been completed. Power wiring to the major components is now under way.

Figure 9 is an overall view of the major components of the high-voltage power supply. The top left unit in this view is the 3500-hp, 2400-V, 3-phase, 60-Hz synchronous motor of the main motor–generator set. To its immediate right is the 1300-kV-A, 400-Hz, 3-phase generator which powers the high-voltage power supply. The eddy current clutch and 300-hp cranking motor appear to the right of the generator.

The box-shaped unit in the left center of Fig. 9 is the drawout disconnect for the 3500-hp motor. To its right is the breakmaster for the 1300-kV-A generator and finally, to its right appears the starter for the 300-hp motor. In the left foreground is the high-voltage vault room and to the extreme right is the still and chiller pad. Installation has been partially accomplished.

Motor–generator set. Figure 10 is a view of the main motor–generator pad looking to the south. The pedestal of the 210-ft DSS 14 antenna appears in the background. Progress in the areas of conduit fitting and wire pulling is evident from this view. Conduit and power wires have been installed for the motor starter, breakmaster, and drawout units.

Still and chiller. Figure 11 is a view of the still and chiller pad. These units will be used to provide a ready means of replenishing pure cooling water for various components of the transmitter.

In the right background of Fig. 11 is the auxiliary heat exchanger. This heat exchanger will be used to cool the eddy current clutch and the high-voltage power supply. Power wire has been pulled to this unit.

High-voltage power supply. The high-voltage power supply is capable of a 1-MW output and will be operating at approximately 64 kV for the Mark III klystron.

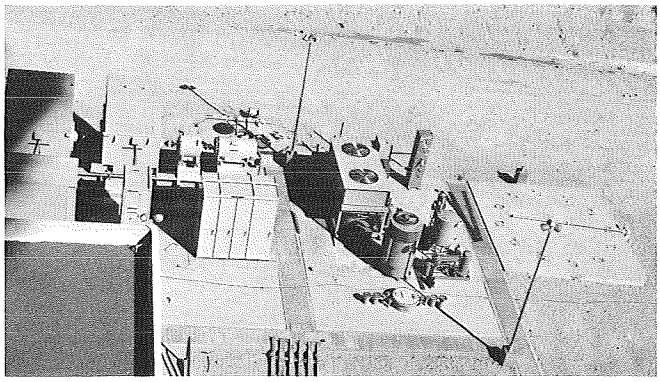


Fig. 9. High-voltage power supply

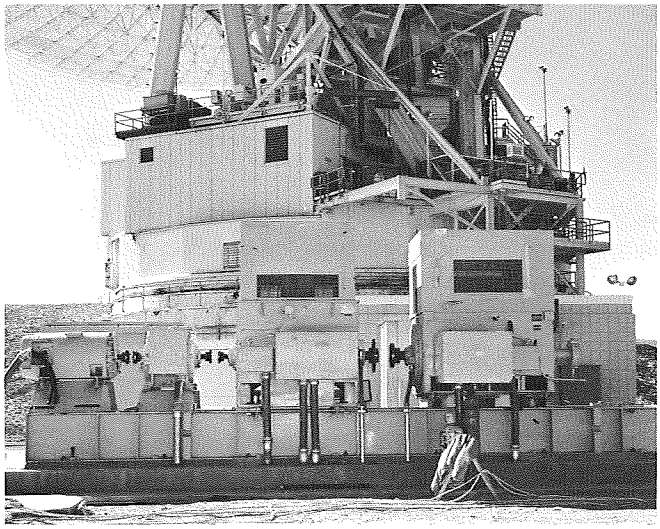


Fig. 10. Main motor–generator

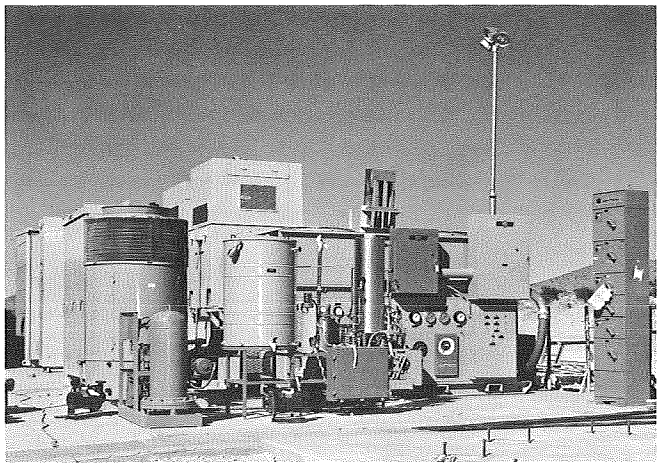


Fig. 11. Still and chiller pad

Weight of this power supply is approximately 42,000 lb. Power wiring has been pulled to all components with the exception of the high-voltage output wiring.

Main heat exchanger pad. The main heat exchanger pad does not appear in Fig. 9, but is located about 350 ft east of the still and chiller pad. Major assemblies have been installed on this pad and power wiring has been pulled.

The main heat exchanger, which has five 10-hp fans and four 50-hp pumps, is capable of dissipating 1 MW of heat. Under normal operations at 400 kW, only two pumps will be used at one time.

This main water-to-air heat exchanger, which uses a water–glycol solution will operate into an antenna-mounted water-to-water heat exchanger (pure heated water) which, in turn, will be used to cool the klystron in the tri-cone base.

b. System testing. System testing should begin on December 1. Prior to that time the power-supply component wiring will be completed. A dummy load for the power supply will be installed. Control wiring, which is fabricated and on site, will be installed by the electrical contractor. The alidade (water-to-water) pumping unit will be mounted on the antenna. Subsystem level testing will be done.

6. DSIF Monitor System Phase I Development, *R. Flanders*

The DSIF Monitor System Phase I (DSIF MSØI) provides the DSSs in the DSIF with a capability for monitoring the performance and alarm status of the various subsystems within each station. A record is also maintained on magnetic tape for postmission analysis, and real-time status and alarm messages prepared for transmission to the SFOF via high-speed data line.

The DSIF MSØI consists of a hardware segment composed of the Digital Instrumentation Subsystem Phase II (DIS II) and the station monitor and control console (SMC), together with a software segment represented by the DSIF MSØI program running in the DIS II.

The current effort involves the update of both the hardware and software, in order to provide monitor support for *Mariner* Mars 1971 and subsequent missions. Hardware development has been initiated to implement six stations (DSSs 12, 14, 41, 51, 62, and the Cape Kennedy Spacecraft Compatibility Station) with a capability for display of status and alarm data for station operational personnel. This equipment will typically consist of the following elements:

(1) Cathode ray tube (CRT) display.

(2) Image refreshing logic.

(3) Character generator.

(4) Addressable memory for data storage.

(5) High-speed data input/output registers.

(6) Control logic.

Data communication between the display equipment and the DIS II will be serial by bit via the high-speed data register and will be transmitted at rates of up to 50 kilobits/s. A keyboard on the terminal will provide for manual data entry and for addressing the display format of specific interest.

The principal effort in the software development involves the extension of the existing DSIF MSØI program. The present version was implemented on an interim basis for support of *Mariner* Mars 1969. As such, it offered considerably less than the full Phase I monitor capability. The version of the MSØI program to be implemented for *Mariner* Mars 1971 will contain routines for angle and range data processing, which were deleted from the present version due to core memory limitations. In addition, the program will provide for output to a graphical (X-Y) plotter for recording and displaying critical parameters. Typical parameters to be plotted as a function of time would include signal strength (AGC), static phase error, signal-to-noise ratio, transmitter power output, system temperature, and pseudoresiduals for doppler, angles, and range.

The program will also contain the capability to process data for display on the CRT and to output various display formats under operator control (addressable from the SMC display terminal keyboard). A revision of the present system for processing monitor criterion data (MCD) sets is also under consideration to reduce the volume and variations of MCD and provide for their definition at the individual DSS. The capacity for receiving and processing MCD, tracking, and RF predicts by way of high-speed data inbound to the station also offers a new capability.

The content of the high-speed data periodic and alarm messages to the SFOF is also under study, to investigate

the possibility of returning higher resolution data. The larger high-speed data block (1200 bits instead of 600 bits), together with a possibility for higher transmission rates may result in a redefinition of the DSN periodic and alarm messages.

The program will also be required to process monitor data from subsystems and equipment newly implemented for *Mariner* Mars 1971 support. This will include additional telemetry and command functions, and frequency and timing subsystem phase II (FTS II) monitor input parameters, when available.

The monitor functions within the DSS are also being redefined to be of greater value to station personnel for DSIF performance and alarm monitoring. The operational experience gained through use of the DSIF monitor system during the *Mariner* Mars 1969 missions will be reflected in these changes. Greater flexibility and control over alarm parameters to be displayed and the manner in which they are displayed will be provided at the station level. The means for calling up and displaying formats containing specific parameters will allow operational personnel to monitor critical parameters in greater detail than previously possible.

In summary, the DSIF monitor system phase I hardware is being extended, and the software is undergoing an extensive revision to process the new monitor functions to be implemented for *Mariner* Mars 1971 and increase the value of the monitor system to the DSIF by incorporating the experience gained in support of *Mariner* Mars 1969.

7. Frequency and Timing Subsystem, Phase II, *M. Galitzen*

For the past year the frequency and timing subsystem at DSSs 14, 41, 51, and 62 has been in a hybrid configuration referred to as FTS I/II. This configuration was necessary because of problems in the use of commercial equipment. The FTS II configuration required two commercially built isolation amplifiers for signal distribution. The digital isolation amplifier (DIA) exhibited bit pickup, bit dropout, and oscillation problems. The precision frequency isolation amplifier exhibited amplitude modulation, low isolation, spurious signals, and other lesser problems.

During the past months these problems have been under investigation, and steps have been taken to correct them. The DIA design has been changed, and the first reworked unit has been returned from the vendor. This unit was tested at JPL by connecting the FTS II outputs to the DIA. The DIA outputs were then connected through an FTS junction module to a load bank. Through one of the junction modules parallel outputs, monitor points were connected. Data from the points was recorded on a strip chart recorder.

No failures of the DIA were detected during this testing. This unit is now at DSS 14 where it has been installed in the FTS racks. At this time preliminary tests have revealed no problems with the DIA. On three separate shifts the FTS II configuration was connected, and the DIA's performance was flawless. At the end of these test periods the station was restored to the FTS I/II configuration for operational use. Further FTS II testing at DSS 14 will be undertaken before an effort is made to convert to the FTS II system operation on a permanent basis.

The precision frequency isolation amplifiers have been under investigation at JPL and at the standards laboratory at the Goldstone DSCC. These performance tests have verified that the amplifiers under test have been improved by the vendor. One of the units has been tested at DSS 12. The tests were accomplished by observing the stations' operation with and without the amplifier in the operations loop. Future evaluations are necessary before these units can be used.

The auxiliary reference divider and its control panel have been installed at DSS 14. The auxiliary divider is a working spare to the FTS II reference timing pulse generator. In the present configuration the spare divider provides a 1-pulse/s back-up pulse to the FTS standard 1 pulse/s. The standard FTS 1-pulse/s signal is clocked from signals derived from the FTS primary frequency standard. The auxiliary divider now provides an additional 1 pulse/s which is clocked from a secondary frequency standard.

The control panel for the auxiliary divider provides a means of synchronizing the auxiliary divider's 1 pulse/s output to the FTS primary 1 pulse/s signal. In addition the auxiliary reference divider control panel provides status indications on the 1-MHz secondary signal used to drive the auxiliary reference divider. At present it is planned to install this auxiliary system as DSSs 12, 41, 51, and 62 when these stations are converted to the FTS II configuration.

8. Analog Recording Flutter Sensitivity Tests, *J. P. Buffington*

In SPS 37-58, Vol. II, pp. 127–129, it was shown that the primary source of the data degradation in the telemetry recording subsystem is time displacement error (TDE). This was deduced from the shape of the constant 1-dB data loss flutter amplitude FA versus flutter frequency curves. The relationship

$$\text{TDE} = (FA)/\omega \cos \omega T$$

(where ω is the angular velocity of the flutter component) was developed, and initial steps have been taken to optimize the recording subsystem.

That amount of TDE which results in a 1-dB data loss can be computed by taking values of FA and ω off the data curves in the referenced article and substituting them in the equation above. Table 1 gives the permissible TDE for three subcarriers and their corresponding data rates.

Table 1. Values of TDE for subcarriers

Subcarrier frequency, kHz	Data rate, bits/s	TDE for 1-dB data loss, μs
24	8 1/3	25
34	66 2/3	10
259	16,200	3

A survey was made of the recorder field to determine the industry capability in minimizing TDE, and the Ampex FR 1600 tape transport was selected for evaluation. An abbreviated table of specifications is shown in Table 2, together with specifications for the FR 1400 (presently used in the DSIF net telemetry recording subsystem).

Table 2. Comparison of FR 1400 and FR 1600 at 30 in./s

Specification	FR 1400	FR 1600
Capstan servo carrier frequency	60 Hz	50 kHz
TDE, μs	400	2
2-Sigma flutter, %	0.25	0.30
Servo crossover Frequency (12 dB per octave), Hz	2	80
Reproduce bandwidth, kHz	350	500

The very large improvement in TDE in the FR 1600 over the FR 1400 is due to a substantial improvement in the bandwidth of the capstan servo and in the use of vacuum columns in the tape path to provide isolation from reel disturbances. The following schematic drawings illustrate the differences in the two mechanical tape transports. The relatively large diameter of the capstan on the FR 1600 facilitates reducing the length of magnetic tape between the capstan and the magnetic reproduce heads, which makes possible the relatively wide capstan servo bandwidth (Fig. 12).

The FR 1600 transport, when used as a subcarrier recorder–reproducer does, in fact, hold the TDE to a low enough value to allow the SDA to lock on to the reproduced data without any external flutter and/or TDE correction. The results (exclusive of conversion losses) are given in Table 3.

Table 3. TDE measurements for FR 1600 transport

Subcarrier frequency, kHz	Tape speed, in./s	ST_B/N_0 real-time	ST_B/N_0 after recording	Δ
259	30	3.5	2.4	1.1
34	15	5.6	4.7	0.9
24	15	5.8	5.0	0.8

These results were obtained with the capstan reference recorded on the adjacent track to the data in the same head stack. Tests indicate that the TDE of the FR 1600 is about four times as great under these conditions as it is between the local reference and the recorded reference track. A method of multiplexing the recorded reference in with the recorded subcarrier to take advantage of this improvement is being investigated in the laboratory at this time (Fig. 13).

It would appear that substantial improvements in the TDE of longitudinal recorders will be effected in the future, though in smaller increments and at great difficulty because of limitations in the supporting technology (e.g., grinding, machining, bearings, as well as the electromechanical components such as motors, etc.). As a result, electronic flutter and TDE correction methods are being studied in an effort to further optimize the recording subsystem. A block diagram of a TDE correction system that has been used with considerable success with rotary head transports is shown in Fig. 14.

In this system, a pilot tone from the local reference is multiplexed with the data and then separated out with comb filters and the reproduced pilot tone is again com-

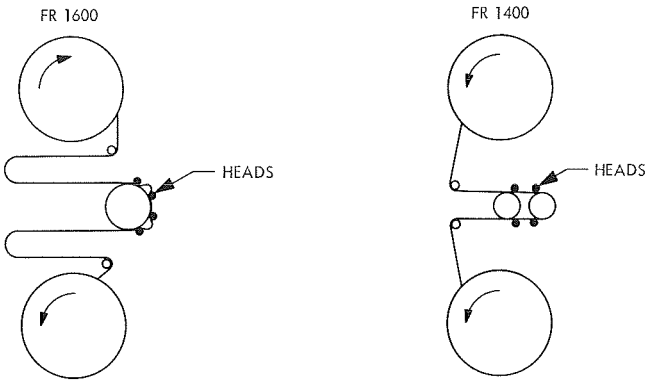


Fig. 12. Tape paths of FR 1400 and FR 1600 recorders

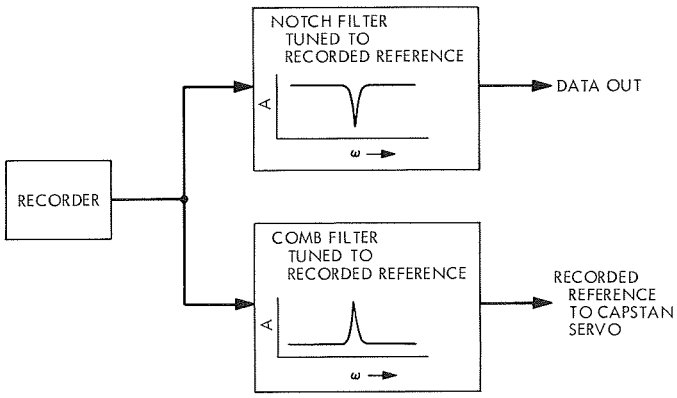


Fig. 13. Reproduce system using reference multiplexed with data

pared with the local reference; the difference, proportional to the time displacement error, is used to program the voltage variable delay line. In effect, the phase detector generates negative TDE which, when added to the positive TDE in the data, tends to cancel out in the voltage variable delay line.

9. Motor Field Control, *T. W. Rathbun*

a. Introduction. The 1750-hp motor generator set at DSS 13 is used to supply 400-Hz primary power to the 70-kV high-voltage power supply. It is important that the motor be operated at unity power factor so that the incoming power line is affected as little as possible by load conditions at DSS 13. This minimizes interaction between facilities at Goldstone DSCC, improves voltage regulation, and reduces power costs. Power-factor correction may be accomplished by adjusting field current in the synchronous motor. Originally, the power factor was controlled by a carbon pile regulator. The operation of the carbon pile regulator depends upon sensing low-line voltage caused by the high-line current associated with low-power factor. However, the incoming line to DSS 13 was of such low impedance that the line voltage was not sufficiently affected by low-power factor so the power factor correction did not operate reliably. During the start cycle the synchronous motor is acting as a generator whose output is controlled by field current. It is, therefore, possible to match the voltage output of the motor with the incoming line voltage. In the original installation no provisions were made for matching the line and motor voltage. The result was that the motor's protective circuitry prevented synchronization until man-

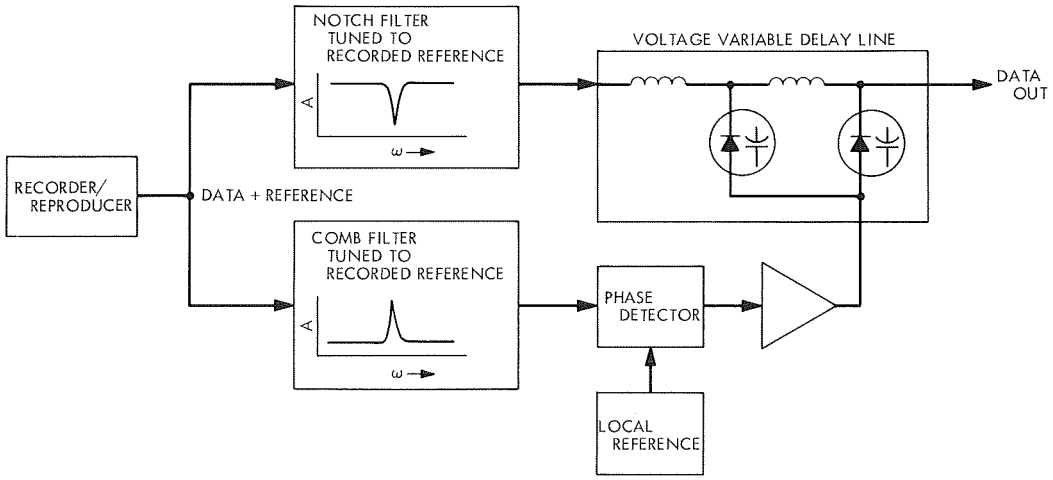


Fig. 14. Time-displacement error correction system block diagram

ual adjustment of the field current matched the voltages. This adjustment resulted in a power factor error when the motor was on the line, and readjustment was necessary.

A commercial power factor control unit was tested to determine its suitability to replace the carbon pile regulator. However, the operation of this unit was not satisfactory because of errors in the order of 5% when the motor was lightly loaded.

b. Description of new unit. A new control was designed, breadboarded, and installed at DSS 13. This control contains line-motor voltage matching circuitry (Fig. 15), and a digital phase detector (Fig. 16) for power-factor control after the motor is brought on the line.

The line-motor voltage matching section of the motor field control contains a voltage transducer, which is a full-wave bridge that is linearized by the use of a small value of resistance in parallel with the output resistance. A transducer is used on both the line and motor voltages. The dc voltage output of these transducers is then applied to a voltage comparator circuit whose output controls the motor field-power supply.

The power factor section of the motor field control consists of a digital phase detector, which samples the motor current and motor-voltage phase relationship. The output of the phase detector is zero at unity power factor,

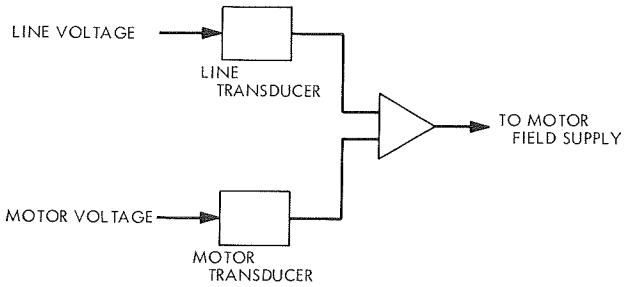


Fig. 15. Line-motor voltage matching circuit

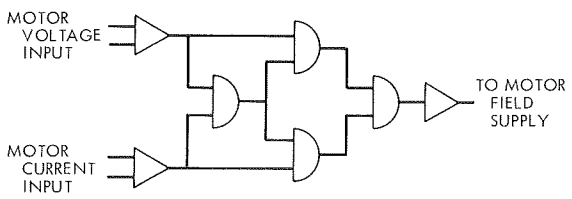


Fig. 16. Digital phase detector logic

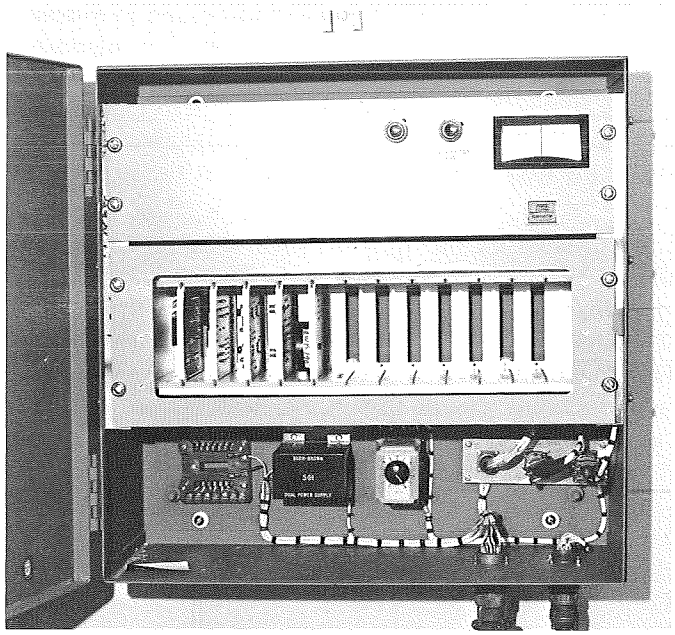


Fig. 17. Prototype motor field control on time-synchronization transmitter

positive for a leading power factor, and negative for a lagging power factor. This output is integrated and applied to an operational amplifier capable of driving the motor field-power supply, resulting in a power-factor control that is not dependent upon line variations nor upon motor loading for control. Laboratory tests of the phase detector showed an accuracy of ±0.5% at worst-case conditions.

The original breadboard has been in operation at DSS 13 in the S-band system for approximately 1 yr with no failures. A prototype (Fig. 17) has been built and installed in the X-band clock synchronization transmitter system of DSS 13. Operation of this unit has been satisfactory for about three months.

c. Future plans. Two production units are scheduled to be delivered during the next reporting period. One of these units will replace the original breadboard model at DSS 13, and the other will be installed at DSS 14 during December of this year.

B. DSN Projects and Systems Development

1. Clock-Synchronization System Performance, *H. W. Baugh*

a. Introduction. A precision clock-synchronization network is being established to meet the requirements of the DSN. The immediate goal for this system was to provide