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THEORY AND DESIGN OF
RELIABLE SPACECRAFT DATA SYSTEMS

Project Director

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Jet Propulsion Laboratory
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TABLE OF CONTENTS

	Page
1. Introduction	1
2. Redundancy Techniques - Summary	4
3. Redundancy Techniques - Bibliography	11
4. Fault Diagnosis - Summary	16
5. Fault Diagnosis - Bibliography	22
6. Reliability Analysis - Summary	27
7. Reliability Analysis - Bibliography	36

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1. INTRODUCTION

The principal effort during this past quarter (2/10/69 - 5/9/69) has been a survey of literature related to each of the three proposed areas of investigation (as stated in Article I of the contract), namely:

- i) Design and analysis of redundant combinational and sequential networks,
- ii) Fault diagnosis of redundant systems at both the component and subsystem level, and
- iii) Data system reliability analysis.

This survey was conducted by three Research Assistants who have been working one-half time on the project since 2/10/69. They are Gail Gray, John Kinkel, and Ken Yeh; Gray and Yeh are graduate students in the Program in Computer, Information and Control Engineering (College of Engineering) and Kinkel is a graduate student in the Department of Computer and Communication Sciences (College of Literature, Science, and the Arts).

The scope of the literature surveyed was intended to be broad enough to include any previous effort that might be relevant, either in substance or methodology, to at least one of the proposed areas of investigation. Accordingly, three general subject areas were designated for the purpose of the survey:

- A) Redundancy techniques
- B) Fault diagnosis
- C) Reliability analysis

with one Research Assistant assigned to each area: Gray (A), Yeh (B), and Kinkel (C).

Summaries of the individual surveys appear in Sections 2), 4), and 6) of this report. Each summary is based on a bibliography of 50 references selected from a total bibliography of about 500 entries. The latter is maintained in a card file at the University and will periodically be updated. The selected bibliographies are documented in Sections 3), 5), and 7) of this report. The bibliography format chosen conforms closely to that of the IEEE publications. The authors' names, title of article, and name of source - book, periodical, or contract report - follow in succession. Then comes the name of the publisher (books), volume and number (periodicals), or company report/ADA number (reports). Following the date of publication, the length of books is indicated by the number of pages; the beginning and ending page numbers are given for all other articles.

As of the beginning of the next quarter (5/10/69) and per agreement with JPL, future effort on the project will be limited to areas i) and ii) above. During the next quarter we will begin a more detailed investigation of some of the questions posed in the statement of work. In particular we intend to fully explore the model of permanent memory failure discussed in the proposal with initial emphasis on classifying various types of finite-state realizable behavior according to some appropriate measure of memory error susceptibility. If we take the measure of susceptibility of an n -state realizable function f to be

"the minimum number of (2-state) memory cells required in any network realization of f that masks all combinations of m or less memory cell failures", it can be shown that certain types of behavior are inherently more susceptible to error than others. In this regard, one conjecture which we hope to establish is that modulo n "counters" (or "clocks") are highly susceptible to memory error and, for certain moduli, require a maximum amount of redundant memory in their realization.

In connection with the general problem of diagnosing redundant networks, a second question we wish to explore immediately is one of formalizing the concepts of "network" and "fault" in a way that permits an investigation of tradeoffs between fault tolerance and fault diagnosability. One possibility is a formulation similar to Urbano's notion of a "polyfunctional net" where relative to a given "function assignment", a network N is "perfectly fault-tolerant" if N realizes a single function (under the assignment) and N is "perfectly fault-diagnosable" if the number of functions realized by N is equal to the cardinality of the assignment. The second Quarterly Progress Report will also include a more definitive statement of the work to be performed during the first year of the project.

2. REDUNDANCY TECHNIQUES - SUMMARY

This article is a concise survey of recent literature pertaining to redundancy techniques in switching networks, sequential machines, and computers. The three areas considered are listed below:

1. Coding techniques for error-correction and error-detection,
2. Replication of circuit elements at the component or basic function level,
3. Organizational techniques for sub-system redundancy.

This summary and the attached bibliography describe specific examples of progress in each area. An attempt is made to include representative samples of distinct approaches to circuit redundancy rather than to compile a complete bibliography. Multiple papers by the same author on related topics are omitted, and only the most recent or most important papers describing a particular technique appear.

One way to improve the reliability of switching networks is to introduce signal redundancy through the use of error-correcting codes. Early coding techniques described by Peterson [A26] were developed to correct or to detect errors that occur during the transmission of data over a noisy channel. A general method of applying error-correcting codes to the design of synchronous digital systems was first discussed by Armstrong [A4]. These methods allow a more precise localization of faults than do such replication techniques as

triplication and voting [A45]. However, because an efficient maintenance routine is required to achieve reliability improvement, Armstrong's methods may not be applicable to the ultra-reliable requirements of space-borne data systems.

Kautz observed [A18] that known optimal codes for communication channels are not necessarily optimal for data system applications and evaluated the extent to which codes may be applied to data systems. A class of codes called "low density codes" was proposed for applications where communications channel codes failed to be optimal. Kautz concluded that error-correcting codes, including low density codes, could best be applied to the elimination of errors originating in I/O links, memory, control and index registers, and during transmission of data along communication buses, but that other techniques were required to handle errors originating in arithmetic units, code converters, and in portions of the system that analyze, transform, and process data.

More recently, error correcting codes have been applied to the design of basic sequential circuits. It has frequently been observed that a state assignment for a sequential machine is a binary code with each internal state corresponding to a word (or message) in the code. In fact, it is always possible to use a minimum-distance 3 code as the state assignment in a redundant counter to mask single faults of either the permanent or temporary variety [A35]. Transient faults are also automatically corrected

provided only that the affected flip-flop is not required to change state at every step in the counting sequence. A recent short note [A11] suggests a generally applicable technique for applying error-correcting codes to the feedback loops of sequential machines in order to improve reliability. No specific design procedures are given.

Other researchers have investigated separately the masking of permanent and transient faults in sequential machines. A completely general model for the study of permanent memory failure in finite automata is developed by Meyer [A20]. Results are obtained that allow masking of any fixed number of elementary cell failures, i. e. cells that fail to the zero state or to the one state. Several interesting and important questions are raised that merit further research investigation. The identification and classification of finite automata behaviors that are intrinsically less susceptible to permanent memory failure than others is perhaps the most promising.

Transient errors in sequential machines have also been approached from the machine-theoretic viewpoint. Winograd [A48] identified a class of finite automata that is capable of recovering from an input error in a bounded period of time. Input error limiting automata is the name often applied to this class. Harrison obtains results on the structure of such machines and shows the equivalence of the class of input error limiting automata with the class of automata capable of recovering in a bounded period of time from errors caused by being in an erroneous

internal state [A15].

Investigation of a second class of redundancy techniques, often referred to as massive redundancy or replication, began with von Neumann's classical work [A45]. Since then, various techniques involving circuit replication have been proposed and investigated. In particular, the von Neumann scheme of triplication and voting has been rather thoroughly explored. Such investigations include the optimization of voter placement [A33] and the reduction of triplication to duplication by assuming a unique failure mode [C6]. However, this uniqueness assumption is invalid for most devices and circuit designs currently in use. In a Russian paper [A37], von Neumann's techniques are combined with coding techniques to produce reliable finite automata.

Other replication techniques are based on the iteration scheme first proposed by Moore and Shannon [A21] for contact networks. In particular, Urbano attempted the iteration of more general types of networks with success in specialized cases. He reduced the problem to convergence of a sequence of sets of functions which was found difficult to solve in general. Another replication technique known as "quadding" [A41] was used successfully in the design of combinational and simple sequential fault-masking circuits.

Stochastic models for finite automata have been used to obtain a two step design procedure for reliable sequential networks [A42, A43]. The first step obtains the required reliability of each component

in a system to produce a desired system reliability. The second step uses known replication techniques to achieve the necessary reliability of each component.

A third area of investigation is concerned with methods of organizing systems with redundancy at the sub-system level. Such techniques are generally more efficient than replication techniques for the ultra-reliable requirements of space-borne data systems because sub-systems may be added or removed in flight to meet widely varying computational loads encountered during different phases of a mission. One such study [A19] analyzes the memory, speed, reconfiguration, availability, and reliability requirements for a Mars landing mission hypothetically scheduled for 1980. A modular processor organization was found to be more efficient than either a multi-computer organization or a distributed processor organization using small groups of LSI components as switchable modules.

Several architectures for self-repairing computers have been proposed. A technique called "partitioning" has been demonstrated to be an effective means of achieving self-diagnosis with small amounts of additional hardware and a minimum of hardware [A1]. An experimental Self-Testing-And-Repairing (STAR) computer has been designed and is being built by Jet Propulsion Laboratories to serve in further research and evaluation of self-repair techniques [A5]. The STAR computer employs a balanced mixture of coding,

fault-detecting, standby redundancy (switchable sub-systems), and triplication with voting to obtain self-repair controlled by system hardware and to protect against transient faults.

Another promising scheme for sub-system modular redundancy in space-borne data systems assumes that a large ratio of program storage to data storage exists, and a large number of independent control loops that manipulate relatively small amounts of data exists [A3]. This condition exists in guidance computers for space missions, for example. Modules consist of central processing units, fixed program memory units, job stacks, common data memory units used by all programs, and I/O units all interconnected via a common communication data bus. A multiplexing scheme is employed to allow all units sequential access to the bus. In actual operation, a job stack broadcasts a job request onto the bus. All available processing units record this request, and the first processor to gain access to the bus accepts the job and transmits a job acceptance message onto the bus. Upon completion of the job, a processor broadcasts an end of job message recorded by the job stacks. No processing unit is a master unit that must be operating to control the others. All have equal status and may be removed from the system in case of failure without causing a system breakdown. Thus, the number of modules could be reduced to the extent that the total work load is handled without adverse effects on the system. Graceful

degradation is then possible to allow only the handling of high priority jobs as long as even one module of each type is operational.

Jobs are organized to issue results only at the end of job execution, so that any error detected by the processor during the job can be corrected by having the processor issue an error message on the bus at its next access time. The job stack then reassigns the task to another processor and removes the faulty processor from the system if required. Memory modules store words in electrically separate units. Job stack modules store job status redundantly in electrically separate stack units. Several similar or alternate I/O units are provided. The data bus is the central problem and must be itself designed using replication techniques discussed previously.

The relationship between fault diagnosability and fault tolerance in a network is an open research problem. It appears that some generalization of the analysis of polyfunctional networks [A44] could be applied to the solution of this problem. A system can be viewed as a network of interconnected nodes. Each node is assigned a set of functions that includes the desired function of the node as well as all error modes. If a fault at some node does not change the network output function, then that particular fault is masked regardless of its origin. If, however, a fault changes the network output function, then it is diagnosable at the terminals of the network. A fault cannot be both masked and diagnosed at the network terminals. This model may allow investigation of tradeoffs between fault tolerance and fault diagnosability.

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4. FAULT DIAGNOSIS - SUMMARY

This summary and the bibliography that follows is the result of a survey of literature related to the problem of diagnosing faults in switching networks and systems. The summary includes a brief discussion of fault detection and location in combinational networks, but emphasis is placed on the diagnosis of sequential networks and digital systems.

The most fundamental approach to the problem of fault diagnosis in combinational networks is a truth table method [B25] in which all input combinations of the network are checked. An analysis procedure has also been developed which incorporates the network structure into an output Boolean expression [B38] from which a fault table can be constructed. Although these methods give rise to optimum solutions, they are too lengthy to be applicable to networks of practical size. Armstrong [B2] has used the concept of "path sensitization" for analyzing a network and developed an algorithm for deriving near optimal fault detecting tests for logical failures of stuck at 1 and stuck at 0. Roth [B43] has also used the same concept to develop an algorithm suitable for computer implementation. The removal of test redundancy has been considered by Chang [B8] who used the distribution of 0 and 1 of each test in the fault table to determine the weight of the test. Most recently, Powell [B40] has considered a probability weighting of tests for fault location to within package

level. One crucial assumption in most of these methods is that there is at most one fault at any given instant of time. Tests designed under this assumption may not be valid if the fault is preceded by another fault even in the case where the preceding fault is undetectable.

Regarding the fault diagnosis of sequential machines, there is still need for a "good" general diagnosis procedure that is not exhaustive in nature and applicable only to machines with a small number of states. This situation will probably remain unchanged until some better synthesis procedures incorporating diagnosability into machine design can be achieved. There is also a need to investigate special diagnosis procedures applicable to special classes of machines and networks, particularly the class of networks in which the reliability is enhanced by fault-masking redundancy.

A "synthesis for diagnosability" point of view has been taken by Kohavi and Lavalley [B29] where they have considered the problem of designing "definitely diagnosable" (D. D.) sequential machines.

(A sequential machine with n states is definitely diagnosable if every input sequence of length greater than $n(n-1)/2$ is a distinguishing sequence.) However, definite diagnosability is not a necessary condition for the design of a checking experiment and does not contribute to reducing the length of the checking experiment. All that is needed in designing a short fault detecting experiment is to find a distinguishing sequence of repeated symbols of shortest length.

The major contribution of the paper is a reduction of Hennie's upper

bound [B20] on the length of a checking experiment rather than a new synthesis method for fault detecting sequential machines. The problem of whether the D.D. property can be employed to design good fault locating sequences remains unanswered.

The second article that deals with diagnosability from a design point of view is due to Preparata, et. al. [B41]. They considered the problem of partitioning a system into mutually exclusive units where each unit is a well defined portion of the system which cannot be further partitioned for the purpose of diagnosis. The units are then preconnected in such a fashion that each unit can test a subset of units. It is then possible to design diagnosis experiments for all diagnosable fault patterns. The necessary and sufficient condition for a one step t -fault diagnosable pattern bears close resemblance to that of t -error correcting codes. Interesting questions raised in the paper are: what is the best network topology; what is the complexity of the new architecture; and what are the limiting factors it may impose on the performance of the machine.

Hannigan and Masters [B19] have considered the problem of test point allocation in triple modularly redundant digital systems. The criterion for selecting test points is based on maximizing the information gain of observing an erroneous signal. Each test point, therefore, could be located at either the output of a restored function or a system output. The procedure involves computing each potential test point's conditional probability that a failure will be observed,

given that the system is functionally operational. This conditional probability is then used as a basis for selecting test points. One major difficulty of the method developed lies in the assumption of being able to find independent "blocks" in the system. The optimality of test points selected is reduced significantly when the interdependence of blocks increases. Furthermore, the grouping of subsystems into "blocks" may not be an easy task for more complex systems.

Other approaches to the fault diagnosis problem employ fault simulation. In the category of fault simulation, two techniques have been widely practiced so far; physical fault simulation and digital fault simulation.

Physical fault simulation was first employed in the compilation of fault dictionary for the maintenance of Bell Telephone's No. 1 ESS central control as described by Tsiang and Ulrich [B50] in 1962. The diagnostic programs consist of many sets of test patterns each designed to exercise some portion of the machine. These tests are manually derived by engineers who analyze individual circuits. The dictionary is compiled with the actual insertion of physical faults into the central control by means of a Fault Simulation Unit. For each fault, the package number and test identifications that failed to pass are recorded on a magnetic tape which is later sorted, processed and printed out in a dictionary form. To locate a faulty package in the field, the technician simply "looks up" the observed fault pattern (which is just the sequence of tests the machine failed to pass) in the dictionary. The

major difficulty of this method are test inconsistencies that accounted for 15 to 20 percent of the total faults encountered. This difficulty has been greatly reduced by using different methods of interpreting the test results as reported by Chang and Thomis [B9].

The late Professor Seshu pioneered the work of digital simulation for the automatic generation of diagnostic schedules for asynchronous sequential machines [B46]. The first problem he dealt with was to write a computer program which read in the logical description of a circuit and produced a sequential testing schedule for that circuit. The testing philosophy is essentially a multiple experiment in the sense of Moore. Consider first an asynchronous machine which has N possible faults. If each fault is considered as a transformation of the original machine into a different machine then there is a total of $N+1$ machines to distinguish for fault location. The program, therefore, implements a decision tree which branches out to each isolated fault or to a set of indistinguishable faults as the test proceeds. Two criteria for test acceptance are used; the first one is to choose a test which minimizes the number of machines in the equivalence class containing the good machine; the second one is to choose the test which maximizes the information gain from the test. The major weakness of the algorithm is that it is very sensitive to the reset memory state and the first input used. Furthermore, no "good" basis for choice is available at the beginning of the test.

A comparison of these two fault basis simulation methods has been made by Chang and Manning [B36]. At present, physical simulation uses less computer time than does digital simulation. However, improvement in digital methods may result in more efficient algorithms in the near future. Moreover, the amount of flexibility enjoyed by digital methods may offset efficiency considerations in many present-day applications.

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6. RELIABILITY ANALYSIS - SUMMARY

This summary of reliability analysis methods covers seventeen papers drawn from six journals. Thirteen of the papers appeared in the IEEE Transactions on Computers or the IEEE Transactions on Reliability. An emphasis has been placed on articles published in the last five years and preferably in the last three. Results based on obsolete technologies or unique equipment configurations are rarely generalizable.

The papers are grouped into two categories: models for reliability analysis and calculations of performance measures. The first category contains papers that deal with physics models, redundant systems and adaptive systems. The papers in the second category are concerned with probability formulas, failure-rate relations, and performance measures.

Models for Reliability Analysis

Considerable attention has been given to modeling systems for analysis on a macroscopic basis. Macroscopic models are introduced to explain general failure phenomena, such as deterioration with age. In [C37] the usual probability distributions - exponential, normal, Rayleigh and Weibull - are developed on such a heuristic basis. The approach is to consider the strengths of the component or subsystem in the aggregate and the stresses placed on it by the environment. Parameters are available for fitting distributions to empirical results.

but none are offered. In particular no hard justification of the whole procedure is offered.

A rebuttal to the above methods has been made by Flower in [C11]. The author discredits the probabilistic origin of failures, but allows for their stochastic detection. The contribution of the paper is a classification of failure sources: improper design or insufficient capability, faulty or damaged hardware, and deterioration arising from physics of implementation or environment. The author's suggestions for controlling these sources of failure are relevant to the extent that certain types of failures - such as bonding and "purple plague" - will not continue to predominate over others.

An overview of component failure analysis in [C50] describes component failures that were uncovered by the failure analysis program at JPL. The discussion clearly indicates that the most troublesome failures result from manufacturing and testing malpractices, thereby supporting Flower's point of view. This also indicates, however, that the failures are technology dependent. The implication is strong that when manufacturing and testing are automated, the methods of [C37] (physics models) may become useful.

Apart from the immediate implications of technology, there are problems of allocating limited resources to maximize system effectiveness. Questions of system organization naturally arise, but the primary emphasis is on the methods and measurements of resource utilization.

In [C28] the optimum strategy is determined for repairing sub-systems to achieve maximum system life. The prototype system has only two components, each with a redundant copy, such that all four combinations are usable. The strategies are to repair in the order of failure or to allow component priority. The problem is central to dynamically organizing systems for maximum life, but the author's analysis appears to be unnecessarily cumbersome.

Both [C10] and [C12] consider the allocation of redundancy to an n -stage serial system under a cost constraint. A weight constraint is also included in [C12]. The number of parallel copies for each stage is determined for subsequent use depending on stage implementation and reliability and the system constraints. The problem is solved with a variational technique in [C10] and with dynamic programming in [C12]. A natural extension of this approach is to consider functional requirements, instead of resource constraints, for a more general analysis of system performance.

The papers [C25] and [C24] deal with specific designs for graceful degradation. Under the assumption that certain system states are acceptable failure states, the object in [C25] is to design the system to home in on these states under all failures. The method is based on obtaining monotonic switching functions. At most twice the hardware necessary to realize a function is necessary to achieve fail-safe behavior.

In [C24] a system is described to circumvent failures in computer logic. The object is to use alternative groups of microinstructions to perform calculations when individual instructions are compromised by hardware failures. The modularity of the system is emphasized, but only a few examples of software alternatives are described.

A more specific application of modular construction to computing is given in [C40] and [C41]. The papers do not consider the reliability problem, but clues to related questions abound. In particular the problem of communicating in a modular environment is handled in detail. Also the question of a basic set of instructions - at least for this organization - is answered. As several references note, asynchronous operation reduces dependency on a central clock and related connections.

Calculation of Performance Measures

Several methods are available for computing the reliability of systems; these include Laplace transforms, differential equations and analysis of Markov chains. These methods, however, are applicable only to very simple systems.

In [C19] a special case is introduced which yields a practical method for computing system reliability for some systems. The special condition is that the product of the number of components and the time interval of interest are small compared to the mean life of the components. A systematic consideration of only those failure patterns critical to the system leads to a simple reliability calculation.

The enumeration of failure patterns begins with the simplest and continues until the accuracy specified by the problem is exceeded. This approach depends on assuming that the system failures are Poisson distributed and the failure rate is much less than the repair rate.

The probability of exactly i failures in a time period of length t is derived in [C48]. The system consists of n independent, identical subsystems with s spares. The spares are substituted instantaneously with probability equal to one upon failure. The derivation is based on developing a recurrence relation and using induction; the result is expressed in terms of Sterling numbers.

To develop a relationship between system and component rates, Esary and Proschan [C9] consider a structure composed of independent identical components with common probability distribution $F(t)$. Each component has reliability $p = 1 - F(t)$ at a given instant of time and designating the system reliability by $h(p)$, the authors prove that

$$\left. \frac{ph'(p)}{h(p)} \right|_{p=1-F(t)} = \frac{R(t)}{r(t)}.$$

$R(t)$ is the system failure rate and $r(t)$ is the component failure rate, both at time t . The importance of this result is to note that the left hand side is a decreasing function of p if and only if the right hand side is an increasing function of t . An immediate consequence of this observation is that if $r(t)$ is an increasing function of t and $ph'(p)/h(p)$ is a decreasing function of p , then $R(t)$ is an increasing function of t .

Thus a simple sufficient condition has been obtained for a system to have an increasing failure rate when the identical components have an increasing failure rate. Those systems which operate if and only if at least k out of n components operate constitute an important class of structures for which $ph'(p)/h(p)$ is a decreasing function. New structures with this property can also be obtained by composition of structures with the property. For systems of non-identical components satisfying the property, $R(t)$ can be bracketed by bounds which are strictly increasing if the component failure rates are increasing.

Brender in [C3] considers the uncertainty that exists between predicted and actual failure rates. The purpose of his paper is to relate 1) the uncertainty in the number of predicted system failures to the uncertainty in the system failure rate, and 2) the uncertainty of the system failure rate to the uncertainty in the failure rates of the components. The reduction of uncertainty improves system failure rate prediction and is clearly information about system performance. In the paper an expression for uncertainty in the system failure rate is obtained, average component uncertainty is defined, and the minimum uncertainty in system failure rate when component types are the same is calculated. Then the uncertainty in the number of system failures and the relation to subsystem failure uncertainty is evaluated. The conclusions of the paper are that 1) the uncertainty about system failure rate is often considerably less than that associated with the average component type, and 2) the uncertainty in the number of

system failures is always greater than the uncertainty of system failure rate for all intervals.

The more general question of system effectiveness is taken up in [C21] where "system effectiveness" is a generalization of the various concepts of "system availability" which have been proposed. (The author shows that availability can be given eighteen "meaningful" definitions.) The study of effectiveness is meant to formalize the interaction between behavior statistics, performance capability, and functional requirements. System effectiveness is defined as the extent to which performance objectives are met. Estimation of system effectiveness is by probabilistic analysis covering capability, state probability distributions, and vulnerability (environmental influences). Analytic methods for system effectiveness prediction are supposedly given in the references. An example of one technique is applied to a data processing complex. The measure of effectiveness was service availability based on total computing speed.

In [C23] Meyer defines a measure of system reliability that accounts for not only total success, but also for various degrees of partial success. First the system is defined in terms of its component set, probability space, and behavior; these are the attributes that influence its reliability. Then the concepts of performance and utility are introduced and used to define system reliability. The paper concludes with a discussion of permanent failures and consistency.

In [C8] Dorrough approaches the problem of designing and evaluating a self-repairing computer. He equates failure with error and treats dynamic systems informationally both with respect to failure and repair. Self-repair is the correction of or compensation for internal error and is accomplished by redundancy or adaptation. Configurational and functional redundancy are discussed in detail. The problem of developing a self-repairing system requires a system effectiveness measure and an informational network for detecting and repairing (or adapting to) failures. The system effectiveness measure employed is called the Performance Capability Measure (PCM). It is the sum over non-catastrophic system states of the probability that an error in a critical parameter is less than some maximum allowed amount while in a given state, weighted by the probability of being in the state. Probabilities are computed from Laplace transform and Markov chain methods. Use of the PCM for evaluation of effectiveness is accomplished by partitioning the state space according to a method developed by Pierce. Figures of merit are introduced for optimizing the tradeoff between PCM and constraints on system implementation. Implementation of self-repairing systems is based on interwoven logic for configurational redundancy and multifunction logic for functional redundancy. The design of a self-repairing computer is undertaken to demonstrate the various techniques. A hard-core is presumed and simulation is required to evaluate the design techniques

applied to the memory, central processing, control, and input-output units. No consideration is given to the collection of diagnostic information or more modular types of organization.

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