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A SERIES CAPACITOR INVERTER-CONVERTER FOR MULTIKILOWATT POWER CONVERSION

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Cambridge, Mass.

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SUMMARY

A nonlinear, active network that transforms the voltage waveform of a unipolar source of energy is presented. This network consists of ideally lossless elements such as inductors, capacitors, and on-off switches. Control is obtained by variation of the mode of switch operation. A circuit philosophy is applied which is adapted to the characteristics of switch operation and confines the stresses imposed on circuit components to moderate levels. Results of experimental work are reported and include (1) test data of a 95% efficient, 2-kW dc transformer having a power density of 0.4 kW/kg; (2) integration of this transformer with an ion propulsion engine.

INTRODUCTION

A network is introduced which transforms the voltage waveform $e_s(t)$ of a source of electric energy to another voltage waveform $v_O(t)$ as required at a load Z_L. The network is first presented in form of a dc transformer; this is followed by indication of other applications, such as power amplifiers, inverters and converters.

Transformation of dc potentials, such as scaling and stabilization, requires the successive processes of inversion, ac scaling with the aid of a transformer, rectification, and finally, filtering. Inversion can include forms of pulse modulation, such as pulse width or pulse frequency modulation, and implement dc voltage stabilization and scaling, concurrently (refs. 1,2). The physical weight and size of an apparatus, and its efficiency of conversion, depend largely on the frequency of the inversion process which is, in turn, limited by the interdependence of the characteristics of networks with those of their component parts.

Semiconductor switching components, such as power transistors and controlled rectifiers, are the most vulnerable circuit elements (refs. (2,3). The damage susceptibility of switching elements during their on-off operation increases with the ratio of transient to steady-state stresses. This is proportional to the efficiency of conversion or processing of power and is due to the intended minimization of the ratio of resistive to reactive elements in these circuits.

Modes of Current Switch Operation

Common solid-state converter circuits, such as parallel inverter-converters, employ modes of operation that are based on the forced interruption of load currents as part of their cyclic operation (refs. 2,4,5). This mode of operation imposes considerable stresses on the switching components, especially at the termination of the quasi-rectangular current pluses. The power dissipation in the collector circuit of a power transistor operating in the indicated switching mode is illustrated in Figure 1. The oscilloscope trace displays the power dissipation as a function of time. The dissipation curve is similar in shape to that of the pulsating load current, except for the sudden and substantial rise after the initiation of pulse termination. The display was observed on a conventional oscilloscope and obtained from the signal output of a wideband wattmeter (ref. 2). The "tail" in the dissipation curve occurs as the switching element undergoes the transition from the conducting to the nonconducting state. The shape and size of this part of the dissipation curve depend solely on the network and device characteristics, and are independent of the frequency of operation. The area under this part of the curve corresponds to the dissipated energy per cycle. The power loss due to this phenomenon is proportional to the resulting watt-seconds per second, i.e., the number of cycles per second, and constitutes the frequency-heat barrier for efficient inverter

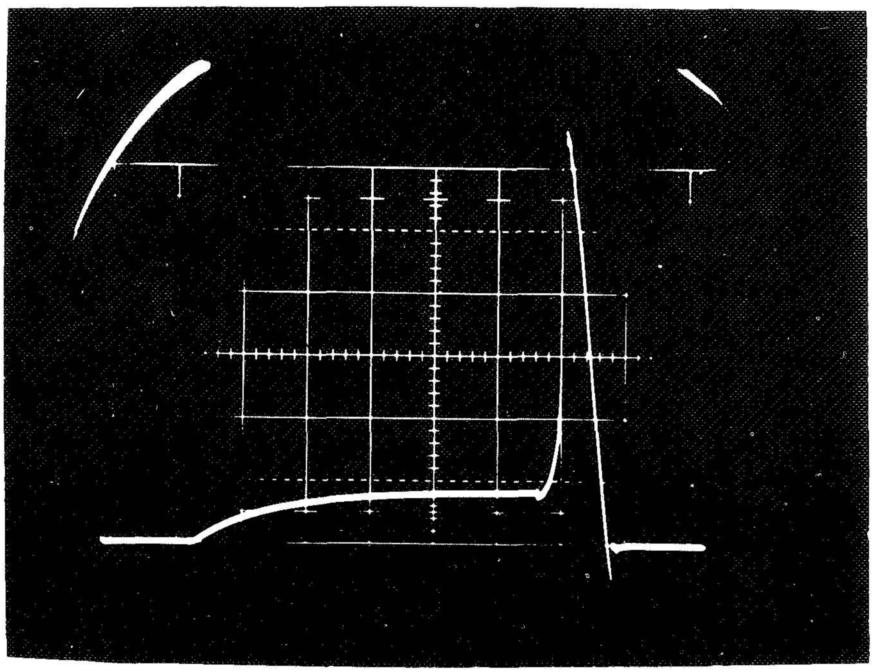

Figure 1.- Power dissipation of the switching transistor in an inductive circuit, $i_{cmax} = 5A$; $L \approx 10\mu H$

operation. The series capacitor inverter-converter employs underdamped series resonant circuits in which cessation of the load current precedes, and is the causal mechanism for opening of the switching elements (refs. 1,2,6).

The power dissipation in the switching element is therefore near zero during its opening process. The series inductor L in Figure 2 limits the rate of rise of current after initiation of current conduction in any of the switching elements CR_{11} or CR_{12} such that this current cannot attain a value of significance during the closing process of the switch. The trace of an oscilloscope shown in Figure 3 indicates the power dissipation in the switching element of a series resonant circuit. Power dissipation

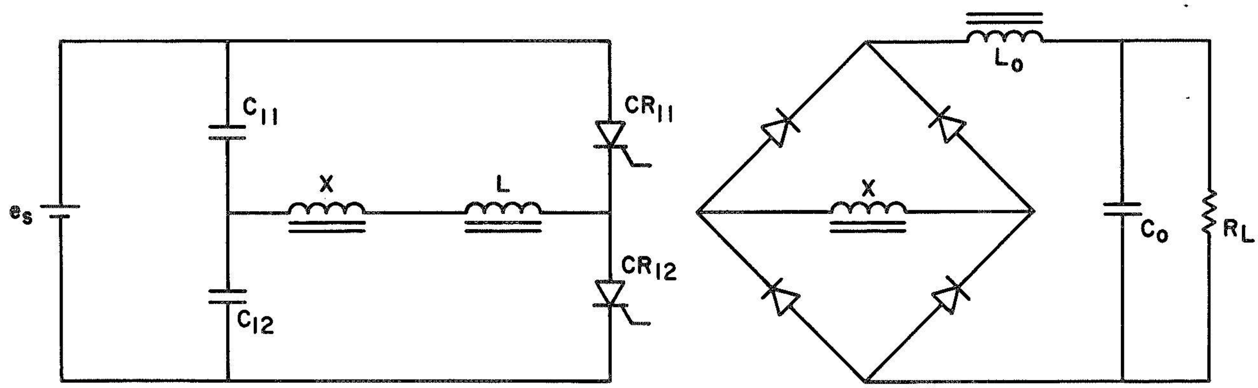

Figure 2.- Conventional series inverter-converter circuit

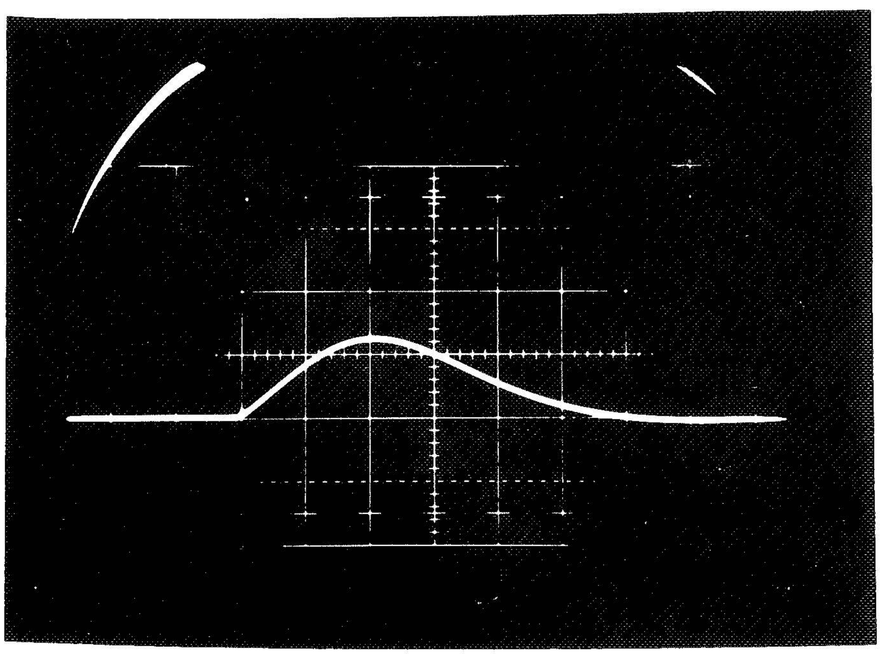

Figure 3.- Power dissipation of the switching controlled rectifier in a series resonant circuit, i_{max} = 7A

in the switching elements is confined to the conduction time and is therefore independent of the frequency of operation for a given current level and of the ratio T_k/T_{ok} where T_k is the time of conduction during one cycle with duration T_{ok}. The frequency-heat barrier is thus removed and the frequency of operation is limited only by the speed with which the switching elements can close and open.

The Series Inverter

The common series inverter is said to suffer from two significant inadequacies (ref. 1): (1) it cannot be controlled; (2) it is load sensitive. Other shortcomings one hears mentioned are: (1) the relatively low frequency of operation resulting from a lengthy recovery time for silicon controlled rectifiers (SCR's) and (2) the hazard of an unscheduled initiation of conduction in SCR's due to spurious signals, a situation that would cause short circuits in the system and lead to its ultimate destruction. These, however, are erroneous. It has been demonstrated that a controlled rectifier is capable of operating at frequencies comparable to those of power transistors and that it will not fire accidentally when its control circuits are properly designed and constructed.

The series inverter, unlike the parallel inverter, is indeed uncontrollable and load sensitive when operated at a fixed frequency. This difference of behavior is rooted in the network characteristics of these two classes of inverters. Looking into the transformer terminals of a parallel inverter, a resistive load R_L sees the source voltage $ae_s{}^*(t)$ which implies that the input voltage source $e_s(t)$ has been modified by a scaling factor a and has been inverted to a pulsating voltage waveform with a pulse duration ratio T_k/T_{ok}. The average value, V_o, of the output voltage v_o for each cycle of operation which starts at time t_k and ends at $t_k + T_{ok}$ is:

$$V_o = \frac{1}{T_{ok}} \int_{t_k}^{t_k+T_{ok}} v_o \, dt = \frac{a}{T_{ok}} \int_{t_k}^{t_k+T_k} e_s \, dt \qquad (1)$$

Hence, control of the dc output voltage can be obtained by varying the pulse duration ratio T_k/T_{ok}. The reflection of the modified source voltage e_s to the output terminals provides this network with its load-insensitive transfer characteristics.

Looking into the transformer terminals of a series inverter, the load R_L sees a power source, P, which depends on the input voltage source $e_s(t)$. The energy transferred to the load during each cycle of operation of this nonlinear RLC network is (under conditions of cyclic stability) equal to the difference of energy stored in the series capacitor $E_c(t_k)$ before, and $E_c(t_k + T_k)$ after, each cycle of operation (ref. 7).

The power P in the load R_L is given by

$$P = \frac{1}{2} \left[2e_s v_{c1}(t_k)\right] C_1 (2f_i) \tag{2}$$

where

$v_{c1}(t_k)$ = the voltage amplitude of oscillation of the series capacitors C_1

$C_1 = C_{11} + C_{12}$ (see Figure 2)

f_i = the inversion frequency

The amplitude $v_{c1}(t_k) = g(e_s, R_L)$ is a function of the input source voltage $e_s(t)$ and the load R_L in addition to other network parameters. The rms value of the output voltage of the series inverter V_{orms} is related to the power P by

$$V_{orms} = \left[2f_i e_s g(e_s, R_L) R_L C_1\right]^{1/2} \tag{3}$$

Relation (3) characterizes the lack of controllability, and the load sensitivity, of the common series inverter operated at a fixed frequency f_i, since V_{orms} is a function of e_s and R_L. Control is regained when the rate of transfer of energy from the source e_s to the load R_L is adjusted such that a constant output voltage V_{orms} is maintained. This is achieved by varying the frequency of inversion $f_i(k) = 1/2T_{ok}$ such that $V_{orms}(k) \approx V_{orms}(k+1) \approx V_o$ for any variations of e_s and R_L within design limits (ref. 8). Inverter operation, however, still suffers from a lower frequency limit of operation that is due to the cut-off frequency of the low-pass filter associated with the conversion process. The limit can be extended by changing the size of the series capacitor during operation, but it cannot be entirely overcome. Application of this type of inverter has been restricted because of its inability to operate from full-load to no-load while maintaining a prescribed output voltage. An improved series inverter-converter is presented in this report, which is free of this shortcoming and maintains a prescribed output voltage for any variation of e_s and R_L within design limits, including $R_L \to \infty$.

THE LOAD INSENSITIVE SERIES INVERTER-CONVERTER

The series capacitor inverter-converter can be viewed as a nonlinear LC oscillator coupled through a transformer-rectifier to a low-pass filter. The conventional second-order filter indicated in Figure 2 is reduced to a first-order network by removal of inductor L_o. The remaining capacitor C_o and the associated load R_L then become part of the resonant primary circuit under appropriate impedance transformation.

Capacitor C_o alone now constitutes the low pass output filter and has to be selected to assure that the maximum deviation 1/2 r_{pp} of the output voltage v_o from its average V_o will not be exceeded in between recharging cycles. A functional mechanism which adjusts the inverter frequency f_i to accomplish this is described later in this report. The intended functional philosophy that would transform dc potentials in a controllable and load-insensitive manner has thus been formulated.

Steady-state operation of the series inverter-converter circuit depicted in Figure 4 will be considered in this discussion of characteristics for small source voltage variations. For this case, the voltage amplitude $v_{C1}(t_k)$ will be related to the system input voltage e_s, the quality Q of the resonant circuits, the ratio of capacitors C_1 and C_o, and the average output voltage V_o which results from the degree of loading. It will be shown that a state of equilibrium can be reached for relatively small variations in the specific values of e_s, V_o, and the critical circuit parameters. Confinement of $v_{C1}(t_k)$ during transient conditions, such as systems start-up, is considered in the discussion of transient conditions. Finally in the discussion of characteristics for large-source voltage variations additional techniques will be introduced that permit wide variations of e_s and V_o as required for more general applicability of this inverter-converter.

Characteristics for Small-Source Voltage Variations

Steady-State Operation. - Operation of the network depicted in Figure 4 is discussed with reference to the associated characteristic voltage and current waveforms illustrated in Figure 5(a), (b), (c), and (d). The power switches of this converter operate

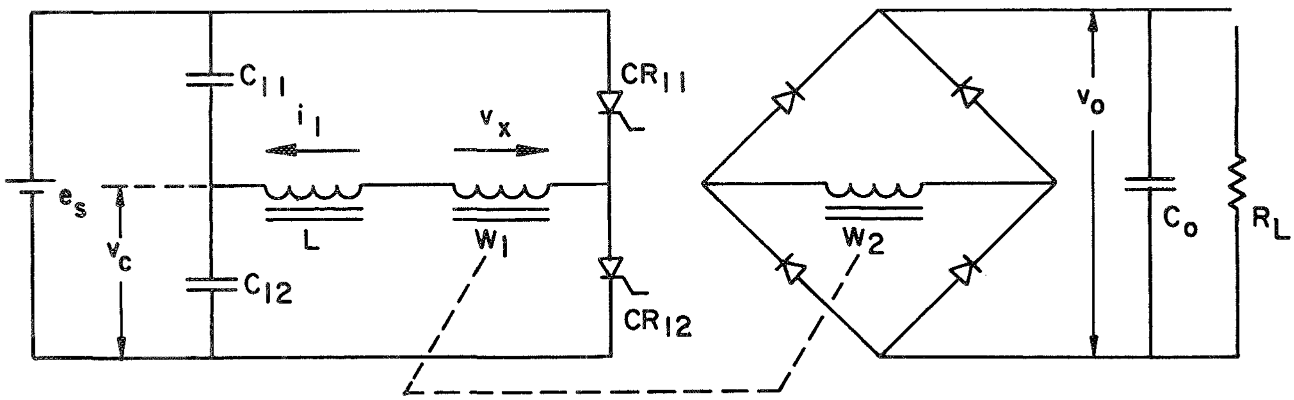

Figure 4.- Simplified schematic of the controllable, load-insensitive series capacitor converter

in a manner such that CR_{11} conducts during the interval $t_k<t<t_k+T_k$, while CR_{12} conducts during the interval $t_{k+1}<t<t_{k+1}+T_{k+1}$.

A rectangular voltage waveform v_x appears at the terminals of winding W_1 of the primary transformer and is depicted in Figure 5(b). The magnitude v_{xa} of this rectangular wave is given by

$$v_{xa} = V_o/a \text{ for } t_k<t<t_k+T_k \tag{4}$$

where V_o is the output voltage at the load terminals and $a = N_2/N_1$ is the turns ratio of the secondary (W_2) and the primary (W_1) windings of transformer X.

Similarly, the negative of this occurs during interval T_{k+1}. The primary transformer voltage v_x appears during each phase of switch conduction as a quasi-fixed potential v_{xa} which opposes the source voltage e_s, provided

$$\frac{1}{V_o} dv_o/dt \approx 0 \tag{5}$$

Consideration of this circuit can be simplified using Thevenin's equivalents for the source of electric energy and the two shunting capacitors C_{11} and C_{12} whereby e_s is transformed to $e_s' = e_s/2$ and the series capacitor $C_1 = 2C_{11}$, provided that for reasons of symmetry, $C_{11} = C_{12}$. Attention is now directed to one of the critical areas of this mechanism: to maintain the voltage amplitude $v_{c1}(t_k)$ of the high Q series resonant circuits within the limits imposed by its component characteristics, especially those of the semiconductor switching elements. Resistive damping is excluded, because it would impair the efficiency of operation.

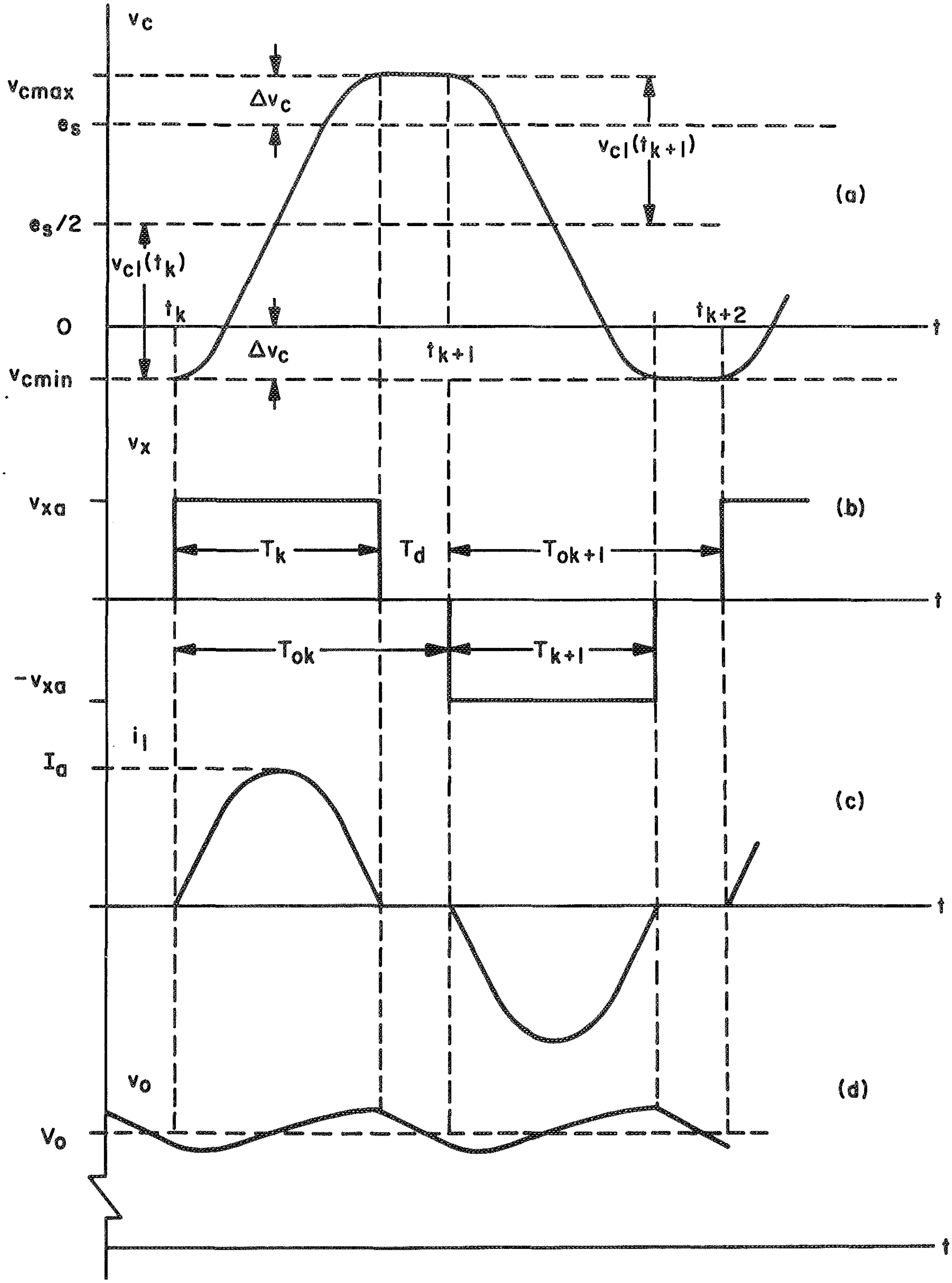

Figure 5.- Characteristic voltage and current waveforms of the load insensitive, controllable series capacitor converter

An equivalent circuit for each cycle of operation of the converter is shown in Figure 6. Capacitor C_2 represents the equivalent of filter capacitor C_o, of Figure 4, as reflected into the primary circuit;

that is

$$C_2 = (N_2/N_1)^2 C_o \tag{6}$$

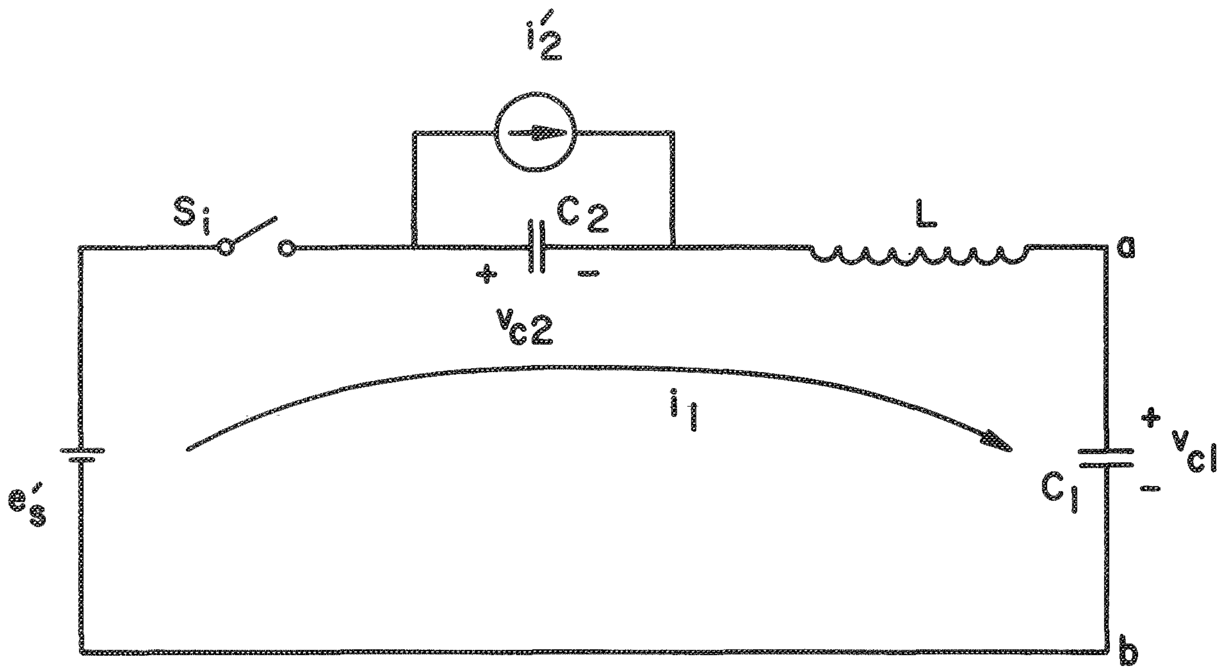

Figure 6.- Equivalent converter circuit during an individual cycle of operation

Current source i_2' represents the almost-constant load current V_o/R_L as reflected into the primary circuit. It is assumed that:

1. All components in the equivalent circuit of Figure 6 have ideal characteristics. (This assumption will subsequently be modified.)

2. Current i_2' counteracts the effects of current i_1 on capacitor C_2 in such a manner that it will return to the same potential $v_2 = v_x(t_k)$ before initiation of any current pulse.

3. Capacitor C_1 is turned around end-to-end between circuit terminals a and b after each current pulse, and before initiation of the succeeding pulse, such that under conditions of cyclic stability

$$v_{c1}(t_{k+1}) = -v_{c1}(t_k + T_k) \quad \text{and} \tag{7a}$$

$$v_{c1}(t_k) = -v_{c1}(t_{k+1} + T_{k+1}). \tag{7b}$$

Capacitor C_1 is initially charged to a potential $v_{c1}(t_k)$, a negative value. Switch S_i closes at time $t = t_k$ and for $t_k<t<t_k+T_k$ we have

$$e_s'(t) = L di_1/dt + v_{c1}(t_k) + v_2 + \frac{1}{C}\int_{t_k}^{t} i_1 \, dt \tag{8}$$

where $C = C_1C_2/(C_1 + C_2)$. Solving for the current yields

$$i_1(t) = I_a \sin \omega_o t \tag{9}$$

where

$$I_a = \Delta v\sqrt{C/L}$$

$$\Delta v = e_s' - v_{c1}(t_k) - v_2$$

$$\omega_o = 1/\sqrt{LC}$$

The output voltage variations, as illustrated in Figure 5(d), depend on the load R_L, the pulse repetition rate, and the size of capacitors C_1 and C_o.

The voltage $v_{c1}(t)$ across C_1 is

$$v_{c1}(t) = v_{c1}(t_k) + \frac{1}{C_1}\int_{t_k}^{t} i_1 \, dt \tag{10}$$

which at time $(t_k + T_k)$ becomes

$$v_{c1}(t_k + T_k) = v_{c1}(t_k) + \Delta v \frac{2C_2}{C_1 + C_2} \tag{11a}$$

where

$$T_k = \pi\sqrt{LC}$$

The behavior of a highly underdamped RLC circuit is briefly considered next. The series resistive element $R_S << \sqrt{L/C}$ is assumed to be sufficiently small to permit use of the relations governing lossless LC circuits except for a small but finite loss of energy during each half cycle of oscillation. With reference to Figure 6, capacitor C_1 is initially charged to potential $v_{c1}(t_k)$, a negative value, and switch S_i is open. It is assumed for now that $e_s' = 0$ and that C_2 is short-circuited. Switch S_i closes and a reversal of the voltage across C_1 is caused by the resonant current through L_1, C_1, and the short-circuited element C_2. Switch S_i opens immediately after polarity reversal of the voltage across C_1, and

$$v_{c1}(t_m + T_m) = -xv_{c1}(t_m) \tag{11b}$$

where $(1 - x) << 1$. The factor $(1 - x)$ is introduced as a measure of the loss of energy due to presence of the series resistance R_s. If one considers the voltage difference $2rv_{c1}$ across C_1 rather than the individual voltages before and after polarity reversal, then one can relate

$$2rv_{c1} = (1 + x)v_{c1} \tag{12}$$

where r is defined as the "loss factor." The energy $\mathcal{E}_R$ dissipated in resistance R_s during polarity reversal is equal to the ensuing loss of energy $\mathcal{E}_C$ in C_1 and can be expressed as

$$\mathcal{E}_R = \int_0^{\pi\sqrt{LC}} i^2 R_s \, dt + \tfrac{1}{2} v_{c1}^{\,2}(1 - x^2)C_1 = \mathcal{E}_C \tag{13}$$

The loss factor r of the capacitor voltage "swing" due to the presence of series resistance R_S can be obtained from relations (12) and (13) as

$$r \cong 1 - \pi/Q \tag{14}$$

provided that

$$Q = \frac{\omega_o L}{R} >> \pi \tag{15}$$

If the loss factor r is now introduced into relation (11a), which governs the behavior of the equivalent circuit, then this relation can be modified to

$$v_{c1}(t_k + T_k) = v_{c1}(t_k) + r\Delta v \frac{2C_2}{C_1 + C_2} \tag{16}$$

where r is associated with the actual voltage "swing" $\Delta v 2C_2/(C_1 + C_2)$ of capacitor C_1 in the presence of capacitor C_2.

Simultaneous solution of relations (7) and (16) for the k-th and (k+1)-th cycle yields:

$$v_{c1}(t_k + T_k) = \frac{1}{2}\frac{rC_2}{C_1 + C_2}\frac{e_s - 2v_2}{1 - r\dfrac{C_2}{C_1 + C_2}} \tag{17}$$

Under conditions of cyclic stability and the given assumptions

$$v_{c1}(t_{k+1} + T_{k+1}) = v_{c1}(t_k + T_k) \tag{18}$$

Removal of the hypothetical "turned around" capacitor C_1 (as stated under assumption 3) leads to the realization that in the actual circuit, shown in Figure 4, and the associated voltage waveforms in Figure 5, one has

$$v_{c1}(t_k) = -v_{c1}\left[t_k + 1\right] \tag{19}$$

Substitution of relation (14) into (17) yields

$$v_{c1}(t_k + T_k) = \frac{\dfrac{Q}{\pi} - 1}{\dfrac{Q}{\pi}\dfrac{C_1}{C_2} + 1}\left(\frac{e_s}{2} - v_2\right) \tag{20}$$

This can be reduced to

$$v_{c1}(t_k + T_k) \approx \frac{Q}{\pi}\left(\frac{e_s}{2} - v_2\right) \tag{21}$$

for $Q >> \pi$ and $QC_1/\pi C_2 << 1$, as is often found in practice.

Relation (21) is a convenient abbreviation of expression (20) and is useful for first-order approximations.

If $R_S \to 0$, then $Q \to \infty$ and $v_{c1}(t_k + T_k) \to (C_2/C_1)(e_s/2 - v_2)$ provided that i_2 continues to remove energy from capacitor C_2. Under conditions of cyclic stability, the maximum excursions of v_{c1} are confined in most practically realizable cases of interest.

Power Capacity and Efficiency

The power transfer capacity P of the system is expressed by relation (2). The highest physically possible frequency of operation f_{imax} is limited by the inequality

$$2f_i < \frac{1}{\pi\sqrt{LC} + T_{dmin}} = \frac{d}{\pi\sqrt{LC}} = 2df_o \qquad (22)$$

where

T_d = the time interval between pulses and T_{dmin} is the minimum time required for recovery of the electronic switches

d = the maximum "duty cycle" of switch operation or ratio of "on" time T_k to the duration T_{ok} of the cycle

f_o = the natural frequency of the equivalent resonant circuit as illustrated in Figure 6.

At relatively high efficiency of operation, the processed power $P \cong v_2{}^2/R_L'$, where R_L' is the load resistance as reflected into the primary circuit. The relative power loss in the system can be approximated by

$$1 - \eta = \rho^2 \frac{R_s}{R_L' + R_s} \qquad (23)$$

where

η = the efficiency of the system

ρ = the ratio i_{rms}/i_{av} between the rms and the average value of the converter current i_1 illustrated in Figure 5 (ref. 9).

The ratio

$$\rho = \frac{\pi}{2\sqrt{2}} \sqrt{1 + T_d/\pi\sqrt{LC}} \qquad (24)$$

is verified through inspection and interpretation of Figure 5(c). Relations (2), (14), and (21) through (24) were used to derive the efficiency

$$\eta \approx 1 - \frac{1}{4}\left(\frac{e_s}{2v_2} - 1\right) \frac{e_s}{2v_2} \qquad (25)$$

from

$$\frac{v_2}{R_L'} = 2v_{c1}(t_k)e_sC\, f_{imax} \tag{26}$$

with the restrictions that $R_s << R_L'$ and $Q >> \pi$.

The average primary load current is

$$I_{av} = \frac{P}{v_2 \eta d} \tag{27}$$

and its amplitude

$$I_a = \frac{\pi}{2d} I_{av} = \frac{1}{2\eta} \frac{\pi}{d^2} \frac{P}{v_2} \tag{28}$$

The system requirements of I_{av}, Δv and f_o allow selection of L and C from

$$I_a = \Delta v \sqrt{C/L} \tag{29}$$

and

$$\frac{1}{2f_o} = \pi \sqrt{LC} \tag{30}$$

Functional and Protective Features

A simple control system maintains a relatively constant output voltage v_o. The output signal hv_o of a resistive voltage divider shown in Figure 7, consisting of resistors R_a and R_b, is compared to the potential of the reference source voltage E_R. The difference between these two signals $(hv_o - E_R)$ is illustrated in Figure 8. The comparator emits a 1-0 signal depending upon whether $hv_o - E_R \gtrless 0$. This 1-0 signal is processed by a sequencer which directs it in alternating succession to the firing pulse generators 1 and 2. The firing pulses cause conduction of controlled rectifiers CR_{11} and CR_{12}, respectively. Each of the current pulses which are caused by conduction of the controlled rectifiers is terminated by resonant turn-off as the switch current becomes zero. Continuous converter operation and a minimum output voltage E_R/h is thus maintained. The output voltage, v_o, is bounded by the limits indicated by the inequality.

$$V_o - \frac{1}{2} r_{pp} \leq v_o \leq V_o + \frac{1}{2} r_{pp} \tag{31}$$

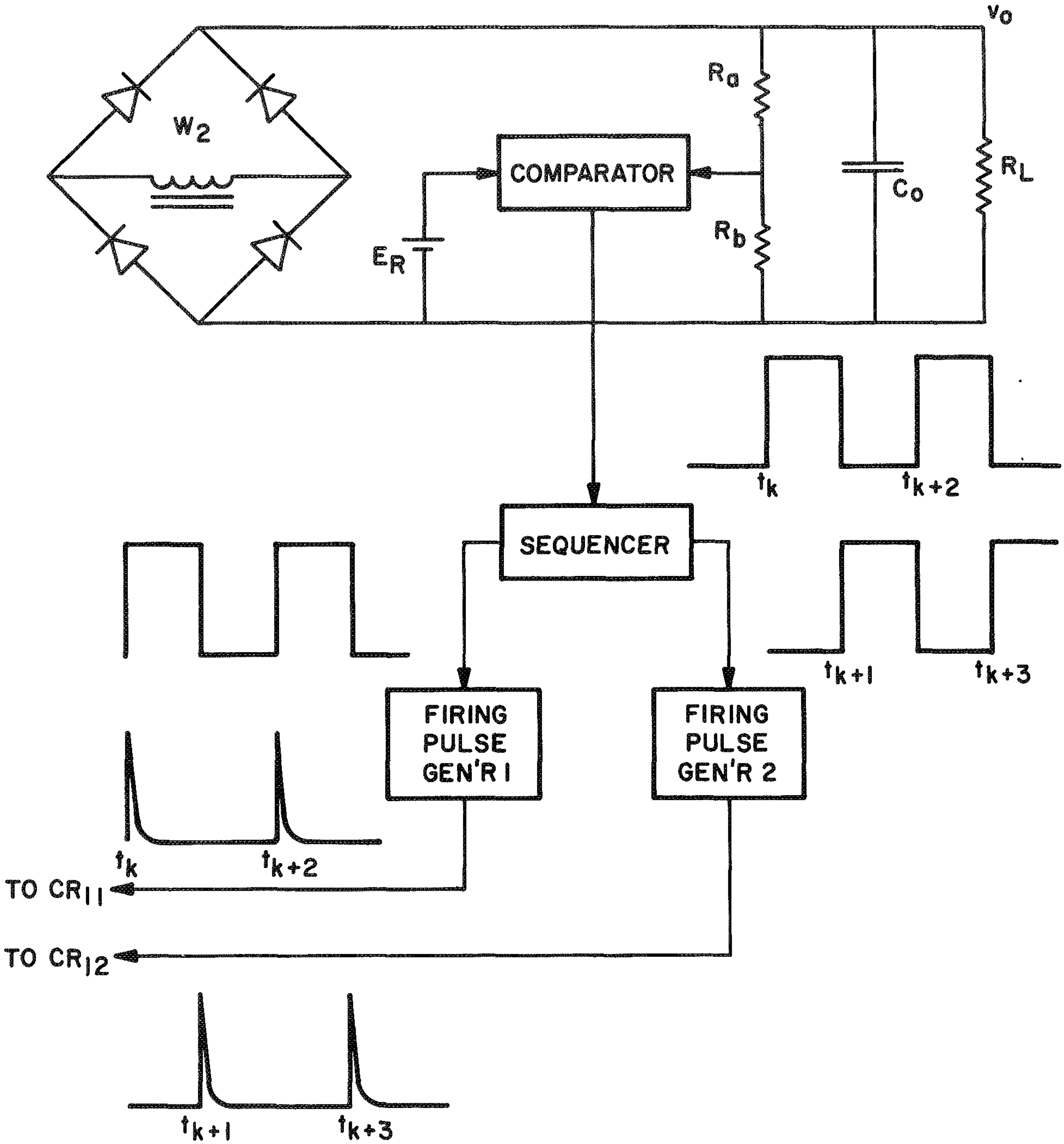

Figure 7.- Symbolic block diagram of converter control system

The maximum peak-to-peak voltage ripple of the output voltage follows from simple geometrical considerations and partial use of relation (11a). The magnitude of this voltage ripple at full load is

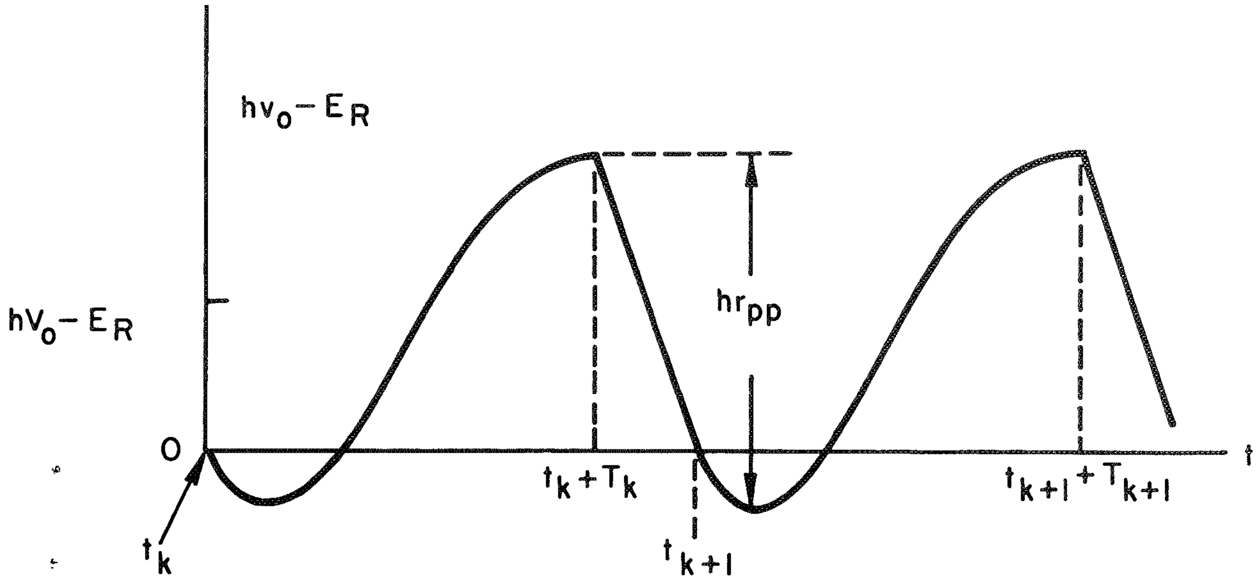

Figure 8.- Difference voltage waveform applied to comparator

$$r_{pp} = 2\ \Delta v\ \frac{C_1}{C_1 + C_2}\ \frac{V_o}{v_2}\ \frac{T_d}{\pi\sqrt{LC} + T_d} \qquad (32)$$

provided that $r_{pp} \ll V_o$. It is recalled that $C_2 = C_o(V_o/v_2)^2$, where V_o/v_2 is approximately equal to the turns ratio N_2/N_1 of the power transformer. The ripple, r_{pp}, then becomes a function of the output filter capacitor C_o, the load R_L, and the pulse repetition rate $2f_i$. The frequency of operation decreases linearly with decreasing load current. The output voltage ripple can increase in the limit to

$$r_{ppmax} = 2\ \Delta v\ \frac{C_1}{C_1 + C_2}\ \frac{V_o}{v_2} \qquad (33)$$

under zero load conditions.

Operation of series capacitor inverters with controlled rectifiers requires protective measures to prevent simultaneous conduction by both primary switches. This is accomplished by gating the firing pulses sent to the individual controlled rectifiers in a manner that will allow no firing pulse to reach its destination unless current flow in the companion controlled rectifier has ceased for at least a minimum length of time. This required additional time interval corresponds to the recovery time T_{dmin} of the controlled rectifiers.

Transient Conditions

The previously derived voltage excursions v_{C1} of capacitor C_1 are valid for steady-state operation. The uncharged capacitor C_o effectively short circuits the transformer during turn-on of the system. The voltage excursions, v_{C1}, across capacitor C_1 are therefore substantially larger during this transient phase. These potentials require considerable excess tolerance in the voltage ratings of the circuit elements used, especially those of the controlled rectifier switches. Measures that prevent occurrence of these voltage "overshoots" associated with system turn-on are discussed next.

Removal of electric energy from the series inductor L at a time when it is being transferred to the series capacitor C_1 will result in nondissipative damping of the resonant circuits. The degree of damping depends on the instant at which the removal of this driving force is initiated. Temporary return of the excess energies of inductor L to the source e_s during transient conditions, such as initiation of system operation, will be presented now.

The inductor L in the inverter circuit is equipped with two secondary windings W_{L21} and W_{L22} with opposing polarities, each connected through one diode to the voltage supply e_s. This is illustrated in Figure 9. The ratio of the N_{L1} primary turns and the N_{L2} turns of any of the secondary windings W_{L21} of inductor L is such that

$$\frac{N_{L1}}{N_{L2}} = \frac{v_{cmax} - e_s + v_2}{e_s} = \frac{v_{Lf}}{e_s} \tag{34}$$

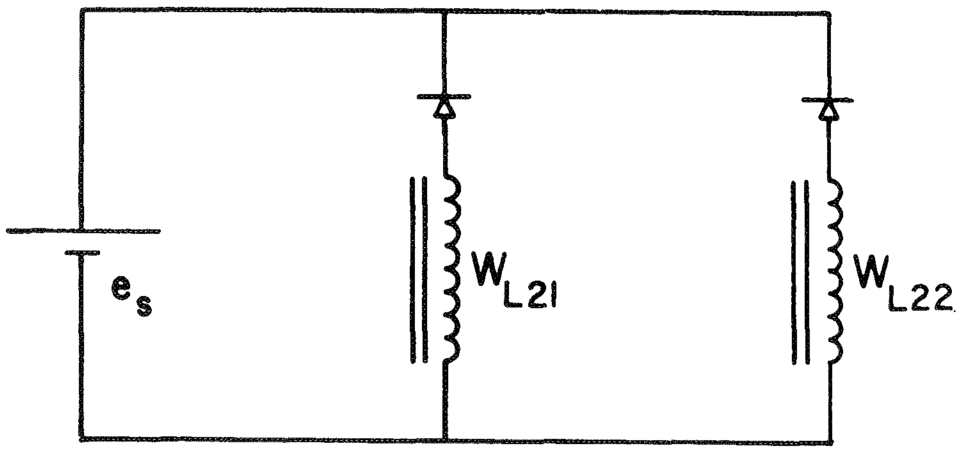

Figure 9.- Secondary inductor circuit of series capacitor converter for energy transfer

The significant voltage and current waveforms associated with this circuit are discussed with reference to Figure 10. The maximum excursions of the capacitor voltage v_c are bounded by clamping the secondary inductor winding to the source voltage e_s, as expressed by relation (34), at a time when v_c is tending to exceed the prescribed values v_{cmax} or v_{cmin}.

The quasi-sinusoidal steady-state voltage waveform with amplitude Δv_{Lss} across L is indicated by the dashed curves in Figure 10(a). The full-wave rectifier bridge associated with the secondary inductor winding W_{L2} remains non-functional when the secondary inductor voltage $v_{L2}<e_s$. When $v_{L2}\geq e_s$, then the rectifier bridge clamps v_{L2} to e_s and the corresponding primary inductor potential v_{L1} to a fixed voltage level Δv_{max}. The ensuing voltage waveform v_{L1} is indicated by the solid curves in Figure 10(a). The voltage waveform v_{L1} is "arrested" at time T_a in the cycle. The capacitor voltage v_c is therefore clamped to v_{cmax} at that time. The clamping of the capacitor voltage is due to the fact that the only source of electric energy which causes a change in v_c after $v_c>e_s$ or $v_c<0$, respectively, is the energy stored in inductor L. Current i_1 indicated in Figure 4 is thus terminated, since $C_1 dv_c/dt = 0$, and controlled rectifier CR_{11} will open. This current i_1 is identical to the inductor current i_L shown in Figure 10(b) for $t_k<t<t_k + T_a$. For $t_k + T_a<t<t_{k+1}$, $i_1 = 0$. The magnetic energy remaining in inductor L is discharged into the voltage source e_s.

If $de_s/dt \cong 0$, then for each cycle

$$i_{L2}(t) = \begin{cases} 0 \text{ for } t_k<t<t_k + T_a \\ \\ \dfrac{\Delta v_{max}}{e_s}\, i_{L1}\,(t_k + T_a) - \dfrac{e_s t}{L_2} \text{ for } t>t_k + T_a \text{ and } i_{L2}>0 \end{cases} \qquad (35)$$

$+ T_a$ and $i_{L2}>0$

where i_{L2} = secondary inductor current

L_2 = inductor value as viewed from its secondary winding terminals

The secondary inductor current is indicated as i'_{L2} when reflected into the primary circuit, and $i_{L2}>0$ for all times. The voltage waveform v_c is shown in Figure 10(c) and illustrates the objective of this non-dissipative damping technique. The series capacitor voltage "swing" is limited to $2v_{c1max}$, with v_{cmax} as its

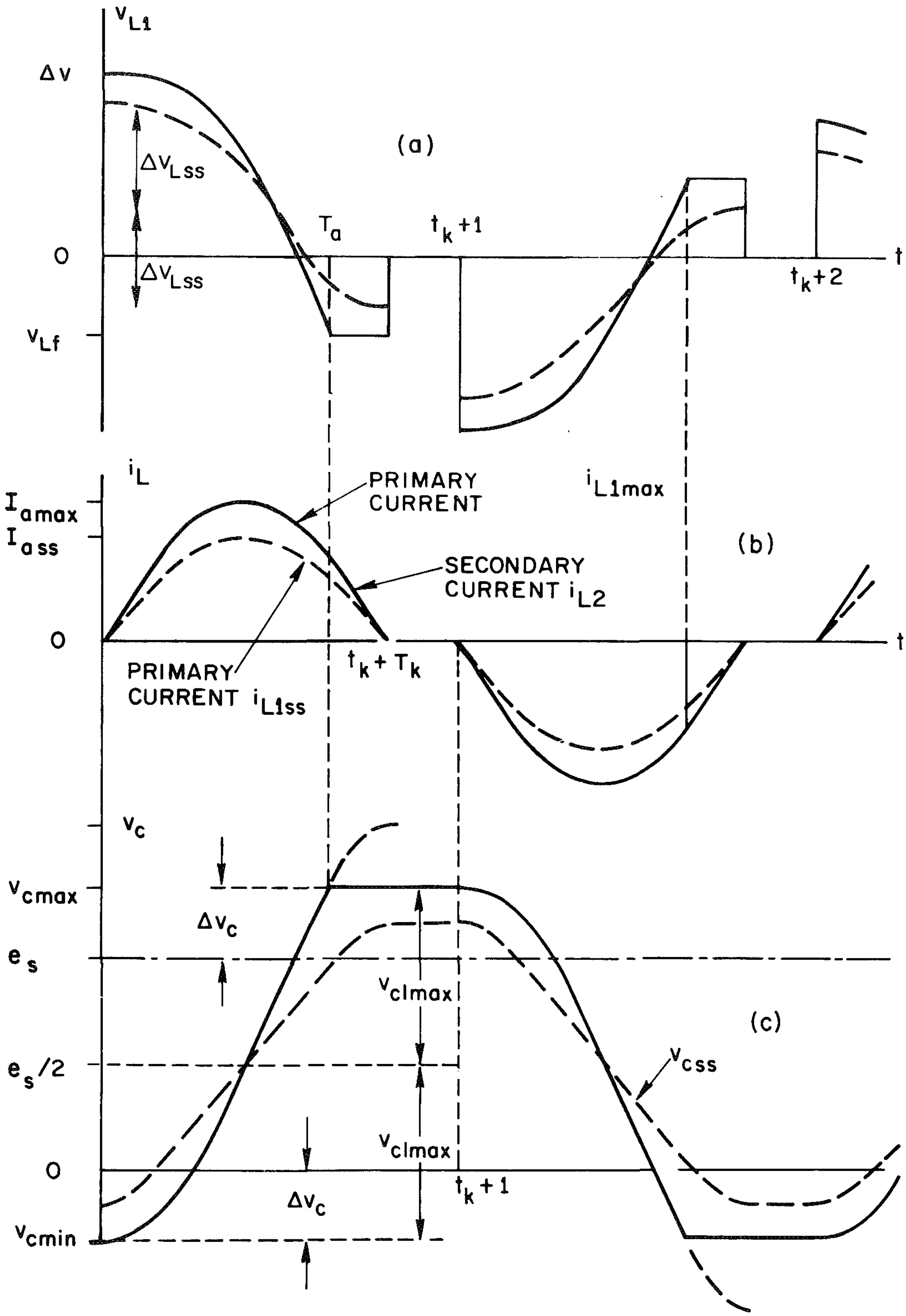

Figure 10.- Voltage and current waveforms associated with inductive energy transfer

upper limit and v_{cmin} as its lower limit. These limits are dictated by the maximum ratings of components, especially those of the semiconductor switching devices. The dashed curve in Figure 10(c) indicates the capacitor voltage waveform under steady-state operating conditions, when the secondary inductor winding remains inoperative and primary circuit operation is not affected by the presence of winding W_{L2}. An excessive overshoot Δv_c of the capacitor voltage during turn-on conditions is thus prevented by clipping this voltage at preset levels. The system "ignores" this imposed limitation during steady-state operation, as intended.

Characteristics for Large Source Voltage Variations

The clipping technique discussed previously under Transient Conditions could also be used to accommodate variations of the source voltage e_s or intended load voltage variations, and prevent occurrence of a steady-state voltage amplitude $v_{c1}(t_k)$ (as stated by relation (21)) that would exceed the component limitations. Such an approach appears valid, but would lead to a reduction of the system efficiency since heat would be generated by sizable currents during the return of energy from the inductor to the supply source rather than during the transfer of energy to the load. The variation in efficiency would be reflected by variations of the current ratio ρ as defined by relation (23).

However, a similar technique can be used to transfer excess energy from the series inductor to the load and thus avoid degradation of the efficiency. Inductors L_{11} and L_{12} are connected in series with the controlled rectifiers CR_{11} and CR_{12} as shown in Figure 11. The secondary windings W_{L21} and W_{L22} of each of the inductors are connected to the secondary diodes S_{21} and S_{22}. These switches are back-biased during the first half of the individual resonant half cycles. This is consistent with the relative polarity of the windings as indicated by the dots. Diode S_{2i} will conduct during portions of the second half of each individual resonant interval whenever

$$v_{L1i} \frac{N_{L2i}}{N_{L1i}} > v_o \tag{36}$$

where N_{Lji} = number of turns in the respective inductor windings
V_{L1i} = inductor primary voltage

The time T_{ao} at which conduction in the secondary inductor windings is established is determined by the relation

$$T_{ao} = \sqrt{LC}\left\{\pi - \text{arc cos } \frac{v_o}{v_{Lt}} \frac{N_{L1i}}{N_{L2i}}\right\} \tag{37}$$

for

$$\frac{\pi}{2}\sqrt{LC} < T_{ao} < \pi\sqrt{LC}$$

where $v_{Lt}=v_2(t_k)-e_s/2-v_{cl2t}(t_k)$,and $v_{cl2t}(t_k)$ is defined by relation (49). The voltage $\Delta v = e_s/2 - v_2(t_k) - v_{cl}(t_k)$ is variable under transient conditions, such as turn-on, since the load voltage as reflected into the primary circuit $v_2(t_k)$ varies from cycle-to-cycle starting from zero to its steady-state value v_2. The cut-in time T_{ao} of the secondary inductor circuits varies accordingly, but the absolute maximum excursions of the capacitor voltages, v_{cmax} and v_{cmin}, remain bounded until the output v_o approaches its intended level and thereafter. The turns ratio N_{L2i}/N_{L1i} can be, again, chosen in such a manner that inequality of Eq. (36) is not satisfied during conditions of cyclic stability, in order that the inductive energy transfer remain only effective during transient conditions of operation. The method just discussed, however, is suited for steady-state operation.

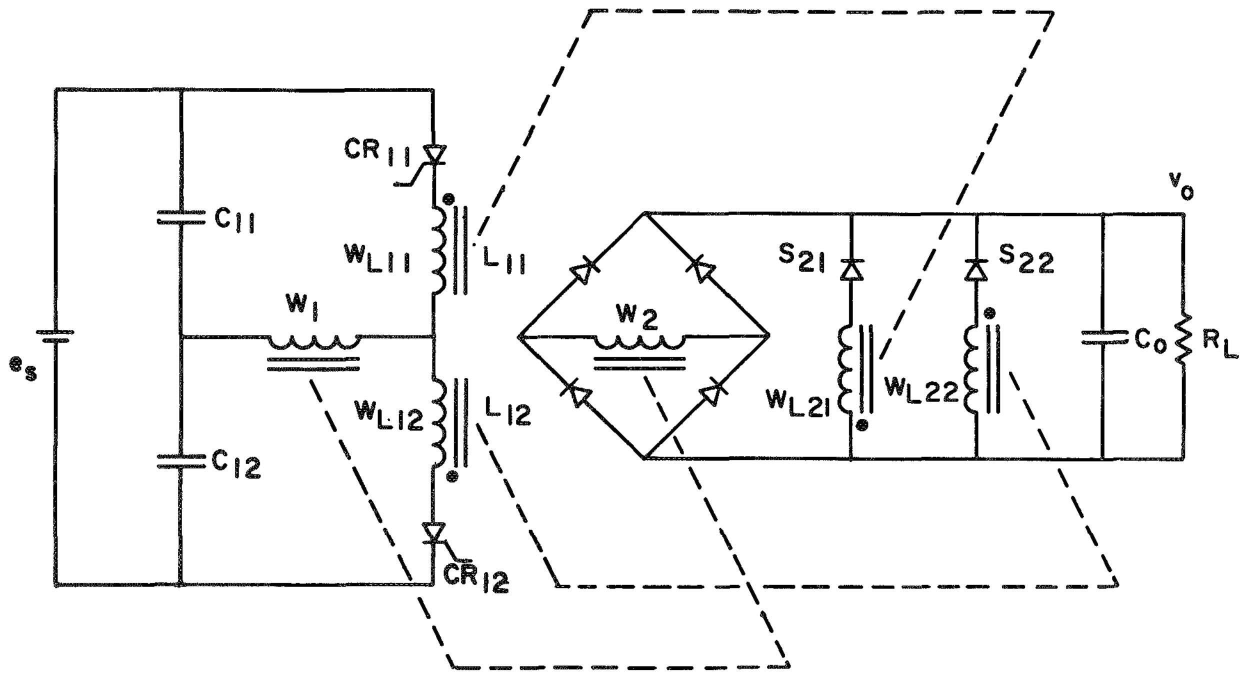

Figure 11.- Simplified schematic of the controllable, load-insensitive, series capacitor inverter-converter with inductive energy transfer to the load

Another degree of freedom may be added to this technique by addition of a controlling function to the switching elements S_{2i} connected to the secondary inductor windings. This can be implemented by using controlled rectifiers which are then provided with appropriate gate-firing signals.

The cut-in time $T_a(k)$ now becomes a variable and can be chosen arbitrarily provided that

$$T_{ao} \leq T_a(k) \leq \pi\sqrt{LC} \tag{38}$$

This technique can be used to reduce the swing of the capacitor voltage v_{c1} as expressed by relations (20) and (21) to any value, as long as the desired value is such that

$$v_{c1}(t_k + T_k) \leq \frac{Q}{\pi}\left[e_s/2 - v_2\right] \tag{39}$$

A significant cause of excessive capacitor voltage build-up is a variation of the source voltage e_s. The quality factor Q of the circuit should be relatively high in order to provide the system with an acceptable efficiency. The product (Q/π) $(e_s/2 - v_2)$ will vary by the multiple Q/π of any variation of the relatively small difference $e_s/2 - v_2$ where both e_s and v_2 have usually large values.

If the voltage source e_s were to vary by a significant amount, then the system will cease operation when $e_s/2 \leq v_2$ as noted by inspection of Figure 6. The capacitor voltage v_c may exceed a safe maximum v_{cmax} if $e_s/2$ were to substantially exceed v_2 as indicated by relations (20) and (21). The method for capacitor swing-limitation discussed with reference to Figure 11 not only prevents an excessive voltage v_c, but also permits system operation with an approximately constant current amplitude I_a, even though the voltage e_s of the source may increase substantially. Maintenance of an approximately constant current ratio ρ, as defined by relation (23), for a given load and for a widely varying e_s offers unparalleled advantage of approximately constant efficiency for a wide range of source voltages. This unique property is discussed with reference to Figure 12.

The capacitor voltage waveform v_c is shown for a voltage source e_{s1} and for a voltage source $e_{s2} = be_{s1}$, where $b>1$. The objective of this technique is to assure that the difference voltage Δv, defined by relation (10) remains constant for any value of $e_{s1} \leq e_s \leq e_{s2}$ such that the current amplitude I_a remains invariant. The difference voltage Δv associated with each of these two source voltages is designated with an index (Δv_i) for purposes of distinction. This designation indicates the desire that

$$\Delta v_1 = e_{s1}/2 - v_{c11}(t_k) - v_2 = e_{s2}/2 - v_{c12}(t_k) - v_2 = \Delta v_2 \tag{40}$$

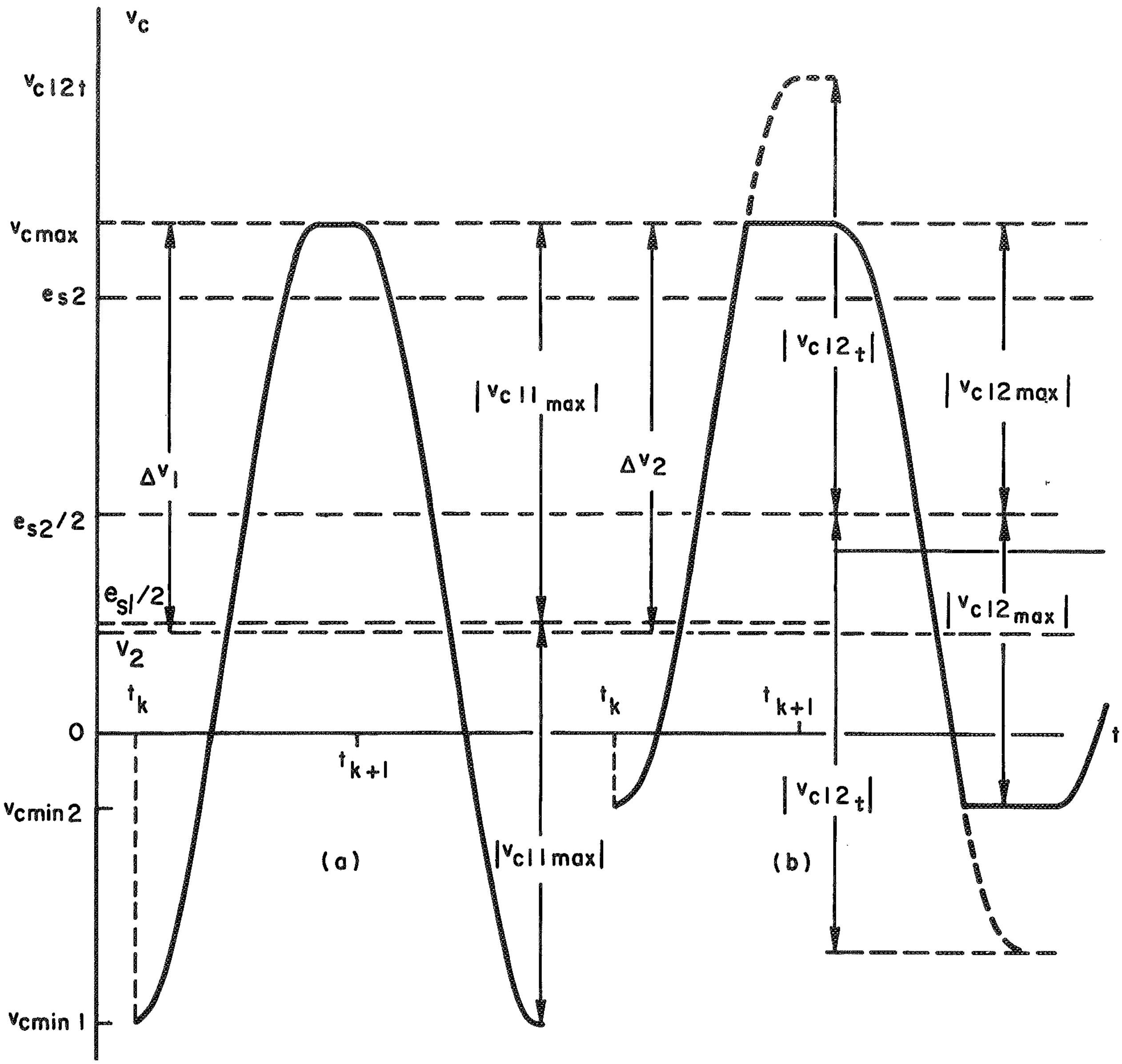

Figure 12.- Voltage waveform v_c of the series capacitor for (a) source e_{s1} and (b) source voltage e_{s2}

where the capacitor voltage amplitudes $v_{c1i}(t_k)$ also appears with distinct indices. It becomes immediately evident that Δv_i will remain unchanged if

$$e_{s1}/2 - v_{c11}(t_k) = e_{s2}/2 - v_{c12}(t_k) \tag{41}$$

It is recalled here that $v_{c1i}(t_k)$ and v_{c1imax} are negative values as defined by relations (7a) and (7b). The relationship between the v_{c1i} is here established by rearrangement of (41).

$$v_{c12}(t_k) = \frac{e_{s1}}{2}(b - 1) + v_{c11}(t_k) \qquad (42)$$

It is necessary that

$$v_{c12}(t_k) > be_{s1}/2 \qquad (43)$$

to secure unfailing turn-off of the controlled rectifiers, and that $be_{s1}/2 - v_{c12}(t_k)$ be smaller than the safe operating voltage of the switching components.

This technique can be implemented by the circuit shown in Figure 11. This circuit will cut-in whenever the secondary inductor voltage v_{L2} tends to exceed the load voltage and thus

$$\frac{v_{L1}}{V_o} = \frac{v_{Lf}}{v_o} = \frac{N_{L1}}{N_{L2}} \qquad (44)$$

consistent with relation (34). The initial inductor voltage Δv_i is invariant for an invariant output voltage v_o, since the inductor winding turns ratio is fixed. Hence, the objective of this technique is attained. The steady-state value $v_{c12s}(t_k + T_k)$ to which the non-restricted capacitor voltage amplitude v_{c12} associated with the source voltage e_{s2} would tend is given by

$$v_{c12s}(t_k + T_k) = v_{c11}(t_k + T_k)\,\frac{be_{s1} - 2v_2}{e_{s1} - 2v_2} \qquad (45)$$

where $v_{c11}(t_k + T_k)$ is the "arrested" capacitor voltage amplitude. It will, however, start each time with the same value $\Delta v_1 = \Delta v_2$, whichever of the sources e_{s1} or e_{s2} may power the circuit. To what extent the voltage amplitude v_{c1i} will tend to increase will depend on the time constant of the resonant circuit. The time constant of the exponential term of an RLC circuit is given by

$$\alpha = \frac{R}{2L} = \frac{\pi}{2QT_o} \qquad (46)$$

The change in amplitude will attain 63% of its final value when $\alpha t_1 = 1$. This will occur when $t_1 = NT_o$ where N is the number of intervening converter cycles. Thus number, N, is found from the relation

$$\frac{\pi}{2QT_o} NT_o = 1 \qquad (47)$$

as

$$N = 2Q/\pi \tag{48}$$

The target value $v_{c12t}(t_k)$ of each cycle of the capacitor voltage amplitude is then

$$v_{c12t}(t_k) = v_{c11}(t_k) \left\{ 1 + \frac{\pi}{2Q} \frac{\frac{e_{s1}}{2v_2}(b - 1)}{\frac{e_{s1}}{2v_2} - 1} \right\} \tag{49}$$

This is obtained by using straight-line approximation for the incipient portion of the exponential term and using relation (42). The "target path" of the overshoot of v_c is indicated in Figure 12(b) by a dashed curve. The rms value of the converter current associated with the transfer of energy from the source to the load will remain approximately constant, even though part of it will flow through the secondary inductor winding.

This method requires two inductors, each equipped with one secondary winding. A certain weight penalty could be imposed on the system since two inductors are required, each with one secondary winding, and each possibly involving high-voltage insulation.

This difficulty is circumvented by employing the main power transformer as the energy transfer and voltage level transforming element. This is accomplished by adding controlled rectifiers CR_{13} and CR_{14} to yield the circuit shown in Figure 13. This circuit operates in a similar manner to the one discussed with reference to Figure 4, except for operation of controlled rectifiers CR_{13} and CR_{14}. Inductor L is in series with the power transformer X. The voltage waveform seen by the inductor is the same as the one shown in Figure 10(a) for $t_k < t < t_k + T_a$. The inductor current is the same as depicted in Figure 10(b) for the same time interval, and so is the capacitor voltage v_c shown in Figure 10(c). At time $t = t_k + T_a$, controlled rectifier CR_{13} is fired. It will clamp the voltage v_c to the cathode of controlled rectifier CR_{11} and thus turn off CR_{11}, since its anode current is reduced to zero. However, the inductor L remains connected across the transformer X. Current i_1 will continue to flow governed by the relation

$$i_1(t) = i_1(t_k + T_a) - \frac{v_2}{L} t \qquad (50)$$

for $t_k + T_a < t$, $i_1 > 0$

This current is stepped up or down by transformer X and thus transferred to the load. No additional power loss is involved through the addition of the two new controlled rectifiers since the primary current falls only through one semiconductor voltage drop at one time, as before. The firing signals for CR_{13} and CR_{14} can be derived from a secondary signal level winding on inductor L operating against some constant reference voltage, or from an appropriate control circuit which emits a signal when v_L reaches v_{Lf} or when v_c attains v_{cmax} or v_{cmin}.

The effect of this last technique is exactly the same as that previously discussed with reference to Figures 11 and 12, that is, it secures a safe start-up of the system with confined excursions of the voltage waveform v_C and approximately constant efficiency for a given load and for variations of the source voltage e_s.

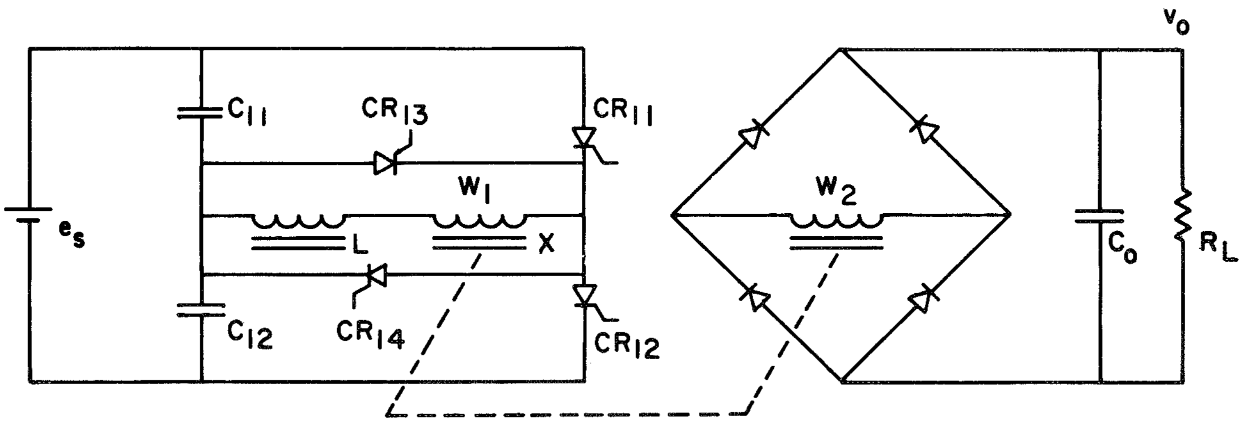

Figure 13. - Alternative simplified schematic of a controllable and load insensitive series capacitor dc converter with transfer of inductive energy to the load

APPLICATIONS

The previous discussion of the series inverter-converter was limited to its application for scaling and stabilization of the voltage of a source of dc power. The basic network can be applied to perform other functions; in many cases, this requires application of conventional engineering techniques to a new electronic system, rather than the generation of circuit concepts with novel functional philosophies. Several such systems are briefly outlined in the following. They constitute, however, only an arbitrary sample of potential applications.

Voltage Stabilizing dc Transformer

This application was used for the presentation of this network; further information is contained under Experimental Results.

Secondary Sources of Pulsating Power

The dc transformer can supply pulsating power to certain loads such as radar or laser systems. The output capacitor C_o is charged by the load between individual pulse demands to a preset voltage V_o. A sensor detects the flow of current into the load during each of its work cycles, and sends a signal to the control mechanism of the converter which prevents its operation until the load current has subsided. Subsequently, the converter resumes operation and recharges its output capacitor C_o and is then ready for the next work cycle. Capacitor C_o is in this case part of the pulse-forming network. The advantages of this system are: (1) its high efficiency, since a resonant impedance rather than a resistive element is used to limit the capacitor charging current, or (2) the elimination of the bulky dc filter associated with the efficient supply of power for pulsating loads.

Controlled Three-Phase ac to dc Conversion

The power derived from a source of conventional three-phase ac power is first processed by a full-wave-rectifier bridge and then by the controllable dc transformer. The load receives dc power with stabilized voltage, or current, or energy per unit of time, as required. This process is indicated by the block diagram shown in Figure 14. The system performs the functions of (1) conversion of three-phase ac to dc power, (2) voltage scaling, (3) voltage, current, or power stabilization, and (4) rejection of the ac ripple $r(t)$ contained in the rectified voltage waveform $e_s(t)$ by an active filtering process. The advantages of this process consist in the elimination of the conventional needs for (a) a low-frequency transformer to scale $e_s(t)$ and (b) the low pass filter for rejection of the ac content of $e_s(t)$, where both (a) and (b) constitute the main cause of bulk, weight and cost of conventional ac-to-dc conversion equipment.

An Amplifier of Unipolar Signals

Substitution of a time-varying signal $e_r(t)>0$ for the fixed-voltage reference signal E_R discussed with Figure 7 results in a time-varying output voltage $v_o(t)$. If the load impedance Z_L, the capacitor C_o, and the inversion frequency band are appropriately

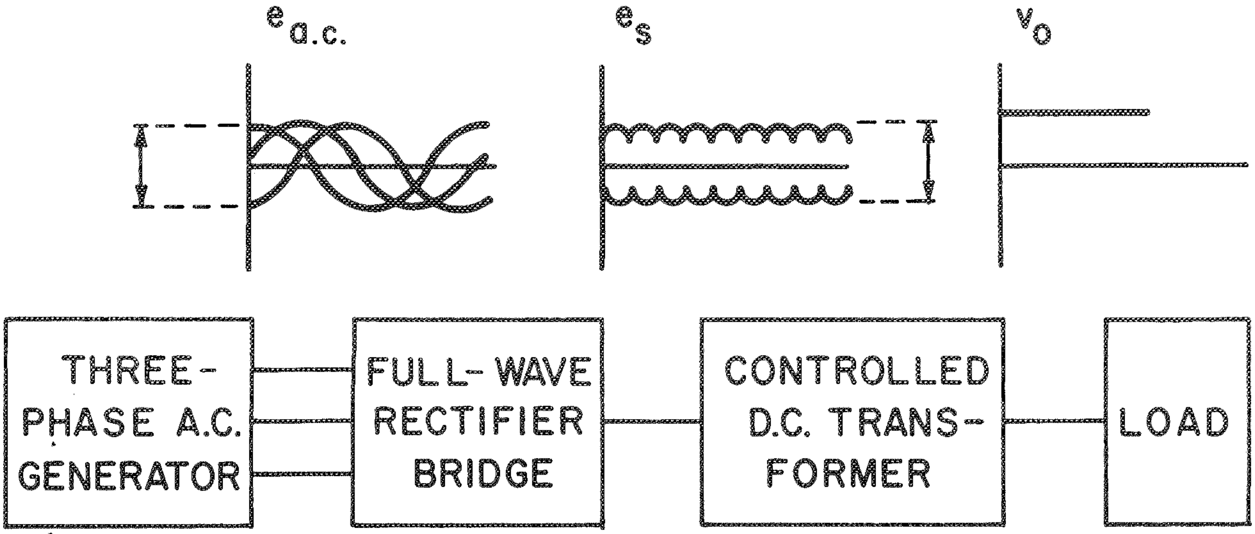

Figure 14.- Controlled three-phase ac-to-dc converter

chosen, then $v_o(t) \simeq he_r(t)$ independent of the variations of $e_s(t)$. No attempt for analysis was made, as being beyond the scope of this report; the underlying philosophy is found in the literature (ref. 7).

Amplifiers of Bipolar Signals

Logical extension of the amplifier of unipolar signals leads to the amplifier of bipolar signals. The uncontrolled switching elements in the rectifier circuit shown in Figure 4 are replaced by controlled unilateral switches, such as controlled rectifiers; the secondary winding W_2 of the power transformer is, furthermore, split into two secondary windings W_{21} and W_{22} as shown in Figure 15. A bipolar signal $e_r(t) \gtrless 0$ is compared to the output voltage $v_o(t)$ instead of the previously unipolar signal and then processed to transform $e_s(t)$ accordingly. The comparator discussed with reference to Figure 7 is designed to energize the sequencer whenever for equal polarity of e_r and v_o for a preset margin

$$|hv_o| < |e_r|$$

The further aspects of this type of operation appear self-explanatory. The classical example of such an amplifier is the inversion of dc-to-ac power with sinusoidal voltage waveform.

Operation of Several Loads

The discussed group of networks can power several loads simultaneously as is customary with related types of networks such as the parallel inverter-converter. The case where the voltage v_{o1}

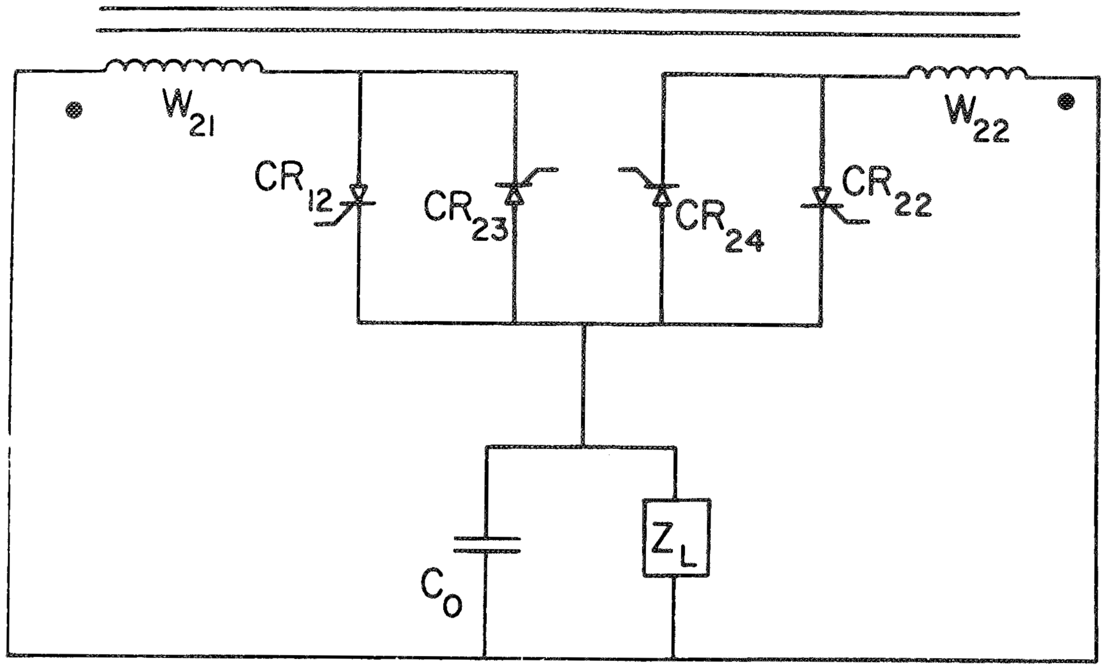

Figure 15.- Output network for amplifier of bipolar signals

of one of two dc loads is closely controlled and the voltage of V_{o2} of the other load is "slaved" to it is discussed first with reference to Figure 16. Shown are two center-tapped secondary windings of the power transformer which power loads R_{L1} and R_{L2} via the corresponding pairs of switches S_{21i} and S_{22i}, respectively.

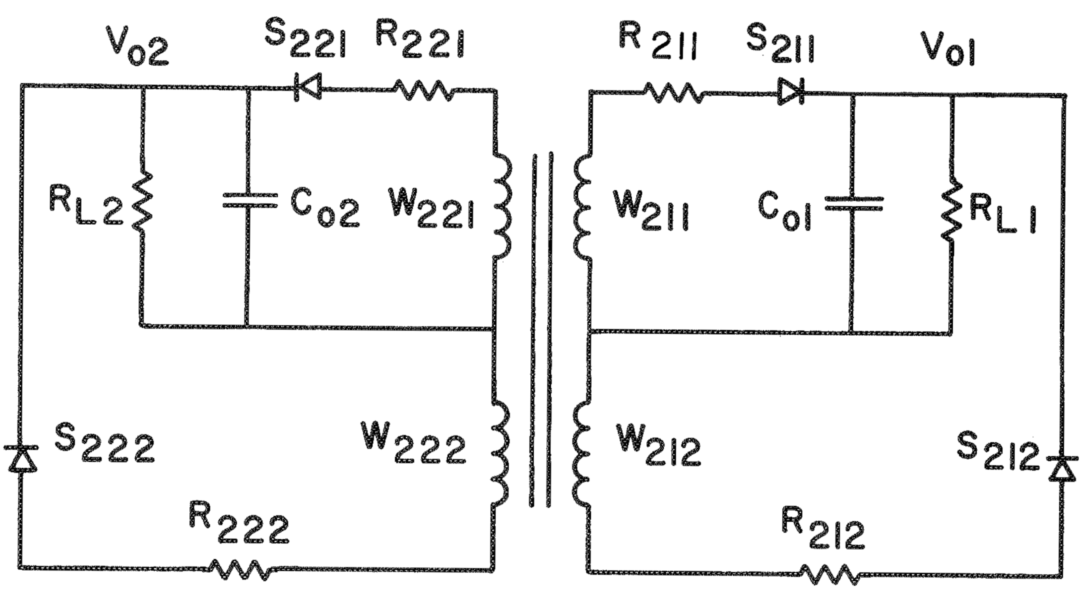

Figure 16.- Parallel loads R_{L1} and R_{L2} of one series inverter-converter

Assume that the output voltage v_{o1} indicated in Figure 16 is controlled by an electronic mechanism as discussed with reference to Figure 7. A predetermined average output voltage v_{o1} is maintained at load R_{L1} independent of the loading caused by R_{L2}, provided that the maximum energy transfer capacity of the primary converter circuit is not exceeded. This behavior is rooted in the functional philosophy of the control mechanism which will call for another pulse (supply of energy) independent of the nature of causes that led to the condition $hv_{o1} \leq E_R$. If the unilateral uncontrollable switches (ref. 7) S_{21j} were ideal and all $R_{2ij} = 0$, then v_{o2} is related to v_{o1} by the turns ratio $N_{21}/N_{22} = k_{o2}$ of the windings W_{22i} and W_{21i} such that $k_{o2}v_{o2} \cong v_{o1}$. Capacitor C_{o2} looks through switches S_{22i} and S_{21i} onto capacitor C_{o1} as reflected into the circuit of R_{L2}, that is, whenever these switches are closed. If $k_{o2}v_{o2} > v_{o1}$, then switch S_{22i} opens (the diode is back-biased) and current flow toward load R_{L2} is interrupted. Conversely, if $hk_{o2}v_{o2} = hv_{o1} < E_R$, then the control mechanisms associated with load R_{Li} calls for another pulse, even though the deficiency of v_{o1} was actually caused by load R_{L2}. The voltage v_{o2} of load R_{L2} is thus slaved to the voltage v_{o1}. Furthermore, if $R_{L2}k_{o2}^2 = R_{L2}' = R_{L1}$ and if concurrently $C_{o2}/k_{o2}^2 = C_{o2}' = C_{o1}$, then switches S_{21i} and S_{22i} conduct the respective load current during concurrent and equal time intervals. This is symbolically indicated in Figure 17(a). If, however, $R_{L2}' \neq R_{L1}$ and/or $C_{o2}' \neq C_{o1}$, then the load current associated with the smaller load, for example, R_{L2}, will flow during shorter time intervals than its companion load current, because $v_{o2} = v_{o1}$. This is indicated in Figure 17(b). The uncontrolled unilateral switches S_{22i} thus perform concurrently and automatically the functions of rectification and pulse width modulation without application of any mechanism to control the circuit elements associated with load R_{L2}.

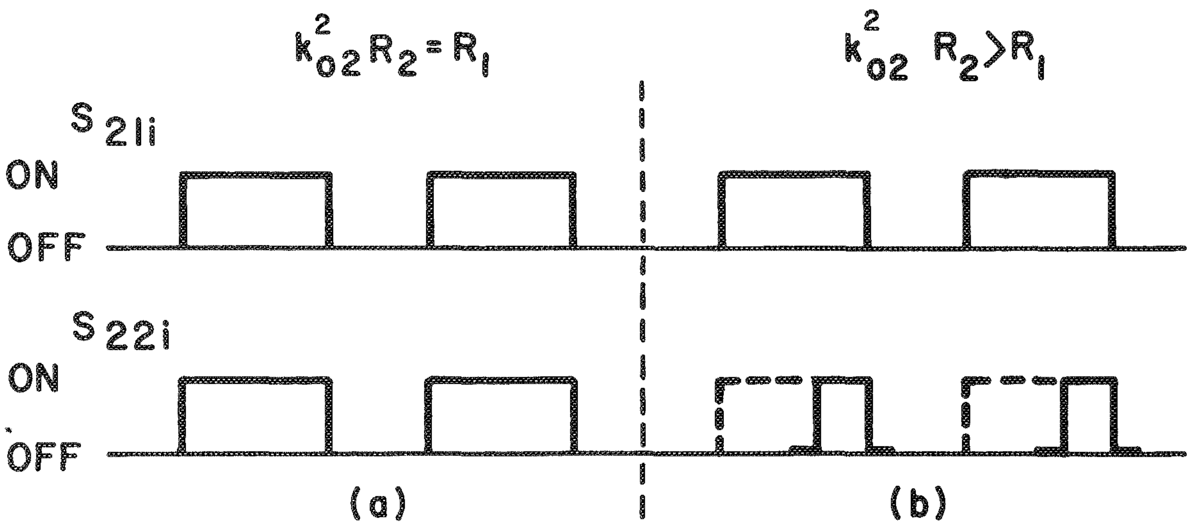

Figure 17.- Symbolic illustration of current condition in switches S_{2ij}

Reintroduction of the intrinsic voltage drop in the switching elements S_{2ij} and of the cumulative circuit series resistance R_{2ij}, illustrated in Figure 16, indicates that the voltage v_{o2} will deviate from its nominal value $k_{o2}v_{o2} = v_{o1}$ within certain limits. These limits are determined in conventional manner by the circuit parameter values and the conditions of operation of the common primary circuit of the series inverter. Closer tracking of the individual load voltages is attained when the output voltage of each of the two load circuits is monitored individually by a separate comparator circuit of the type illustrated in Figure 7. The load voltage dividers are divided such that $h_1v_{o1} = h_2v_{o2}$ and $h_2/h_1 = k_{o2}$. The output signal of the two comparators operate into one common OR gate which in turn energizes the sequencer. The control circuit operates otherwise exactly as discussed with reference to Figure 7; this is illustrated in Figure 18. The case of different potentials of the reference nodes of R_{L1} and R_{L2} requires, of course, two reference sources E_{R1} and E_{R2} and appropriate signal flow to the OR gate.

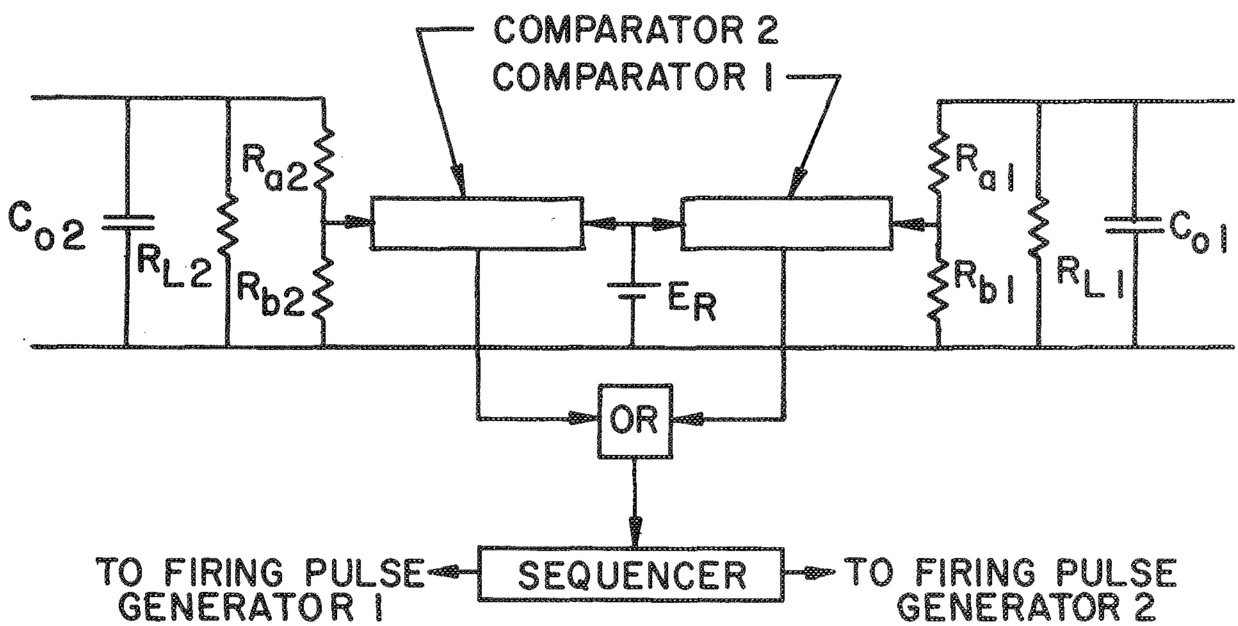

Figure 18.- Converter control system for two loads

Completely independent control of two loads is attained when switches S_{2ij} are controllable, such as implemented by controlled rectifiers, and independent phase angle control is applied during each of the resonant periods. The control mechanism can be implemented for this purpose by application of any of the known electronic circuit techniques.

Parallel operation of more than two loads follows from an extension of the indicated methods or modified techniques that implement the present functional philosophies. Parallel operation of two or more loads for amplification of unipolar or bipolar signals is implemented by appropriate extension and application of the functional philosophies that were presented to maintain several stabilized dc output voltages of one converter. Known control mechanisms, other than the type discussed with reference to Figures 7 and 18, can be applied for the purpose of control of voltage, current, or average power.

General Comments

Only a relatively small number of circuits and system configurations was presented for purpose of discussion of the underlying principles. The methods applied for removal of excess energy from the series inductor(s) were not included in the previous discussions to simplify and amplify the presentation of the significant aspects of the discussed techniques. Their application is, however, tacitly assumed, wherever needed. Known control mechanisms, other than the type discussed with reference to Figures 7 and 18, can be applied for the purpose of control of voltage, current, or average power.

Many other configurations appear possible that could reduce to equivalent circuits which incorporate the functional philosophies presented in this report. They can be summarized in simple language. These configurations would show transfer of energy in discrete quantities via resonant circuits, from a source of electrical energy to the load which is shunted by a capacitor. The load, in turn, is part of the resonant circuit. The configuration would show control of this transfer of energy such that the load voltage, or current, or power waveform becomes a scaled replica of a control signal $s_r(t)$. The configurations would show how excess energy that would cause a build-up of excessive potentials in the high Q circuit is recurrently removed from the series inductor(s) and returned to the source of electrical energy, or better, transferred to the load.

EXPERIMENTAL RESULTS

Several series capacitor inverter-converters of the type discussed previously were constructed including one experimental model to provide the beam power for an ion propulsion engine of a spacecraft. The power derived from a 300-volt dc source was transformed to 2-kV at a beam current of 1 ampere. This transformation was achieved with an efficiency of over 95% and an internal operating frequency of 10 kHz at the 2-kW power level. The power components of this model weigh approximately 4 kg. This converter is provided with a progressive overload mechanism which interrupts system operation at the occurrence of overloads and short circuit

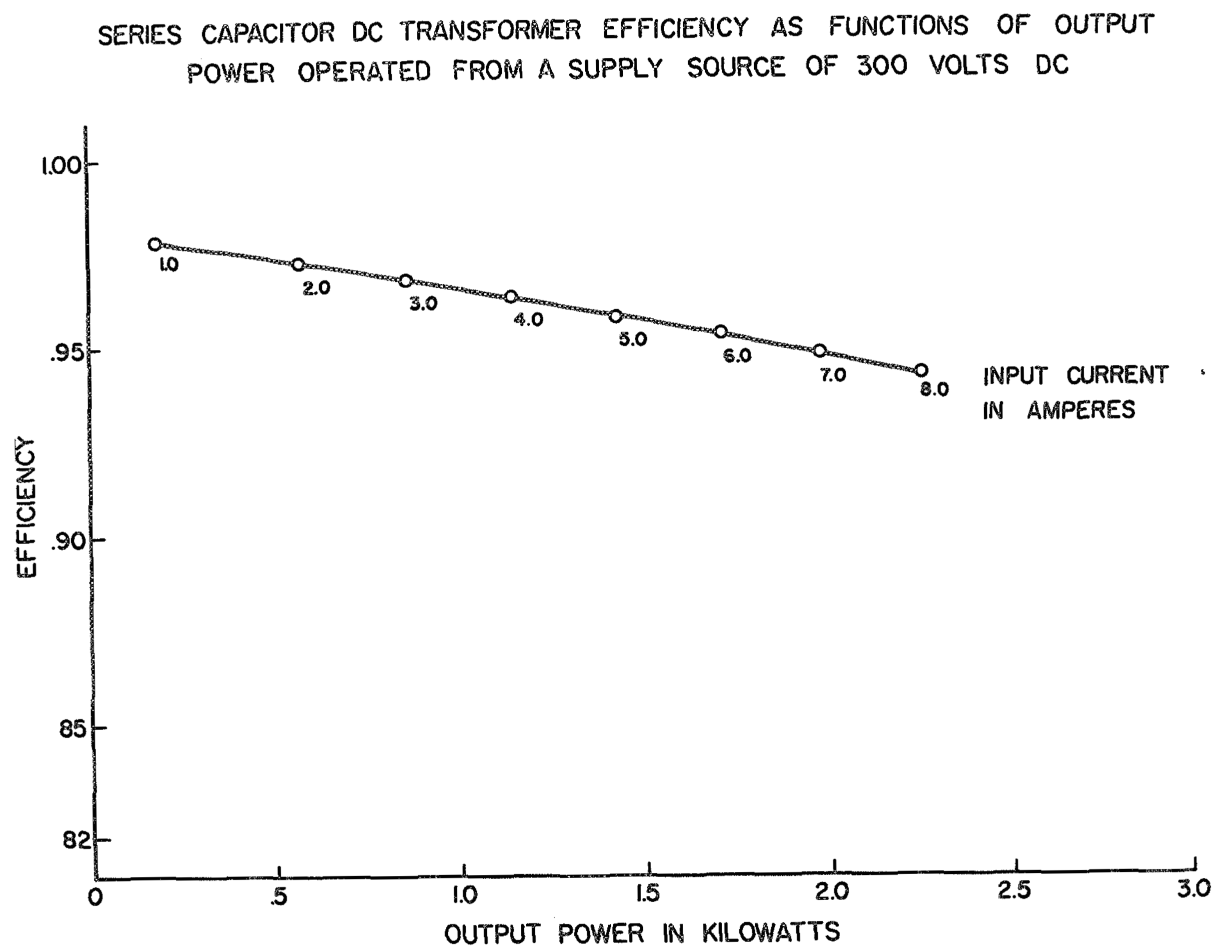

Figure 19.- Efficiency of series capacitor inverter-converter

currents of up to 10^3 times the magnitude of their steady-state value. The output voltage was maintained within 1% of its intended level. This model was integrated with an ion engine for spacecraft propulsion. During extensive tests, it withstood the rigors imposed by recurring arcing inside the engine. No stability problems were observed. Test data on the efficiency of power conversion are shown in Figure 19.

CONCLUSIONS

Principles of operation and the technology of a controllable, load-insensitive dc transformer in the form of a series capacitor inverter-converter have been formulated and established. The functional philosophy of its network is adapted to the characteristics of current switching operation at high power frequencies in excess of 10 kHz, in order to impose only moderate stresses on the switches and the other circuit elements. Application of these principles led to the attainment of efficiencies of power transformation in excess of 95% since no significant penalties were imposed by the utilization of high power frequencies for purposes of minimization of physical weight and size of apparatus. The time $(T_d)_{min}$ between cessation of current flow in a controlled rectifier and the recovery of its capacity to block the flow of forward current presently limits the frequency of efficient operation of the dc transformer to about 10 kHz.

Construction of flight equipment with power densities of 0.4 kW/kg can be implemented with currently available silicon-controlled rectifiers having a recovery time of 10 μsec. It is expected that the power density capability will be increased to 1 kW/kg with equal efficiency, when silicon-controlled rectifiers having a recovery time of 2 μsec, currently under development, become available. In addition, this should extend internal frequencies of operation to approximately 50 kHz. Further reduction of the recovery time of controlled rectifiers could be expected in the light of past progress in semiconductor technology. However, other limitations in the way of yet higher frequencies may have to be overcome before miniaturization of efficient electric power conversion apparatus may become feasible.

The network described in this report performs voltage scaling and stabilization in one single operation. The first-order low-pass filter secures unconditional stability. The zero frequency component of the output impedance "seen" by the load is approximately zero, since the system operates on the principle of a simple regulator. Even in an adverse thermal environment the output voltage can be maintained within close limits, such as 0.1%, by application of electronic volt-seconds integration processes which incorporate autocompensatory techniques against variation of component characteristics due to variation of their operating temperature.

Automatic termination of current conduction of the controlled rectifier by the resonant circuit in this network appears essential to fail-safe operation of controlled rectifiers in dc-driven networks; dc transformers with ratings of tens of kilowatts and operated from power sources at conventional voltage levels appear feasible with currently available circuit components.

Availability of an efficient multikilowatt dc transformer could influence the choice of electric power distribution systems that have thus far relied almost entirely on the conventional ac transformer for voltage scaling. The power circuit of the dc transformer is relatively simple. The effects of the complexity of the electronic control system appears currently acceptable for applications in which physical weight and size are at a high premium; moreover, its effects can be greatly reduced by application of large-scale microcircuit integration. The relatively small quantities of material needed for this type of transformer and its high efficiency could eventually lead to dc distribution systems that are more attractive than the ac distribution systems presently employed.

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