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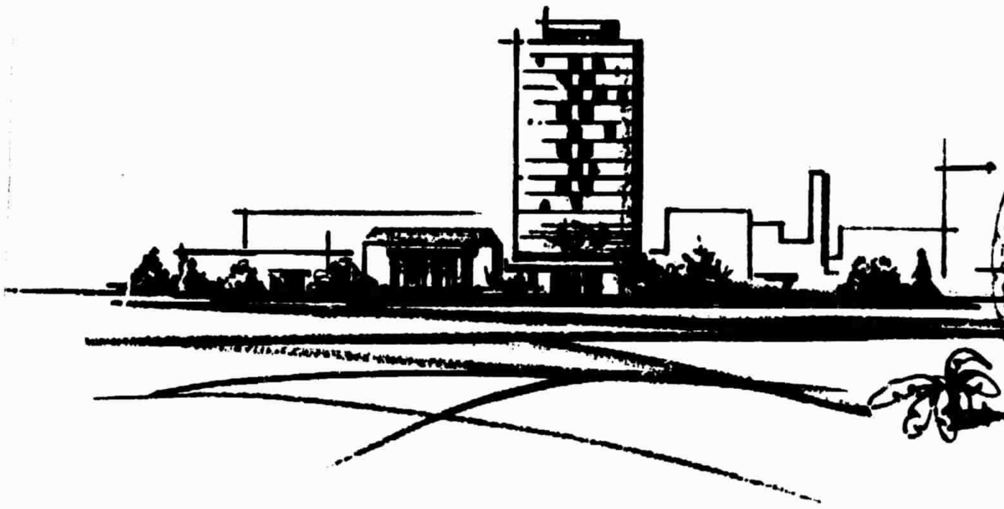

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FINAL REPORT

on

MICROCIRCUIT CONSTRUCTION ANALYSIS

to

GEORGE C. MARSHALL SPACE FLIGHT CENTER
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

February 27, 1970

by

D. A. Kaiser, R. E. Staub, and L. H. Stember

Contract No. NAS8-25103
June 27, 1969, to February 27, 1970

BATTELLE MEMORIAL INSTITUTE
Columbus Laboratories
505 King Avenue
Columbus, Ohio 43201

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INTRODUCTION

The advent of microcircuits has raised new obstacles for the personnel who must assess the reliability and assure the continued operation of electronic equipment. In conventional circuitry, the materials, fabrication processes, and workmanship could usually be conveniently inspected. These factors are now largely concealed within a miniature hermetically sealed package. The implication here is not that intentionally defective materials or workmanship is being concealed, but rather that it is a very difficult task to mass produce circuits of the complexity and dimensions that present day microcircuits represent without quality defects and inherent reliability problems escaping visual and electrical inspection. One approach to ascertaining the quality of fabrication techniques and personal workmanship is an objective construction analysis on a sample of circuits from the particular manufacturer in question.

Battelle conducted a detailed inspection of 20 sample circuits from two manufacturers using current techniques and equipment. This work was performed under Contract NAS8-25103 during the period June 27, 1969 to February 27, 1970.

SUMMARY

Twenty microcircuits, five specimens each of four circuit types from two manufacturers, were subjected to a construction analysis. The microcircuits were visually inspected externally; uncapped, visually inspected internally according to applicable paragraphs of MIL-STD-883 Method 2010; and photographed in color. All specimens were then subjected to a deep-field inspection in the scanning electron microscope. Various aspects of the specimens were inspected and measured using interferometry. Selected specimens were potted and metallographically sectioned for further investigations.

The program was oriented toward determining defects in fabrication processes and personal workmanship which have potential for affecting the long-term performance of the devices. The results of these studies showed that none of the circuit types was completely free of potential failure mechanisms. Microcircuits from Manufacturer A showed a high incidence of cracking and necking in the internal lead wires immediately above the ball bonds. These same circuits also exhibited induced defects in the thin-film interconnections on the surface of the silicon chip.

Microcircuits from Manufacturer B showed good workmanship in the interconnection and packaging of the integrated chip but had serious defects in the metallization at oxide steps where physical contact is made to the electrical regions of the silicon device.

OBJECTIVES

The purpose of this program was to perform a construction analysis on four types of silicon microcircuits and to document the construction analysis procedure used. The objectives were to:

(1) Determine metallization variances and manufacturing imperfections which have potential to cause device failure

(2) Comparatively evaluate aluminum and molybdenum-gold metallization systems.

DISCUSSION

This research program was performed to determine the quality of construction in similar types of microcircuits from two different manufacturers. Techniques and equipment similar to those employed in the failure analysis of microcircuits were used for this purpose. However, the microcircuits investigated in this construction analysis were all new. Except for the electrical measurements and screening tests conducted at the manufacturing plant and possible incoming inspection tests at NASA, the microcircuits had not been subjected to electrical or environmental stresses. Accordingly, no preliminary electrical tests were performed in this program.

Microcircuit Specimens

Twenty-three digital microcircuits of four different types were furnished to Battelle for the construction analysis. These specimens were all of the transistor-transistor logic (TTL) family but represented alternative fabrication methods and materials. The pertinent details of the microcircuit specimens are given in Table 1, Specimen Identification and Description, which lists the device family, logic function and complexity, package type and lid seal, chip-bond process, lead material, lead-bonding method, and metallization system.

Five devices from each of the four sample groups were arbitrarily selected as program specimens before the packages were uncapped. The sixth device in each of the first three groups was used as a control specimen.

Program Plan

The approach used in this construction analysis program was a step-by-step inspection of each specimen starting with the package exterior and working inward to the heart of the device, the silicon chip. The microcircuit packaging and intraconnection processes were inspected and evaluated for the quality of lead and lid seals on the external package, inclusion of foreign material within the package, chip orientation and bond quality, orientation and condition of the internal lead wires, bond quality and placement at both ends of the internal leads, and induced damage in the metal film conductors on the silicon die. The metallization system was further inspected for alignment on the die, photolithographic defects, corrosion, intermetallic compound formation at lead-to-metallization interfaces, and contact window defects.

Internal Visual Inspection

Visual inspection was performed at various magnifications from 45X to 500X using stereo microscopes and vertical illumination. Identified and suspected defect areas were noted and documented during the visual inspection, and color photomicrographs were made. The documented information for each speciman is

TABLE 1. SPECIMEN IDENTIFICATION AND DESCRIPTION

Specimens	Mfg. Code	Circuit Type	Lot Number	Device Family	Logic Function and Complexity	JEDEC Package	Lid Seal	Chip Bond	Internal Leads	Pad Bond	Post Bond	Metallization System	Notes
11 to 16	A	SN5451	541A	TTL	Dual 4-input NAND Gate	TO-84	Weld	Glass frit	Gold	T.C. Ball bond	Wedge	Single layer, Aluminum	10mw/gate
21 to 26	A	SN54L51	6805A	LPTTL	Dual 4-input/ 6-input NAND Gate	TO-84	Weld	Glass frit	Gold	T.C. Ball bond	Wedge	Two layer, Molybdenum-Gold	Low-power, 1mw/gate
31 to 36	B	SN54L78T	6941	LPTTL	Dual J-K Flip-Flop with R&S	TO-86	Solder	Gold eutectic	Aluminum	Ultrasonic	Ultrasonic	Single layer, Aluminum	Low-power
41 to 45	B	SN54L73T	6941	LPTTL	Dual J-K Flip-Flop with R only	TO-86	Solder	Gold eutectic	Aluminum	Ultrasonic	Ultrasonic	Single layer, Aluminum	Low-power

included in a separate Internal Visual Inspection (IVI) report (twenty of which are included in Appendix A) which lists in detail the type, location and severity of the observed defects. This information is summarized in the following section. To identify the defect location on the die, an imaginary grid was superimposed on the die topography. This grid uses letter identification on the abscissa and numerals on the ordinate. An example reference guide for each sample type, which also includes the internal lead numbers, is located with the IVI reports in Appendix A. These should be used to identify and locate the defects, lead numbers, ball-bond numbers, pad numbers, etc., referenced in the Defect Identification and Enumeration section of this report.

Scanning Electron Microscope

All specimens were then subjected to deep-field inspection in the scanning electron microscope (SEM) at magnifications from 50X to 10,000X in either secondary electron mode (SE) or back-scattered electron mode (BSE) as warranted by the subject of interest. Scanning micrographs were made as needed to illustrate and document the SEM findings. These also are used as Figures in the following sections.

Interferometry and Metallography

Selected specimens were submitted to interferometry for determination of metallization thickness and thickness variations. The information from this inspection step is found in Appendix B. These same specimens plus two control specimens were then metallographically cross sectioned and inspected optically and in the scanning electron microscope for deficiencies in the chip-to-package bond, for the presence of intermetallics at the lead-bond interface, and for the quality of bond at the metallization-oxide interface. Appendix C contains the detailed results of the metallographic studies.

DEFECT IDENTIFICATION AND ENUMERATION

The principal criteria used in identifying defects in the microcircuits was the MIL-STD-883, Method 2010. Where this specification was inadequate, published literature dealing with the fabrication processes of interest, past experience with similar circuits, and engineering evaluation were employed. The results of the Construction Analysis program are presented concisely in Table 2, "Summary of Defect Incidence in the Microcircuits". Table 2 is organized to show the total number of each type of defect that was found in each specimen. The column headings across the top of the table include only those inspection points where a defect was identified. Inspection points at which no defects were observed are not included in the headings. The specimen numbers are listed down the left side of the table. General headings show manufacturer and circuit type. Total defects are indicated by the numbers at the line-column intersections. Appropriate comments instead of numbers are found under the column headings of Corrosion and Window Problems since defects at either of these inspection points are usually general conditions instead of isolated incidences. Where comment instead of, or in addition to, a defect count was appropriate, footnotes were used.

The data in Table 2 were compiled from the information in the three Appendices, from visual observation of the scanning-electron-microscope presentations, and from study of the color photomicrographs and the scanning micrographs. While Table 2 is very useful in determining at a glance where the major problems were found, it does not suffice as the only accounting of defects. A more detailed discussion of the findings for each circuit type together with figures that illustrate the defects is given in the following three sections.

TABLE 2. SUMMARY OF DEFECT INCIDENCE IN THE MICROCIRCUITS

	Foreign Matter Within Package					Internal Head Wires					Post Bond		Pad Bond		Metallization				
Specimen	Loose	Attached	Chip Bond	Die Condition	Foreign Matter on Die	Looping	Cracking	Necking	2-mil Clearance	0.5-mil Perpendicular	Size	Placement	Rebond	Placement	Scratch or Void	Corrosion	Bridge	Alignment	Window Problems
									Manufacturer A, Type SN5451										
11		(a)	1				13	3		7		1		1	2				
12		(a)	1	(b)	4		14	2		2	5			3	2		4		
13		(a)	1	(c)		3	7	2		4	3			7	3		1		
14		(a)	1	(d)		2	10			2				8	5				Cracks
15	1		1				12	9		12	3		2	3					
									Manufacturer A, Type SN54L51										
21	1				1	2	3 (e)								2	Some			
22			1				2 (e)	1						3	2				
23							1 (e)								1	Some			
24				(f)	1		2 (e)	1					1	1		Some			
25			1	(g)		3	1 (e)								1				
									Manufacturer B, Type SN54L78										
31																			
32														3	1				
33																			Porosity
34					1										1				Possible Cracks
35														1					Cracks
									Manufacturer B, Type SN54L73										
41	1			(h)	1				2						1				Cracks
42									3						1				Cracks and tunneling
43									3										Cracks and tunneling
44									3								1		Cracks, etchpits and scratch
45									3										Cracks

(a) Unplated center area of package floor appeared to be corroded but scale was firmly attached.
(b) Crack in die, starting from edge and leading toward active circuit area.
(c) Two cracks in die across total width.
(d) One crack in die across total width. Die surface was spherical (convex).
(e) Remaining ball bonds showed less severe cracks in wire-to-ball transition region.
(f) Die surface speckled with gold flecks from incomplete metallization removal.
(g) Same as (f) but less extensive.
(h) Die showed color changes from one end to other probably due to oxide thickness variations.

Type SN5451 Gates
(Manufacturer A, Specimens 11 to 15

General

The specimens in this group were housed in the TO-84 package having a metal lid and bottom, welded lid-seal and glass lead-seals. The chips were bonded to the package floor by a nonmetallic bonding agent that appeared to be glass frit. Aluminum metallization, approximately 1.6 microns thick was used as the interconnect system on the die. Internal wiring consisted of flying gold leads, thermal compression ball-bonded to expanded pads at the periphery of the die, and wedge bonded to the posts or lands of the external leads.

Package Exterior

All packages were considered to be satisfactory with the following exceptions: one package (Specimen 15), exhibited a short section of lid weld-seam which did not appear to be thoroughly melted, two packages (Specimens 13 and 15) had several glass seals that each appeared to have shallow cracks, and two packages (Specimens 11 and 15) had the leads grossly offset in the lead slots almost to the point of touching the metal walls.

Package Interior

None of the packages included loose foreign material. Two specimens each had one attached foreign particle, neither of which was located in an area that could cause electrical problems.

The amount of bonding agent under the chip varied considerably from package to package, but only one specimen had an excessive amount. In all specimens, the bonding agent showed cracks and crazing that extended the depth and breadth of the fillet on all sides of the die. In approximately half of the specimens, the bonding-agent surface was rough and the material was opaque. In the specimens that were cross sectioned, the bond under the die was laced with small bubbles and contained some larger voids as well. (Figure C-2 in Appendix C.)

The orientation of the die with respect to the package leads was satisfactory for all specimens. However, the die installation was indiscriminant as to centering and tilt. In particular, the thickness of the bonding agent under the die was found to vary considerably from one edge to the other for the same die and from one package to another.

Die Condition

Three specimens were found to have cracked dies. The cracks are believed to have occurred during specimen marking. In Specimen 12, two cracks were seen leading from the die edge near Pad 3 into the die (see Figure 1). One of these was oriented parallel with and very near the die edge; the other crack led toward the active circuit area and disappeared under a bonding pad. In Specimen 13, two cracks were observed, both of which traversed the entire width of the die cutting through many active-circuit regions (Figure 2). Specimen 14 had one such crack across the die. The surface of Specimen 14 was found to be slightly domed with a center-to-edge relief of about 1 micron. Figure B-5 in Appendix B is an interference photomicrograph that illustrates the domed nature of this die. Specimen 14, when subsequently cross sectioned, also showed a noticeable curve

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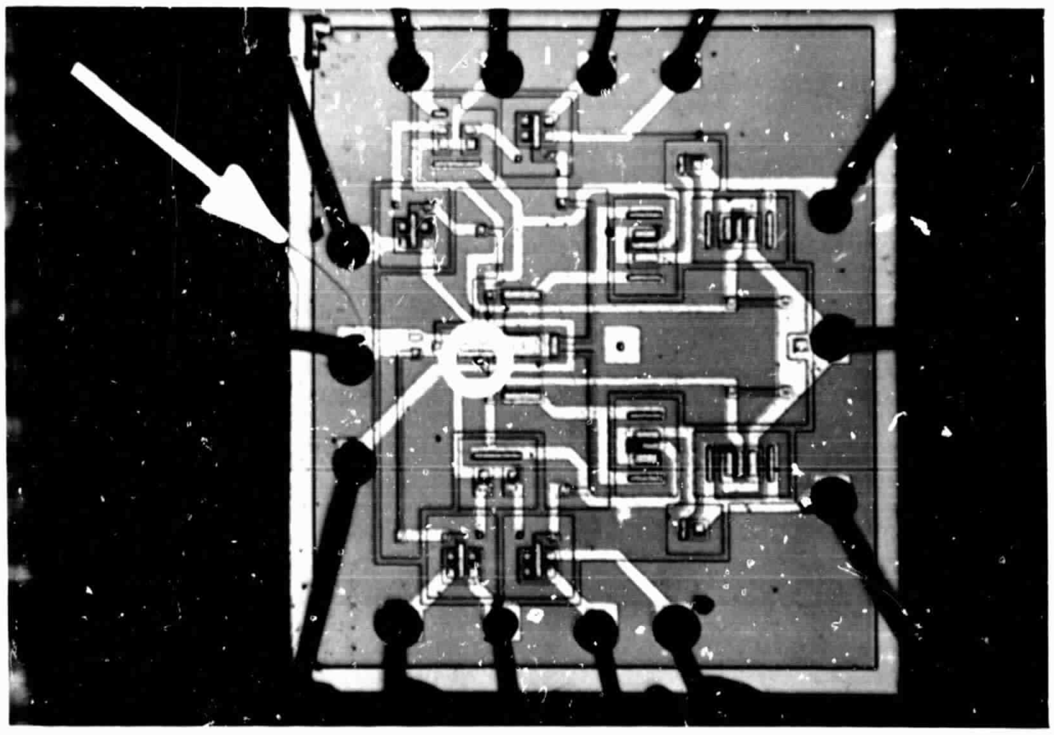

55X 1-1

FIGURE 1. TYPE SN5451 MICROCIRCUIT, SPECIMEN 12, SHOWING CRACKS IN SILICON DIE (ARROW) AND GOLD PARTICLES BRIDGING METAL STRIPES (CIRCLE)

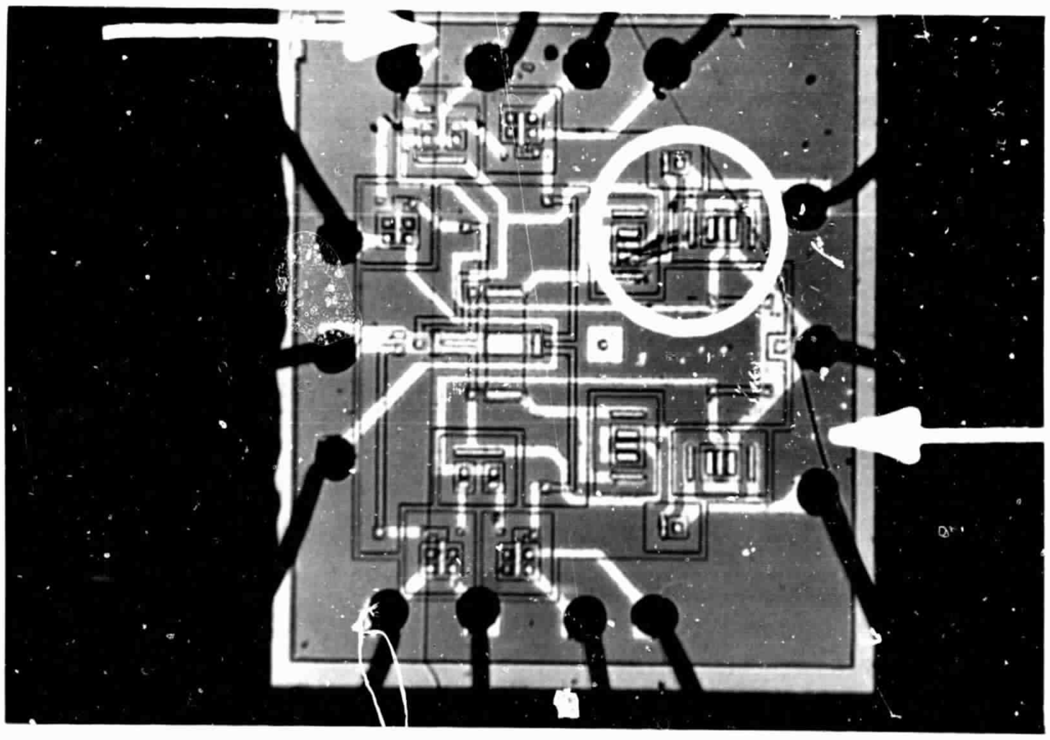

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FIGURE 2. TYPE SN5451 MICROCIRCUIT, SPECIMEN 13, SHOWING TWO CRACKS IN SILICON DIE (ARROWS) AND SMEAR IN METALLIZATION (CIRCLE)

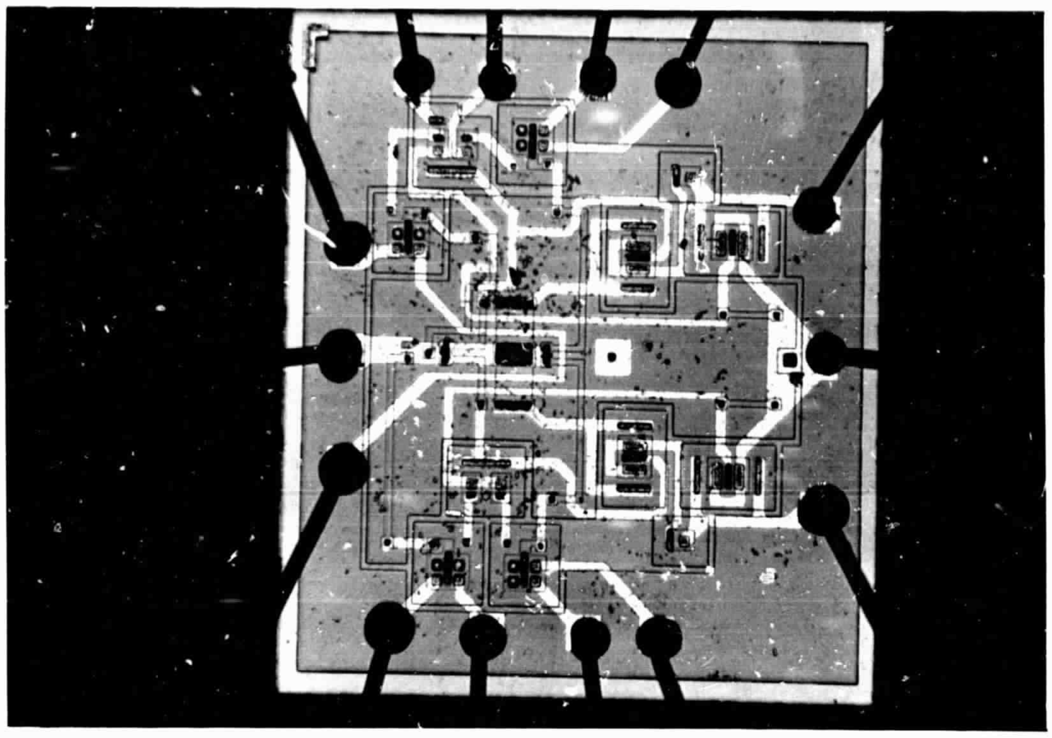
in the package bottom in the same direction as that seen in the die surface (Figure C-2 in Appendix C). The thickness of the silicon chips varied appreciably between the two circuits of this group that were cross sectioned. Specimen 14 contained a chip that was 5.9 mils thick: Specimen 16 (a control sample) contained a chip 8.1 mils thick. All six devices in this group were marked with the same lot number.

Specimen 11 was peppered with spots on the die surface (Figures 3 and 4). Since these spots were visible over both the active and the passive regions of the die and, also under the metallization, they evidently were holes in one of the layers of silicon dioxide. The sharp definition and random location of the spots, coupled with the ragged edges of the contact window cuts is indicative of masking problems in the final SiO_2 etch step during wafer fabrication.

The die surface of all specimens had varying amounts of attached foreign particles, most of which were organic, but also some metallic, chiefly gold. Only Specimen 12 was considered to be defective, having four such particles that bridged or nearly bridged between metal stripes or over active elements (Figures 1, 5, and 6). Specimen 14 had numerous minute gold particles over the whole die principally located along the vertical edges of the microtopography such as metallization edges, oxide steps and contact window cuts (Figure 7). At one point on this die, a gold particle was bulldozed across a metal stripe (Figure 8). The die had the appearance of being slid on its top face across a gold-contaminated surface prior to mounting in the package.

Internal Lead Wires

The internal lead wires were inspected for dress, nicks, scrapes, cracks, necking and clearance. The principal type of defect observed in these specimens



55X 1-0

FIGURE 3. TYPE SN5451 MICROCIRCUIT, SPECIMEN 11, SHOWING EXTENT OF OXIDE DEFECTS

500X 2-20

FIGURE 4. TYPE SN5451 MICROCIRCUIT, SPECIMEN 11, SHOWING DETAILED VIEW OF OXIDE DEFECTS AND WINDOWS HAVING RAGGED OUTLINES IN SECTIONS F3, F4, G3 AND G4

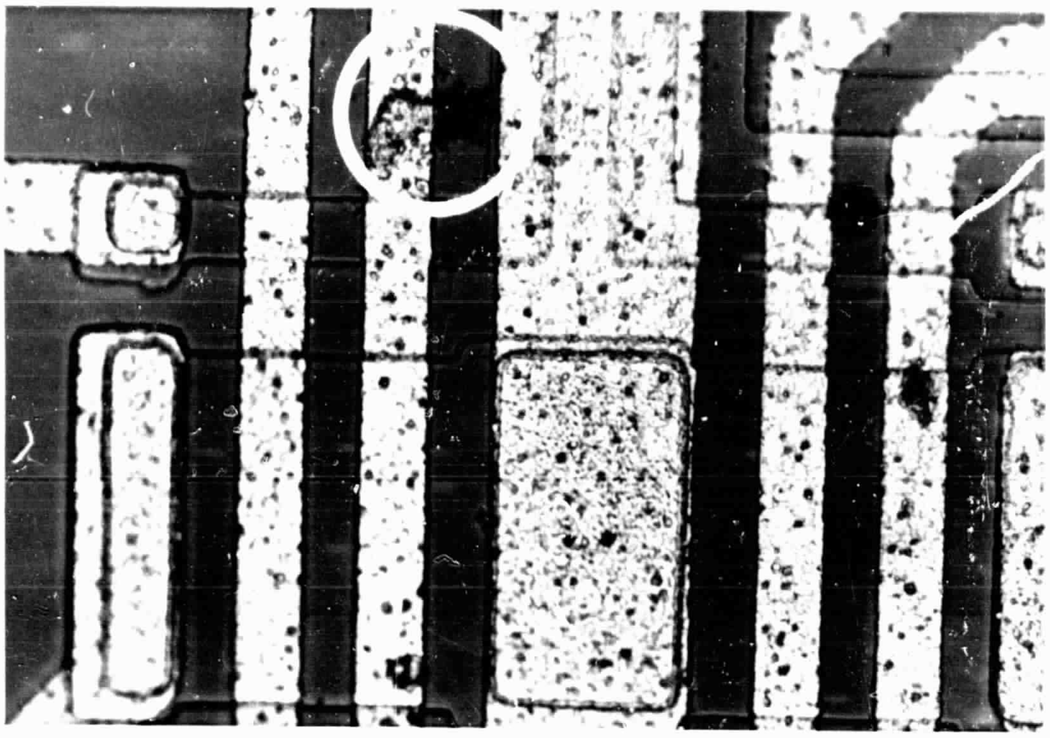


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FIGURE 5. TYPE SN5451 MICROCIRCUIT, SPECIMEN 12, SHOWING FOREIGN PARTICLES BETWEEN METAL STRIPES IN SECTIONS E4 AND F4

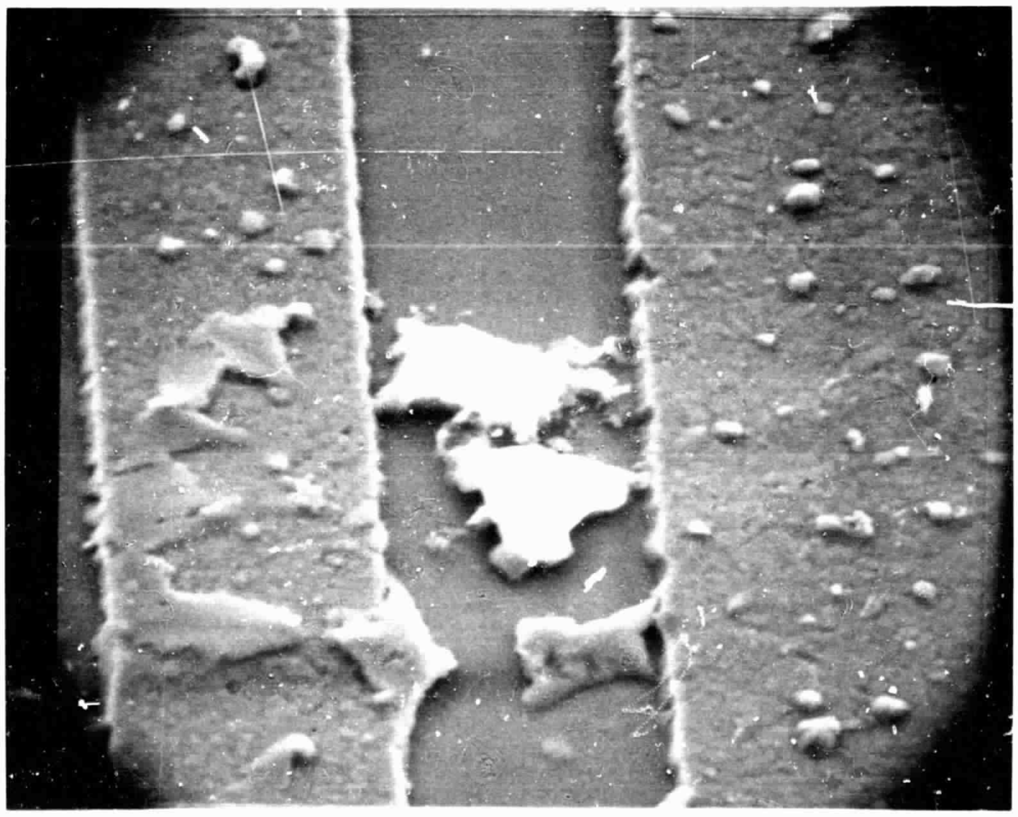

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FIGURE 6. HIGH MAGNIFICATION VIEW OF ENCIRCLED FOREIGN PARTICLE IN FIGURE 5 (SE)

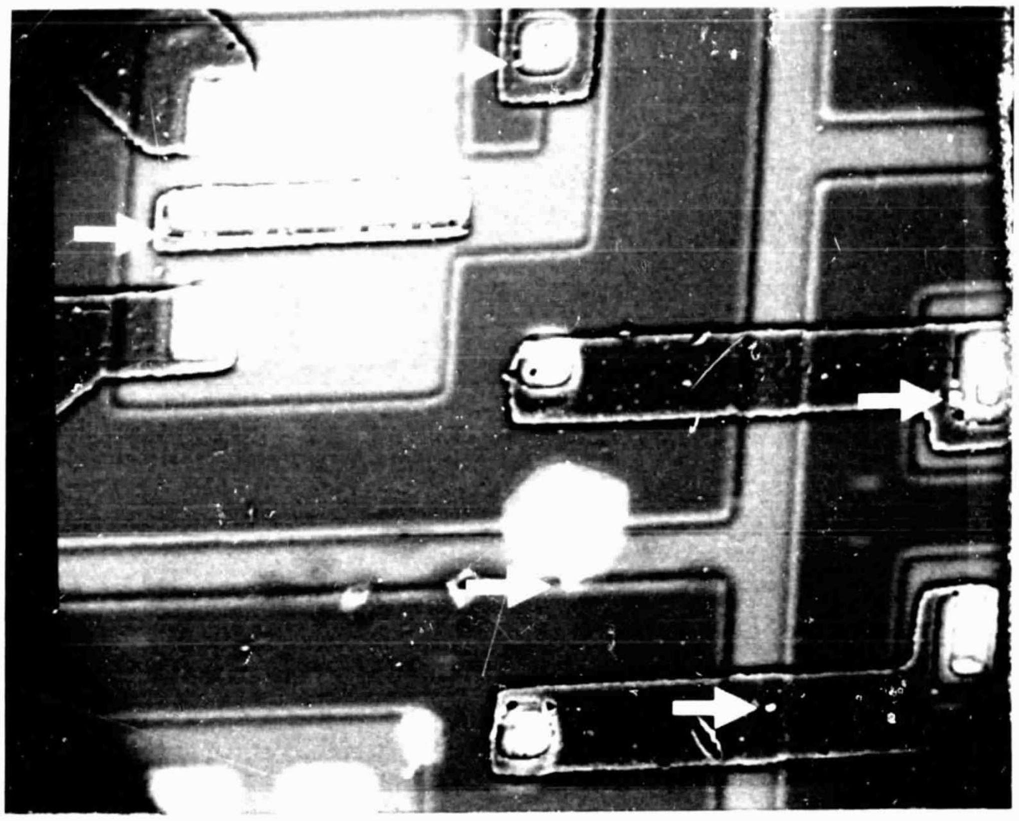

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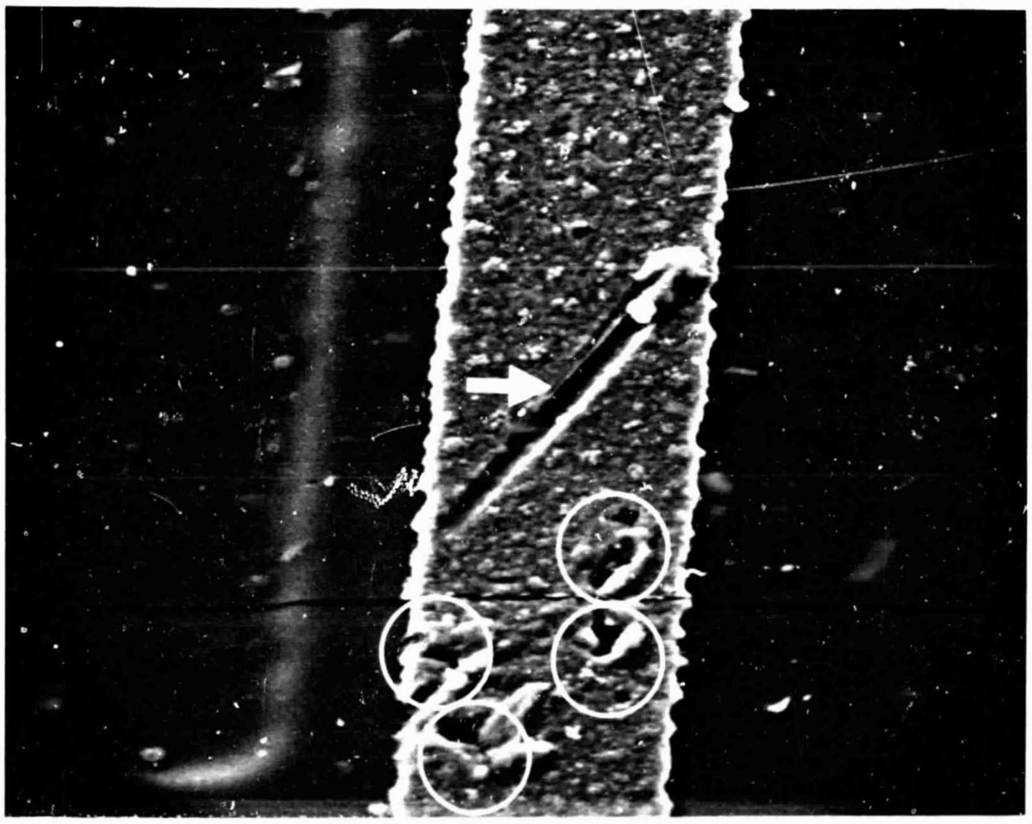
FIGURE 7. TYPE SN5451 MICROCIRCUIT, SPECIMEN 14, SHOWING GOLD PARTICLES AT VERTICAL EDGES OF MICROTOPOGRAPHY IN SECTIONS B3, B4, C3, AND C4 (BSE)



2000X S1086

FIGURE 8. TYPE SN5451 MICROCIRCUIT, SPECIMEN 14, SHOWING SCRATCH CAUSED BY GOLD PARTICLE (ARROW) AND POCKS IN METALLIZATION (CIRCLES) IN SECTION E7 (SE)

was the presence of annular cracks in the lead wire where the wire swells into the ball (Figure 9). As shown in Table 2, the incidence of this defect was very high. A significant number of leads were pulled tightly at right angles immediately above the ball bond (Figure 10). As can be seen in the Figures 11 and 12, this caused a necking down of the lead wire in the stress region. Two specimens exhibited several leads, each of which deviated from a straight line between pad bond and post bond by more than three times the lead-wire diameter. In both specimens, the defective leads appeared to have been bumped or snagged after installation.

Wire Bonds on Posts

The wire bonds on the posts or lands of the external leads were inspected for placement and size, i.e., spread in the wire caused by the bonding tool. One instance of improper bond placement was observed. As seen in the Figure 13, the wire shows no spread in the land area. Three circuits exhibited several leads that were overbonded to the posts. Figure 14 shows the worst case of this type of defect. A total of eleven such leads were observed.

Wire Bonds on Pads

The wire bonds on the pads all passed the requirement for size, i.e., a ball bond that is two to six times the wire diameter. However, the expanded metal pads on these circuits are of such size that a ball bond much greater than three times the wire diameter overlapped the pad in all directions. MIL-STD-883 specifies that a ball bond covering the fillet area (where the metal stripe emerges from the pad) is a defect. Many defects of this type were observed. Figure 15 shows an example of a well-centered bond covering the fillet, while Figure 16 shows the result of a slightly off-center bond placement.

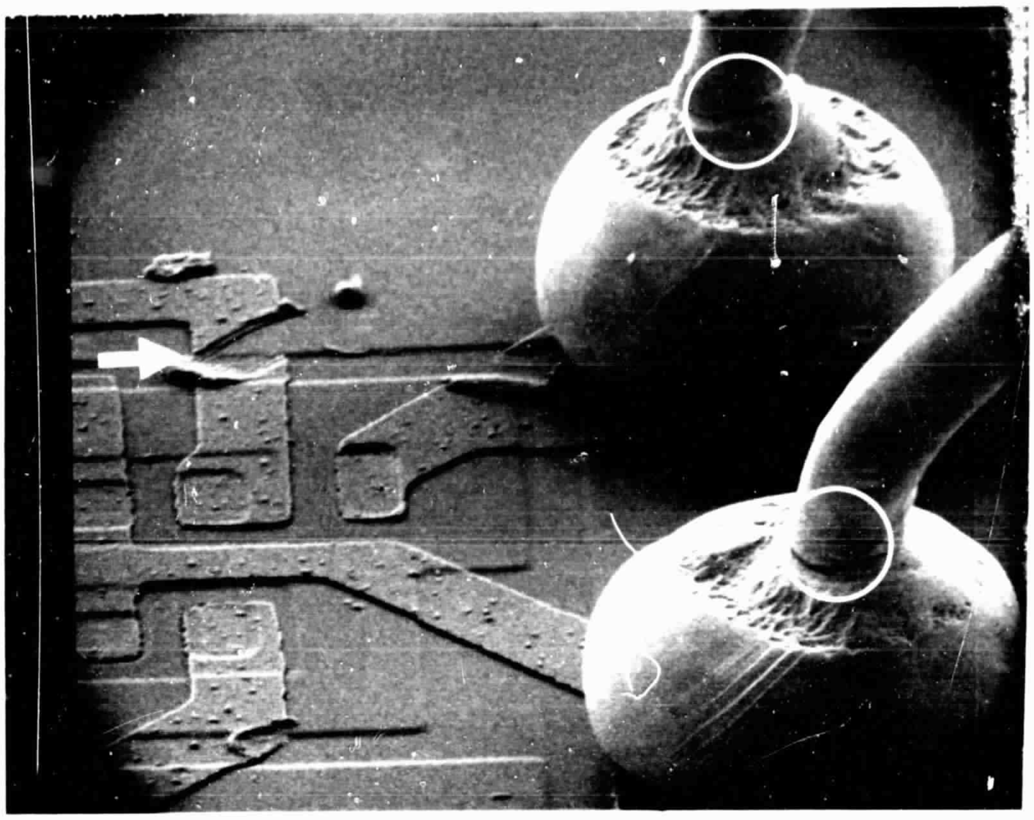


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FIGURE 9. TYPE SN5451 MICROCIRCUIT, SPECIMEN 13, SHOWING CRACKS IN LEAD WIRES (CIRCLES) AND DAMAGED METALLIZATION (ARROW) IN SECTIONS I2, J2, AND J4 (SE)

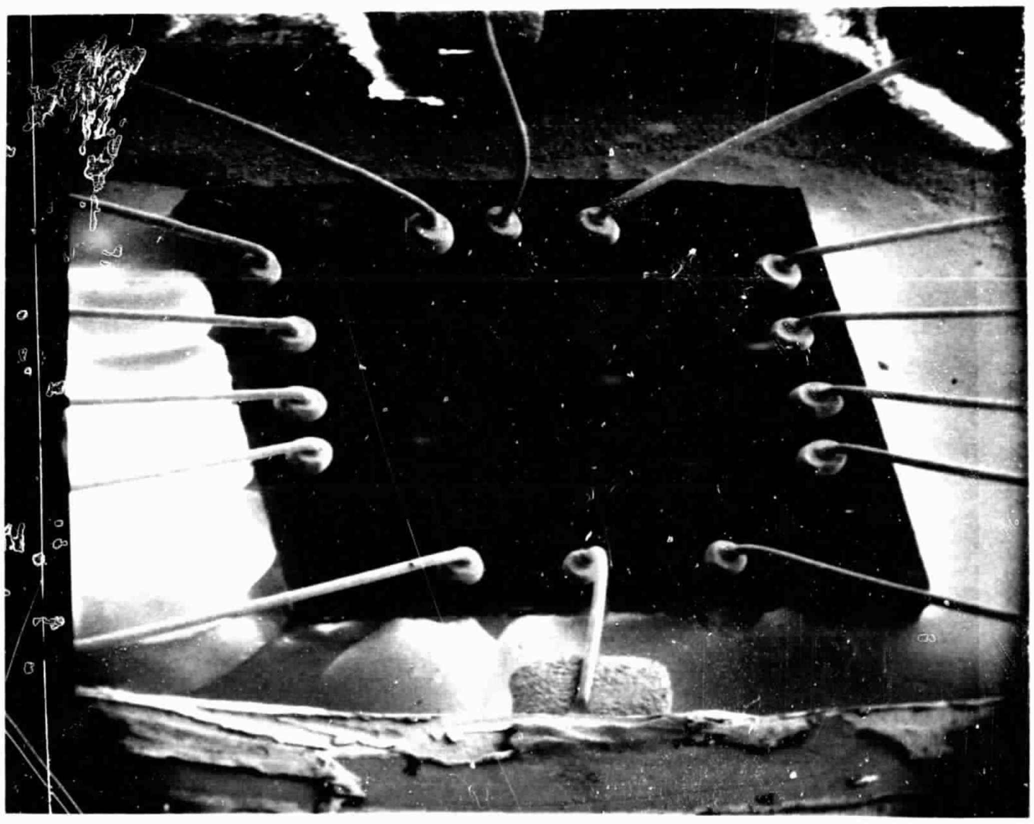

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FIGURE 10. TYPE SN5451 MICROCIRCUIT, SPECIMEN 15, SHOWING VARIATIONS IN BALL-BOND SIZE AND STRETCHED INTERNAL LEAD WIRES (SE)

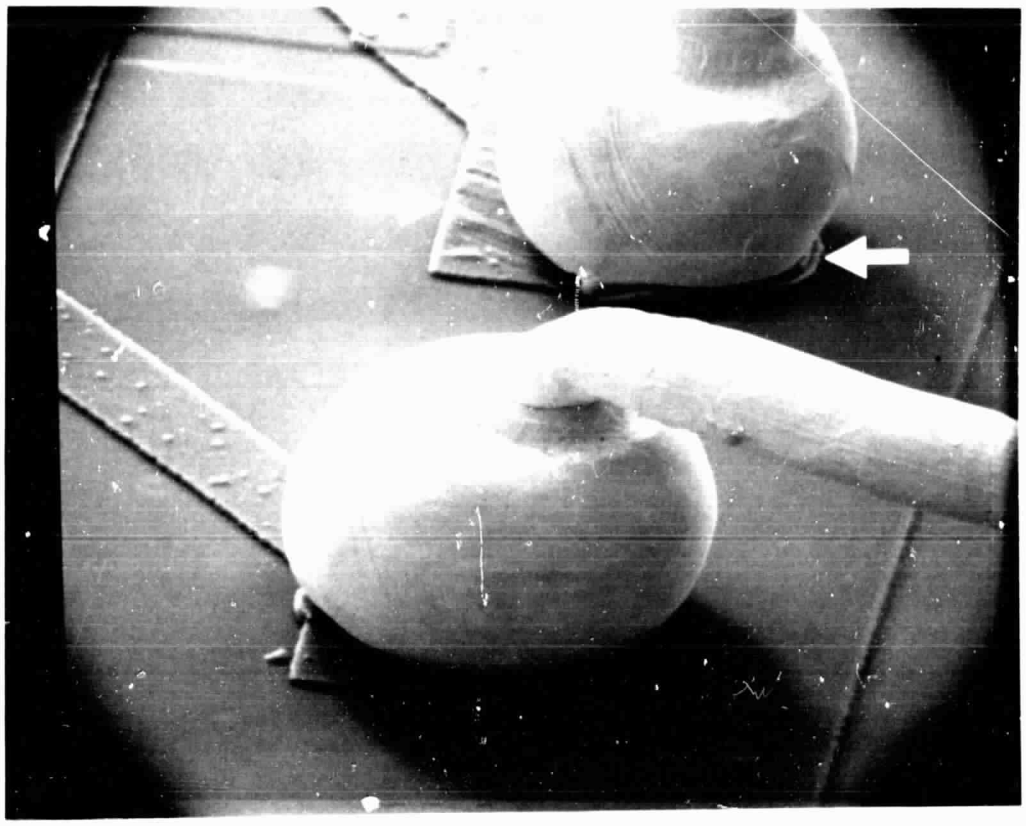

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FIGURE 11. TYPE SN5451 MICROCIRCUIT, SPECIMEN 11, SHOWING NECKING IN LEAD WIRE ABOVE BALL BOND AND METALLIZATION DAMAGE ON BONDING PAD (ARROWS) IN SECTIONS J5, J6, AND J7 (SE)

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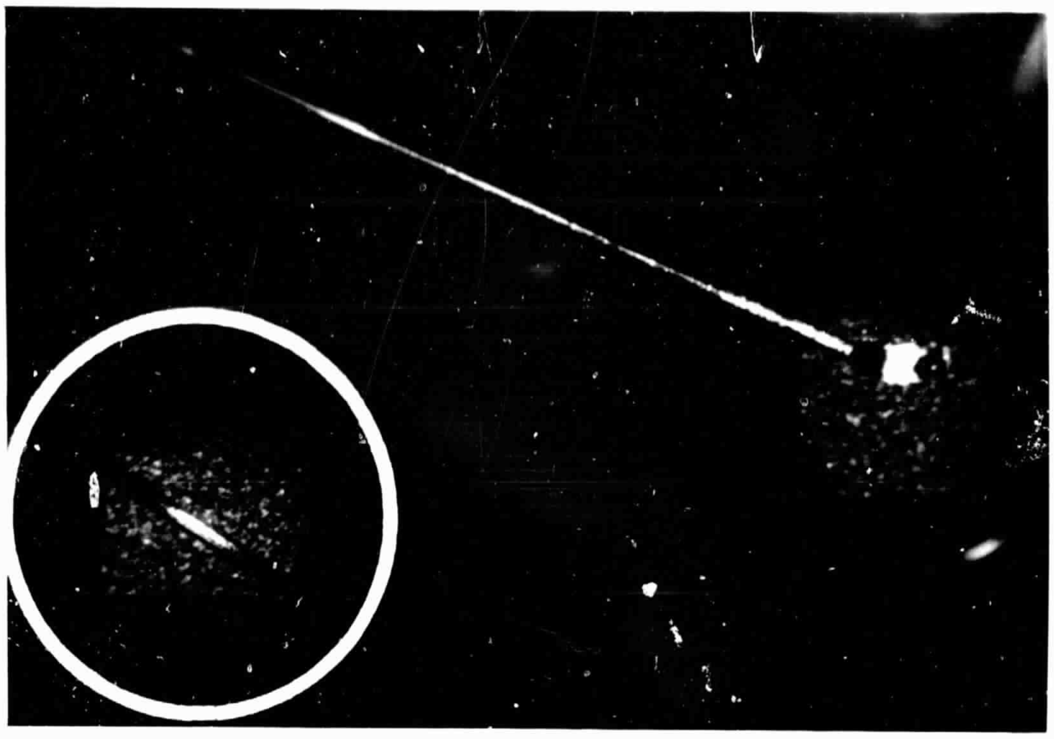
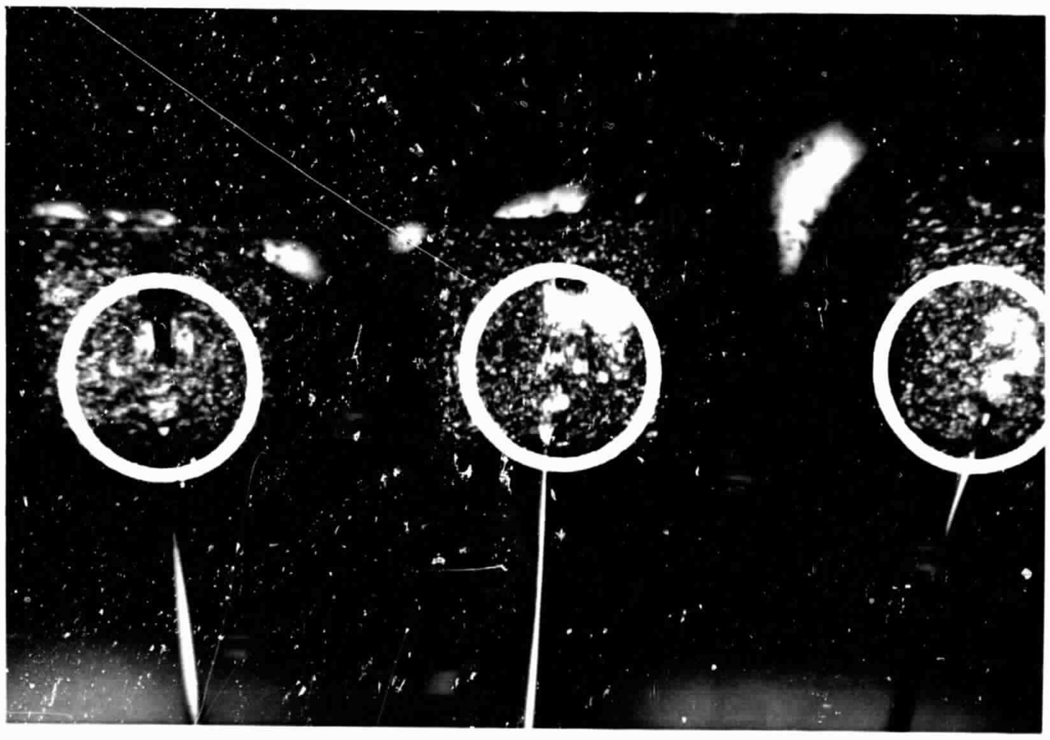
FIGURE 12. DETAILED VIEW OF THE BALL BOND FROM FIGURE 11 SHOWING NECKED WIRE AND CRACK AT TOP OF BALL BOND (ARROW) (SE)



91X 2-19

FIGURE 13. TYPE SN5451 MICROCIRCUIT, SPECIMEN 11, SHOWING DEFECTIVE LEAD WIRE BOND ON POST 12



91X 3-9

FIGURE 14. TYPE SN5451 MICROCIRCUIT, SPECIMEN 13, SHOWING OVERBONDED LEAD WIRES ON POSTS 6, 7, and 8

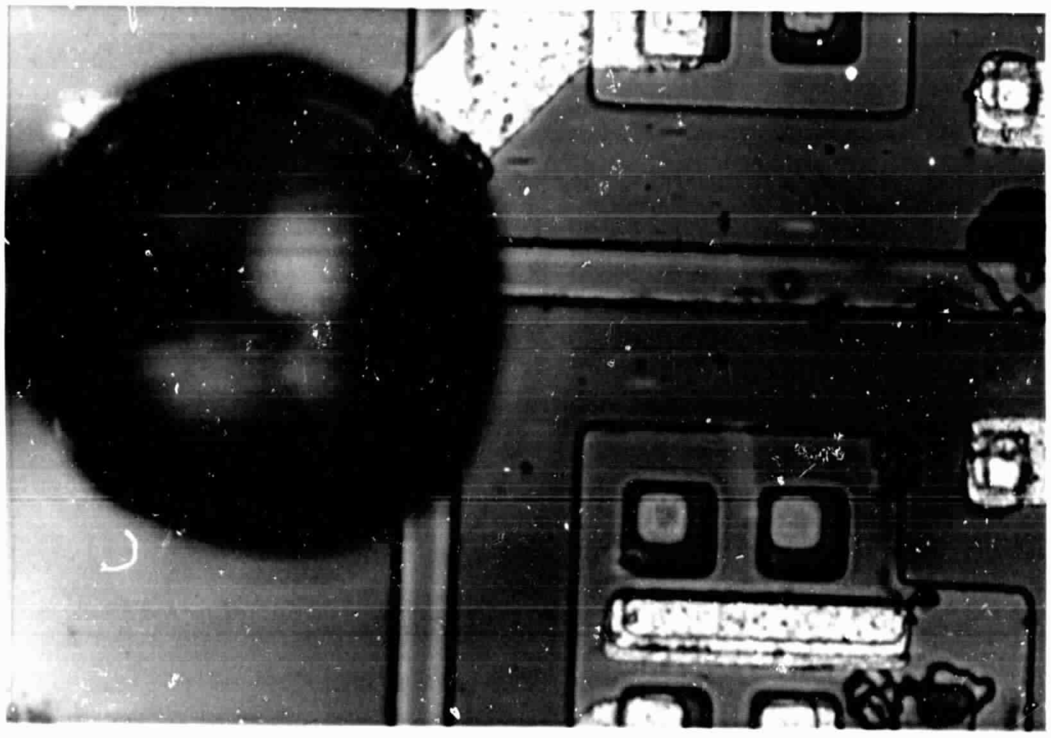


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FIGURE 15. TYPE SN5451 MICROCIRCUIT, SPECIMEN 14, SHOWING AN OVERSIZE BALL-BOND COVERING FILLET BETWEEN BONDING PAD AND STRIPE IN SECTION A4

500X 3-16
FIGURE 16. TYPE SN5451 MICROCIRCUIT, SPECIMEN 14, SHOWING OFF-CENTER BALL-BOND COVERING FILLET BETWEEN BONDING PAD AND STRIPE IN SECTION J5

Several instances of rebonding or false strikes with the ball bonder were noted, but only two of these were considered to be defects because the first strikes had occurred within the pad area. Figure 17 shows an example of an acceptable first strike made outside of the pad.

Metallization

The metallization pattern on these dies was well defined and satisfactorily aligned. Window coverage was nearly always 100 percent and never less than 90 percent. Bridging from photolithographic defects did not exist. A few very small photolithographic voids were observed as in Figure 18, but none of these were large enough to be considered defective.

The principal type of defect in the metallization on these circuits was induced damage in the form of scratches, smears, and bridging. From the evidence accumulated, the damage occurred primarily during two steps in the packaging process (chip handling and ball bonding) and one step in wafer production (electrical probing).

Damage as manifested by nicks, cuts, long sweeping cosmetic scratch networks and particulate bulldozing is traceable to improper handling of the loose chips. The nick, in Figure 19, suggests accidental probing with a handling tool such as a tweezers; the cuts in Figures 20 and 21 may have been caused by a collision with the sharp edge of another die; the scratching and bulldozing in Figures 22 and 8 likely resulted from sliding the die, face down, across a dirty or contaminated surface.

A more serious kind of damage can be traced to problems in the ball-bonding operation. Numerous scrapes, gouges, and smears, resulting sometimes in

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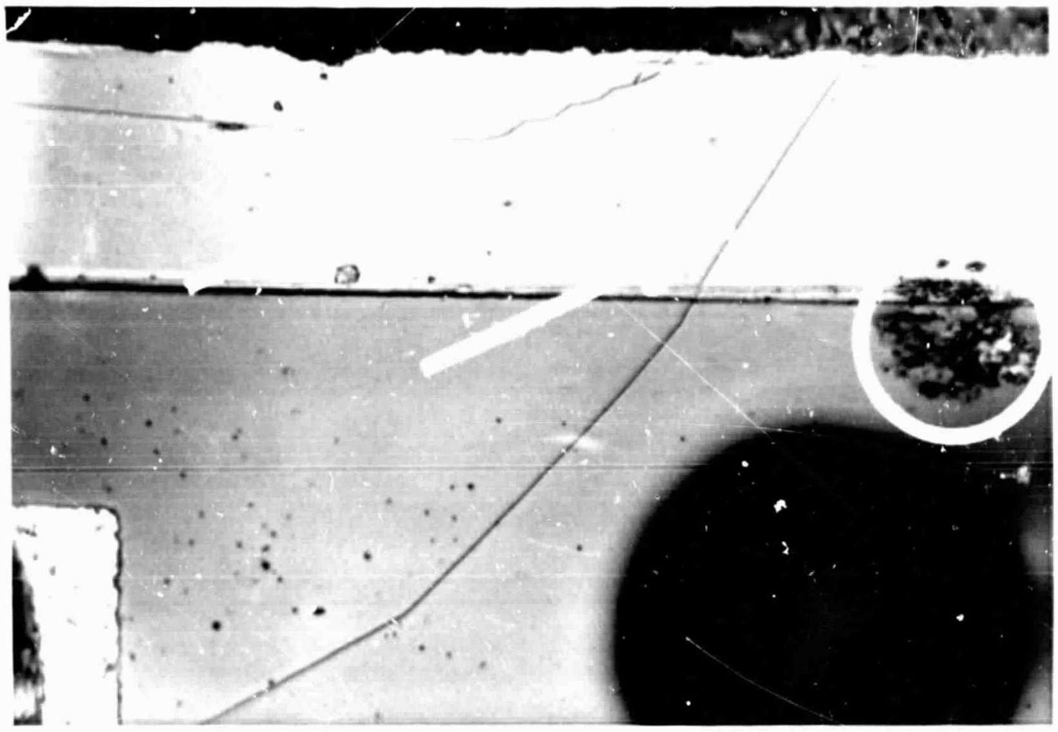

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FIGURE 17. TYPE SN5451 MICROCIRCUIT, SPECIMEN 12, SHOWING CRACKS IN SILICON DIE (ARROWS) AND EVIDENCE OF A FALSE BALL-BOND STRIKE (CIRCLE) IN SECTIONS F1 AND G1

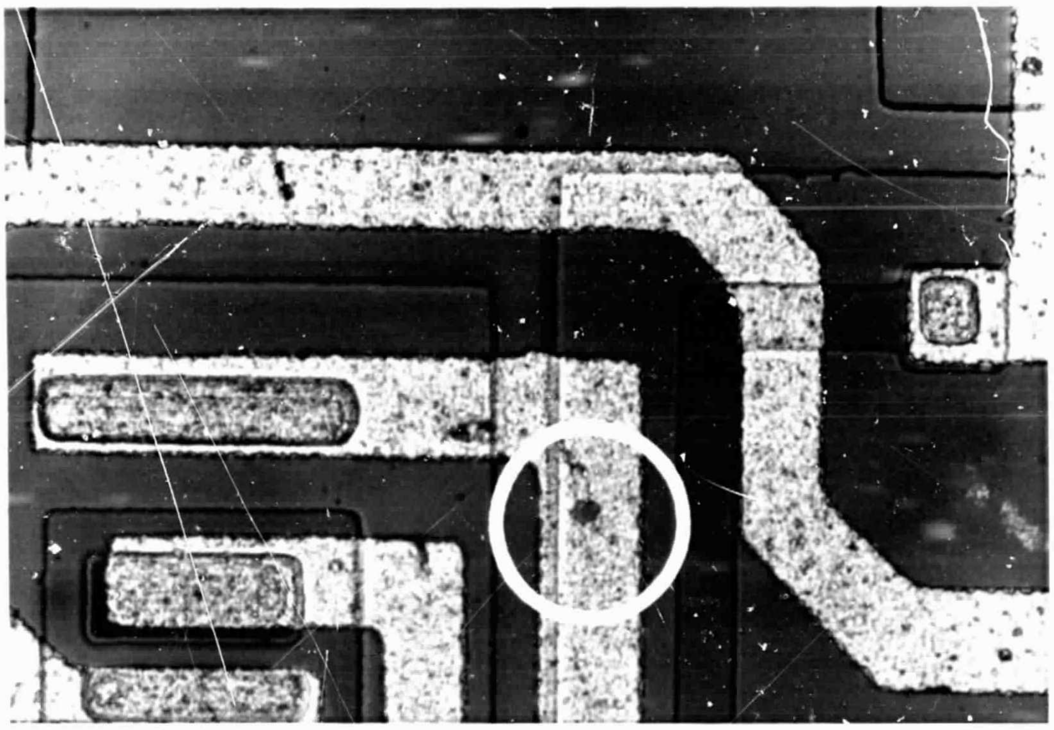

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FIGURE 18. TYPE SN5451 MICROCIRCUIT, SPECIMEN 15, SHOWING PHOTOLITHOGRAPHIC VOID IN METAL STRIPE IN SECTION D6

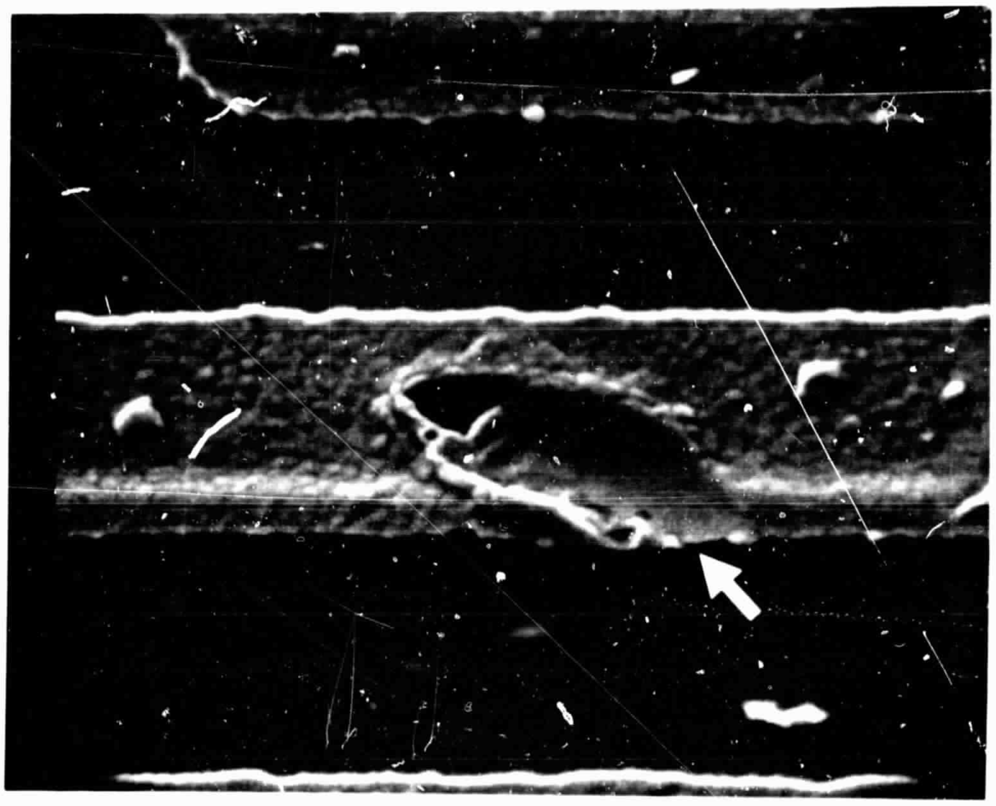

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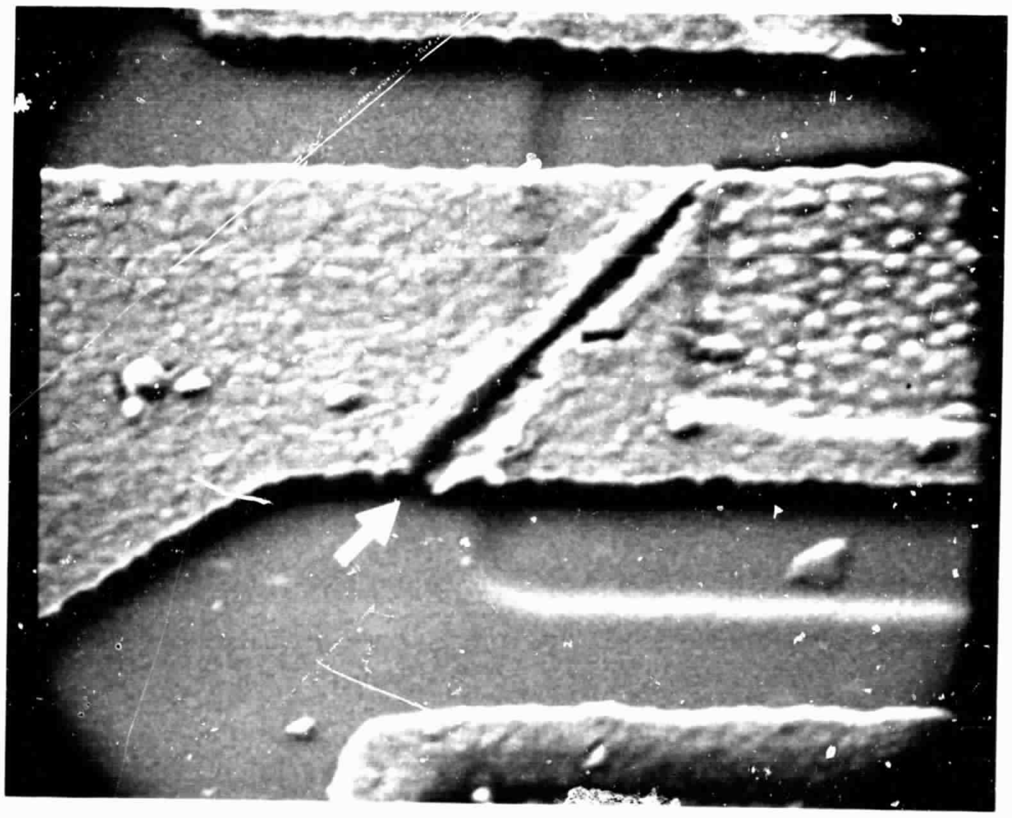
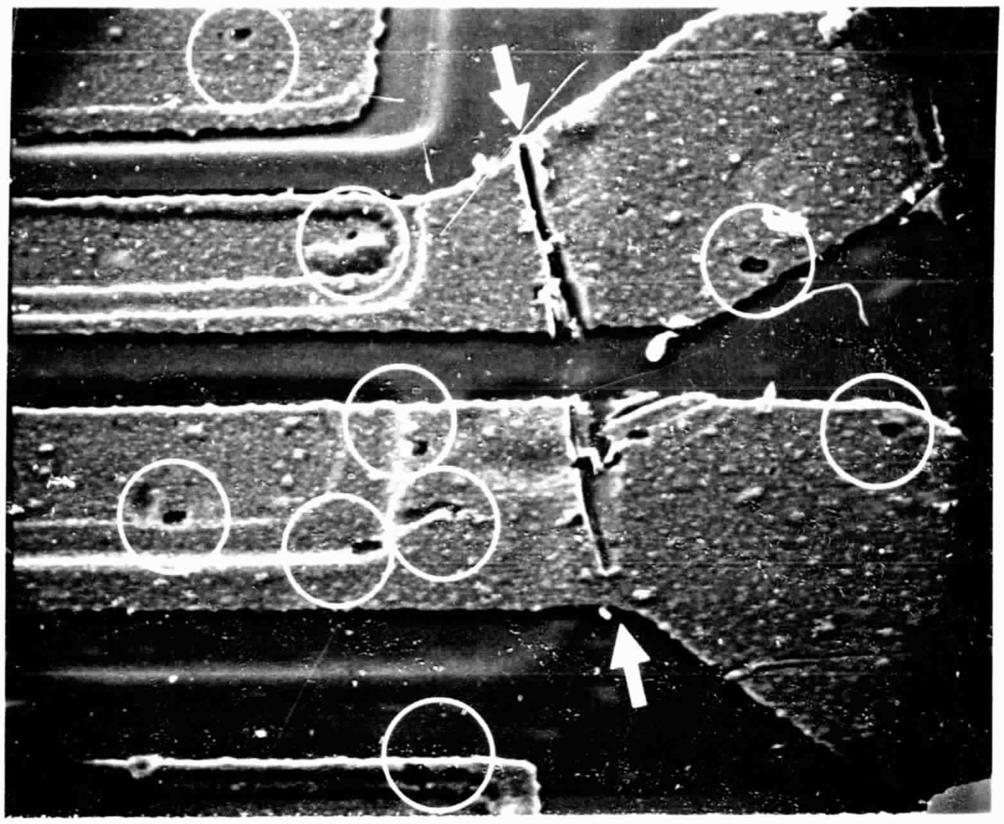
FIGURE 19. TYPE SN5451 MICROCIRCUIT, SPECIMEN 11, SHOWING NICK IN METAL STRIPE IN SECTION G7 (SE)



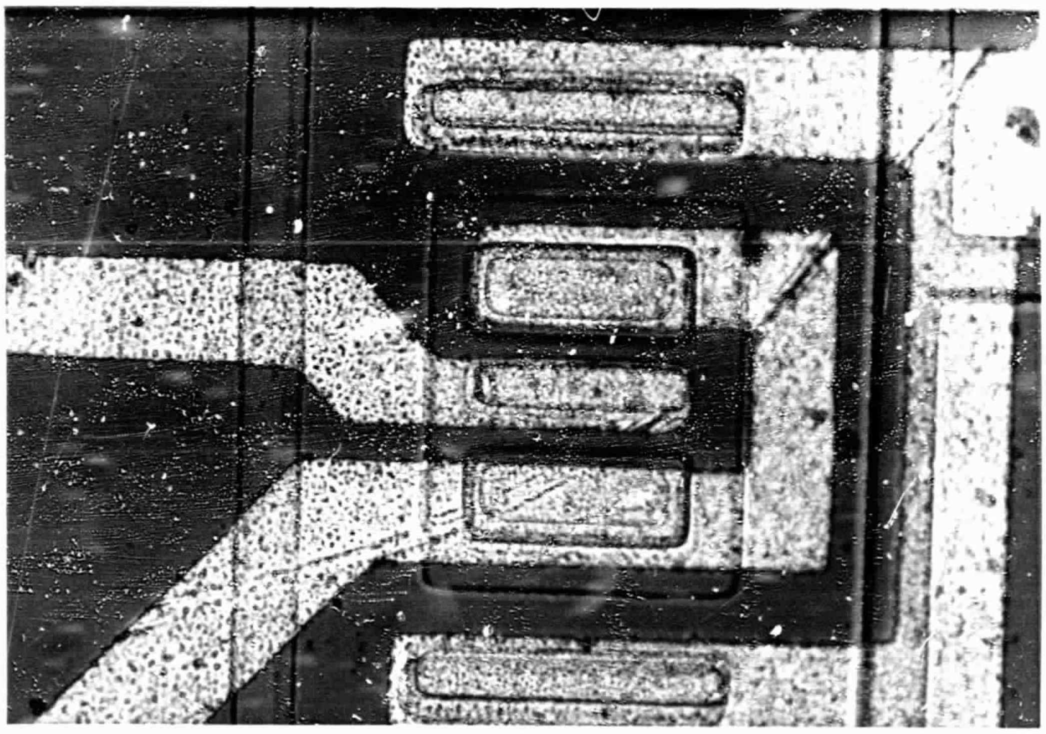
2000X S1033

FIGURE 20. TYPE SN5451 MICROCIRCUIT, SPECIMEN 11, SHOWING CUT IN METAL STRIPE IN SECTION G8 (SE)



2000X S1087

FIGURE 21. TYPE SN5451 MICROCIRCUIT, SPECIMEN 14, SHOWING CUTS IN METAL STRIPES (ARROWS) AND SMALL POCKS (CIRCLES) IN SECTION D8 (SE)



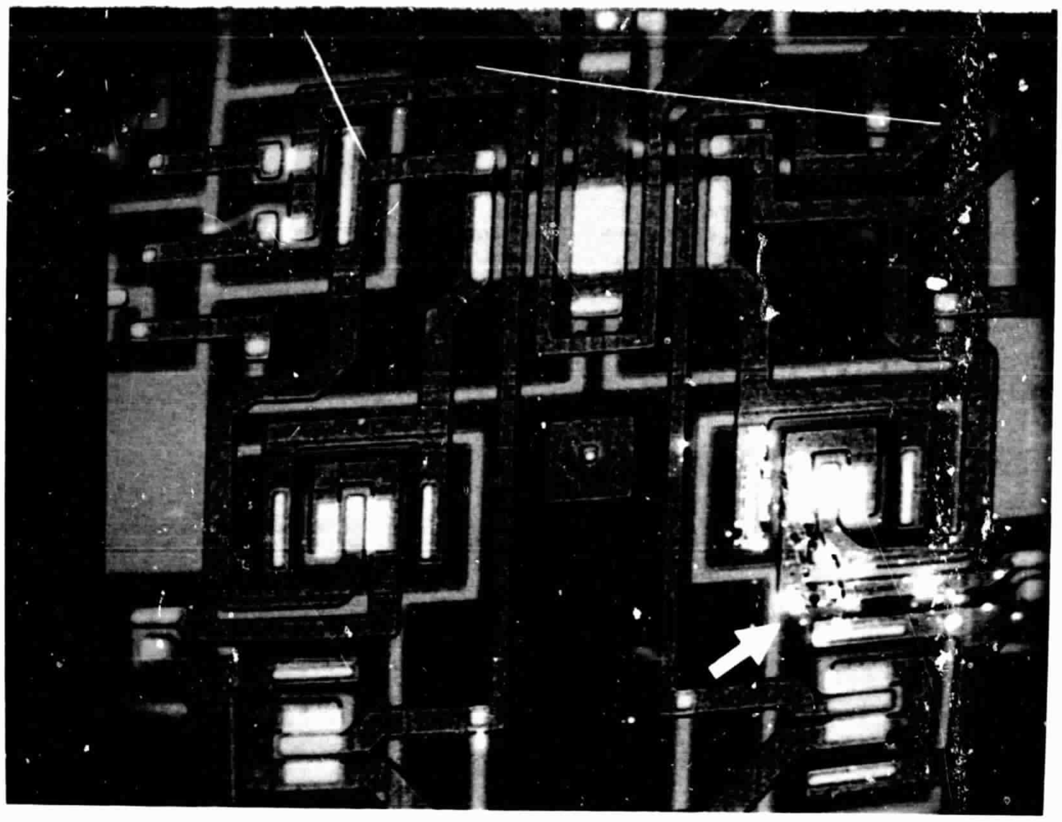
500X 8-13

FIGURE 22. TYPE SN5451 MICROCIRCUIT, SPECIMEN 14, SHOWING LONG SWEEPING SCRATCH ACROSS METALLIZATION IN SECTION G8, G9, H8, AND H9

bridging between metal stripes, was observed in these circuits. The fact that the ball bonds were dragged across the surface is indisputable. One type of damage that resulted was observed in Specimen 13. In Figure 2, a major smear can be seen curving from near the center of the die to Bonding Pad 12. The SEM backscatter presentation of this area (Figure 23) shows the damaged region to be laddened with gold particles. In Figure 24, a 2000X SEM view of the most seriously damaged area, a metal stripe is severed, less serious smearing surrounds the cut, and numerous gold particles are visible. Figure 11 shows the effect of dragging the gold ball onto the bonding pad. The aluminum surface is gathered in front of the ball and wiped thin behind it. Not all pad damage is thought to have resulted from dragging ball bonds into place, however. Figure 2 shows evidence of pad damage probably caused by electrical probes in the wafer-characterization station. Tooling of the metallization is evident on the inward edge of Pads 13, 14, 1, and especially 2 (see Figures 25 and 9) and on the outward edge of Pads 6, 7, 8, and 9 on the opposite edge of the die. In so far as can be determined, all of these smears are of approximately the same length, in the same direction, and have no gold particles present. Probably the wafer or the probe-holder assembly changed position slightly while the probes were resting on the pads.

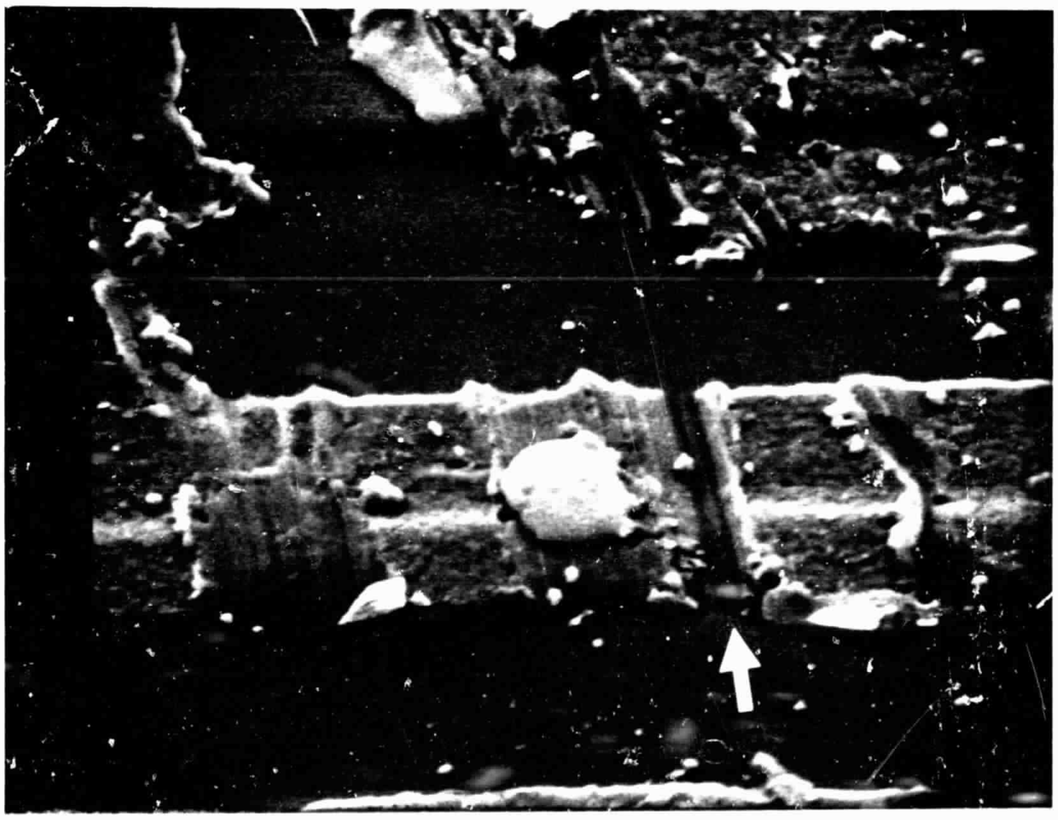
Windows

Metallization defects in the window cuts were observed in only one circuit of this group. Specimen 14 exhibited very definite cracks in the metal at the oxide step in the window regions (see arrow in Figure 26). But, then, the same characteristic was noted at less-severe oxide steps away from window cuts (Figure 27). The metallization had a brittle appearance and was speckled with



130X S1050

FIGURE 23. TYPE SN5451 MICROCIRCUIT, SPECIMEN 13, SHOWING GOLD PARTICLES IN DAMAGED REGION OF METALLIZATION, SECTIONS G6, G7, AND H7 (BSE)



2000X S1055

FIGURE 24. DETAILED VIEW OF FIGURE 23 SHOWING SEVERED CONDUCTOR, SMEARS, AND GOLD PARTICLES IN SECTION G7 (SE)

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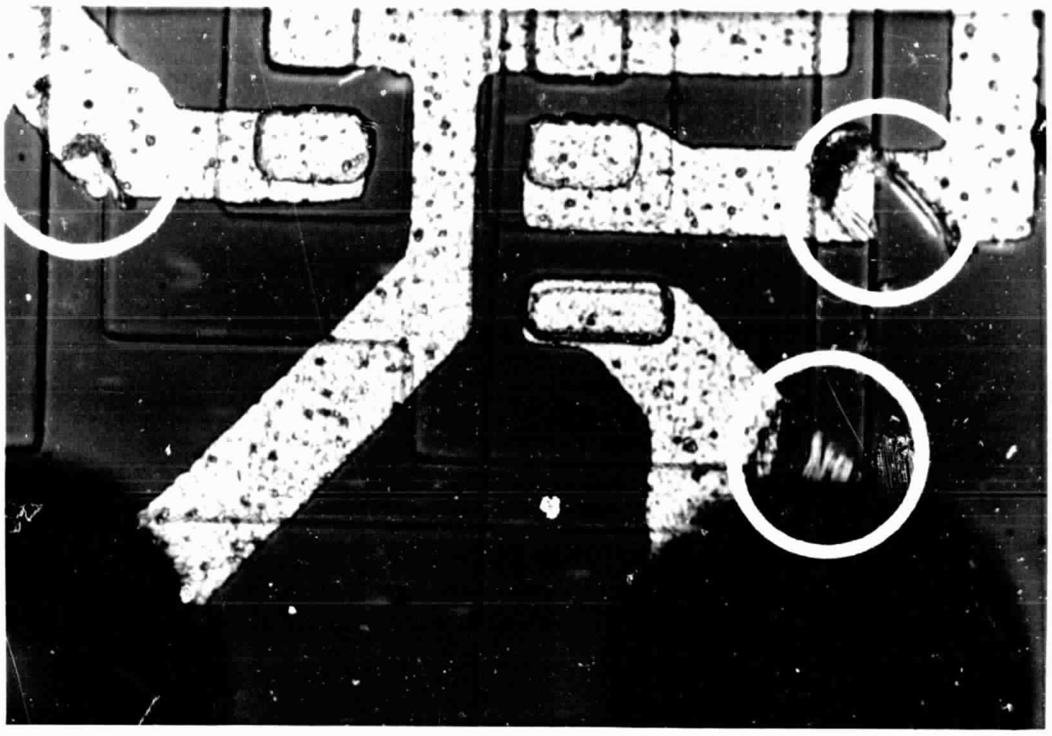
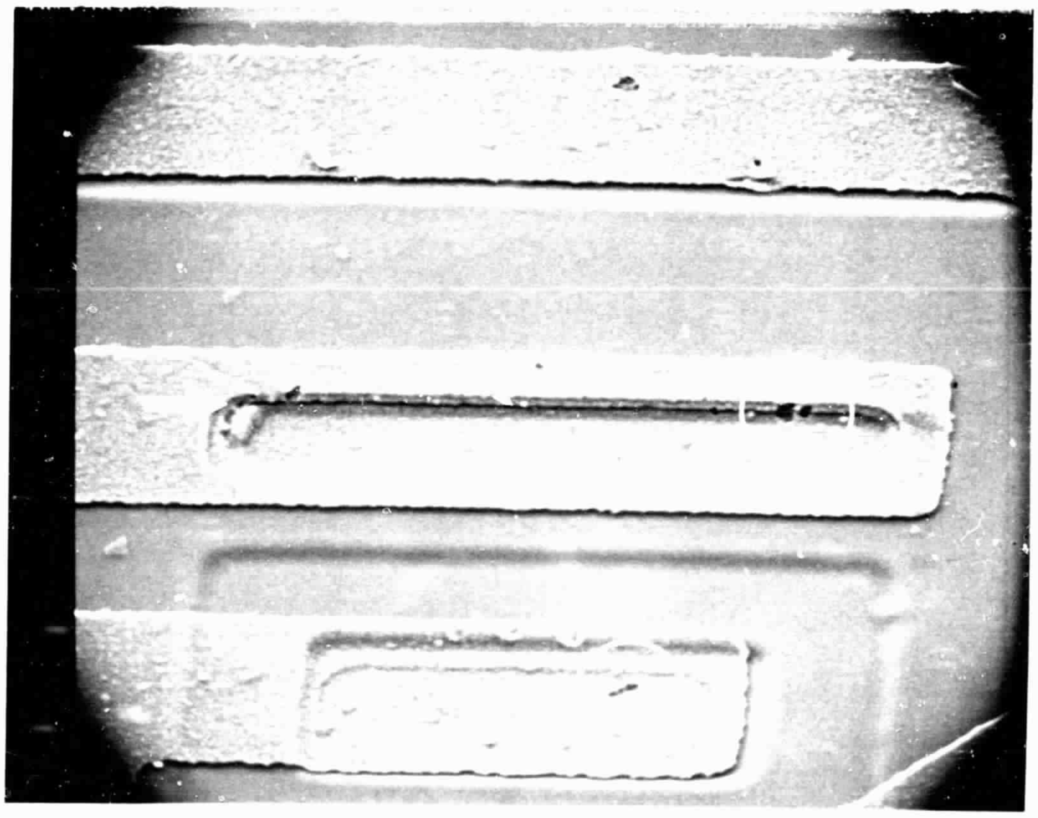


500X 3-12

FIGURE 25. TYPE SN5451 MICROCIRCUIT, SPECIMEN 13, SHOWING SMEARS IN METALLIZATION CAUSED BY ELECTRICAL PROBES, SECTIONS I2, I3 AND I4



1000X S1085

FIGURE 26. TYPE SN5451 MICROCIRCUIT, SPECIMEN 14, SHOWING CRACK IN METALLIZATION AT OXIDE-STEP IN WINDOW CUT (ARROW) AND POCK MARKS (CIRCLES) IN SECTIONS G6, G7, H6, AND H7 (SE)

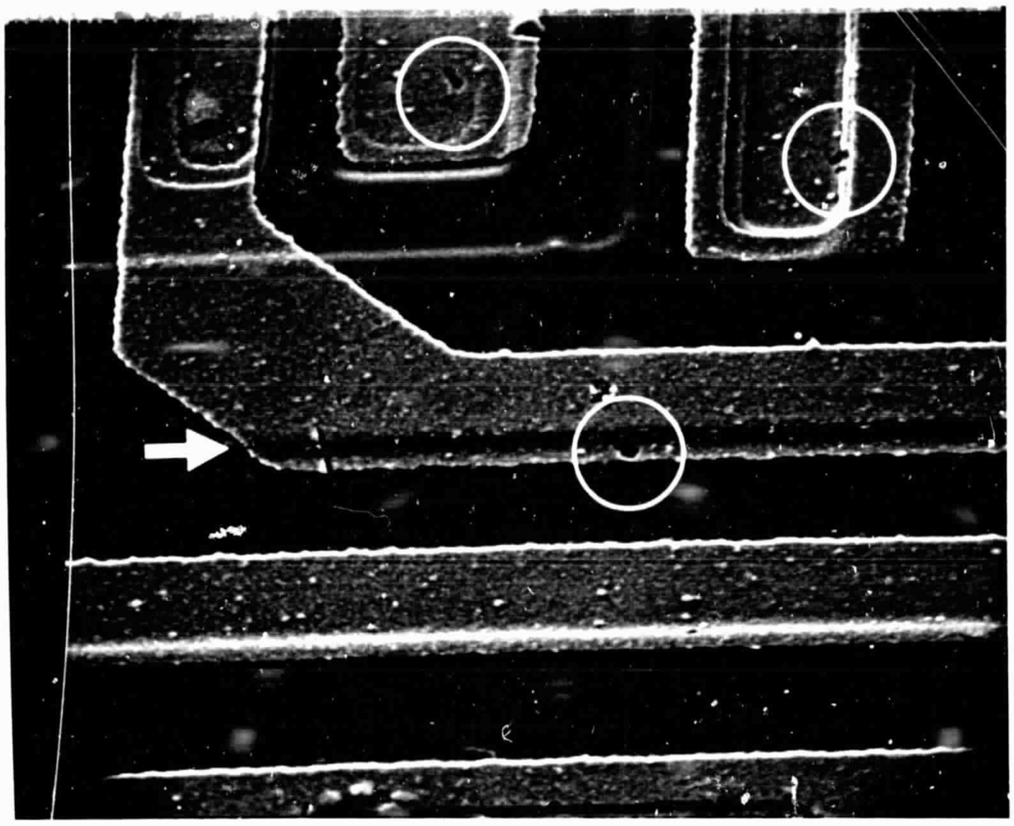
numerous small pocks such as seen in Figures 8, 21, 26, and 27. These pocks occurred randomly at oxide steps, in the flat regions of the windows, and in the flat regions of of metal stripes. Specimen 15 showed similar pock marks occurring randomly in the metallization but the cracks at oxide steps were not observed.

The ragged edges of some of the windows on Specimen 11, previously mentioned under Die Condition, appear to be a photolithography problem. However, the metallization in all the windows of this die has a granular off-color appearance seen in Figure 3. Observed at 2000X in the Scanning Electron Microscope, (Figures 20 and 28) the metallization surface in the windows is rough, much more so than observed in similar circuits. Further study shows that the windows in the p-type regions (bases, anodes, and resistors) appear darker in hue than do the windows in the n-type regions (emitters, collectors, and cathodes).

Type SN54L51 Gates
(Manufacturer A, Specimens 21 to 25)

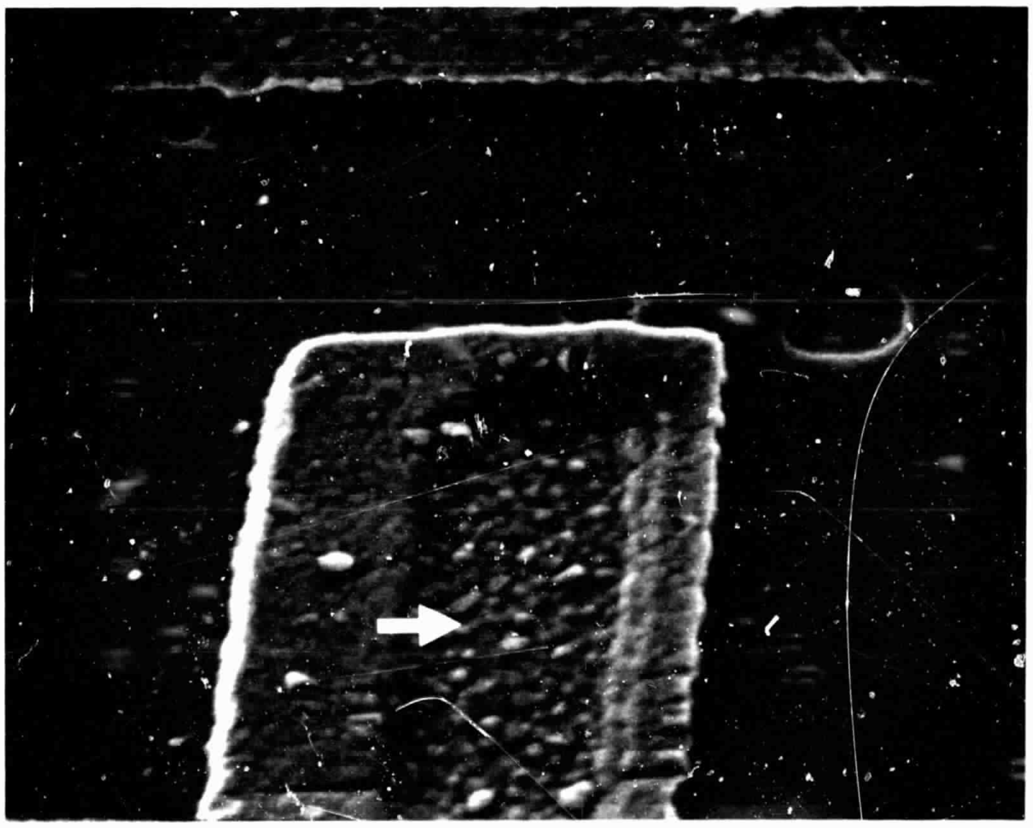
General

The Type SN54L51 specimens were contained in the TO-84 package having a metal lid and bottom, welded lid-seal and glass lead-seals. A nonmetallic bonding medium was used to fasten the chips into the package; the material appeared to be a glass frit. A two-layer metallization system (gold over molybdenum) of approximately 2 microns total thickness was used in these circuits. Internal leads were flying gold wires, ball bonded to the die pads and wedge bonded to the package posts.



1000X S1080

FIGURE 27. TYPE SN5451 MICROCIRCUIT, SPECIMEN 14, SHOWING CRACK IN METALLIZATION AT OXIDE STEP NOT IN WINDOW CUT (ARROW) AND POCKS (CIRCLES) IN SECTIONS G7 AND H7 (SE)



2000X S1035

FIGURE 28. TYPE SN5451 MICROCIRCUIT, SPECIMEN 11, SHOWING GRANULARITY OF METALLIZATION SURFACE IN CONTACT WINDOW IN SECTION H3 (SE)

Package Exterior

No defects were observed in any of the package exteriors. Specimens 21 showed several small bubbles in the glass seal around one lead but none of these bubbles reached the outer surface.

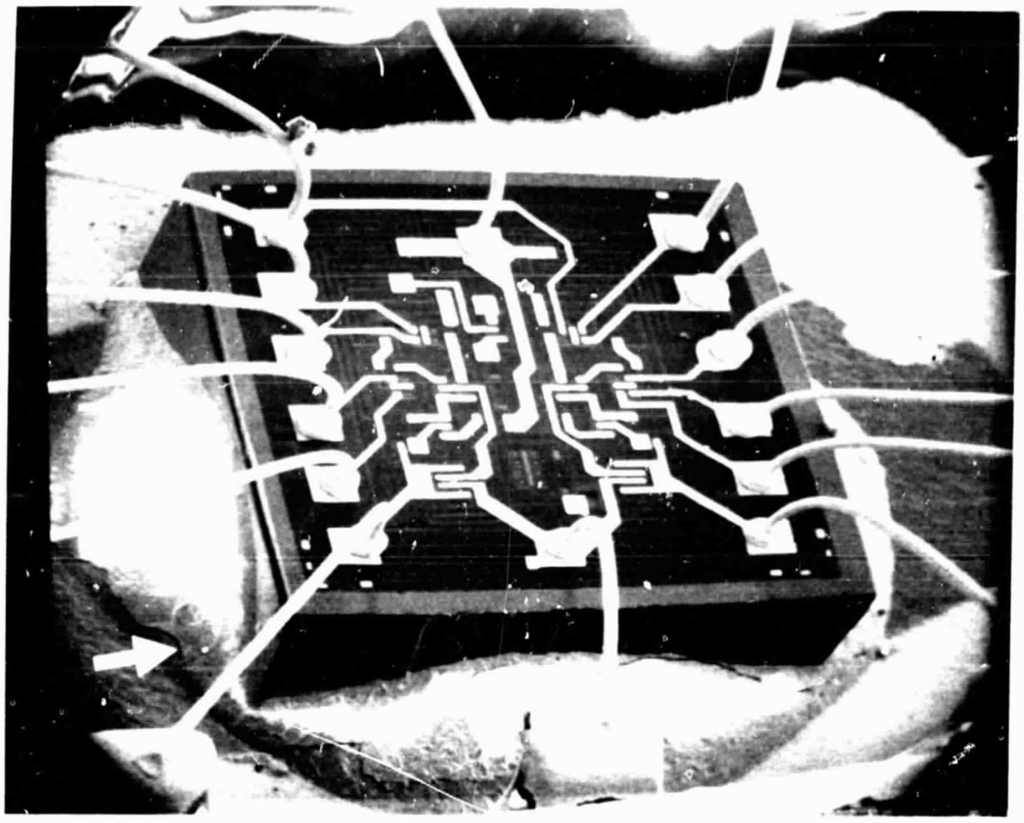
Package Interior

One package contained a loose foreign particle, an opaque strand approximately 0.2 mil in diameter by 40 to 50 mils long. In attempting to remove the strand with tweezers it broke easily and continued to break each time the tweezers touched it.

The center area of the package floor lacked the gold plating of the other surfaces of the package. Although this area showed discoloration in two of the packages, no corrosion scale was visible.

Two specimens showed crazing in the fillet of bonding material around the chip and some evidence of chip delamination from package floor (Figure 29). In one of these specimens, the chip popped loose when prodded moderately with a microtool. In the specimens that were cross sectioned, small bubbles ranging in size up to 1.5 mils in diameter, were found in the bonding material under the chip.

The orientation of the die with respect to the package leads was satisfactory in all specimens, but considerable variation existed in the centering and leveling of the chip with respect to the package floor. The thickness of the bonding agent varied as much as 2.9 mils from one edge of a given chip to the opposite edge (see Figure C-1 in Appendix C).



50X S1353

FIGURE 29. TYPE SN54L51 MICROCIRCUIT, SPECIMEN 22, SHOWING DELAMINATION OF CHIP BONDING MATERIAL FROM PACKAGE FLOOR (SE)

Die Condition

In general, the die surface of the specimens in this group was free of large foreign particles. Specimen 21 (Figure 30) had a foreign particle approximately 0.75 x 1.5 mil that did not dislodge during the dry-nitrogen gas blow. Specimen 24 (Figure 31) was peppered with minute flecks of gold that suggested photolithography problems during etching of the gold metallization. Specimen 25 showed a similar, but much less-severe condition. Several specimens exhibited accumulations of organic material along the edges of metal stripes.

Internal Lead Wires

As observed in the SN5451 circuits, annular cracks were present in the lead wires just above the ball bonds. Figure 32 shows a typical view of these cracks. The occurrence of severe cracks was somewhat lower than in the SN5451 circuits but most of the leads exhibited the defect to some degree. An anomalous ball-bond defect was discovered in Specimen 23 (Figure 33). This unusual defect appears to have resulted from some malfunction of the ball-bond machine causing a section of the lead wire to lap sideways and become flattened along with the ball. The incidence of necking in the lead wires was very low. One such observed defect also appeared to be due to ball-bond-machine malfunction.

Specimen 25 exhibited three lead wires that deviated by more than three wire diameters from a straight-line path between the two endpoints. These leads appear to have been bumped after installation. In general, the gold leads showed a tendency to sag toward the package floor although none approached the metal floor or each other by less than 6 mils.

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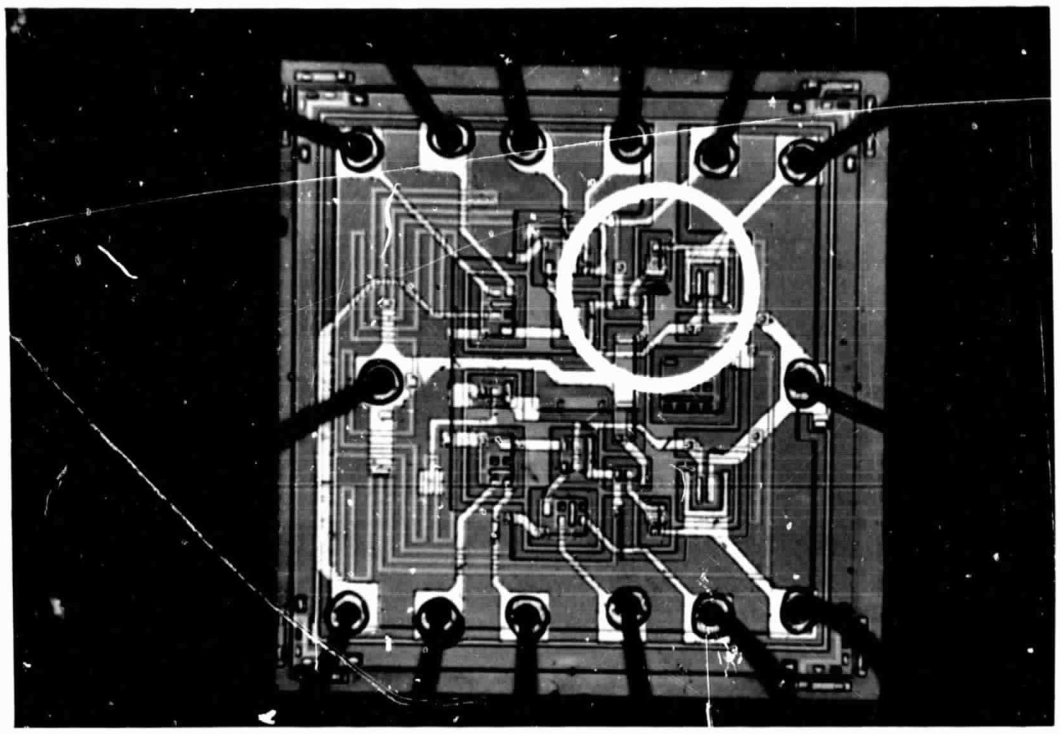
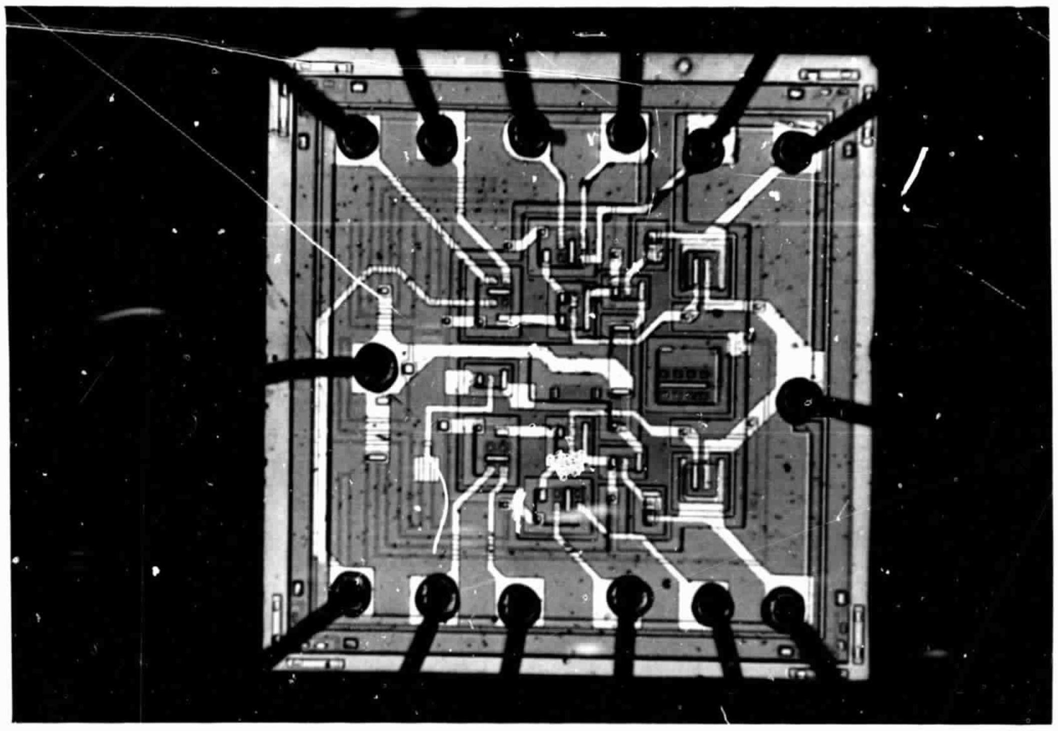


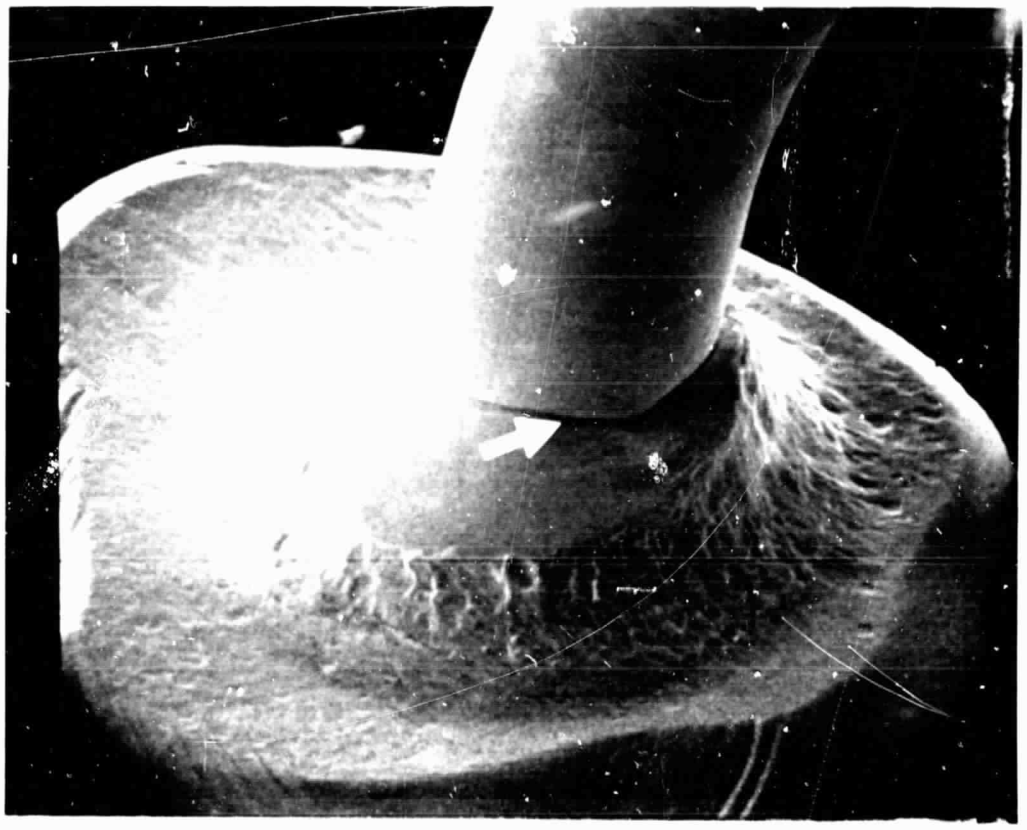
50X 1-5

FIGURE 30. TYPE SN54L51 MICROCIRCUIT, SPECIMEN 21, SHOWING LARGE FOREIGN PARTICLE ON DIE SURFACE



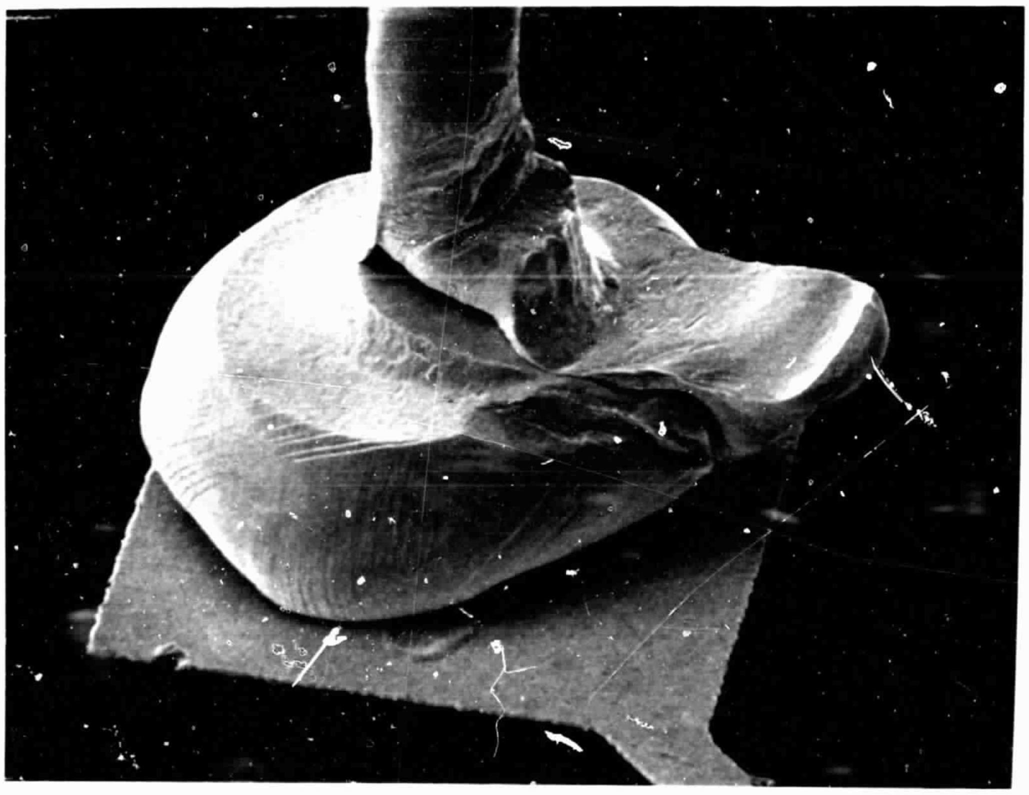
50X 1-8

FIGURE 31. TYPE SN54L51 MICROCIRCUIT, SPECIMEN 24, SHOWING GOLD FLECKS OVER WHOLE DIE SURFACE



1000X S1117

FIGURE 32. BALL BOND IN SPECIMEN 24 SHOWING CRACK IN LEAD WIRE AT TOP OF BALL (SE)



670X S1130

FIGURE 33. DEFECTIVE BALL BOND IN SPECIMEN 23 (SE)

Wire Bonds on Posts

No defects were observed in this inspection step. All leads of all specimens were satisfactorily placed and adequately bonded.

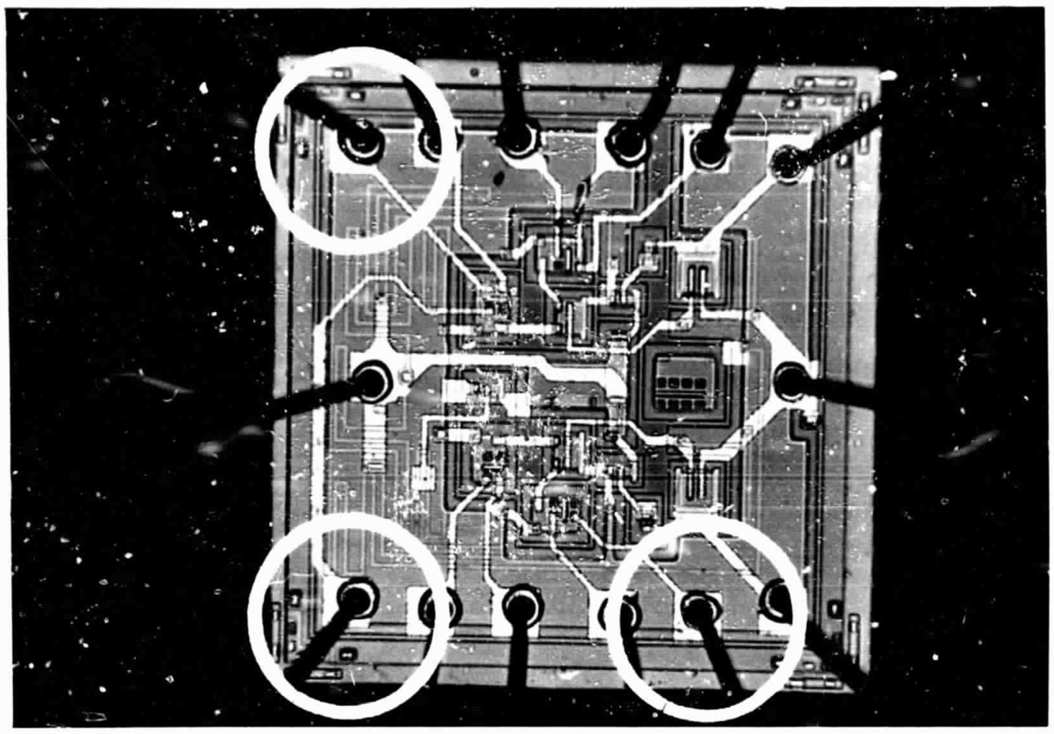
Wire Bonds on Pads

All ball bonds were well within the specified size and, with a few exceptions, were very satisfactorily placed on their pads. Specimen 22 exhibited three ball bonds so placed as to cover all or part of the fillet between the pad and the metal stripe emerging onto the circuit (Figure 34). Specimen 24 had one such ball bond (Figure 36) and one identified instance of a rebond (see circle in Figure 37).

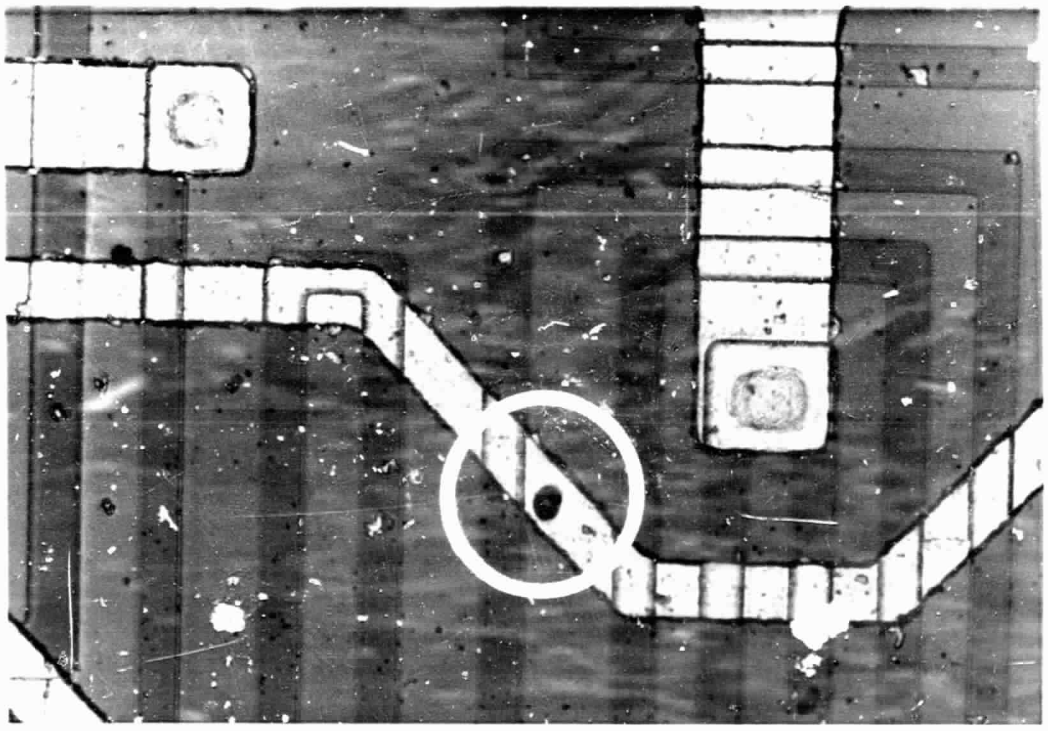
In the cross-sectioned specimen, no evidence was found of the lack of bonding, interdiffusion, or intermetallic-compound formation at the bond-to-metallization interface.

Metallization

The total metallization thickness was determined by interferometry to be 2.1 microns thick and to be essentially uniform over the whole die. From a cross-sectioned specimen, the molybdenum layer was determined to be approximately 20 percent of the total thickness or about 0.4 microns. Examination of the cross section in the scanning electron microscope showed that the bonds between the gold and molybdenum and the silicon dioxide were continuous. No evidence of poor bonding was found. Some evidence of undercutting along the edges of the metal stripes was observed in the scanning-electron-microscope studies. Figures 39 and 41 illustrate this to some degree. Figure C-5 in Appendix C substantiates this evidence clearly.



55X 1-6
FIGURE 34. TYPE SN54L51 MICROCIRCUIT, SPECIMEN 22, SHOWING THREE BALL BONDS (CIRCLES) OFFSET ON BONDING PAD AND COVERING METALLIZATION FILLET



500X 1-21
FIGURE 35. TYPE SN54L51 MICROCIRCUIT, SPECIMEN 24, SHOWING PHOTOLITHOGRAPHIC VOID IN METAL STRIPE IN SECTION G2

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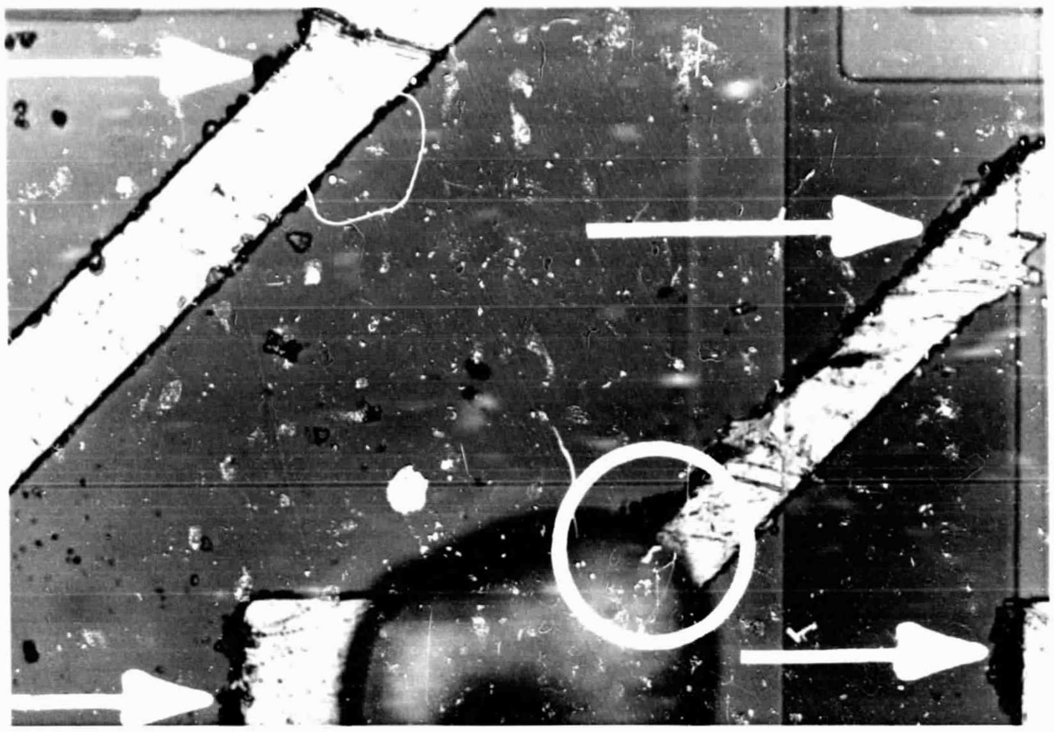
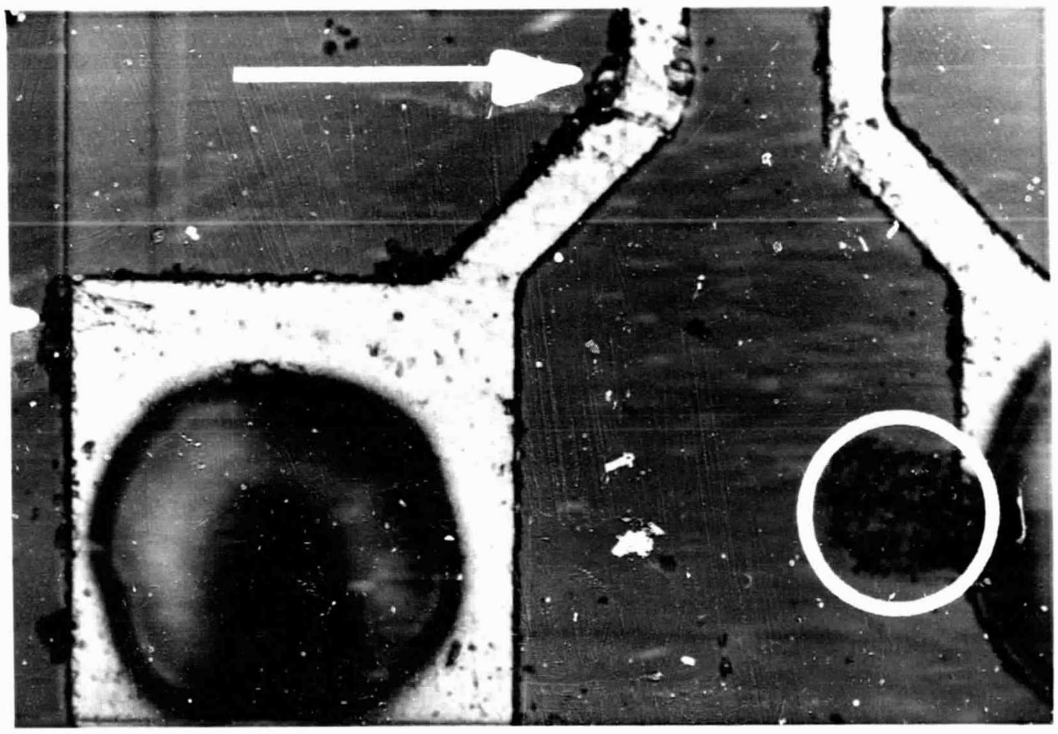


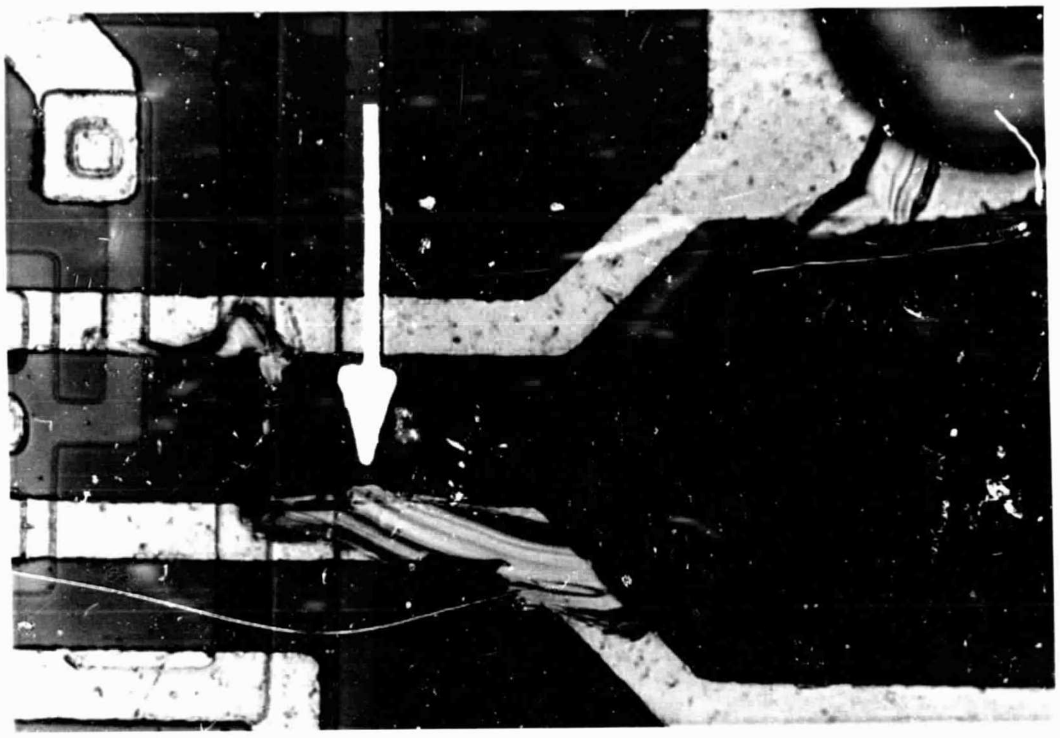
500X 1-19

FIGURE 36. TYPE SN54L51 MICROCIRCUIT, SPECIMEN 24, SHOWING ACCUMULATIONS OF FOREIGN MATERIAL AT EDGES OF METAL STRIPES (ARROWS) AND BALL BOND OVER METALLIZATION FILLET (CIRCLE) IN SECTIONS H7, H8, I7, AND I8



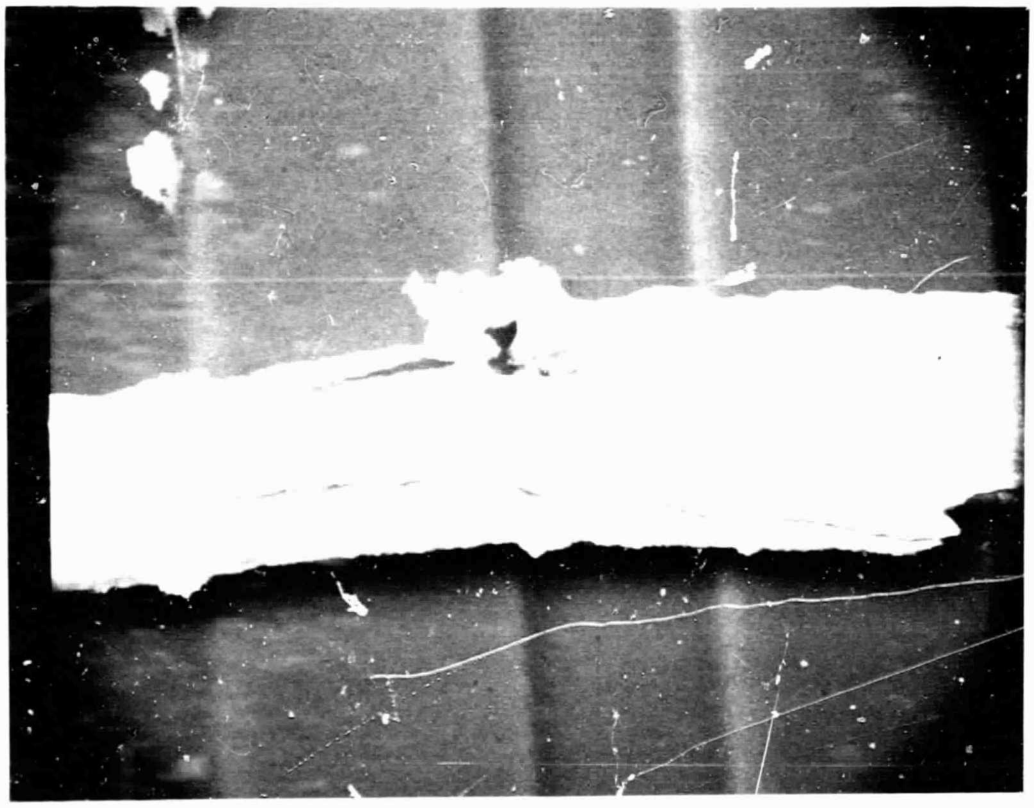
500X 1-17

FIGURE 37. ADJACENT VIEW TO FIGURE 36 SHOWING FOREIGN MATERIAL (ARROWS) AND FALSE BALL BOND STRIKE (CIRCLE) IN SECTIONS I5, I6, J5, AND J6



500X 2-5

FIGURE 38. TYPE SN54L51 MICROCIRCUIT, SPECIMEN 22, SHOWING DEEP SMEAR IN METALLIZATION CAUSED BY BALL BOND IN SECTIONS I5, I6, AND J5

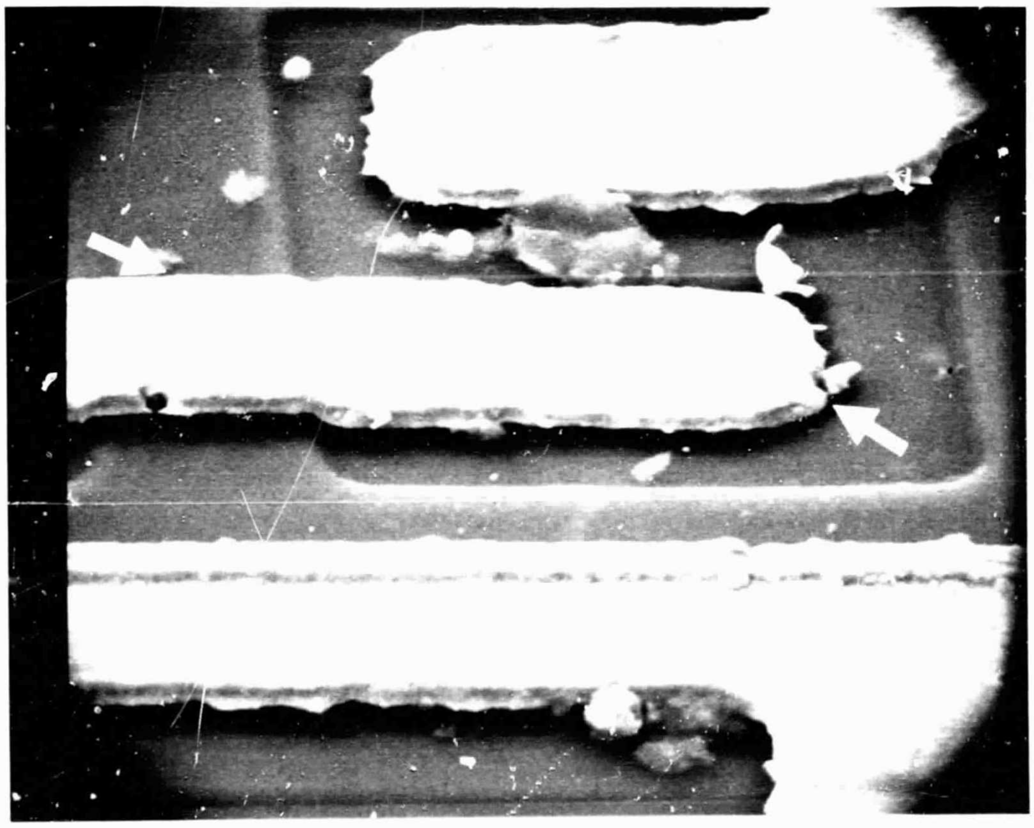


2000X S1354

FIGURE 39. DETAILED VIEW OF FIGURE 38 SHOWING SMEARED METAL STRIPE (SE)

500X S1114

FIGURE 40. TYPE SN54L51 MICROCIRCUIT, SPECIMEN 24, SHOWING COSMETIC SCRATCHES ON METALLIZATION IN SECTIONS F5, F6, G5, AND G6. (SE)



2000X S1123

FIGURE 41. DETAILED VIEW OF COSMETIC SCRATCHES IN FIGURE 40 (SE,

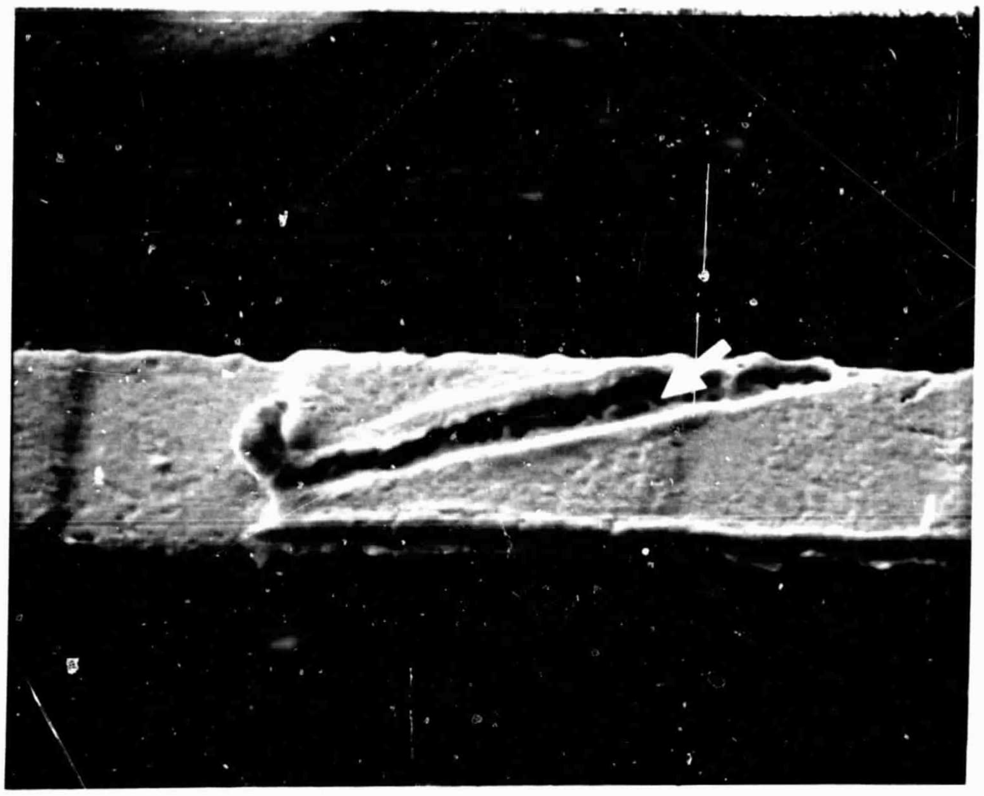
The definition and alignment of the metallization pattern on the die was very good. Window coverage as a function of pattern alignment was excellent. No bridging due to photolithographic problems was observed; only one instance of a photolithographic void was observed (Figure 35).

Induced damage in the form of scratches and smears was the major metallization problem in these specimens. The source of this damage appeared to be twofold: (1) deep scratches and major smears caused mostly by gold balls being dragged across the surface during ball bonding of the internal lead wires, and (2) minor scratches caused by face-down sliding of the loose chips, and shallow nicks probably caused by collision with the sharp corners and edges of other loose chips. Serious damage such as described in Item 1 above is typified in Figures 38 and 39. In most cases the damage inflicted in Item 2 was of a cosmetic nature (Figures 40 and 41). But where hard particles were present between the die face and the sliding surface, damage such as seen in Figures 42 and 43 resulted.

Further evidence of face-down sliding of the loose chips is shown by the accumulation of debris, mostly organic, along the vertical surfaces of the metal stripes (Figures 36 and 37). Not all such accumulations were organic, however. Figure 43 shows the presence of numerous nodules of corrosion growth along the edge and over the damaged areas of the metal stripes. This type of corrosion was identified in Specimens 21, 23, and 24. The amount of the corrosion in these specimens was not extensive at the time of inspection.

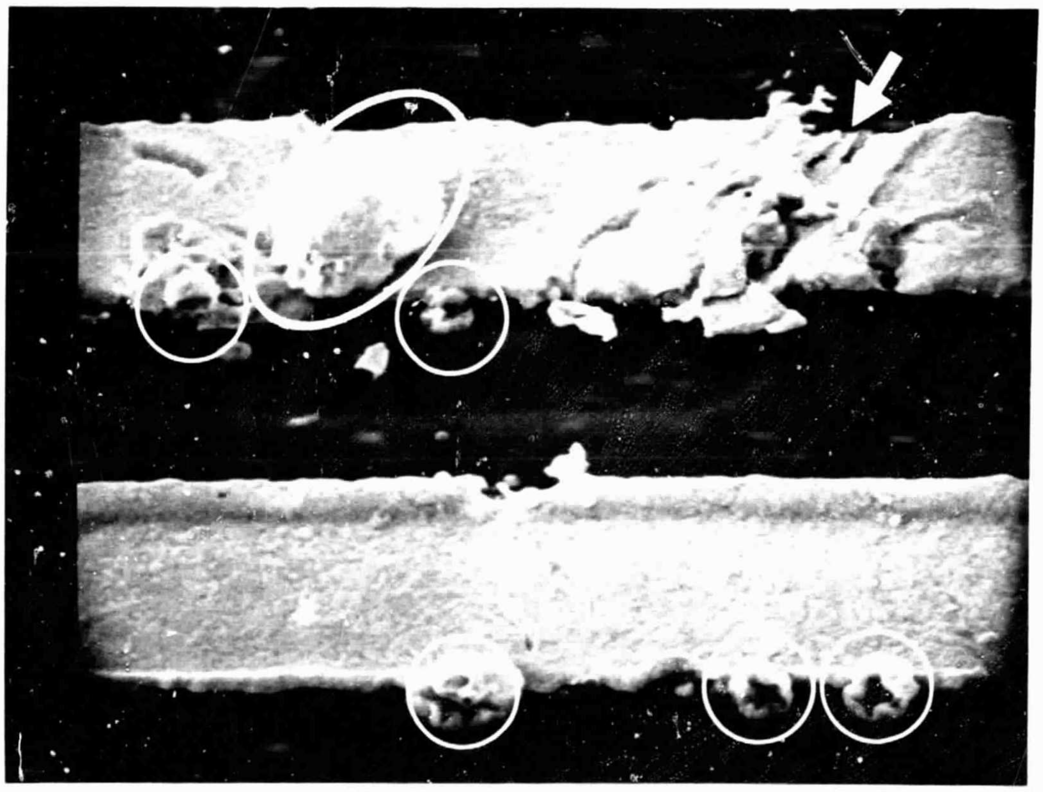
Windows

No direct evidence of inherent window problems was observed, i.e., cracks at oxide steps or pits in the metallization. Specimen 25 exhibited



2000X S1351

FIGURE 42. TYPE SN54L51 MICROCIRCUIT, SPECIMEN 21, SHOWING DEEP SCRATCH IN METAL STRIPE IN SECTION H5 (SE)



2000X S1125a

FIGURE 43. TYPE SN54L51 MICROCIRCUIT, SPECIMEN 23, SHOWING DEEP SCRATCH IN METAL STRIPE (ARROW) AND CORROSION GROWTH ALONG SIDE OF METAL STRIPES (CIRCLES) IN SECTIONS G5 AND G6 (SE)

granularity in the gold surface at the oxide step in the window cuts (Figure 44), which was not observed in other specimens of this type. The presence of the gold granules along the window-cut periphery could be indicative of cracks in the underlying molybdenum barrier layer at the top edge of the step.

Type SN54L78 and SN54L73 Flip-Flops
(Manufacturer B, Specimens 31 to 45)

From topographical appearances, the same basic silicon chip is used in both the Type SN54L78 and Type SN54L73 integrated circuits with appropriate changes in the metallized interconnect pattern providing the slightly different circuit functions. Due to the nearly identical construction and common origin of these two groups of specimens, they are discussed concurrently.

General

The packages used for these integrated circuits were the TO-86 hermetically sealed unit having exterior dimensions of 0.25 x 0.25 inch, metal lid and bottom, soldered lid-seal and glass lead-seals. Internally, the chips appeared to be bonded to the package floor with gold eutectic paste. Aluminum metallization, approximately 2.7 microns thick, was employed in the interconnect pattern on the die. These circuits used aluminum flying leads ultrasonically bonded both to the expanded aluminum contacts at the die periphery and to the gold-plated package lands.

Package Exterior

No major defects were observed during external visual inspection. Many lid seals showed discontinuities in the visible solder fillet along the seam when

1000X S1356

FIGURE 44. TYPE SN54L51 MICROCIRCUIT, SPECIMEN 25, SHOWING GRANULARITY IN METALLIZATION AT WINDOW CUT PERIPHERY IN SECTIONS G5 AND G6 (SE)

inspected at 30X. However, these apparent voids proved to be quite shallow when the lids were removed. The top edge of the package wall, 30 mils in width, was continuously solder coated and provided an adequate hermetic seal.

Package Interior

In all specimens, the chips were nominally centered in the package cavity, oriented correctly with respect to the package leads, and mounted flat to the package floor. Three specimens showed evidence of inadequate chip bond when viewed obliquely at 50X in the scanning electron microscope as illustrated in Figures 45 and 46. This evidence was not substantiated in the cross-sectioned specimens where the bond under the chip proved to be more than 90 percent continuous. The voids around the bottom edge of the chips were caused by an edge-chamfer effect which probably occurred when the wafer was scribed and separated.

Die Condition

The die surface of eight of the ten specimens in these two groups was free of both loose and attached foreign material. On the die of Specimen 41, there was an attached orange-colored translucent spot that bridged between three metal stripes over a transistor region (Figure 47). A similar but much smaller spot that did not bridge between metal stripes was observed in Specimen 34. The translucent nature of these spots is indicative of nonconductive material.

Of greater consequence in Figure 47 is the adjacent brown depression in the silicon dioxide surface which underlies the metallization stripe leading to the emitter contact of the transistor. This type of defect, i.e., oxide fault either partly or entirely underlying a metal stripe, was also observed on the dies

50X S1133

FIGURE 45. TYPE SN54L78 MICROCIRCUIT, SPECIMEN 34, SHOWING APPARENT VOID IN CHIP-BOND MATERIAL (SE)

50X S1373

FIGURE 46. TYPE SN54L73 MICROCIRCUIT, SPECIMEN 35, SHOWING APPARENT VOID IN CHIP BOND (ARROW) AND INADEQUATE CLEARANCE UNDER LEAD WIRES (CIRCLES) (SE)

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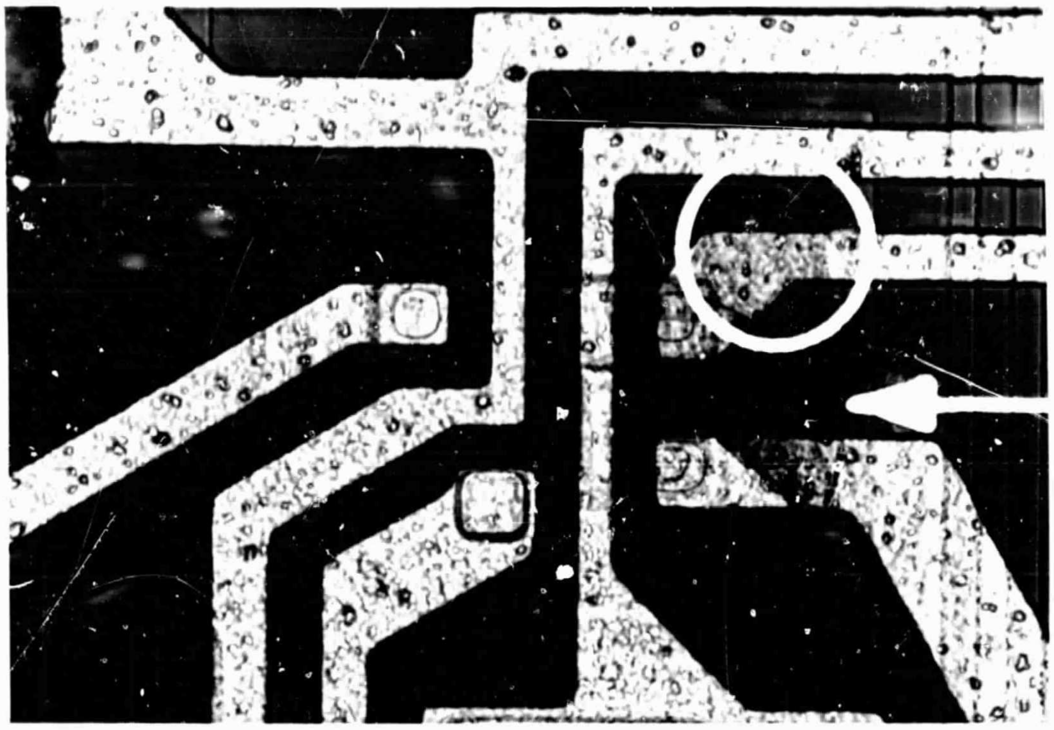
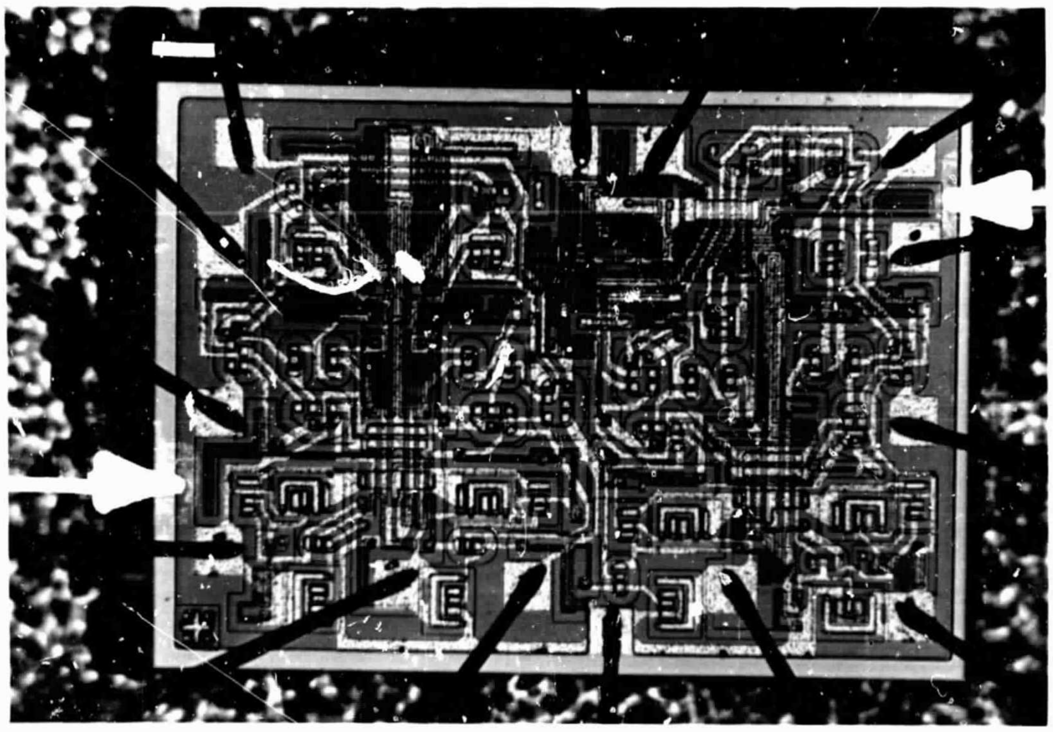


500X 6-3

FIGURE 47. TYPE SN54L73 MICROCIRCUIT, SPECIMEN 41, SHOWING ATTACHED FOREIGN MATTER (ARROW) AND OXIDE FAULT (CIRCLE) IN SECTION B2 AND C2



55X 5-8

FIGURE 48. TYPE SN54L73 MICROCIRCUIT, SPECIMEN 14, SHOWING GRADATION IN COLOR OF BOTH BACKGROUND AND DIFFUSIONS (ARROWS) FROM END TO END OF SILICON DIE

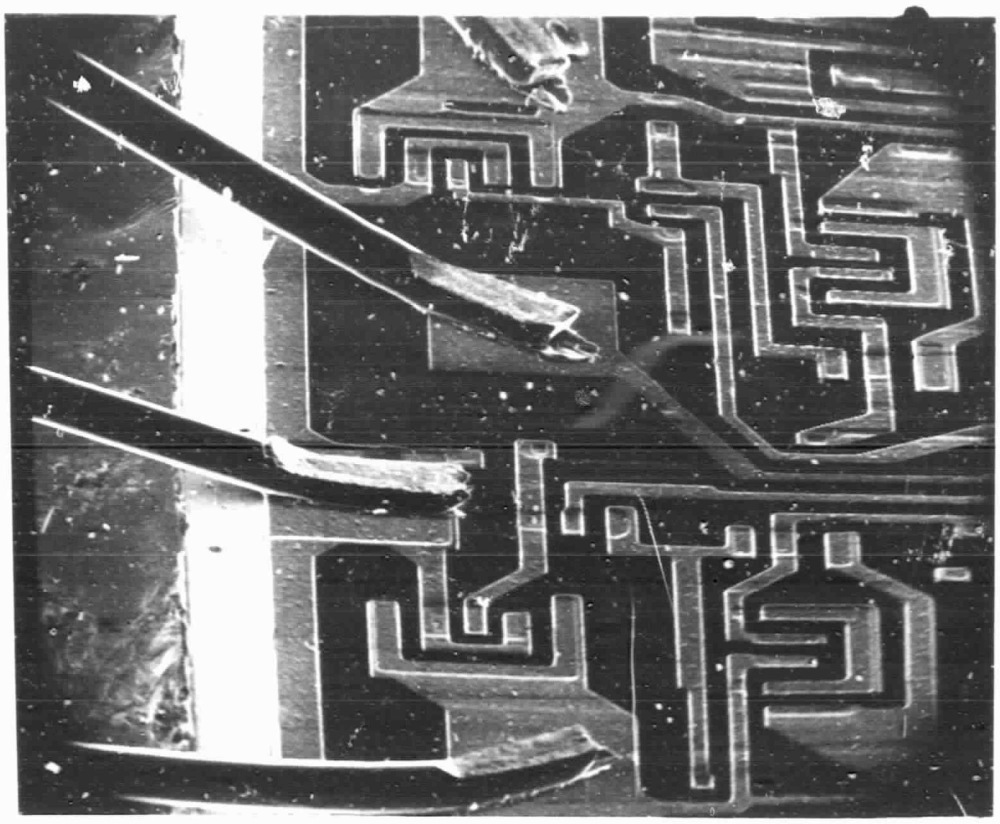
of Specimens 44 and 45. The degree of electrical contact in these oxide faults was not determined.

An unusual appearance was observed in the color of the die in Specimen 41 (Figure 48). The basic or background color of the silicon dioxide was green at one end of the die (Lead 1) and faded gradually to a gray color at the opposite end (Lead 7). The resistor diffusions at the green end were purple and these changed to a blue, then blue-green, and finally to a vivid green as the length of the die was traversed. The evidence suggests variation in the silicon dioxide thickness from one end of the die to the other.

Internal Lead Wires

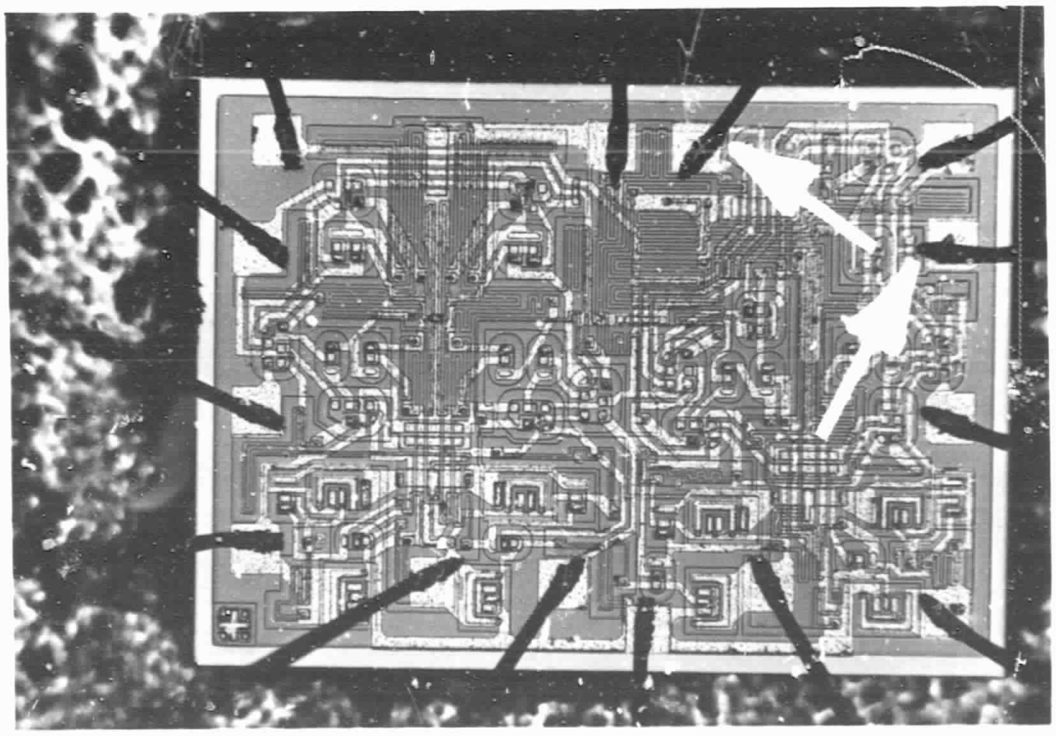
No defects were observed in the wires relative to nicking, scoring, cracking, necking, or looping. In fact, no lead-wire defects were observed in Specimens 31 to 35.

A potential defect was observed in Specimens 41 to 45 which is not specifically covered in the inspection criteria of MIL-STD-883, Method 2010. As shown in Figure 46, three bonding pads are located internal to the ground metallization stripes along the edge of the die. The lead wires to these pads must cross over and above the ground stripes to reach the posts of the package. In the figure, one lead appears to be very close to touching the ground stripe and another appears to clear it by approximately 1 mil. Figure 49 shows a 200X view of this same area rotated 90 degrees from the view in Figure 46. The low angle and close clearance of the leads are very apparent. All five specimens had 2 or 3 leads with clearances of less than 2 mils. Figure 45, a 50X SEM view of the die in Specimen 34, shows that it is possible to install Leads 9, 10, and 12 with adequate clearance.



200X S1146

FIGURE 49. TYPE SN54L73 MICROCIRCUIT, SPECIMEN 44, SHOWING LOW ANGLE AND CLOSE CLEARANCE OF LEAD WIRE OVER GROUND STRIPE IN SECTION E7 (SE)



55X 8-2

FIGURE 50. TYPE SN54L78 MICROCIRCUIT, SPECIMEN 32, SHOWING LEAD BONDS COVERING METALLIZATION FILLET (ARROWS) IN SECTIONS G1 AND I2

Wire Bonds on Posts

All wire bonds on the posts were satisfactorily placed and appeared to be adequately bonded. The bonds were almost uniformly one and one-half times the diameter of the lead wire.

Wire Bonds on Pads

On the whole, the wire bonds on the pads were properly placed and appeared to be adequately bonded. Exceptions to this would be the misplacement of the bonds on two pads in Specimen 32 (arrows in Figures 50 and 51), and on one pad in Specimen 35 (Figure 52). These three defective bonds were placed in proximity to the point from which the metal stripe leaves the pad causing an inadequate fillet of metal to show between the pad and the emerging stripe.

Another defect-prone characteristic of the bonds in these specimens is the "gouge" in the bonding pad just at the toe of the bond. This gouge appears to result from the ultrasonic scrubbing of the wire as the bond is formed. In most instances, it is of no consequence. But when the bond is lined up with an emerging stripe as in Specimen 32 (arrow in Figure 53), a defect results. This same scrubbing action produces disruption in the aluminum-pad surface at the periphery of the bonded wire. The nature of these perturbations can be ascertained in Figure 54 which shows the scuffed-up metal around the base of the bond. The top surface of the bonds in these circuits, while somewhat roughened, did not exhibit deep cracks or fissures.

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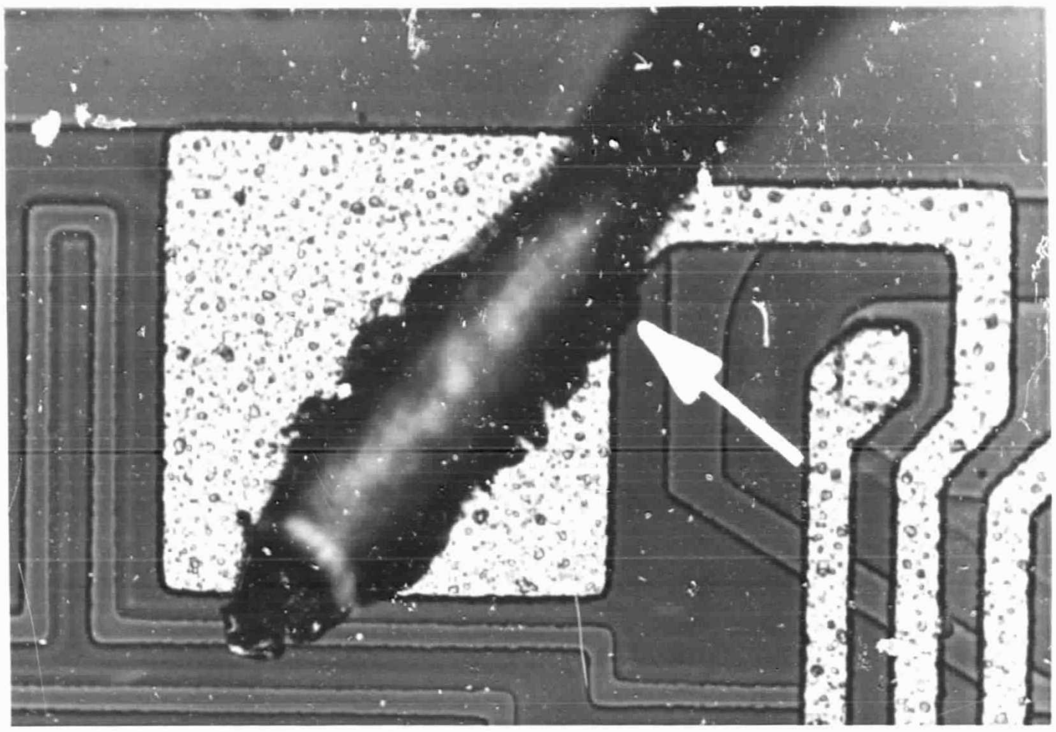
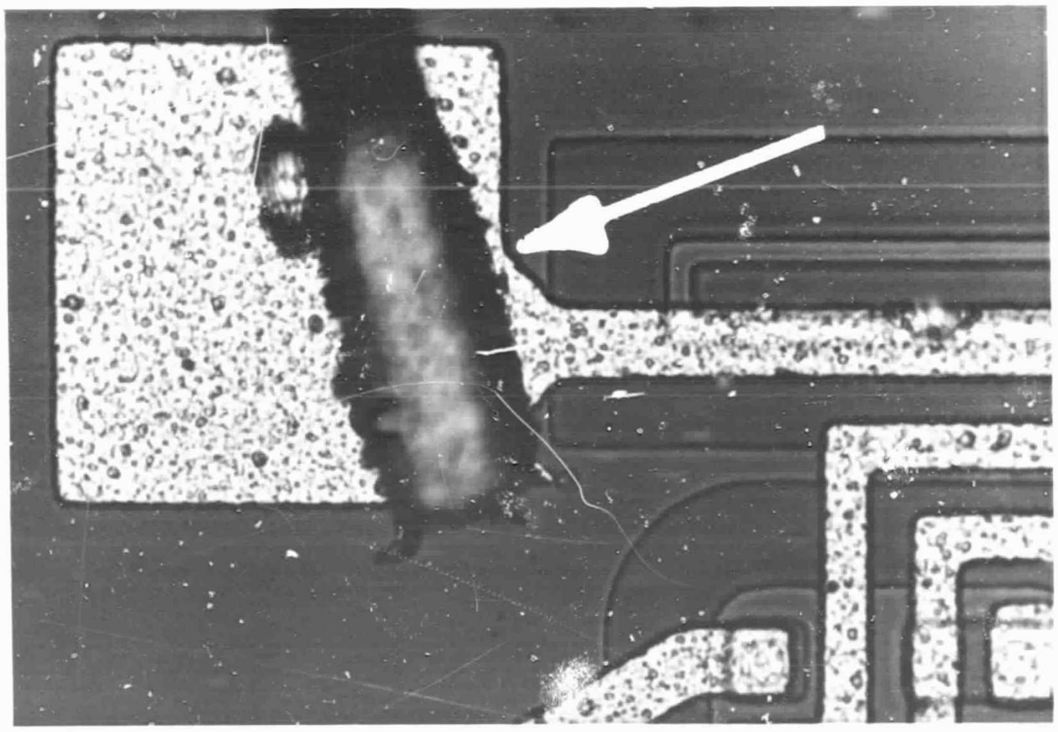


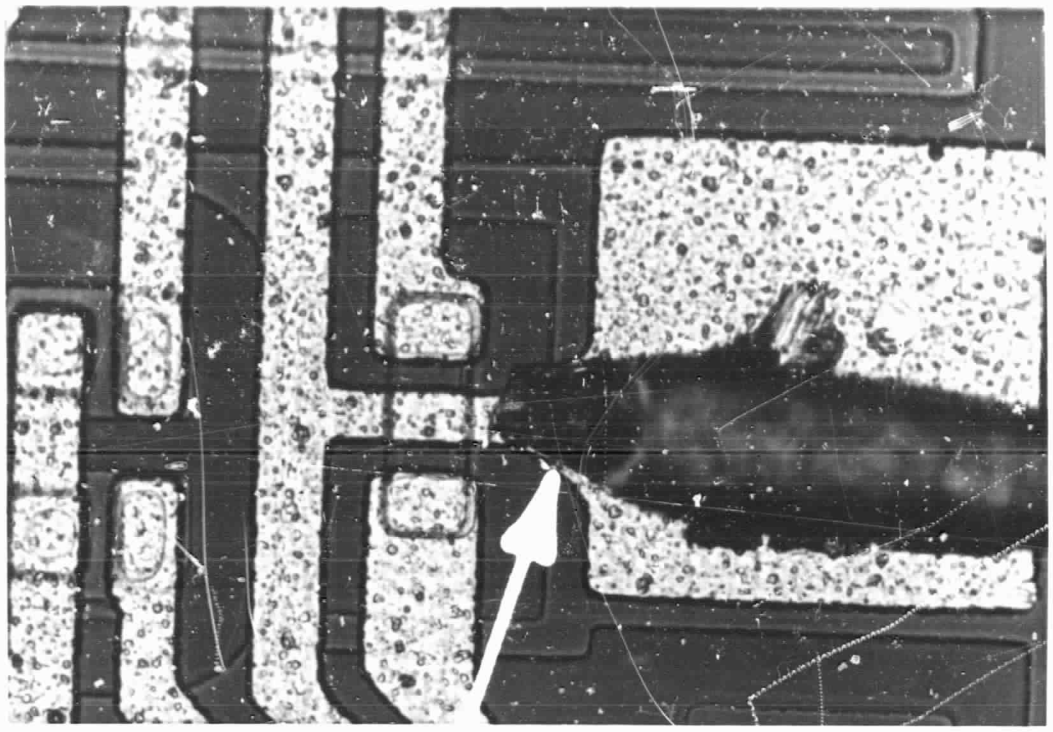
500X 7-3

FIGURE 51. TYPE SN54L78 MICROCIRCUIT, SPECIMEN 32, SHOWING LEAD BOND COVERING METALLIZATION FILLET IN SECTION G1



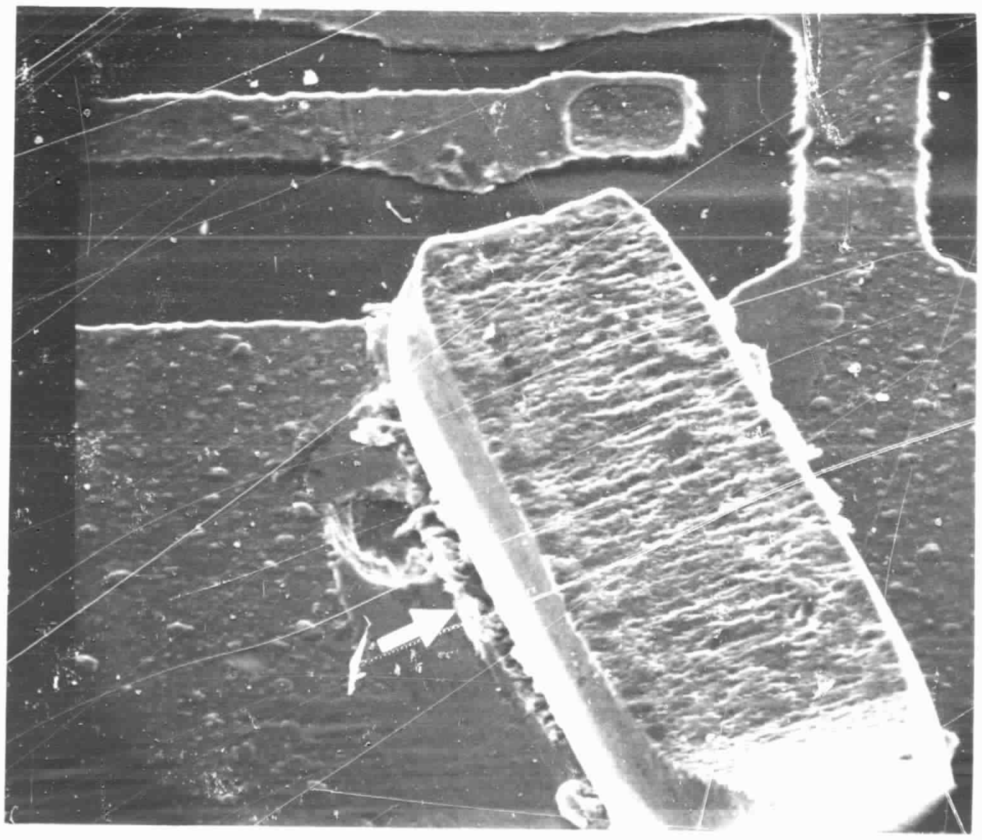
500X 6-13

FIGURE 52. TYPE SN54L78 MICROCIRCUIT, SPECIMEN 35, SHOWING LEAD BOND WITH INADEQUATE CLEARANCE AT METALLIZATION FILLET IN SECTION B1



500X 7-2

FIGURE 53. TYPE SN54L78 MICROCIRCUIT, SPECIMEN 32, SHOWING DAMAGE TO METAL STRIPE IN FILLET AREA IN SECTION I-3



1000X S1134

FIGURE 54. TYPE SN54L78 MICROCIRCUIT, SPECIMEN 34, SHOWING DISRUPTION IN ALUMINUM SURFACE OF BONDING PAD IN SECTIONS G6 AND G7 (SE)

Metallization

The metallization pattern was satisfactorily aligned on all dies in the two groups of specimens. When inspected optically with vertical illumination, window coverage appeared to be nearly 100 percent on all dies. In general, the interconnect pattern was very well defined and few photolithographic defects were found. Only one significant photolith void was observed, this in Specimen 41 (Figure 55). A near bridge due to induced damage was observed in Specimen 44 (Figures 56 and 57). It appears that the metal stripe had been "tooled" and the resulting chip was still attached to, but at a right angle to, the damaged stripe. Two photolith spurs were observed (Figure 58 shows one of these) but neither was considered to be a defect.

The few smears observed in the ten specimens were principally of a cosmetic nature (Figure 59). An exceptionally massive smear was located near Bonding Pad 12 of Specimen 34 (Figures 60 and 61) which resulted in one stripe in the smear area being scribed deeply. This defect is shown more clearly in the SEM view in Figure 62. It is estimated that the cross section of the stripe is reduced to less than one-half the designed cross section through the region of the deep scratch.

Windows

The greatest potential problem in the SN54L78 and SN54L73 integrated circuits is in the metallization at the window cuts. Evidence of defects was observed in three of the SN54L78 circuits and all five of the SN54L73 circuits. Six different types of window defects that were observed could be traced to three areas of fabrication processes: (1) metal deposition, (2) pattern definition,

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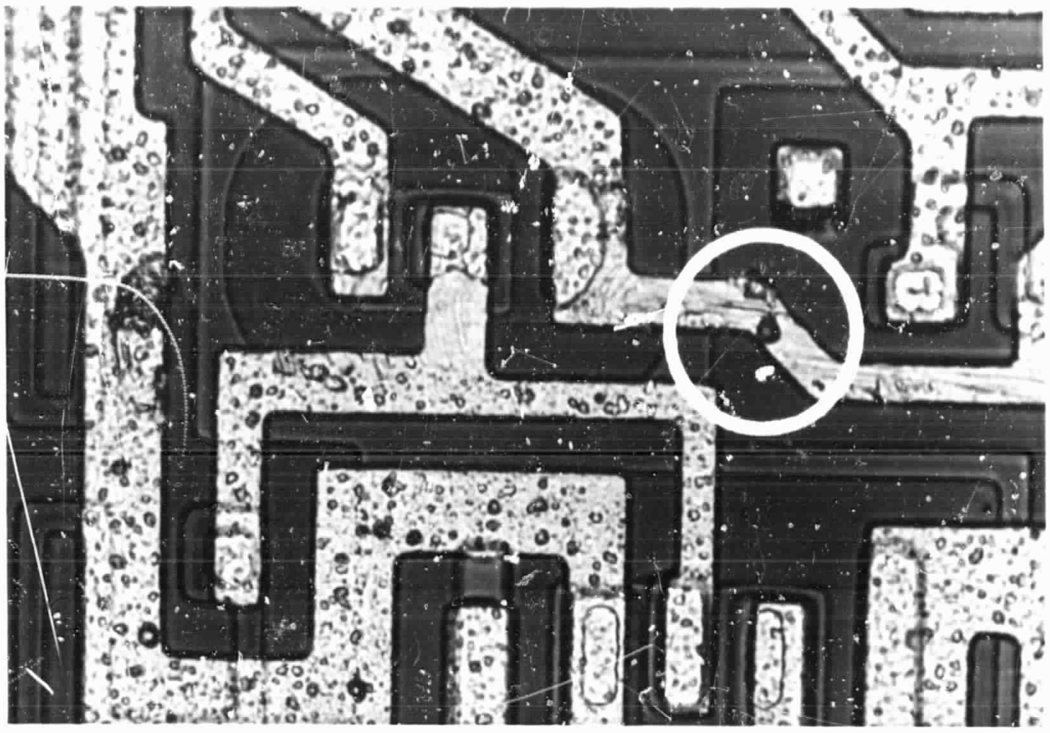
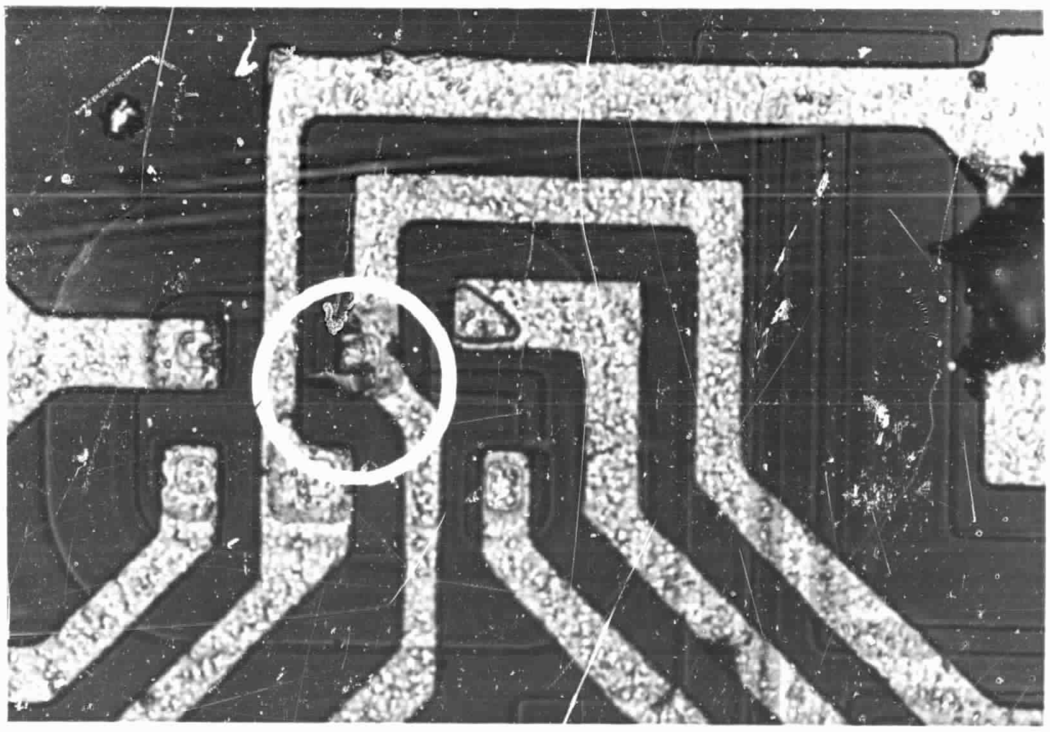


500X 6-1

FIGURE 55. TYPE SN54L73 MICROCIRCUIT, SPECIMEN 41, SHOWING PHOTOLITHOGRAPHIC VOID IN METAL STRIPE IN SECTION I6



500X 5-17

FIGURE 56. TYPE SN54L73 MICROCIRCUIT, SPECIMEN 44, SHOWING SPUR ON METAL STRIPE FROM INDUCED DAMAGE IN SECTIONS A3 AND A4

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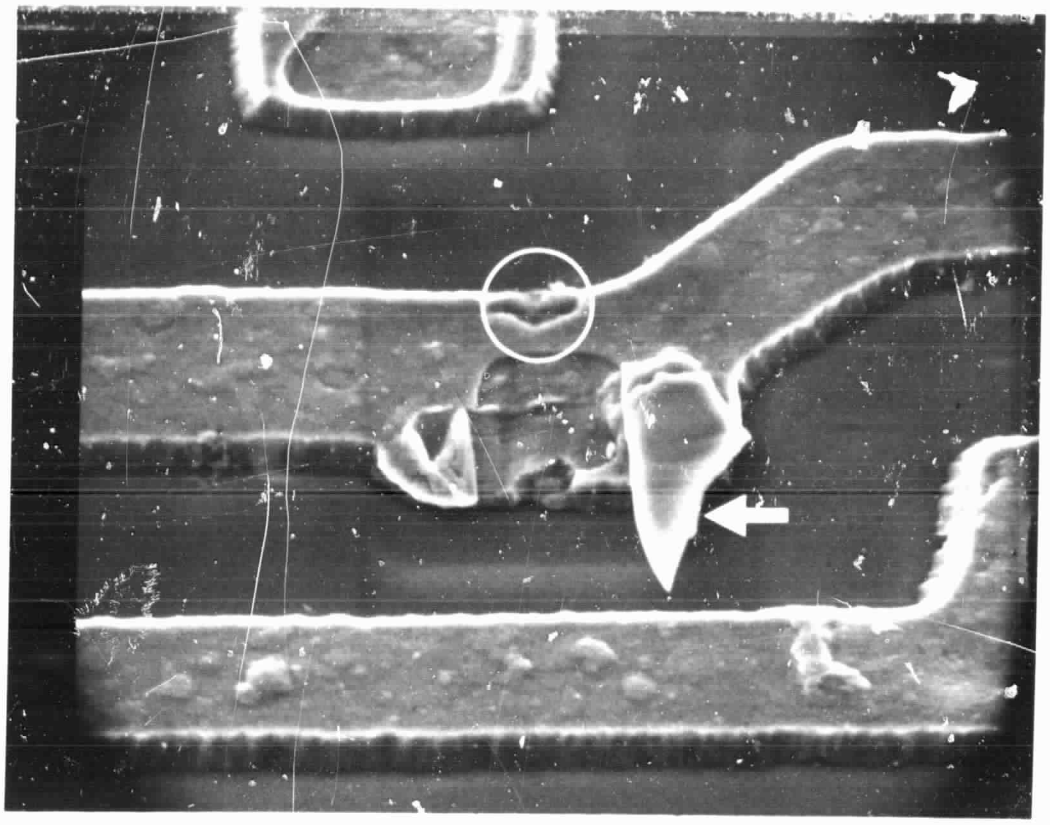
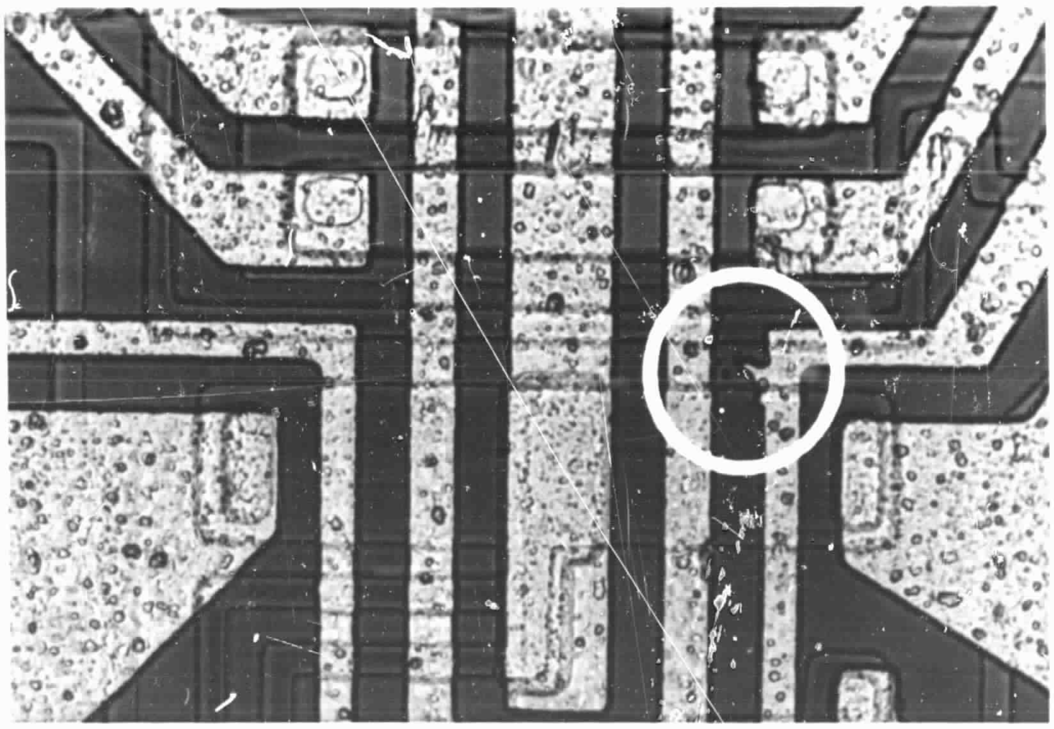


2000X S1142

FIGURE 57. DETAILED VIEW OF THE METAL SPUR (ARROW) IN FIGURE 56 AND ADJACENT ETCH PIT (CIRCLE) (SE)



500X 6-2

FIGURE 58. TYPE SN54L73 MICROCIRCUIT, SPECIMEN 41 SHOWING PHOTOLITHOGRAPHIC SPUR IN SECTION H5

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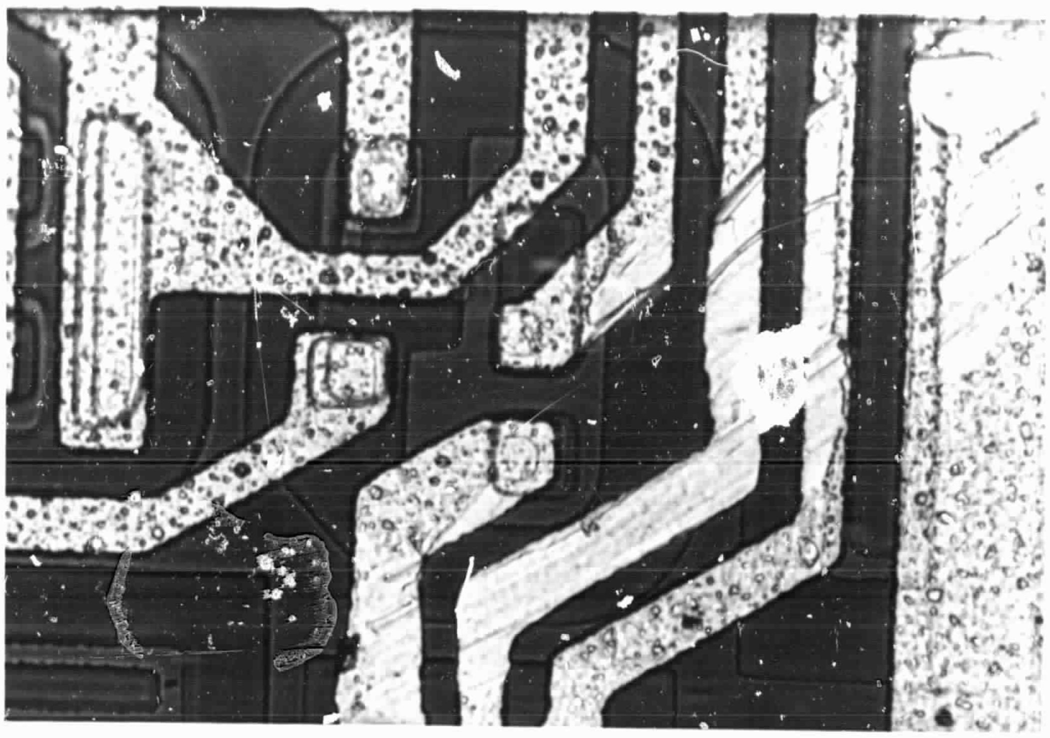
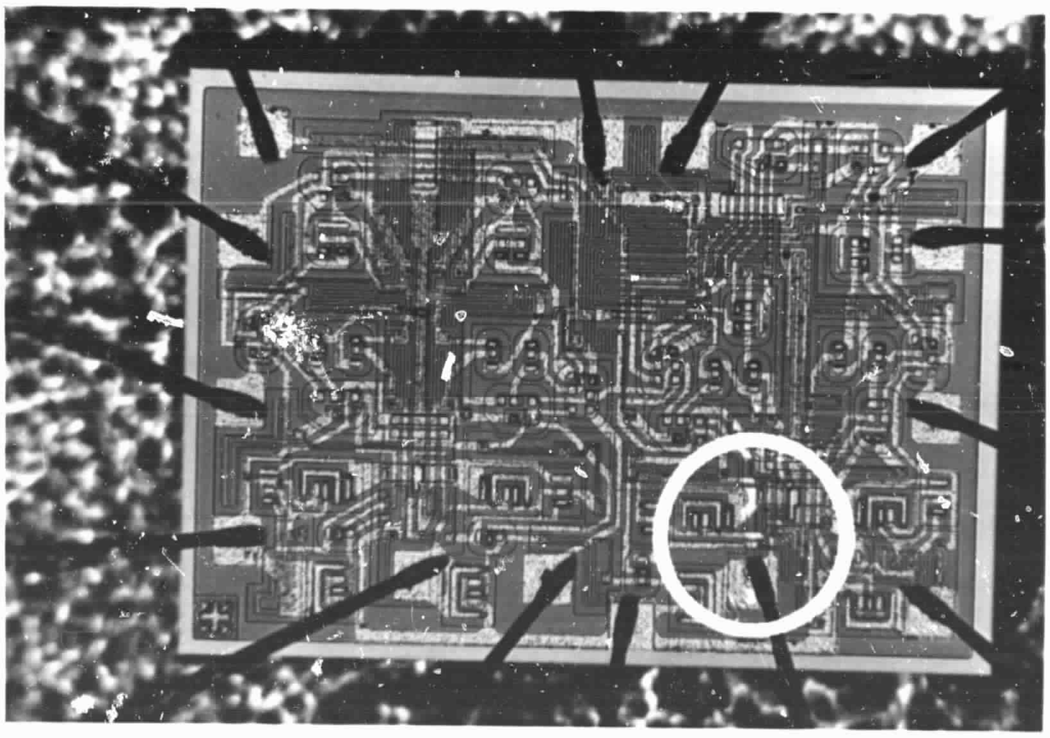


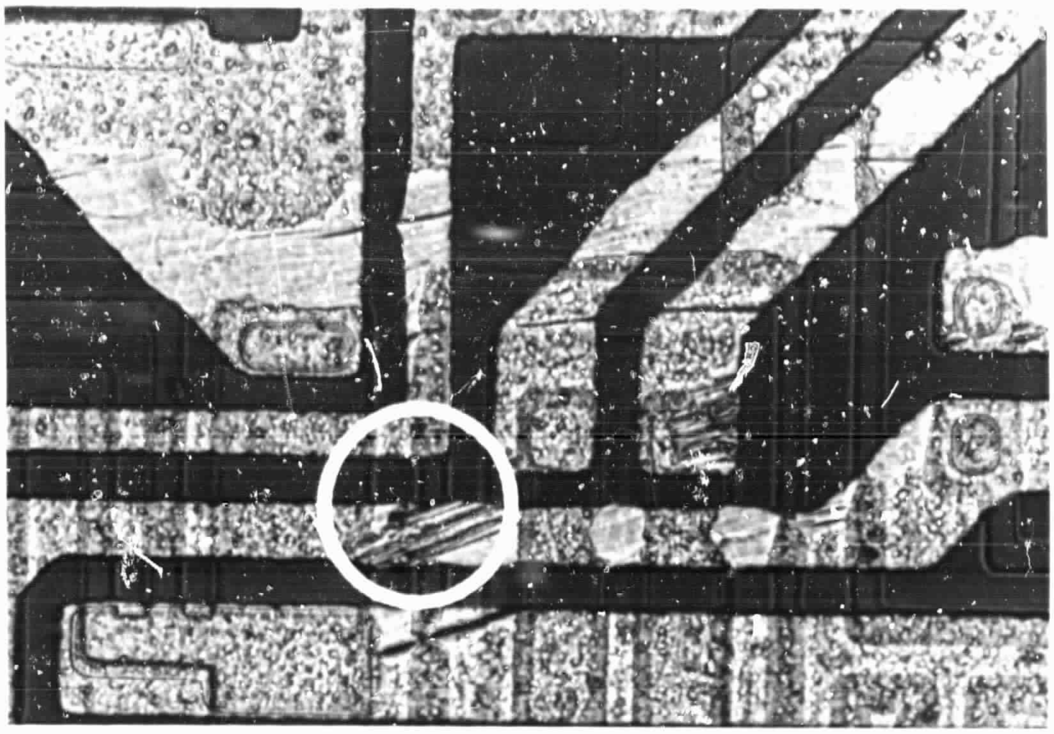
500X 7-9

FIGURE 59. TYPE SN54L78 MICROCIRCUIT, SPECIMEN 34, SHOWING COSMETIC TYPE SMEAR IN METALLIZATION IN SECTIONS D1, D2, E1 AND E2



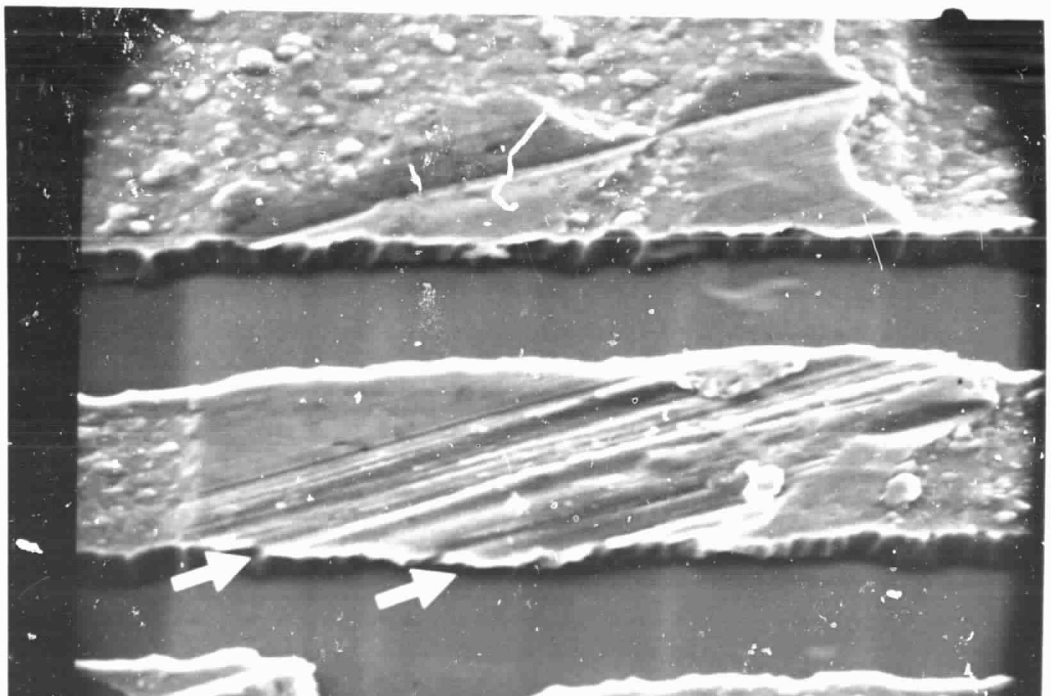
55X 5-4

FIGURE 60. TYPE SN54L78 MICROCIRCUIT, SPECIMEN 34, SHOWING DEFECTIVE TYPE SMEAR IN METALLIZATION IN SECTIONS G5, G6, H5, AND H6



500X 6-15

FIGURE 61. DETAILED VIEW OF MOST SERIOUS AREA OF SMEAR IN FIGURE 60



2000X S1136

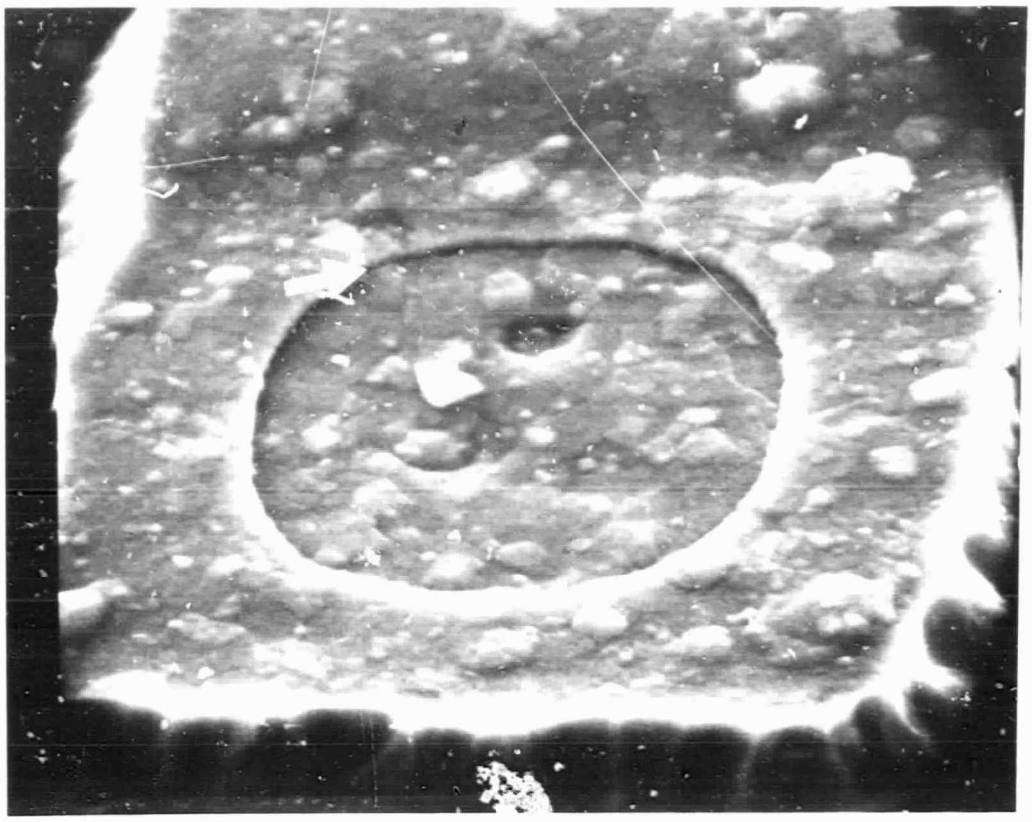
FIGURE 62. SCANNING MICROGRAPH OF SCRATCH IN METAL STRIPE ENCIRCLED IN FIGURE 61 (SE)

(3) chip handling. The occurrence of defects under the first two items was much more frequent than under the third.

Metal Deposition. One of the two types of defects traceable to this fabrication step is cracking in the metal at the oxide step in the window cut. Specimens 34, 35, and 41 through 45 showed evidence of this type defect. The condition was general over the whole die. Figure 63, a 5000X SEM view of a Specimen 35 window, shows a crack that extends the distance across the far side of the window. A 90-degree rotated view of this window showed the crack continuing around the adjacent side. Figure 64 is a 10,000X view of a similar window on Specimen 45.

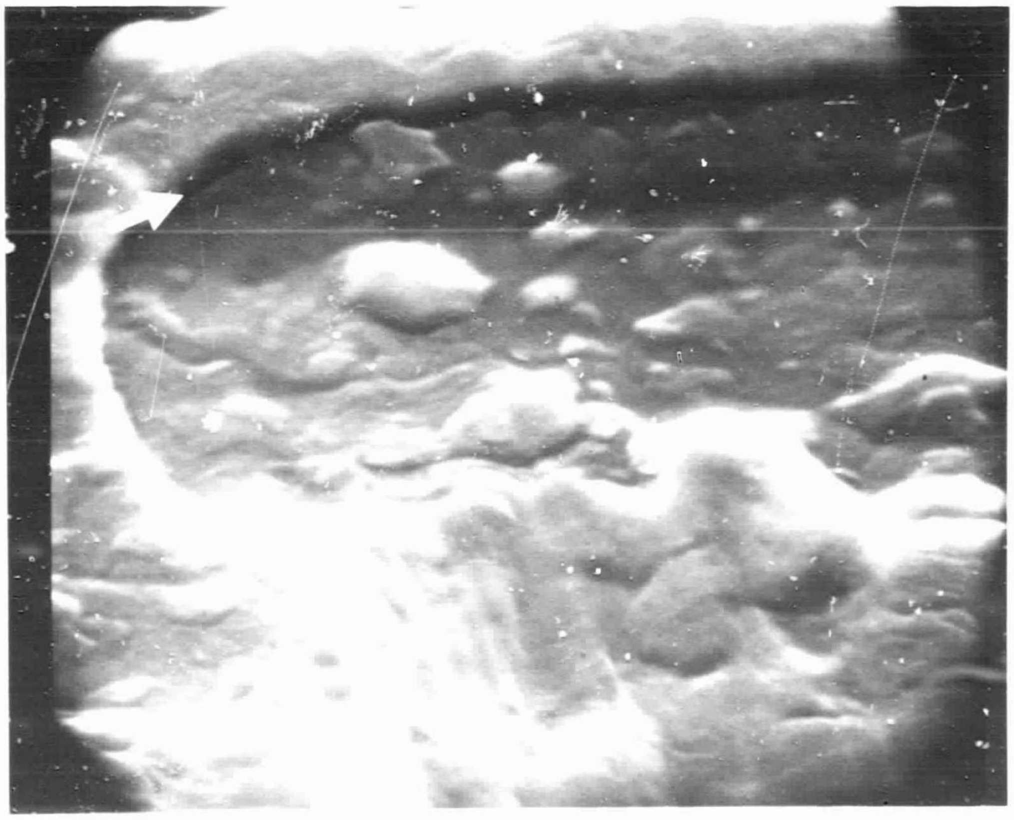
The other type of defect was porosity in the metal at the oxide step. Figure 65 is a general view of a section of Specimen 33. Figure 66 is a 5000X SEM view of one afflicted window and Figure 67 is a 10,000X close-up of the same window. Only Specimen 33 exhibited this unusual effect at the windows.

Pattern Definition. Two types of defects were traceable to the etching step used to define the interconnect pattern. Tunneling into the side of the metallization at contact window cuts was observed as shown in Figure 68. This type of defect occurred where the interconnect pattern was slightly offset on the die. It appears that the tunnel followed the contact-cut periphery. This suggests that some defect, such as a deep fissure, already existed in the metal at the oxide step and that the etchant followed the fissure and widened it. The crack-like appearance in the top surface of metallization in Figure 68 is not unlike that seen so clearly in Figures 63 and 64. Specimens 42 and 43 exhibited this tunneling defect. Etch-like pits were seen at several windows on Specimen 44. These can



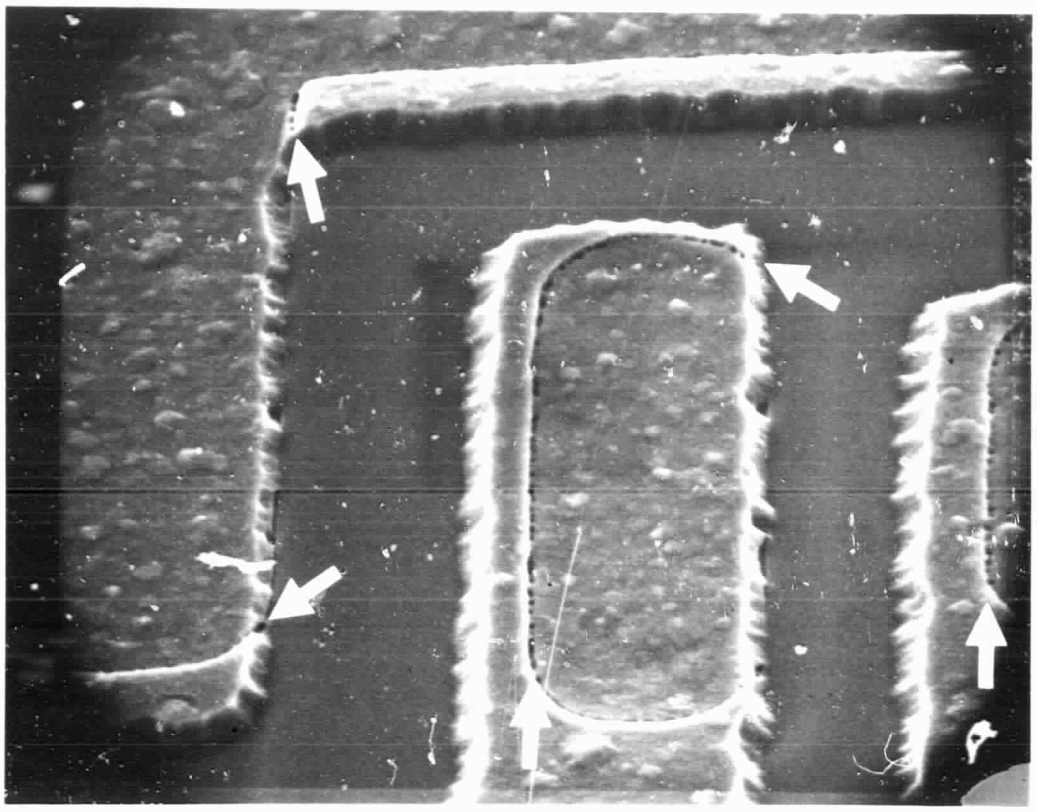
5000X S1368

FIGURE 63. TYPE SN54L78 MICROCIRCUIT, SPECIMEN 35, SHOWING CRACK IN METALLIZATION AT OXIDE STEP IN WINDOW CUT (SE)



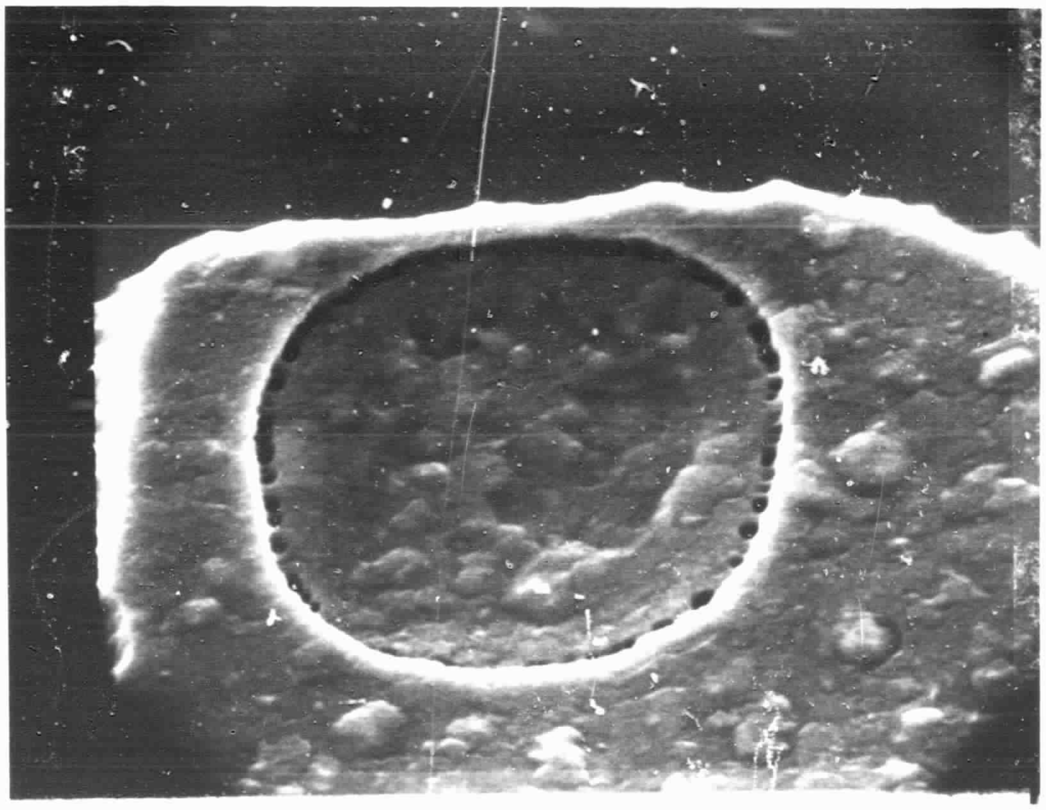
10,000X S1379

FIGURE 64. TYPE SN54L73 MICROCIRCUIT, SPECIMEN 45, SHOWING CRACK IN METALLIZATION AT OXIDE STEP IN WINDOW CUT (SE)



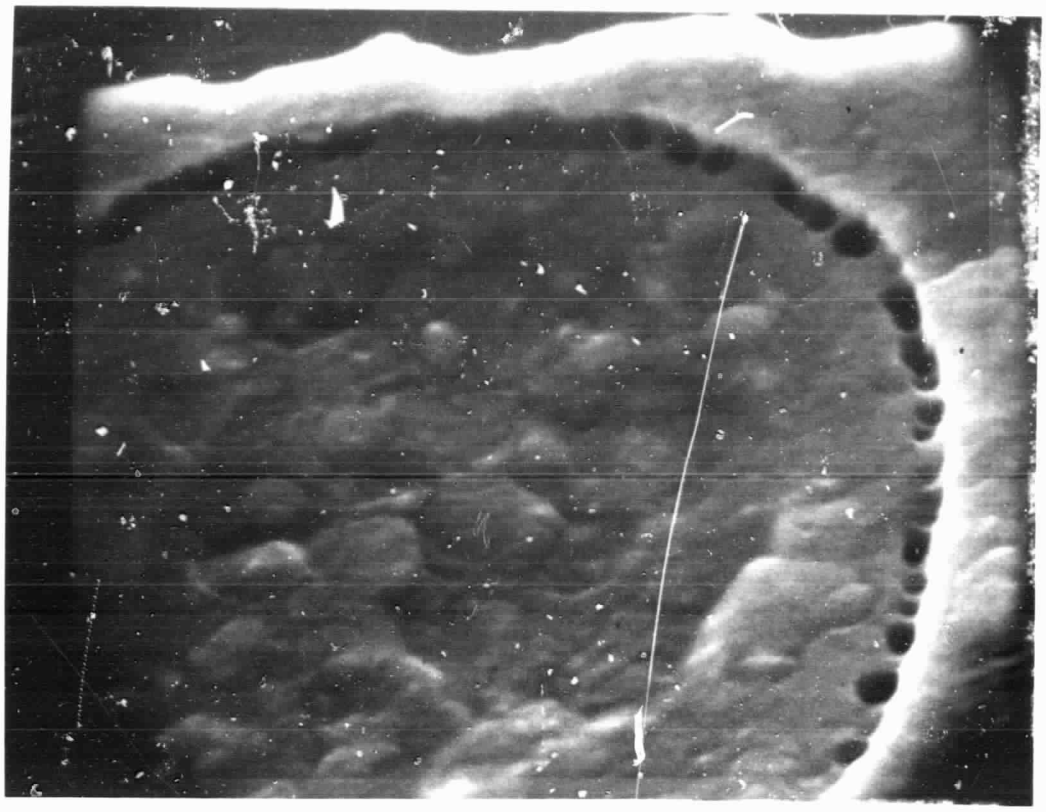
2000X S1364

FIGURE 65. TYPE SN54L78 MICROCIRCUIT, SPECIMEN 33, SHOWING POROSITY IN METALLIZATION AT OXIDE STEP IN WINDOW CUT (SE)



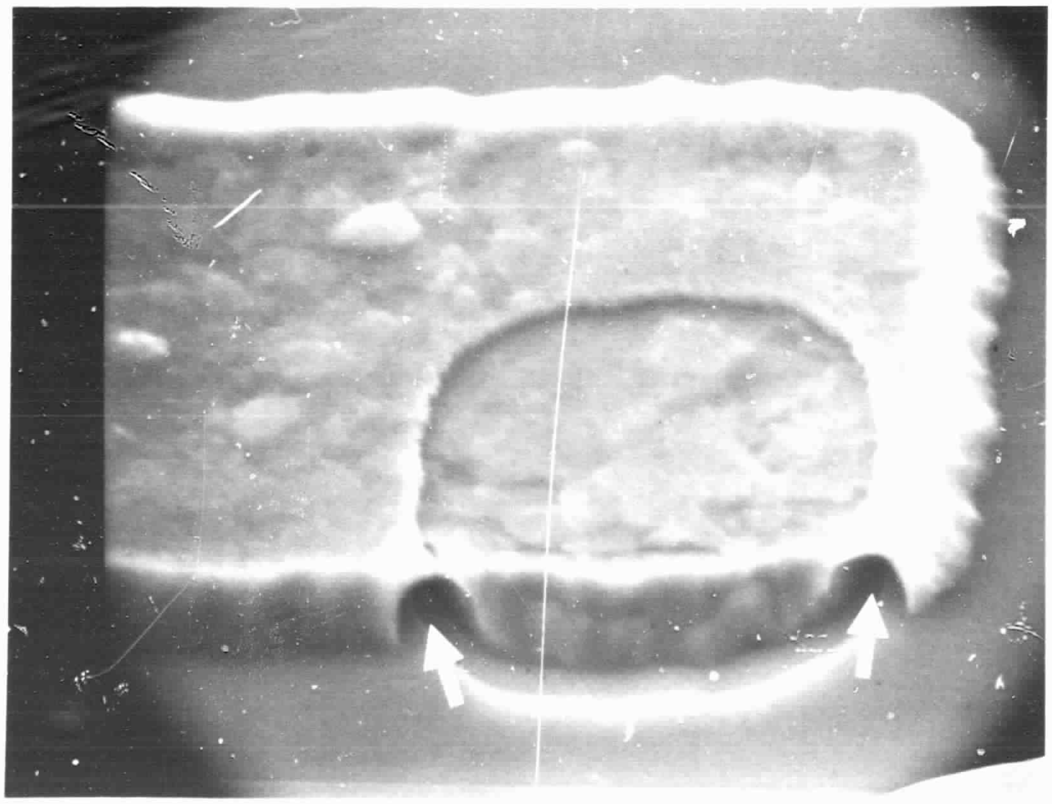
5000X S1366

FIGURE 66. POROSITY IN METALLIZATION OVER SINGLE SMALL WINDOW OF SPECIMEN 33 (SE)



10,000X S1365b

FIGURE 67. DETAILED VIEW OF POROSITY IN METALLIZATION OVER WINDOW SHOWN IN FIGURE 66 (SE)



5000X S1376

FIGURE 68. TYPE SN54L73 MICROCIRCUIT, SPECIMEN 42, SHOWING TUNNELING IN SIDE OF METAL STRIPE AT CONTACT WINDOW (SE)

be seen in Figures 57 and 69. The appearance of these suggests photolithographic problems. Frequency of occurrence was small.

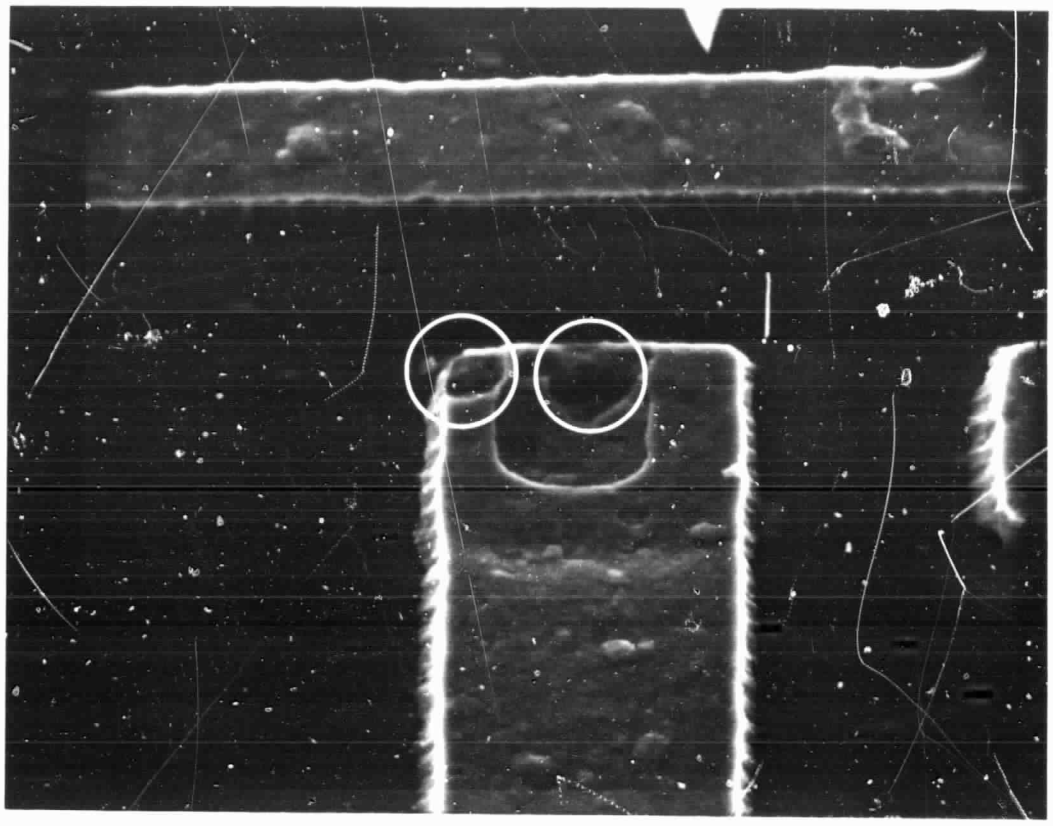
Chip Handling. Only a few defects traceable to chip handling were observed. Figure 57 which has previously been discussed, shows the thinning of the metallization over a window from induced damage. This small-area chipping and scuffing of the metallization was seen in other regions on the same die. Figure 70 shows five such minor damage points that proved to be curled up corners and edges on the metal stripes. Figure 71 shows damage at a window due to scouring by a small foreign particle.

ANALYSIS

Defects having potential to cause device failure were observed in all four circuit types. The most serious problems in the two circuit types from Manufacturer A were cracks in lead wires at ball bonds, scratched metallization, necking in lead wires, and improper ball-bond size and placement. Manufacturer B microcircuits had problems in the metallization at the contact window cuts. The Type SN54L78 circuits had less problems as a group but even these can not be considered to be completely free of manufacturing defects.

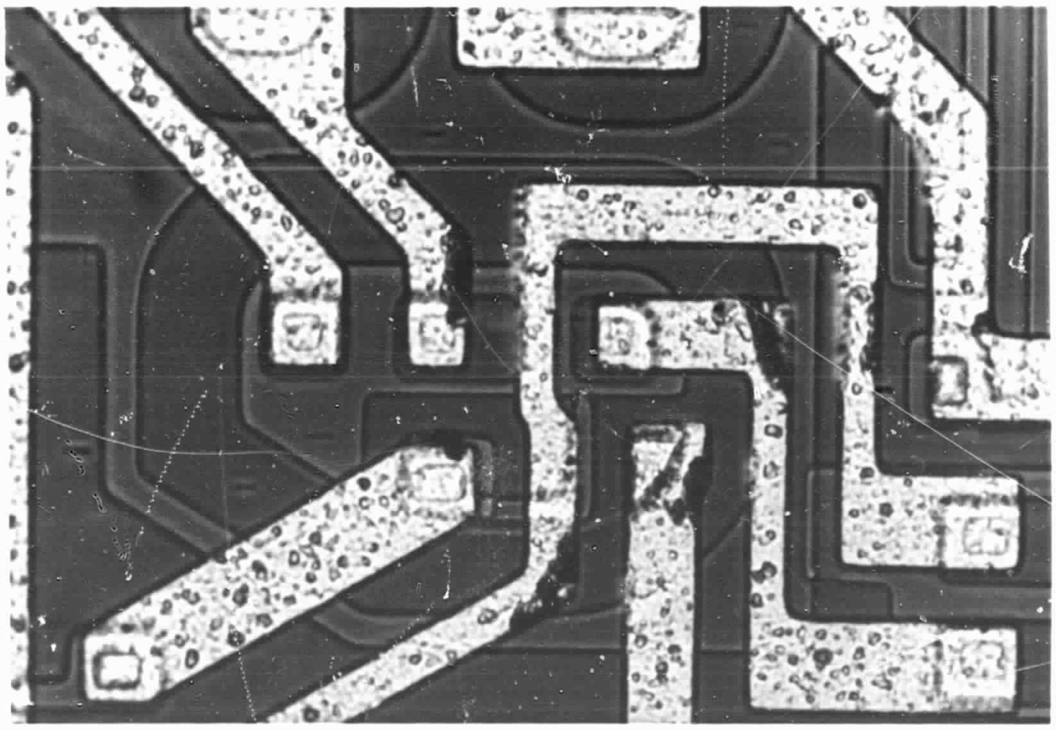
Manufacturer A Microcircuits

The most frequently observed defect in both the SN5451 and SN54L51 circuits (and the one considered to have the greatest potential for causing device failure) was the crack in the lead wire at the top of the ball bond. The environments most likely to cause device failure from this defect would be those involving shock, acceleration, and vibration, especially high-frequency vibration.



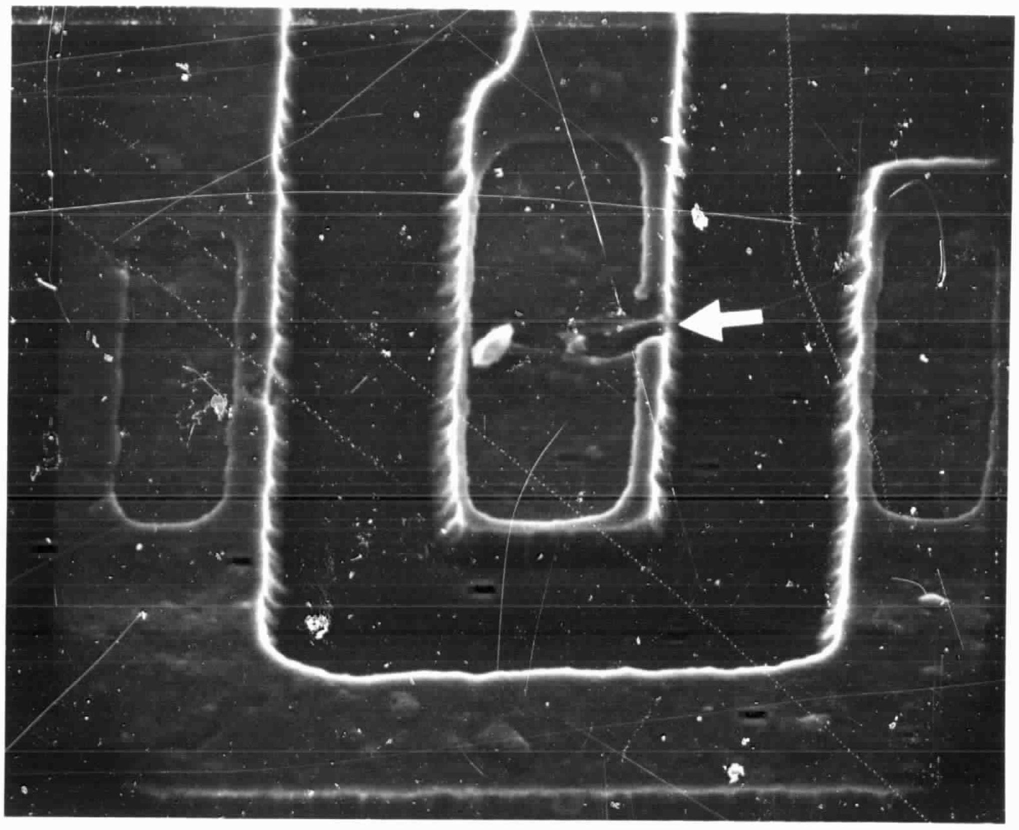
2000X S1143

FIGURE 69. TYPE SN54L73 MICROCIRCUIT, SPECIMEN 44, SHOWING ETCH-TYPE PITS IN METALLIZATION AT CONTACT WINDOW IN SECTION A4



500X 5-16

FIGURE 70. TYPE SN54L73 MICROCIRCUIT, SPECIMEN 44, SHOWING CHIPPING OF EDGES AND CORNERS OF METAL STRIPES IN SECTIONS B4, B5, C4, AND C5



2000X S1145-2

FIGURE 71. TYPE SN54L73 MICROCIRCUIT, SPECIMEN 44, SHOWING DAMAGE IN METALLIZATION AT WINDOW CAUSED BY FOREIGN PARTICLE IN SECTION I7 (SE)

The SN5451 circuits that use the single-layer aluminum metallization, showed more serious and more frequent scratch defects that did the SN54L51 curcuits which use the two-layer gold-over-molybdenum metallization. This is probably due more to the difference in workmanship between two production lines than to any superiority of one system over the other. Neither type of metallization showed any indication of peeling from the die surface where it was seriously marred. Nor did the gold show any tendency to separate from the molybdenum at deep scratches. The aluminum showed evidence of variation in process control while the gold-molybdenum system did not. In particular, the aluminum had a particular roughness in the contact window cuts, an appearance of brittleness, pits in the surface of the metal, and cracks in the metal at oxide steps.

A study of the metal roughness in the windows on one die showed that the windows in the p-type regions (bases, anodes, and resistors) appeared to have a rougher surface than the windows in the n-type regions (emitters, collectors, and cathodes). Based on published information(1), it is hypothesized that the observed roughness of the metallization surface in the windows indicates over-alloying of the aluminum and silicon due to excessive temperature or inadequate controls during the alloying step. Silicon dissolved during contact alloying may precipitate at grain boundaries in the aluminum, and cause reliability problems.

The appearance of brittleness, accompanied by pits in surface of the metal and cracks in the metal at oxide steps, also seems to indicate some variation in process control but different from that ascribed to window roughness. Observed evidence indicates that the problem may be due primarily to the metal-deposition process (presence of impurities) and is aggrevated by the sintering procedure. This type of metallization gave an unusual display when examined in back-scattered electron mode in the scanning electron microscope, i.e., a much darker appearance than the aluminum metallization on the other circuits of the same group.

The random tilting of the chips with respect to the package floor in both the SN5451 and SN54L51 specimens is traceable to inadequate process control in the bonding down of chips with glass-frit material. Chips that are grossly tilted are liable to damage in a production lead-bonding station. Operators will not always be aware of the tilted die in time to make the necessary height adjustment of the bonding tool in the "search" position. Deep scratches, bridging from smears, and metal flakes in and around the conductor stripes are the result. The tightly pulled lead wires in the SN 5451 specimens resulted in necking of the lead wire in the region just above the ball bond. This excessive pulling of the wire stresses both the wire and the ball bond unnecessarily and increases the chance of a failure occurring in physical-stress environments.

A design problem exists in the relationship between contact-pad size on the die and ball-bond size in the SN5451 circuits. The contact pads are undersize for the ball bonds being used which results quite often in the ball bond being placed too near the point where the metal stripe leading into the circuit emerges from the contact pad. When variations in the ball-bond size exist, as they did in these circuits, or the ball bond is slightly offset on the pad, the metal stripe could suffer considerable damage.

The SN5451 specimens that had cracked dies were given further study to determine, if possible, the reason for these occurrences. This study indicated that light scribing of the package bottoms to identify specimens may have caused these cracks. Although all microcircuits were handled identically, the SN5451 circuits had a combination of conditions that could have caused cracks in these circuits and not in the others. These conditions were:

(1) Packages having very thin metal bottoms (5 mils as compared to 15 mils for Manufacturer B)

(2) Thin silicon dies (approximately 5 mils as compared to approximately 8 mils for the circuits which did not crack)

(3) A generous fillet of glass frit around the chip which contained bubbles and voids

(4) Possible chip-bonding stresses as indicated by the dome effect seen in one of the cracked specimens.

The important aspect of this study is that the SN5451 circuits have a built-in construction weakness that must be considered in device application.

Neither circuit type from Manufacturer A exhibited the high-quality workmanship essential for high-reliability microcircuits.

Manufacturer B Microcircuits

The microcircuits from Manufacturer B nearly all showed defects in the metallization at contact window cuts. This type of defect is rarely detected in the screening tests employed to sort out early failures, but it usually becomes apparent when the device is subjected to temperature cycling or after extended periods of electrical stress at high temperature(2). A thorough discussion of the various appearances of these defects is given in the previous section of the report. The evidence that the cracking, porosity, and tunneling exists at the oxide step in the window cuts of these circuits is well documented in the previous section of the report.

The only other potential defect observed in these circuits was the very close clearance between the flying aluminum wires routed to the three internal bonding pads and the thin-film ground conductor along the edge of the die. As noted in the text, it is possible to install the internal leads in such a way as to provide ample clearance.

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(1) G. L. Schnable, and R. S. Keen, "Aluminum Metallization - Advantages and Limitations for Integrated Circuit Applications", Proc. IEEE, Vol 57, pages 1570-1580, 1969.

(2) Dr. G. V. Browning, "Monolithic Integrated Circuit Failure Mechanisms", IEEE-1969 Symposium on Designing with Monolithic Circuits, Boston, Massachusetts, May 20, 1969.

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W. O. Shurtleff, Reliability Handbook for Silicon Monolithic Microcircuits, Volume-Z, Failure Mechanisms of Monolithic Microcircuits, NASA CR-1347, April, 1969.

W. L. Workman, Reliability Handbook for Silicon Monolithic Microcircuits, Volume-3, Failure Analysis of Monolithic Microcircuits, NASA CR-1348, April, 1969.

APPENDIX A

DETAILED INFORMATION FROM CONSTRUCTION ANALYSIS PROGRAM

APPENDIX A

DETAILED INFORMATION FROM CONSTRUCTION ANALYSIS PROGRAM

This appendix contains written and pictorial documentation generated during the performance of this program. Included in this section are:

(1) Outline of Method of Approach

(2) External Visual Inspection Comments

(3) Color photomicrograph of each specimen type with grid overlay sheet

(4) Internal Visual Inspection Reports for all 20 specimens.

METHOD OF APPROACH

All samples were subjected to a step by step inspection procedure that progressed from the package exterior, to the package interior, the internal lead wire system, the lead wire bonds to the integrated circuit chip and the package leads, the metallized interconnect pattern on the surface of the I.C. chip and finally the connections between the metallized conductors and the active and passive regions in the monolithic silicon structure.

The program was conducted according to the following plan:

I. External Visual Inspection

(1) Optical inspection at 30X using vertical and oblique lighting of package exterior, lid seal and lead seals

(2) Mark by scribing package bottom and top of Lead 1

(3) Clean by immersion in hot triclorethylene, hot deionized (D.I.) water, D. I. water rinse and dry nitrogen blast.

II. Uncap

(1) Attach package to wafer lapping jig with low temperature wax (~ 80°C)

(2) Abrasively thin lid on wet 600-grit paper on lapping board

(3) Clean off abrasive agents and dry the parts

(4) Transfer package to glass slide

(5) In clean room, mechanically peel thinned lid section from cavity.

III. Internal Visual Inspection Using Applicable Paragraphs of MIL-STD-883 Method 2010

(1) Internal Package Condition. Examined at 45X under vertical illumination. Paragraph 3.1.14.

(2) Chip Orientation and Bond. Examined at 45X under vertical illumination. Paragraph 3.1.13.1.

(3) Foreign Material on Die (after dry N_2 gas-blown). Examined at 45X under vertical illumination. Paragraph 3.1.9.

(4) Internal Lead Wires. Examined at 45X under vertical illumination. Paragraph 3.1.12.1.

(5) Wire Bonds on Posts (package). Examined at 45X under vertical illumination. Paragraphs 3.1.11 through 3.1.11.3.

(6) Wire Bonds on Pads (die). Examined at 45X under vertical illumination. Paragraphs 3.1.10 through 3.1.10.2.

(7) Metallization Defects. Examined at 80X minimum under vertical illumination. Paragraph 3.1.1.

(7a) Scratches and voids. Paragraph 3.1.2.

(7b) Corrosion. Paragraphs 3.1.3 and 3.1.3.1.

(7c) Bridging. Paragraphs 3.1.4 and 3.1.4.1.

(7d) Alignment and Window Coverage. Paragraphs 3.1.5 through 3.1.5.2.

IV. Photomicrography

(1) Photograph in color the total die surface at applicable low magnification.

(2) Photograph in color identified and suspected defect areas at a magnification appropriate to show the details.

V. Deep Field Inspection in Scanning Electron Microscope (photographs of SEM presentations made as required)

(1) Inspect chip, chip bond and internal lead wires at 50X in secondary electron mode (SE).

(2) Inspect die surface in back-scattered electron mode (BSE) at 50-200X to resolve and delineate foreign matter on die.

(3) Inspect bonds on die.

(4) Inspect identified defects observed in III and IV using SE or BSE modes as required.

(5) Scan die surface for other defects.

(6) Examine windows during conduct of (5).

VI. Interferometry

(1) Determine metallization thickness and variations on circuit from each sample.

VII. Metallographic Sectioning

(1) Pot device and grind to region of interest.

(2) Polish sectioned device.

(3) Examine cross-section optically and in scanning electron microscope for deficiencies in chip to package bond, lead to metallization bond, and metallization to oxide bond. Also examine for presence of intermetallics or contamination at interfaces.

VIII. Analyze Results

(1) Study data and pictures generated in each phase of program.

(2) Verify defects.

(3) Report.

External Visual Inspection(a)

Manufacturer A; welded lids.

Specimen No.	Lid Seal	Lead Seals	
11	ok	ok	Leads are grossly offset in glass seals and nearly touch metal wall.
12	ok	ok	Slight chipping of glass at end leads (Leads 1, 7, 8, and 14).
13	ok	(see notes)	Glass seal at Lead 8 appears to be cracked; others are ok.
14	ok	ok	Slight chipping of glass at end leads (Leads 1, 7, 8, and 14).
15	(see notes)	--	Lid seal above Lead 6 very doubtful. In general, the lid seal on this specimen is not nearly as wetted as other specimens.
	--	(see notes)	Side lead seals are ok; glass seals especially Leads 1 and 8. Depth of cracks was indeterminant. Leads are offset in glass seals. Lead 6 nearly touches metal wall.
21	ok	ok	Bubbles in glass at Lead 13 which did not reach the surface.
22	ok	ok	Excess glass filleted onto leads gave appearance of chipping at lead seals.
23	ok	ok	
24	ok	ok	
25	ok	ok	Ditto Specimen No. 22 note.

(a) A visual inspection was performed on Specimens No. 11-15 and 21-25 before removal from the plastic shipping frames, on Specimens No. 31-35 after removal from metallized cardboard folders, and on Specimens 41-45 after removal from the plastic shipping frames.

Manufacturer B; soldered lids.

Specimen No.	Lid Seal	Lead Seals	
31	(see notes)	--	Solder is not filleted between lid and body in several areas around lid periphery, i.e., above Lead 9 at corner, between Leads 2 & 3, between Leads 4 & 5, and between Leads 6 & 7.
		(see notes)	Small voids in glass at narrow sides of Leads 4 & 13.
32	(see notes)	--	Solder is spotty or apparently absent for total distance between Leads 6 & 7; lid seal in doubt at corner between Leads 13 & 14.
		(see notes)	Small voids in glass at narrow sides of Leads 2, 3, 6, 9, & 13.
33	(see notes)	--	Lid is twisted slightly clockwise on package, overhanging edges by ~ .015 inch. Small void in solder seal above Lead 14.
		(see notes)	Small voids in glass at narrow sides of Leads 2, 3, 6, 9, & 13.
34	ok	(see notes)	Small voids in glass at narrow sides of Leads 1, 7, 9, & 13.
35	(see notes)	ok	Voids in solder lid-seal between Leads 1 & 2, Leads 4 & 6 and Leads 13 & 14.
41	(see notes)	--	Solder is spotty in led seal between Leads 3 & 4 and Leads 8 & 9.
		(see notes)	Small voids in glass at narrow sides of Leads 2, 5, 6, & 13.
42	(see notes)	--	Four apparent voids in solder seal along the 9 to 13 lead side of package.
		(see notes)	Small voids in glass at narrow sides of Leads 2, 9, & 13.

Manufacturer B; soldered lids. (Continued)

Specimen No.	Lid Seal	Lead Seals	
43	(see notes)	--	Solder seal integrity in doubt along two adjacent sides of lid from Lead 2 to Lead 9. No solder was visible in seam above Lead 9.
		(see notes)	Small voids in glass at narrow sides of Leads 2, 6, 9, & 13.
44	(see notes)	--	Integrity of solder seal questionable along end of lid above Leads 1 & 14; also above Lead 10.
		(see notes)	Small voids in glass at narrow sides of Leads 2, 3, 9, & 13.
45	(see notes)	--	Solder was discontinuous in seam around periphery of lid and noticeably absent between Leads 1 & 2, 3 & 5, 7 & 9, and 12 & 13, and above Lead 6.
		(see notes)	Small voids in glass at narrow sides of Leads 2, 6, 7, 9, & 13.

Most of Manufacture-B packages have a slight rectangular depression in the package bottom from the die-bonding-station pedestal. The depression in Specimen 45 was rather deep by comparison.

INTERNAL VISUAL INSPECTION

Following are 20 Internal Visual Inspection sheets that report the detailed observations made at the time the inspection was performed. Each group of five sheets is accompanied by a color photomicrograph with a grid overlay on clear acetate that serves as a reference figure for the defect locations described in the inspection sheet and for the figures in the body of the report. Internal-lead numbers are also indicated on these reference figures.

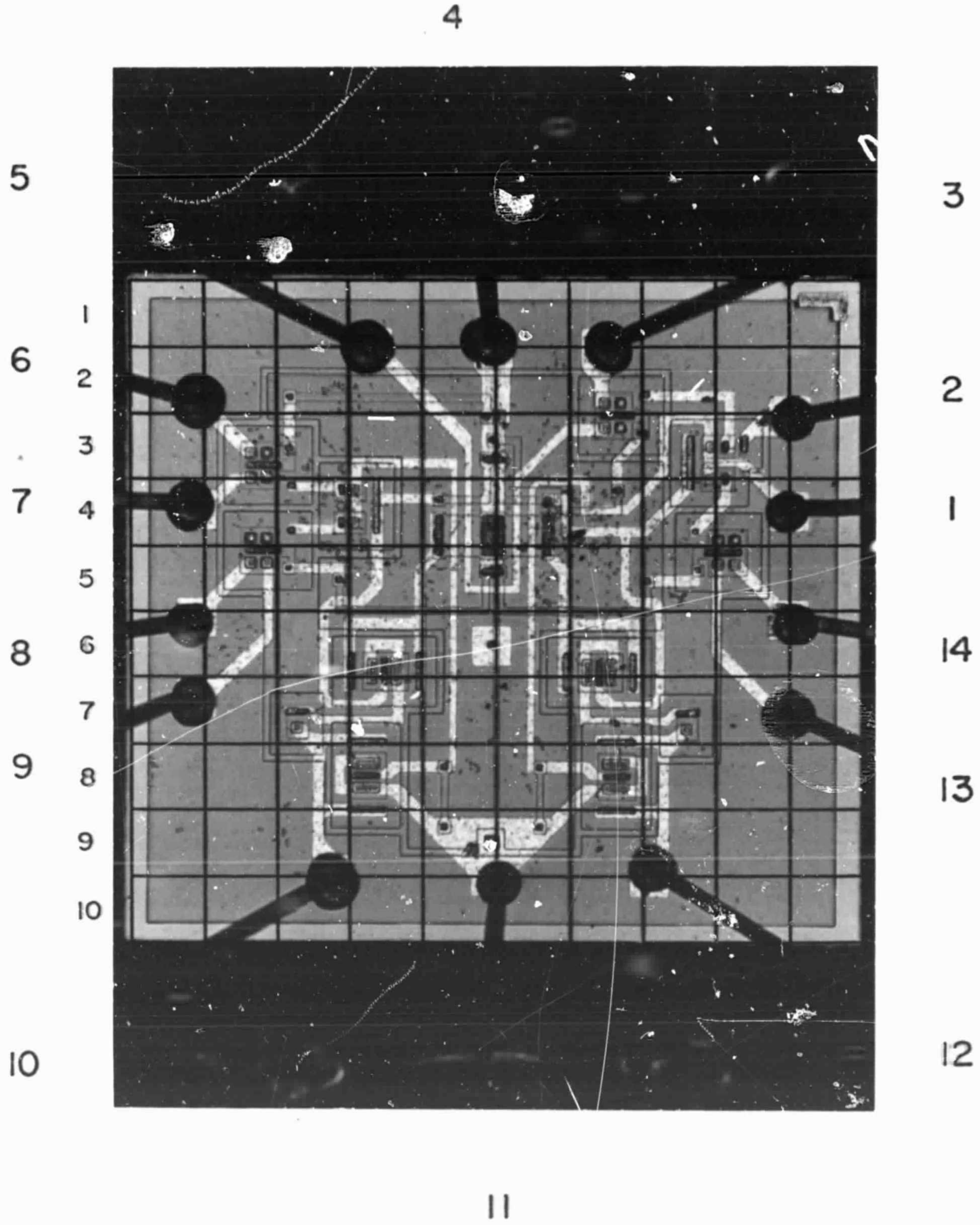


FIGURE A-1. TYPE SN5451, MANUFACTURER A
SPECIMEN NUMBERS 11-15

MICROCIRCUIT CONSTRUCTION ANALYSIS

INTERNAL VISUAL INSPECTION

(Inspection Criteria - MIL-STD-883, Method 2010)

Manufacturer: A	**Inspector:** D. A. Kaiser
Circuit Type: SN5451	**Site:** Microelectronic Cleanroom
Sample: 11	**Date:** September 29, 1969

1. **INTERNAL PACKAGE CONDITION examined at 45X under vertical illumination; Paragraph 3.1.14.**

   Cavity is clean and free of foreign matter. The center area of package floor is not gold plated. Corrosion is visible in this unplated area but the corrosion scale is minimal and appears to be firmly attached.

2. **CHIP ORIENTATION AND BOND examined at 45X under vertical illumination; Paragraph 3.1.13.1.**

   Chip is well centered in package and oriented correctly. Bonding medium appears to be glass frit, the amount of which is satisfactory.

3. **FOREIGN MATERIAL ON DIE (after dry N_2 gas-blow) examined at 45X under vertical illumination; Paragraph 3.1.9.**

   There is no loose foreign matter on the die, however, there appears to be surface problems that are more in the nature of diffusion anomalies or surface contamination inherent to the die.

4. **INTERNAL LEAD WIRES examined at 45X under vertical illumination; Paragraph 3.1.12.1.**

   All lead wires go directly to the posts without looping. There are no nicks, cuts, scorings or necking down apparent in the lead wires. The only defects seen are Leads 1, 7, 8, 13, and 14 being pulled at right angles just above the ball bond. The required 0.5 mil distance before bending toward the package is not present for these leads.

5. **WIRE BONDS ON POSTS (package) examined at 45X under vertical illumination; Paragraph 3.1.11 through 3.1.11.3.**

   The placement and formation of the wire bonds on the posts are satisfactory for all posts except Post 12. The wire on this post is bonded somewhat along the side instead of on the top and the bond is of doubtful quality.

6. WIRE BONDS ON PADS (die) examined at 45X under vertical illumination; Paragraphs 3.1.10 through 3.1.10.2.

All ball bonds are of satisfactory size, relative to the diameter of the lead wire. There is no evidence of rebonding at any pad. All bonds are centered on the pad except for Bond 12 which is offset toward the metal stripe leading into the circuit.

In general, most of the ball bonds would be rejected according to the criteria of Method 2010, Paragraph 3.1.10, due to the small size of the metal pads on the die. The ball bonds in all but one case are larger in size than the pads to which they are attached. This results in the ball bonds overhanging the pad and covering the fillet between the pad and the metal stripe leading into the circuit. Approximately one-half of the pads do not have adequate fillet showing between the pad and the metal stripe.

7. METALLIZATION DEFECTS examined at 80X minimum under vertical illumination; Paragraph 3.1.1.

7a. Scratches and Voids; Paragraph 3.1.2.

A scratch is noted in a metal stripe in Section G8. There are no voids in the metallization. However, because of the surface condition of the die the metallization has a peculiar appearance in many areas, especially where it crosses the underlying diffusion anomalies.

7b. Corrosion; Paragraphs 3.1.3 and 3.1.3.1.

There is no apparent corrosion on the metallization. The metallization has a peculiar granular, off-color appearance over most of the contact windows on the die. There is a small amount of opaque matter on the metallization in Section G4, but does not appear to be corrosion product.

7c. Bridging; Paragraphs 3.1.4 and 3.1.4.1.

The interconnect pattern is well defined. There is no bridging.

7d. Alignment and Window Coverage; Paragraphs 3.1.5 through 3.1.5.2.

The interconnect pattern is properly aligned on the die. Window coverage is satisfactory as far as alignment is concerned. However, some windows appear to have anomalies in the metallization that may very well be causing inadequate window coverage. These windows are principally in Sections E3, F3, D4, and F4 although there are other windows on the die that have that same appearance.

MICROCIRCUIT CONSTRUCTION ANALYSIS

INTERNAL VISUAL INSPECTION

(Inspection Criteria - MIL-STD-833, Method 2010)

Manufacturer: A
Inspector: D. A. Kaiser

Circuit Type: SN5451
Site: Microelectronic Cleanroom

Sample: 12
Date: September 29, 1969

1. INTERNAL PACKAGE CONDITION examined at 45x under vertical illumination; Paragraph 3.1.14.

   Cavity is clean and free of foreign matter. The center area of package floor is not gold plated. A small amount of corrosion is visible in this unplated area but appears to be firmly attached.

2. CHIP ORIENTATION AND BOND examined at 45X under vertical illumination; Paragraph 3.1.13.1.

   The chip is offset in the package in the direction of Lead No. 4. The bonding medium appears to be glass frit the amount of which is slightly more than adequate. At one point the material has gotten on to the top edge of the die. The glass frit appears to be cracked or crazed rather deeply although none of it appears to be loose at this time.

3. FOREIGN MATERIAL ON DIE (after dry N_2 gas-blow) examined at 45X under vertical illumination; Paragraph 3.1.9.

   There are several specks of foreign matter on the die. One of these is in Section A7 just adjacent to the bonding pad. Another, in Section I7, appears to be a dust moat. There are several minor specks outside of the circuit pattern in Sections B8, D3, and G9.

4. INTERNAL LEAD WIRES examined at 45X under vertical illumination; Paragraph 3.1.12.1.

   All internal lead wires are properly oriented and without excessive looping. There are no nicks, scratches, or cuts apparent in any of the wires. There is no noticeable necking down of the bonding wires. Lead 14 is pulled at right angles just above the ball bond, the required 0.5 mil distance above the ball bond before bending not being present.

5. WIRE BONDS ON POSTS (package) examined at 45X under vertical illumination; Paragraph 3.1.11 through 3.1.11.3.

   All wire bonds are nominally centered on the posts and are satisfactorily formed except for those on Posts 2, 3, 12, 13, and 14 which appear to be overbonded. The appearance of these posts suggests that the bonding tool may have been dragged across the bond area after the bond was performed. Post 12 has a visible tooling mark on it. Post 2 has the wire rather mashed across the top area of the post as though the bonding tool was dragged across the wire. All bonds appear to be intact, however.

6. WIRE BONDS ON PADS (die) examined at 45X under vertical illumination; Paragraphs 3.1.10 through 3.1.10.2.

All ball bonds are of satisfactory size. The bonds on Pads 4 and 11 are offset on the pads by approximately 50 percent. The ball bonds on Pads 1, 13, and 14 are offset toward the center of the circuit and are covering the fillet between the pad and the metal stripe leading into the circuit. On Pads 7, 10, 13, and 14, the balls appear to have been dragged across the pad before being bonded into place.

7. METALLIZATION DEFECTS examined at 80X minimum under vertical illumination; Paragraph 3.1.1.

7a. Scratches and Voids; Paragraph 3.1.2.

There are no scratches or voids on any part of the metallization other than that noted at the pads.

7b. Corrosion; Paragraphs 3.1.3 and 3.1.3.1.

There is no corrosion visible on any part of the metallization.

7c. Bridging; Paragraphs 3.1.4 and 3.1.4.1.

There is no bridging of metallization, however, several of the foreign specks on the die surface appear to bridge between two of the metal strips. These particles are located in Sections E3, F4, and G6.

7d. Alignment and Window Coverage; Paragraphs 3.1.5 through 3.1.5.2.

The alignment of the interconnect pattern on the die is satisfactory. Window coverage appears to be 100 percent.

Note: There is a crack propagating from the edge of the die toward the active circuit area in Sections F1 and G1. This crack was probably induced during specimen marking before uncapping.

MICROCIRCUIT CONSTRUCTION ANALYSIS

INTERNAL VISUAL INSPECTION

(Inspection Criteria - MIL-STD-883, Method 2010)

Manufacturer: A	Inspector: D. A. Kaiser
Circuit Type: SN5451	Site: Microelectronic Cleanroom
Sample: 13	Date: September 29, 1969

1. INTERNAL PACKAGE CONDITION examined at 45X under vertical illumination; Paragraph 3.1.14.

The cavity is clean and free of foreign matter. The package floor is not gold plated in the center area. The few spots of corrosion noted in this unplated area are firmly attached.

2. CHIP ORIENTATION AND BOND examined at 45X under vertical illumination; Paragraph 3.1.13.1.

The chip is offset in the package toward Lead 10 but is oriented correctly. The bonding medium appears to be glass frit.

3. FOREIGN MATERIAL ON DIE (after dry N_2 gas-blow) examined at 45X under vertical illumination; Paragraph 3.1.9.

There is no excessive foreign matter on the die. Several small specks can be seen outside of the circuit area and appear to be metallic rather than nonmetallic. An important item of note at this point is that the die appears to be cracked in two places. One crack starts at the edge of the die near Pad 10 (Section B 10) following under that pad, under Pad 11 and Pad 13 to the edge of the die (Section J-7). The other crack starts from the die edge between Pads 6 and 7 (Section A 3) and goes directly across the die coming out between Pads 1 and 2 (Section J3).

4. INTERNAL LEAD WIRES examined at 45X under vertical illumination; Paragraph 3.1.12.1.

Leads 1, 12, 13 have excessive looping between the pad and the post. The mentioned leads are leaning generally towards the No. 10 pin side of the package as though they had all been bumped in unison. Lead 7 is pulled tightly at right angles just above the ball bond.

5. WIRE BONDS ON POSTS (package) examined at 45X under vertical illumination; Paragraph 3.1.11 through 3.1.11.3.

The wire bonds on the posts are satisfactorily placed and bonded for all leads except Leads 5, 7, and 8 which appear to be somewhat overbonded. Post 7 shows marks which suggest that the bonding tool was dragged across the surface. All bonds appear to be intact, however.

6. WIRE BONDS ON PADS (die) examined at 45X under vertical illumination; Paragraphs 3.1.10 through 3.1.10.2.

All ball bonds are of satisfactory size. The appearance of Pad 13 suggests a rebond at this pad. The ball bond at Pad 12 is approximately 50 percent off the pad and that at Pad 4 is approximately 30 percent off the pad. The ball bonds at Pads 1, 2, 6, 7, 9, and 14 are offset toward the die center and cover the fillet between the pad and the emerging stripe.

7. METALLIZATION DEFECTS examined at 80X minimum under vertical illumination; Paragraph 3.1.1.

7a. Scratches and Voids; Paragraph 3.1.2.

A major smear in the metallization is present in Sections G6, G7, and G8. The smear which was probably caused by a gold ball being dragged across the die has caused deep scratches in the metal stripes and a condition of near-bridging between stripes. Another serious smear from similar causes is present in Section I2 adjacent to Pad 2. Less serious smearing is noted at several of the bonding pads. A suspicious appearing spot is seen in the middle of a metal stripe in both Sections H7 and C4. Since these have the same appearance as the voids along the edge of the stripes, they may be etching anomalies. The extent of the apparent defect is difficult to determine optically.

7b. Corrosion; Paragraphs 3.1.3 and 3.1.3.1.

There is no corrosion apparent on any part of the metallization.

7c. Bridging; Paragraphs 3.1.4 and 3.1.4.1.

There is no bridging between any of the metal stripes. However, the smear in Sections G6 and G7 would be cause for rejection of this circuit because of reduction in stripe clearance to less than 25% of design width.

7d. Alignment and Window Coverage; Paragraphs 3.1.5 through 3.1.5.2.

The interconnect pattern is properly aligned on the die and window coverage is satisfactory over the whole die.

Note: The cracks in the die are believed to have been caused during specimen marking before uncapping.

MICROCIRCUIT CONSTRUCTION ANALYSIS

INTERNAL VISUAL INSPECTION

(Inspection Criteria - MIL-STD-883, Method 2010)

Manufacturer: A
Circuit Type: SN5451
Sample: 14

Inspector: D. A. Kaiser
Site: Microelectronic Cleanroom
Date: September 29, 1969

1. INTERNAL PACKAGE CONDITION examined at 45X under vertical illumination; Paragraph 3.1.14.

   Cavity is clean of foreign matter except for a transparent blob of material attached to package floor near one end of cavity. The center area of package floor is not gold plated. Corrosion scale can be seen in this unplated area but appears to be firmly attached.

2. CHIP ORIENTATION AND BOND examined at 45X under vertical illumination; Paragraph 3.1.13.1.

   Chip is well centered in package. Bonding medium appears to be glass frit.

3. FOREIGN MATERIAL ON DIE (after dry N_2 gas-blow) examined at 45X under vertical illumination; Paragraph 3.1.9.

   Die is free of large foreign particles. There are small splatter-like spots on the surface of the die but these are mostly outside of the circuit area. One such splatter can be seen in the circuit area in Section E6. The die appears to be cracked across one corner. The crack extends from Pad 12 (Section H10) toward Pad 13 (Section J7).

4. INTERNAL LEAD WIRES examined at 45X under vertical illumination; Paragraph 3.1.12.1.

   All lead wires are properly oriented except for Leads 6 and 11. These wires have loops greater than the specified 3 times wire diameter. The loops appear to have been caused by snagging with the bonding tool. Both leads are intact, however. There is no nicking, cutting, or necking down apparent on any of the lead wires. Leads 2 and 6 are pulled sharply at right angles just above the ball bond.

5. WIRE BONDS ON POSTS (package) examined at 45X under vertical illumination; Paragraph 3.1.11 through 3.1.11.3.

   All post bonds are satisfactorily placed and appear to be adequately bonded.

6. WIRE BONDS ON PADS (die) examined at 45X under vertical illumination; Paragraphs 3.1.10 through 3.1.10.2.

All ball bonds are of satisfactory size. On Pads 2 and 14 the bonds are offset toward the center of the circuit. Bond 12 is offset towards one side of the pad. Additionally, the ball bonds on Pads 1, 6, 7, 8, 10, and 13 cover the fillet between the pad and the metal stripe leading onto the circuit.

7. METALLIZATION DEFECTS examined at 80X minimum under vertical illumination; Paragraph 3.1.1.

7a. Scratches and Voids; Paragraph 3.1.2.

The suspected crack in the corner of the die is not a crack. It is a string of diffusion anomalies that appear to be a crack at lower magnification. There is, however, a crack completely across the die in a straight line from Pad 9 (Section A7) to Pad 13 (Section J7). There are scratches in several of the metal stripes above the transistor in Section G8. There are also scratches in the bonding pads adjacent to the ball bonds at Pads 1, 2, 5, 6, 10, 11, 12, and 13. At 200X a scratch is apparent in the metal stripe leading from Pad 14 into the circuit. This appears to have been caused by a gold ball being dragged across the stripe. There are numerous other scratches and defects in the metallization located in Sections D6, D7, D8, E6, H5, and I4. In addition, there are pock marks in the metallization surface over the whole die. These pock marks are in the order of 10 to 20 percent of the metal stripe width and occur variously along the edges or in the center of the metal stripes.

7b. Corrosion; Paragraphs 3.1.3 and 3.1.3.1.

There is no corrosion visible on any part of the metallization.

7c. Bridging; Paragraphs 3.1.4 and 3.1.4.1.

There is no bridging apparent on this die.

7d. Alignment and Window Coverage; Paragraphs 3.1.5 through 3.1.5.2.

The interconnect pattern appears to be slightly offset toward the 6, 7, 8, 9-lead side of the die. However, the alignment is satisfactory and the window coverage is adequate at all contact windows.

Note: In general this is a poor circuit. The die is cracked, the appearance of the metallization leaves more than a little to be desired. This circuit shows poor workmanship in that the metallization has been scratched and marred at most of the pads as well as over some of the circuit area apparently by the gold balls prior to ball bonding.

The crack in the die is believed to have been caused during specimen marking before uncapping.

MICROCIRCUIT CONSTRUCTION ANALYSIS

INTERNAL VISUAL INSPECTION

(Inspection Criteria - MIL-STD-883, Method 2010)

Manufacturer: A	Inspector: D. A. Kaiser
Circuit Type: SN5451	Site: Microelectronic Cleanroom
Sample: 15	Date: September 29, 1969

1. INTERNAL PACKAGE CONDITION examined at 45X under vertical illumination; Paragraph 3.1.14.

The cavity is clean and free of foreign matter except for a translucent fiber strand attached to Post No. 2. This appears to be a cloth fiber approximately 0.2 mil is diameter by 15 or 20 mils long. The fiber was not removed during a normal gas blow. The center area of the package floor is not gold plated and is free of corrosion.

2. CHIP ORIENTATION AND BOND examined at 45X under vertical illumination; Paragraph 3.1.13.1.

The chip is centered in the package and oriented correctly. Bonding medium appears to be glass frit.

3. FOREIGN MATERIAL ON DIE (after dry N_2 gas-blow) examined at 45X under vertical illumination; Paragraph 3.1.9.

The die is essentially free of foreign material. Several small opaque splatters can be seen on the die surface but these are mostly outside of the active circuit area. There is one small splatter to be seen within the circuit area in Section I3. Another smaller splatter is in Section D4.

4. INTERNAL LEAD WIRES examined at 45X under vertical illumination; Paragraph 3.1.12.1.

The internal lead wires are oriented correctly without excessive looping. No nicks, cuts, or scratches are visible. Several of the wires appear to have a rippled surface as though they had been stretched but do not show serious necking down. All wires except Leads 4 and 11 are pulled sharply at right angles just above the ball bond. At this low magnification there appear to be stress cracks in the gold where the wire and the ball join on most of the leads.

5. WIRE BONDS ON POSTS (package) examined at 45X under vertical illumination; Paragraph 3.1.11 through 3.1.11.3.

The bonds appear to be adequately placed and formed with the exception of Posts 5, 7, and 8. On these posts, the bonds were achieved on the curving side of the post rather than on the top. These bonds appear to be somewhat overbonded and mashed probably due to the tool skittering down the side of post during the bonding operation.

6. WIRE BONDS ON PADS (die) examined at 45X under vertical illumination; Paragraphs 3.1.10 through 3.1.10.2.

All ball bonds are of satisfactory size. The ball bonds are satisfactorily placed on all pads except No. 3, 4, 5, 6, 7, and 11 which are offset. On Pads 3, 5, and 7 the bonds are offset toward the metal stripe leading into the circuit area thus covering the fillet between the pad and the stripe. Pads 10 and 14 show evidence of rebonding.

7. METALLIZATION DEFECTS examined at 80X minimum under vertical illumination; Paragraph 3.1.1.

7a. Scratches and Voids; Paragraph 3.1.2.

Except for some marring at several of the pads this die appears to be free of scratches. The pads which show evidence of marring are No. 2, 3, 4, 7, 11, 12, 13, and 14. The die is free of major voids in the metallization, however, there are minor voids over the whole circuit area. These are spotted along the edges of the metal stripes as well as in the center. In particular, silicon dioxide shows through the voids in the metallization in Sections C5, D5, D6, E3, F4, and G9. There are many other smaller voids through which silicon dioxide does not show.

7b. Corrosion; Paragraphs 3.1.3 and 3.1.3.1.

There is no corrosion visible on any part of the metallization.

7c. Bridging; Paragraphs 3.1.4 and 3.1.4.1.

The metallization pattern is well defined. There is no bridging apparent over the whole surface of the die.

7d. Alignment and Window Coverage; Paragraphs 3.1.5 through 3.1.5.2.

The alignment of the interconnect pattern on the die is satisfactory. Window coverage is adequate at every contact window.

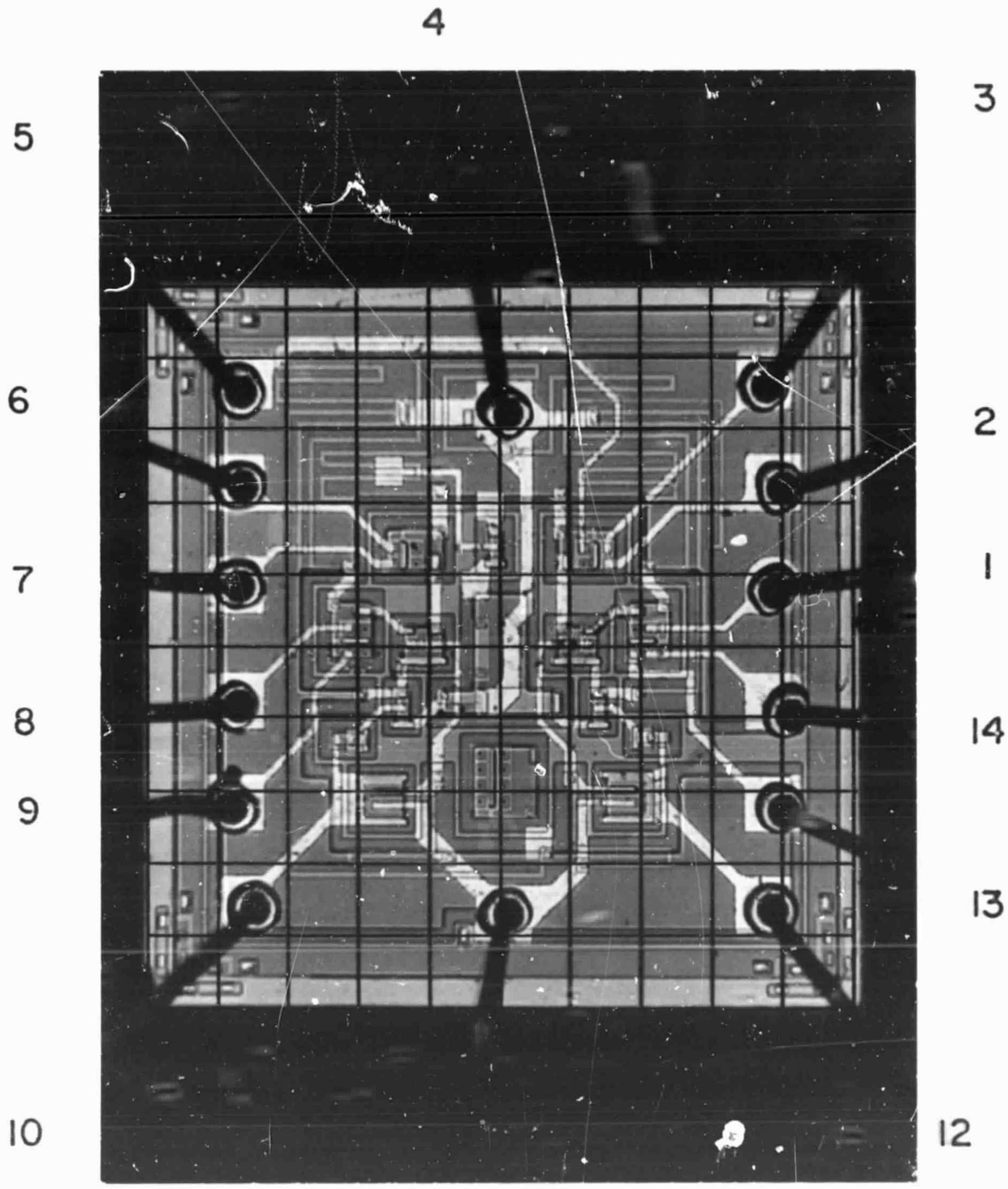


FIGURE A-2. TYPE SN54L51, MANUFACTURER A
SPECIMEN NUMBERS 21-25

MICROCIRCUIT CONSTRUCTION ANALYSIS

INTERNAL VISUAL INSPECTION

(Inspection Criteria - MIL-STD-883, Method 2010)

Manufacturer: A	Inspector: D. A. Kaiser
Circuit Type: SN54L51	Site: Microelectronic Cleanroom
Sample: 21	Date: September 29, 1969

1. INTERNAL PACKAGE CONDITION examined at 45X under vertical illumination; Paragraph 3.1.14.

   The cavity is clean. One loose foreign particle can be seen within the cavity. It is an opaque strand approximately 0.2 mil in diameter by 40 to 50 mils long.

2. CHIP ORIENTATION AND BOND examined at 45X under vertical illumination; Paragraph 3.1.13.1.

   Chip is offset in package toward the No. 1 lead end. Orientation is correct. Chip is bonded to package by glass frit.

3. FOREIGN MATERIAL ON DIE (after dry N_2 gas-blow) examined at 45X under vertical illumination; Paragraph 3.1.9.

   There are no large particles of foreign material on the die in the circuit area. There is one particle partly on Bonding Pad 14, partly on the die of approximately 0.75 X 1.5 mil in size. There are several smaller particles spotted about the die that may be foreign particles. These will have to be examined at higher magnification.

4. INTERNAL LEAD WIRES examined at 45X under vertical illumination; Paragraph 3.1.12.1.

   All lead wires except Nos. 9 and 10 go directly from the pad to the post. Leads 9 and 10 loop slightly more than 3-wire diameters from a straight line. There are no nicks, cuts, crimps, or scorings visible on the lead wires. There is no serious necking down of any of the lead wires.

5. WIRE BONDS ON POSTS (package) examined at 45X under vertical illumination; Paragraph 3.1.11 through 3.1.11.3.

   All wire bonds on posts are adequately placed and formed. All bonds appear to be intact.

6. WIRE BONDS ON PADS (die) examined at 45X under vertical illumination; Paragraphs 3.1.10 through 3.1.10.2.

The gold ball bonds all appear to be of satisfactory size. The bonds are Pads 2, 8, 9, and 14 appear to be slightly offset on the pad but all are within the required limits. The bond at Pad 14 has the appearance of a rebond. What was earlier thought to be foreign material at Pad 14 appears to be a bond that was pulled loose.

7. METALLIZATION DEFECTS examined at 80X minimum under vertical illumination; Paragraph 3.1.1.

7a. Scratches and Voids; Paragraph 3.1.2.

The metallization on this die has been scuffed, over the greater part of the circuit. There are scuff marks visible in Sections C3, C4, D4, D6, D7, F3, F7, F8, G9, and H5. In Section E7 a metal stripe appears to have been scribed deeply enough to cause an open-circuit. There are no major voids in the metal stripes. There are numerous small spots in the stripes that have the appearance of voids. One of these spots is in Section G6, another in I5.

7b. Corrosion; Paragraphs 3.1.3 and 3.1.3.1.

There is no identified corrosion on any part of the metallization. However, there are several suspicious spots along the edges of metal stripes that could be corrosion. The larger of these are located in Sections E8, F3, and F7.

7c. Bridging; Paragraphs 3.1.4 and 3.1.4.1.

There is no bridging involving the metallization itself. However, in section G6 there is a foreign particle that bridges from one metal stripe across a second and touches a third. This appears to be a fleck of gold. There are other similar flecks spotted around on the metallization but none of these are bridging between two stripes.

7d. Alignment and Window Coverage; Paragraphs 3.1.5 through 3.1.5.2.

The alignment of the interconnect pattern on the die is very good. Window coverage seems to be 100 percent over the whole die.

Note: In retrospect, the particle of foreign material described in Item 3 above is probably the same particle mentioned in Item 7 and seen in yet a different location in the overall photomicrograph of the die. It was evidently loose and moving around but for some reason was not removed during the N_2 gas blow.

MICROCIRCUIT CONSTRUCTION ANALYSIS

INTERNAL VISUAL INSPECTION

(Inspection Criteria - MIL-STD-883, Method 2010)

Manufacturer: A	**Inspector:** D. A. Kaiser
Circuit Type: SN54L51	**Site:** Microelectronic Cleanroom
Sample: 22	**Date:** September 29, 1969

1. INTERNAL PACKAGE CONDITION examined at 45X under vertical illumination; Paragraph 3.1.14.

   The cavity is clean and free of foreign matter.

2. CHIP ORIENTATION AND BOND examined at 45X under vertical illumination; Paragraph 3.1.13.1.

   The chip is nominally centered in the package and oriented correctly. The bonding medium appears to be glass frit.

3. FOREIGN MATERIAL ON DIE (after dry N_2 gas-blow) examined at 45X under vertical illumination; Paragraph 3.1.9.

   There are several small specks less than 1 mil in size on the die surface. None of these can be seen in the circuit area. Along one edge of the die near Bonding Pad 14 there is a translucent speck of material right at the die edge. The particle is about 1 mil in diameter.

4. INTERNAL LEAD WIRES examined at 45X under vertical illumination; Paragraph 3.1.12.1.

   All lead wires are oriented correctly from pad to post. Only Lead 14 shows the slightest loop and it is less than the specified 3-wire diameters. There is no nicking, cutting, or scoring in any of the lead wires nor can any necking down of the wires be observed. All leads have greater than the 0.5 mil distance before bending toward the package.

5. WIRE BONDS ON POSTS (package) examined at 45X under vertical illumination; Paragraph 3.1.11 through 3.1.11.3.

   All wire bonds on the posts are satisfactorily placed and adequately bonded.

6. WIRE BONDS ON PADS (die) examined at 45X under vertical illumination; Paragraphs 3.1.10 through 3.1.10.2.

   All ball bonds are of satisfactory size. There is no evidence of rebonding at this magnification. The bonds on Pads 6, 10, and 12 are offset toward the circuit and cover the fillet between the pad and the metal stripe leading onto the circuit.

7. METALLIZATION DEFECTS examined at 80X minimum under vertical illumination; Paragraph 3.1.1.

7a. Scratches and Voids; Paragraph 3.1.2.

There is a major scratch in the metal stripe leading from Pad 14 into the circuit. This is in Section I6. There is another scratch under the ball bond on Pad 1 (Section J-5). Both of these appear to have been caused by the gold ball being dragged across the surface of the die. When viewed at 200X the scratch previously mentioned in the stripe leading from Pad 14 also has touched the stripe leading from Pad 1 onto the circuit (Section H5) severing approximately 50 percent of the stripe width. There are numerous small voids in the surface of the metallization over several parts of the circuit. In particular, Sections C5, D4, D5, and E5 have these defects. Bonding Pad 8 also shows evidence of a smear in the bonding pad surface at both sides of the gold ball.

7b. Corrosion; Paragraphs 3.1.3 and 3.1.3.1.

There is no identified corrosion apparent on any part of the metallization, but there are suspicious spots along the edges of the metal stripes that may be corrosion.

7c. Bridging; Paragraphs 3.1.4 and 3.1.4.1.

There is no bridging between any of the metal stripes.

7d. Alignment and Window Coverage; Paragraphs 3.1.5 through 3.1.5.2.

The alignment of the interconnect pattern on the die is very good. Window coverage is 100 percent at all windows.

MICROCIRCUIT CONSTRUCTION ANALYSIS

INTERNAL VISUAL INSPECTION

(Inspection Criteria - MIL-STD-883, Method 2010)

Manufacturer: A	Inspector: D. A. Kaiser
Circuit Type: SN54L51	Site: Microelectronic Cleanroom
Sample: 23	Date: September 30, 1969

1. INTERNAL PACKAGE CONDITION examined at 45X under vertical illumination; Paragraph 3.1.14.

   Cavity is clean and free of foreign matter. Center area of package floor is not gold plated. No corrosion is visible in this unplated area.

2. CHIP ORIENTATION AND BOND examined at 45X under vertical illumination; Paragraph 3.1.13.1.

   The chip is nominally centered in the package and oriented correctly. The chip is bonded to the package with glass frit.

3. FOREIGN MATERIAL ON DIE (after dry N_2 gas-blow) examined at 45X under vertical illumination; Paragraph 3.1.9.

   There is no excessive foreign material on the die. Several very small spots can be seen on the die surface outside of the active circuit area.

4. INTERNAL LEAD WIRES examined at 45X under vertical illumination; Paragraph 3.1.12.1.

   All lead wires are oriented correctly between the pads and the posts. Leads, 1, 2, 6, 7, 8, 9, 13, and 14 have excessive vertical loops that sag toward the package floor. However, none of the wires are closer than 2 mils to each other or to the package floor. There are no nicks, cuts, scrapes, or necking down apparent in any of the lead wires.

5. WIRE BONDS ON POSTS (package) examined at 45X under vertical illumination; Paragraph 3.1.11 through 3.1.11.3.

   All post bonds are properly placed and formed.

6. WIRE BONDS ON PADS (die) examined at 45X under vertical illumination; Paragraphs 3.1.10 through 3.1.10.2.

   All ball bonds are of satisfactory size. All bonds are well situated on bonding pads except for Bonds 3 and 6. These bonds are slightly offset toward the center of the die and just barely leave an adequate fillet between the pad and the metal stripe leading into the circuit. There is no evidence of rebonding at any pad.

7. METALLIZATION DEFECTS examined at 80X minimum under vertical illumination; Paragraph 3.1.1.

7a. Scratches and Voids; Paragraph 3.1.2.

The metallization in the center area of the die has numerous small scratches. It gives the appearance of the die having been scooted around face down on some surface during the manufacturing process. The scratches seem to be relatively shallow and minor in nature. A possible exception to this is the metallization in Section G5. The scratches in the metallization at this point appear to be somewhat deeper. There are no major voids in the metallization. There are a number of minor voids along the edges of the metal stripes having the appearance of etching anomalies.

7b. Corrosion; Paragraphs 3.1.3 and 3.1.3.1.

There does not appear to be corrosion on the surface of the metallization but there are a number of spots along the edges of the metal stripes that could possibly be corrosion. These spots are general over the whole surface of the die. Typical example would be in Section G6. Spots can be seen along the edge of almost all the metal stripes in this section.

7c. Bridging; Paragraphs 3.1.4 and 3.1.4.1.

There is no bridging between any of the metal stripes on the die.

7d. Alignment and Window Coverage; Paragraphs 3.1.5 through 3.1.5.2.

The alignment of the interconnect pattern on the die is satisfactory. Window coverage is 100 percent at all contact windows on the die.

MICROCIRCUIT CONSTRUCTION ANALYSIS

INTERNAL VISUAL INSPECTION

(Inspection Criteria - MIL-STD-883, Method 2010)

Manufacturer: A	Inspector: D. A. Kaiser
Circuit Type: SN54L51	Site: Microelectronic Cleanroom
Sample: 24	Date: September 30, 1969

1. INTERNAL PACKAGE CONDITION examined at 45X under vertical illumination; Paragraph 3.1.14.

Package is clean and free of foreign matter. Center area of package floor is not gold plated. The unplated area is discolored but no corrosion scale is apparent.

2. CHIP ORIENTATION AND BOND examined at 45X under vertical illumination; Paragraph 3.1.13.1.

The chip is off center in the cavity toward No. 12 lead. The chip is bonded into the package by glass frit.

3. FOREIGN MATERIAL ON DIE (after dry N_2 gas-blow) examined at 45X under vertical illumination; Paragraph 3.1.9.

There are no large foreign particles on the die, however, the die appears to be speckled with spots that are in the order of 0.02 mils or smaller. These minute spots are over the whole surface of the die from edge to edge. They were not removed with a normal gas blow.

4. INTERNAL LEAD WIRES examined at 45X under vertical illumination; Paragraph 3.1.12.1.

All wires are oriented correctly between the bonding pads and the posts. Leads 2, 6, 7, 8, 9, and 14 have excessive sagging between the pad and the post. However, none of these leads approach each other or the package floor by less than 2 mils. There are no nicks, cuts, scrapes, or necking down apparent in any of the lead wires.

5. WIRE BONDS ON POSTS (package) examined at 45X under vertical illumination; Paragraph 3.1.11 through 3.1.11.3.

All wires are satisfactorily placed on the posts and appear to be adequately bonded.

6. WIRE BONDS ON PADS (die) examined at 45X under vertical illumination; Paragraphs 3.1.10 through 3.1.10.2.

All ball bonds are of satisfactory size. Most of the ball bonds are properly placed on the pads. Bond 11 is approximately 50 percent offset to the side and Bonds 6, 12, and 13 are offset toward the center of the circuit covering the fillet between the pad and the metal stripe. There is a spot adjacent to Pad 1 which suggests that this pad was rebonded, the first attempt having almost missed the pad completely.

7. METALLIZATION DEFECTS examined at 80X minimum under vertical illumination; Paragraph 3.1.1.

7a. Scratches and Voids; Paragraph 3.1.2

Compared to the companion samples this circuit has few scratches. There are scratches across the metal stripes in I6 and I7 which probably were caused by a gold ball being dragged across the die prior to bonding. A scratch in Section H8 appears to be deep enough to cause problems. There are no major voids in the metallization over the whole die. However, there are minor voids in many of the stripes. Typical of these are located in Sections E2, G2, E5, and F5.

7b. Corrosion; Paragraphs 3.1.3 and 3.1.3.1.

There is no corrosion apparent on the surface of the metallization. However, there are spots along the edges of the metallization that could either be corrosion or incomplete removal of the molybdenum during the etching process. These spots are rather general over the whole circuit. They are more pronounced in the nine sections described as G, H, and I, 6, 7, and 8.

7c. Bridging; Paragraphs 3.1.4 and 3.1.4.1.

There is no bridging apparent on any part of the circuit.

7d. Alignment and Window Coverage; Paragraphs 3.1.5 through 3.1.5.2.

The alignment of the interconnect pattern on the circuit is very good. Window coverage is 100 percent at all windows.

Note: The minute speckles on the die observed in Item 3 were recognized as gold flecks at higher magnification. The appearance of these flecks suggests photolithography problems prior to etching of the metallization.

MICROCIRCUIT CONSTRUCTION ANALYSIS

INTERNAL VISUAL INSPECTION

(Inspection Criteria - MIL-STD-883, Method 2010)

Manufacturer: A	**Inspector:** D. A. Kaiser
Circuit Type: SN54L51	**Site:** Microelectronic Cleanroom
Sample: 25	**Date:** September 30, 1969

1. INTERNAL PACKAGE CONDITION examined at 45X under vertical illumination; Paragraph 3.1.14.

   Cavity is clean and free of foreign matter. The center area of package floor is not gold plated. The unplated area appears to be tarnished but no corrosion scale is visible.

2. CHIP ORIENTATION AND BOND examined at 45X under vertical illumination; Paragraph 3.1.13.1.

   The chip is slightly offset in the package toward the Lead 1 end but is oriented correctly. The chip is bonded to the package by glass frit.

3. FOREIGN MATERIAL ON DIE (after dry N_2 gas-blow) examined at 45X under vertical illumination; Paragraph 3.1.9.

   There is no loose foreign material on the die. Several small specks can be seen at various points on the die. These are mostly outside the circuit area. The specks within the circuit area are of such small size that they appear to be causing no problems. Typical of these is the speck in Section C6 adjacent to the metallization stripe.

4. INTERNAL LEAD WIRES examined at 45X under vertical illumination; Paragraph 3.1.12.1.

   All lead wires go directly from the bonding pads on the die to the posts except for Leads 1, 13, and 14. These three leads have excessive looping. It appears that the leads have been bumped at some time after they were bonded to the post. There are no nicks, cuts, scratches, or necking down apparent in any of the lead wires.

5. WIRE BONDS ON POSTS (package) examined at 45X under vertical illumination; Paragraph 3.1.11 through 3.1.11.3.

   All bonds are satisfactorily placed on the posts and appear to be adequately formed.

6. WIRE BONDS ON PADS (die) examined at 45X under vertical illumination; Paragraphs 3.1.10 through 3.1.10.2.

All bonds are of satisfactory size. Several of the bonds are slightly offset on the pad but all would meet the specification requirements. There is no evidence of rebonding at any pad.

7. METALLIZATION DEFECTS examined at 80X minimum under vertical illumination; Paragraph 3.1.1.

7a. Scratches and Voids; Paragraph 3.1.2.

There is a major scratch in the Vcc metallization through the center of the circuit. This is in Sections F4 and F5. This same scratch crosses Bonding Pad 4 in Section F2. There is a network of smaller scratches on the surface of the metallization in eight sections described as G and H, 3, 4, 5, and 6 which appear to be the result of the die having been scrubbed on its top surface prior to bonding in the package. There are no major voids in the metallization on any part of the die. There are, however, a number of small voids spotted around the circuit which could cause trouble. These are located variously in Sections D3, D6, D8, I6.

7b. Corrosion; Paragraphs 3.1.3 and 3.1.3.1.

There is no corrosion on the surface of the metallization. There are spots along the edge of several of the metal stripes that could either be corrosion or traces of molybdenum that were not removed during etching. These are located in Sections D6, E4, G6, and G7, among others.

7c. Bridging; Paragraphs 3.1.4 and 3.1.4.1.

There is no bridging between any of the metallization stripes.

7d. Alignment and Window Coverage; Paragraphs 3.1.5 through 3.1.5.2.

The interconnect pattern is well aligned on the die. Window coverage appears to be 100 percent at all contact windows. However, at several of the windows in the area where the metallization was scratched, the circuit continuity at the windows is doubtful.

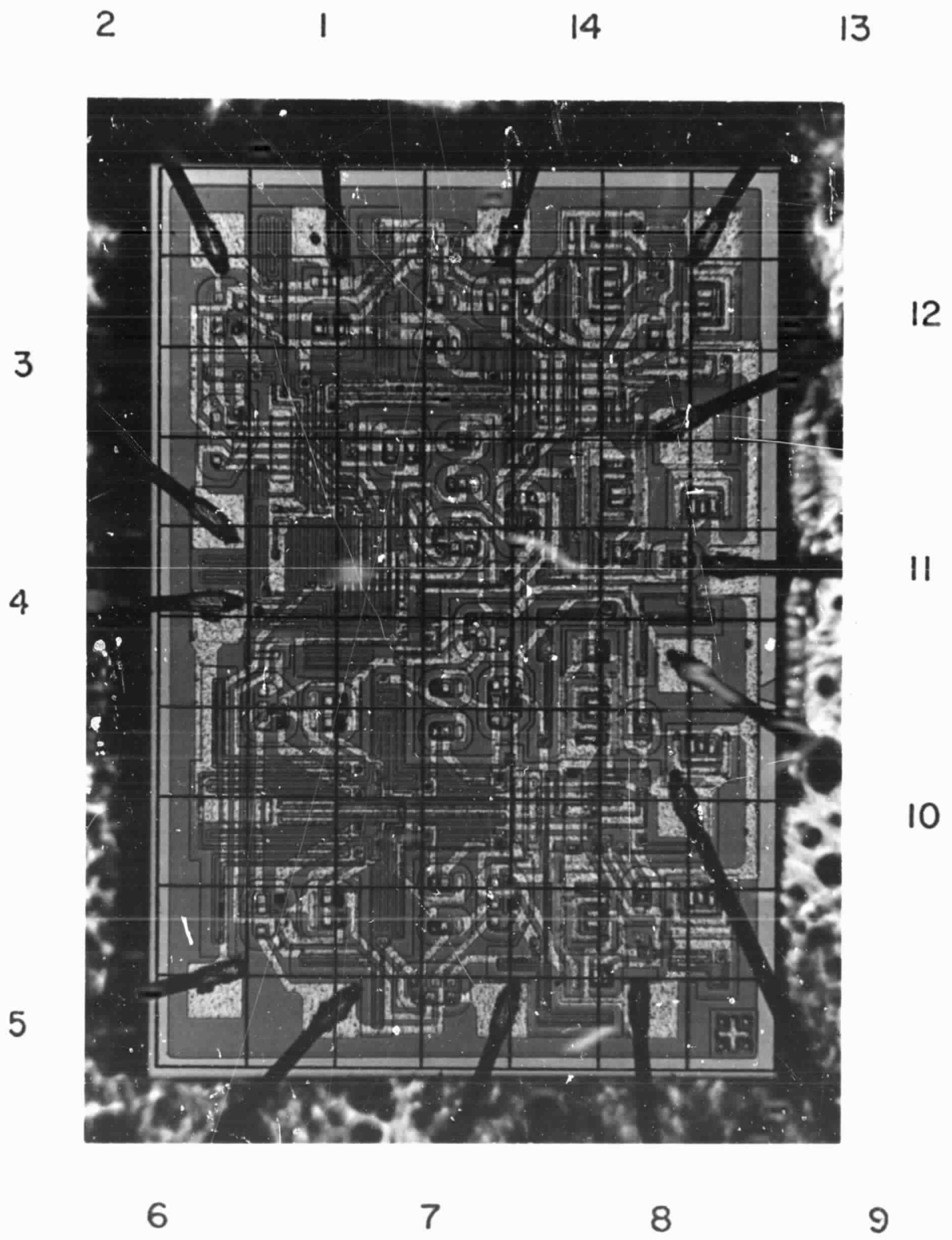


FIGURE A-3. TYPE SN54L78T, MANUFACTURER B
SPECIMEN NUMBERS 31-35

MICROCIRCUIT CONSTRUCTION ANALYSIS

INTERNAL VISUAL INSPECTION

(Inspection Criteria - MIL-STD-883, Method 2010)

Manufacturer: B	Inspector: D. A. Kaiser
Circuit Type: SN54L78T	Site: Microelectronic Cleanroom
Sample: 31	Date: November 17, 1969

1. INTERNAL PACKAGE CONDITION examined at 45X under vertical illumination; Paragraph 3.1.14.

   Interior of package is clean and free of foreign matter. There is a void in the glass adjacent to Lead 10 which appears to be a bubble at surface. The depth of the void cannot be determined without probing.

2. CHIP ORIENTATION AND BOND examined at 45X under vertical illumination; Paragraph 3.1.13.1.

   The chip is nominally centered on the package floor and is oriented correctly. The bond appears to be gold eutectic paste, the amount of which is satisfactory.

3. FOREIGN MATERIAL ON DIE (after dry N_2 gas-blow) examined at 45X under vertical illumination; Paragraph 3.1.9.

   There is no foreign material of any kind on the die.

4. INTERNAL LEAD WIRES examined at 45X under vertical illumination; Paragraph 3.1.12.1.

   The internal lead wires are in very good condition. There is no looping between the bonding pads and the posts. There is no nicking, cutting, crimping, or scoring of the wires nor is there any necking down of the bonding wires. There are no extra lead tails or lead wires. No leads are closer than 2 mils to each other at any point.

5. WIRE BONDS ON POSTS (package) examined at 45X under vertical illumination; Paragraph 3.1.11 through 3.1.11.3.

   All wire bonds on posts are satisfactorily placed and well formed. The bonds are almost uniformly one and one-half times the diameter of the lead wire. The only discrepancy seen is an extra bond placed on Post 9. The excess wire has been removed from this bond, however, and it is causing no problem.

6. WIRE BONDS ON PADS (die) examined at 45X under vertical illumination; Paragraphs 3.1.10 through 3.1.10.2.

All bonds are nominally centered on the pads. There are no tails longer than 3 mils. There are no bonds over any area of the silicon surface. The bonds appear to be uniformly made and spread to approximately 1-1/2 times the wire diameter. The bond at Pad 4 appears to have a small tail less than 1 mil long extending over the metal stripe leading into the circuit.

7. METALLIZATION DEFECTS examined at 80X minimum under vertical illumination; Paragraph 3.1.1.

7a. Scratches and Voids; Paragraph 3.1.2.

There is a smear in the metallization in Sections E1 and E2. The smear is of a cosmetic nature and is not causing bridging between the metal stripes.

7b. Corrosion; Paragraphs 3.1.3 and 3.1.3.1.

There is no corrosion apparent on any part of the metallization. There are several suspicious areas along the edges of the metal stripes in Section B1. However, it is doubtful that these are really corrosion.

7c. Bridging; Paragraphs 3.1.4 and 3.1.4.1.

There is no bridging between any of the metal stripes on the die.

7d. Alignment and Window Coverage; Paragraphs 3.1.5 through 3.1.5.2.

The interconnect pattern is properly aligned on the die and all windows are 100 percent covered.

MICROCIRCUIT CONSTRUCTION ANALYSIS

INTERNAL VISUAL INSPECTION

(Inspection Criteria - MIL-STD-883, Method 2010)

Manufacturer: B	Inspector: D. A. Kaiser
Circuit Type: SN54L78T	Site: Microelectronic Cleanroom
Sample: 32	Date: November 17, 1969

1. INTERNAL PACKAGE CONDITION examined at 45X under vertical illumination; Paragraph 3.1.14.

   The package is clean and free of foreign matter.

2. CHIP ORIENTATION AND BOND examined at 45X under vertical illumination; Paragraph 3.1.13.1.

   The chip is centered in the package, oriented correctly, and appears to be well bonded. The gold alloy melt is visible for approximately 90 percent around the periphery of the chip.

3. FOREIGN MATERIAL ON DIE (after dry N_2 gas-blow) examined at 45X under vertical illumination; Paragraph 3.1.9.

   There appears to be no foreign material on the die surface.

4. INTERNAL LEAD WIRES examined at 45X under vertical illumination; Paragraph 3.1.12.1.

   All internal lead wires appear to be satisfactory.

5. WIRE BONDS ON POSTS (package) examined at 45X under vertical illumination; Paragraph 3.1.11 through 3.1.11.3.

   All bonds are properly placed and appear to be well formed.

6. WIRE BONDS ON PADS (die) examined at 45X under vertical illumination; Paragraphs 3.1.10 through 3.1.10.2.

   All bonds appear to be adequately formed and with the exception of Pads 1 and 3, the bonds are properly placed. The bonds on Pads 1 and 3 are placed in close proximity to the point at which the metal stripe leaves the pad. According to the criteria of Method 2010, these two bonds would probably be rejected.

7. METALLIZATION DEFECTS examined at 80X minimum under vertical illumination; Paragraph 3.1.1.

7a. Scratches and Voids; Paragraph 3.1.2.

There are no scratches or voids in the metallization on any part of the die.

7b. Corrosion; Paragraphs 3.1.3 and 3.1.3.1.

There is no recognized corrosion on any of the metallization. However, on every pad there is a corrosion—like appearance around the periphery of the bond. It cannot be ascertained even at high magnification whether this is a corrosion product. It seems unlikely that it is corrosion since these are ultrasonically bonded aluminum leads to aluminum pads. Final definition of this apparent problem must await the scanning-electron microscope.

7c. Bridging; Paragraphs 3.1.4 and 3.1.4.1.

There is no bridging between any of the metal stripes on this die.

7d. Alignment and Window Coverage; Paragraphs 3.1.5 through 3.1.5.2.

The interconnect pattern is satisfactorily aligned on the die. All windows are adequately covered.

Note: At this higher magnification (200X) there are several small specks visible on the die surface. These are located in Sections D2, D4, D5, D6, and F6. None of these specks are large enough or located in such a place as to cause electrical problems.

MICROCIRCUIT CONSTRUCTION ANALYSIS

INTERNAL VISUAL INSPECTION

(Inspection Criteria - MIL-STD-883, Method 2010)

Manufacturer: B	**Inspector:** D. A. Kaiser
Circuit Type: SN54L78T	**Site:** Microelectronic Cleanroom
Sample: 33	**Date:** November 17, 1969

1. INTERNAL PACKAGE CONDITION examined at 45X under vertical illumination; Paragraph 3.1.14.

   Package is very clean and free of foreign matter.

2. CHIP ORIENTATION AND BOND examined at 45X under vertical illumination; Paragraph 3.1.13.1.

   Chip is centered in package, oriented correctly, and appears to be adequately bonded.

3. FOREIGN MATERIAL ON DIE (after dry N_2 gas-blow) examined at 45X under vertical illumination; Paragraph 3.1.9.

   There are no large foreign particles on the surface of the die.

4. INTERNAL LEAD WIRES examined at 45X under vertical illumination; Paragraph 3.1.12.1.

   There are no internal lead wire problems.

5. WIRE BONDS ON POSTS (package) examined at 45X under vertical illumination; Paragraph 3.1.11 through 3.1.11.3.

   All wire bonds are properly placed, well formed, and appear to be adequately bonded to the posts.

6. WIRE BONDS ON PADS (die) examined at 45X under vertical illumination; Paragraphs 3.1.10 through 3.1.10.2.

   All wire bonds are well placed and appear to be satisfactorily bonded to the pads.

7. METALLIZATION DEFECTS examined at 80X minimum under vertical illumination; Paragraph 3.1.1.

7a. Scratches and Voids; Paragraph 3.1.2.

A shallow cosmetic-type smear is located in Section C2. There are numerous void-like spots along the edges of the metallization stripes over the whole surface of the die. Typical of these are seen in Section E1, G2, and F3. While these are not voids as such; they appear to be shallow spots in the metallization.

7b. Corrosion; Paragraphs 3.1.3 and 3.1.3.1.

There is no corrosion visible on the metallization on this die.

7c. Bridging; Paragraphs 3.1.4 and 3.1.4.1.

There is no bridging between any of the metal stripes on the die surface. In Section H2 there is a small spur off one of the stripes but it does not actually bridge to the next stripe.

7d. Alignment and Window Coverage; Paragraphs 3.1.5 through 3.1.5.2.

The interconnect pattern is satisfactorily aligned on the die and window coverage appears to be 100 percent over the whole die.

Note: There are several small flecks of foreign matter seen on the die at 200X. These are located in Sections G1, F3, F6, G6, and I7. They are all of such small size and located in such a place as to be insignificant.

MICROCIRCUIT CONSTRUCTION ANALYSIS

INTERNAL VISUAL INSPECTION

(Inspection Criteria - MIL-STD-883, Method 2010)

Manufacturer: B	Inspector: D. A. Kaiser
Circuit Type: SN54L78T	Site: Microelectronic Cleanroom
Sample: 34	Date: November 17, 1969

1. INTERNAL PACKAGE CONDITION examined at 45X under vertical illumination; Paragraph 3.1.14.

   Cavity is clean and free of foreign matter.

2. CHIP ORIENTATION AND BOND examined at 45X under vertical illumination; Paragraph 3.1.13.1.

   Chip is nominally centered in cavity and oriented correctly. The chip appears to be adequately bonded to the package.

3. FOREIGN MATERIAL ON DIE (after dry N_2 gas-blow) examined at 45X under vertical illumination; Paragraph 3.1.9.

   There is no foreign material apparent on the surface of the die.

4. INTERNAL LEAD WIRES examined at 45X under vertical illumination; Paragraph 3.1.12.1.

   There are no internal lead wire problems.

5. WIRE BONDS ON POSTS (package) examined at 45X under vertical illumination; Paragraph 3.1.11 through 3.1.11.3.

   All bonds appear to be satisfactorily placed and adequately bonded.

6. WIRE BONDS ON PADS (die) examined at 45X under vertical illumination; Paragraphs 3.1.10 through 3.1.10.2.

   All bonds are satisfactorily placed on the pads and appear to be well formed and adequately bonded.

7. METALLIZATION DEFECTS examined at 80X minimum under vertical illumination; Paragraph 3.1.1.

7a. Scratches and Voids; Paragraph 3.1.2.

There is a smear on the metallization that extends through Sections G4, G5, G6, and G7 and H4, H5, H6, and H7. The nature of this smear varies from very shallow or cosmetic to an appreciably deep scratch. However, silicon dioxide does not show through at any point.

7b. Corrosion; Paragraphs 3.1.3 and 3.1.3.1.

There is no recognized corrosion visible on the surface of the die. However, this circuit has a problem similar to Sample 32 where a suspicious corrosion-like product surrounds the wire bonds on most of the pads. It also has suspicious looking areas along the edges of the metallization, much like Sample 33, that probably are more in the nature of etching anomalies than corrosion.

7c. Bridging; Paragraphs 3.1.4 and 3.1.4.1.

There is no bridging between any of the metal stripes on this circuit. The smear previously described did not actually cause bridging although some of the stripes were widened slightly by the smearing action. In Section I2, there is a foreign particle that covers approximately 75 percent of the distance between two of the metal stripes. It does not cause a short circuit, however.

7d. Alignment and Window Coverage; Paragraphs 3.1.5 through 3.1.5.2.

The interconnect pattern is properly aligned on the die and all windows appear to be satisfactorily covered.

MICROCIRCUIT CONSTRUCTION ANALYSIS

INTERNAL VISUAL INSPECTION

(Inspection Criteria - MIL-STD-883, Method 2010)

Manufacturer: B	Inspector: D. A. Kaiser
Circuit Type: SN54L78T	Site: Microelectronic Cleanroom
Sample: 35	Date: November 17, 1969

1. INTERNAL PACKAGE CONDITION examined at 45X under vertical illumination; Paragraph 3.1.14.

The cavity is very clean and free of foreign matter. There is a small void in the glass adjacent to the land of Post 6. It appears to be a small bubble and very shallow.

2. CHIP ORIENTATION AND BOND examined at 45X under vertical illumination; Paragraph 3.1.13.1.

The chip is centered in the cavity, oriented correctly, and apparently well bonded.

3. FOREIGN MATERIAL ON DIE (after dry N_2 gas-blow) examined at 45X under vertical illumination; Paragraph 3.1.9.

There is no foreign material on the surface of the die.

4. INTERNAL LEAD WIRES examined at 45X under vertical illumination; Paragraph 3.1.12.1.

There are no apparent internal lead wire problems.

5. WIRE BONDS ON POSTS (package) examined at 45X under vertical illumination; Paragraph 3.1.11 through 3.1.11.3.

All post bonds appear to be satisfactorily placed and adequately bonded.

6. WIRE BONDS ON PADS (die) examined at 45X under vertical illumination; Paragraphs 3.1.10 through 3.1.10.2.

All leads appear to be adequately bonded to the pads. All bonds are satisfactorily placed with exception of Bond 5. This bond is too close to the point at which the metal stripe emerges from the pad and would probably fail the criteria of Method 2010.

7. METALLIZATION DEFECTS examined at 80X minimum under vertical illumination; Paragraph 3.1.1.

7a. Scratches and Voids; Paragraph 3.1.2.

There are no major scratches or voids in this circuit. There is a very small scratch in the metal stripe adjacent to Pad 14 in Section I4 and another in Section I3. Both scratches appear to be relatively minor, however.

7b. Corrosion; Paragraphs 3.1.3 and 3.1.3.1.

There is no corrosion apparent on this die other than the suspicious appearance around several of the wire bonds previously mentioned for Samples 32 and 34.

7c. Bridging; Paragraphs 3.1.4 and 3.1.4.1.

There is no bridging between any of the metal stripes.

7d. Alignment and Window Coverage; Paragraphs 3.1.5 through 3.1.5.2.

Pattern alignment is very good. Window coverage appears to be 100 percent.

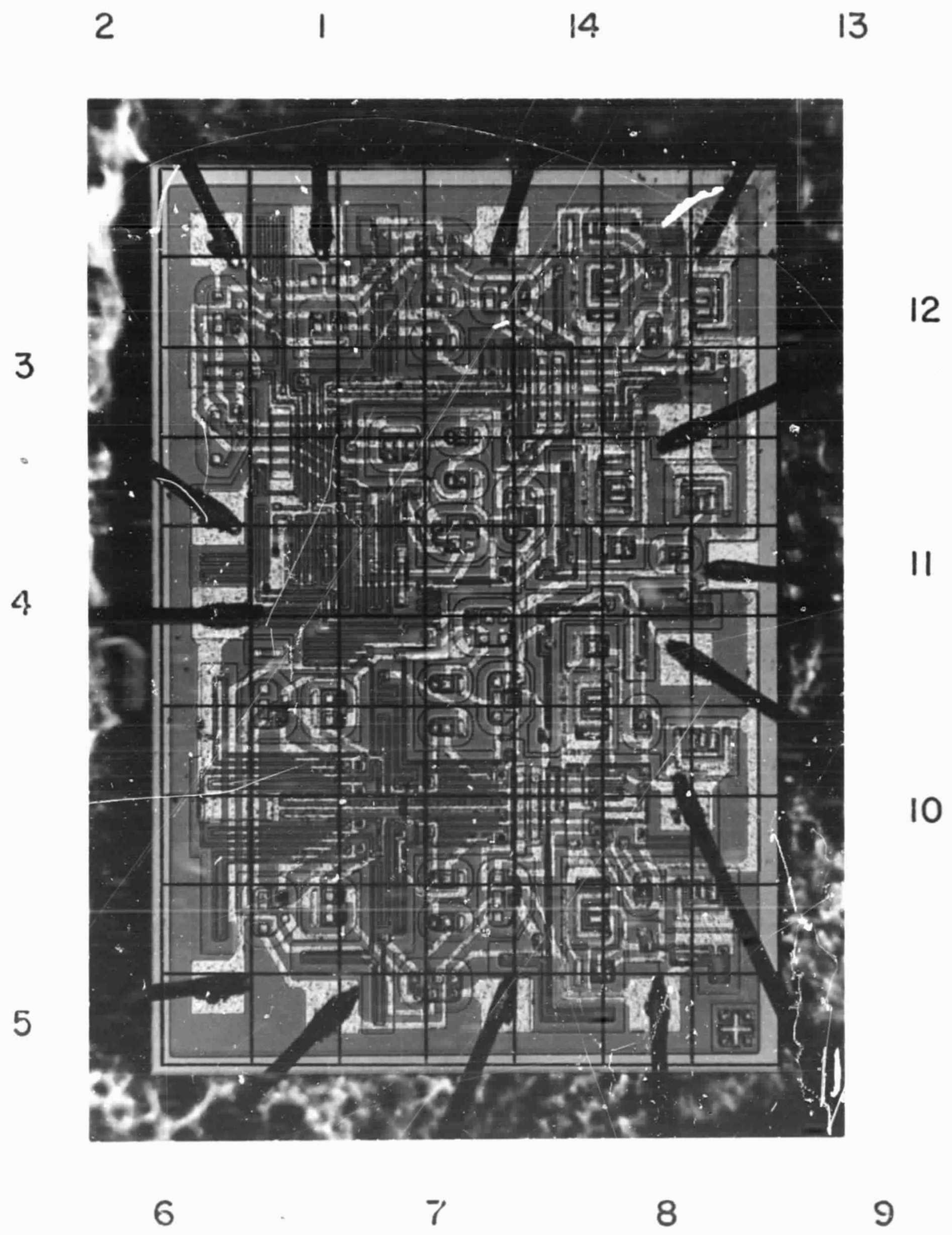


FIGURE A-4. TYPE SN54L73T, MANUFACTURER B
SPECIMEN NUMBERS 41-45

MICROCIRCUIT CONSTRUCTION ANALYSIS

INTERNAL VISUAL INSPECTION

(Inspection Criteria - MIL-STD-883, Method 2010)

Manufacturer: B	Inspector: D. A. Kaiser
Circuit Type: SN54L73T	Site: Microelectronic Cleanroom
Sample: 41	Date: November 17, 1969

1. INTERNAL PACKAGE CONDITION examined at 45X under vertical illumination; Paragraph 3.1.14.

   Package is clean and free of foreign matter except for one translucent strand seen on the surface of the die when the lid was removed. This strand which was about 1 mil is diameter by 3 to 4 mils long fell off the die when the package was inverted and tapped lightly.

2. CHIP ORIENTATION AND BOND examined at 45X under vertical illumination; Paragraph 3.1.13.1.

   Chip is centered in cavity, oriented correctly, and appears to be adequately bonded. The chip appears to be bonded to the package with gold eutectic paste.

3. FOREIGN MATERIAL ON DIE (after dry N_2 gas-blow) examined at 45X under vertical illumination; Paragraph 3.1.9.

   In Section C2, there is a translucent orange-colored spot approximately 1-1/2 x 3 mils in size. There are several small flecks on the surface of the die that will be examined in more detail at higher magnification.

4. INTERNAL LEAD WIRES examined at 45X under vertical illumination; Paragraph 3.1.12.1.

   There are no internal lead wire problems.

5. WIRE BONDS ON POSTS (package) examined at 45X under vertical illumination; Paragraph 3.1.11 through 3.1.11.3.

   All post bonds are satisfactorily placed and appear to be adequately bonded.

6. WIRE BONDS ON PADS (die) examined at 45X under vertical illumination; Paragraphs 3.1.10 through 3.1.10.2.

   All wire bonds on pads are satisfactorily placed and appear to be adequately bonded.

7. METALLIZATION DEFECTS examined at 80X minimum under vertical illumination; Paragraph 3.1.1.

7a. Scratches and Voids; Paragraph 3.1.2.

There are no scratches or smears on any part of the metallization. There is one small void in a metal stripe in Section I6.

7b. Corrosion; Paragraphs 3.1.3 and 3.1.3.1.

There is no corrosion apparent on any part of the metallization.

7c. Bridging; Paragraphs 3.1.4 and 3.1.4.1.

There is no bridging between any of the metal stripes. In Section H5, one of the metal stripes has a small spur along the side that extends approximately 50 percent of the distance to the next stripe. There is no short circuit however. In Section C2, there is an orange colored translucent film that covers an area bridging between three metal stripes over a transistor. This probably is not a short circuit. In Section H2, there is a small opaque spot on the silicon dioxide surface between two of the metal stripes. The diameter of the spot is approximately 50 percent of the design width between the stripes but the substance does not touch either of the stripes.

7d. Alignment and Window Coverage; Paragraphs 3.1.5 through 3.1.5.2.

The interconnect pattern is satisfactorily aligned on the die and window coverage is adequate over the whole surface of the die.

Note: This die has a peculiar anomaly not heretofore observed by this inspector. The basic or background color of the silicon dioxide is green at the No. 1 lead end of the die and fades to a gray color at the No. 7 lead end of the die. The resistor diffusions at the No. 1 lead end are purple and these fade into a blue, then blue-green, and into a vivid green going across the die to the No. 7 lead end. This indicates that the silicon dioxide thickness varies from one end of the die to the other.

MICROCIRCUIT CONSTRUCTION ANALYSIS

INTERNAL VISUAL INSPECTION

(Inspection Criteria - MIL-STD-883, Method 2010)

Manufacturer: B	**Inspector:** D. A. Kaiser
Circuit Type: SN54L73T	**Site:** Microelectronic Cleanroom
Sample: 42	**Date:** November 17, 1969

1. INTERNAL PACKAGE CONDITION examined at 45X under vertical illumination; Paragraph 3.1.14.

   A small amount of foreign matter (fine abrasive grit) entered this package during decapping. Some of this got onto the die surface at Pad 13. The following comments will ignore this contaminate since its source is known.

   Cavity is clean and free of included foreign matter.

2. CHIP ORIENTATION AND BOND examined at 45X under vertical illumination; Paragraph 3.1.13.1.

   Chip is well centered and oriented correctly in package. The chip seems to be adequately bonded to the package.

3. FOREIGN MATERIAL ON DIE (after dry N_2 gas-blow) examined at 45X under vertical illumination; Paragraph 3.1.9.

   There are several very small flecks on the surface of the die that will be evaluated at higher magnification.

4. INTERNAL LEAD WIRES examined at 45X under vertical illumination; Paragraph 3.1.12.1.

   There are none of the normal lead wire problems apparent in this circuit. Leads 9, 10, and 12 are bonded to internal bonding pads. As such, the wires coming to these pads must cross over and above a metallization stripe along the edge of the die which is the ground line connected to Pad 11. On this particular circuit, the leads coming to Pads 10 and 12 pass within 2 mils of the ground stripe. This would be cause for rejection according to the specification requirements.

5. WIRE BONDS ON POSTS (package) examined at 45X under vertical illumination; Paragraph 3.1.11 through 3.1.11.3.

   All leads are satisfactorily placed and appear to be adequately bonded to the posts.

6. WIRE BONDS ON PADS (die) examined at 45X under vertical illumination; Paragraphs 3.1.10 through 3.1.10.2.

All leads appear to be satisfactorily placed and adequately bonded. One item of note is that every bond appears to have been dragged backward over the pad in the direction of the post during the bonding operation for a distance of perhaps 1 to 1-1/2 mils. This results in smearing and in some cases gouging of the pad at the front end of the bond. In all but one case, this does not cause a problem. On Pad 2, however, the smear is very close to the point where one of the metal stripes emerges from the pad.

7. METALLIZATION DEFECTS examined at 80X minimum under vertical illumination; Paragraph 3.1.1.

7a. Scratches and Voids; Paragraph 3.1.2.

There is a minor scratch along the edge of a metal stripe in Section E1.

7b. Corrosion; Paragraphs 3.1.3 and 3.1.3.1.

There is no recognized corrosion on any part of the metallization.

7c. Bridging; Paragraphs 3.1.4 and 3.1.4.1.

There is no bridging apparent between any of the metal stripes.

7d. Alignment and Window Coverage; Paragraphs 3.1.5 through 3.1.5.2.

The interconnect pattern is properly aligned on the die and window coverage is satisfactory over the whole die.

Note: There are a very few small opaque flecks on the surface of the die. Two of these can be seen in Section B3 and H6. None are large enough to be considered troublesome.

MICROCIRCUIT CONSTRUCTION ANALYSIS

INTERNAL VISUAL INSPECTION

(Inspection Criteria - MIL-STD-883, Method 2010)

Manufacturer: B

Inspector: D. A. Kaiser

Circuit Type: SN54L73T

Site: Microelectronic Cleanroom

Sample: 43

Date: November 17, 1969

1. INTERNAL PACKAGE CONDITION examined at 45X under vertical illumination; Paragraph 3.1.14.

   Cavity is clean and free of foreign matter.

2. CHIP ORIENTATION AND BOND examined at 45X under vertical illumination; Paragraph 3.1.13.1.

   Chip is centered on package floor and oriented correctly. The chip appears to be adequately bonded to the package.

3. FOREIGN MATERIAL ON DIE (after dry N_2 gas-blow) examined at 45X under vertical illumination; Paragraph 3.1.9.

   There is no foreign material on the surface of the die apparent at this magnification.

4. INTERNAL LEAD WIRES examined at 45X under vertical illumination; Paragraph 3.1.12.1.

   There are no internal lead wire problems other than the close proximity of Leads 9 and 10 where they rise over and above the "ground" metallization stripe.

5. WIRE BONDS ON POSTS (package) examined at 45X under vertical illumination; Paragraph 3.1.11 through 3.1.11.3.

   All wire bonds are satisfactorily placed and appear to be adequately bonded.

6. WIRE BONDS ON PADS (die) examined at 45X under vertical illumination; Paragraphs 3.1.10 through 3.1.10.2.

   All leads appear to be adequately bonded to the pads. All bonds are satisfactorily placed on the pads.

7. METALLIZATION DEFECTS examined at 80X minimum under vertical illumination; Paragraph 3.1.1.

7a. Scratches and Voids; Paragraph 3.1.2.

There is a smear on Pad 13 in Section J7 parallel to the orientation of the wire bond. The smear appears to be more cosmetic than scratch. There are no voids apparent in the metallization.

7b. Corrosion; Paragraphs 3.1.3 and 3.1.3.1.

There is no corrosion visible on the surface of the metallization.

7c. Bridging; Paragraphs 3.1.4 and 3.1.4.1.

There is no bridging between any of the metal stripes.

7d. Alignment and Window Coverage; Paragraphs 3.1.5 through 3.1.5.2.

The alignment of the interconnect pattern is very good. Window coverage appears to be satisfactory over the whole die.

MICROCIRCUIT CONSTRUCTION ANALYSIS

INTERNAL VISUAL INSPECTION

(Inspection Criteria - MIL-STD-883, Method 2010)

Manufacturer: B	Inspector: D. A. Kaiser
Circuit Type: SN54L73T	Site: Microelectronic Cleanroom
Sample: 44	Date: November 17, 1969

1. INTERNAL PACKAGE CONDITION examined at 45X under vertical illumination; Paragraph 3.1.14.

   The cavity is very clean and free of foreign matter.

2. CHIP ORIENTATION AND BOND examined at 45X under vertical illumination; Paragraph 3.1.13.1.

   The chip is centered in the package, oriented correctly and appears to be adequately bonded to the package floor.

3. FOREIGN MATERIAL ON DIE (after dry N_2 gas-blow) examined at 45X under vertical illumination; Paragraph 3.1.9.

   There appears to be no foreign material on the surface of the die.

4. INTERNAL LEAD WIRES examined at 45X under vertical illumination; Paragraph 3.1.12.1.

   Except for Leads 9, 12, and especially Lead 10 which comes dangerously close to the ground metal stripe, there are no internal lead wire problems.

5. WIRE BONDS ON POSTS (package) examined at 45X under vertical illumination; Paragraph 3.1.11 through 3.1.11.3.

   All bonds appear to be satisfactorily placed and adequately bonded.

6. WIRE BONDS ON PADS (die) examined at 45X under vertical illumination; Paragraphs 3.1.10 through 3.1.10.2.

   All leads except Lead 5 are satisfactorily placed on the pad and adequately bonded. The bond at Pad 5 is approximately one-third off the pad but still passes the criteria of Method 2010. This circuit also exhibits the dragback of the bonds on the pads probably during the bonding operation resulting in a smear on the pad just ahead of the lead. On this circuit, however, none of these smears show any criticality.

7. METALLIZATION DEFECTS examined at 80X minimum under vertical illumination; Paragraph 3.1.1.

7a. Scratches and Voids; Paragraph 3.1.2.

There are no noticeable scratches or voids on any part of the metallization.

7b. Corrosion; Paragraphs 3.1.3 and 3.1.3.1.

There is no recognized corrosion on any of the metallization. There are a number of dark colored spots on the metallization at various points on the die. Section C4 has a concentration of these spots by way of example.

7c. Bridging; Paragraphs 3.1.4 and 3.1.4.1.

In Section A4, there is a small spur of metallic looking substance that appears to be bridging between two metal stripes. It appears to be attached to rather than integral with the metallization.

7d. Alignment and Window Coverage; Paragraphs 3.1.5 through 3.1.5.2.

The interconnect pattern is properly aligned on the die and window coverage is satisfactory over the whole die.

Note: In Section I6, there is an opaque spot adjacent to one of the metal stripes. However, it appears to be firmly attached and is not large enough to bridge to the next stripe.

MICROCIRCUIT CONSTRUCTION ANALYSIS

INTERNAL VISUAL INSPECTION

(Inspection Criteria - MIL-STD-883, Method 2010)

Manufacturer: B	Inspector: D. A. Kaiser
Circuit Type: SN54L73T	Site: Microelectronic Cleanroom
Sample: 45	Date: November 17, 1969

1. INTERNAL PACKAGE CONDITION examined at 45X under vertical illumination; Paragraph 3.1.14.

   Cavity is clean and free of foreign matter.

2. CHIP ORIENTATION AND BOND examined at 45X under vertical illumination; Paragraph 3.1.13.1.

   Chip is centered within cavity, oriented correctly, and appears to be adequately bonded.

3. FOREIGN MATERIAL ON DIE (after dry N_2 gas-blow) examined at 45X under vertical illumination; Paragraph 3.1.9.

   There are no foreign particles of any consequence on the surface of the die.

4. INTERNAL LEAD WIRES examined at 45X under vertical illumination; Paragraph 3.1.12.1.

   There are no internal lead wire problems except for the close proximity of Lead 9 to ground stripe.

5. WIRE BONDS ON POSTS (package) examined at 45X under vertical illumination; Paragraph 3.1.11 through 3.1.11.3.

   All leads appear to be adequately bonded to the posts. The bonds are satisfactorily placed.

6. WIRE BONDS ON PADS (die) examined at 45X under vertical illumination; Paragraphs 3.1.10 through 3.1.10.2.

   The wire bonds on the pads of this circuit are exceptionally good. They are well placed and uniformly bonded.

7. METALLIZATION DEFECTS examined at 80X minimum under vertical illumination; Paragraph 3.1.1.

7a. Scratches and Voids; Paragraph 3.1.2.

There are no scratches and no voids on the metallization of this circuit. A peculiar depression is observed in a metal stripe in Section 14 where there is no underlying reason (i.e. contact window or diffusion channel) for such a depression. It suggests a void in the silicon dioxide surface under the metal.

7b. Corrosion; Paragraphs 3.1.3 and 3.1.3.1.

There is no corrosion apparent on the metallization.

7c. Bridging; Paragraphs 3.1.4 and 3.1.4.1.

There is no bridging between any of the metal stripes.

7d. Alignment and Window Coverage; Paragraphs 3.1.5 through 3.1.5.2.

The interconnect pattern is properly aligned and all windows are satisfactorily covered.

APPENDIX B

INTERFEROMETRY DETERMINATION OF METALLIZATION THICKNESS

APPENDIX B

INTERFEROMETRY DETERMINATION OF METALLIZATION THICKNESS

Four microcircuits were submitted to a quantitative evaluation of the metallization thickness by interferometry. A Zeiss two-beam interferometer of the Linnik type was used for the measurements. The four microcircuits were identified as follows:

BMI Sample No.	Manufacturer	Report Number
14	A	SN 5451
23	A	SN 54L51
34	B	SN 54L78T
44	B	SN 54L73T

At least 5 determinations of the metallization thickness (one in each quadrant and one at the center) were made on each microcircuit. The determinations were made using a white light source with an average wavelength of 0.6 micron.

The metallization thickness was uniform on each individual microcircuit. The maximum variation in metallization thickness was 0.06 micron.

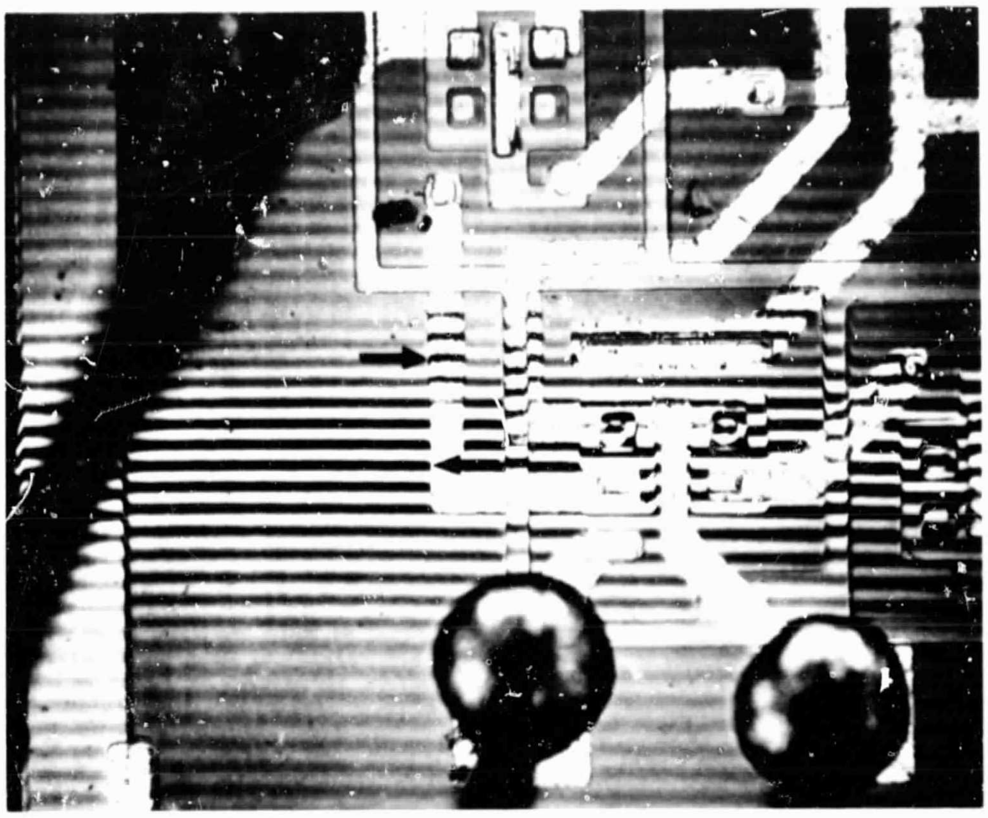
The metallization thickness varied from 1 microcircuit to the next, from 1.6 microns on Sample 14 to 2.8 microns on Sample 44. The metallization thickness measured on each microcircuit is given in Table B-1.

TABLE B-1. METALLIZATION THICKNESS ON FOUR MICROCIRCUITS MEASURED BY INTERFEROMETRY

Sample No.	Metallization Thickness Range	
	Interference Fringes	Microns
14	5.2/5.4	1.56/1.62
23	6.9/7.0	2.07/2.10
34	8.8/8.9	2.64/2.67
44	9.2/9.3	2.76/2.79

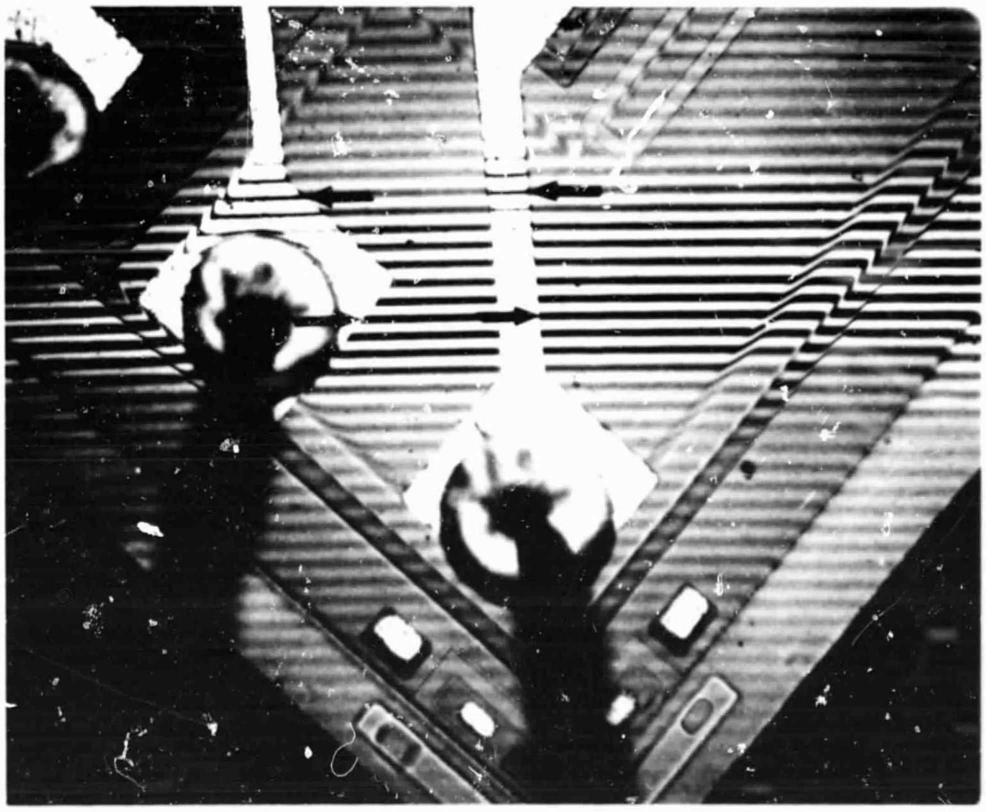
Because the metallization thickness was uniform on each of the four microcircuits, only one representative interference micrograph (Figure B-1 to B-4) from each sample has been included with this report. The corresponding interference fringes on the metallization and die surface are indicated by arrows in these photographs.

The surface of each of the four microcircuits was found to be slightly curved. The relief from center to edge of Samples 23, 34, and 44 was 0.3 micron or less. However, the surface of Sample 14 was found to be domed, with a center-to-edge relief of about 1 micron. Figure B-5 is an interference photomicrograph which illustrates the domed nature of this microcircuit. Sample 14 was also found to be cracked. Perhaps the domed shape and crack are indicative of stresses produced in the silicon die during fabrication of Sample 14.



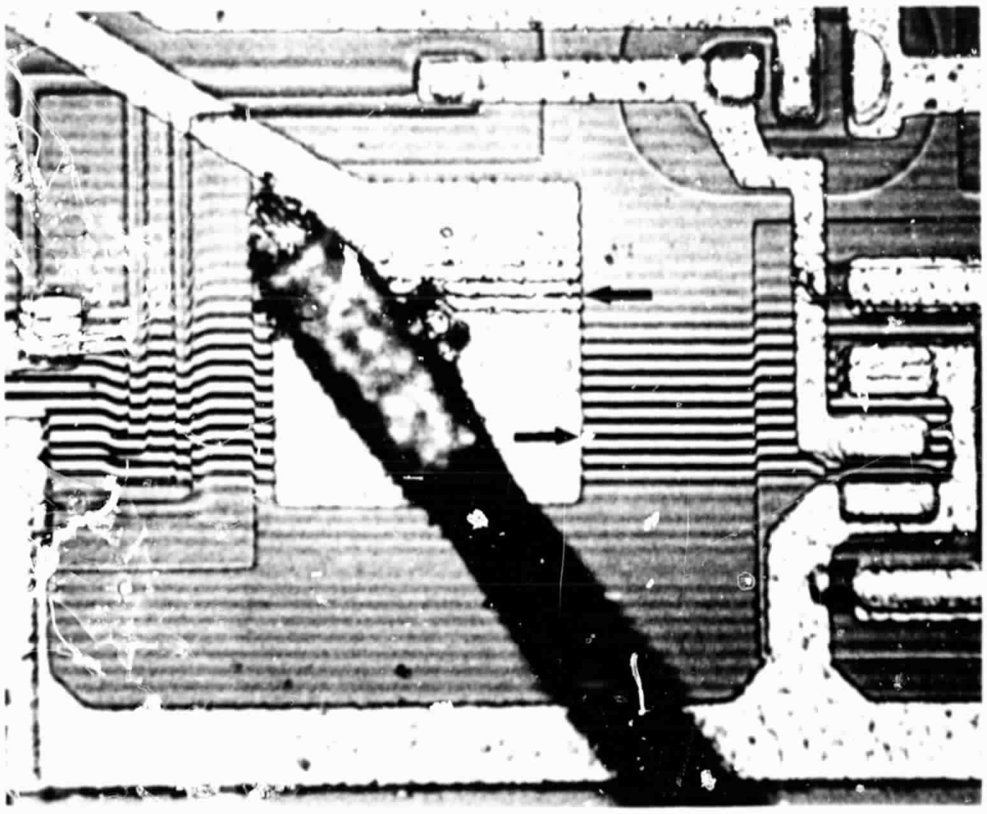
200X 5E919

FIGURE B-1. THE METALLIZATION THICKNESS ON SAMPLE 14 CORRESPONDED TO 5.2 TO 5.3 INTERFERENCE FRINGES OR 1.56 TO 1.59 MICRONS



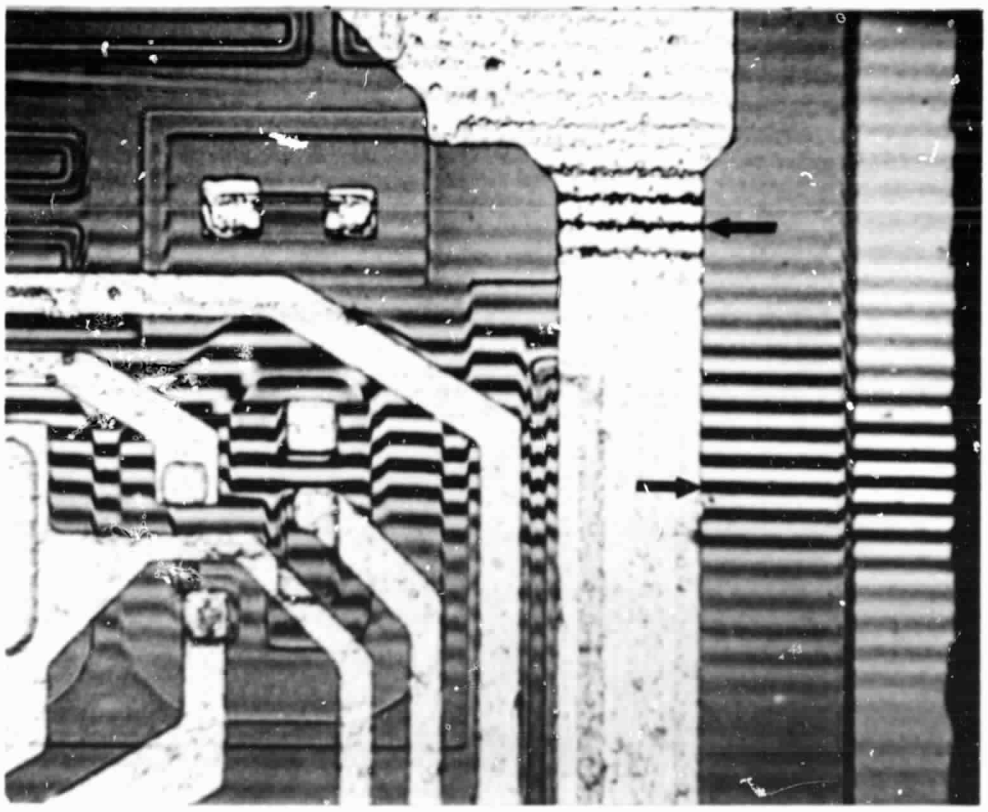
200X 5E918

FIGURE B-2. THE METALLIZATION THICKNESS ON SAMPLE 23 CORRESPONDED TO 6.9 TO 7.0 INTERFERENCE FRINGES OR 2.07 TO 2.10 MICRONS



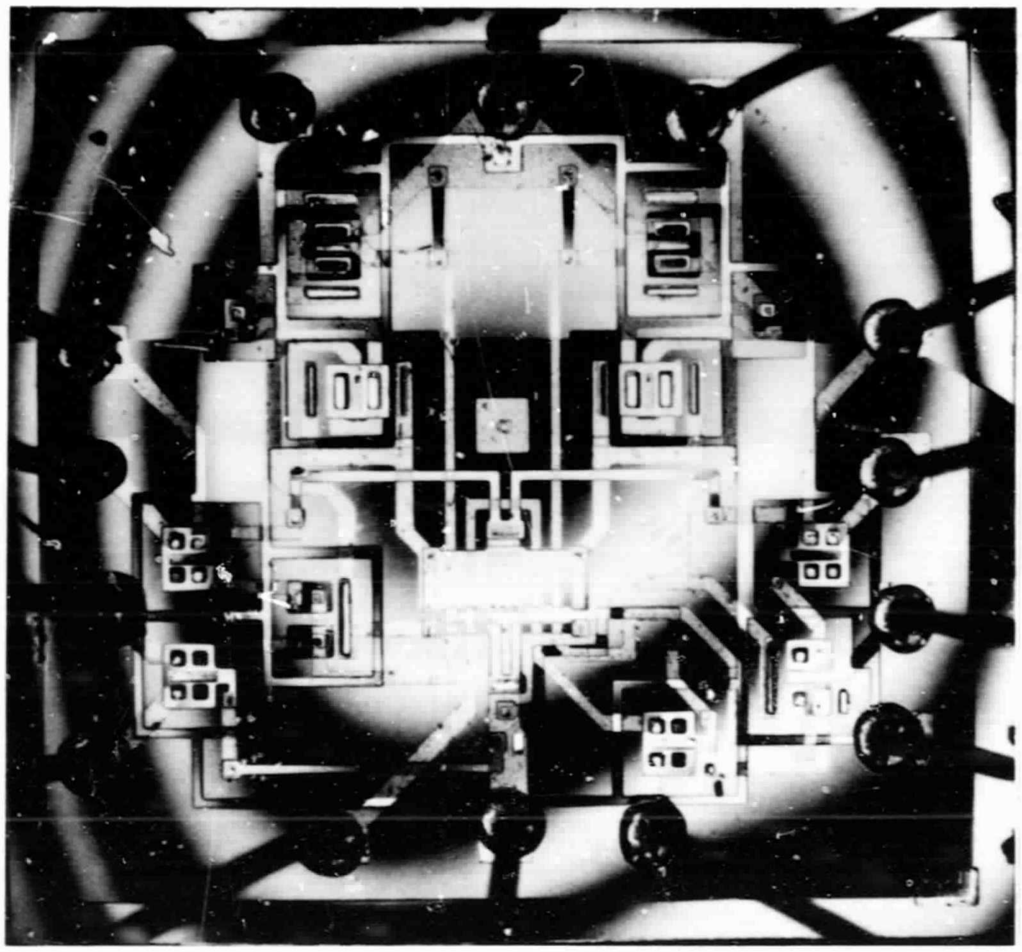
330X 5E917

FIGURE B-3. THE METALLIZATION THICKNESS ON SAMPLE 34 CORRESPONDED TO 8.8 TO 8.9 INTERFERENCE FRINGES OR 2.64 TO 2.67 MICRONS



330X 5E921

FIGURE B-4. THE METALLIZATION THICKNESS ON SAMPLE 44 CORRESPONDED TO 9.2 TO 9.3 INTERFERENCE FRINGES OR 2.76 TO 2.79 MICRONS



78X 5E920

FIGURE B-5. INTERFERENCE FRINGES ADJUSTED TO SHOW THE SPHERICAL SURFACE OF SAMPLE 14

The center to upper left-corner relief is slightly more than 3 interference fringes or about 1 micron.

APPENDIX C

EXAMINATION OF METALLOGRAPHIC CROSS SECTIONS OF MICROCIRCUITS

APPENDIX C

EXAMINATION OF METALLOGRAPHIC CROSS SECTIONS OF MICROCIRCUITS

Six microcircuits were submitted for preparation and examination of metallographic cross sections. The primary purpose of the metallographic examination was to characterize the electrical lead and surface metallization bond to the silicon die. The six microcircuits were identified as follows:

BMI Sample No.	Manufacturer	Part Number
14	A	SN 5451
16	A	SN 5451
23	A	SN 54L51
26	A	SN 54L51
34	B	SN 54L78T
44	B	SN 54L73T

Metallographic Techniques

Each of the submitted microcircuits were mounted in a clear epoxy. While the epoxy was still fluid, the mounts were placed in a vacuum to ensure that all voids or crevices in the specimens would be completely filled with epoxy. Each specimen was oriented in the mount such that the metallographic cross section was perpendicular to the top surface plane of the silicon die.

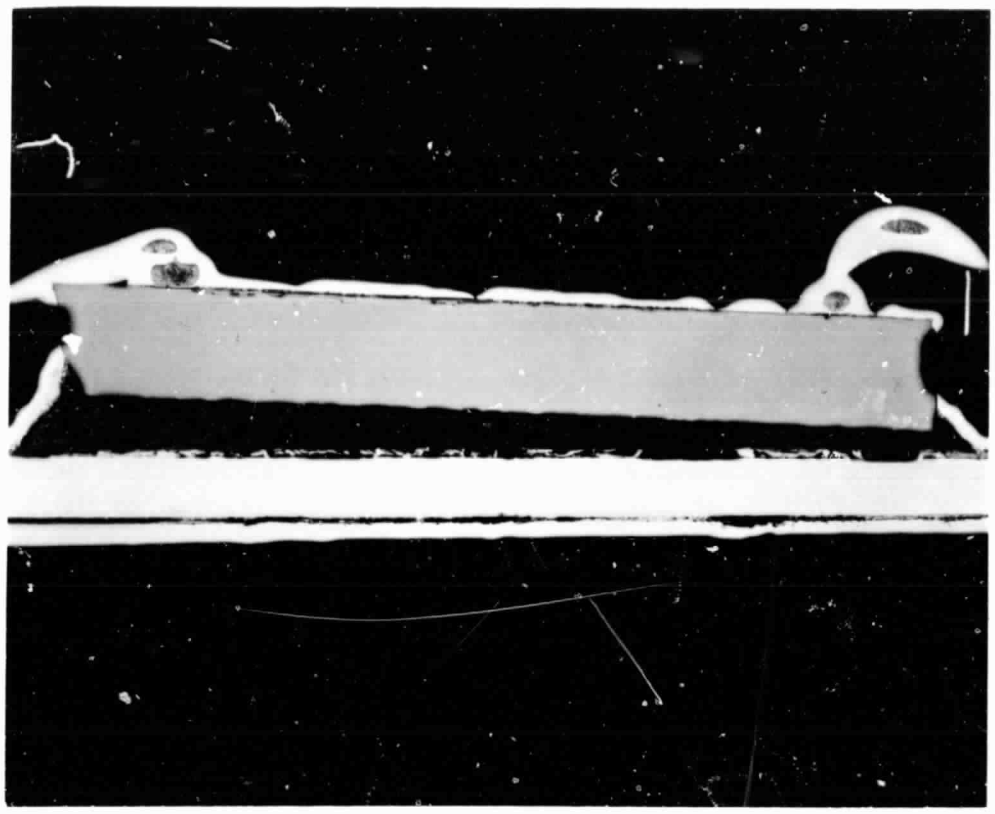
Specimens 14 and 23 were nickel-plated prior to mounting in epoxy. This is done in order to protect the edges of specimens from rounding during polishing. The nickel deposited rather erratically on the microcircuits, and often did not adhere tightly. Intermittent and loosely adhering nickel plating is often found to be more troublesome than helpful in the preparation and examination of metallographic specimens.

Initially, the mounted specimens were hand-ground to the edge of the silicon die on 240-, 400-, and 600-grit silicon carbide paper. The section was then polished to the plane of interest using 1.0-micron diamond abrasive on a silk cloth. All of the polishing was done unidirectionally, i.e., in a direction perpendicular to and toward the top surface of the silicon die. Polishing in other directions or more than one direction resulted in chipping and damage to the edge of the silicon die. Final polishing was performed by a few turns with light pressure on a Microcloth using 0.02μ Al_2O_3 abrasive.

Results

Some of the microcircuits were mounted at an angle to the surface of their package. Consequently, the thickness of the material bonding the circuit to the package varied considerably. The thickness of the bonding material varied from 1.2 to 4.1 mils from one edge to the opposite edge of Specimen 23. This is shown quite well in Figure C-1. Bubbles or voids were commonly observed in the nonmetallic bonding material used between the silicon die and package in Specimens 14, 16, 23, and 26.

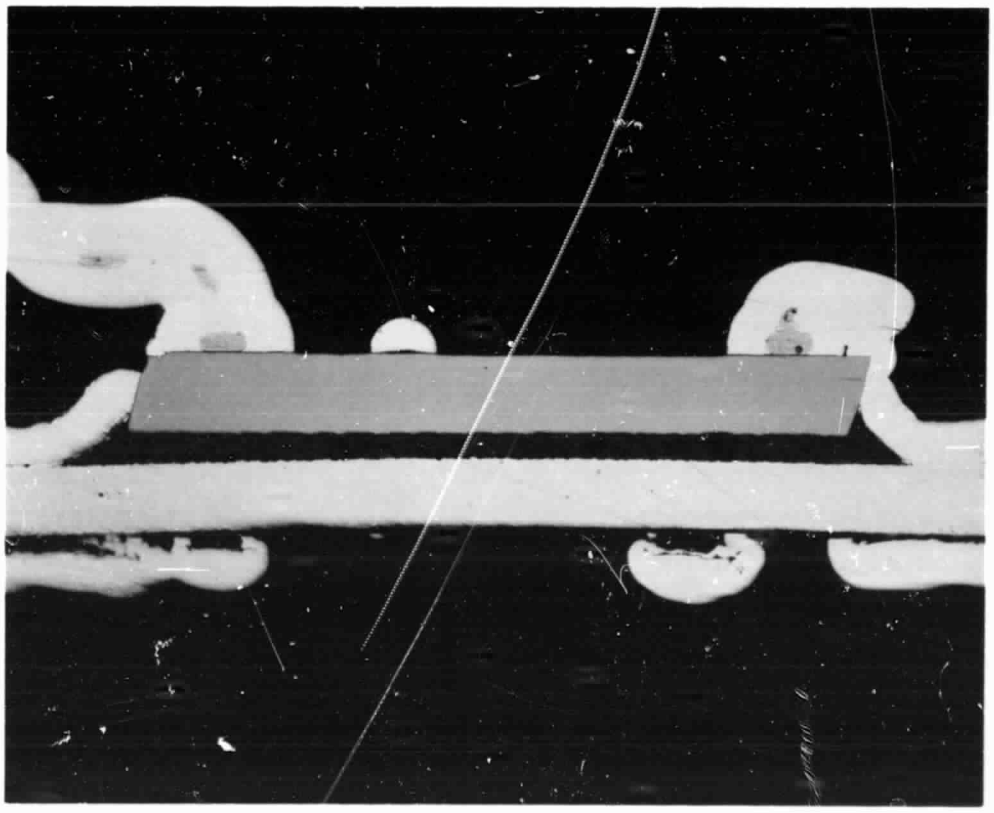
Some of the microcircuits were mounted parallel to the package surface. For example, Figure C-2 shows a cross section of Specimen 14.



60X 5E974

FIGURE C-1. CROSS SECTION THROUGH SPECIMEN 23

The specimen has been nickel plated.



60X 5E957

FIGURE C-2. CROSS SECTION THROUGH TWO GOLD BALL-BONDS ON SURFACE OF SPECIMEN 14

The specimen has been partially nickel plated.

The thickness of the silicon dies varied somewhat. Since the cross sections were perpendicular to the flat surfaces of the dies, the cross-sectional thickness measurements should be accurate. The silicon die of Specimens 14 and 16 (supposedly identical microcircuits from the same lot) were 5.9 and 8.1 mils thick, respectively. The results of the cross-section dimensional measurements on all six submitted specimens are given in Table C-1.

TABLE C-1. DIMENSIONAL MEASUREMENTS ON PERPENDICULAR CROSS SECTIONS OF SIX MICROCIRCUITS

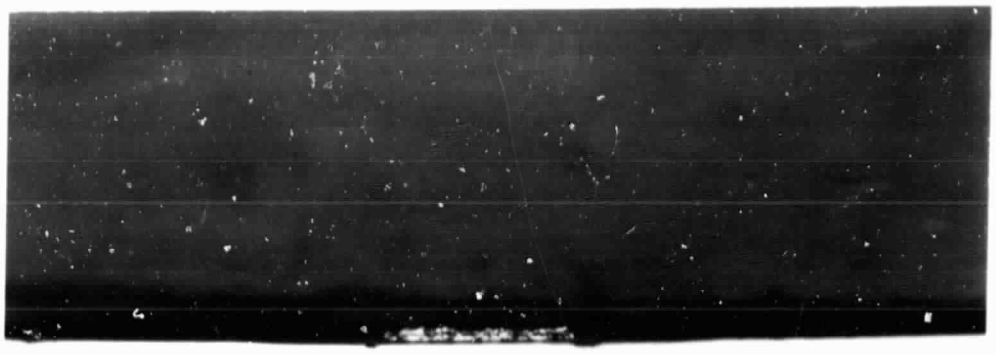
Specimen No.	Silicon Die Thickness, mils	Die/Container Bond Thickness, mils		Type of Bond
		Left Edge	Right Edge	
14	5.9	2.0	2.0	Nonmetallic
16	8.1	1.5	2.1	Nonmetallic
23	7.9	4.1	1.2	Nonmetallic
26	7.8	2.1	1.5	Nonmetallic
34	8.3	0.3	0.7	Metallic
44	8.9	0.4	0.1	Metallic

Examination of the cross sections revealed that a good bond existed between the surface leads and/or metallization to the silicon die in all of the submitted specimens. Surface relief due to polishing was produced between the soft metallized layers and the relatively hard silicon die. Primarily because of the polishing relief, it was not possible to accurately record the appearance of the metallization to silicon bond by optical photomicrography. The sharp relief step at the metallization/silicon interface produced the appearance of a crack or separation under vertical illumination, as illustrated in Figure C-3. By tilting the specimen and using oblique illumination, it was possible to demonstrate that the dark line between the metallization and silicon (as seen in Figure C-3) was in all cases due to polishing relief and was not a line of actual bond separation.

Because of the extremely thin layers of metallization on the surface of the microcircuits, it was not possible to resolve any evidence of diffusion or chemical interaction between the various metal layers and the silicon die. An attempt was made to determine the presence of measurable diffusion or intermetallic compound formation with an electron microprobe analyzer. Unfortunately, the resolution of the microprobe (~1-2 microns) was not sufficient to be of any value in this application.

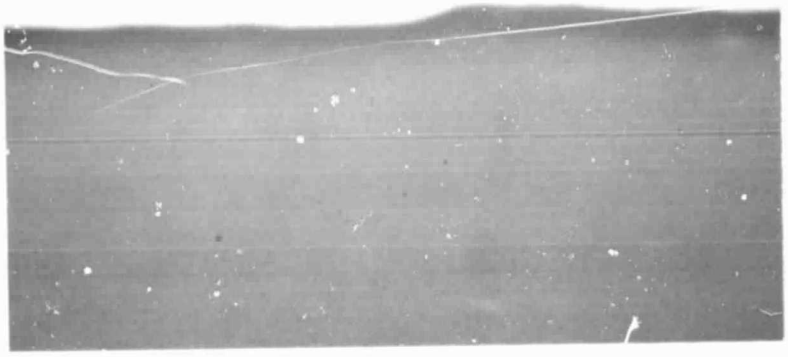
The metallographic cross sections were finally examined in a scanning electron microscope. Because of the similar atomic weights of Al and Si, it was not possible to reveal any details of the metallization bonds on circuits with Al metallization. (The backscattered mode of the scanning electron microscope depends on atomic weight differences to produce image contrast. Also, light elements such as silicon and aluminum produce low signal-to-noise ratios in the scanning microscope, resulting in essentially fuzzy images lacking in detail.)

Two of the microcircuits (Specimen 23 and 26) had metallization consisting of Au on Mo. The bonds between the Au, Mo, and Si on Specimen 23



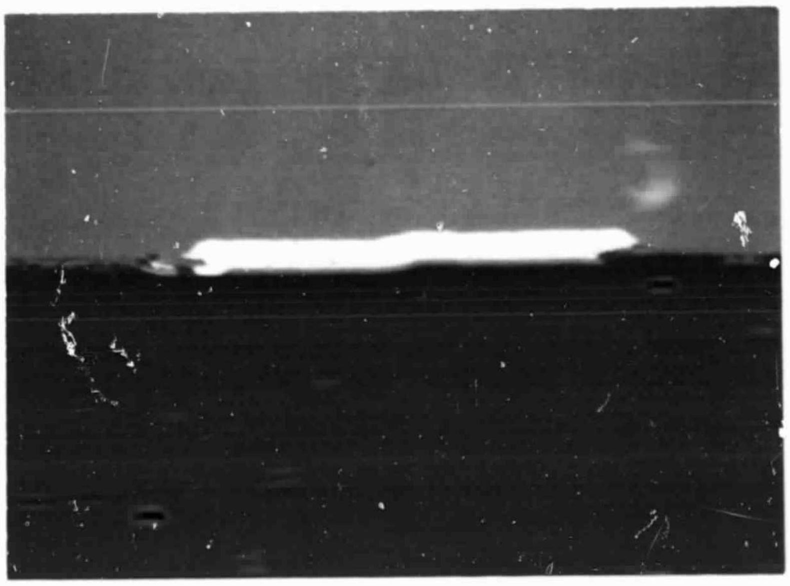
1000X 6E100

FIGURE C-3. CROSS SECTION OF ALUMINUM METALLIZATION LAYER ON SURFACE OF SPECIMEN 14



5000X S1447

FIGURE C-4. BACK SCATTERED ELECTRON IMAGE OF Au/Mo METALLIZATION ON SURFACE OF SPECIMEN 23



2000X S1448

FIGURE C-5. UNDERCUTTING OF Au LAYER OF Au/Mo METALLIZATION ON SURFACE OF SPECIMEN 23 were examined in the scanning electron microscope and were found to be continuous. No evidence of poor bonding was found. Figure C-4 is a photograph showing a typical metallization layer on Specimen 23. The specimen had been nickel-plated prior to metallographic preparation, so the various layers represented in Figure C-4 are (from top to bottom) nickel, gold, molybdenum, and silicon. No evidence of lack of bonding, interdiffusion, or intermetallic compound formation was observed.

Some evidence of undercutting at the edges of metallization layers was observed in the scanning electron microscope surface studies. Figure C-5 is a scanning micrograph of a cross section of a metallization layer on Specimen 23 where undercutting of the gold layer can be seen.