

General Disclaimer

One or more of the Following Statements may affect this Document

- This document has been reproduced from the best copy furnished by the organizational source. It is being released in the interest of making available as much information as possible.
- This document may contain data, which exceeds the sheet parameters. It was furnished in this condition by the organizational source and is the best copy available.
- This document may contain tone-on-tone or color graphs, charts and/or pictures, which have been reproduced in black and white.
- This document is paginated as submitted by the original source.
- Portions of this document are not fully legible due to the historical nature of some of the material. However, it is the best reproduction available from the original submission.

27

DEVELOPMENT OF GaAs AND GaAs_{1-x}P_x THIN-FILM BIPOLAR TRANSISTORS

BY

J. P. DISMUKES, R. H. DEAN, AND C. J. NUESE

FINAL REPORT

DECEMBER 1969

Distribution of this report is provided in the interest of information exchange and should not be construed as endorsement by NASA of the material presented. Responsibility for the contents resides with the organization that prepared it.

PREPARED UNDER CONTRACT NO. NAS 12-2091

RCA LABORATORIES
PRINCETON, NEW JERSEY

ELECTRONICS RESEARCH CENTER
CAMBRIDGE, MASSACHUSETTS
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

70-26272

(ACCESSION NUMBER)	(THRU)
31	1
(PAGES)	(CODE)
CR-86361	09
(NASA CR OR TMX OR AD NUMBER)	(CATEGORY)

FACILITY FORM 602

DEVELOPMENT OF GaAs AND GaAs_{1-x}P_x THIN-FILM BIPOLAR TRANSISTORS

BY

J. P. DISMUKES, R. H. DEAN, AND C. J. NUESE

FINAL REPORT

DECEMBER 1969

Distribution of this report is provided in the interest of information exchange and should not be construed as endorsement by NASA of the material presented. Responsibility for the contents resides with the organization that prepared it.

PREPARED UNDER CONTRACT NO. NAS 12-2091

RCA LABORATORIES
PRINCETON, NEW JERSEY

ELECTRONICS RESEARCH CENTER
CAMBRIDGE, MASSACHUSETTS
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

TABLE OF CONTENTS

<u>Section</u>	<u>Page</u>
SUMMARY	1
I. INTRODUCTION	3
II. TECHNICAL DISCUSSION	4
A. N-P-N GaAs Transistors	4
1. Fabrication Techniques	4
2. Transistor Characteristics	9
B. P-N-P GaAs _{1-x} P _x Transistors	14
1. Fabrication Techniques	14
2. Transistor Characteristics	15
C. Electrical Behavior of Vapor-Grown p-n Junctions.	15
1. Lifetime and Diffusion Length	15
2. I-V and C-V Characteristics	20
3. Reverse Currents.	22
III. CONCLUSIONS AND RECOMMENDATIONS	23
IV. REFERENCES	24
V. NEW TECHNOLOGY APPENDIX	24
APPENDIX Doping of Vapor-Grown GaAs	25

LIST OF ILLUSTRATIONS

<u>Figure</u>	<u>Page</u>
1. Schematic representation of vapor-grown transistor structures	4
2. GaAs sputter-etched transistor array	5
3. Fabrication steps for n-p-n GaAs sputter-etched transistors	6
4. Sputter-etched GaAs n-p-n transistor after complete fabrication	7
5. Vapor-growth of GaAs transistor structure through SiO ₂ mask	8
6. GaAs n-p-n transistor prepared with vapor-regrown p-type channel to the base	9
7. I-V characteristics of vapor-grown n-p-n transistor prepared by sputter-etching	10
8. Effect of sputter-etch damage on vapor-grown junctions	11
9. Transistor currents in regrown or Zn-diffused GaAs transistor structures	12
10. I-V characteristics of vapor-grown n-p-n transistor: sputter-etched vs. vapor-regrown channel to base . . .	12
11. I-V characteristics of n-p-n GaAs transistors prepared by Zn-diffused channel	13
12. Apparatus for lifetime measurements in GaAs _{1-x} P _x p-n junctions	16
13. Minority-carrier lifetimes vs. GaAs _{1-x} P _x p-n junctions	17
14. Minority-carrier diffusion lengths vs. GaAs _{1-x} P _x alloy composition, x	18
15. Temperature dependence of minority-carrier lifetimes in GaAs _{1-x} P _x p-n junctions	19
16. Common-emitter current gain as a function of the ratio of diffusion length to base width for GaAs _{1-x} P _x n-p-n and p-n-p transistors	20

LIST OF ILLUSTRATIONS (Cont'd)

<u>Figure</u>		<u>Page</u>
17.	C-V characteristics of GaAs and GaAs _{0.55} P _{0.45} vapor-grown junctions at room temperature and 300°C	21
18.	Reverse currents in GaAs _{1-x} P _x p-n junctions at 300°C vs alloy composition	22
A-1.	Electron concentration in GaAs vs. H ₂ Se concentration in gas phase	25
A-2.	Hole concentration in GaAs vs. temperature of Zn source.	26

DEVELOPMENT OF GaAs AND GaAs_{1-x}P_x THIN
FILM BIPOLAR TRANSISTORS

by

J. P. Dismukes, R. H. Dean, and C. J. Nuese

RCA Laboratories
Princeton, New Jersey

SUMMARY

The purpose of this research is to develop a vapor-grown bipolar transistor of either GaAs or GaAs_{1-x}P_x capable of operation at a minimum ambient temperature of 300°C, and to evaluate its characteristics.

During this investigation, the first n-p-n GaAs and p-n-p GaAs_{0.55}P_{0.45} transistors prepared entirely by a vapor-phase growth technique have been fabricated. Utilizing a sputter-etch technique for exposing the 1- to 2 μ-thick base layers of n-p-n GaAs transistor structures, we have been able to fabricate individual transistors with common emitter current gains as large as 10 at room temperature. The gain of several GaAs transistors with gains of 2 to 3 have been found to be relatively independent of temperature between 25° and 300°C. Furthermore, leakage currents in the vapor-grown transistors have not been significant, even at 300°C. In addition, one GaAs transistor has been held at 300°C for over 100 hours with no observable change in its high-temperature I-V characteristics.

P-n-p GaAs_{0.55}P_{0.45} transistors have also been successfully fabricated by employing a NaOH electrolytic etching technique to expose the base region. However, common emitter current gains for the GaAs_{0.55}P_{0.45} transistors were less than 1, due to the short hole diffusion length measured for such junctions.

An extensive evaluation has been made of the I-V and C-V characteristics and of the minority-carrier lifetime in GaAs and GaAs_{1-x}P_x vapor-grown p-n junctions over the temperature range 25° to 300°C. Reverse currents at 300°C decrease with increasing GaAs_{1-x}P_x alloy composition from a value of 3 x 10⁻² A/cm² at x = 0, to about 5 x 10⁻⁴ A/cm² at x = 0.6. I-V and C-V measurements at high temperatures indicate that the impurity distributions and the injection and recombination mechanisms do not change significantly between 25 and 300°C. Minority hole and

electron lifetimes in GaAs and GaAs_{1-x}P_x p-n junctions are about 10 and 5 nsec, respectively for $x \lesssim 0.3$. However, because of the high electron mobility in GaAs and in As-rich alloys of GaAs_{1-x}P_x, the diffusion length for electrons in such junctions is about 6 to 8 μ , whereas that of holes is only about 2 μ .

Based on the data obtained under this contract, a simple calculation indicates that gains of up to 50 are possible for n-p-n vapor-grown transistors with base widths of 1 μ . In addition, such gains would be virtually temperature independent in the range of 25° to 300°C.

I. INTRODUCTION

The potential of GaAs for high-temperature devices, including transistors, is a well-established fact. Indeed, RCA was one of the pioneers in this field. However, this potential has never been fully realized. For GaAs bipolar transistors, this is in part due to the relatively short minority-carrier lifetimes, which necessitate a narrow base region, thereby introducing severe fabrication difficulties. In the past, the use of high temperature (900°C - 1000°C) processing steps, such as diffusion, has made it difficult to define narrow regions while maintaining good p-n junction characteristics. As a result, large reverse leakage currents have been observed, particularly at high operating temperatures ($\geq 300^{\circ}\text{C}$). In addition, the high temperature processing often creates problems of reduced lifetime and thermal conversion.

Our approach to the fabrication of high-temperature GaAs or $\text{GaAs}_{1-x}\text{P}_x$ transistors involves the preparation of n-p-n⁺ or p-n-p⁺ three-layered structures by a vapor-phase growth technique [1]. The low growth temperature of $\approx 750^{\circ}\text{C}$ used here reduces contamination, and contributes to the reasonably high minority-carrier lifetimes ($> 10^{-8}$ sec) obtained for vapor-grown p-n junctions. The fact that impurity concentrations, layer thicknesses, and alloy composition can be precisely controlled for epitaxial layers as thin as $1\ \mu\text{s}$ is an important vapor-growth feature. The application of this technique to the fabrication of GaAs or $\text{GaAs}_{1-x}\text{P}_x$ transistors therefore appears to be reasonable. It is the purpose of the present research to evaluate the effectiveness of this vapor-growth approach, with an end goal of reproducibly preparing transistors capable of operation in a 300°C ambient.

The high electron mobility of GaAs and the large energy gap of $\text{GaAs}_{1-x}\text{P}_x$ each offer advantages for the successful development of a high-temperature transistor. Hence, in an attempt to clearly delineate the advantages and disadvantages of each, the initial efforts under this contract have included both n-p-n GaAs and p-n-p $\text{GaAs}_{1-x}\text{P}_x$ transistors. Our research has also included an extensive investigation of the basic high-temperature characteristics of vapor-grown p-n junctions, including measurements of the I-V and C-V characteristics and of the minority-carrier lifetimes at temperatures as high as 500°C . The results of our evaluation of such junctions and transistors for high-temperature applications are the subject of this report.

II. TECHNICAL DISCUSSION

A. N-P-N GaAs Transistors

1. Fabrication Techniques. -- The strength and potential of our approach to fabricating high-temperature GaAs transistors relies on the promise of high-quality p-n junctions, vapor-grown in the three-layered n-p-n structures shown in Figure 1.

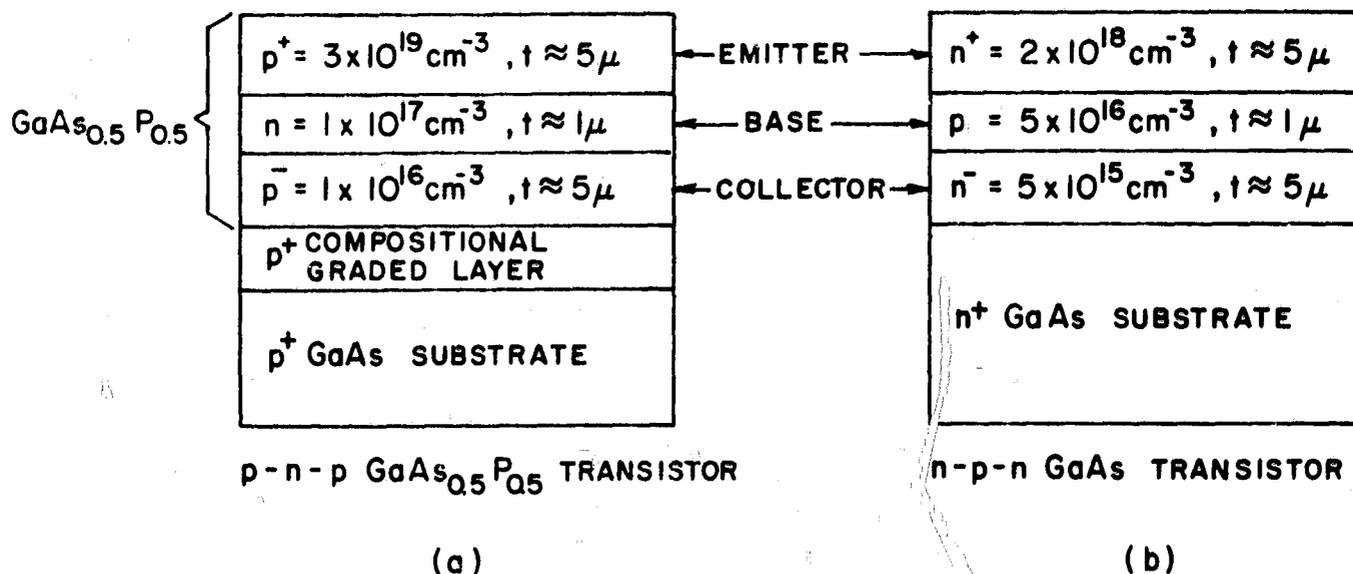


Figure 1 - Schematic representation of vapor-grown transistor structures.

Here, the large emitter/base doping concentration ratio provides a high minority (electron) injection into the base, while the large base/collector doping ratio causes the base-collector depletion layer to extend primarily into the collector. (See the Appendix for a discussion of the doping technique.) An extension of the depletion layer into the base, instead, is undesirable since the base transport factor, and hence the transistor current gain, then becomes strongly dependent on the applied voltage.

The successful development of the vapor-grown transistor shown in Figure 1 requires a satisfactory technique for exposing and contacting the very thin base layer sandwiched between the emitter and collector layer. At the beginning of this contract, no suitable technique had yet been developed for this purpose. Accordingly, during this contract we have investigated a variety of techniques for exposing selected regions of the base, including:

1. Chemical etching of holes through the emitter
2. Sputter etching of holes through the emitter

3. Vapor-growth of the collector and base layers, followed by SiO₂ masking and regrowth of emitter mesas
4. Diffusion of a p-type channel into or through the base from the uppermost emitter surface
5. Regrowth of a p-type channel after etching holes into or through the base.

Two chemical etchants investigated for the purpose of exposing the base are (H₂SO₄, H₂O₂, H₂O) and (NaOH, H₂O₂). Both of these polish etches provide relatively smooth, flat surfaces. However, their etching rates are difficult to control with sufficient accuracy to etch through the emitter layer without penetrating the thin ($\approx 1 \mu$) base layer. No transistors have been fabricated by chemical etchants primarily for this reason.

The sputter-etch technique, to the contrary, has frequently been used for our transistor fabrication, and has been a key factor in preparing GaAs transistors with current gains as high as 10. During our investigation we have sputter-etched GaAs at rates of 1000 Å/min to depths of 3 to 5 μ , with control of the final depth to within 0.1 μ . The use of a simple molybdenum mask has provided a resolution of about 1 mil, and has been used to sputter-etch transistor arrays like those shown in Figure 2.

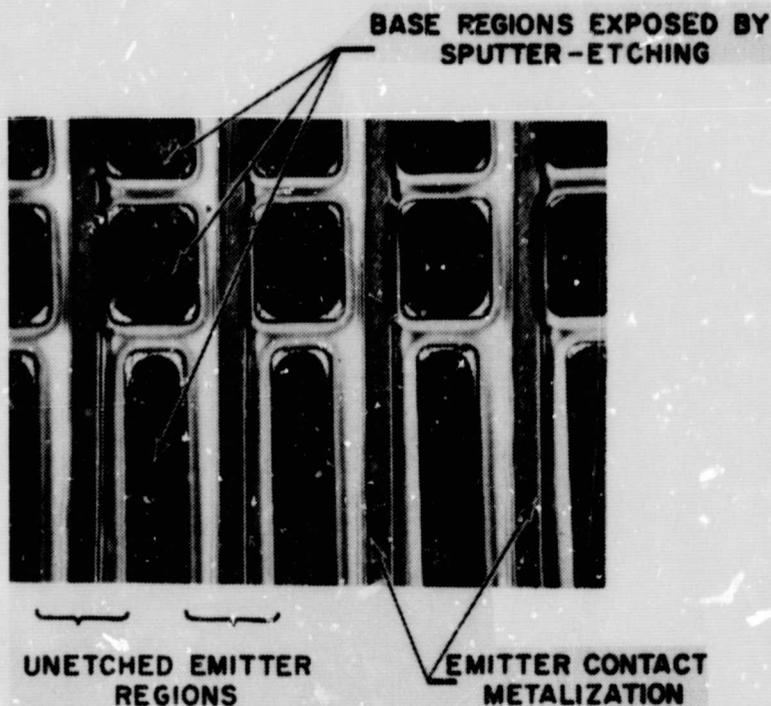


Figure 2 - GaAs sputter-etched transistor array.

The fabrication procedure used in the preparation of sputter-etched transistors is shown in Figure 3 and is outlined briefly below.

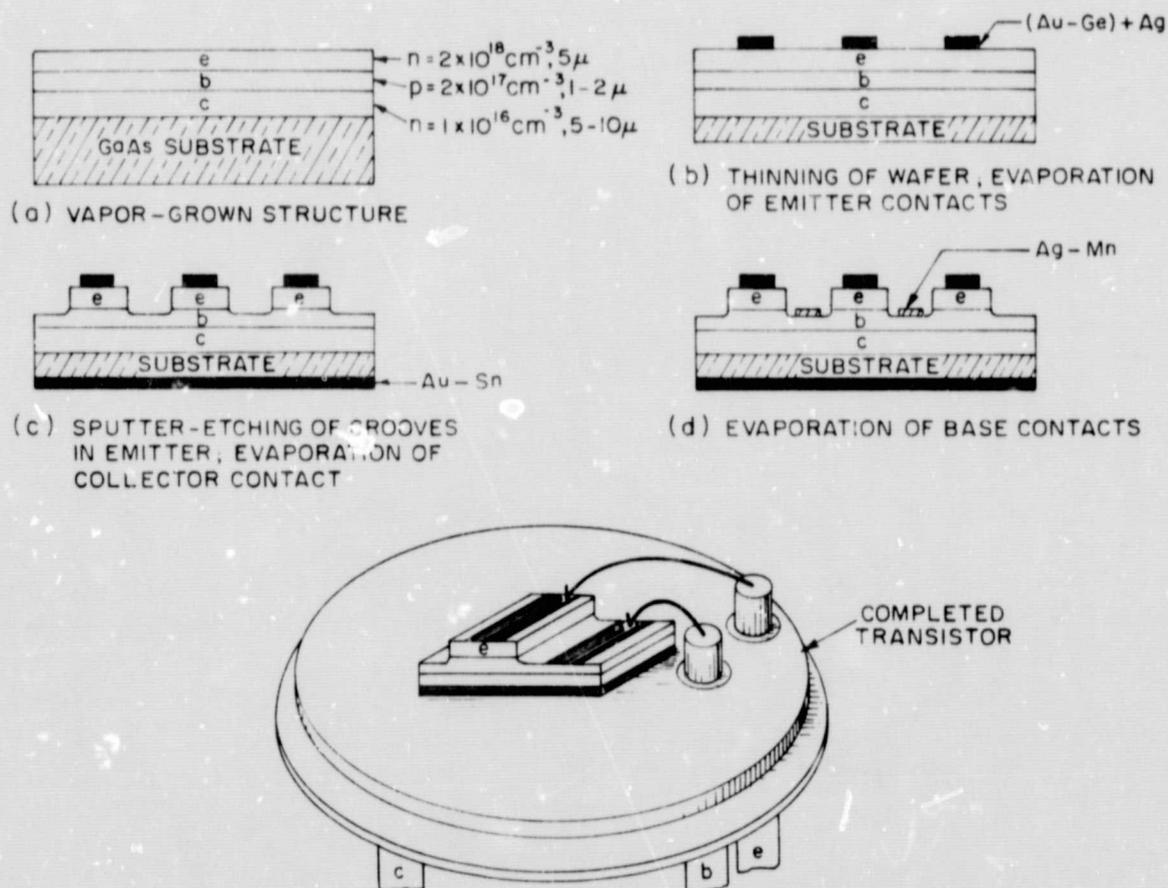


Figure 3 - Fabrication steps for n-p-n GaAs sputter-etched transistors.

The first step in the fabrication is to evaporate consecutive layers of Au-Ge and Ag through a metal mask onto the emitter (Figure 3b), and to sinter the contacts for about 2 min at 550°C in H₂. After lapping the substrate side of the wafer to a total thickness of 5 mils, grooves are sputter-etched in the emitter (Figure 3c) using a simple molybdenum mask to define the pattern. A film of Au-Sn is then evaporated onto the lapped substrate to serve as a collector contact (Figure 3c), and stripes of Ag-Mn[2] are evaporated onto the exposed regions of the base (Figure 3d). The base and collector contacts are simultaneously sintered at 550°C in H₂. The wafer is finally diced into individual transistors, approximately 0.5 mm² in area, which are then mounted on TO-5 headers and contacted with Au leads by conventional ultrasonic wire-bonding. A schematic drawing and photomicrograph of a sputter-etched GaAs transistor after complete fabrication are shown in Figure 3 and Figure 4, respectively. Evaluation of such transistors is described in detail in Section II.2 on page 9.

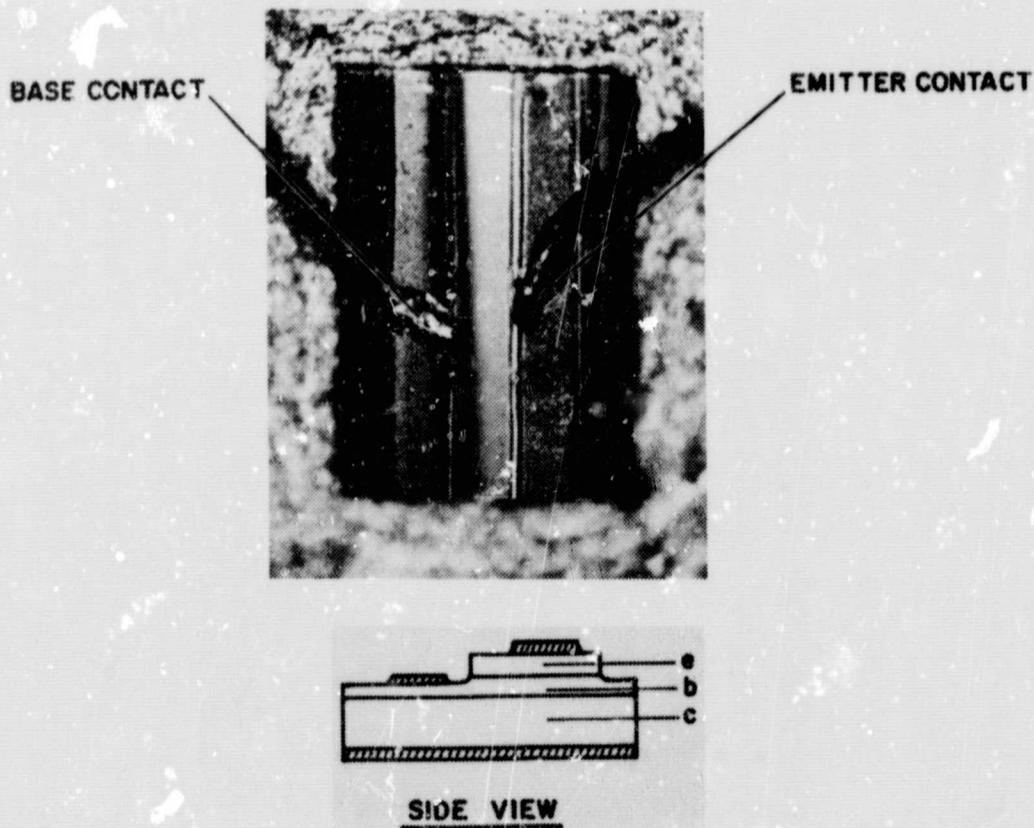


Figure 4 - Sputter-etched GaAs n-p-n transistor after complete fabrication.

The technique of masking a base layer with SiO_2 and depositing the emitter layer through holes etched in selected regions of the SiO_2 was suggested in our technical proposal, Descriptive Specification PP68-080. To evaluate this technique, several vapor-grown GaAs p-n junctions have been prepared in this fashion and evaluated electrically. The reverse currents of these junctions, however, were about 1 A/cm^2 at 300°C which is about a factor of 20 larger than current densities for uninterrupted vapor-grown junctions. Furthermore, a three-layered n-p-n transistor structure was similarly prepared (Figure 5) and contacted, but no transistor action was observed due to the inferior junctions. In light of these difficulties, preliminary research efforts with vapor-phase regrowth have been discontinued in favor of sputter-etching. However, the simple geometry provided by regrowth is a strong advantage of this technique, and it may well justify further research efforts in the future. In this regard, in situ chemical etching immediately prior to growth and annealing of regrown junctions offers untried possibilities.

The diffusion of a small p-type channel through the emitter and into the base was proposed in our Descriptive Specification PP68-080 as a method for contacting the intermediate base layer of an n-p-n GaAs transistor. The virtue of this method is that it is possible to penetrate *through* the base layer without deleterious effects, and therefore it can be used with smaller

transistor base widths ($< 1 \mu$) than those presently employed for sputter-etching ($\approx 1 \mu$). Experiments carried out during this contract investigation have shown that an 80-minute Zn-diffusion at 700°C is adequate for penetrating a base layer located 3 to 4μ below the epitaxial surface.

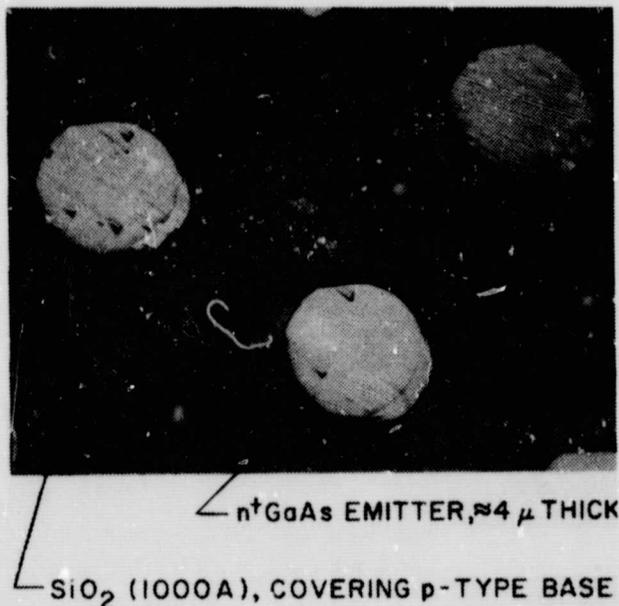


Figure 5 - Vapor-growth of GaAs transistor structure through SiO₂ mask.

A 5000 \AA -thick layer of phosphorus-doped SiO₂ is deposited on the emitter surface at 500°C and is used as a diffusion mask for this process. GaAs transistors with current gains up to 5 have been thus prepared, and are described further in Section II.2. Their fabrication is straight forward since both the emitter and the Zn-diffused channel to the base are located on the uppermost epitaxial surface. Thus far, no thermal conversion has occurred in the n-type collector layers doped as low as $5 \times 10^{15} \text{ cm}^{-3}$ during the low-temperature Zn-diffusion. By comparison, during the fabrication of *diffused* n-p-n GaAs transistors[3], the diffusion of donors (S, Se, Te, etc.) to form an emitter in a moderately doped base layer requires temperatures on the order of 1000°C , and it is known to convert n-type GaAs with $n < 10^{16} \text{ cm}^{-3}$ to p-type.

Lastly, we have also fabricated a few GaAs transistors by first etching an array of holes through selected regions of the emitter *and* the base layers, and by then depositing p-type GaAs into the holes by vapor-phase growth. A transistor prepared in this fashion is shown in Figure 6. The geometry with the regrown

p-type channel is identical to that previously described for the Zn-diffused channel. In both cases, the ohmic contacts are provided by the evaporation of Ag-Mn to the base channel, and Au-Ge followed by Ag to the emitter.

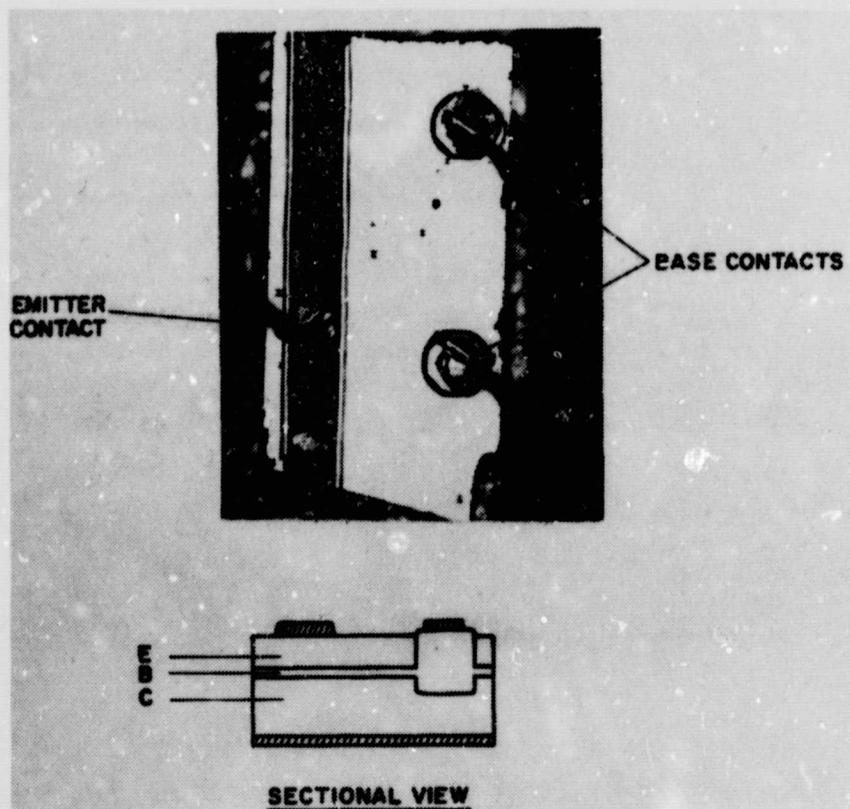


Figure 6 - GaAs n-p-n transistor prepared with a vapor-regrown p-type channel to the base.

2. Transistor Characteristics. -- Most transistors thus far investigated have utilized sputter-etching for exposing selected regions of the base for contacting. For initial n-p-n wafers, with 2μ base widths, current gains on the order of 2 to 3 were obtained, as described in Quarterly Report No. 2. However, more recent wafers, with $1.5\text{-}\mu$ base widths, have yielded transistors with room-temperature current gains of 10, as shown in Figure 7. Unfortunately, the specific transistors with gains of 10 were not adequately bonded to allow high-temperature evaluation, although sputter-etched transistors from the same vapor-grown wafer, but with lower current gains of 2 to 3, were found to have the same gain at 25°C and 300°C . In addition to a narrower base, the recent sputter-etched transistors had somewhat lower base doping concentrations, about $2 \times 10^{17} \text{ cm}^{-3}$ rather than $5 \times 10^{17} \text{ cm}^{-3}$. Lower base doping should result in higher emitter injection efficiencies and longer electron recombination times, both of which lead to higher transistor current gains. Efforts to further reduce the base doping and base width of n-p-n GaAs transistor structures are in progress.

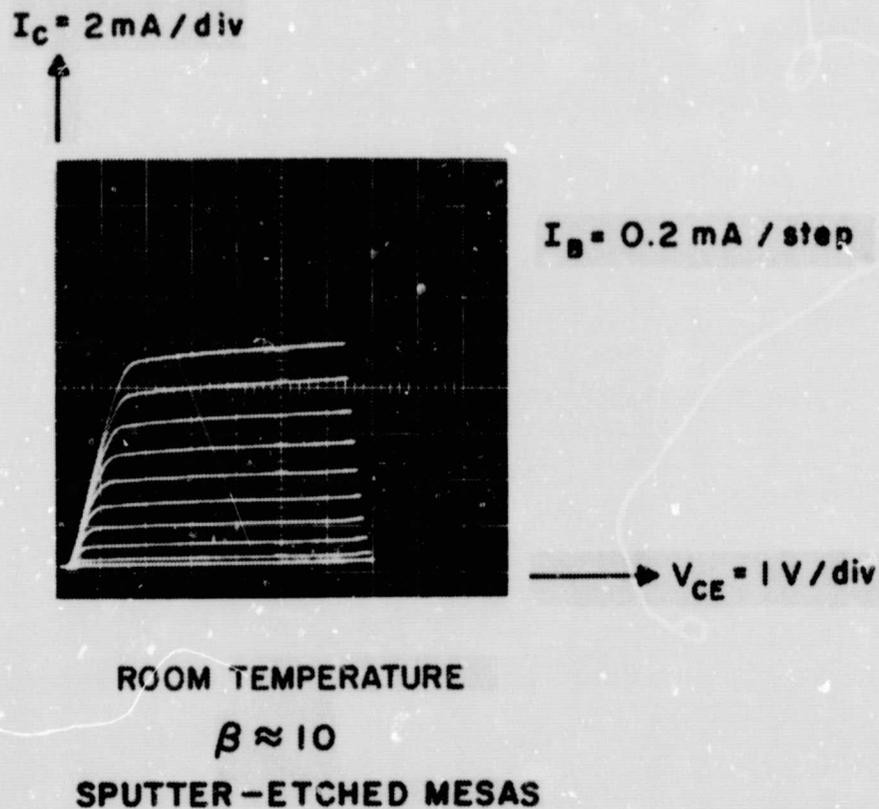


Figure 7 - I-V characteristics of vapor-grown n-p-n transistor prepared by sputter-etching.

One problem evident in the I-V characteristics of Figure 7 is the relatively large saturation resistance associated with the sputter-etched transistors. The saturation resistance of $\approx 200 \Omega$ in Figure 7 is due to a relatively large series resistance in either the emitter or collector layers or in the contacts to them. Further consideration of this problem is required to determine and eliminate the source of this problem.

The possibility of surface damage being induced by the sputter-etch process is under present consideration. In this regard, a vapor-grown n^+ -p wafer was partly masked with molybdenum and exposed to sputtering until the p-n junction of the unmasked areas was penetrated by the etching. In this way, mesas were formed by the sputter-etching, as shown in Figure 8. The room-temperature I-V characteristics of such diodes were compared with those of unetched diodes fabricated from the same vapor-grown wafer. Their I-V characteristics are nearly identical, with no evidence of surface leakage in either case. Although these diodes must also be similarly compared at high temperatures, where leakage currents are significantly larger, the room-temperature results in Figure 8 suggest that the extent of sputter-etch damage to our vapor-grown junctions is relatively small.

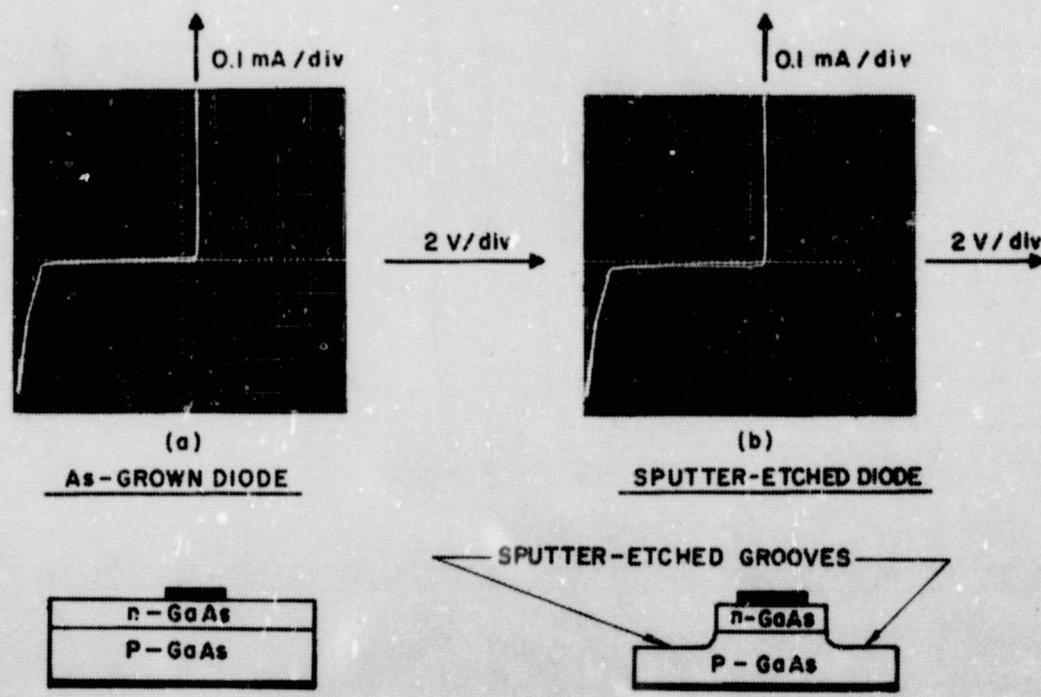


Figure 8 - Effect of sputter-etch damage on vapor-grown junctions.

As described in the previous section, an alternate technique (to sputter-etching) for the fabrication of n-p-n GaAs transistors is the formation of a p-type channel from the emitter to the base, which then allows contacting of the base to be made on the uppermost (exposed) portion of the wafer. During our research, channels formed both by Zn-diffusion and by vapor-phase regrowth have yielded successful GaAs transistors with common-emitter current gains as high as 5.

The basic structure for a channel-type n-p-n transistor is shown in Figure 9. The room-temperature I-V characteristics for such a GaAs transistor with a 1.5μ base width is compared with those for a sputter-etched transistor in Figure 10. The negative incremental resistance which is evident in the uppermost curves of Figure 10a may result from slight shifts in the I-V characteristics due to heating at the highest current levels (200 mA). Note in Figure 10 the low saturation resistance ($\approx 8 \Omega$) generally observed for transistors prepared with p-type channels to the base, in contrast to the high saturation resistance ($\approx 200 \Omega$) for sputter-etched transistors. The reason for the difference in the saturation resistances is not certain, but probably involves the effective resistance of the emitter and the detailed manner in which the currents travel across the active junction in the two different structures.

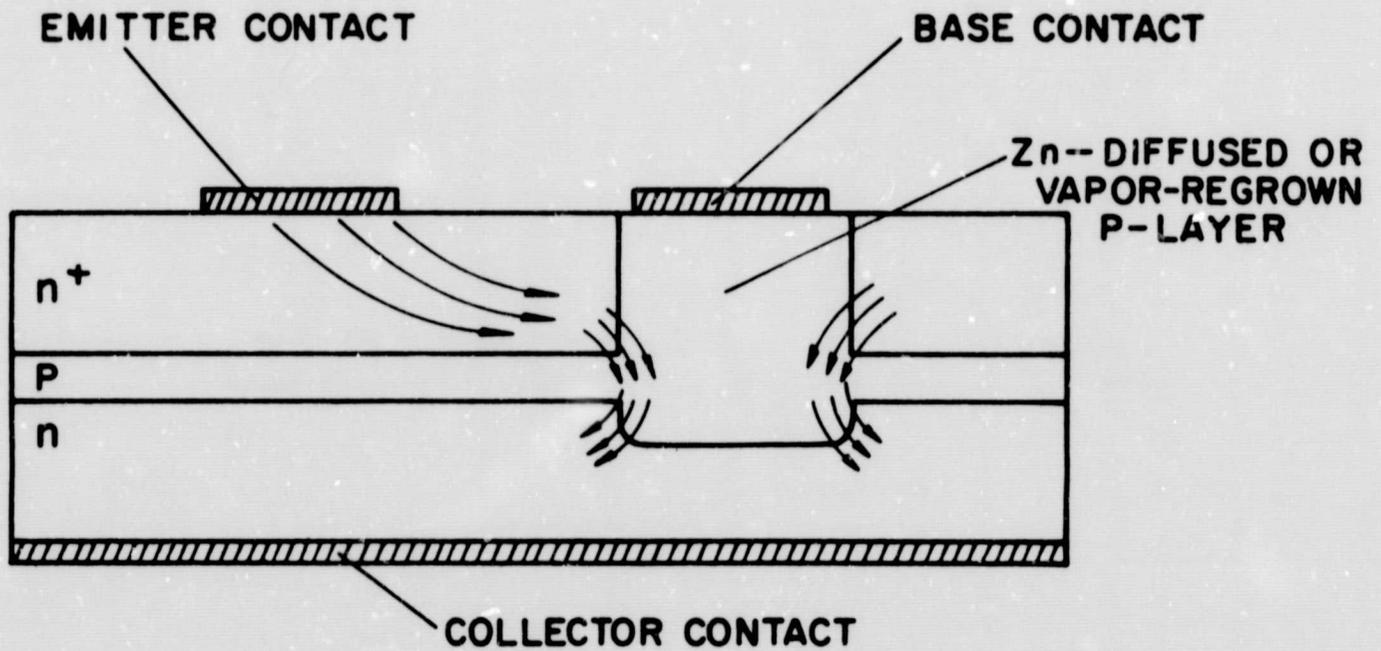
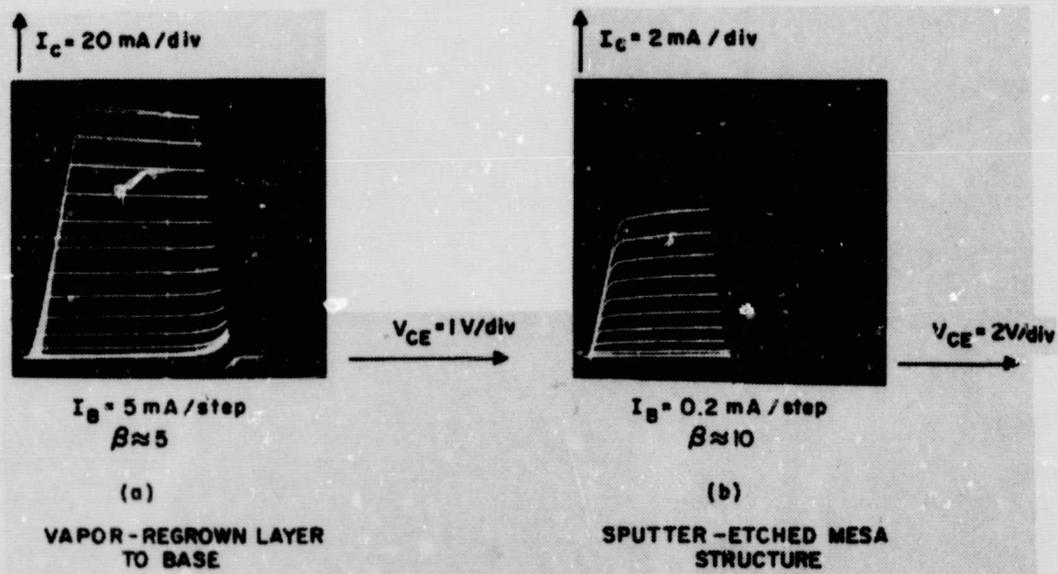


Figure 9 - Transistor currents in regrown or Zn-diffused GaAs transistor structures.



**GeAs n-p-n TRANSISTORS
(MATERIAL 9-924)**

Figure 10 - I-V characteristics of vapor-grown n-p-n transistors: sputter-etched vs. vapor-regrown channel to base.

In this regard, the active junction for transistors with the p-type channel is known to be located primarily at the periphery of the channel, as shown in Figure 9. When the base-emitter junction of the vapor-regrown transistor is forward-biased, infrared bandgap radiation is emitted only in the channel region, suggesting that the transistor action occurs via the current paths shown in Figure 9. The reason for the current passing primarily through the contact region is due to the relatively large resistance of the base layer. The thin, 1μ , base layer doped to only about 10^{17} cm^{-3} , causes a significant voltage drop to occur between the base and emitter contacts, so that the effective voltage across the junction is greatest near the base contact, thereby causing a significantly larger forward current injection in this area. We should mention that even for the current paths indicated, the current gain is primarily determined by the width of the original vapor-grown p-n junction.

Extensive high-temperature evaluation was carried out for the transistors with a Zn-diffused channel to the base. The I-V characteristics of such a transistor at 25°C and at 300° are shown in Figure 11. In both cases, a current gain of about 2

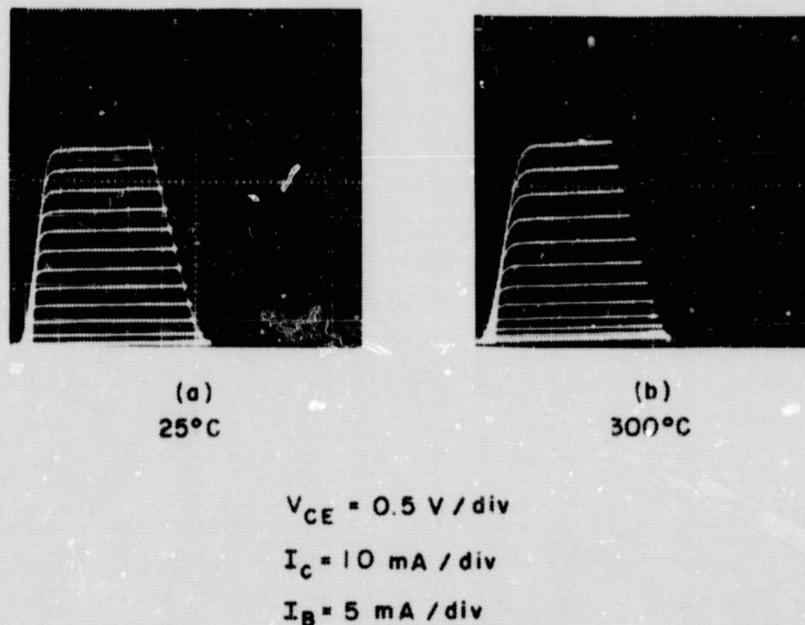


Figure 11 - I-V characteristics of n-p-n GaAs transistors prepared by Zn-diffused channel.

was measured for an n-p-n structure with a $1.5\text{-}\mu$ base width. Particularly encouraging is the absence of significant leakage currents in the I-V characteristics of Figure 11, even at high temperatures where leakage is most severe. This observation is

consistent with the relatively low reverse currents measured in our vapor-grown junctions at 300°C (described in Section II.C. on page 15). In fact, one such GaAs transistor was held at 300°C for over 100 hours with no apparent change in its transistor I-V characteristics.

The results described above indicate that vapor-grown three-layered structures can be used to fabricate GaAs n-p-n transistors with current gains at least as high as 10. Moreover, the transistors so prepared do not show any serious degradation in their characteristics to temperatures as high as 300°C. It is thus expected that further optimization of material and fabrication parameters will result in GaAs transistors with higher room-temperature current gains, and that these gains, in general, will remain constant to temperatures at least as high as 300°C.

B. P-N-P GaAs_{1-x}P_x Transistors

1. Fabrication Techniques. -- An electrolytic etching technique was described in RCA Descriptive Specification PP68-080 and in Quarterly Technical Reports No. 1 and 2. This technique, which utilizes a sprayed aqueous solution of NaOH, selectively removes large-area p-type layers of GaAs and GaAs_{1-x}P_x in such a way as to leave the underlying n-layer surface mirror-smooth. During the course of this contract, the electrolytic etching technique has undergone evaluation and development for the purpose of etching through selected portions of the p-type emitter, and thereby exposing regions of the base for subsequent contacting. In this way several p-n-p GaAs_{0.55}P_{0.45} transistors have been prepared for the first time entirely by the vapor-phase growth. However, these transistors were found to have very low current gains, slightly less than unity, despite the fact that the fabrication procedures appeared to have been successful. The fabrication procedure used for these transistors is described briefly below.

An array of Ag-Mn dots was first evaporated onto the emitter and sintered in H₂ at 550°C. These dots served not only as ohmic contacts to the emitter, but also as masks to protect portions of the emitter from subsequent electrolytic etching. The emitter surface of the wafer was then immersed in NaOH and sprayed during the electrolytic etching to form an array of emitter mesas separated by exposed regions of the base. The base was then contacted by evaporation of Ag-Te dots between the mesas, and the collector by evaporation of a Au-Zn film onto the substrate of the wafer.

After the contacts were sintered, the wafer was diced into individual transistors which were mounted on T0-5 headers and bonded ultrasonically.

2. Transistor Characteristics. -- Although several GaAs_{0.55}P_{0.45} p-n-p structures with base widths ranging from 1 to 5 μ were vapor grown and fabricated in the manner previously described, transistor behavior was observed for only two such wafers, those with 1- and 3- μ base widths. The current gains for these transistors were very low, about 0.5 and 0.2, respectively. Since, for both transistors, the base-emitter and base-collector junctions displayed reasonably good I-V characteristics, the low gains are attributed primarily to short hole diffusion lengths for these transistors. Hole diffusion lengths in p⁺-n GaAs_{0.55}P_{0.45} junctions were independently measured to be on the order of 2 μ , consistent with the low transistor gains observed here. Lifetime measurements and their relationship to GaAs_{1-x}P_x transistors are discussed in depth in Section II.C. below.

C. Electrical Behavior of Vapor-Grown P-N Junctions

In order to provide an accurate frame of reference for evaluating transistor performance, and to guide us in the optimization of material parameters for successful transistor operation, we have carried out an extensive evaluation of vapor-grown GaAs and GaAs_{1-x}P_x p-n junctions at temperatures between 25°C and 300°C. This evaluation includes measurements of I-V and C-V characteristics, and minority-carrier lifetimes and diffusion lengths for a series of diodes with a variety of GaAs_{1-x}P_x alloy compositions between x=0 and x=0.8.

To evaluate the base-emitter junction of the p-n-p GaAs_{1-x}P_x structure, p⁺-n diodes were fabricated with x=0.15, 0.30, 0.45, 0.60, and 0.80. Similarly, for the n-p-n structure, n⁺-p diodes were prepared with x=0 and x=0.15. Measurements carried out on these diodes are summarized below.

1. Lifetime and Diffusion Length. -- Measurements of the minority-carrier lifetime and diffusion length are essential for determining the maximum base width to be used for a practical transistor. Obviously, for high gain, the diffusion length must be much greater than the transistor base width.

In order to measure the very short (nsec) lifetimes in diodes of GaAs and GaAs_{1-x}P_x alloys, we have employed a microwave pulse variation of the classical charge-storage measurement used to measure lifetimes in the microsecond range[4]. With our present circuit, shown schematically in Figure 12, lifetimes as short as approximately 0.5 nsec (5×10^{-10} sec) can be resolved. In this measurement, the diode is mounted in a special coaxial holder and is initially dc forward-biased. A sharp (0.2-nsec rise time) reversing pulse is then applied, which is reflected by the diode and monitored by a sampling oscilloscope. The

response of the junction to the reversing pulse occurs in a finite time, defined as the "storage time," during which most of the previously injected charge is removed by the reversing field. The storage time, which is related to the minority-carrier lifetime, is observed directly on the oscilloscope as the time required for the junction to begin changing its impedance from the initial short-circuited (forward-biased) condition to the final open-circuited (reverse-biased) condition. Measurements of the minority-carrier lifetimes for the p-n junctions described above are illustrated in Figure 13 as a function of the $\text{GaAs}_{1-x}\text{P}_x$ alloy composition, x .

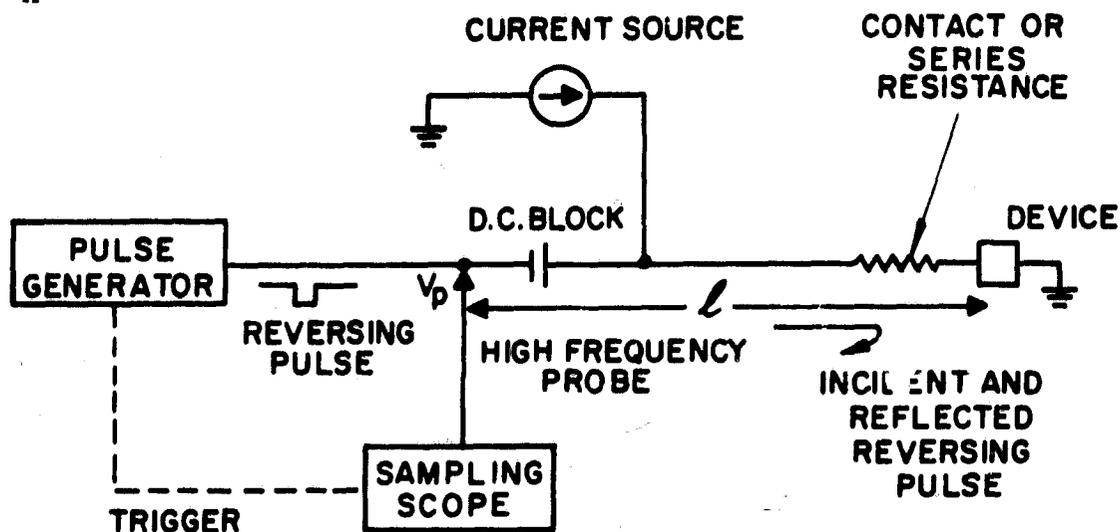


Figure 12 - Apparatus for lifetime measurements in $\text{GaAs}_{1-x}\text{P}_x$ p-n junctions.

Hole lifetimes for p^+-n junctions are on the order of 10 to 20 nsec for $\text{GaAs}_{1-x}\text{P}_x$ with $x < 0.4$, but increase to values of about 40 nsec for larger values of x . This trend, corroborated during the last quarter of our research by measurements at $x = 0.6$ and $x = 0.8$, shows that the minority-carrier lifetime for indirect-bandgap $\text{GaAs}_{1-x}\text{P}_x$ is longer than for direct-bandgap $\text{GaAs}_{1-x}\text{P}_x$. This result suggests that the lifetimes in our $\text{GaAs}_{1-x}\text{P}_x$ are limited by radiative recombination processes, which are known to be less efficient, i.e., have longer lifetimes, in indirect-bandgap semiconductors. Measured lifetimes as large as 4×10^{-8} sec for $\text{GaAs}_{.20}\text{P}_{.80}$ are somewhat higher than those usually observed or estimated for GaAs and GaP, and reflect the relatively high quality of the completely fabricated vapor-grown p-n junctions used here. Measurements of electron lifetimes in n^+-p junctions are also entered in Figure 13, and they are found to be slightly less than the hole lifetimes at the same alloy composition.

The diffusion length, L , of injected minority carriers in $\text{GaAs}_{1-x}\text{P}_x$ is obtained from the lifetime measurements from the relationship

$$L = \sqrt{D\tau} \quad (1)$$

where D , the diffusion coefficient for the appropriate carrier, is obtained from the Einstein equation

$$D = \frac{kT}{q} (\mu) \quad , \quad (2)$$

and from estimates of the electron or hole mobility.

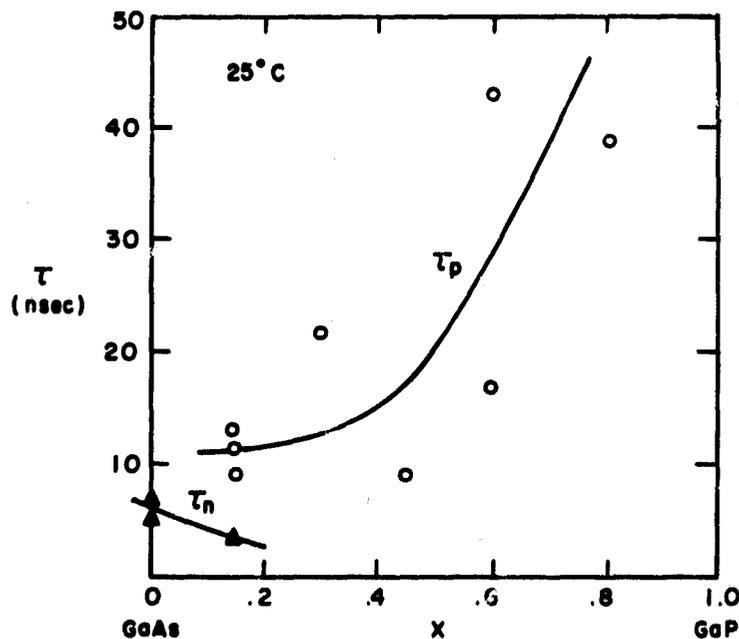


Figure 13 - Minority-carrier lifetimes vs. $\text{GaAs}_{1-x}\text{P}_x$ p-n junctions.

Calculations of the electron and hole diffusion lengths in $\text{GaAs}_{1-x}\text{P}_x$, based on Equation (2), are presented in Figure 14 as a function of alloy composition. Diffusion lengths for electrons are about 6 to 8 μ , and 3 to 4 times larger than for holes because of the large electron mobility for GaAs and for As-rich alloys of $\text{GaAs}_{1-x}\text{P}_x$ [5]. The increase in the hole diffusion length with increasing alloy composition is much less pronounced than is the corresponding increase for the hole lifetime (Figure 13), because of a reduction in the hole mobility with increasing composition.

The temperature dependence of minority-carrier lifetimes in $\text{GaAs}_{1-x}\text{P}_x$ junctions is shown in Figure 15. For the direct-bandgap samples with $x = 0$, $x = 0.15$, and $x = 0.30$, the temperature dependence is relatively weak. However, for the indirect-bandgap samples with $x = 0.6$ and $x = 0.8$, the temperature dependence becomes significantly stronger, with a drop in lifetimes by a factor of 2 observed for a temperature increase from 25°C to 300°C. The reason for the strong temperature dependence in the indirect-bandgap alloys is not yet understood and is under further investigation.

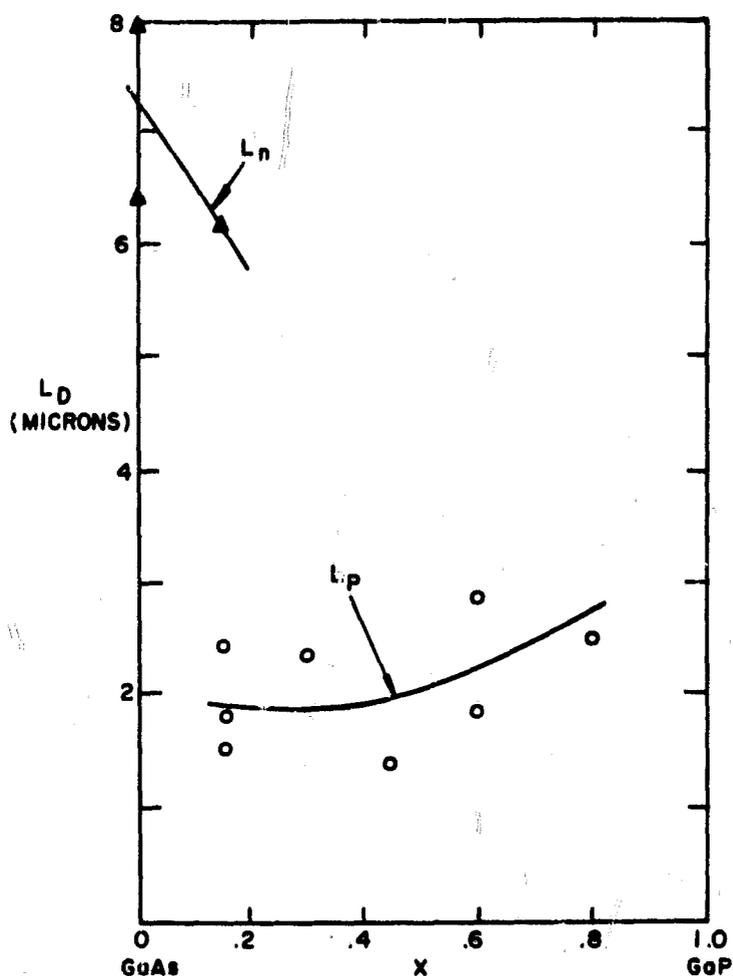


Figure 14 - Minority-carrier diffusion lengths vs. $\text{GaAs}_{1-x}\text{P}_x$ alloy composition, x .

In order to determine the transistor current gains which might be expected for GaAs and $\text{GaAs}_{1-x}\text{P}_x$ transistors with lifetimes and diffusion lengths on the order of those presented on the previous pages, calculations of the emitter injection efficiency and the base transport factor have been made for appropriately doped n-p-n and p-n-p transistors. For any given value of the emitter injection efficiency, the current gain of a transistor is then simply a function of the base transport factor, which, in turn, is related to the ratio of the minority-carrier diffusion length to the base width. Based on such calculation, and on an assumption of unity collection efficiency at the base-collector junction, the curves of Figure 16 show the theoretical current gains of GaAs and $\text{GaAs}_{1-x}\text{P}_x$ transistors as a function of the diffusion length/base width ratio.

First, for a given ratio of diffusion length to base width, expected current gains are highest for n-p-n GaAs transistors because of the high emitter injection efficiencies possible with

the relatively high value of the electron mobility. For an n-p-n GaAs transistor with a $1\text{-}\mu$ base width, and a diffusion length of about $6\ \mu$, current gains on the order of 50 are possible. On the other hand, for p-n-p transistors of GaAs_{0.5}P_{0.5} with a $1\text{-}\mu$ base width and a $2\text{-}\mu$ hole diffusion length, gains no larger than 2 can be expected, consistent with the low gains actually obtained with such transistors. Figure 16 shows that highest gains in p-n-p transistors can theoretically be obtained with GaP or GaP-rich alloys of GaAs_{1-x}P_x. However, even with diffusion length/base width ratios as large as 4 (which might be possible for GaP based on an extrapolation of the hole diffusion lengths in Figure 14) current gains would not be expected to exceed 10. Furthermore, the strong temperature dependence found for the indirect-bandgap alloys of GaAs_{1-x}P_x would decrease the gain at higher temperatures more so than for the direct-bandgap alloys of GaAs_{1-x}P_x. For these reasons, most of our recent transistor research has been directed toward the As-rich alloys of GaAs_{1-x}P_x.

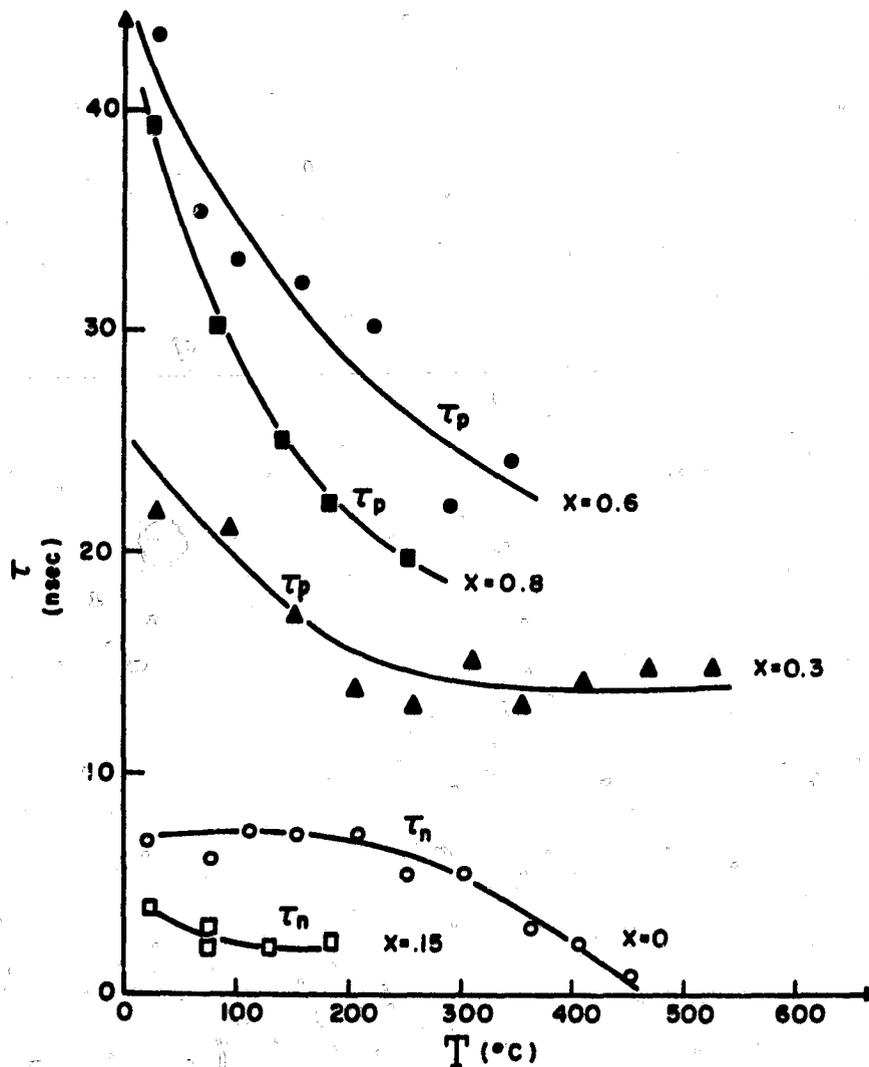


Figure 15 - Temperature dependence of minority-carrier lifetimes in GaAs_{1-x}P_x p-n junctions.

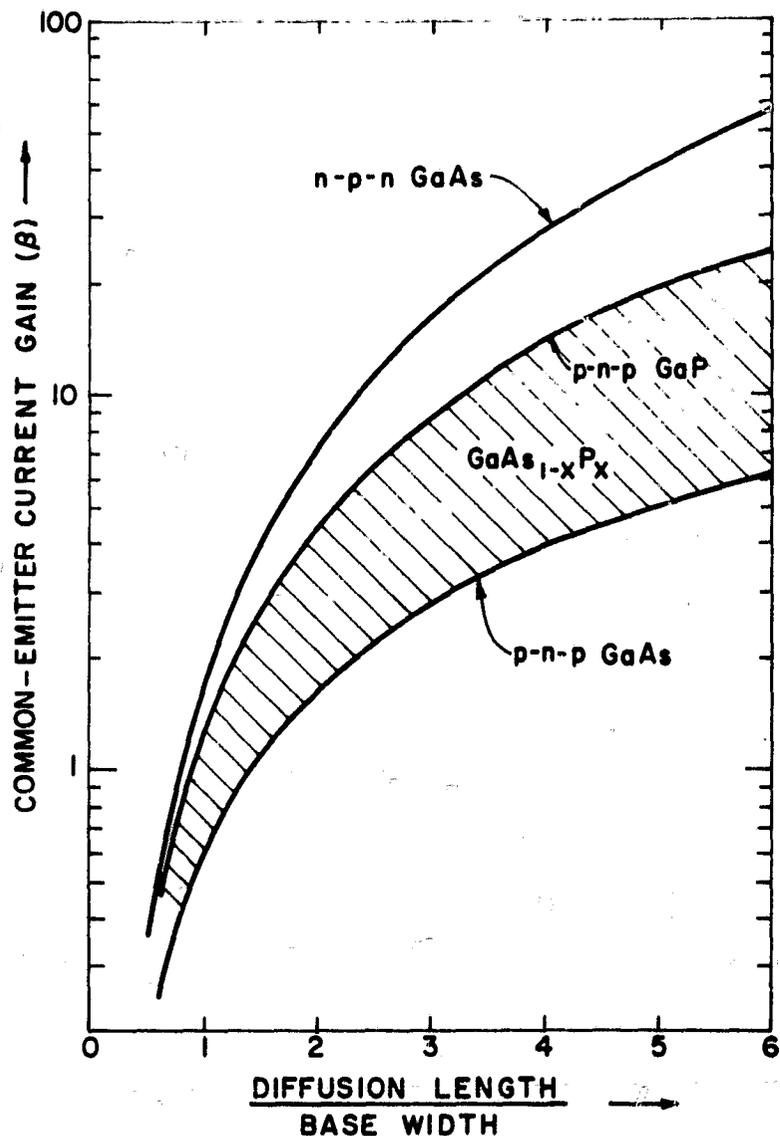


Figure 16 - Common-emitter current gain as a function of the ratio of diffusion length to base width for $\text{GaAs}_{1-x}\text{P}_x$ n-p-n and p-n-p transistors.

2. I-V and C-V Characteristics. -- In order to thoroughly characterize GaAs and $\text{GaAs}_{1-x}\text{P}_x$ vapor-grown junctions at high temperature, two p-n junctions were prepared, one each with appropriate impurity concentrations for the base-emitter junction of a transistor, n^+-p for GaAs, and p^+-n for $\text{GaAs}_{.55}\text{P}_{.45}$. Several 1-mm^2 diodes were cleaved from each junction layer and mounted on transistor headers by conventional bonding techniques. Measurements of I-V and C-V characteristics were then made on these diodes over the temperature range 20° to 300°C , the results of which are described below.

For moderate current densities ($J > 10^{-6} \text{ A/cm}^2$), the forward-bias I-V characteristics of both GaAs and $\text{GaAs}_{.55}\text{P}_{.45}$ junctions in this temperature range were closely represented by an expression of the form

$$I = I_0 \exp(qV/\beta kT)$$

with temperature-independent values of β between 1.4 and 1.5. At very low currents ($10^{-8} < J < 10^{-6}$ A/cm²) the values of β were temperature-dependent and were somewhat larger ($\beta \approx 2$), perhaps due to low-level injection and recombination processes such as tunneling, saturating nonradiative centers, or surface effects. However, the fact that β is temperature-independent at current levels used in practical transistor operation implies that the junction injection and recombination processes in the transistor will not change significantly at high temperatures. Reverse-bias currents are discussed separately in Section II.3 on page 23.

Measurements of capacitance (C) versus voltage (V) showed two important features. First, capacitance was described by the relation

$$C = C_0 (V + V_0)^{-1/m} \quad , \quad (3)$$

Where V_0 is the diffusion potential, with constant values of $m \approx 2.25$ throughout the temperature range 20 to 300°C. Thus, the junctions are intermediate between abrupt ($m = 2$) and graded ($m = 3$). Second, plots of A^2/C^2 versus V, where A is the junction area, for GaAs and GaAs.₅₅P.₄₅ diodes (Figure 17) exhibit

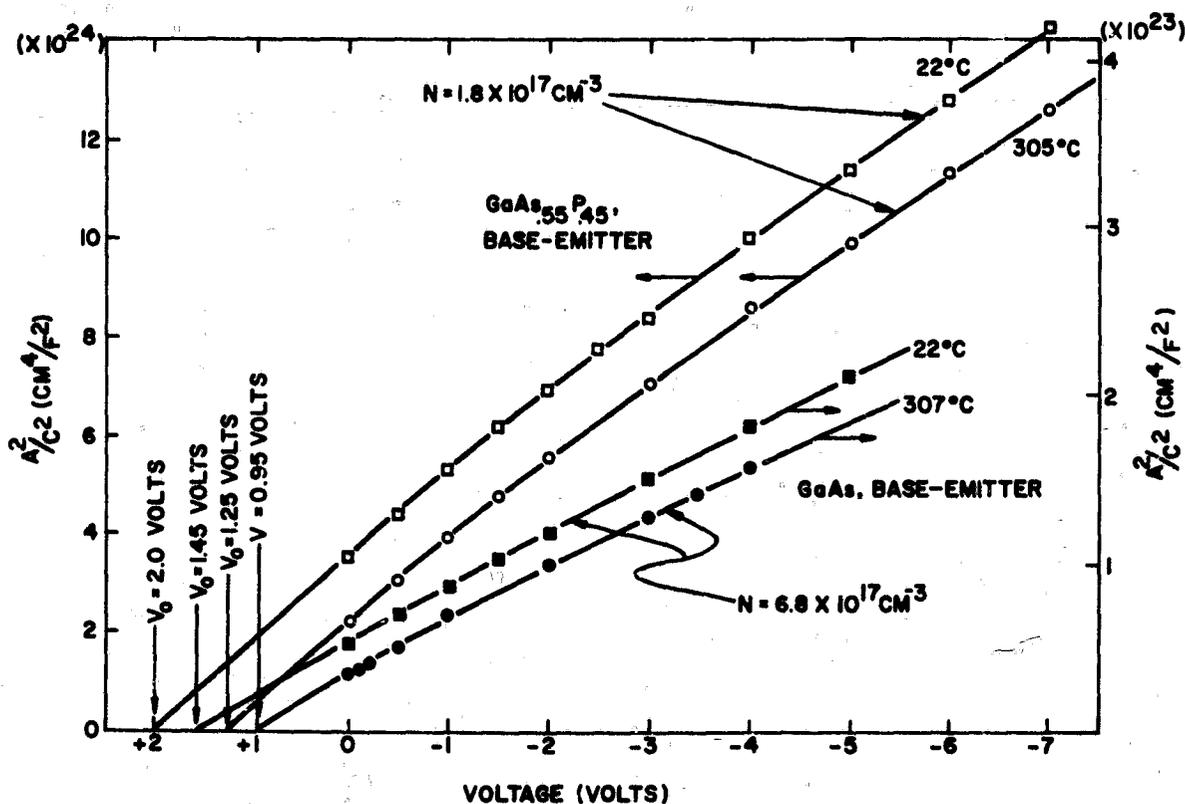


Figure 17 - C-V characteristics of GaAs and GaAs.₅₅P.₄₅ vapor-grown junctions at room temperature and 300°C.

the same slope at 20°C and 300°C. This indicates a temperature-independent carrier concentration, since the slopes of the curves are proportional to the carrier concentrations on the more lightly doped side of the p-n junction. The translation of the curves along the horizontal (voltage) axis is due to the decrease in the diffusion potential, V_0 , at high temperatures. The reduction in V_0 at 300°C by 0.75 V for GaAs_{0.55}P_{0.45} and 0.5 V for GaAs is due primarily to the reduction in the energy gap and the accompanying increase in the intrinsic carrier concentration.

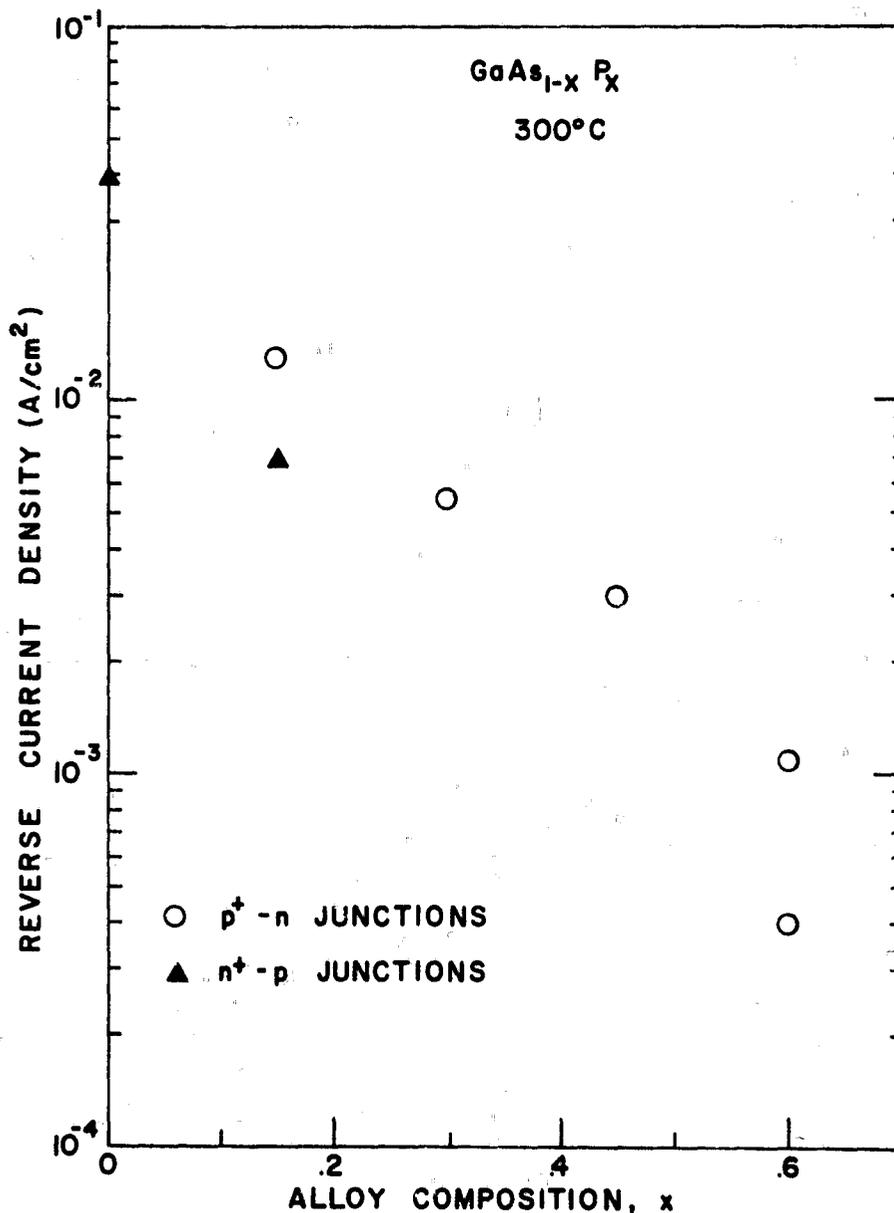


Figure 18 - Reverse currents in GaAs_{1-x}P_x p-n junctions at 300°C vs. alloy composition.

3. Reverse Currents. -- Reverse bias currents in the base-collector junction of a transistor vary strongly with temperature because of their direct dependence on the intrinsic carrier concentration, n_i , and because of the exponential dependence of n_i

on temperature[6]. During normal transistor operation, such currents exist even in the absence of injected minority carriers from the emitter. At high temperatures, the increase in reverse currents can be significant, and in fact, such currents were the primary source of difficulty in earlier diffused GaAs transistors. For this reason, the magnitude of the reverse currents in our vapor-grown junctions is of primary interest.

Reverse currents at 300°C for the series of vapor-grown $\text{GaAs}_{1-x}\text{P}_x$ p⁺-n and n⁺-p junctions described above are shown in Figure 18. Here, a large decrease in the reverse current is shown to occur with increasing phosphorus content in the $\text{GaAs}_{1-x}\text{P}_x$ alloy series. This decrease in reverse current in $\text{GaAs}_{1-x}\text{P}_x$ reflects the dependence of the intrinsic carrier concentration on the semiconductor energy gap. The reverse currents in Figure 18 are reasonably low in all cases and should be satisfactory for our transistor requirements. However, should leakage currents become a problem in GaAs, or should temperatures in excess of 300°C be required, n-p-n transistors of $\text{GaAs}_{1-x}\text{P}_x$ with small values of x could be used to obtain lower reverse currents while still preserving the high electron mobility and long electron diffusion length of GaAs.

III. CONCLUSIONS AND RECOMMENDATIONS

GaAs n-p-n transistors with bases widths of 1 to 2 μ have been prepared by sputter-etching grooves in selected areas of the emitter, and by the formation of a p-type channel from the emitter to the base. Transistors with room-temperature current gains of 10 and 5 have been achieved by these respective fabrication techniques. Furthermore, several GaAs transistors of each type have been investigated to temperatures as high as 300°C without significant changes in their gain. Particularly significant is the fact that leakage currents in GaAs transistors have not been excessive, even at 300°C. Moreover, one such transistor showed no degradation after 100 hours heat treatment at 300°C. To our knowledge, the GaAs transistors prepared under this research contract are the first transistors ever prepared entirely by vapor-phase growth.

P-n-p transistors have also been prepared in $\text{GaAs}_{.55}\text{P}_{.45}$; however, gains here have been less than unity, consistent with the small hole diffusion lengths measured in $\text{GaAs}_{1-x}\text{P}_x$.

The high-temperature capabilities of vapor-grown GaAs and $\text{GaAs}_{1-x}\text{P}_x$ p-n junctions have been extensively evaluated. I-V and C-V measurements indicate that their impurity concentrations and injection mechanisms are basically temperature-independent between 25° and 300°C. Reverse currents at nominal voltages (5 to 10 V) are on the order of 1 to 3 $\times 10^{-2}$ A/cm² for GaAs junctions at 300°C, and decrease significantly in $\text{GaAs}_{1-x}\text{P}_x$

junctions to values as low as 5 to 10^{-4} A/cm² for $x \approx 0.6$. Lifetime measurements for junctions of GaAs and GaAs_{1-x}P_x with $x \leq 0.15$ show that the minority electron lifetime at 300°C decreases only slightly from its room-temperature value.

Our research to date has demonstrated that GaAs transistors can be prepared by vapor-phase growth, and that such transistors can indeed be operated at ambient temperatures of 300°C. Future efforts should concentrate on optimizing the vapor-growth, regrowth, sputter etching, and other fabrication parameters to provide further improvements in the transistor current gain. Gains approaching 50 appear to be possible using n-p-n GaAs or GaAs_{1-x}P_x ($x < 0.15$) transistors. In addition, the high-temperature performance of such transistors is expected to approximate closely their room-temperature characteristics.

IV. REFERENCES

1. J. J. Tietjen and J. A. Amick, J. Electrochem. Soc. 113, 724 (1966).
2. C. J. Nuese and J. J. Gannon, J. Electrochem. Soc 115, 327 (1968).
3. H. Becke, D. Flatley, and D. Stolnitz, Solid-State Electronics 8, 255 (1965).
4. E. M. Pell, Phys. Rev. 90, 278 (1953).
5. J. J. Tietjen and L. R. Weisberg, Appl. Phys. Letters 7, 261 (1965).
6. R. A. Smith, Semiconductors, (Cambridge University Press, New York, 1959) page 78.
7. R. T. C. Tsui, SCP and Solid-State Technology, Dec. 1967, page 33.

V. NEW TECHNOLOGY APPENDIX

A Sputter-Etch Technique For Fabricating Transistors

Research under this contract has resulted in one item of new technology: A Sputter-Etch Technique for Fabricating Transistors. This invention, described on pages 4-7 of this report, is summarized below.

The first vapor-grown GaAs transistors with positive gain have been prepared. Common-emitter current gains, β , of up to 10

have thus far been achieved with a base width of 1.5μ . Values of β remain constant from room temperature up to 300°C .

The use of sputter etching to contact the base of these n-p-n structures was a key factor in achieving this result. Sputter-etching is commonly used[7] to etch very thin layers (1000 \AA) at rates of 100 \AA min^{-1} . But in this work we have sputter-etched at rates of $1000 \text{ \AA min}^{-1}$ to depths of 3 to 5μ , with control of the final depth to 0.1μ , and without evident damage to the p-n junctions. The use of a simple molybdenum mask has provided a resolution of about 1 mil, which is more than adequate for this purpose.

APPENDIX

DOPING OF VAPOR-GROWN GaAs

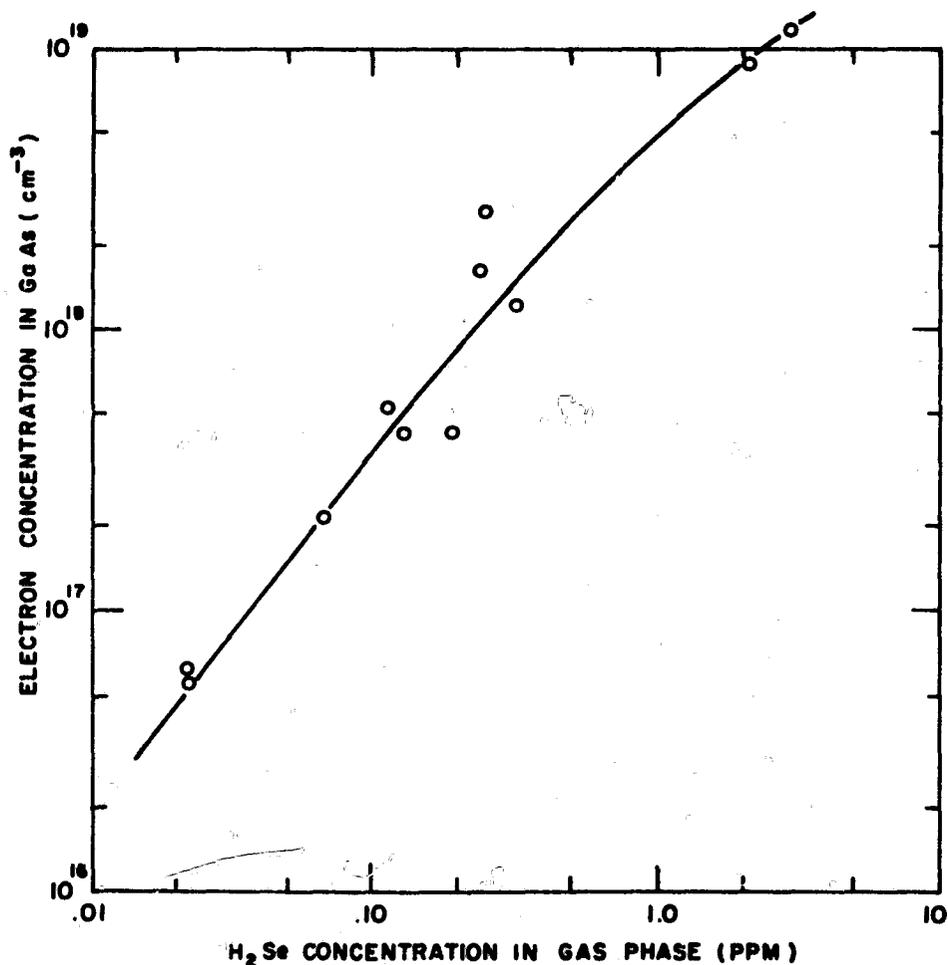


Figure A-1 - Electron concentration in GaAs vs. H_2Se concentration in gas phase.

A. Introduction. -- The basic vapor-phase growth system used for the preparation of the present GaAs and $\text{GaAs}_{1-x}\text{P}_x$

transistor structures has been described in the literature[1]. In this appendix, we include for completeness, the manner in which donor and acceptor concentrations are controlled during vapor-phase growth.

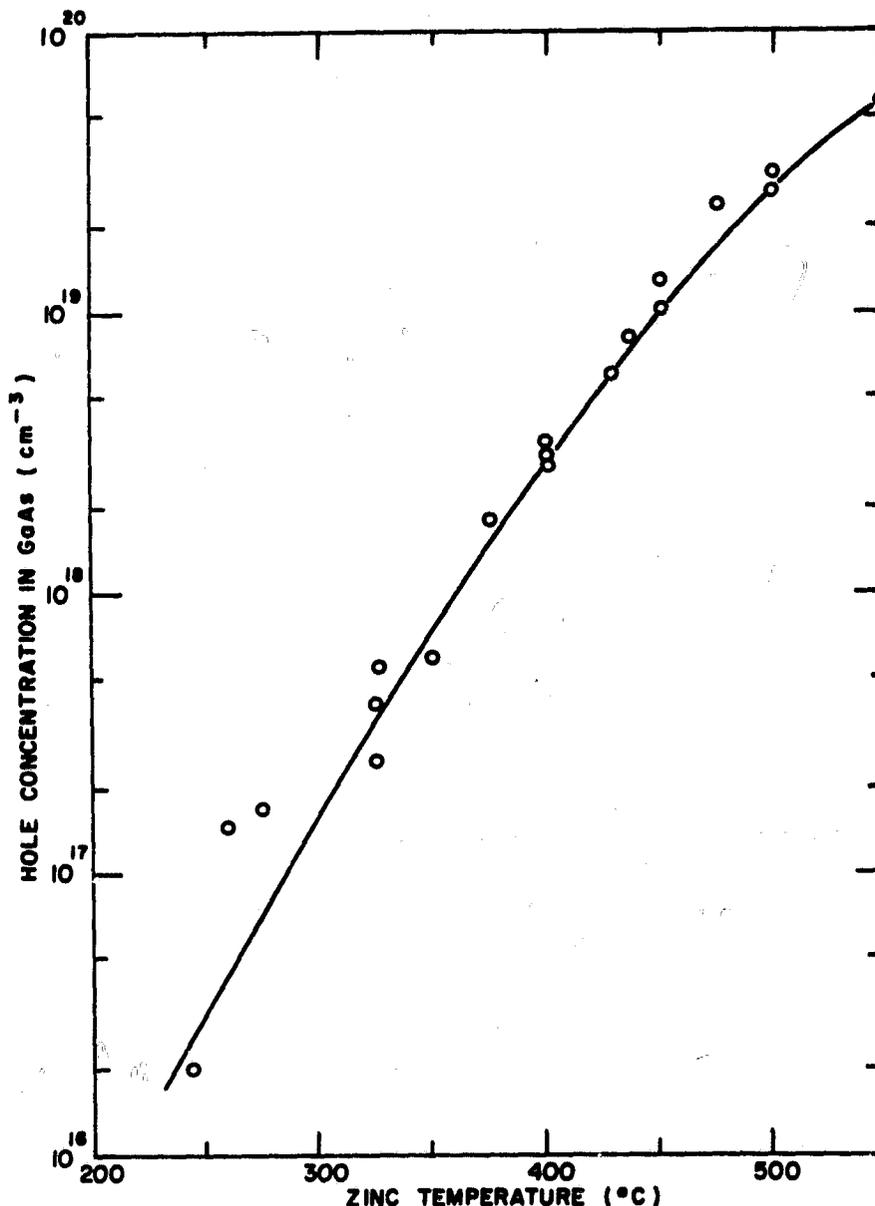


Figure A-2 - Hole concentration in GaAs vs. temperature of Zn source.

B. Donor Concentrations. -- N-type doping in GaAs and GaAs_{1-x}P_x epitaxial layers is provided by cracking H₂Se. The total concentration of H₂Se in the vapor stream is simply controlled by diluting the source of H₂Se with varied amounts of H₂, which can be accurately determined by precision flow meters and valves. The concentration of H₂Se can be readily regulated between 0.02 and 3 parts per million. These concentrations of

H₂Se have been found empirically to provide donor concentrations in GaAs between $5 \times 10^{16} \text{ cm}^{-3}$ and $1 \times 10^{19} \text{ cm}^{-3}$, as shown in Figure A-1. The GaAs donor concentrations here were determined by Hall measurements.

Very lightly doped samples, having donor concentrations on the order of 10^{15} to 10^{16} cm^{-3} , are obtained *without* the use of an intentional dopant. They probably result from small amounts of silicon introduced from the quartz tubing.

C. Acceptor Concentrations. -- Acceptor doping is accomplished in our vapor-growth system by heating high-purity elemental zinc in a stream of H₂. The relative concentration of Zn carried into the epitaxial growth zone by the H₂ is determined by regulating the temperature (and hence, the vapor pressure) of the Zn between 250°C and 550°C. Within this temperature range, GaAs acceptor concentrations between 2×10^{16} and $5 \times 10^{19} \text{ cm}^{-3}$ can be obtained, as shown in Figure A-2. Here, the acceptor concentrations in GaAs were determined primarily from 4-point probe measurements of resistivity, and the known relation between resistivity and acceptor concentrations in p-type GaAs[2]. These results were corroborated by means of Hall effect measurements.

REFERENCES

1. J. J. Tietjen and J. A. Amick, J. Electrochem. Soc. 113, 724 (1966).
2. S. M. Sze and J. C. Irvin, Solid-State Electronics 11, 599 (1968).