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FINAL REPORT

16-CHANNEL MULTIPLEXER

September 1968

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FACILITY FORM 602



Prepared Under Contract NAS8-20890

by

PHILCO-FORD CORPORATION
Microelectronics Division
Blue Bell, Pennsylvania 19422

George C. Marshall Space Flight Center

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

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INTRODUCTION

The subject contract required the design, development and manufacture of twenty 16-channel multiplexers. In addition to the delivery of the multiplexers, the contract specified the provision of eight man-weeks of training for MSFC personnel and four man-weeks of support in the semiconductor laboratory at MSFC.

This is the final report on this contract. It includes a report of the progress for the period July-August 1968.

FACTUAL DATA

Device Production and Delivery

Several production runs were processed through the entire production cycle. Twenty of the devices from these production runs were shipped against this contract on August 23, 1968. Subsequently, the product was transferred to the Philco-Ford Microelectronics Division's Eastern Operations production facilities in Lansdale, Pennsylvania. This transfer included all production test specifications, test programs, diode boards, probe cards, and other pertinent information.

Training and Support Services

During the month of August 1968, several personnel of the Philco-Ford Microelectronics Division were sent to Huntsville,

Alabama, to provide the technical and process training and support required in the contract. These personnel were:

R. Hippert
A. Jaddam
J. Karp
L. Paxton

In the period August 23 to 30, 1968, L. Paxton assisted in the processing and testing of devices by NASA personnel. The discrete devices that were fabricated produced the following typical parameters:

V_{GST} . . . . . -2.5 volts

BV_{DSS} . . . . . -45 volts

A-C Transconductance . . . . . 1000 to 1200 μmhos

These devices were briefly life tested and demonstrated satisfactory results. Certain process revisions are suggested: they are given in a letter included as Appendix A to this report.

Pertinent Device Technical Data

Appendix B to this report includes technical data pertinent to the devices involved in the subject contract. These technical data are:

Tentative Data Sheet, M-31, on the 16-Channel MOS Multiplexer, pL4S16C;

Tentative Data Sheet, M-20, on the 16-Channel MOS Multiplexer, pL4S16;

Application Note No. 406, on the pL4S16 MOS 16-Channel Multiplexer.

CONCLUSION

The completion of the technical training and support services, the delivery of the twenty production devices, and the delivery of this final report complete the contractual commitments. Any technical questions related to this contract should be referred to Mr. John A. Ekiss, Manager Integrated Circuit Operations, Philco-Ford Corporation, Microelectronics Division, 1400 Union Meeting Road, Blue Bell, Pennsylvania 19422.

APPENDIX A

L. PAXTON LETTER TO D. ANDERSON GIVING SUGGESTED PROCESS REVISIONS

To: D. Anderson Date: August 30, 1968

From: L. Paxton (Philco-Ford Microelectronics)

Subject: Suggestions for Improving Existing Semiconductor Processing Equipment and Elimination of Possible Areas of Contamination

---

1. Order kit from Micro Tech for modifying alignment jig for improved resolution and wafer contact. (Approximate cost $600.00) Include new mask loading and holding arm; semisphere chuck for holding wafers; clippard valve for use of H_2 during exposure; and pneumatic cylinder to apply pressure to mask during exposure.

2. Order new electron beam gun system (Temescal type) for metallization vacuum system.

3. Eliminate positive resist development from area used for processing MOS devices.

4. Eliminate all cleaning and metal etchning from hoods and sinks used for processing MOS wafers.

5. Adjust the flat zone (center zone) of furnace to obtain the maximum length obtainable. It should be possible to get a flat zone of $\pm 1/2°C$ over a length 20 inches in the large furnaces by adjusting left and right zones.

6. Profile furnaces at least one hour before using.

7. Run capacitance vs. voltage checks on initial oxidation and diffusion furnaces periodically to check for contamination.

8. Steam the 1150°C boron diffusion furnace for 30 minutes and then purge with dry O_2 for at least 60 minutes prior to diffusing and reoxidation of wafers.

9. Clean tweezers daily in boiling trichloroethylene.

10. Clean furnace boats prior to use in 1:1 HF for 30 seconds; DI rinse for 10 minutes; and steam in mouth of 1200°C initial furnace for 15 minutes.

11. Fabricate or buy 3 stage cascade rinser for DI H_2O rinsing of wafers.

12. Obtain better method of drying wafers after DI H_2O rinsing.

13. Use vacuum chuck hold down for holding wafers during developing.

14. Buy an ultraviolet intensity meter for measuring light intensity of photoresist exposure lamp.

APPENDIX B

TECHNICAL DATA PERTINENT TO THE CONTRACT DEVICES

Tentative Data Sheet, M-31, on the 16-Channel MOS Multiplexer, pL4S16C

Tentative Data Sheet, M-20, on the 16-Channel MOS Multiplexer, pL4S16

Application Note No. 406, on the pL4S16 MOS 16-Channel Multiplexer

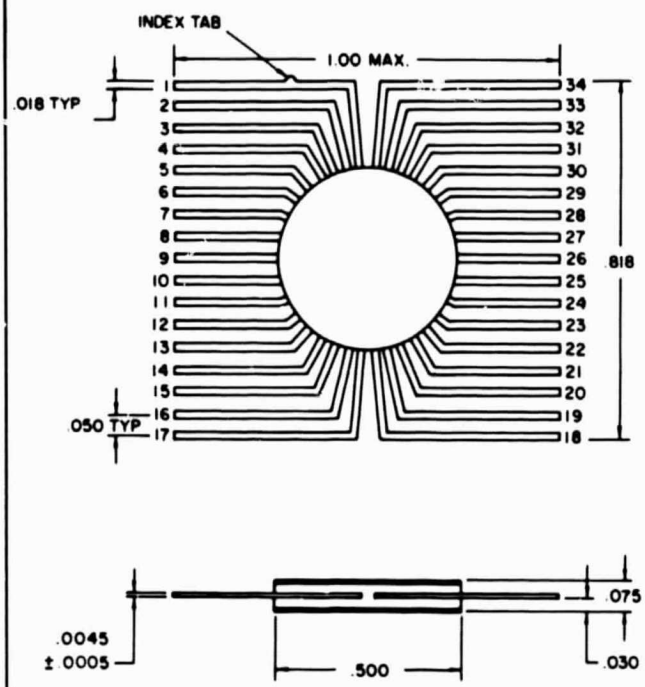
16-CHANNEL MOS MULIPLEXER pL4S16C

TENTATIVE DATA SHEET ■ M-31 **APRIL 1968**

GENERAL DESCRIPTION

The Philco-Ford pL4S16C 16-Channel Multiplexer is a monolithic MOS LSI device which may be used in many applications requiring sequential or random-access multiplexing. The applications include telemetry, satellite communications, sample data systems, etc. The chip contains 16 channel switches, a 4-bit address register/counter, random-access gating, decode matrix and a control flip-flop. The control flip-flop is used for additional address storage when large multiplexing systems (any multiple of sixteen) are formed by suitable interconnection of pL4S16 devices. The device may also be used as an 8-Channel Differential Multiplexer. For detailed device operation, see Application Note No. 406.

PACKAGING



34-Lead Flat Package

Pin No.	Function	Pin No.	Function
1	V_{REF}	18	CH 0
2	V_{DD}	19	CH 1
3	Output Shunt Control	20	CH 2
4	Sync Out	21	CH 3
5	Control F/F Set	22	CH 4
6	Control F/F $\overline{\text{Reset}}$ Out	23	CH 5
7	Control F/F Reset	24	CH 6
8	Control F/F Clock	25	CH 7
9	Matrix Control	26	CH 8
10	8/16 Control	27	CH 9
11	Clock	28	CH 10
12	2^3 Address In	29	CH 11
13	2^2 Address In	30	CH 12
14	2^1 Address In	31	CH 13
15	2^0 Address In	32	CH 14
16	Parallel Load	33	CH 15
17	Multiplex Out (0-7)	34	Multiplex Out (8-15)

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Microelectronics Division
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Phone (408) 245-2966

16-CHANNEL MOS MULTIPLEXER ■ pL4S16C ■ PHILCO

MAXIMUM RATINGS

Storage Temperature Range, Ambient	-65°C to +150°C
Operating Temperature Range	0°C to +70°C
V_{DD}	-33V to +0.3V (See Note 1)

ELECTRICAL CHARACTERISTICS

Standard Conditions (Unless Otherwise Specified):

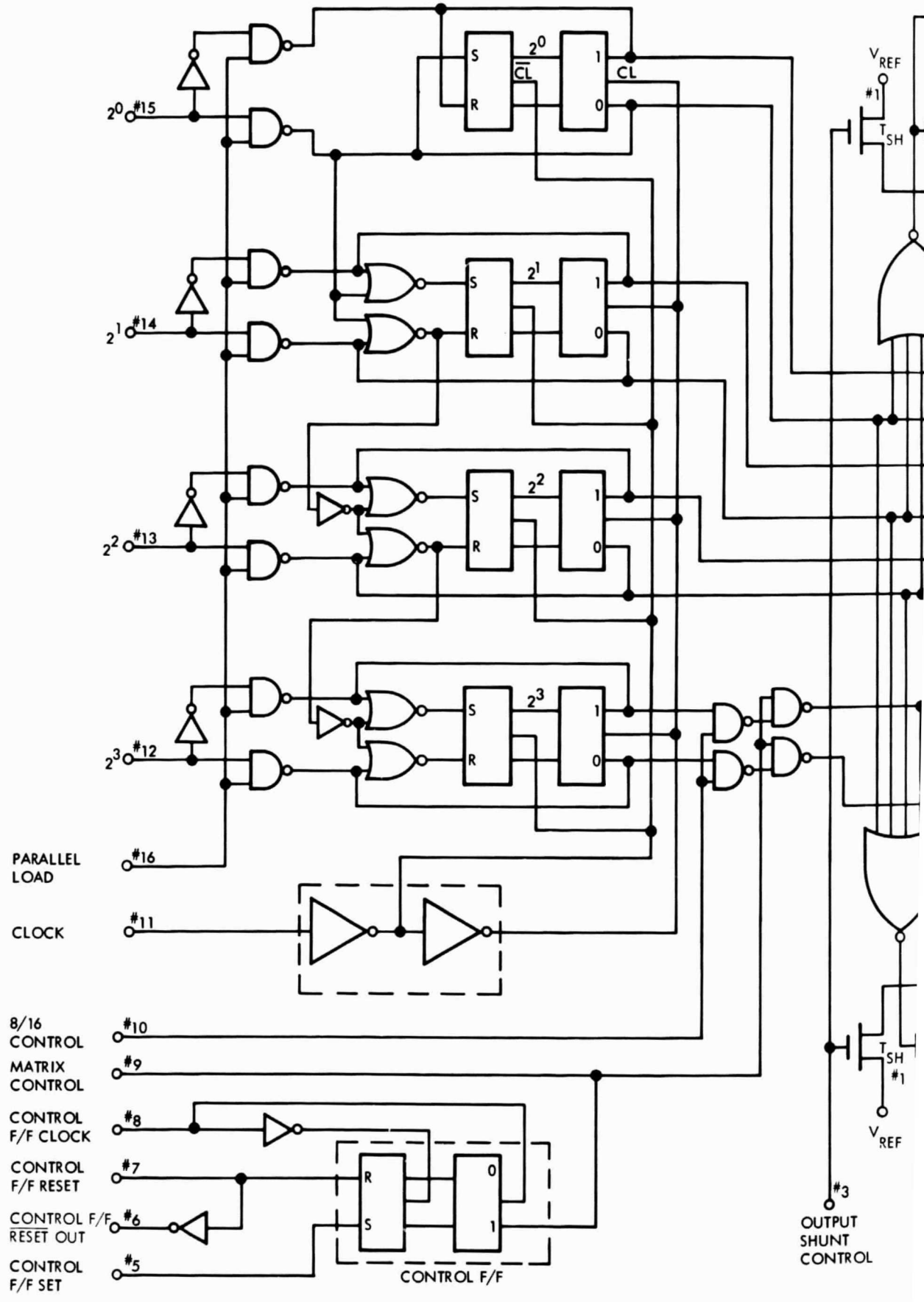
T_A = +25°C V_{DD} = -28 ±1V V_{ref} = GND Load = 500 kΩ, 20 pF to Ground

CHARACTERISTIC	MIN.	MAX.	UNITS	CONDITIONS
Signal Voltages, V_{IN}	0	-10	Volts	See Note 2
Clock Frequency	0	100	kHz	Sequential Mode
Clock and Parallel Load Pulse Width	2		μs	See Note 3
Switch Settling Time		5	μs	From -10V point on clock to 90% point on output; R_S = 1kΩ
All Logic/Control Inputs: "1"	-9		Volts	
"0"		-3	Volts	
Input Capacitance (Each Channel)		5	pF	V_{IN} = -5V
Channel Switch R_{ON}		1000	Ω	V_{IN} = -1V
Shunt Switch R_{ON}		2000	Ω	$V_{pin\ 3}$ = -9V, V_{OUT} = -10mV
Switch Input Leakage		10	nA	V_{IN} = -5V, T_A = +25°C
Output Leakage (16 Channels in Parallel)		20	nA	V_{IN} = -5V, T_A = +25°C
Channel Switch OFF Impedance, Z_{OFF}	3		MΩ	V_{IN} = -10V, f = 50 kHz
Power Dissipation		150	mW	V_{DD} = -28V

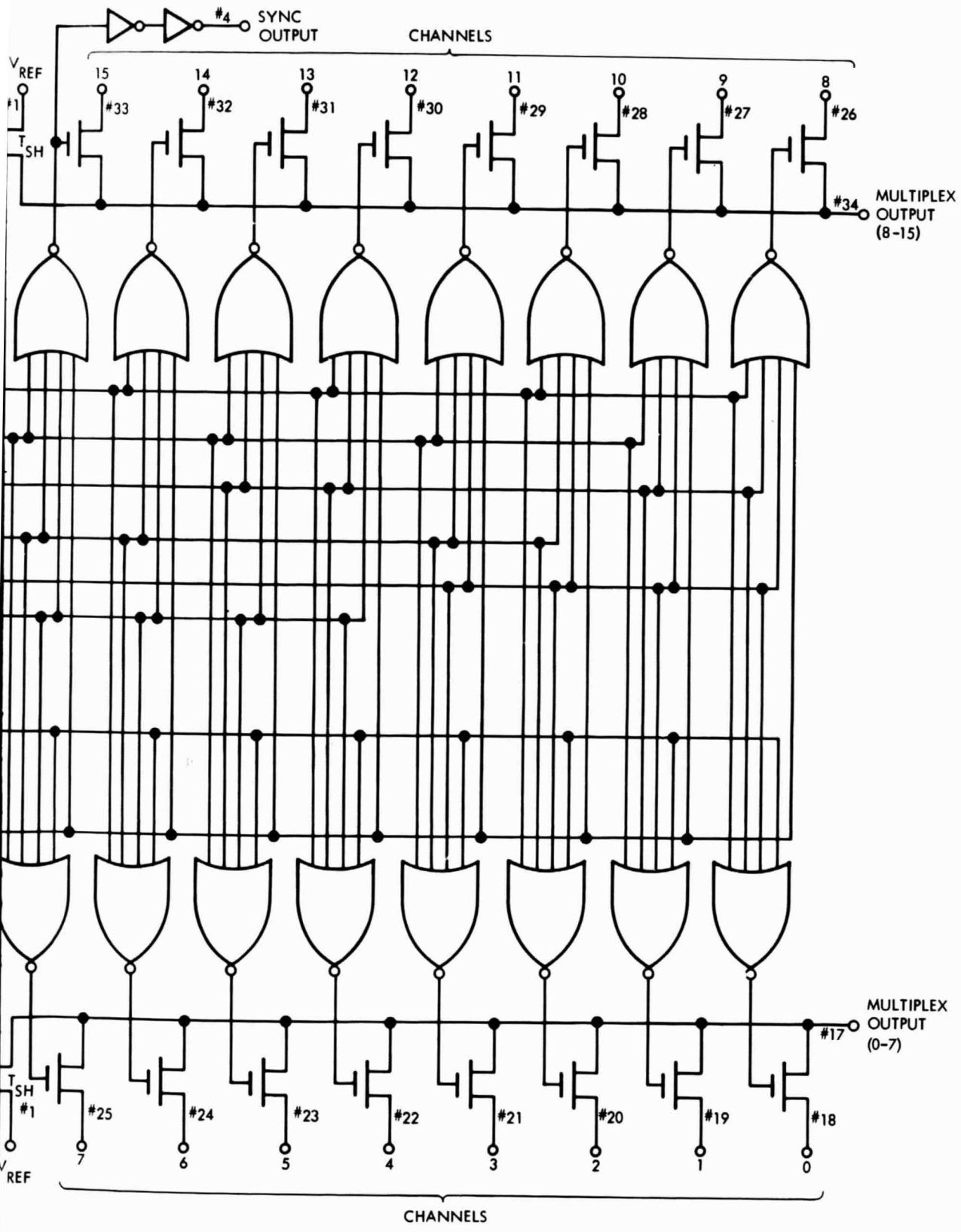
NOTES:

1. A voltage more positive than 0.3 V with respect to V_{ref} (pin 1) should not be applied to any pin. If positive input voltages are used, pin 1 should be held at the most positive input voltage and V_{DD} should be reduced to maintain 28 V + 1 V across the circuit (see Application Note No. 406).
2. Pin 1 (V_{ref}) may be biased to other voltages to change the signal voltage range. For example, if pin 1 is biased to +5V, the signal voltage range becomes ±5V. Pin 2 (V_{DD}) should then be held at -23V ±1V to maintain 28V ±1V across the circuit.
3. The address inputs, pins 12 through 15, should remain at a fixed logic level during the parallel load pulse.

LOGIC DIAGRAM

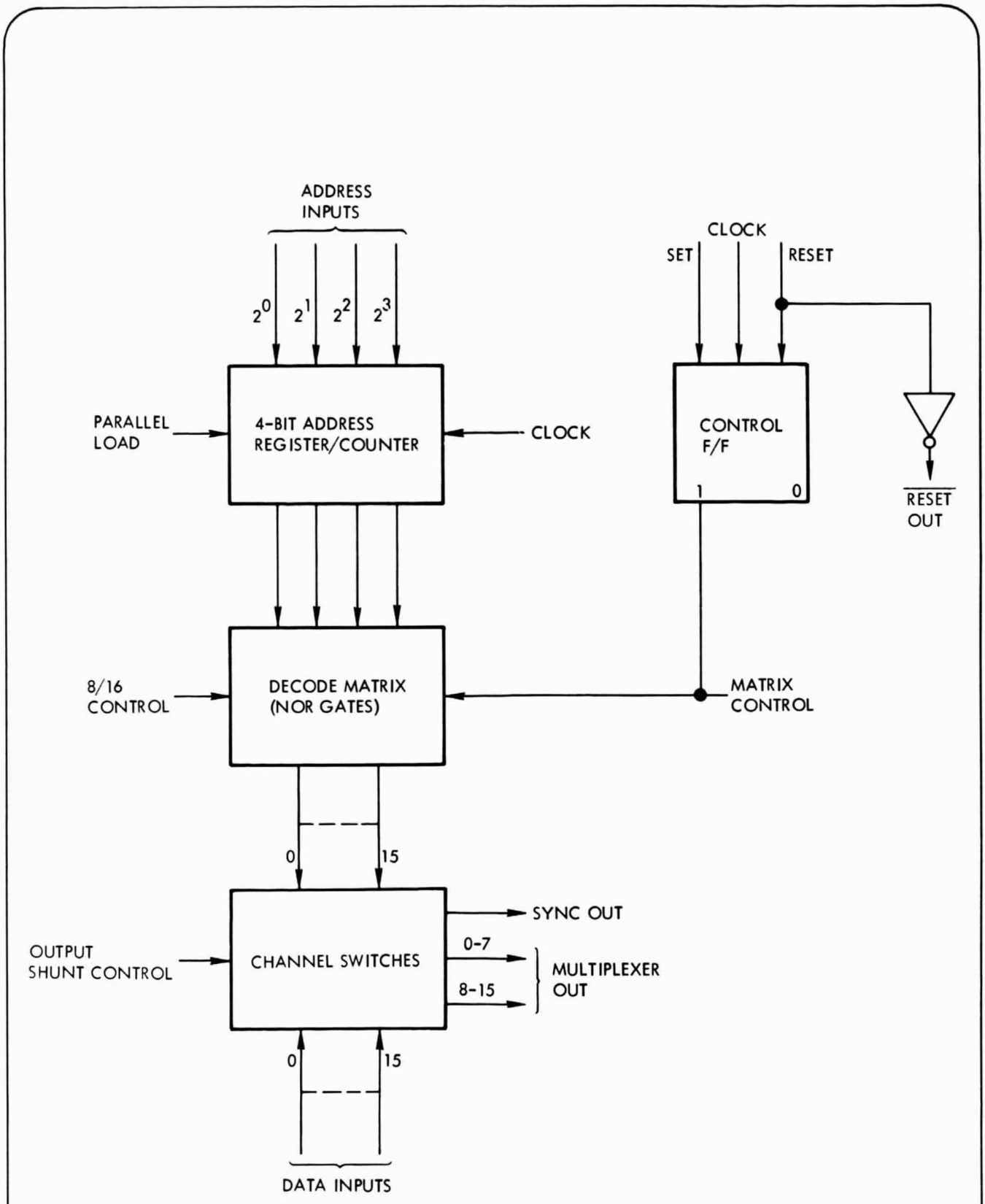


FOLDOUT FRAME

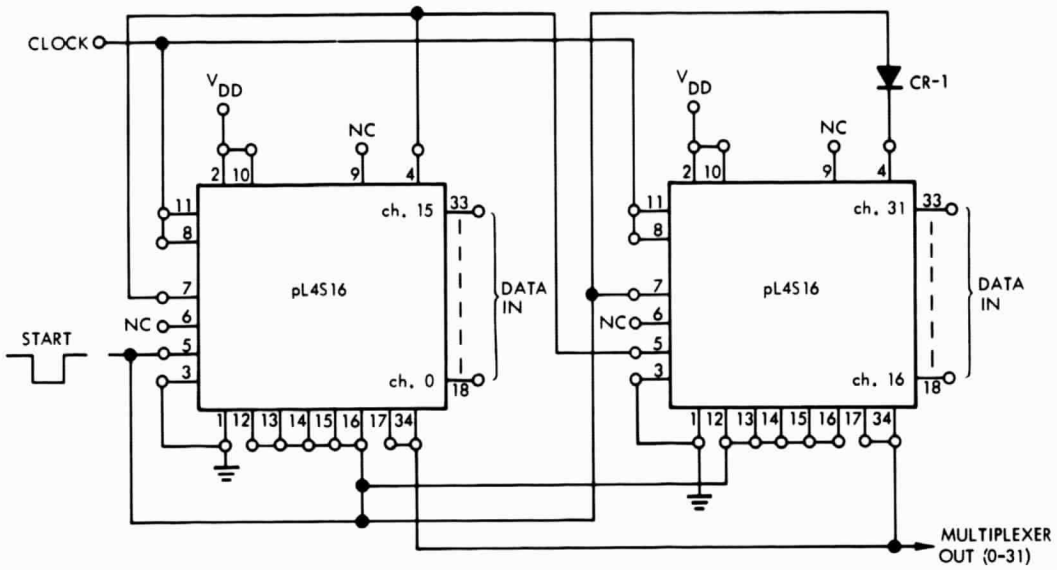


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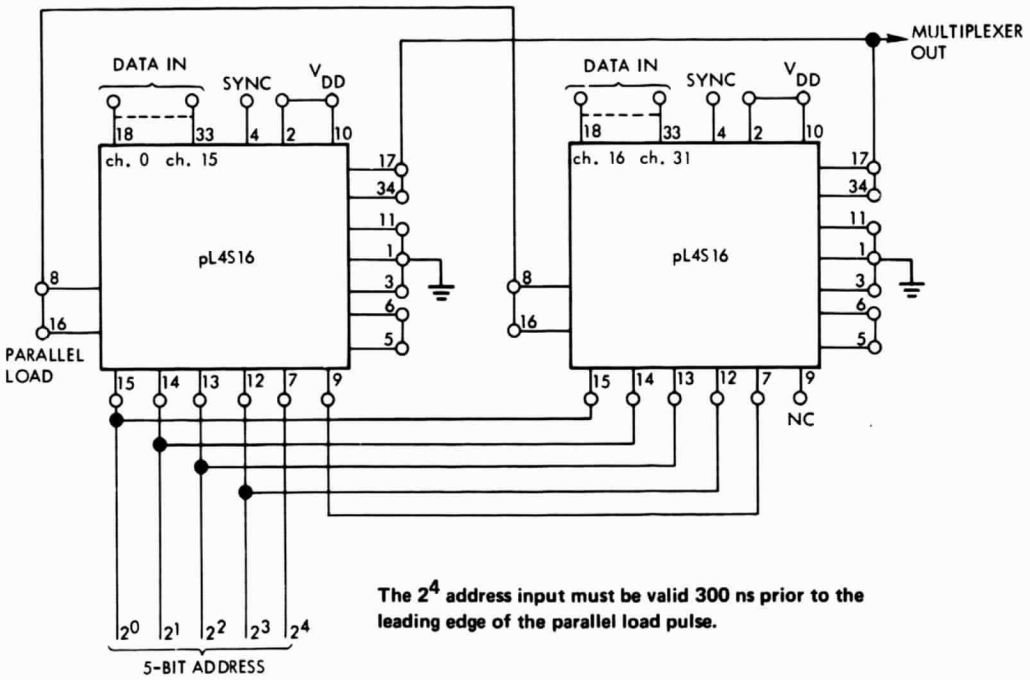
BLOCK DIAGRAM



TYPICAL INTERCONNECTIONS



SEQUENTIAL SAMPLING OF 32 CHANNELS



The 2^4 address input must be valid 300 ns prior to the leading edge of the parallel load pulse.

RANDOM ACCESS TO 32 CHANNELS

The information, diagrams or any other data included herein are believed to be accurate and reliable. However, the Philco-Ford Corporation, Microelectronics Division, assumes no responsibility or liability whatsoever for application, interpretation or use made of such information, diagrams or data, insofar as the use of said information, diagrams or data affects any patent, trademark or proprietary data rights.

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909 North Sepulveda
Suite 414
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TWX: 910-348-6287

Philco-Ford of Canada
900 Don Mills Rd.
Don Mills, Ontario
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(416) 444-2541

Northwest Industrial Park
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TWX: 910-338-0238

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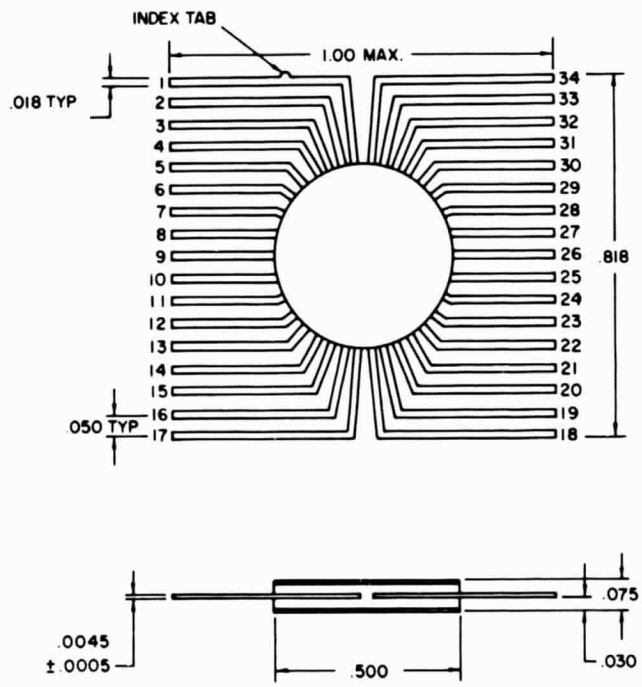
16-CHANNEL MOS MULTIPLEXER pL4S16

TENTATIVE DATA SHEET ■ M-20 **APRIL 1968**

GENERAL DESCRIPTION

The Philco-Ford pL4S16 16-Channel Multiplexer is a monolithic MOS LSI device which may be used in many applications requiring sequential or random-access multiplexing. The applications include telemetry, satellite communications, sample data systems, etc. The chip contains 16 channel switches, a 4-bit address register/counter, random-access gating, decode matrix and a control flip-flop. The control flip-flop is used for additional address storage when large multiplexing systems (any multiple of sixteen) are formed by suitable interconnection of pL4S16 devices. The device may also be used as an 8-Channel Differential Multiplexer. For detailed device operation, see Application Note No. 406.

PACKAGING



34-Lead Flat Package

Pin No.	Function	Pin No.	Function
1	V_{REF}	18	CH 0
2	V_{DD}	19	CH 1
3	Output Shunt Control	20	CH 2
4	Sync Out	21	CH 3
5	Control F/F Set	22	CH 4
6	Control F/F $\overline{\text{Reset}}$ Out	23	CH 5
7	Control F/F Reset	24	CH 6
8	Control F/F Clock	25	CH 7
9	Matrix Control	26	CH 8
10	8/16 Control	27	CH 9
11	Clock	28	CH 10
12	2^3 Address In	29	CH 11
13	2^2 Address In	30	CH 12
14	2^1 Address In	31	CH 13
15	2^0 Address In	32	CH 14
16	Parallel Load	33	CH 15
17	Multiplex Out (0-7)	34	Multiplex Out (8-15)

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MAXIMUM RATINGS

Storage Temperature Range, Ambient	-65°C to +150°C
Operating Temperature Range	-55°C to +125°C
V_{DD}	-33V to +0.3V (See Note 1)

ELECTRICAL CHARACTERISTICS

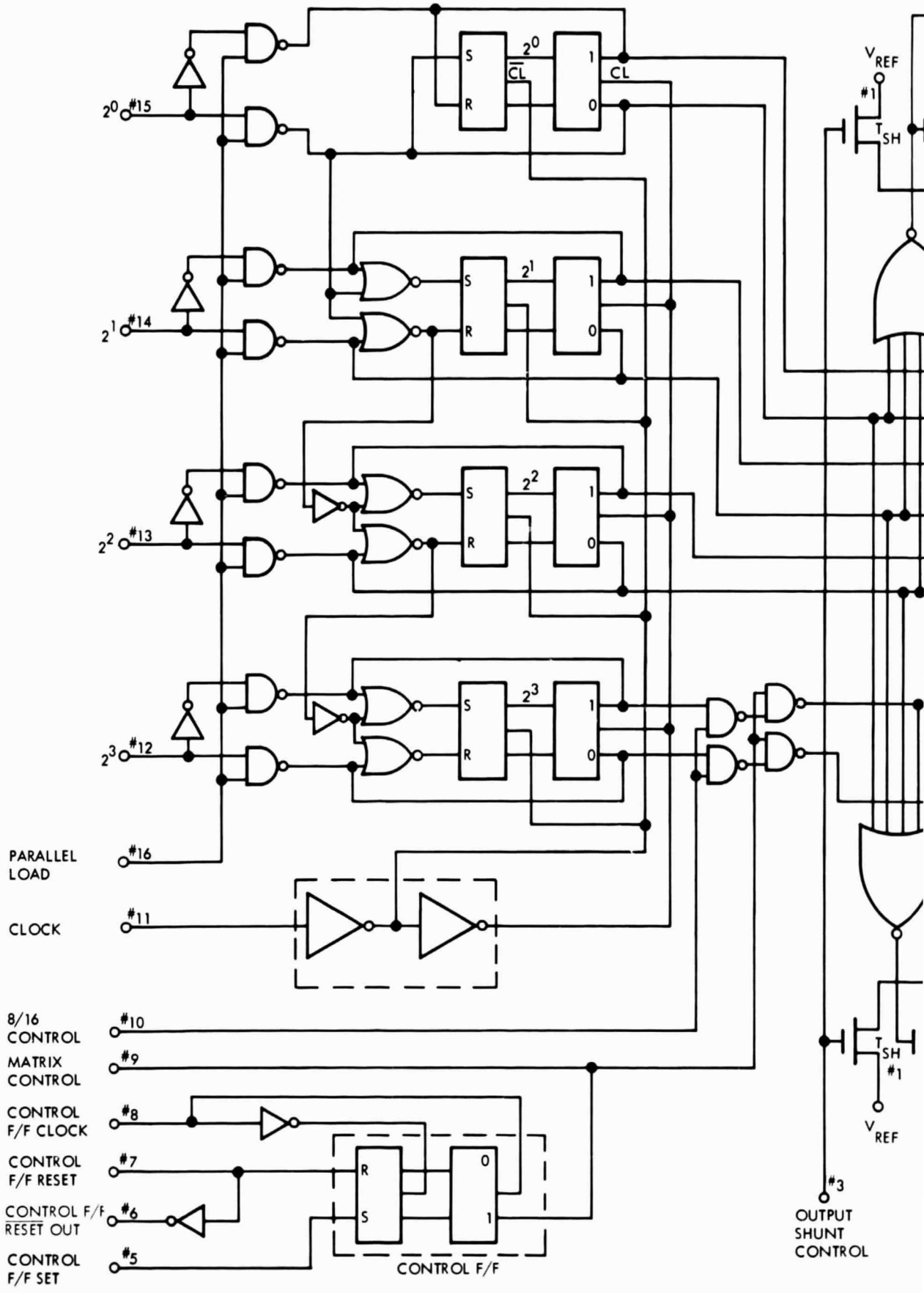
Standard Conditions (Unless Otherwise Specified):

T_A = +25°C V_{DD} = -28 ±1V V_{ref} = GND Load = 500 kΩ, 20 pF to Ground

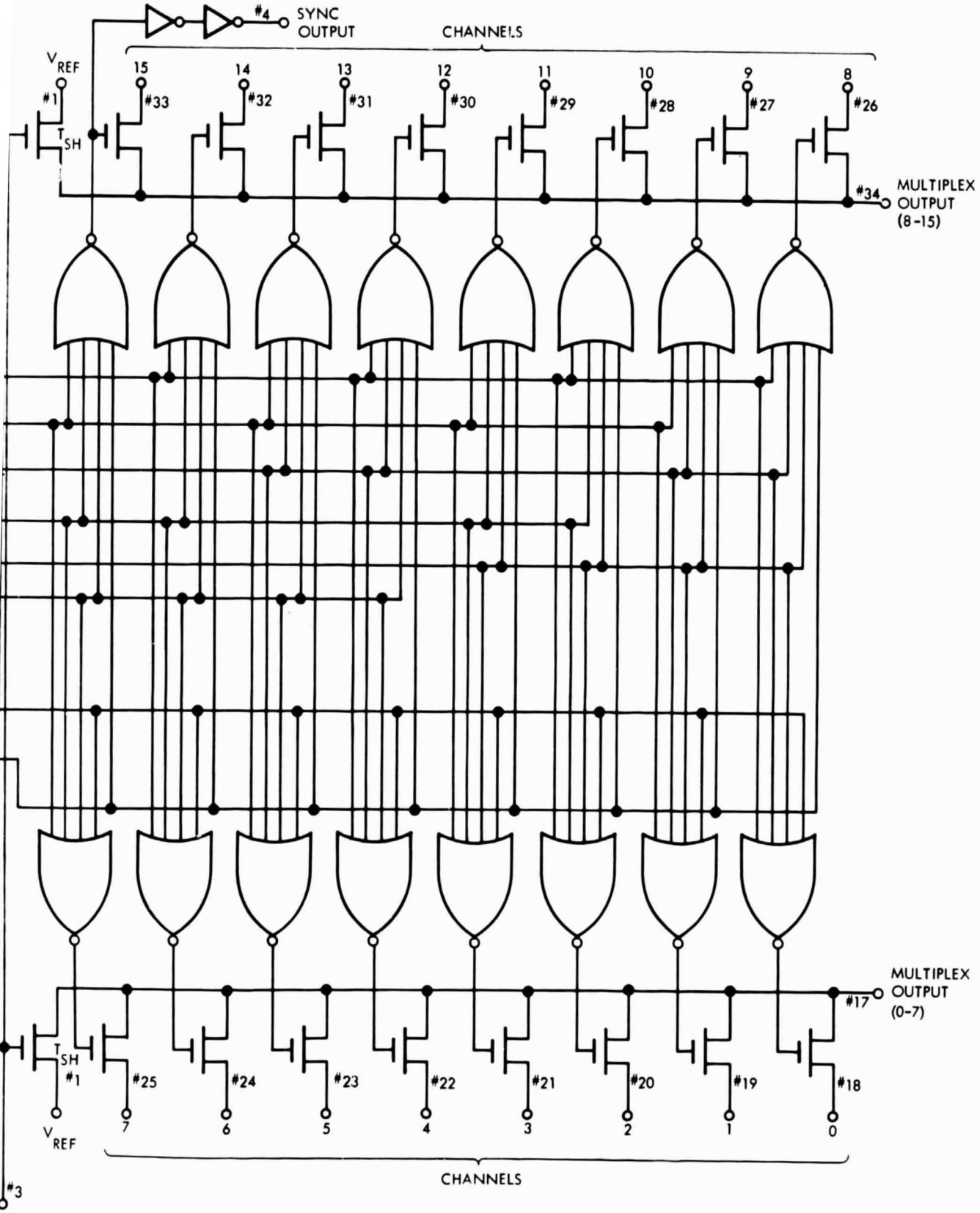
CHARACTERISTIC	MIN.	MAX.	UNITS	CONDITIONS
Signal Voltages, V_{IN}	0	-10	Volts	See Note 2
Clock Frequency	0	100	kHz	Sequential Mode
Clock and Parallel Load Pulse Width	2		μs	See Note 3
Switch Settling Time		5	μs	From -10V point on clock to 90% point on output; R_S = 1kΩ
All Logic/Control Inputs: "1"	-9		Volts	
"0"		-3	Volts	
Input Capacitance (Each Channel)		5	pF	V_{IN} = -5V
Channel Switch R_{ON}		1000	Ω	V_{IN} = -1V
Shunt Switch R_{ON}		2000	Ω	$V_{pin\ 3}$ = -9V, V_{OUT} = -10 mV
Switch Input Leakage		10	nA	V_{IN} = -5V, T_A = +25°C
		100	nA	V_{IN} = -5V, T_A = +125°C
Output Leakage (16 Channels in Parallel)		20	nA	V_{IN} = -5V, T_A = +25°C
		200	nA	V_{IN} = -5V, T_A = +125°C
Channel Switch OFF Impedance, Z_{OFF}	3		MΩ	V_{IN} = -10V, f = 50 kHz
Power Dissipation		150	mW	V_{DD} = -28V

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3. The address inputs, pins 12 through 15, should remain at a fixed logic level during the parallel load pulse.

OGIC DIAGRAM

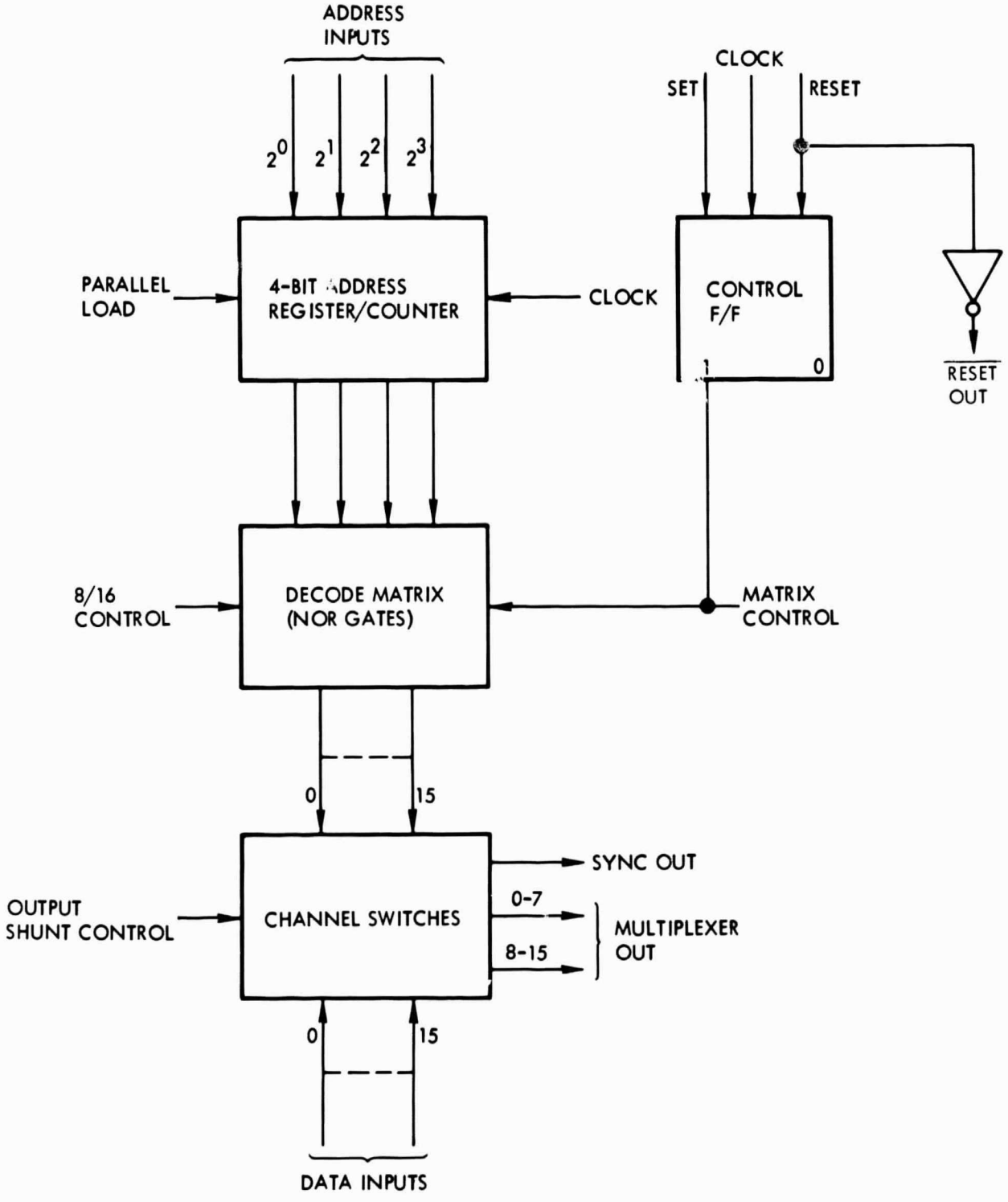


FOLDOUT FRAME 1

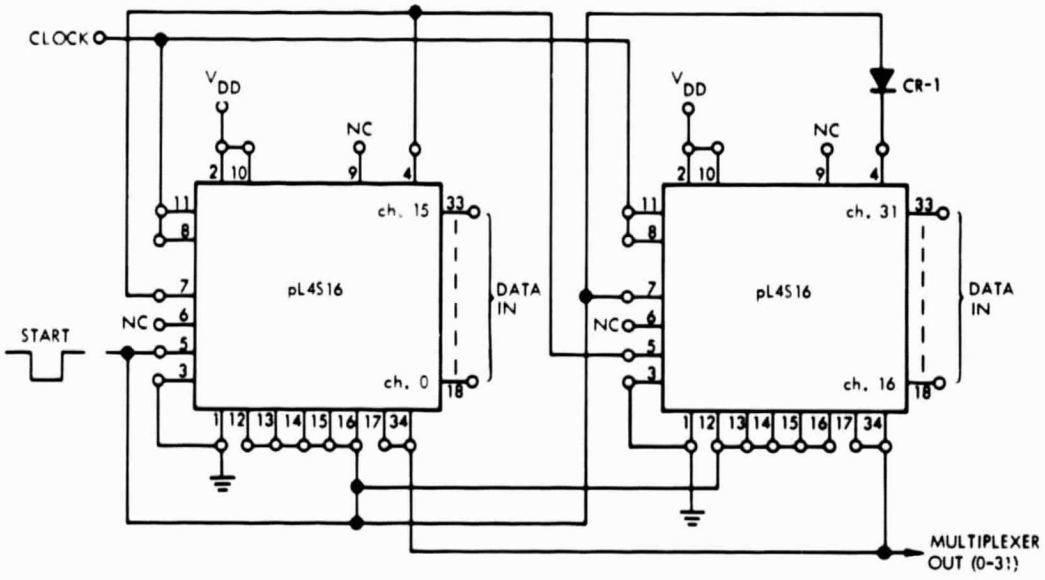


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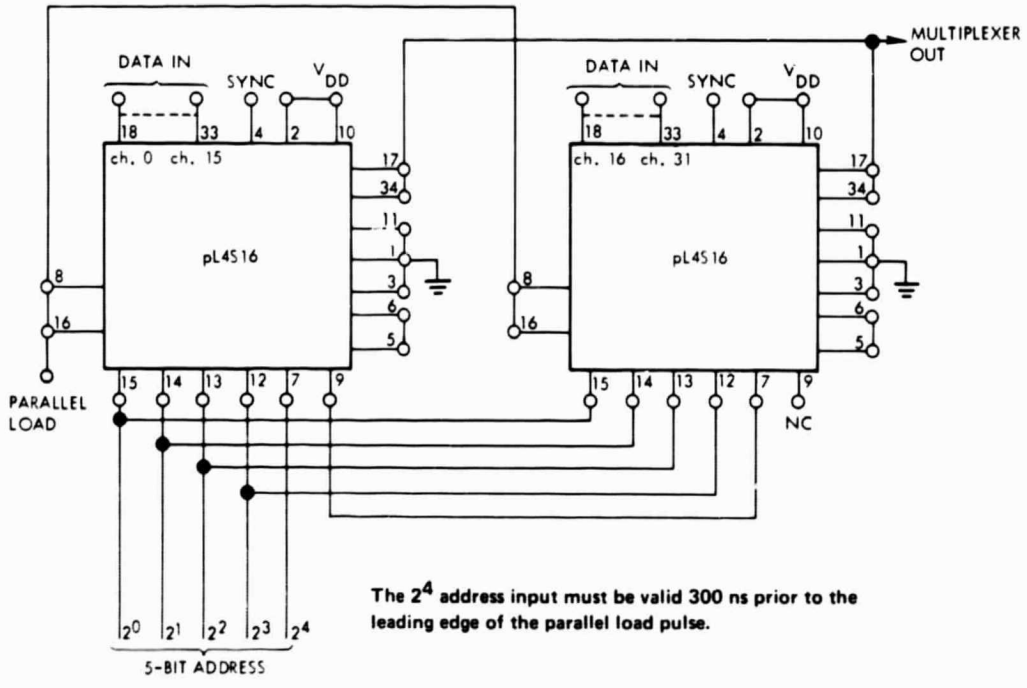
BLOCK DIAGRAM



TYPICAL INTERCONNECTIONS



SEQUENTIAL SAMPLING OF 32 CHANNELS



The 2^4 address input must be valid 300 ns prior to the leading edge of the parallel load pulse.

RANDOM ACCESS TO 32 CHANNELS

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[illegible]
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Burlington, Massachusetts 01803
TWX: 710-332-1364

Union Meeting Road
Blue Bell, Pennsylvania 19422
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TWX: 510-661-0101

[illegible]
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TWX: 710-504-0883

Philco-Ford of Canada
[illegible]
Don Mills, Ontario
Canada
(416) 444-2541

[illegible]
Santa Clara, California 95051
(408) 246-2666
TWX: 910-339-9238

815 Connecticut Ave. N.W.
Washington, D.C. 20006
(202) 293-7010
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THE pL4S16 MOS 16-CHANNEL MULTIPLEXER

By Elizabeth deAtley and Joel A. Karp, MOS Applications Engineering

APPLICATION NOTE NO. 406 APRIL 1968

INTRODUCTION

The pL4S16 is an integrated 16-channel MOS multiplexer containing a four-stage address register/counter, random-access gating, decode matrix, and 16 switches on a single chip. It is packaged in a 34-lead hermetically sealed flat package.

This versatile subsystem can be used in all types of multiplexing applications: for example, in telemetry systems, satellites, sample data systems, etc. It can sample 16 channels sequentially or in the random-access mode; and it can also serve as a single or dual 8-channel multiplexer. For sampling more than 16 channels, two (or more) pL4S16's can be interconnected.

This application note briefly discusses the properties of the MOS switch, describes the operation of the 16-channel multiplexer, and explains how to use it.

THE MOS SWITCH

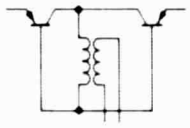
The MOS device offers many advantages as a switch. For example, it has very low leakage and zero offset voltage. Furthermore, it is voltage-driven and therefore requires no complicated drive network, as does the current-driven bipolar switch.

With a logic "1" on its gate, the MOS FET is equivalent to a closed switch in series with a low ON resistance. With a logic "0" on its gate, it is effectively an open circuit with a very low leakage current. In Table 1, the MOS FET is compared with two commonly used bipolar switches. The offset voltage of the MOS FET is of course 0 V, and its leakage is far less than that of either bipolar switch. Its larger ON resistance is not a problem in multiplexer applications, where the following stage usually has an input impedance of 10K or greater.

PHILCO-FORD 16-CHANNEL MULTIPLEXER

A functional block diagram of the Philco-Ford 16-channel multiplexer is shown in Figure 1, and a logic diagram in Figure 2.

TABLE 1. COMPARISON OF MOS FET AND BIPOLAR SWITCHES

	Single Bipolar Transistor	Back-to-Back Bipolar Pair	MOS FET
Electrical Characteristics			
Offset Voltage	≈ 3 mV	≈ 50 μV	0 V
Leakage Currents to Input and Output	≈ 100 nA	≈ 10 nA	≈ 1 nA
Series Resistance	≈ 15 Ω	≈ 30 Ω	≈ 750-1000 Ω*

*R_{ON} is minimum for low signal inputs and increases slightly with high signal inputs.

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CIRCUIT DESCRIPTION

The address register/counter consists of four master-slave flip-flops connected as a synchronous binary counter that can be directly accessed from four parallel lines under the control of the parallel load input (pin 16). For operation in the sequential mode, the random-access NAND gates must be disabled by connecting pin 16 to a logic "0". A schematic diagram of a single address register/counter stage with accompanying NOR gates is shown in Figure 3. The master and slave flip-flops are activated alternately by complementary $\overline{\text{clock}}$ and clock waveforms. These functions are obtained from the outputs of two cascaded buffer inverters (Figure 2) driven by the system clock at pin 11.

Connecting pin 11 to a logic "0" turns off T_{14} (Figure 3), isolating the slave flip-flop from the master. Under these conditions, information can be entered directly into the slave and the decode matrix.

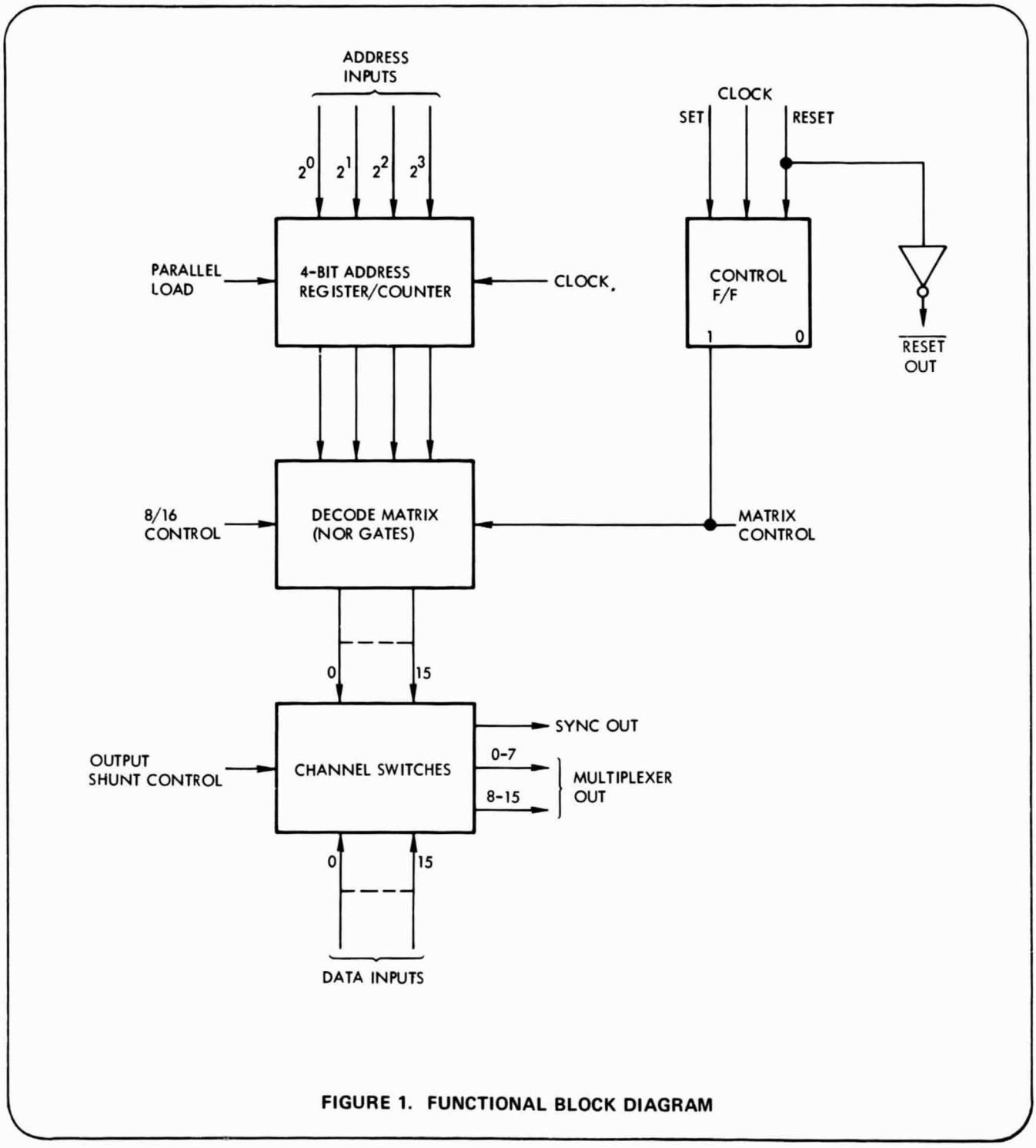


FIGURE 1. FUNCTIONAL BLOCK DIAGRAM

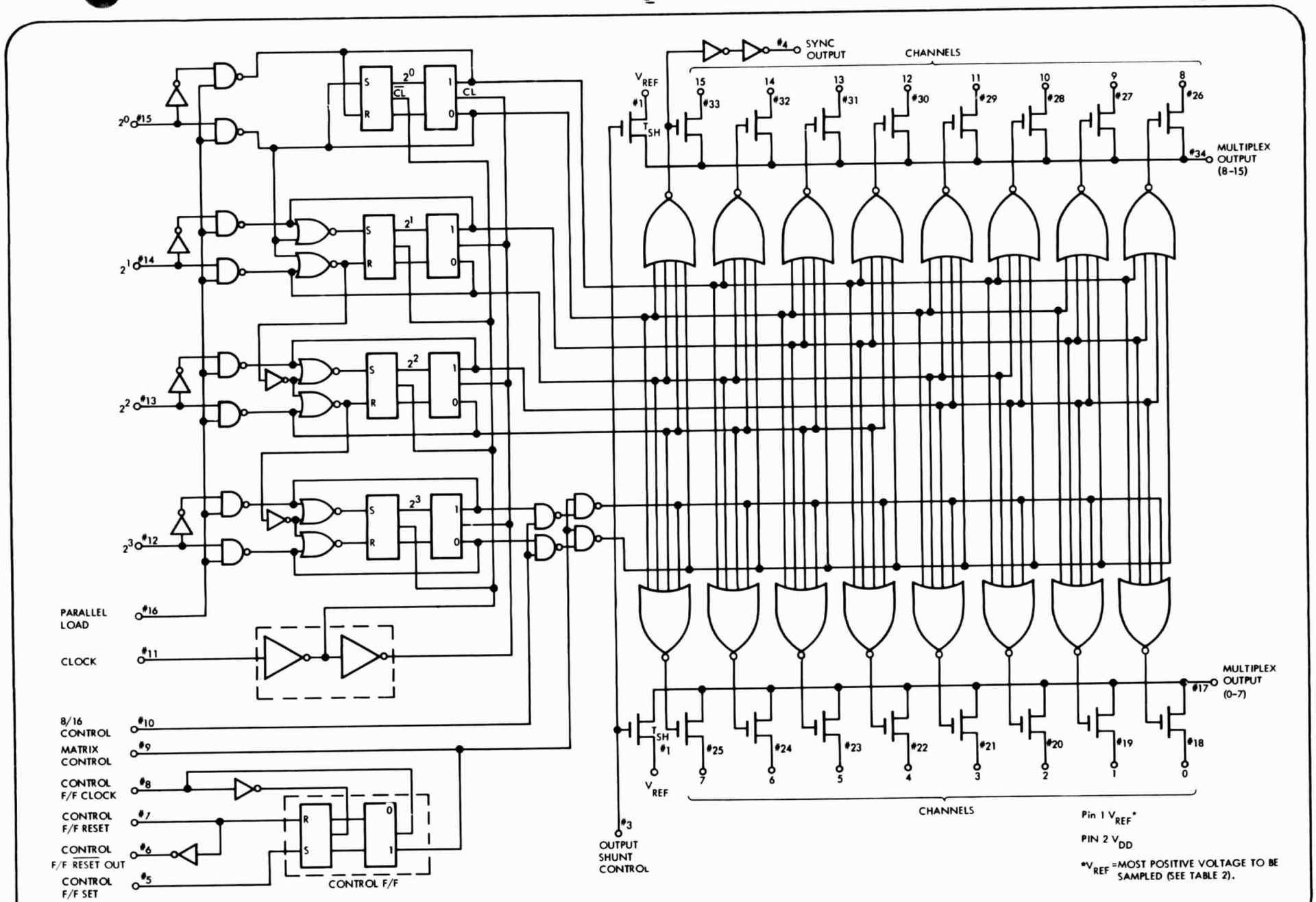


FIGURE 2. LOGIC DIAGRAM

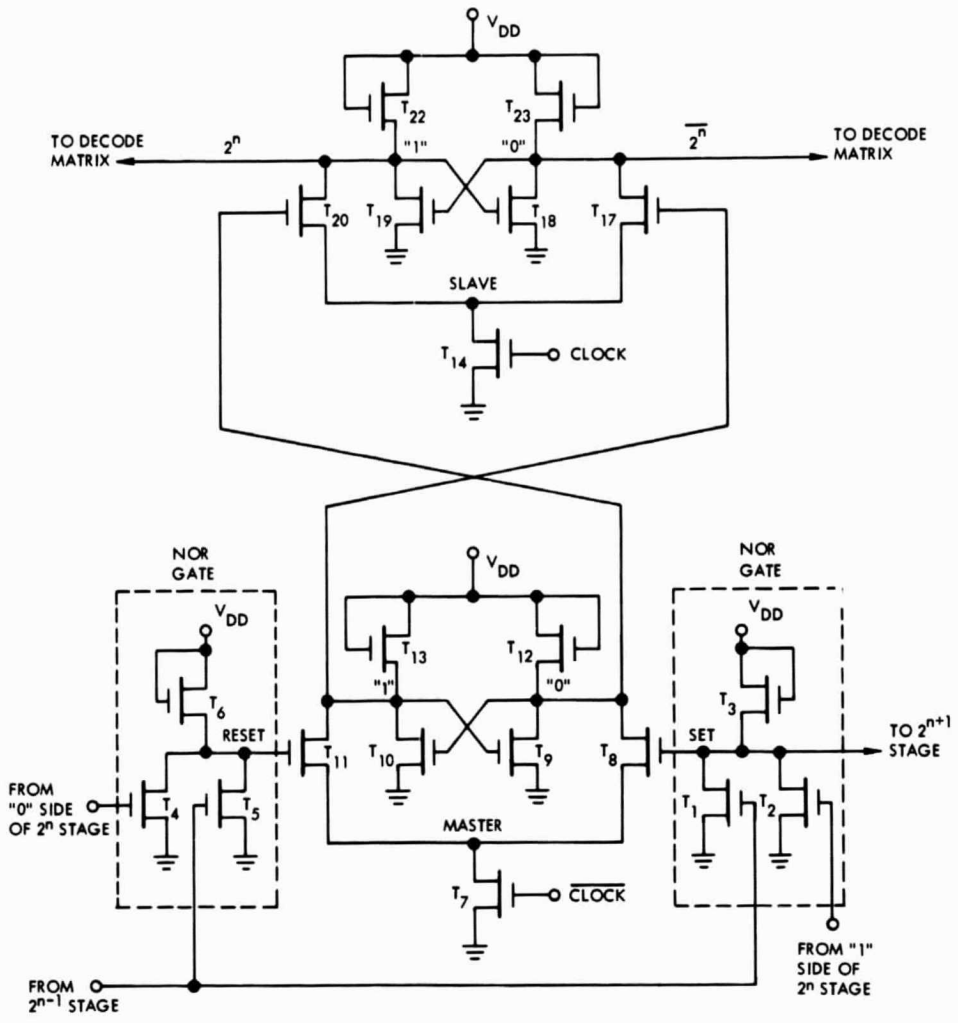


FIGURE 3. SCHEMATIC DIAGRAM OF 2^N STAGE OF ADDRESS REGISTER/COUNTER AND INPUT NOR GATES

The circuitry used for each NAND gate is shown in Figure 4. A logic "1" on the parallel load line activates T_4 and T_5, permitting the entry of the 2^{nth} bit and its complement directly to the decode matrix and the 2^{nth} slave flip-flop.

The decode matrix detects the state of the address register/counter and activates the corresponding channel switch through one of 16 four-input NOR gates. For example, when the counter is in state 1111, switch 15 turns on.

The channel switches are arranged in two banks of eight, which can be connected by shorting pins 17 and 34 together. Both output lines can be shunted to V_{ref} (see Figure 2) by applying a logic "1" to the output shunt control (pin 3) and thus turning on the two shunt transistors (T_{SH}). This eliminates channel overlap and allows multiplex data to be presented in an RZ format if desired.

With a logic "0" on the 8/16 control (pin 10), the 2^3 bit is inhibited and the channels turn on in pairs (0 and 8, 1 and 9, etc.). This permits differential-mode operation if pins 17 and 34 are kept separate, or eight-channel operation if they are tied together. With a logic "1" on pin 10, the output from the 2^3 flip-flop is connected to the decode matrix, and the multiplexer samples the 16 channels one at a time.

The control flip-flop functions as a one-bit address register used when two or more chips are interconnected. It is identical to one of the address register/counter stages, with its own clock input and separate set and reset inputs. An inverter is provided on the reset line for use if single-line control is desired. When the control flip-flop is in the "1" state, the entire chip is enabled. When the control flip-flop is in the "0" state, the entire chip is disabled.

The chip may be controlled directly via the matrix control (pin 9). When the matrix control is used, the clock input to the control flip-flop should be held at logic "0".

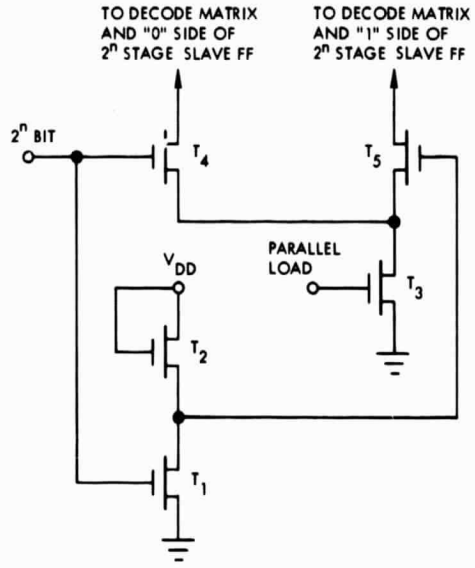


FIGURE 4. INPUT INVERTER AND NAND GATES FOR RANDOM-ACCESS MODE

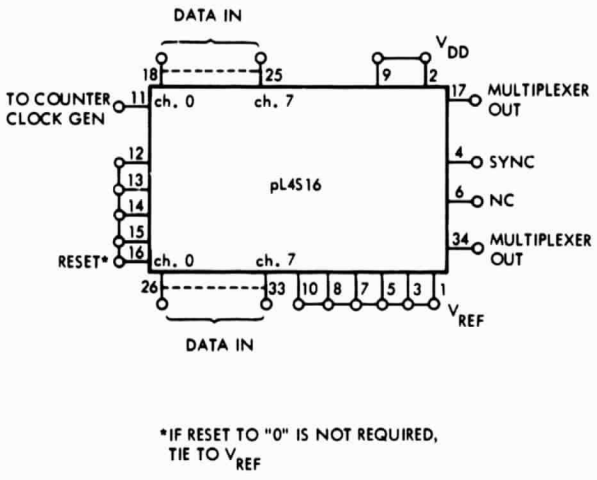


FIGURE 6. SEQUENTIAL SAMPLING OF TWO BANKS OF CHANNELS

SAMPLING MODES

When pin 10 is at logic "1" and pins 17 and 34 are shorted together, the multiplexer can be used to sample 16 channels sequentially. The required pin connections are shown in Figure 5.

When pin 10 is at a logic "0", the output from the 2^3 flip flop is isolated from the decode matrix. The multiplexer can then be used for simultaneous sampling of the two banks of channels at pins 17 and 34, respectively, as shown in Figure 6.

The required pin connections for the random-access mode are shown in Figure 7.

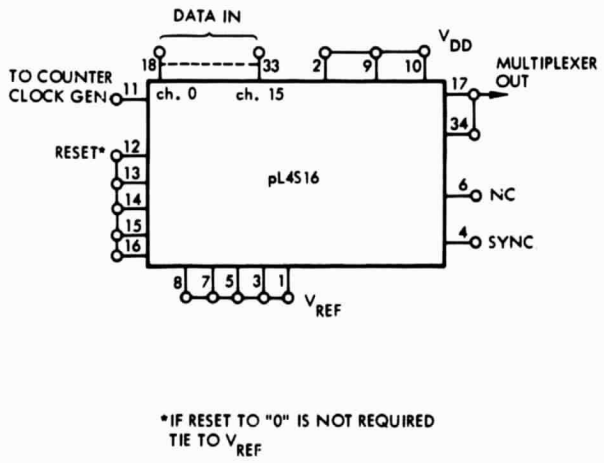


FIGURE 5. SEQUENTIAL SAMPLING OF 16 CHANNELS

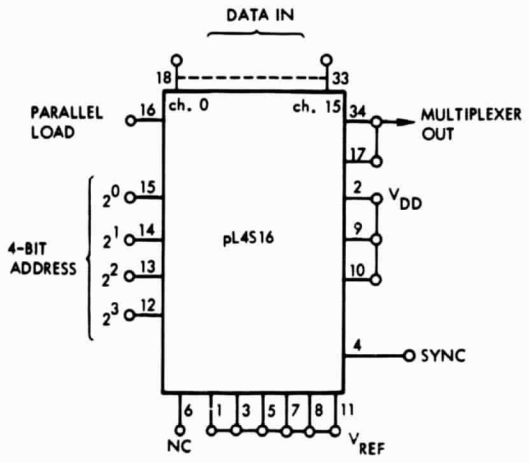


FIGURE 7. RANDOM ACCESS TO 16 CHANNELS

For sequential sampling of 32 channels, two multiplexers are connected as shown in Figure 8. (For counting above 32, additional multiplexers can be connected in the same manner.) The START pulse resets the address register/counter to "0"; sets the first control flip-flop; and resets the second Thus the first multiplexer is enabled and the second disabled. On succeeding clock pulses the switches in the first multiplexer turn on sequentially from 0 to 15. On count 15, the gate of switch 15 goes to a logic "1" and the sync output (pin 4) goes negative. This resets the first control flip-flop and sets the second, enabling the second multiplexer. When count 31 is reached, the sync output of the second multiplexer sets the first control flip-flop and resets the second, starting the process again at count 0. Diode CR-1 shown in Figure 8 isolates the START pulse from the sync output of the second chip.

For random access to 32 channels, two multiplexers can be connected as shown in Figure 9. A five-bit address is entered into the appropriate flip-flops in the two multiplexers by a negative pulse on the parallel load. The clock lines for the two control flip-flops are connected to the parallel load. Thus the fifth bit is entered into the appropriate control flip-flop simultaneously with the entry of the first four bits.

OPERATING VOLTAGES

The pL4S16 will sample a 10 V range of input voltages. If only negative voltages are being sampled, pin 1 (V_{ref}) is grounded. However, if positive input voltages are sampled, then V_{ref} must be held at the most positive input level. This is necessary to avoid forward-biasing the PN junction of the substrate. The V_{DD} supply must be 28 V ± 1 V more negative than V_{ref}.

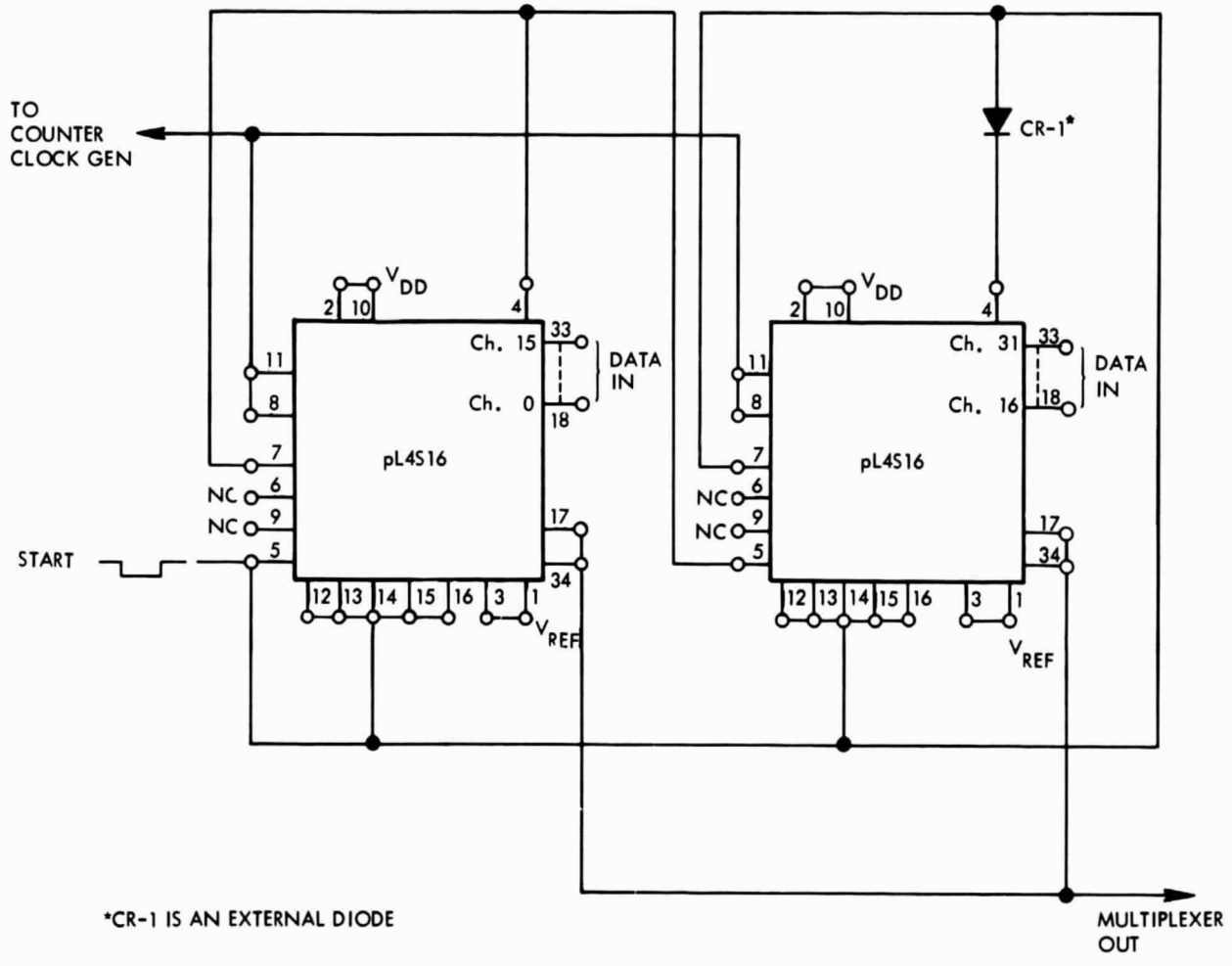


FIGURE 8. SEQUENTIAL SAMPLING OF 32 CHANNELS

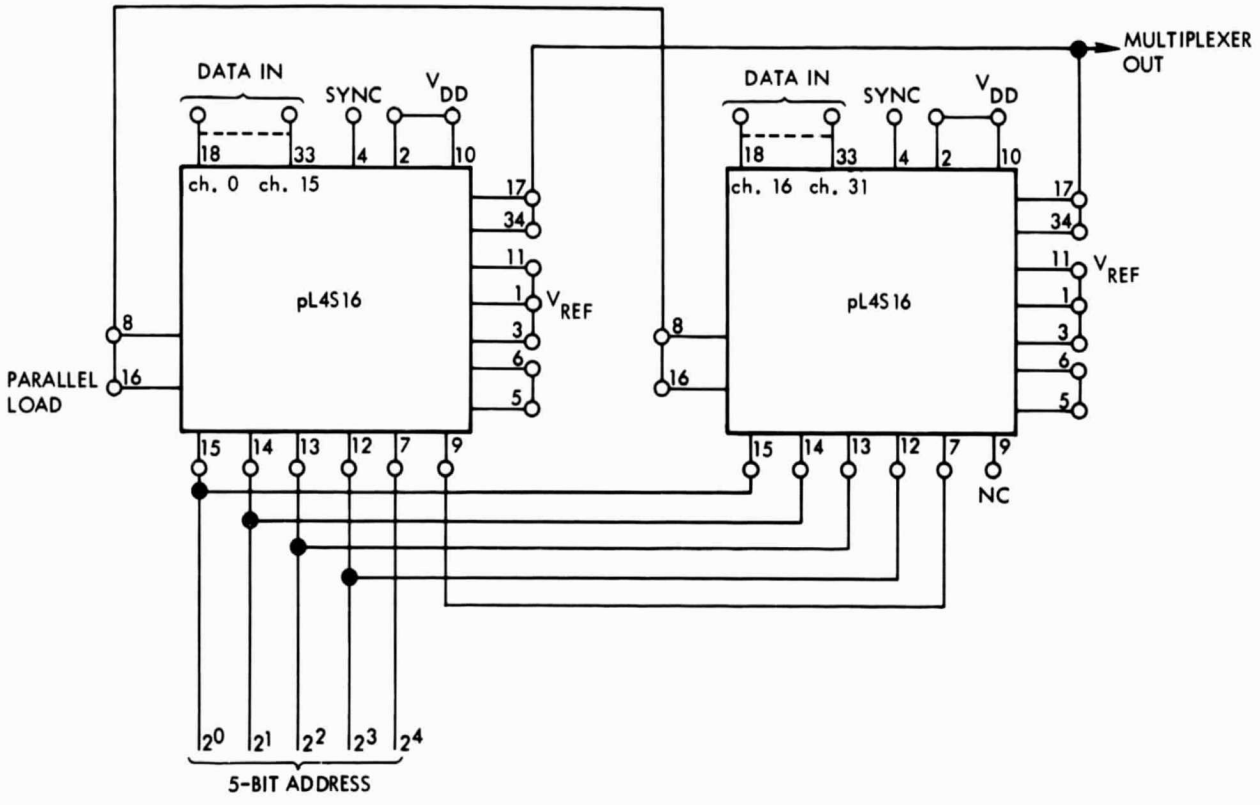


FIGURE 9. RANDOM ACCESS TO 32 CHANNELS

TABLE 2. OPERATING VOLTAGES

Max. Range of Input Voltages	Supply Voltages	Control Logic Input Levels
10 V	V_{ref} = ref. voltage = most positive input voltage $\lvert V_{DD} - V_{ref} \rvert = 28V \pm 1V$	Most neg. "0" = $(V_{ref} - 3V)$ Most pos. "1" = $(V_{ref} - 9V)$

The required operating voltages are shown in Table 2. For example, if the range of input voltages to be sampled is

$$-8\ V \leqslant e_{in} \leqslant +2\ V$$

then

$$V_{ref} = +2\ V$$

$$V_{DD} = -26\ V \pm 1\ V$$

The most negative "0" level is –1V, and the most positive "1" level is –7 V.

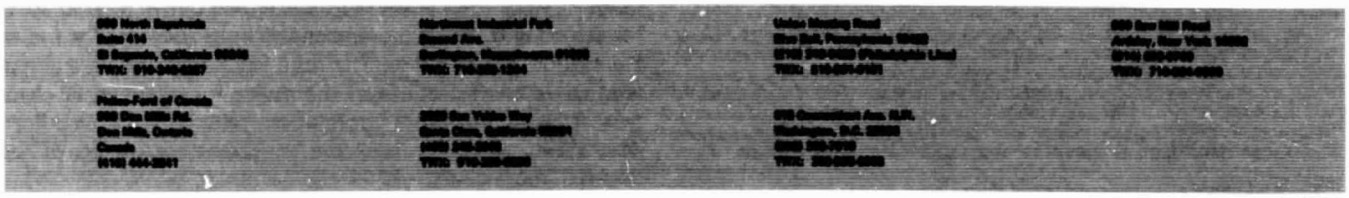
CONCLUSION

This application note has explained the operation of the pL4S16 MOS 16-Channel Multiplexer and shown how to use it for sampling 8, 16 or more channels both sequentially and in the random-access mode. The note has also shown several representative configurations of the device for sampling 32 channels or more. For more information, refer to the Philco-Ford data sheet, which explains the important parameters of the device in more detail.

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APPENDIX C

NEW TECHNOLOGY

The 16-channel multiplexer was designed utilizing standard MOS design circuitry. There were no new circuit techniques developed or utilized for this product.

The designs were based on the MOS parameters that were then being produced in the production department. No new semiconductor techniques were needed to accommodate the multiplexer required on this contract.