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COLLEGE OF ENGINEERING

Department of Electrical Engineering

Computer Science Research Laboratory

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A Hybrid-computer Data-channel Interface and
its Application to the Simulation of Variable Time Delays

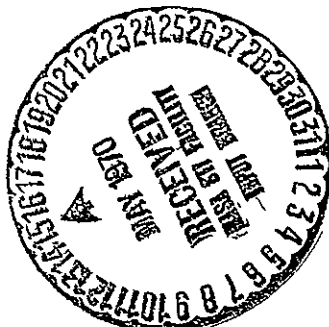
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January, 1970

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ABSTRACT

This report describes implementation of a data-channel interface for the ASTRAC II high-speed iterative differential analyzer and the PDP-9 digital computer, and its application to the simulation of variable time delay (e.g. pipe-line delays in aerospace and chemical problems.) The cycle-stealing data-channel interface effects automatic block transfers of data from and to the digital computer at rates of up to 250,000 words per second in response to request pulses from the analog computer. Variable time delays can be implemented if analog data read in and stored at a constant sample rate are read out into a digital-to-analog converter at a variable rate established by a voltage-controlled oscillator patched on the analog computer. A simple integral equation was solved to test implementation of (constant) time delays.

1. General description

The FDP-9 data channel interface for the ASTRAC II analog computer⁷ provides a fast data transfer between FDP-9 and ASTRAC II. Requests for data channel transfers from or to the ASTRAC II are honored by the channel at the completion of the FDP-9 instruction in progress.

The channel is controlled by word count and current address registers held in the digital-computer core memory. Both registers are initialized by a program instruction depositing suitable words. When the processor honors a data-channel request, the respective device transmits the address of its assigned word-count register. During the first cycle of the channel transfer, the contents of this word counter are incremented, and the address of the current-address register is established.³

In the second cycle, the contents of the current-address register are incremented to establish the effective address of the memory location delivering or receiving the data word.

During the third cycle (or fourth cycle in the case of out-transfer), the actual data transfer occurs. Because of these counting operations, such memory implemented data channels steal three or four computer cycles per data transfer, but still permit maximum word transfer rates exceeding 250,000 words per second at very low cost.

2. Interface Design

The interface shown in Fig. 1.1 can be used to either read data from the FDP-9 into an analog computer or vice versa.

The primary data transfer devices already installed are the AD converter (ADC) with four multiplexed analog inputs (ADIN), and four multiplying DA converters (MDAC). A Digital Equipment Corporation interface card (W 104) is used to establish data-channel requests.

The circuit operates as follows:

1) Device data request flag.

The device data-channel request flag places a ground level on the flag input when a data-channel transfer is required.

This ground level enables the REQ flip-flop in the W104.

The pulse IO SYNC which occurs at 1- μ sec intervals and is available on the IO BUS sets the REQ flip-flop in the W104. This pulls the PDP-9 request line to ground thus, requesting a data-channel break cycle in the computer.

If repetitive data transfers are not desired (or not desired at the maximum possible rate), the device flag must be cleared to prevent false data channel cycles and associated loss of data. In our circuit, the clear flag signal from the W104 is used to reset the device flag.

2) Grant signal.

When the PDP-9 is ready to initiate the requested data-channel break, it issues a grant signal to the device. The trailing edge of this signal produces CLR flag which resets the device flag beforementioned, and also sets the ENA flip-flop gating onto the IO ADDR lines. This flip-flop then enables the ENB flip-flop, which is set with the next IO SYNC pulse. This causes SELECT of the W104 to go to ground. Connected to the force-select input of a W103 device selector, this

simulates the W103's proper device code, permitting IOT pulses to pass through it.

Meanwhile, ENB is used to gate a Read request (RD RQ) or write request (WR RQ) level to the FDP-9. In the case of a read request, the transfer pulse IOP2 is issued and the data buffer gated on the bus. In the case of a write request, the IOP4 is issued on the reset cycle.

3) Enable signal

ENA IN of the W104 must be connected to the data-channel enable line on the IO bus running toward the FDP-9. ENA OUT must be connected to the next lower priority device (if any) on the data-channel bus. This arrangement sets up priorities for data-channel requests from two more devices.

Data channel timing diagrams are shown in Fig. 1.2.

4) Linkage patchbay

On the linkage patchbay of the ASTRAC II which the user can patch to meet the requirement of his particular application, we have provided the following terminals (See Fig. 1.3).

REQ; The positive-going request signal from device to the data channel indicates that device requires data channel transfer.

RDENA; Enabling RD RQ signal indicates that the device wishes the transfer to be in the "input" direction.

WR ENA; Enabling WR RQ signal indicating that the device wishes the transfer to be in the "output" direction.

RD ENA and WR ENA; Enabling the add-to-memory operation which is a combination of reading and writing.

INC ENA: Enabling the memory increment operation, i.e., the word specified on the IO ADDR lines is incremented.

IO OFLO: A pulse originating in the channel logic which indicates that the transfer of specified number of data words has been completed.

MEM OFLO: Indicating data-channel transfer complete.

ADDR: 14 gate inputs specifies WC ADDR for RD and WR operation. (ground is "0", open c.c.t. is "1").

DATA IN: 18 Bus-gate inputs into PDP-9 IO bus strobed by IOT2 pulse. (ground is "0", open c.c.t. is "1").

DATA AVAILABLE: IOT4 pulse indicates that requested data is on the IO Bus lines. Usually wired to DAPLOAD or DAILLOAD depending on MDAC0 or MDAC1 is currently used.

DAP LOAD: Input pulse into this termination produces two timing pulses 1.5 μ sec apart to transfer output data from the accumulator to the buffer register, and from the buffer register to the device register in the MDAC0.

DAL LOAD: Same as DAP LOAD except MDAC1.

B: A pulse to transfer output data from accumulator to buffer register.

D: A pulse to transfer output data from buffer register to device register.

ADC: 12 bit ADC outputs ($-3V$ is "1")

3. Operational description

Figure 1.4 shows an example of a data-channel interface applied

to a variable-time-delay system (see below).

Flip-Flop B202(1) is set by positive-going pulse, which comes from a circuit patched on the analog computer, after the word-count (WC) and current-count (CA) registers have been initialized by the program. This produces a ground-level pulse to set the REQ flip-flop in the W104. Reset-input terminal of the flip-flop B202(1) and CLR REQ is patched from CLR FLAG when repetitive data transfers are not desired, as in the case of variable time delays. The W104 is connected in a standard configuration. It issues a WR EQ pulse when WR ENA is at ground level, and RDEN A is at -3V. Also it issues a RD EQ pulse when RDEN A is ground level and WR ENA is -3V level.

The IO ADDR lines can be connected for any number of different word-count and current-address registers in memory. But the following core-register assignment for this data channel is used, because only one address bit, that is, IO ADDR 14 line is different between READ and WRITE (Fig. 2.2):

Word count 32, Current address 33 for READ.

Word count 22, Current address 23 for WRITE.

The W104 enables a W103 to allow the IOT2 pulse to strobe data from device and the IOT4 pulse to jam transfer data into the device buffer register using both DATA AVAILABLE and DA LOAD. IO power clear is used to reset all flip-flop, when the computer is first turned on.

Figure 1.5 shows the logic-card module layout for the DATA channel interface and, specifically, for variable time delays. This figure indicates the type of logic module found at each location in the interface mounting panels when viewed from the front of ASTRAC II.

Variable-Time-Delay Simulation

1. General Description

Time delay arises from the finite time it takes to propagate an information (signal) for the source to the receiver in a medium. Should the medium in which the signal is propagated change properties as a function of time, the resulting delay could become variable in time.

The magnitude of the delay in propagated signal is dependent on two quantities: the velocity of propagation (V) and the distance between sender and receiver (D). If either of these quantities varies, have a variable-delay problem.

Typical pipeline problems involve a fixed distance with a continuously-variable propagation velocity. Several methods are available to simulate constant time delays, but few are satisfactory for a continuously variable delay. The system described is a relatively new hybrid analog-digital implementation. The basic idea is to sample a data signal at a constant rate, put the samples into core memory, and read them out at a sampling rate proportional to the flow velocity, as determined by a voltage-controlled oscillator (VCO).⁶

2. Variable-Time-Delay Design

The data input signal is converted to 12 bit binary form in an analog to digital converter (ADC) with constant sampling rate. Samples are stored in a block of core memory of the PDP-9, using a data-channel READ operation. An analog voltage proportional to the rate of change of the desired delay velocity in a pipe is applied to an analog-voltage-controlled oscillator whose output-pulses serve as request pulses for data-channel write operations. The pulse repetition rate determines the

rate at which data is taken out of memory, and therefore the time the data is in memory, that is, the delay. The starting address of the CA register for data channel read and data channel write is changed according to the initial time delay required.

The VCO is patched on the analog-computer patchbay (Fig. 2.b). The output of the core memory is converted to analog voltage in a MDAC.

A few modifications of the standard data-channel interface were needed to be used as a variable time-delay system:

- 1) Generation of DCH REQ signal.
- 2) Mode selection between RD RQ and WR RQ, and also establishment of priority between RD RQ and WR RQ.
- 3) Control of the WC and CA register with a single data channel.
- 4) Generation of a pulse proportional to the velocity of delayed signal.
- 5) Data-channel register initialization for making an "endless loop" memory.

The first three requirements are met by the variable-time delay logic shown in Fig. 2.1 and Fig. 2.2.

DCH REQ signal must occur when data signal sampling clock (read instruction) or VCO output pulse (write instruction) comes.

Since the WRITE request pulses from the fixed-rate clock and the READ request pulses from the VCO can overlap or even coincide, the pulse-separation circuit of Fig. 2.3 was designed to give priority to the WRITE request pulse, and also to produce READ and WRITE request pulse waveforms $\frac{1}{2}$ μ sec long and synchronized with the PDP-9 IO SYNC

timing signal (see also the timing diagram of Fig. 2.3-1).

Since the minimum required time interval between data channel read operation and data channel write operation is 7 μ sec, we must separate sampling clock and VCO pulse from each other more than 7 μ sec. Four monostable multivibrators (4 MMV's), two AND-gate, and two OR-gates perform this function of separation.

The 7 μ sec minimum required time interval between read and write is determined by the following considerations. After a device flag is raised, it takes two processor cycles (i.e. 2 μ sec) to receive the grant signal (DCM GR) from the channel of PDP-9. One processor cycle later, the actual data-channel transfer starts. Each output data-channel transfer steals four processor cycles. Therefore, 7 μ sec is needed to complete data channel operations (see Fig. 2.5).

The Mode flip-flop selects between READ request (RD RQ) and WRITE request (WR RQ). An AND-gate receiving the output of the mode flip-flop and the enable signal (ENA) from the W104 card is used to select the address of one of two word-count (WC) registers in core memory; the first corresponds to the WC register for READ (assigned core address 32 in octal notation), and the other corresponds to the WC register for WRITE (assigned core address 22 in octal notation). There is only one bit difference between these two addresses of core memory registers (i.e. IO ADDR line 14), so that the switching logic is simple.

The fourth requirement is met by an analog-voltage-controlled oscillator. Figure 2.6 shows the block diagram of this VCO, which is

patched on the analog-computer patchbay. The VCO operating characteristic (input voltage versus output frequency of the VCO) is shown in Fig. 2.7. When the input voltage changes from 0.5 volts to 9.0 volts, the output frequency changes 150 Hz to 9200 Hz (linearity is within 1%). Output frequency of the VCO is adjusted to 5000 Hz when 5 volt of input voltage is applied.

The last requirement is met by simple initialization programs, (i.e., neither program interrupt facility (PI) nor multilevel automatic priority interrupt facility (API) was used). Because the maximum speed of the data Channel read or write is determined by the highest pulse repetition rate of the VCO, and is relatively slow (max p.r.r. is 9200 Hz; therefore its period is 110 μ sec). An initialization program of this data channel generally consists of two programs; one is a detection routine when WC register has counted up to zero, the other is a service routine that deposits WC, CA register with suitable words. However, if a primary importance is placed on the speed of data channel transfer, then PI or API should be used.

3. Typical performance

The Data-signal-sampling clock rate must be selected according to both the frequency of the data signal and the desired delay time. The period between read-in pulses depends on the sampling clock. The pulse repetition rate from the VCO is $150 + 1065(V-0.5)$ Hz where V is the voltage of input signal to VCO. Since V varies from 0.5 volt to 9.0 volt, this pulse rate varies from 150 pps to 9,200 pps, the

period between write-out pulses is 110 μ sec to 6 msec. If we use, for example, 1000 words of active core memory for this time delay system, the delay obtained is 1000 times the time period (i.e. the delay time is from 110 μ sec to 6 sec.). The more core memory capacity is used, the larger delay time is obtained, although the maximum available core memory capacity will depend on the application. In this case, in order to secure 20 samples per cycle of data signal wave over the whole delay range, the highest frequency of the data signal is about 33 Hz; a delay-bandwidth product of 200 will require 1000 words of "core memory".

Errors in time delay arise from three main sources; 1) The error introduced by the VCO, which has a linearity error of 1.0%. 2) The maximum delay before the data is taken out of memory and reconstructed into an analog voltage by MDAC, 7 μ sec for data channel, 20 μ sec for MDAC; total 27 μ sec. 3) Error in reconvertng the memory output to an analog voltage in the MDAC (0.25%/Half-scale), and converting input data signal to binary form in ADC (0.1%).

The time-delay error for the entire system is the sum of the above errors.

As a demonstration of the use of constant time delays, simple application problem i.e. integral equation was solved. The examples are not meant to be exhaustive studies of particular application; rather it points out how the time delay is used.

1. Statement of problem

The mathematical description of many problems of engineering interest contains integral equations. Typical of a large class of such problems is the Fredholm integral equation of the second kind, namely

$$y(x) = f(x) + \lambda_a^b K(x,t)y(t)dt \quad (1)$$

where

$f(x)$ and the Kernel $K(x,t)$ are given functions

a and b are constants

λ is a parameter

$y(x)$ is the unknown solution

The following equation was actually solved:

$$y(x) = \frac{2}{3} + 2 \int_0^1 (x-t) y(t) dt \quad (2)$$

with the initial approximation $Y_0(t) = 0$. The step size was chosen as $\Delta t = 0.025$, i.e. $1/40$ and the Fisher's iteration method is used. This equation is a trivial example whose solution is easily seen to be $y(x) = x$.

2. Method of solution and result

Fig. 3.1 illustrates a two-time-scale hybrid computer method designed to solve a simple integral equation of (2). The integration variable t is represented by "fast" time $\tau = 1250t$ in an ASTROC II iterative differential analyzer, while x varies in 40 discrete steps

Δx between 0 and 1, stepping once per computer run.

Our time delay system is used as a recirculating function memory (40 DATA words). This memory supplies a complete trial approximation $y_n(t)$ once per computer run, and one function value is erased and corrected at the end of each run (every 1 millisecond of minor cycle). Therefore all function value corrections take 40 millisecond (major cycle).

Fig 3.2 and Fig 3.3 show logic diagram and timing chart for this example. Fig 3.4 presents a flow chart of the solution procedure; a complete listing of the FDP-9 program is given in Table 1.

Fig 3.5 shows successive approximations to the integral equation.

Fig 3.6 shows typical convergence characteristic of this hybrid computer solution with initial approximation $y_0(x) = 0$. Where solutions $y_n(t)$ were compared with exact analytical solution, $Z(t)$ by means of root-mean-square criterion, defined by

$$ERROR_n = \sqrt{\sum_{i=1}^I [Z(x_i) - y_n(x_i)]^2}$$

Fig 3.7 shows the solution wave form of this problem.

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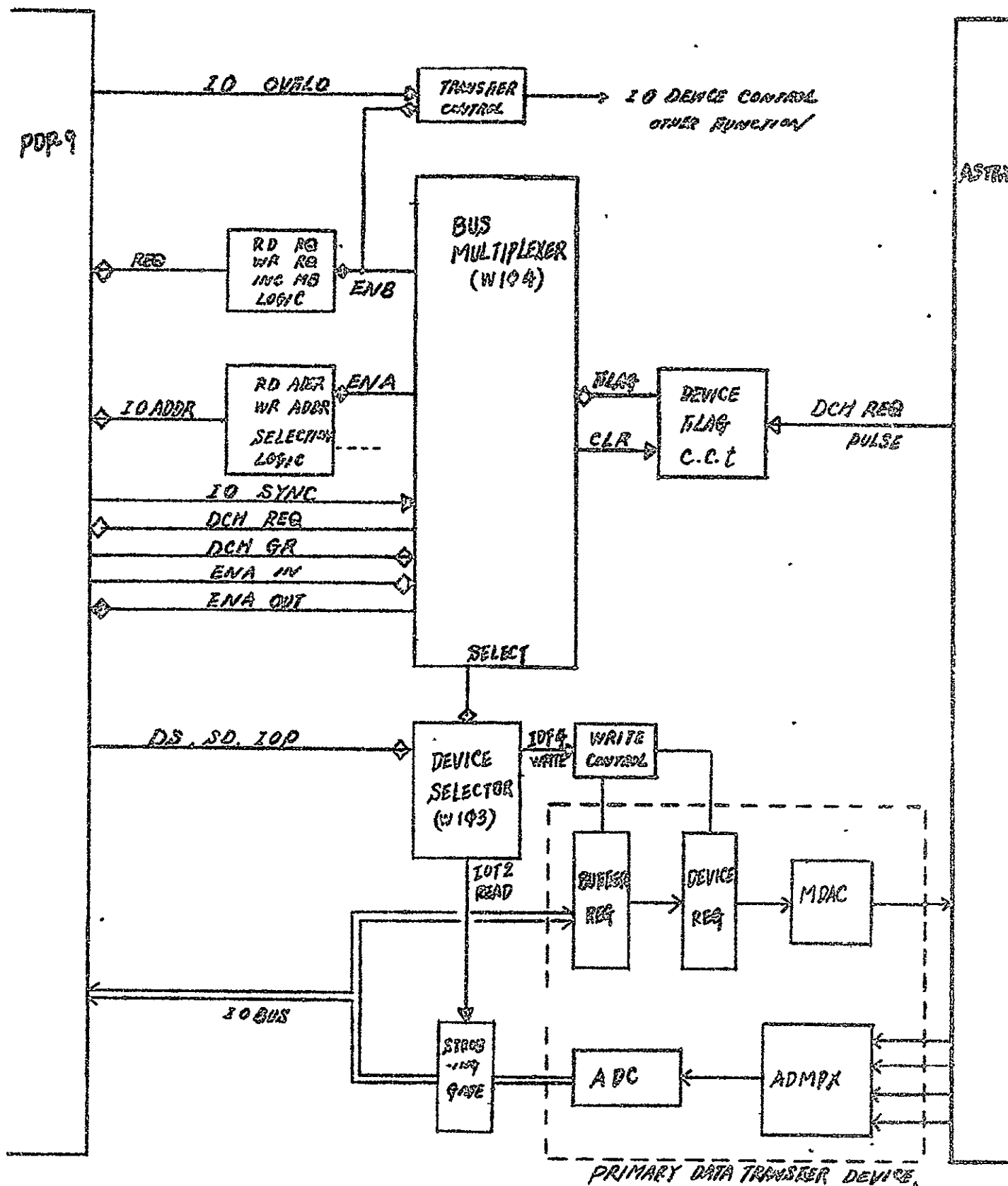


FIG 1.1 BLOCK DIAGRAM OF DATA CHANNEL INTERFACE

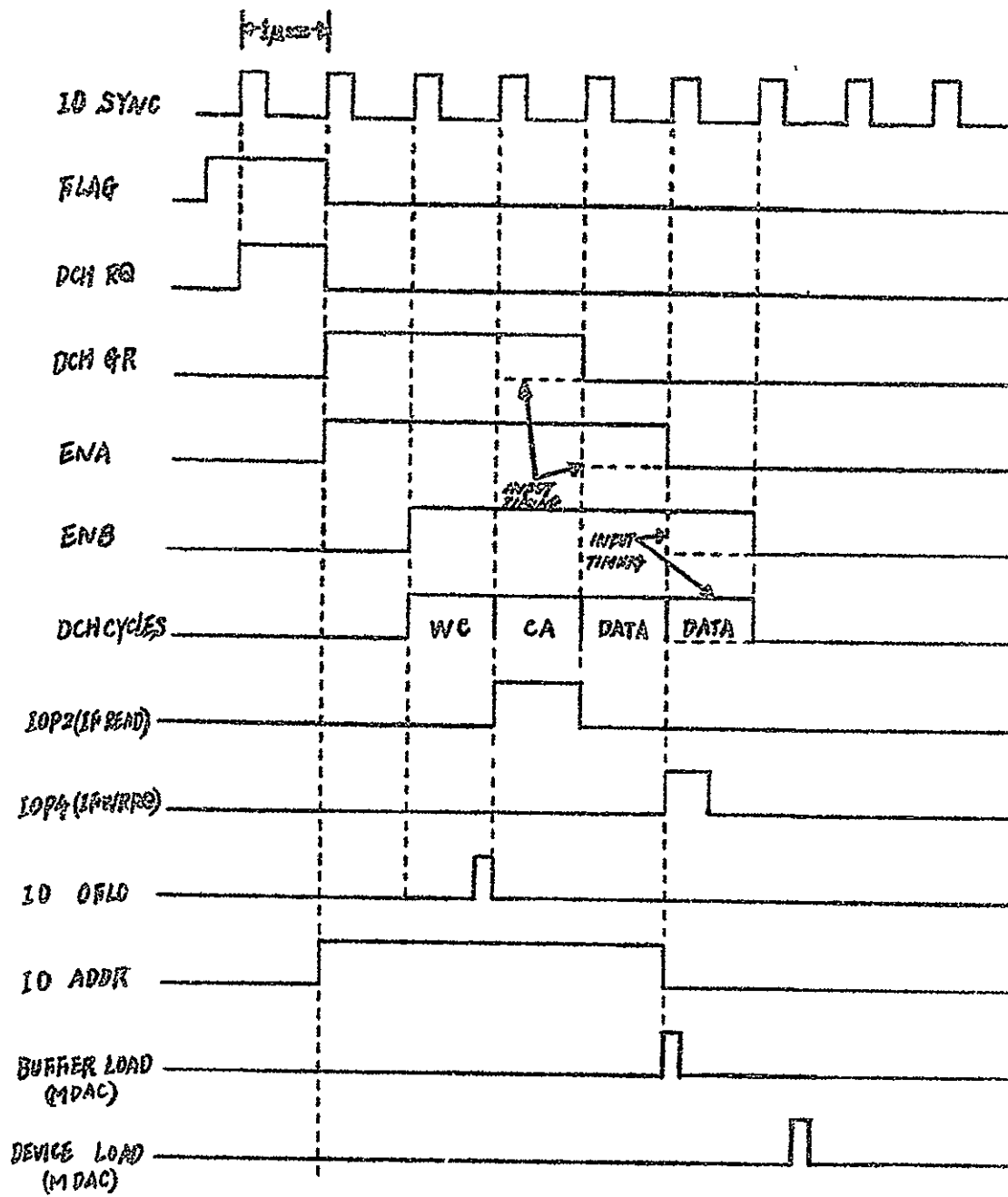
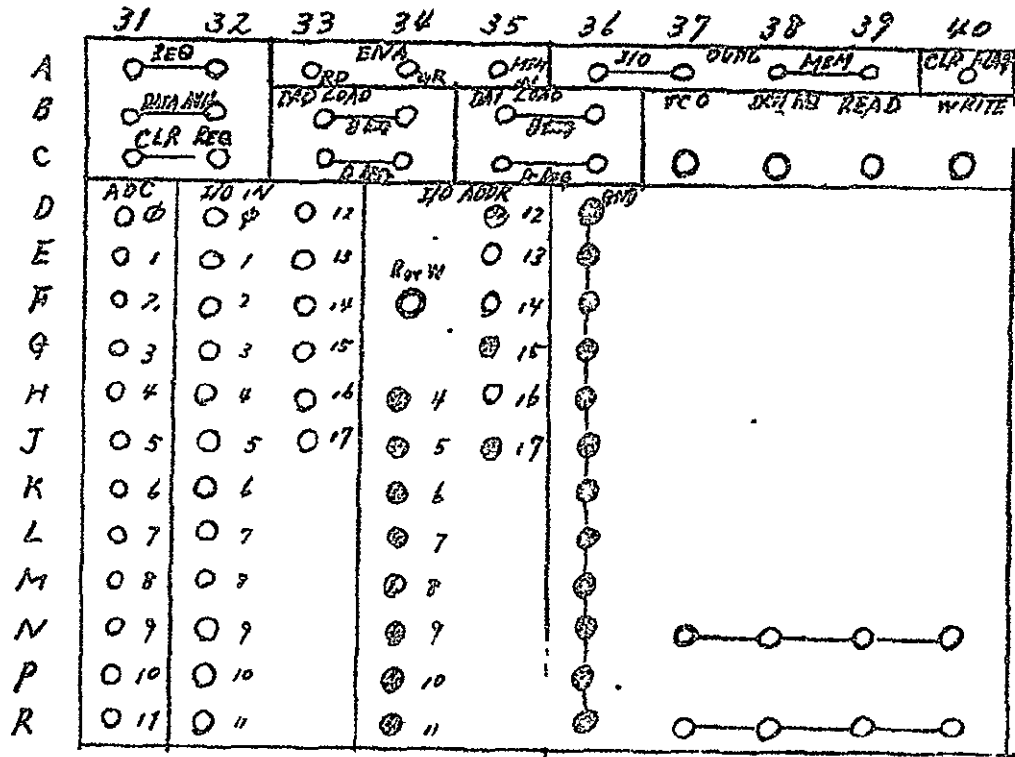
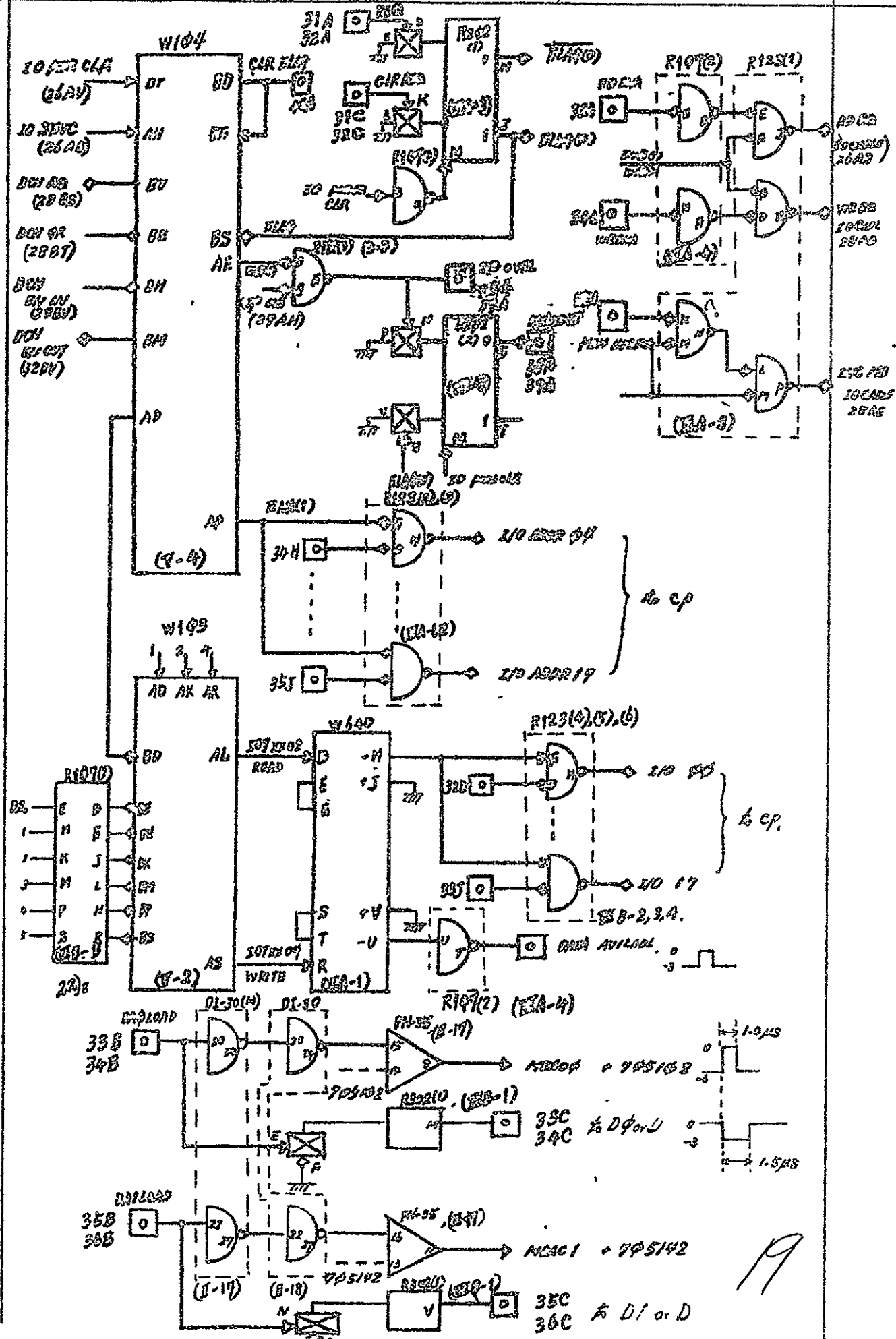


FIG 1.2 DCH TIMING

FIG 1-3 FRONT VIEW OF LPB FOR ASSTRACB/PDZ-9 DCH



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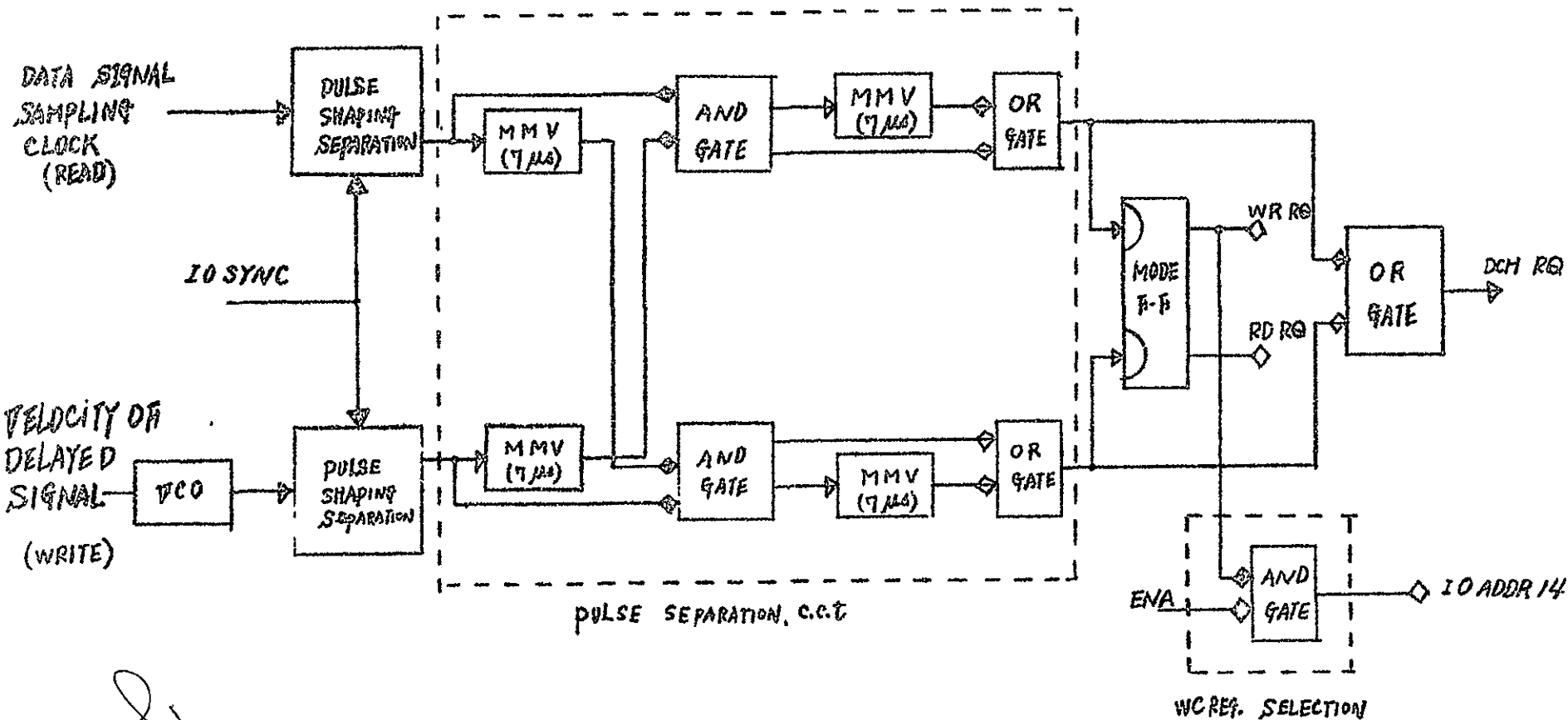


FIG 2-1 VARIABLE TIME DELAY LOGIC FOR DCH READING AND WRITING

		17	18	19
		01-000	01-00	X

	17	18	19
PN-35			

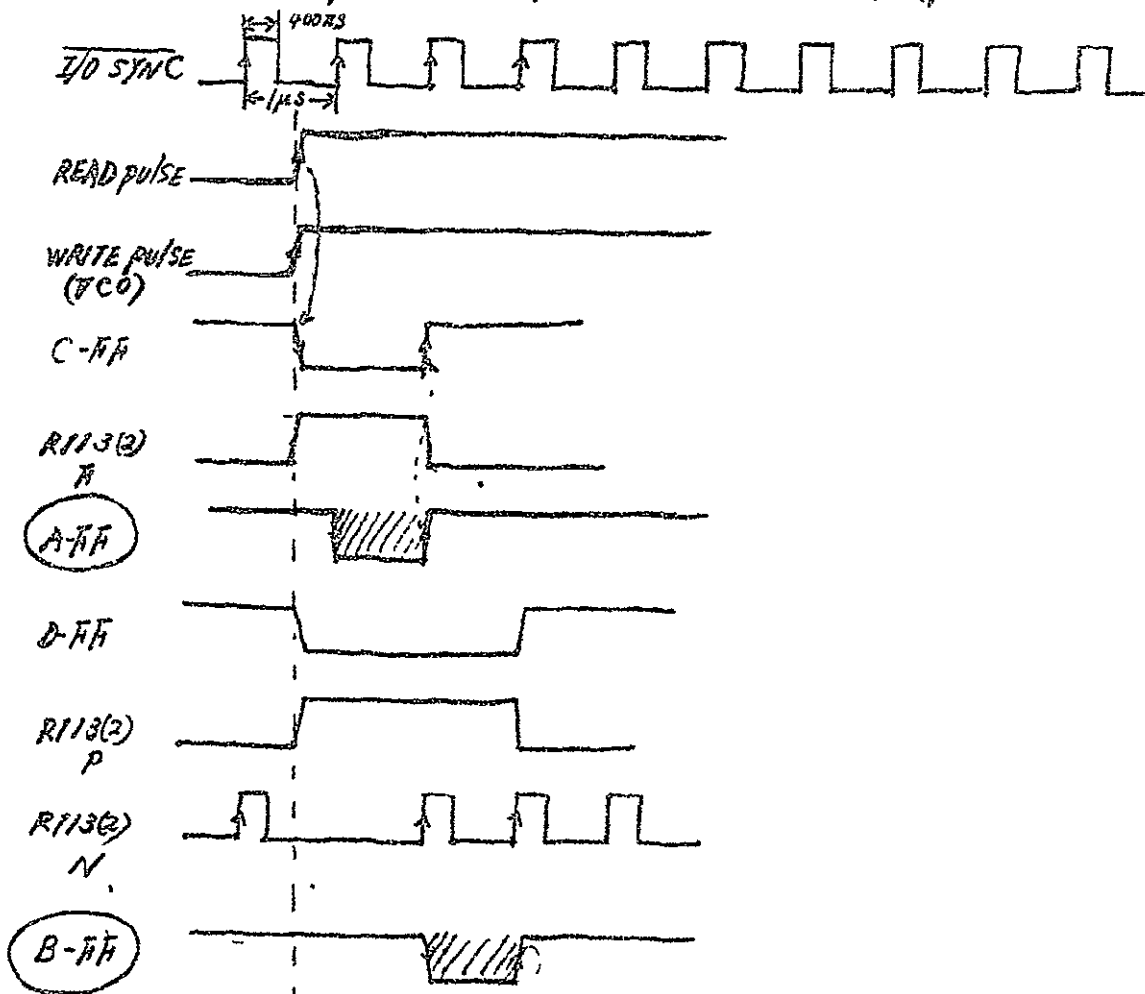
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22		
W640	W103	R202 (1)	W104								PRIMARY 1/0 CABLE				SECONDARY 1/0 CABLE								IA
R107 (1)		R113 (1)																					

	IIA	IIIB
4	R107(2)	R123(4)
3	R123(1)	R123(5)
2	R123(2)	R123(6)
1	R123(3)	<u>R302(1)</u>
		R202(4)
	R107(4)	

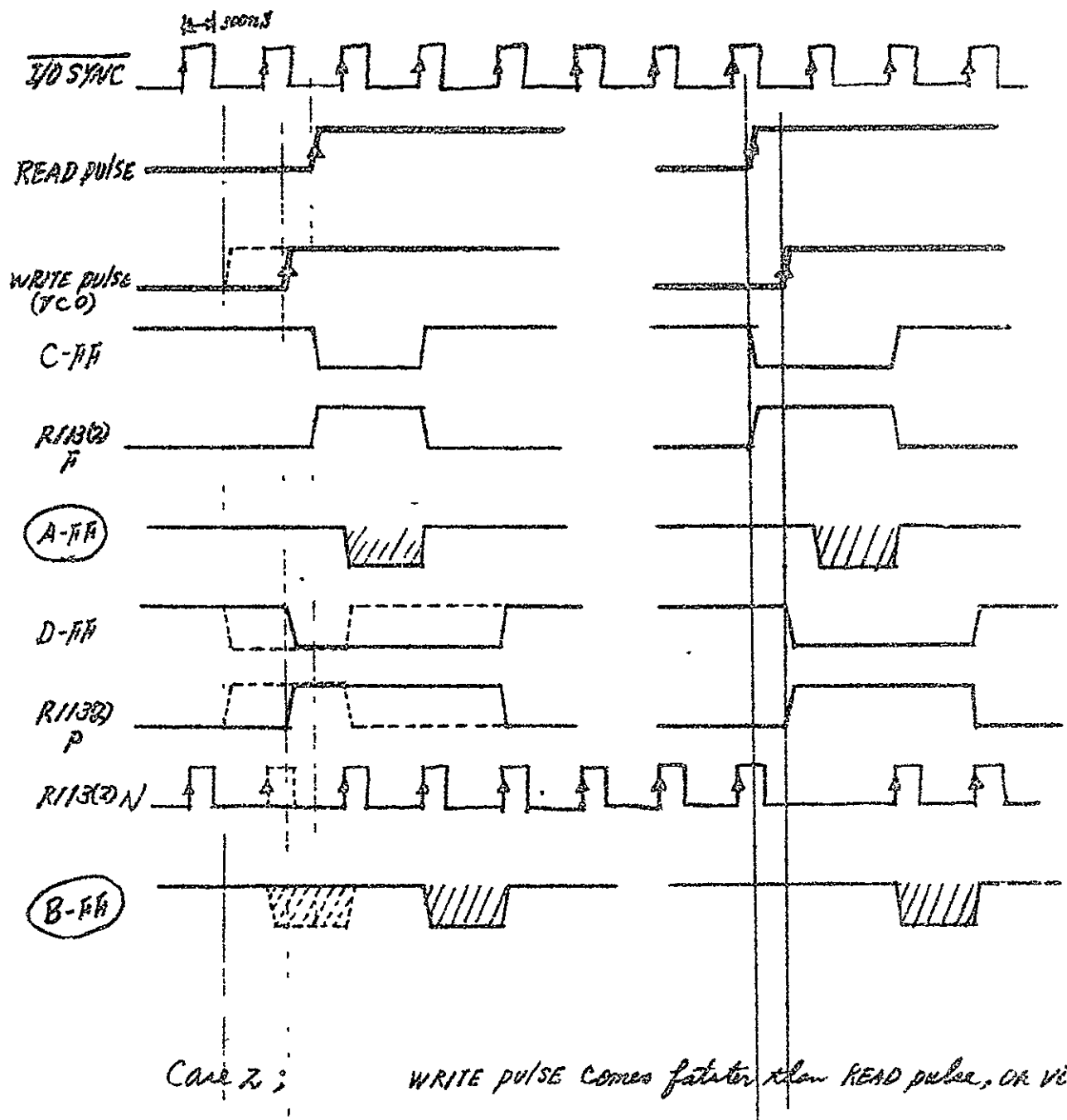
FRONT			
R202 (2)	R202 (3)	R302 (2) No Card	R302 (3)
	R107 (3)	R113 (2)	R113 (3)

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Fig 2.3. one clock pulse time phase shift c.c.t. (pulse shaping separation c.c.t.)



CASE 1 ; READ AND WRITE Request pulse come simultaneously



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FIG 2.4

PULSE SEPARATION C.C.T (MORE THAN 7μsec)

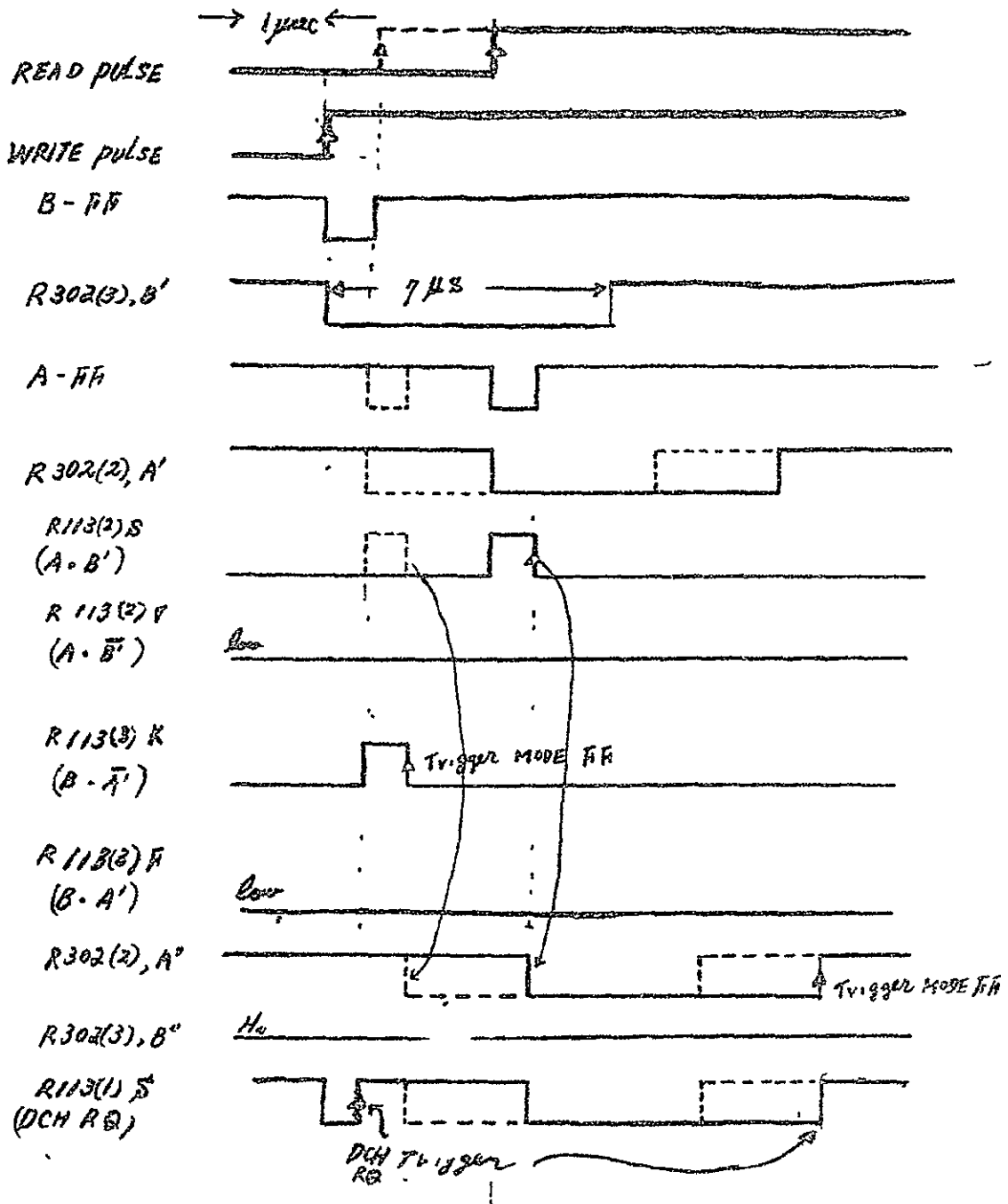
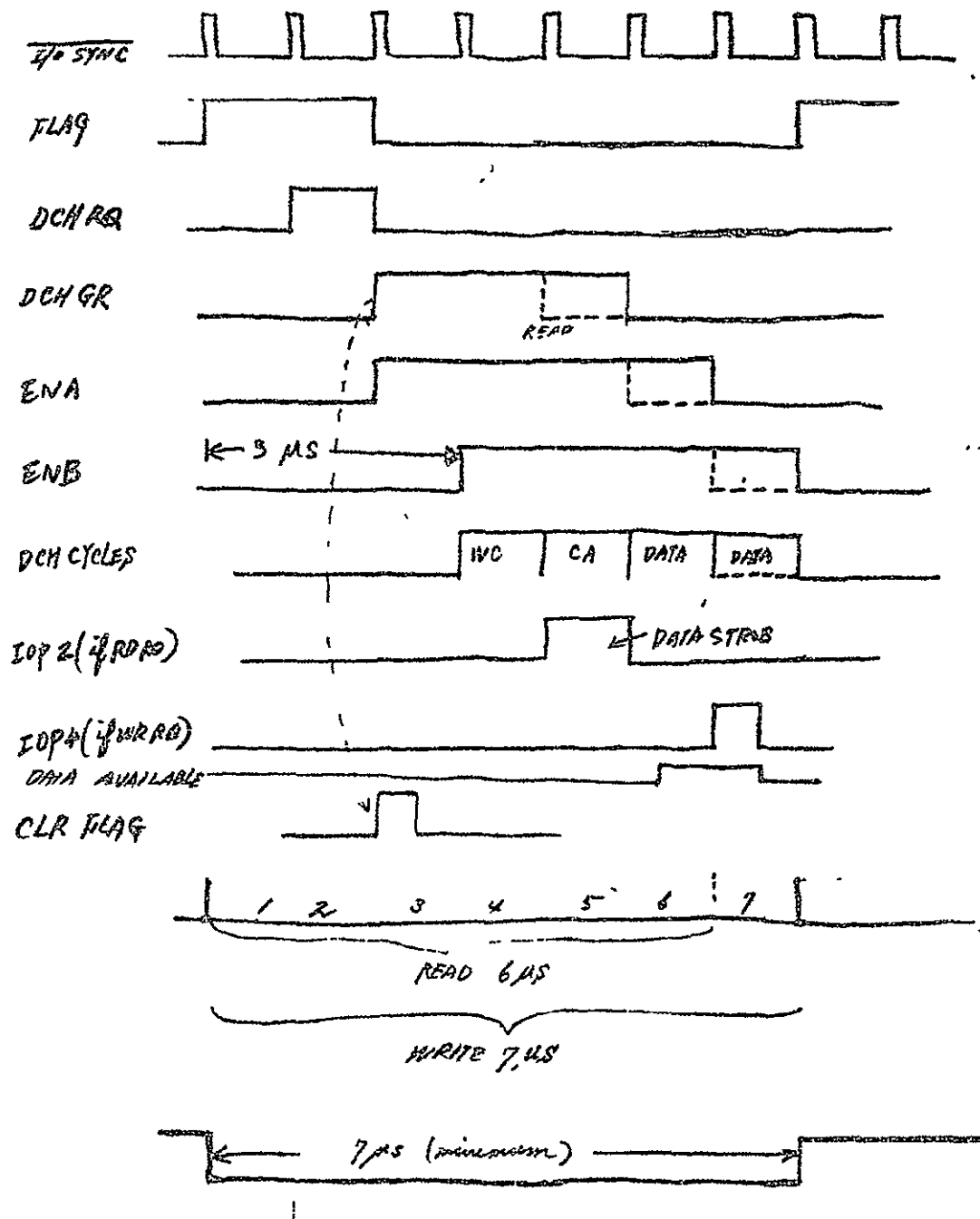
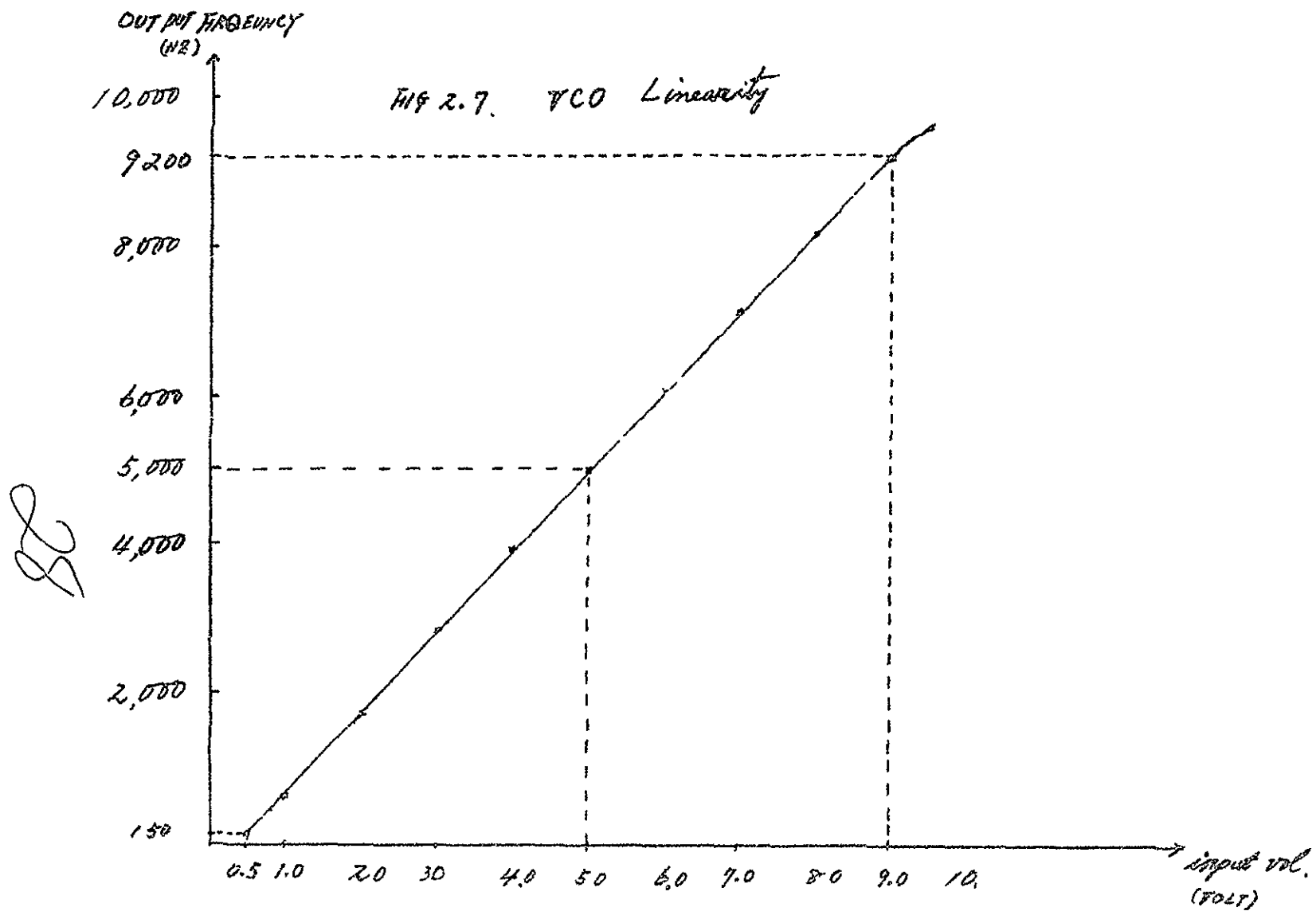
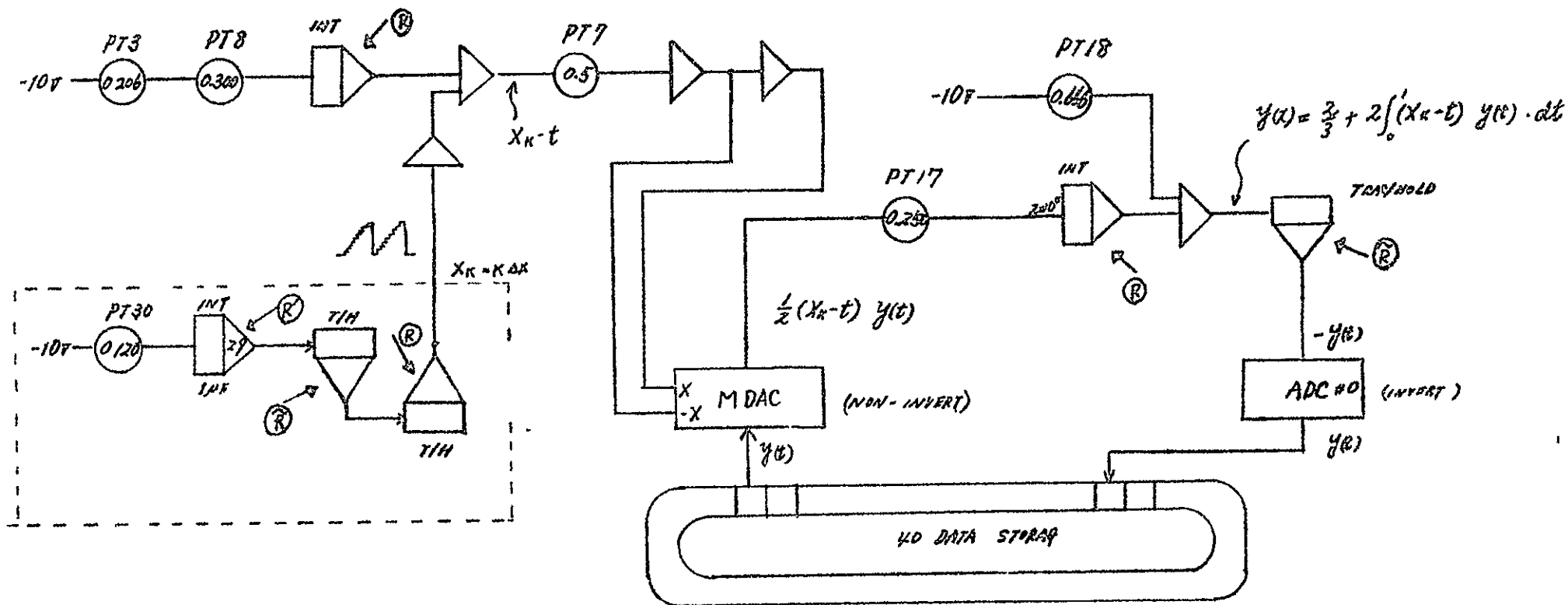


FIG 2.5 Minimum pulse interval between RD pulse and WR pulse.







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A/C RATE	1000 / SEC
T	800 μ S
t _i	970 μ S
n	40 μ S
N	50 μ S
Repeat SW	ON

FIG 3.1 Hybrid computer solution of an integral equation, using time delay

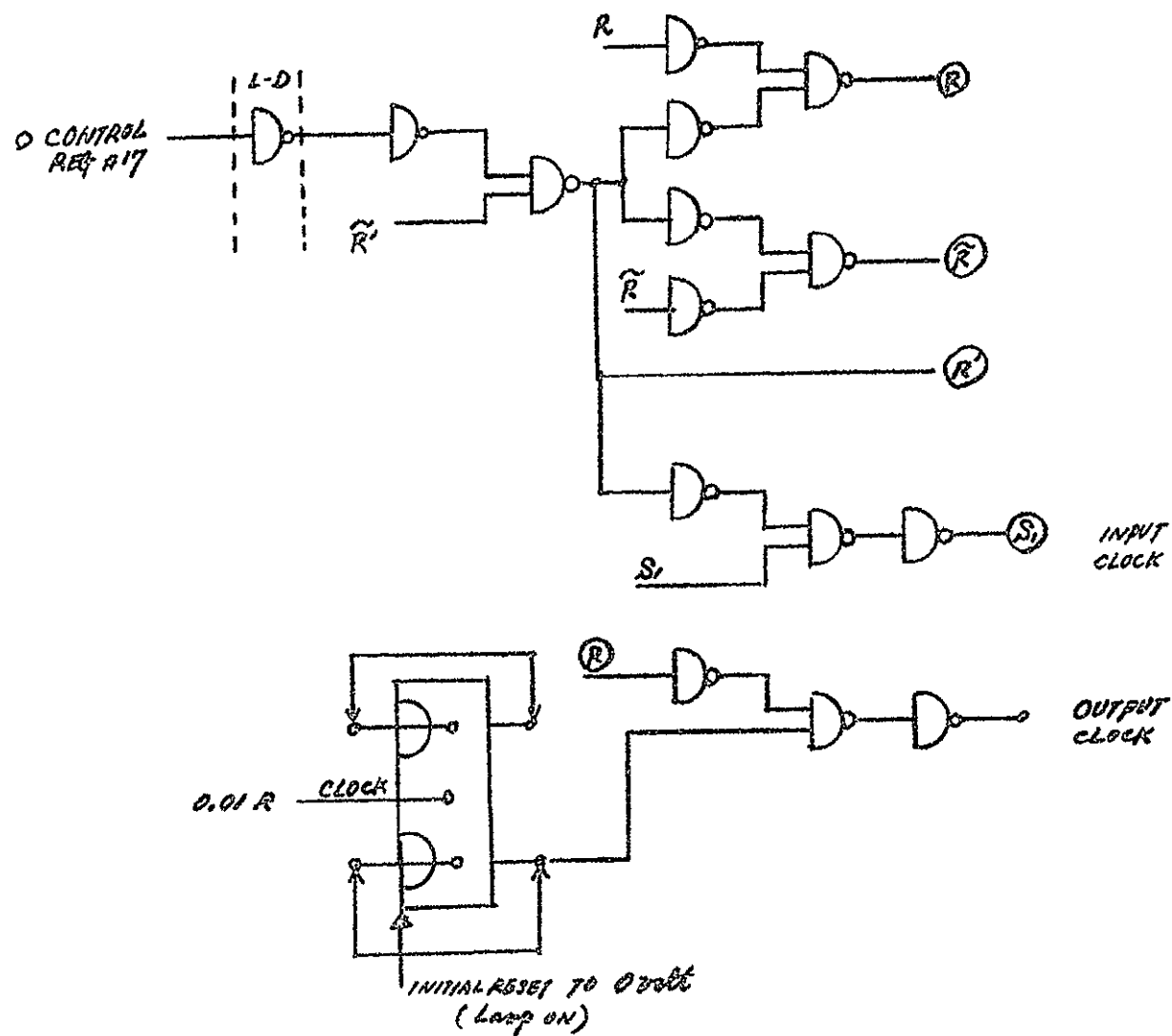


Fig. 3.7 LOGIC DIAGRAM OF TIMING PULSE FOR INTEGRAL EQUATION

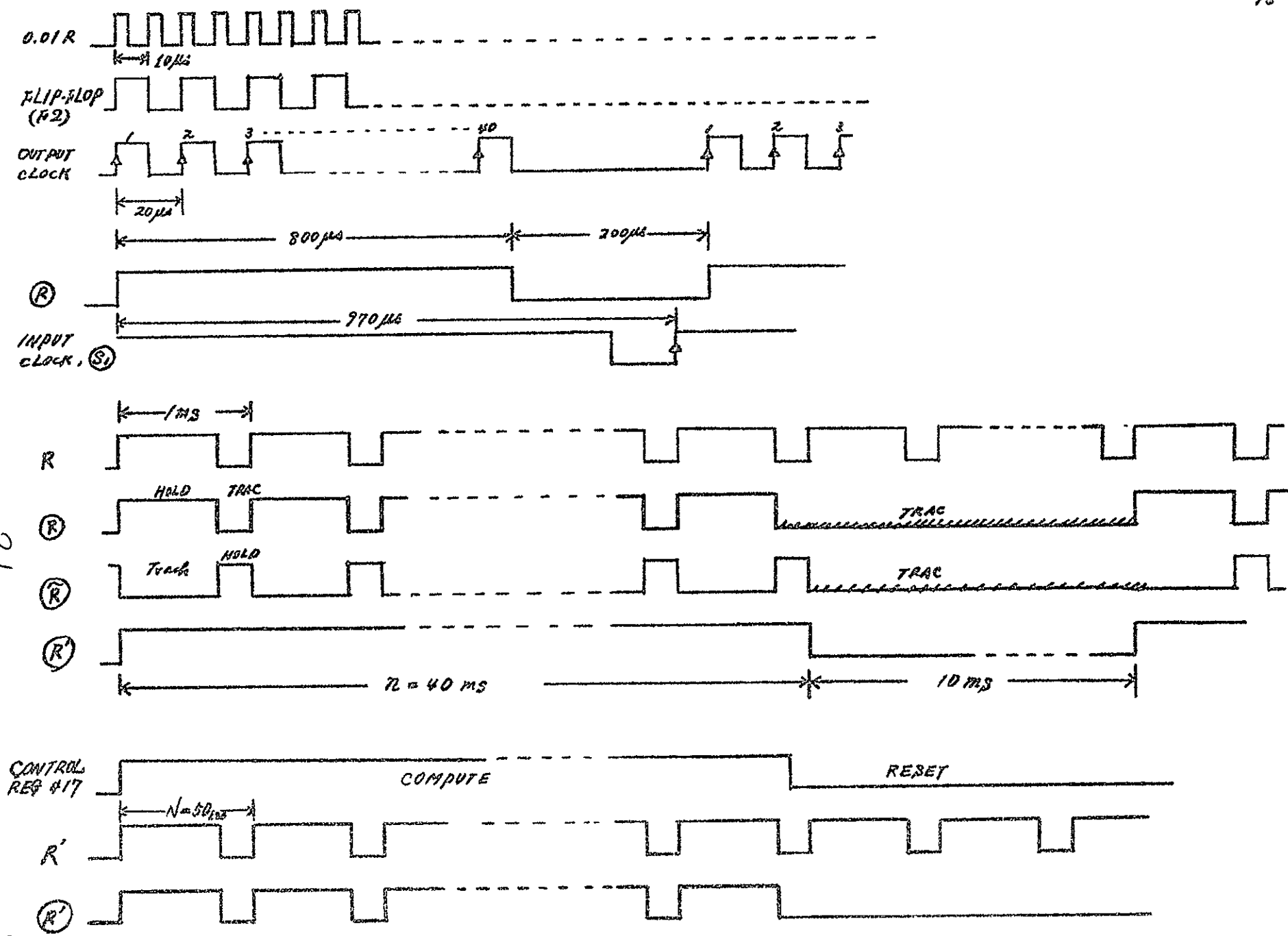
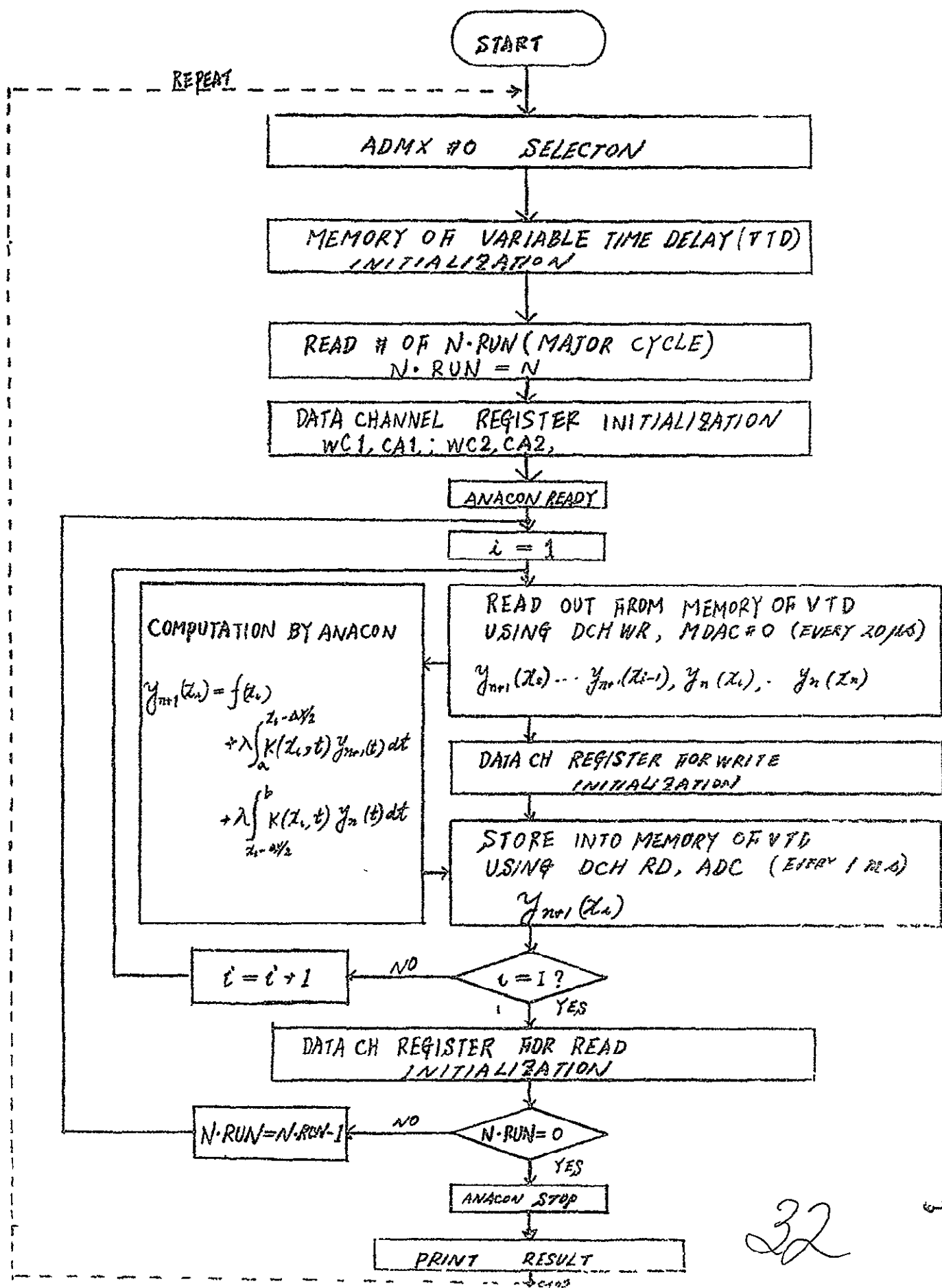
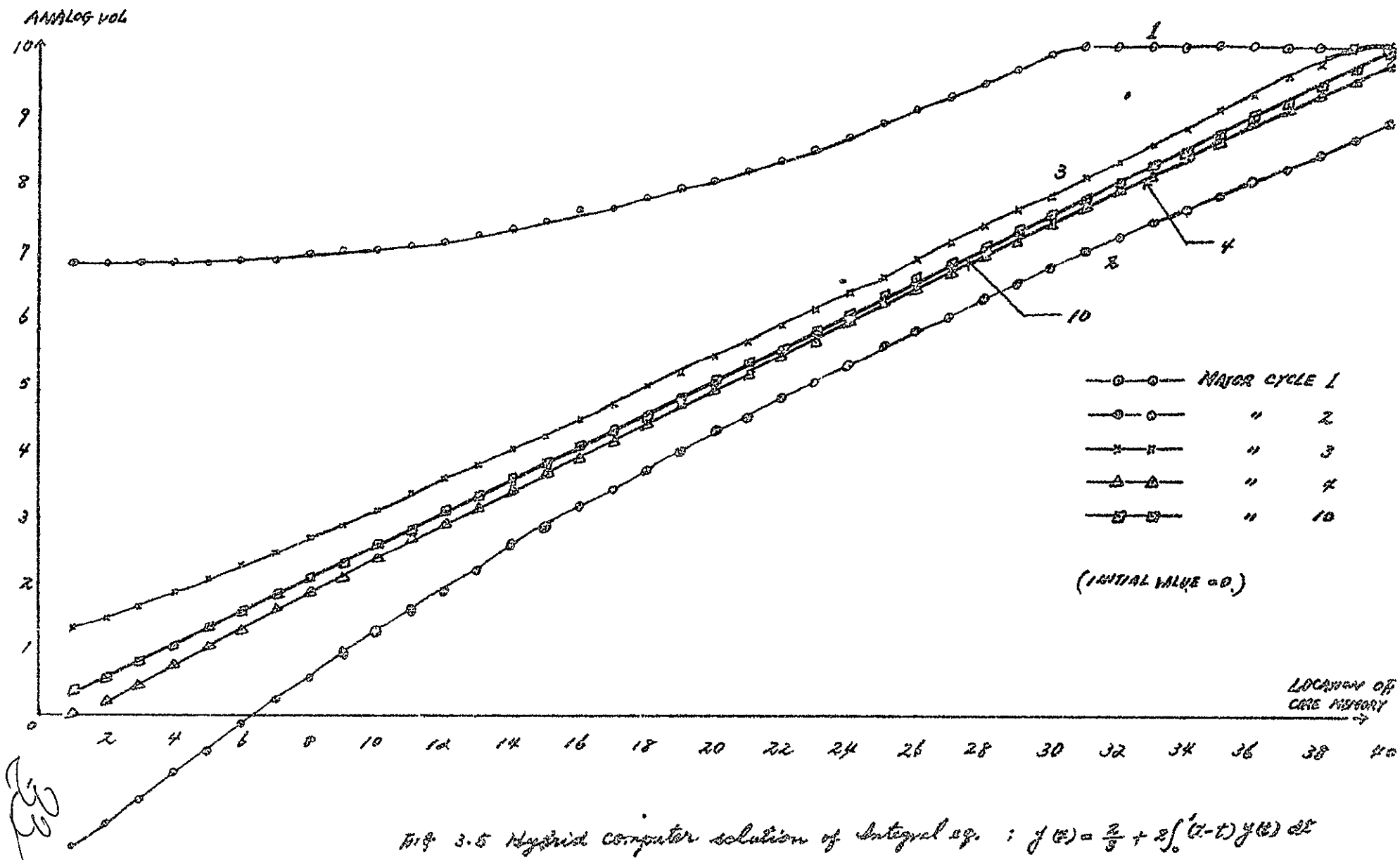


FIG 3-3 TIMING CHART FOR SOLVING INTEGRAL EQUATION

FIG 3 4. HYBRID COMPUTATION FLOW DIAGRAM OF INTEGRAL EQUATION



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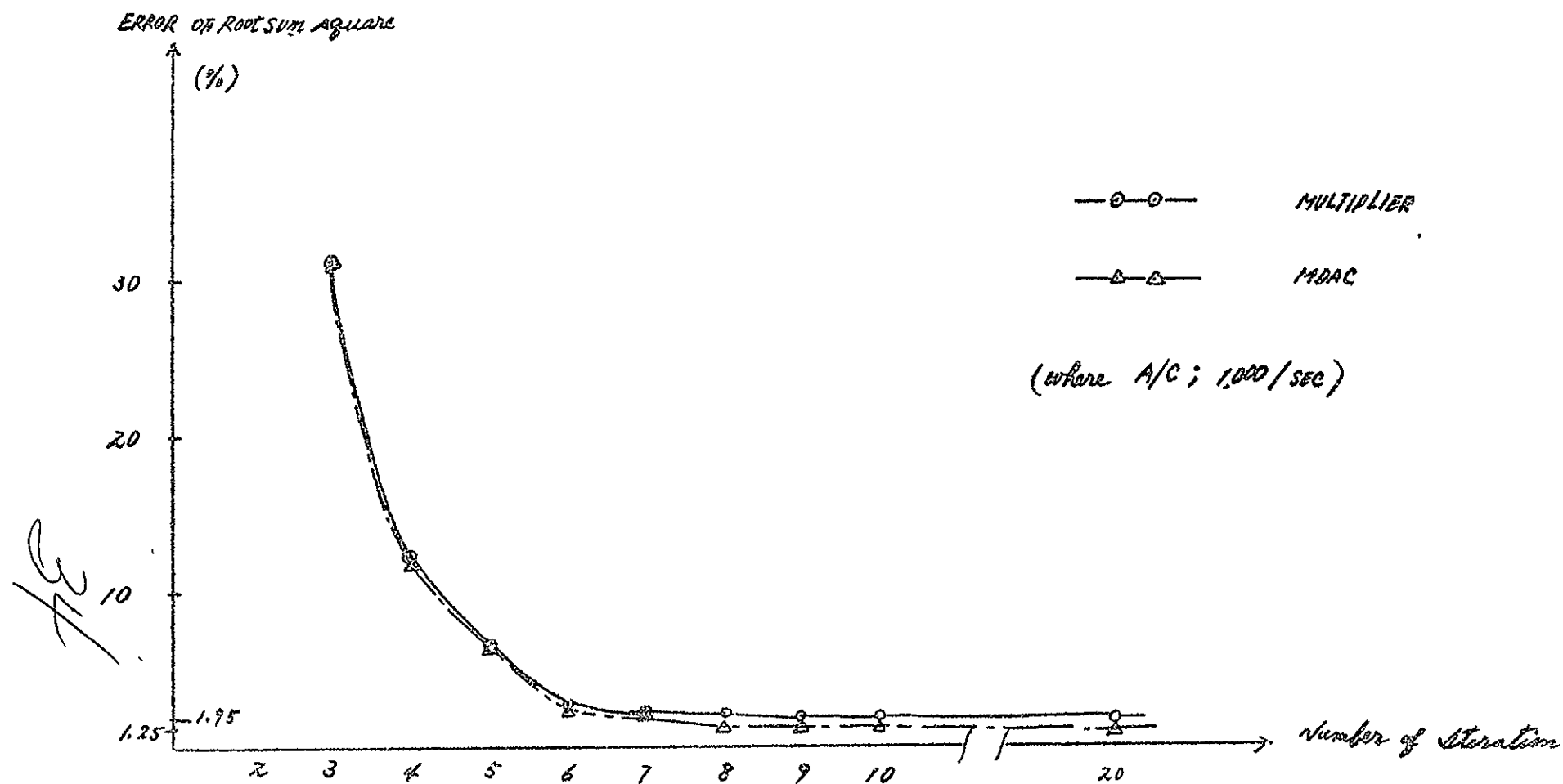


FIG 3-6 CONVERGENCE CHARACTERISTIC

/NAKA NOV28,1969
 /TITLE VARIABLE TIME DELAYS(VTD)
 / USING DATA CHANNEL INTERFACE
 /EXAMPL: SOLUTION OF INTEGRAL EQUATION
 / USING VTD
 /

.GLOBL OUTPUT,INPUT

/SELECTION OF ADMX #0

00000 R 750000 A
 00001 R 705024 A

START CLA /LOAD AC WITH ZERO
 705024 /SELECT ADMX #00

/MEMORY INITIALIZATION

00002 R 200017 R
 00003 R 040022 R
 00004 R 200020 R
 00005 R 060151 R
 00006 R 200016 R
 00007 R 060010 A
 00010 R 440022 R
 00011 R 600007 R

LAC WC
 DAC N.RUN
 LAC CA1
 DAC* (10 /LOC.10=CA1
 LAC IDATA /LOAD AC WITH ZERO
 CLEAR DAC* 10 /SET IDATA
 ISZ N.RUN /RECORD # OF MEMORY
 /TO BE ERASED
 JMP CLEAR

/READ # OF N.RUN(MAJOR CYCLE

00012 R 120147 E
 00013 R 600015 R
 00014 R 000023 R
 00015 R 600025 R

JMS* INPUT
 JMP +2
 CONST0
 JMP MAIN0 /GO TO MAIN

/TABLE OF CONSTANT

00016 R 000000 A
 00017 R 777730 A
 00020 R 000076 R
 00021 R 000076 R
 00022 R 000000 A
 00023 R 000000 A
 00024 R 000001 A

IDATA 000000 /INITIAL DATA
 WC 777730 /# OF WORDS TO BE
 /TRANSFERD(2,COMPL)
 CA1 A-1 /STARTING ADDR FOR
 /INPUT
 CA2 A-1 /START ADDR FOR OUT
 N.RUN 0 /WORKING STRAGE FOR
 /# OF N.RUN
 CONST0 0 /# OF N.RUN SET BY
 /INPUT ROUTIN
 CONST1 000001 /USED BY CTRL REG

00025 R 200017 R
 00026 R 060152 R
 00027 R 060153 R
 00030 R 200020 R
 00031 R 060154 R
 00032 R 200021 R
 00033 R 060155 R
 00034 R 200023 R
 00035 R 040022 R
 00036 R 200024 R
 00037 R 705024 A
 00040 R 740000 A

MAIN0 LAC WC /DCH REGISTER
 DAC* (22 /INITIALIZATION
 DAC* (32 /ROUTIN
 LAC CA1
 DAC* (33
 LAC CA2
 DAC* (23
 LAC CONST0
 DAC N.RUN /# OF MAJOR CYCLE
 LAC CONST1
 ACRL /LOAD CONTRL REG 1
 /
 MAIN1 NOP /DATA TRANSFER

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```

00041 R 740000 A NOP /VIA DATA CHANNEL
00042 R 220152 R LAC* (22 /DCH IN REG WC2
00043 R 740200 A SZL /IS ZERO?
00044 R 600046 R JMP .+2
00045 R 600057 R JMP SR2 /GO TO WC2 SERVICE
/ROUTIN
00046 R 220153 R MAIN2 LAC* (32 /DCH OUT REG WC1
00047 R 740200 A SZL /IS ZERO?
00050 R 600040 R JMP MAIN1 /RETURN TO MAIN
00051 R 600052 R JMP SR1 /GO TO WC1 SERVICE
/ROUTIN
/
/
00052 R 200017 R SRI LAC WC /DCH OUT REG WC1,CA
00053 R 060153 R DAC* (32 /1 INITI ROUTIN
00054 R 200020 R LAC CA1
00055 R 060154 R DAC* (33
00056 R 600040 R JMP MAIN1 /RETURN TO MAIN
/
00057 R 200017 R SR2 LAC WC /DCH IN REG WC2,CA
00060 R 060152 R DAC* (22 /2 INITI ROUTIN
00061 R 200021 R LAC CA2
00062 R 060155 R DAC* (23
00063 R 440022 R ISZ N.RUN /RECORD # OF MJORE
/CYCLE
00064 R 600046 R JMP MAIN2 /RETURN TO MAIN
00065 R 750000 A CLA /LOAD AC WITH ZEROS
00066 R 705204 A ACRL /TURN CTRL REG OFF
/TYPE OUT COMPUTATION RESULT USING F4
00067 R 120150 E JMS* OUTPUT
00070 R 600072 R JMP .+2
00071 R 000076 R DATA
00072 R 600000 R JMP START
/ARRAY DESCRIPTOR BLOCK
00073 R 000050 A 000050 /40(DCMAL) OF WORDS
00074 R 000000 A 000000 /0 FOR 1-D ARRAY
00075 R 000000 A 000000 /0 FOR 1-D ARRAY
00076 R 000077 R DATA A /ADDR OF 1ST DATA
00077 R A A .BLOCK 50 /40 DATA WORDS
. END START
00147 R 000147 E *ETV
00150 R 000150 E *ETV
00151 R 000010 A *LIT
00152 R 000022 A *LIT
00153 R 000032 A *LIT
00154 R 000033 A *LIT
00155 R 000023 A *LIT

```

NO ERROR LINES

MACRO UA44

>^C

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C NAKAI DEC.3, 1969

C PRINT 40 DAT0

C

SUBROUTINE OUTPUT(K)

DIMENSION K(40), XK(40)

WRITE(5,100)

C CONVERSION INTO ANALOG-VOLTAGE

C 2.EXP(17)-1=131071

DO 10 I=1,40

10 XK(I)=FLOAT(K(I))/13107.1

WRITE(5,101) (I,XK(I),I=1,40)

C COMPUTATION OF ROOT SUM SQUARE ERROR

C

SUM=0

DO 20 I=1,40

20 SUM=SUM+(10./40.*FLOAT(I)

1 -XK(I))**2

C ROOT SUM SQUARE ERROR IN PERCENT

ERROR=10.*SQRT(SUM)

WRITE(5,102) ERROR

RETURN

100 FORMAT(1X,*DATA IN MEMORY*)

101 FORMAT(1H,15,5X,F10.3)

102 FORMAT(1X,*ERROR OF ROOT SUM SQUA

1RE=*,F10.4,*Z*)

END

FORTRAN 4 UA5A

>B, L_NAKA2

END PASS1

C NAKA2 DEC.3, 1969

C READ A NUMBER OF MAJOR CYCLE

C

SUBROUTINE INPUT(N)

WRITE(5,200)

READ(4,201) N

RETURN

200 FORMAT(1X,*READ # OF MAJOR CYCLE

1 IN I7*)

201 FORMAT(I7)

END

FORTRAN 4 UA5A

>

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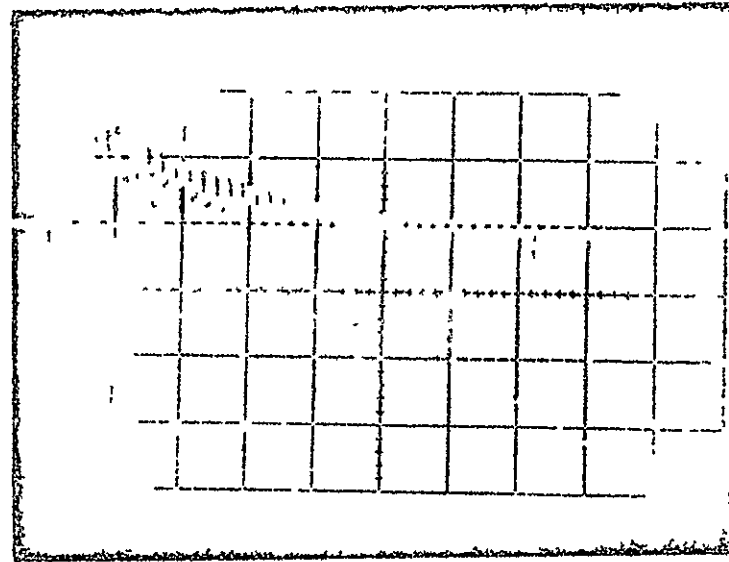


FIG 3.8 OUTPUT WAVE FORM OF TRAC/HOLD AMP. (-y(t))
(5 msec/cm, 2 Volt/cm)

NOT REPRODUCIBLE

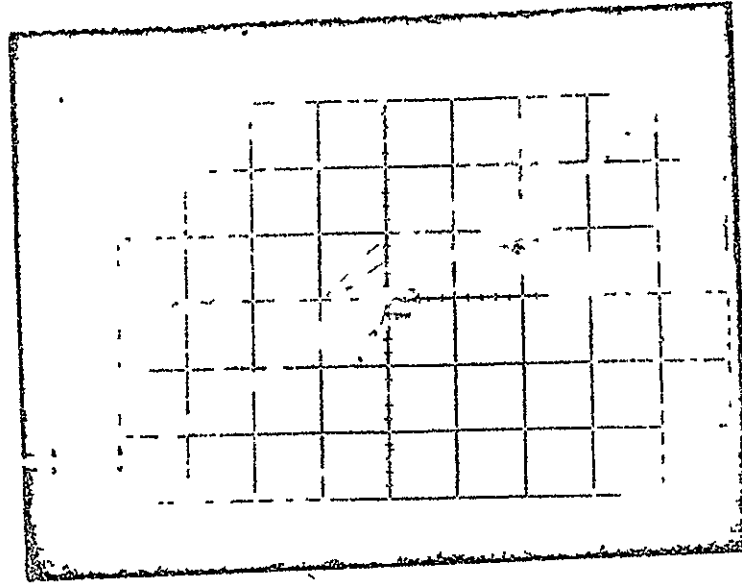


Fig 3.7

Solution; $y(x) = x.$

(5 m sec/cm, 2 Volt/cm.)

NOT REPRODUCIBLE