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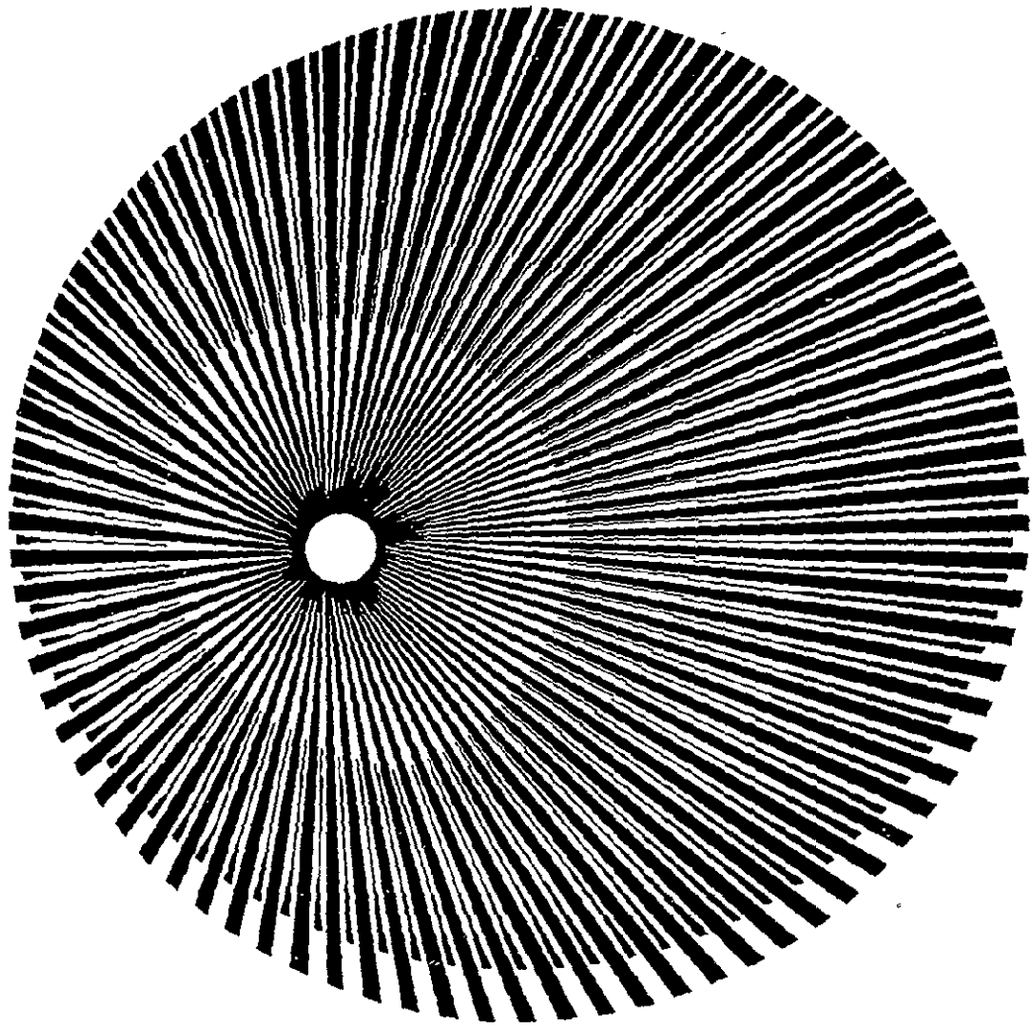

FINAL REPORT
FINE SUN SENSOR - SIGNAL CONDITIONER
CONTRACT NO. NAS8-30033

Approved by: Larry L Brown for
Jim Thomas
Section Manager

Approved by: Don Holcomb
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Prepared by: Ken Eme
Ken Eme
Project Leader

FINAL REPORT
FINE SUN SENSOR - SIGNAL CONDITIONER
CONTRACT NO. NAS8-30033

Prepared for
George C. Marshall Space Flight Center
Marshall Space Flight Center, Alabama
March 18, 1970

MOTOROLA
Government Electronics Division
8201 E McDOWELL ROAD SCOTTSDALE ARIZ 85252

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SECTION I

INTRODUCTION AND FUNCTIONAL DESCRIPTION

The Fine Sun Sensor-Signal Conditioner (FSS-SC) was developed by the Government Electronics Division of Motorola, Inc., Scottsdale, Arizona, for the Marshall Space Flight Center in Huntsville, Alabama, under Contract NAS8-30033. The contract was awarded June 27, 1968 and design efforts were initiated immediately on the logic, power converter, and packaging of the system. The FSS-SC is a portion of the experiment pointing electronics of the Apollo Telescope Mount for the Apollo Applications Program. Its purpose is to furnish a remote indication of positioning of the Fine Sun Sensor to the spacecraft computer. The Signal Conditioner receives optically generated wedge offset signals from the Fine Sun Sensor. These signals are pitch and yaw axis positioning information along with a "zero pulse" input which initializes a Signal Conditioner Counter in synchronism with the Fine Sun Sensor. Since pitch and yaw circuitry is identical, the following functional description is representati of both channels.

Two sine-cosine related wedge input pulse trains are received from the Fine Sun Sensor. Each pulse transition equa 1.25 arc seconds of position change. Input signal characteristics are shown below.

Source Impedance	100 ohms
Load Impedance	1000 ohms min.
High Level (No Load)	5 ± 1.5 V
Low Level (No Load)	-3 ± 1.5 V
Noise	300 mv p-p Max.

Input buffer circuitry consists of a monolithic operational amplifier and its associated discrete components. Positive feedback was selected to provide input hysteresis for noise immunity. A positive going transition is detected at approximately +1 volt and a negative going transition at approximate -1 volt. Output of the buffer amplifier is the 0.0 VDC and +5.0 VDC logic levels required by logic circuitry in the Signal Conditioner. By sensing the input signals for the leading pulse train the up-down logic determines if the counte should be incremented or decremented. The transitions are then counted by the up-down counter and set into the shift register for storage. Position data is available to the computer on demand.

A worst Case Analysis of the logic design is included as Appendix A of this report. To attain the desired reliability the FSS-SC includes a standby redundant sub-system. Selection is by astronaut control via an external switch. With redundancy the system contains four identical logic assemblies, plus normal and redundant power supplies. Figure #3 on page 1 is a block diagram of the system.

The power supply for the signal conditioner is a blocking oscillator dc to dc converter configuration. This type of supply has been used by Motorola on several spacecraft systems. It results in a small and highly efficient converter for applications requiring the low voltage, high current outputs needed for integrated circuits. The Signal Conditioner power converter supplies a 1.2 watt load at 60% efficiency. Regulation is better than 5% under all combinations of line voltage, load and temperature. The blocking oscillator supplies the charging current to an L-C filter for each output voltage. Feedback from an isolated winding on the transformer controls the oscillator duty cycle thus regulating the output voltage. The L-C filters function as energy storage elements and supply system power during the oscillator off-time. Nominal operating frequency of the oscillator is 100 KHz. The worst case analysis of the power converter is included as Appendix B of this report.

SECTION II

MECHANICAL CONFIGURATION

The packaging concept utilized on this program is similar to that implemented successfully on earlier space programs at Motorola.

The power supply is fabricated on an "H Frame" chassis machined from 6061 aluminum alloy stock. The normal supply is on one side of the "H Frame" and an identical redundant supply is on the opposite side. Most discrete parts are mounted on PC boards. The power transistors and power transformers for the supplies are mounted to the wall of the chassis for efficient heat-transfer. All external electrical connections to the power supplies are made via feed-thru capacitors and primary power is supplied through RFI filters.

Pitch and yaw axis logic circuitry is identical. The standby redundancy results in four identical logic module subassemblies. The logic subassemblies are of sandwich construction consisting of two double sided printed circuit boards to which flat pack type integrated circuits and necessary discrete components are mounted. The two boards of a sandwich are assembled with components facing inward toward a heat shunt plate. External electrical connections to the sandwich are made via Amphenol PC board connectors. Sandwiches are potted with Sylgard-182 and spacers are used

at tie-bolt locations in the corners to maintain proper spacing between boards and the heat shunt plate.

Two logic sandwich subassemblies are secured to each side of the power supply by four tie-bolts. This assembly is then secured to the top case cover by screws into each of the sandwich heat shunt plates as well as into the power supply chassis. Figure #1 shows the assembly at this level. Interconnections within the signal conditioner between the logic module subassemblies, the power supplies, and the external connectors are made with No. 24 AWG silver alloy wire. Primary power and normal/redundant control wires to the external connectors are shielded.

All external connections to the signal conditioner are made through four crimp type bayonet connectors. The two piece external housing is made of 6061 aluminum alloy stock and is secured by screws at the horizontal center line. Internal subassemblies are mounted to the top of the housing by screws to insure maximum heat transfer through this surface. Reinforcing ribs on the top surface serve to improve both thermal and vibration characteristics. The overall mechanical configuration of the completed assembly is as follows·

Length.....Not more than 6.53 inches

Width.....Not more than 6.53 inches

Height.....Not more than 4.85 inches

Weight.....Not more than 7.5 lbs. (7.2 lbs. typical)

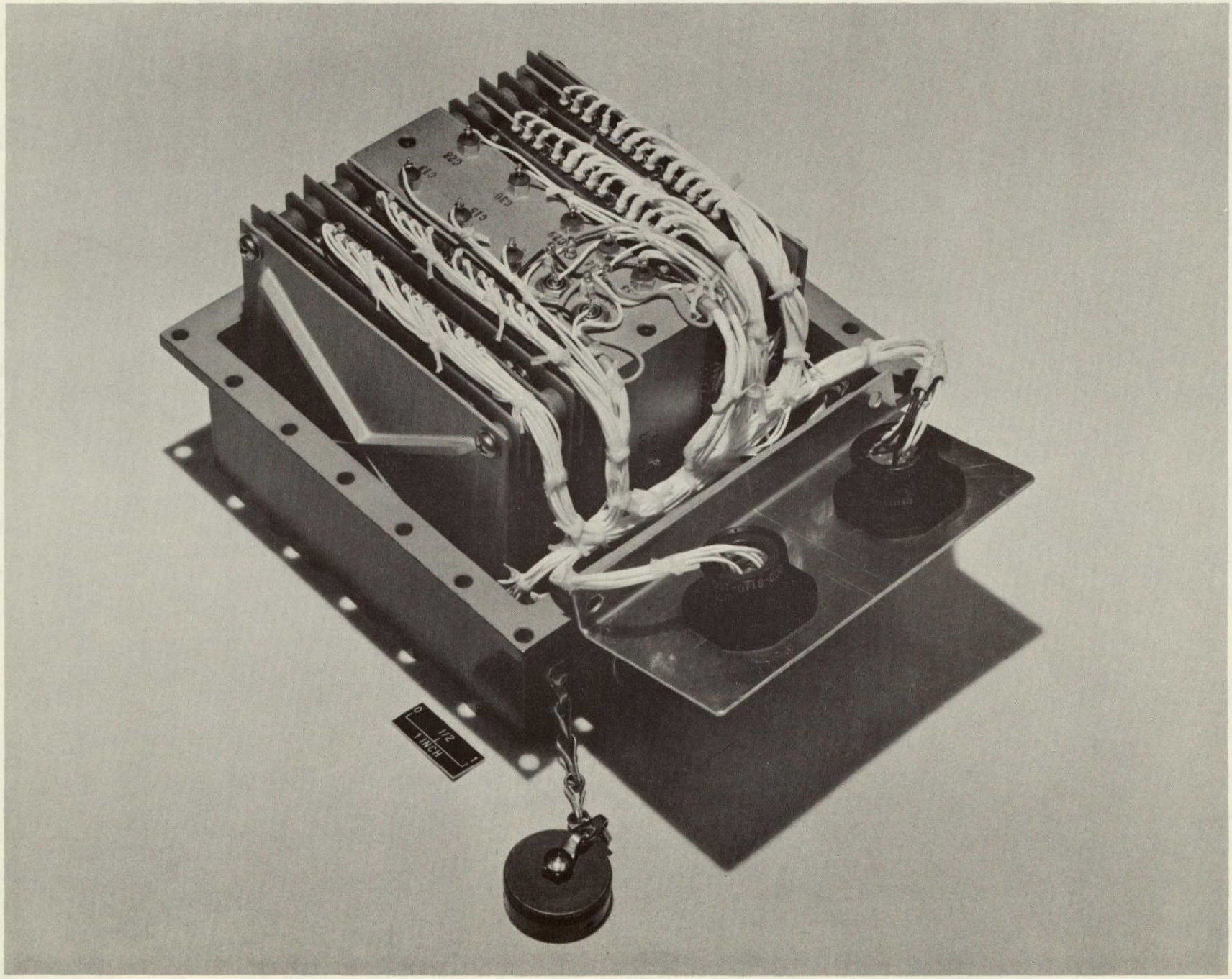

Figure #1. Logic/Power Supply Subassembly

Figure #2 shows the final configuration of the Fine Sun Sensor Signal Conditioner.

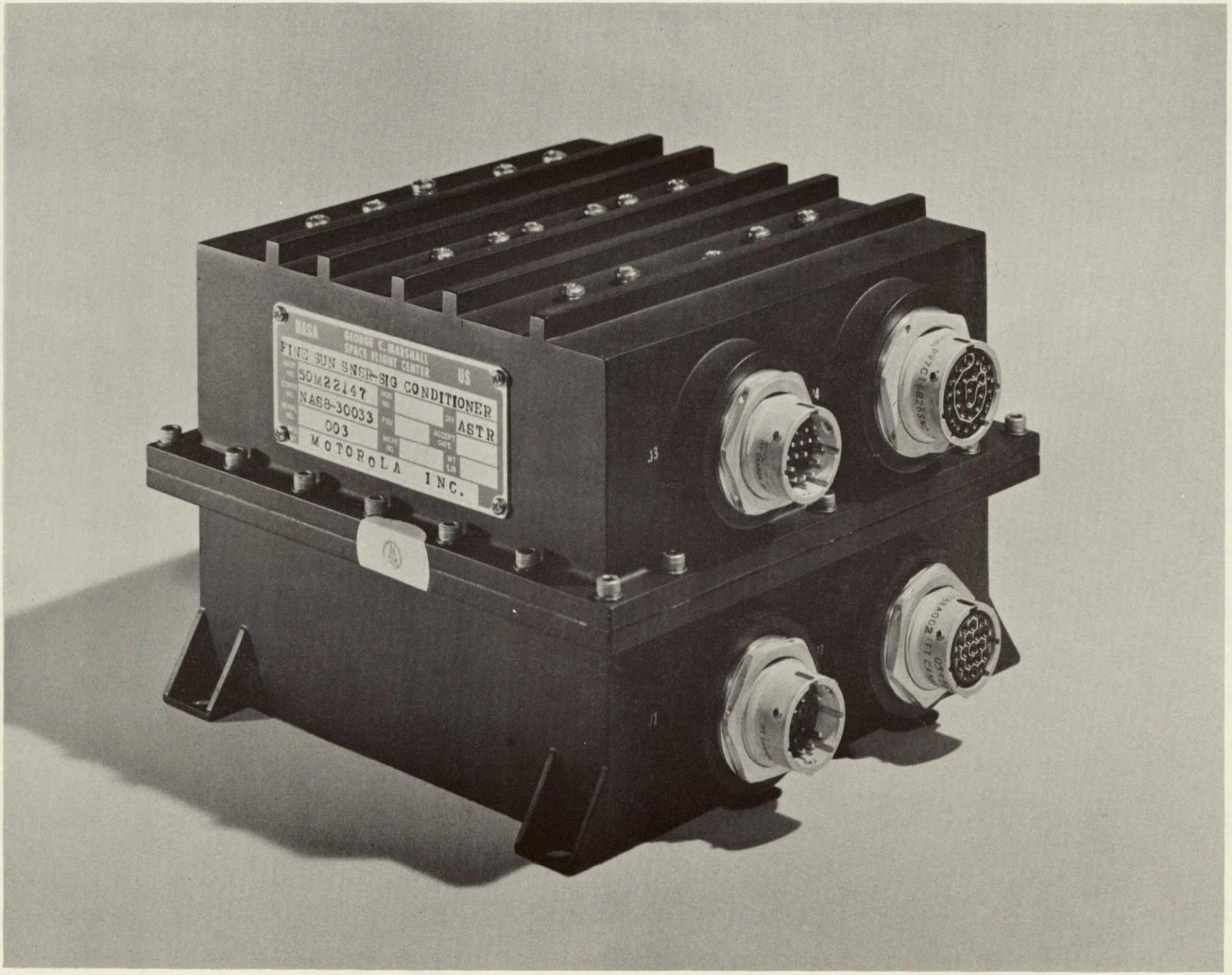

Figure #2. Fine Sun Sensor - Signal Conditioner

SECTION III

PRINCIPAL FABRICATION PROBLEMS

Early in the fabrication effort extensive testing was performed regarding component mounting to printed circuit boards. The tests were patterned from procedures recommended by Ray Van Orden in NASA TMX-53731. Printed circuit boards to simulate those used in the power supplies were used for this test. Appendix C contains a copy of the procedures and results of the test as conducted by the Production Engineering Department. Components on printed boards of the flight system power supplies were mounted according to the recommendations outlined in this report.

Operational problems were experienced at MSFC on the Prototype Signal Conditioner due to the method of switching redundant Sun Sensors in the spacecraft. As a result Motorola was directed to change shield terminations of interface signals. Additional interface noise problems on the prototype system resulted in a customer directive to add capacitors between signal and normal grounds of the power supplies.

During fabrication of the flight systems MSFC discovered that the interface connectors they supplied Motorola did not meet the Apollo Telescope Mount program outgassing requirements. Some fabrication delay was experienced as it was necessary to return these connectors to MSFC for a 72 hour high temperature vacuum bake.

During initial testing of the first flight system noise was found to be triggering the monostable multivibrators used for internal system timing. The problem was resolved by adding V_{cc} decoupling capacitors to driving gates.

A mechanical failure was encountered during vibration Qualification Testing. Bosses used to secure the logic sandwich and power supply subassembly to the lower housing broke loose during this test. A detailed analysis of the problem was performed by the Mechanical Engineering Department. The bosses were removed from the housing as a result of this analysis. See Appendix D for a copy of this report. It is recommended that vibration testing be performed on prototype units in future programs to avoid problems of this type during fabrication of flight hardware.

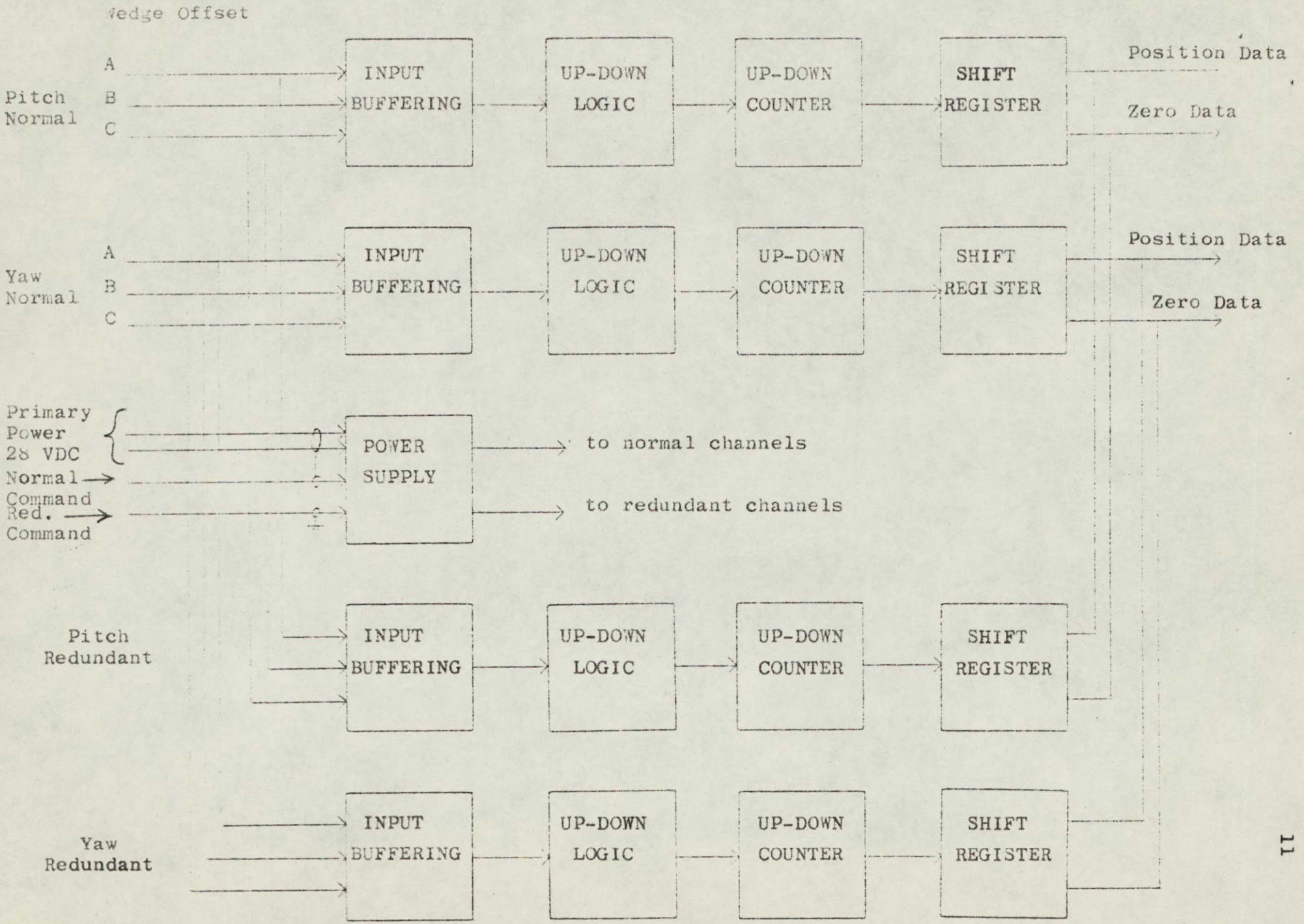

Figure #3. System Block Diagram

APPENDIX A

WORST CASE ANALYSIS OF LOGIC DESIGN

SPACE SYSTEMS LABORATORY

TECHNICAL MEMORANDUM NO. ADS - 23

26 September 1968

Project 3511

ABSTRACT:

This technical memorandum presents a worst case analysis of the logic function portion of the Fine Sun Sensor - Signal Conditioner, (FSS - SC). Included are analyses for all circuits, critical timing functions, logic and error allocation.

"FSS - SC LOGIC FUNCTION WORST CASE ANALYSIS"

By: E. Davis

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1.0 INTRODUCTION

This technical memorandum fulfills the requirement for a worst case analysis of the logical function design of the Fine Sun Sensor Signal Conditioner (FSS-SC). A worst case design analysis of the input buffer circuit is included which covers such items as threshold limits, trigger margins, and maximum signal ratings. Also included in the analysis are an error allocation and definition study of triggering levels on the input signal, an internal timing margin study, and comments on worst case logic design.

2.0 INPUT BUFFER DESIGN ANALYSIS

2.1 Only one discrete component circuit is used in the FSS-SC; specifically, the input buffer circuit. This circuit is used to condition the A,B, and C channel wedge offset input signals for use by the logic in the FSS-SC. The circuit is essentially a linear I/C amplifier in a Schmitt Trigger feedback operating mode.

2.2 The schematic diagram of the input buffer is presented in Figure 1. A summary of the circuit parameters and component variations is presented in Table 1. The input waveform characteristics are shown in Figure 2. The output is required to be compatible with standard TTL circuits; specifically, the logic "1" level shall be greater than +2.4 volts and the logic "0" level shall be in the range -0.7 to +0.7 volts.

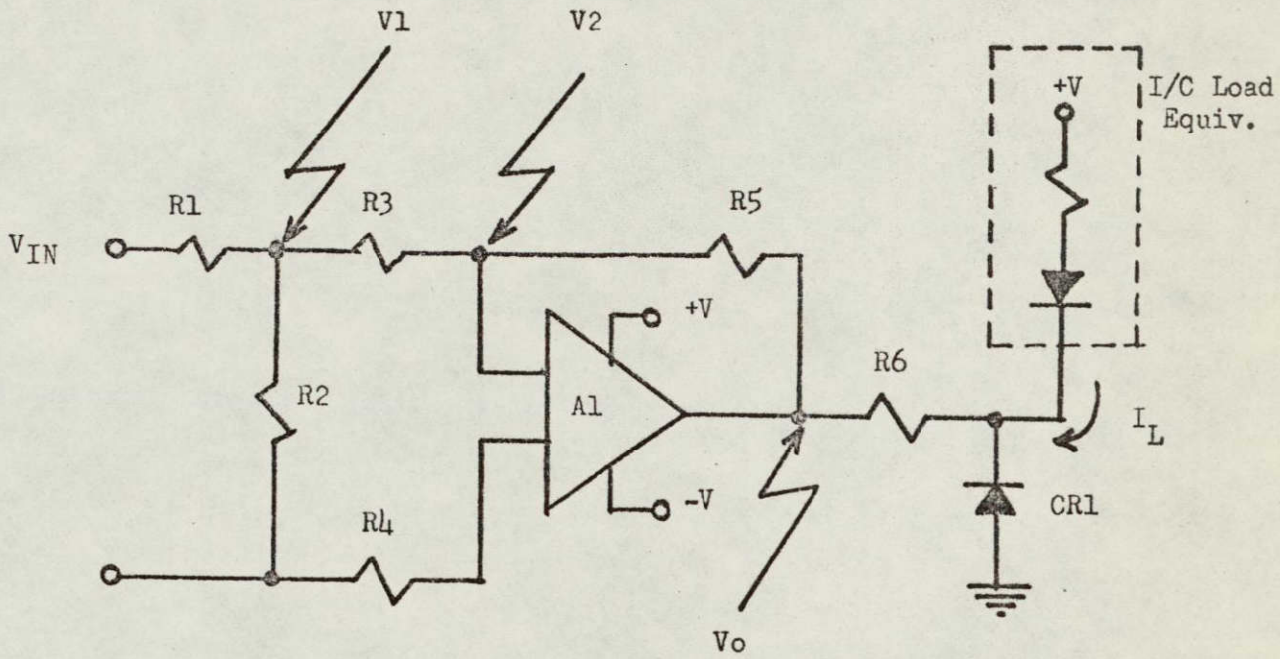

Figure 1: INPUT BUFFER CIRCUIT.

Parameter/ Component	Nominal	Maximum	Minimum
V_{IN} (High)	+5.0 volts	+6.5 volts	+4.5 volts
V_{IN} (Low)	-3.0 volts	-4.5 volts	-1.5 volts
$+V_{CC}$	+5.0 volts	+5.3 volts	+4.7 volts
$-V_{CC}$	-5.0 volts	-5.3 volts	-4.7 volts
V_O* (High)	+4.4 volts	+4.8 volts	+4.0 volts
V_O* (Low)	-3.6 volts	-4.0 volts	-3.2 volts
R_1**	383 ohms	398 ohms	368 ohms
R_2**	1000 ohms	1040 ohms	960 ohms
R3, R4**	28.7K ohms	29.9K ohms	27.5K ohms
R5**	162K ohms	169K ohms	155K ohms
R6**	2370 ohms	2465 ohms	2275 ohms
A_{VOL} of A1	105 db	108 db	92 db
I_N of A1	---	360 na	50 na
V_{IN} of A1	---	$\pm V_{CC}$	---

*Includes ±0.1 volt parametric variation and ±0.3 volt power supply variation.

**Including temperature effect, life, loading and initial offset, the total variation is ±4.0%.

TABLE I: CIRCUIT PARAMETER AND COMPONENT VARIATION DATA

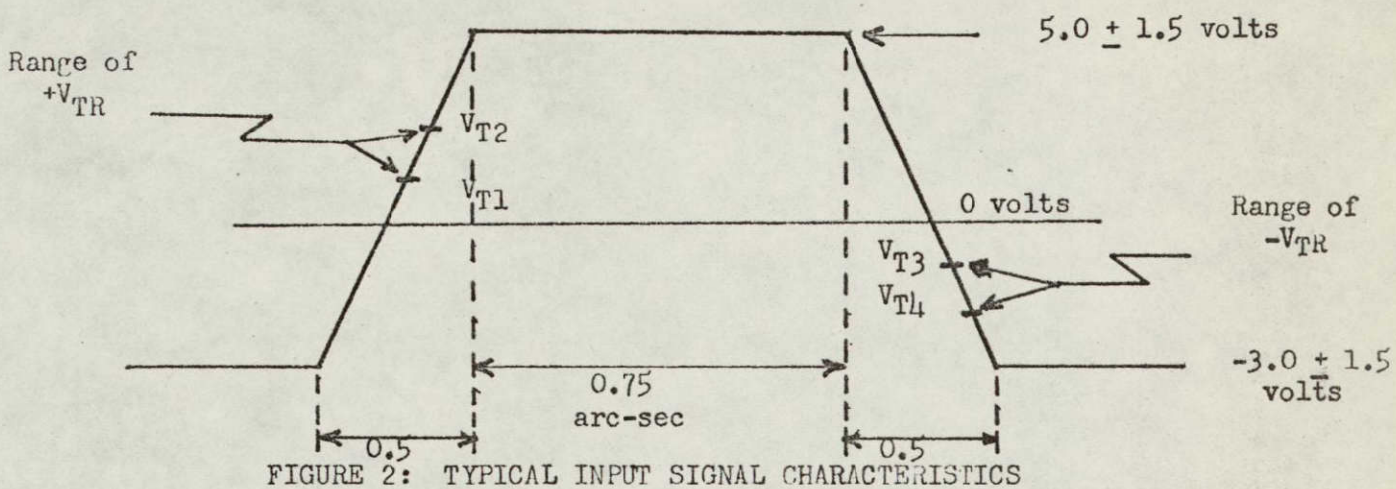

FIGURE 2: TYPICAL INPUT SIGNAL CHARACTERISTICS SHOWING TRIGGER POINTS (V_{TR})

2.3 The prime consideration in the verification of the performance of the input buffer circuit is to establish the worst case threshold point and the resulting margin in the trigger mechanism.

From the schematic, it is noted that V_1 may be expressed as:

$$V_1 = V_{IN} \left(R2/(R2 + R1) \right),$$

neglecting any contribution from V_2 through R3 (max. error of 0.5%). The threshold voltage of the amplifier at point V1 will be considered the circuit threshold, V_{CT}. This is determined by the voltage, V2, threshold that causes a change of state in the output level; specifically, $V_2 = -Vo/A_{VOL} \approx 4.ov/50,000 \angle \pm 1$ mv.

2.3.1 Maximum and minimum values that may occur at V1 are easily determined from the expressions:

$$\underline{V_I} = \underline{V_{IN}} \left[\frac{\underline{R2}}{\underline{R2} + \overline{R1}} \right] \quad \text{and}$$

$$\overline{V_I} = \overline{V_{IN}} \left[\frac{\overline{R2}}{\overline{R2} + \underline{R1}} \right] .$$

Substitution of the appropriate values from Table 1 yields the following:

Maximum Vl = +4.80 volts and $|-3.32|$ volts

Minimum Vl = +2.48 volts and $|-1.06|$ volts

for positive and negative inputs.

2.3.2 If the circuit of Figure 3 is considered, it is noted that maximum and minimum values of V_{CT} may be determined from the expression:

$$V_{CT} = V_1 \text{ (at threshold)} = \left[\frac{V_o}{R5} - I_{IN} \right] R3.$$

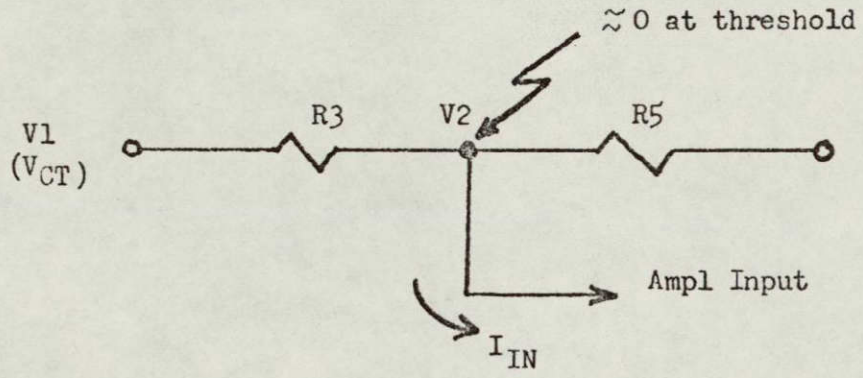

FIGURE 3: AMPLIFIER DRIVE INPUT CIRCUIT.

Worst case values for V_{CT} are expressed as:

$$\overline{V_{CT}} = \left[\frac{\overline{V_o}}{\underline{R5}} - \underline{I_{IN}} \right] \overline{R3} \quad \text{and}$$

$$\underline{V_{CT}} = \left[\frac{\underline{V_o}}{\overline{R5}} - \overline{I_{IN}} \right] \underline{R3} \quad .$$

Substitution of the appropriate values from Table 1 into the above expression yields the following:

Maximum V_{CT} = +0.925 and -0.772 volts

and Minimum V_{CT} = +0.640 and -0.586 volts,

for positive and negative threshold.

2.3.3 The input threshold margin is defined as:

$$\underline{V_1} - \overline{V_{CT}} = TM.$$

Using the results of 2.3.1 and 2.3.2, it is noted that the following threshold margin exists:

1.55 volts for positive threshold

and 0.29 volts for negative threshold.

2.4 A specified maximum input level of $\pm V_{CC}$ exists for the operational amplifier used in the input buffer circuit, where V_{CC} refers to the power supply voltage. In section 2.3.1, it is noted that $\overline{V1}$ is 4.8 volts and represents the only questionable input level condition.

Referring to Figure 3, the maximum value of V2 for $\overline{V1}$ = 4.8 volts is determined using $\overline{R5}$, $\underline{R3}$, $\underline{I_{IN}}$ and $\underline{Vo}$. The resulting value of $\overline{V2}$ is found to be +4.68 volts using standard circuit equations and the values of Table 1. Since the specified input voltage limit is +4.7 volts, the extreme worst case condition is below any maximum input rating.

3.0 ERROR ANALYSIS

3.1 A typical representation of an input signal pulse is presented in Figure 2. The 50% point of the slopes of this wave form are defined as to the 1.25 aro-sec incremental point in the FSS-SC input data. Any variation from this point on the waveform to the actual circuit threshold represents an effective error or "jitter" in the precision of the FSS-SC output data number.

This error analysis shall predict initial offset error and error "jitter" under worst case signal and circuit parameter variations.

3.2 In section 2.3.2, the threshold voltage, V_{CT}, was found to vary in the worst case as follows:

Maximum V_{CT} = +0.93 and -0.77 volts,

and Minimum V_{CT} = +0.64 and -0.59 volts.

The corresponding limits for V_{IN} at threshold may be determined by the expressions:

$$\overline{V_{IN}} = \overline{V_{CT}} \left[\frac{\overline{R2} + \underline{R1}}{\underline{R2}} \right] \quad \text{and}$$

$$\underline{V_{IN}} = \underline{V_{CT}} \left[\frac{\underline{R2} + \overline{R1}}{\overline{R2}} \right] .$$

The resulting ranges in V_{IN} at threshold are +0.87 to +1.30 volts and -0.80 to -1.10 volts.

3.3 As noted in Figure 2, the transition time of the input signal is of 0.5 arc-second duration and is assumed linear. The voltage transition varies from 5.0 volts under minimum signal conditions to 11.0 volts under maximum signal conditions, resulting in a slope of 0.1 arc-sec/volt to 0.0454 arc-sec/volts for the signal transition. The error offset may be defined as:

$$\text{Error} = (V_{IN} - V_{50\%}) \text{ (Transition Slope)}$$

at threshold. The nominal incremental point $V_{50\%}$ is 1.0 volts under both signal conditions. For the threshold ranges calculated in section 3.2, the positive edge count error ranges from -0.013 arc-sec to +0.030 arc-sec. Similarly, the negative edge count error ranges from +0.18 arc-sec to +0.21 arc-sec. Note that the worst case error occurs under minimum signal conditions.

3.4 In section 3.3, the positive and negative extremes of the input levels were assumed to track in their variation. If the rather improbable condition should occur in which one level goes to a maximum, and the other to a minimum, the $V_{50\%}$ point will shift by ± 1.5 volts. This represents an additional ± 0.15 arc-sec of worst case error that must be appropriately included in the results of section 3.3

4.0 INTERNAL TIMING STUDY

Monostable multivibrators are used in two critical functions in the FSS-SC. One application is to generate a clock delay that allows a setup time in the up-down logic prior to the counter clock transition to a positive (logic "1") level. The second application is in the masking of the interrogate enable signal that blocks data transfer into the shift register until a count has had sufficient time to stabilize.

4.1 The clock delay monostable output is nominally set to 1.0 microseconds. The worst case minimum for voltage, temperature and life variations is 0.800 microseconds. The clock delay must allow steering set-up time for the most significant bit of the up-down counter. The steering logic path encounters one flip flop and 14 gates with an accumulative worst case delay of 740 nanoseconds. The clock logic path encounters two monostable and two gates with an accumulative nominal delay of 165 nanoseconds. The net delay to be masked is 575 nanoseconds, resulting in a timing margin of 0.225 microseconds in the worst case.

4.2 The interrogate masking signal is nominally 2.25 microseconds. The worst case minimum for voltage, temperature and life variations is 1.800 microseconds. The masking signal logic delay is 100 nanoseconds (one gate and a monostable). The clock to count stabilization and transfer logic delay is through two flip flops, four gates and the clock pulse width, for an accumulative delay of 1240 nanoseconds. The net required masking interval is 1140 nanoseconds, resulting in a worst case margin of 0.660 nanoseconds.

4.3 In the calculations of 4.1 and 4.2, the following notes apply:

1. Worst case monostable variations are ± 20 %.
2. Variation in the various monostables shall track to within ± 5 %.
3. For stable operation, timing components are external 1% precision metal film resistors and 2% Corning glass capacitors; rather than the I/C internal components.

5.0 LOGIC WORST CASE ANALYSIS

The logic family used in the logic design of the FSS-SC has been specified under restricted voltage, temperature and interface loading parameter boundaries. If the logic elements are used within these parameter boundaries, the logic will function in the worst case. The supply voltage range is 4.7 volts to 5.3 volts as compared to the suggested 4.5 volts to 5.5 volts range. The temperature environment ranges from -40°C to +74°C, whereas the logic family is rated from -55°C to +1.25°C. No fan-out rating was exceeded in the logic design. Since the design limitations of the various devices were respected, the logic portion of the FSS-SC will perform under all worst case conditions.

6.0 SUMMARY

The design of the FSS-SC was reviewed under all environment and operating conditions. Operating margin was shown to exist in all critical areas of operation under the worst case limit conditions. It is concluded, therefore, that the design of the FSS-SC is sound and will meet all worst case operating requirements.

APPENDIX B

WORST CASE ANALYSIS OF POWER CONVERTER

SPACE SYSTEMS LABORATORY

TECHNICAL MEMORANDUM NO. ADS-21

24 September 1968

Project 3511

ABSTRACT:

This TM presents the performance characteristics and circuit analysis for the power supply used in the Fine Sun Sensor, Signal Conditioner.

SUN SENSOR POWER SUPPLY

By: D. Gieske

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INTRODUCTION

This report contains the performance characteristics and an analysis of the major design considerations. The analysis includes the peak flux density and power dissipation of the power transformer, power dissipation and drive to the power switching transistor, and ripple voltage of the tantalum capacitors. The remainder of the supply components are conservatively applied as can be seen from the power dissipations marked on the schematic.

1.0 PERFORMANCE CHARACTERISTICS

1.1 PRIME POWER

The converter shall meet all requirements, except during transient tests, when operating with an input voltage of positive 28v $\pm$ 4vdc and with a source impedance of less than 1 ohm.

1.2 OPERATING TEMPERATURE

The converter shall meet all requirements over the temperature range of -26°C to + 85°C.

1.3 WARMUP TIME

The converter shall meet all requirements 2 minutes after application of B-plus voltage at any temperature specified in 1.2

1.4 POWER LINE CURRENT RIPPLE

The feedback ripple on the input power lines shall not exceed 0.5ma peak to peak while operating under nominal load and 28v input.

1.5 OUTPUT VOLTAGE AND LOADS

Output Voltage	Current		Power	
	Typ.	Max.	Typ.	Max.
+5	170ma	280ma	900mw	1400mw
-5	21ma	24ma	105mw	120mw
Total Power Output			1005mw	1520mw

The +5v power is based on logic power typical and maximum numbers. Therefore probability of system requiring 1520mw is small and supply design was based on 1150mw output power. This power level is considered nominal for supply testing conditions.

1.6 OUTPUT VOLTAGE REGULATION

1.6.1 Regulation vs. Input Voltage

The output voltage shall not vary more than ±2% with input voltage variations of +28v ±4vdc. at 25°C and nominal load.

1.6.2 Regulation vs. Temperature

The output voltage shall not vary more than ±3% over the temperature range of -26°C to +85°C with +28vdc input and nominal load.

1.6.3 Regulation vs. Load

The output voltage shall not vary more than ±5% with load variations of ±20% from nominal with +28vdc input and at 25°C.

1.7 ISOLATION

The converter input terminals, output terminals and case shall be mutually isolated from each other by at least 10 megohms up to 100vdc.

1.8 REVERSE POLARITY

The converter shall not be damaged by application of reverse polarity to the prime power input terminals.

1.9 POWER LINE TRANSIENTS

The supply shall not be damaged by any of the transient voltages described below:

Voltage	Duration
+50	10μsec
+28	350μsec
+10	1μsec
-10	1μsec
-28	350μsec
-100	5μsec

Transient repetition rate is a maximum of 10 per second.

1.10 EFFICIENCY

The converter efficiency shall not be less than 60% under any or all of the following conditions:

1.) Input Voltage, +24v to +32v

2.) Load, ±20% from nominal

3.) Temperature, -26 C^{o} to +85^{o}C

2.0 ANALYSIS

2.1 TRANSFORMER

2.1.1 Flux Density

The maximum flux density the transformer core can handle is 2000 gauss. With a nominal load and +28v input, the inductance required for 100KHz operation is 580μh. If this transformer is now operated at maximum power level 1.52 watts output and at an efficiency of 65%, the peak input current would be 334ma.

$$Pin = \frac{Pout}{E_{ff}} = \frac{1.52}{.65} = 2.34w$$

$$I_{IN\ (ave)} = \frac{Pin}{Ein} = \frac{2.34}{28} = 83.5ma$$

$$I_P = 4Iave = (4)\ (83.5) = 334\ ma$$

This results in an operating frequency of 74.5 KHz assuming a symetrical duty cycle.

$$f = \frac{2E}{LI_P} = \frac{(2)\ (28)}{(5.6x10^{-4})\ (3.34x10^{-1})} = 7.45x10^{4}Hz$$

If the input voltage is now changed, the duty cycle will change to compensate for it. The time current is flowing in the primary is given by

$$t_1 = \frac{P_{IN} L}{E_{IN}^2} + \frac{1}{E_{IN}} \sqrt{\frac{P_{IN} L}{E_N^2} + \frac{P_{IN}^2 L^2}{f}}$$

where f is the frequency with 28v applied to the input (74.5KHz). Thus primary current flows for the following durations:

E_{IN}	t_1
32	5.6 µsec
28	6.7 µsec
24	8.2 µsec

The flux density reached in the transformer core is given by:

$$B = \frac{E_{IN}\ t_1\ (10^8)}{N_P\ A_E}$$

where N_P = primary turns

A_E = effective area of core

For the core used, 1811P-A250-3B7, the effective core area is 0.433 sq.cm. and the primary turns is 48. Thus, the maximum flux densities at the various input voltages with a maximum load are:

V_{IN}	B
32	945 gauss
28	896 gauss
24	815 gauss

This results in a worst case flux density of less than one half the allowed value.

2.1.2 Power Dissipation

The power dissipated in the transformer, due to wire resistance, is 126mw when operating with maximum load. This results in a temperature rise of about 2.5°C in the core. Much less than the allowed 20°C.

2.2 SWITCHING TRANSISTOR

2.2. Power Dissipation

The power dissipated in the 2N2880 transistor would be 1.82 watts maximum. This assumes maximum loading and a constant 0.25v V_{CE} saturation voltage. The power dissipation for the different input voltages are:

V_{IN}	I_P	t_1	f	P_{ave}	T_{rise}
32	320ma	5.6×10^{-6} sec	91.5KHz	1.82w	6°C
28	334ma	5.7×10^{-6} sec	74.5KHz	1.75w	5.8°C
24	352ma	8.2×10^{-6} sec	67KHz	1.65w	5.45°C

The expression for the average power is:

$$P_{ave} = \frac{V_{IN} I_p t_1 f}{2}$$

This does not account for the power dissipated during the switching times, but this is small compared to Pave. The junction temperature rise is based on a 3.3°C/watt junction to stud thermal resistance. Thus, with maximum load and a stud temperature of 85°C, the junction temperature will be 90°C, which is 110°C from the maximum operating junction temperature of 200°C.

2.2.2 Transistor Drive

The drive current to the switching transistor is supplied by Q3 whose drive is in turn supplied by Q1. The nominal collector current of Q1 is 1.68ma. Under worst case conditions this could decrease by 25% to 1.26ma. At the lower temperature encountered, the minimum beta of Q3 would be about 60. Allowing for aging, this beta could decrease to 30, thereby limiting Q4 drive current to 37.8ma. Assuming a worst case beta for Q4 of 10 allows the peak current to reach 378ma, which is more than that required for maximum power and minimum input voltage.

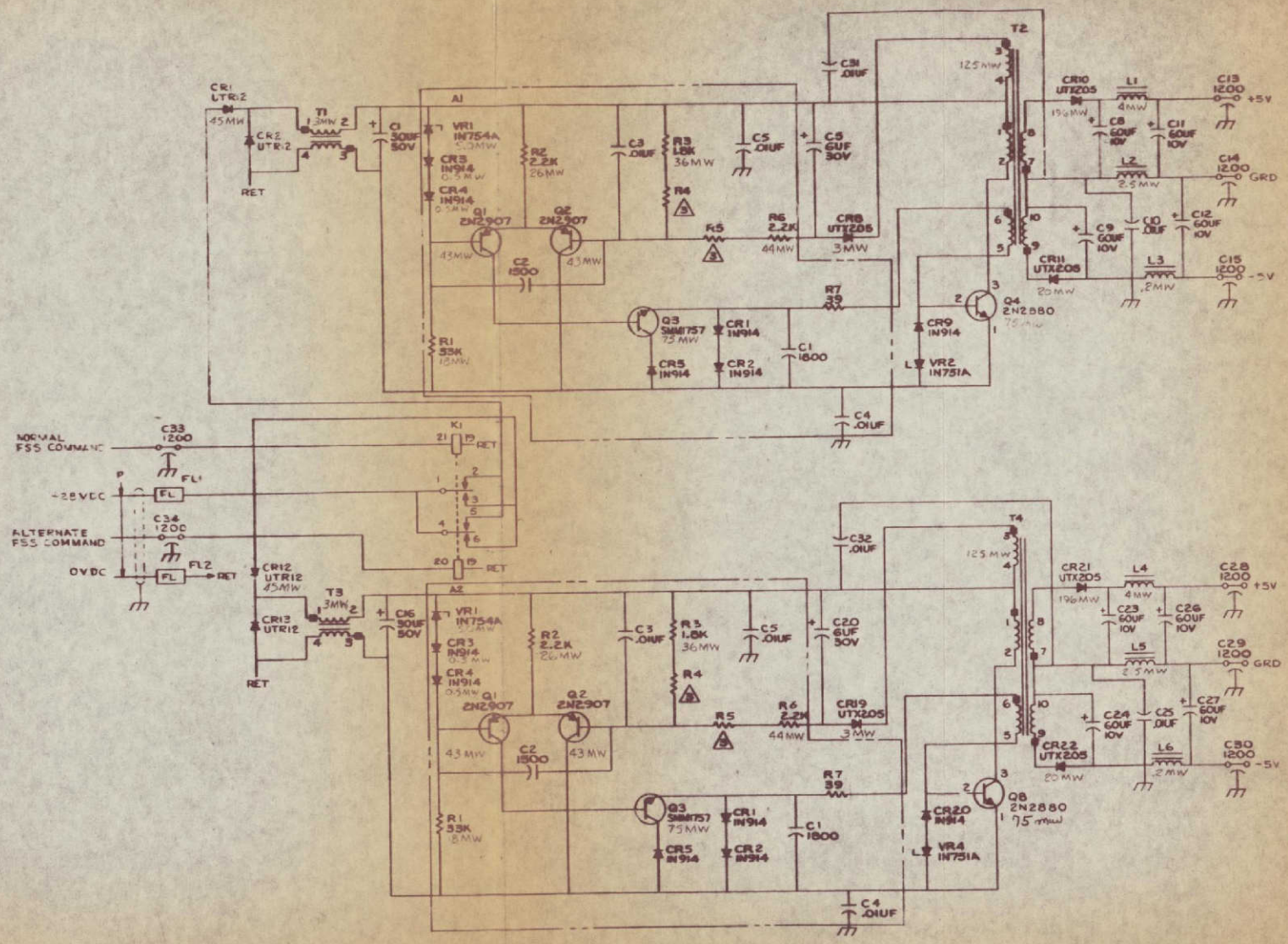
2.3 TANTALUM FOIL CAPACITORS

Tantalum foil capacitors impose restrictions as to the rms value of ripple voltage that can be impressed across them. At the 100KHz operating rate of the supply, the value of the ripple voltage is reduced to the milli volt range. To insure proper application of the capacitors, one of two methods may be employed. First application derating data can be used or the capacitor can be put into the circuit and temperature rise measurements taken. The first method is ultra-conservative, while the second method is realistic.

The capacitors are properly used and not overstressed if a temperature rise of 15°C is not exceeded during operation. The capacitor with the largest ripple voltage in the supply is C8. The temperature rise measured on the body of this capacitor was 1.5°C, only one-tenth the allowed value. Thus, all foil capacitors are conservatively applied.

2.4 GENERAL

The remaining circuit components are operated at conditions which are all well below their rated values.



FOLDOUT FRAME

FOLDOUT FRAME 2

APPENDIX C

STUDY OF COMPONENT MOUNTING TECHNIQUES

interoffice correspondence

From: Joe Clyne

Date: May 14, 1969

To: Ken Eme (7)

SUBJECT: Sun Sensor Power Supply Boards, Thermal Cycling and Component Mounting Techniques.

cc: Pat Armstrong
Fred Davis
Mike Kalember
Barney Leneweaver
Foster Turner
Jim McHenry
Jim Reid
Al Welt

Introduction

Extensive termperature cycling tests and inspection has been performed on power supply board assemblies 01-P01002AC01 and 01-P01002A003 for Sun Sensor, Project 3511. As suggested by the customer, tests were patterned from procedures recommended by Ray VanOrden in NASA TMX-53731, "Mounting of Components to Printed Wiring Boards". Three power supply board assemblies were tested to verify suitability of component mounting and conformal coating practices. Each test board (assembly) was made up of one of the two power supply boards, 84-P01003A01 or 84-P01003A02, which is a single sided, non-plated-thru-hole board of .042" type GE laminate with 2 ounce copper, plus the following components, all with clinched lead ends:

6 each Glass bodied diodes (axial leads)
5 each Composition resistors (axial leads)
3 each Molded capacitors
3 each Transistors (TO-18 cans)

Test Board Assembly

Board finish was hydrosqueegeed solder, all joints made with Sn 63 solder. Staking of components to the board, where applicable, was performed with Stycast 2850 GT (rigid epoxy) per MPS 12.A46. All boards were conformally coated with Hysol PC22 urethane per MPS 12.A45. Table I lists details of assembly variables.

Test Board Number	Component Mounting, See Fig. 1	Conformal Coating See Fig. 2
1	Method A, C	Type I, Thick
2	Method B, C	Type I, Thick
3	Method B, C	Type II, Thin

Table I - Test Board Assembly Variables

Testing Procedure

Following assembly of test boards, a critical inspection of each board was performed to establish basis for evaluation. 100% inspection was performed at 20X (up to 60 X to resolve questionable conditions) after 15, 32, 100, 151, and 200 temperature cycles. Temperature exposures consisted of cycling from -55°C. (-67°F.) to + 100°C. (+212°F.) in an air circulating chamber. Soak time at each temperature extreme was 30 minutes. Duration of each full cycle was approximately three (3) hours. Tests were performed in Motorola temperature chamber #2 located in the Environmental Test Facility. CO_2 was used for cooling. Humidity was not controlled or recorded, but the equipment and procedure suggests it was a "dry" environment.

Definitions of Joint Defects

The following definitions were used as criteria for note taking and reporting during all inspection operations:

Strain - Evidence of movement by a change of texture (orange peel or dullness) in a logical pattern.

Crack - Incomplete separation, generally at heel of clinch, could be at surface only in early stages.

Separation - Complete or apparently complete separation of lead from board. May or may not have electrical continuity.

Test Results

Table II shows final visual inspection results. Note that all joints were declared visually acceptable and without strain prior to tests. Note also that no joint had progressed to "separation" during the test period. The absence of a number in the table indicates a lack of activity for those joints at that time. Report of a crack may or may not have been reported as strain at an earlier inspection period. Inspection worksheets and other details are available in the Materials and Processes office.

	Inspection	Resistors		Transistors		Capacitors		Diodes	
	Total Cycles	Strain	Crack	Strain	Crack	Strain	Crack	Strain	Crack
Test Board No. 1	0								
	15			2		5	1	2	
	32			3			3	1	1
	100	1	1	1			1	3	
	151			1			1		1
	200							2	1

	Inspection	Resistors		Transistors		Capacitors		Diodes	
	Total Cycles	Strain	Crack	Strain	Crack	Strain	Crack	Strain	Crack
Test Board No. 2	0								
	15					1		1	
	32						1	2	
	100					1		2	1
	151		1						1
	200	2						1	
Test Board No. 3	0								
	15							1	
	32								
	100					1		1	
	151								
	200			1				1	1

Table II - Results of Thermal Cycling Inspection

Conclusion

1. Detailed inspection of Board #3 shows a definite correlation between conformal coating thickness and the reported discrepancies. In particular, the single cracked joint had a heavier coating in the immediate vicinity, more like Type I of Figure 2.

2. Components should definitely include significant bend relief on the single sided board joint design if soldered with Sn 63.

3. Conformal coating for the power supply boards should be mixed and applied per MPS 12.445 except for the following:

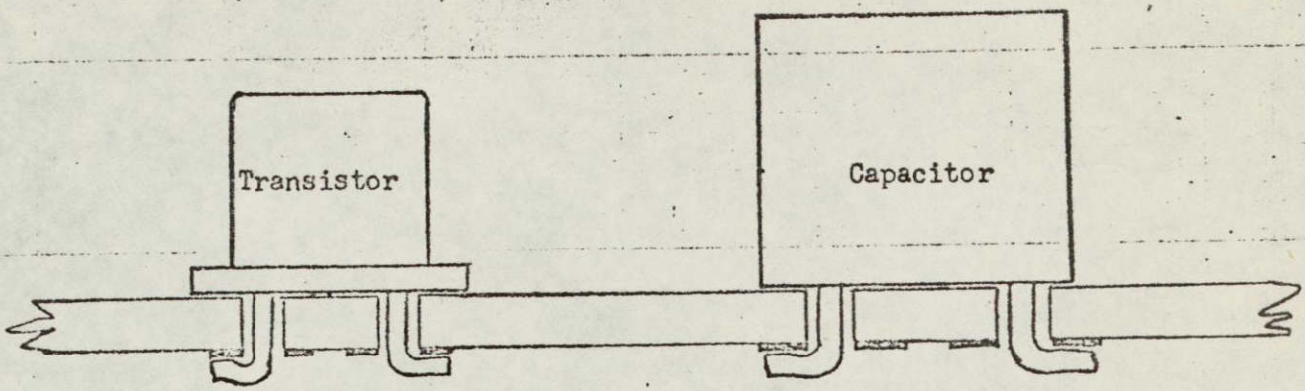
   a. PC22 should be thinned with 30% by weight of toluene.
   b. Coating should be thin enough that bridging of leads to board and between adjacent components does not exist.
   c. Air dry coating 12 hours minimum before baking.

4. It is recommended that assembly procedures used on Test Board #3 plus added coating thinning procedures be used on production assemblies.

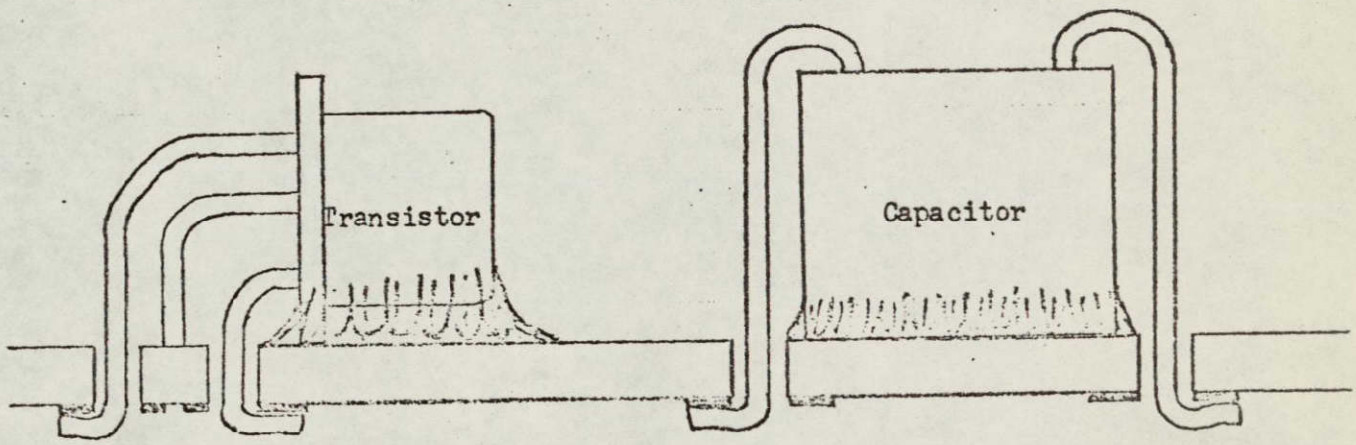
Joe Clyne, Supervisor
Materials And Processes

/kh

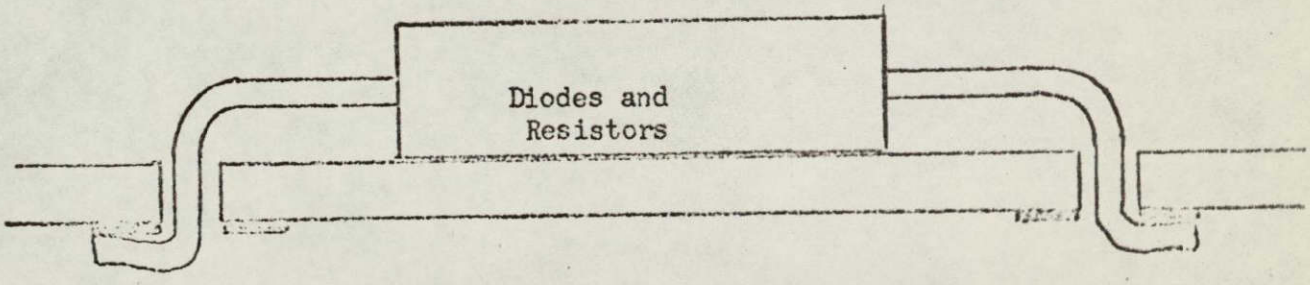
Attachment



Method A - Components mounted flush on boards, no bend relief in leads - used on Test Board #1.

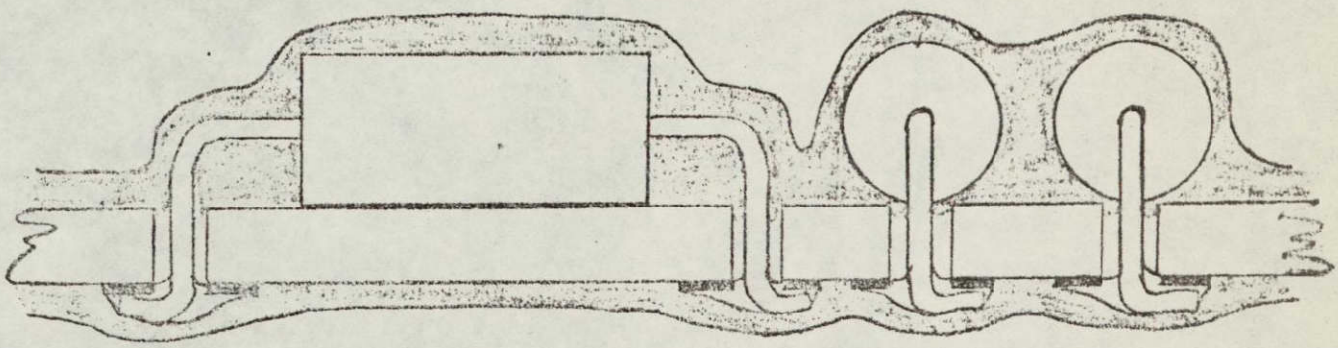


Method B - Components staked to board with Stycast 2850GT, large bend relief in lead - used on Test Boards #2 and #3. Sleeving used over capacitor leads.

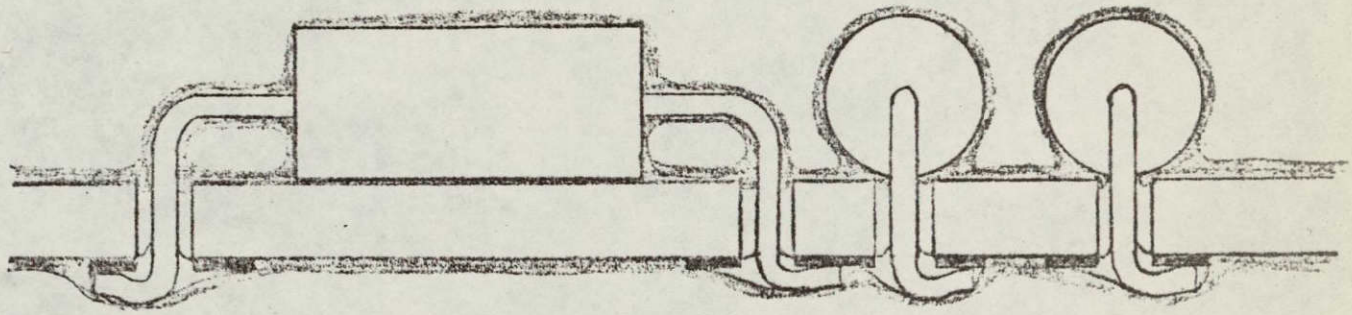


Method C - Axial lead components with normal bend relief used on all test boards.

FIGURE 1 - COMPONENT MOUNTING METHOD



Type I - Thick coating (brush coat without thinning), .010" nominal thickness on flat surface. Coating fills space between components, gap between part leads and board filled. Used on Test Boards #1 and #2.



Type II - Thin coating (brush coat) thinned with 30% by Weight of Toluene, .004" nominal thickness on flat surface. Coating is uniform thickness, covering completely, but not restraining part lead bend relief or adjacent part bodies. Used on Test Board #3.

FIGURE 2

CONFORMAL COATING VARIANCE
(Shaded Areas Represent PC22 Conformal Coating)

APPENDIX D

HOUSING BOSS VIBRATION ANALYSIS

From: Wes Thatcher Date: October 28, 1969

To: Ken Eme Subject: Analysis, Project 3511/Sun Sensor.

Tests on the Sun Sensor using qualification level vibration inputs have caused failures. Two screws are used to attach through the base of the unit into the electronics. Bosses provided for these screws failed in vibration.

Subsequent brief studies indicate bending stresses induced by the electronics mass in an out of phase mode of vibration with respect to the top may be the cause of these failures. Three possible modifications were considered to reduce the stress in the bosses, they were; 1) addition of damping to reduce the out of phase excursions, 2) increasing the strength of the boss/base interface, and 3) removing the screw. Sinusoidal vibration data on the response of the housing in conjunction with calculated responses to random vibration inputs indicate that removing the screws the best solution to the vibration problem.

Analyses were used as one evaluation tool. The response levels of single-degree-of-freedom systems were calculated for two different random vibration inputs to the systems. One random vibration input was as defined by Motorola document 12-P01030A, Figure 2, sheet 32. The end points of straight lines plotted on log-log paper that define this random input, and the calculated 8.5 g rms level for the curve are shown on Calculation Sheet 1. This input level is referred to as the high level random input. The second random input used was and 11.9 g rms level corresponding to the points shown on Calculation Sheet 2. This input is referred to as the new random input.

The single-degree-of-freedom response levels calculated for the two different random inputs are shown on Calcuation Sheets 3 through 6. Calculation sheets 3 and 4 show the response for maximum transmissibilities for 5 and 15 respectively, when excited by the High Level Random Input; Calculation Sheets 5 and 6 show the responses for the same two transmissibilities when excited by the New Level Random Input. All this data is summarized on Figures 1 and 2.

Preliminary tests indicated that damping materials could not be used effectively. Space limitations restricted the amount of damping material that could be used to the point that it was ineffective. Test data was taken, therefore, to compare the unit response with and without the screws. Three points on the

unit were instrumented to determine the acceleration loads. Location and direction of the acceleration responses measured are shown in Figure 3. Transmissibility data (acceleration out/drive acceleration) was taken for a sinusoidal input swept from 90 to 2,000 Hz at approximately 1 oct/min. The level was a constant 1.3 g, 0 to peak. Test data for the three points monitored is given on Data Sheets 1 through 8. Data Sheets 1 and 2 show the response at the top of the case (this same point is the "base" of the electronics), and Data Sheets 3 and 4 show the response at the end of the cantilevered electronics unit, both along the X axis. Refer to Figure 2. Data Sheets 5 through 8 show the responses at equivalent points along the Y axis. The transmissibilities in decibels as shown on the data sheets can be converted to straight ratios using the conversion chart, Figure 4.

The data indicates a case or housing resonance at 700 Hz along the X axis and at 850 Hz along the Y axis. In addition, there is a cantilever resonance of the electronics unit at 350 Hz in the X direction and 420 Hz in the Y direction. The special test data shown on Data Sheets 9 and 10 demonstrates the cantilever response mode. This data was taken by using the top of the housing as an input reference for acceleration and plotting the response of the cantilevered end of the electronics unit. It indicates a cantilever mode of vibration with one major response frequency.

Using the single-degree-of-freedom response calculations as approximates of the actual response data, the random loads on the electronic unit can be predicted. Figure 1 shows a reduction in random response from 29 g rms to 11 g rms in the X direction on the electronics as a result of removing the screws based on the High Level Random Input. Similar reductions can be shown for the other inputs and response point.

Since removing the screws eliminates use of the boss that failed in vibration, and reduces random response levels into the electronics this is the solution recommended. The alternative, strengthing the bosses, could cause increased response loads in the electronic unit and induce component failures.

Wes Thatcher

Wes Thatcher, Senior Staff Engineer
Structural Analysis Group
Mechanical Engineering Laboratory

aak

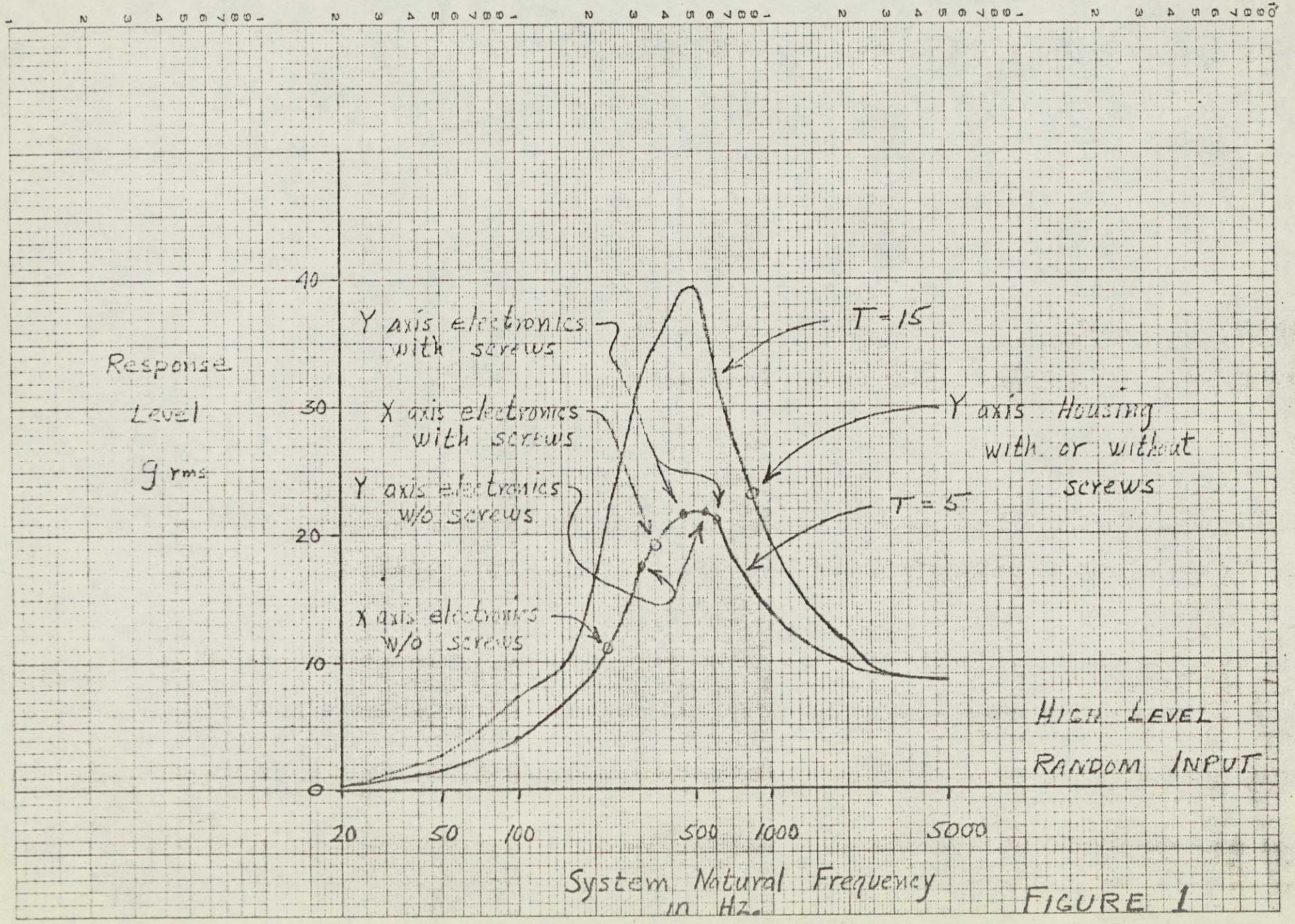


FIGURE 1

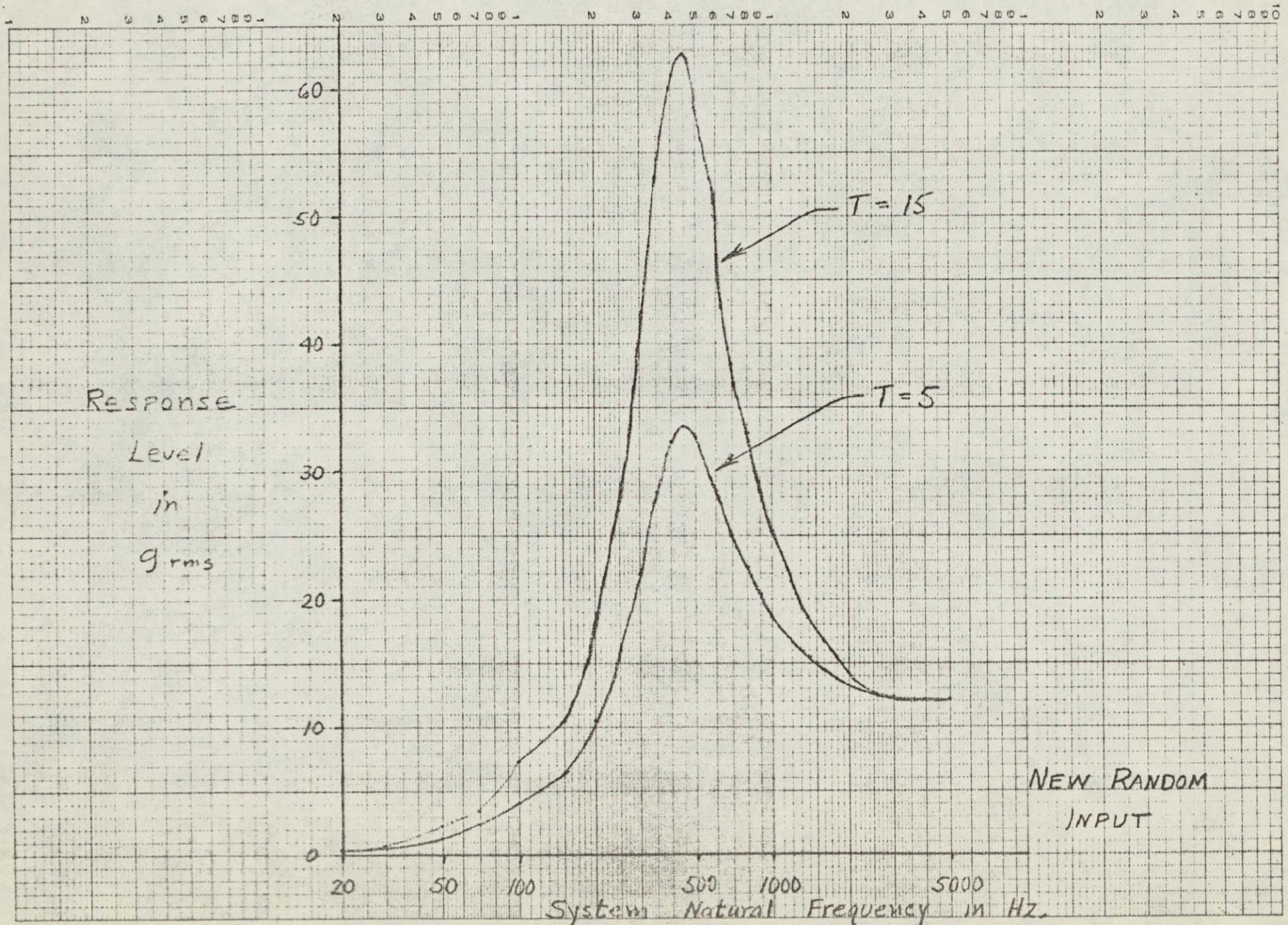


FIGURE 2

K+E AUDIO FREQUENCY 46 6882
MADE IN U.S.A.
KEUFFEL & ESSER CO.

PROJECT ______ UNIT ______ SER. NO. ______

X AXIS FREQ. RANGE [illegible] 000 Hz.

PLOTTER CAL ______ X ______ Y 10 dB/in

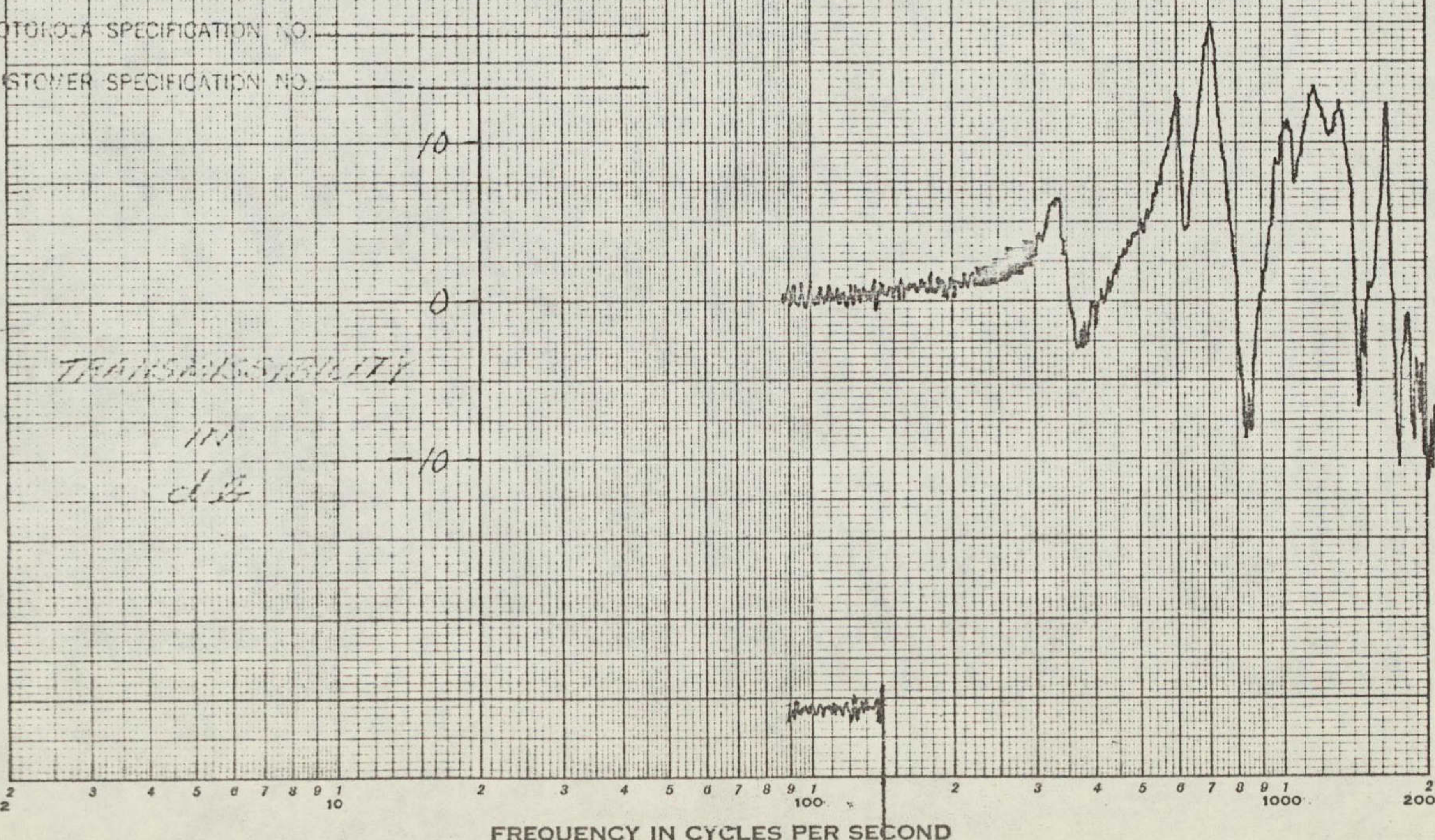
ACCELERATION 1.3 PKGS. DISPLACEMENT ______ DA

VIBRATION DATE [illegible] BY ______

REMARKS [illegible]
[illegible] Accel #3

MOTOROLA SPECIFICATION NO. ______

CUSTOMER SPECIFICATION NO. ______



DATA SHEET 1 OF 10

K•E AUDIO FREQUENCY 46 6882
MADE IN U.S.A.
KEUFFEL & ESSER CO.

PROJECT ______ UNIT ______ SER. NO. ______

X AXIS FREQ. RANGE 90 - 2000 Hz

PLOTTER CAL ______ X ______ Y 10 dB/in

ACCELERATION 1.5 PKGS. DISPLACEMENT ______ DA

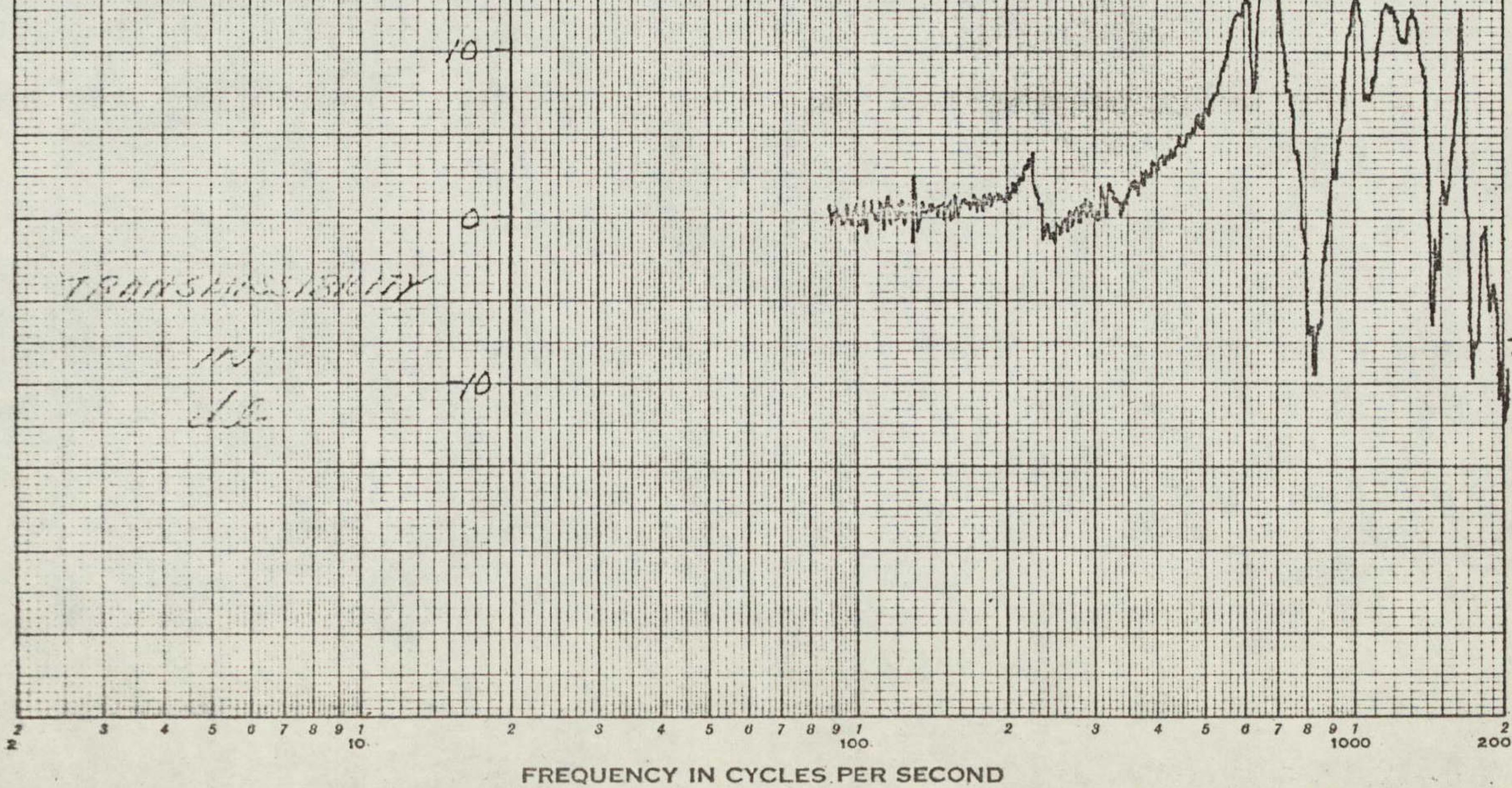
VIBRATION DATE [illegible] BY ______

REMARKS [illegible]

[illegible]

MOTOROLA SPECIFICATION NO. ______

CUSTOMER SPECIFICATION NO. ______



DATA SHEET 2

K+E AUDIO FREQUENCY 46 6882
MADE IN U.S.A.
KEUFFEL & ESSER CO.

PROJECT [illegible] UNIT ESS-5C SER. NO. 2

X AXIS FREQ. RANGE 90-2000

PLOTTER CAL. [illegible] X Y 10 DB/IN

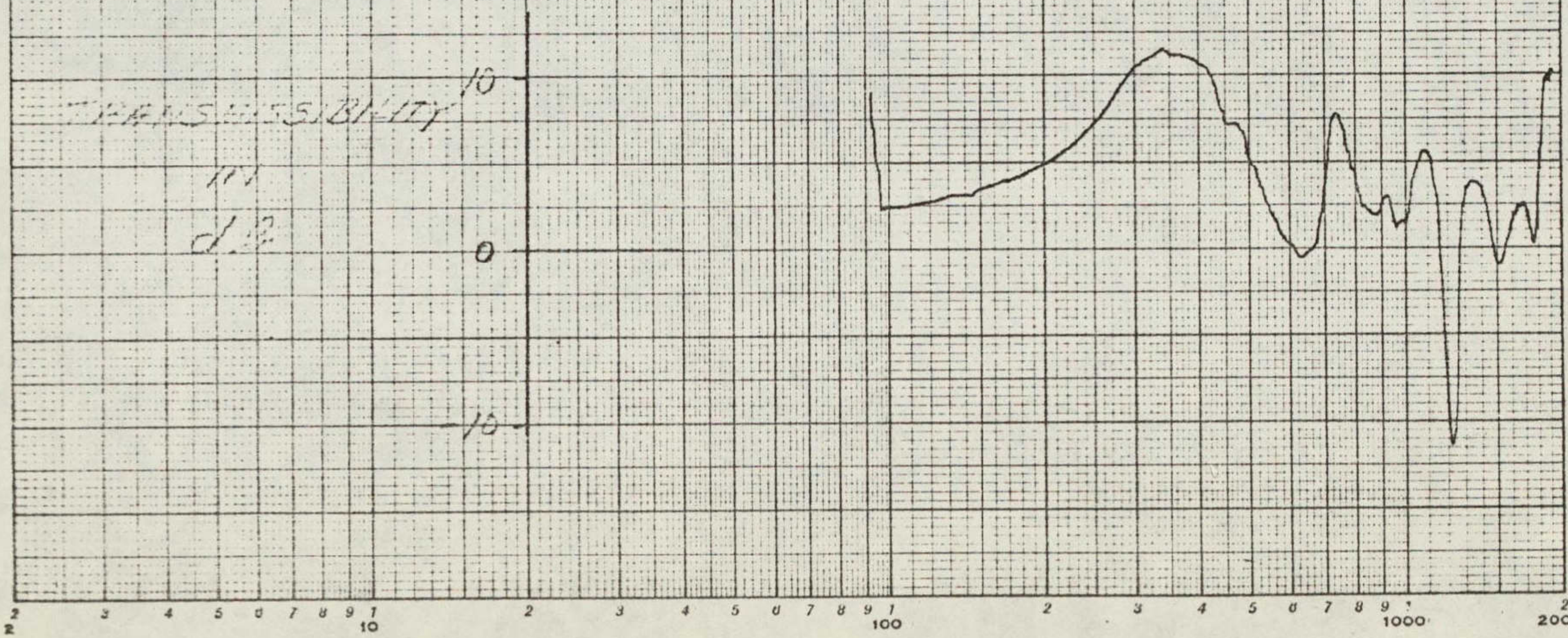
ACCELERATION 2.3 PKGS. DISPLACEMENT DA

VIBRATION DATE [illegible] BY [illegible]

REMARKS [illegible]

MOTOROLA SPECIFICATION NO.

[illegible] SPECIFICATION NO.



FREQUENCY IN CYCLES PER SECOND

DATA SHEET 3

HIGH LEVEL
~~[illegible]~~ RANDOM PROJECT 3511 10-14-69

FREQ. [HZ]	P.S.D. [SQ.G/HZ]	SLOPE [DB/OCT]	AREA [SQ.G]
20.	.0010		
		6.2755	.6646
90.	.0230		
		.0000	1.3800
150.	.0230		
		9.0438	9.6272
280.	.1500		
		.0000	33.0000
500.	.1500		
		-10.8805	27.9222
2000.	.0010		

G [RMS] = .85202070E 01

8.5

CALCULATION - SHEET 1

NEW ~~LEVEL~~ RANDOM PROJECT 3511 10-14-69

FREQ. [HZ]	P.S.D. [SQ.G/HZ]	SLOPE [DB/OCT]	AREA [SQ.G]
20.	.0002		
		9.0500	.5154
90.	.0230		
		.0000	1.1500
140.	.0230		
		9.1816	35.6489
360.	.4100		
		.0000	41.0000
460.	.4100		
		-11.9403	62.7048
2000.	.0012		

G [RMS] = .11875145E 02

11.9

CALCULATION SHEET 2

**MAX. T= 5.0 **D.R.= .10258E 00 **R= .98985E 00 **PER= .100E-01

HIGH LEVEL RANDOM INPUT

NATURAL FREQ. [HZ]	-G- [RMS]	PEAK G [3-SIGMA]
5.000	.030	.090
10.000	.070	.209
20.000	.330	.990
30.000	.752	2.255
50.000	1.629	4.888
70.000	2.674	8.021
100.000	4.085	12.254
150.000	5.774	17.321
200.000	9.253	27.759
250.000	13.590	40.770
300.000	17.124	51.372
350.000	19.112	57.335
400.000	20.576	61.729
450.000	21.653	64.958
500.000	21.911	65.732
600.000	20.282	60.846
700.000	18.118	54.353
800.000	16.374	49.123
900.000	15.019	45.056
1000.000	13.963	41.889
1200.000	12.446	37.337
1400.000	11.483	34.450
1600.000	10.804	32.413
1800.000	10.287	30.861
2000.000	9.792	29.376
2500.000	9.095	27.284
3000.000	8.877	26.631
4000.000	8.706	26.117
5000.000	8.636	25.907

CALCULATION SHEET 3

**MAX. T= 15.0 **D.R.= .33476E-01 **R= .99889E 00 **PER= .100E-01

HIGH LEVEL
RANDOM INPUT

NATURAL FREQ. [HZ]	-G- [RMS]	PEAK G [3-SIGMA]
5.000	.013	.039
10.000	.042	.127
20.000	.497	1.490
30.000	1.275	3.825
50.000	2.802	8.407
70.000	4.681	14.043
100.000	7.233	21.700
150.000	9.372	28.117
200.000	16.004	48.012
250.000	24.518	73.553
300.000	31.480	94.441
350.000	34.436	103.309
400.000	36.899	110.698
450.000	39.025	117.076
500.000	39.620	118.861
600.000	33.998	101.995
700.000	28.527	85.580
800.000	24.934	74.801
900.000	22.034	66.101
1000.000	19.655	58.964
1200.000	16.668	50.003
1400.000	14.557	43.670
1600.000	13.203	39.610
1800.000	12.151	36.454
2000.000	10.697	32.092
2500.000	9.108	27.324
3000.000	8.880	26.640
4000.000	8.706	26.119
5000.000	8.636	25.908

CALCULATION SHEET 4

**MAX. T= 5.0 **D.R.= .10258E 00 **R= .98985E 00 **PER= .100E-01

NEW LEVEL
RANDOM INPUT

NATURAL FREQ. (HZ)	-G- (RMS)	PEAK G (3-SIGMA)
5.000	.035	.105
10.000	.074	.222
20.000	.229	.687
30.000	.520	1.559
50.000	1.327	3.980
70.000	2.456	7.369
100.000	4.116	12.347
150.000	6.322	18.967
200.000	10.605	31.814
250.000	16.043	48.128
300.000	22.326	66.978
350.000	28.399	85.197
400.000	32.210	96.629
450.000	33.636	100.908
500.000	32.800	98.401
600.000	28.628	85.883
700.000	25.015	75.044
800.000	22.308	66.925
900.000	20.286	60.857
1000.000	18.736	56.207
1200.000	16.669	50.007
1400.000	15.363	46.089
1600.000	14.498	43.493
1800.000	13.866	41.599
2000.000	13.322	39.967
2500.000	12.574	37.721
3000.000	12.320	36.959
4000.000	12.111	36.333
5000.000	12.024	36.071

**MAX. T= 15.0 **D.R.= .33426E-01 **R= .99889E 00 **PER= .100E-01

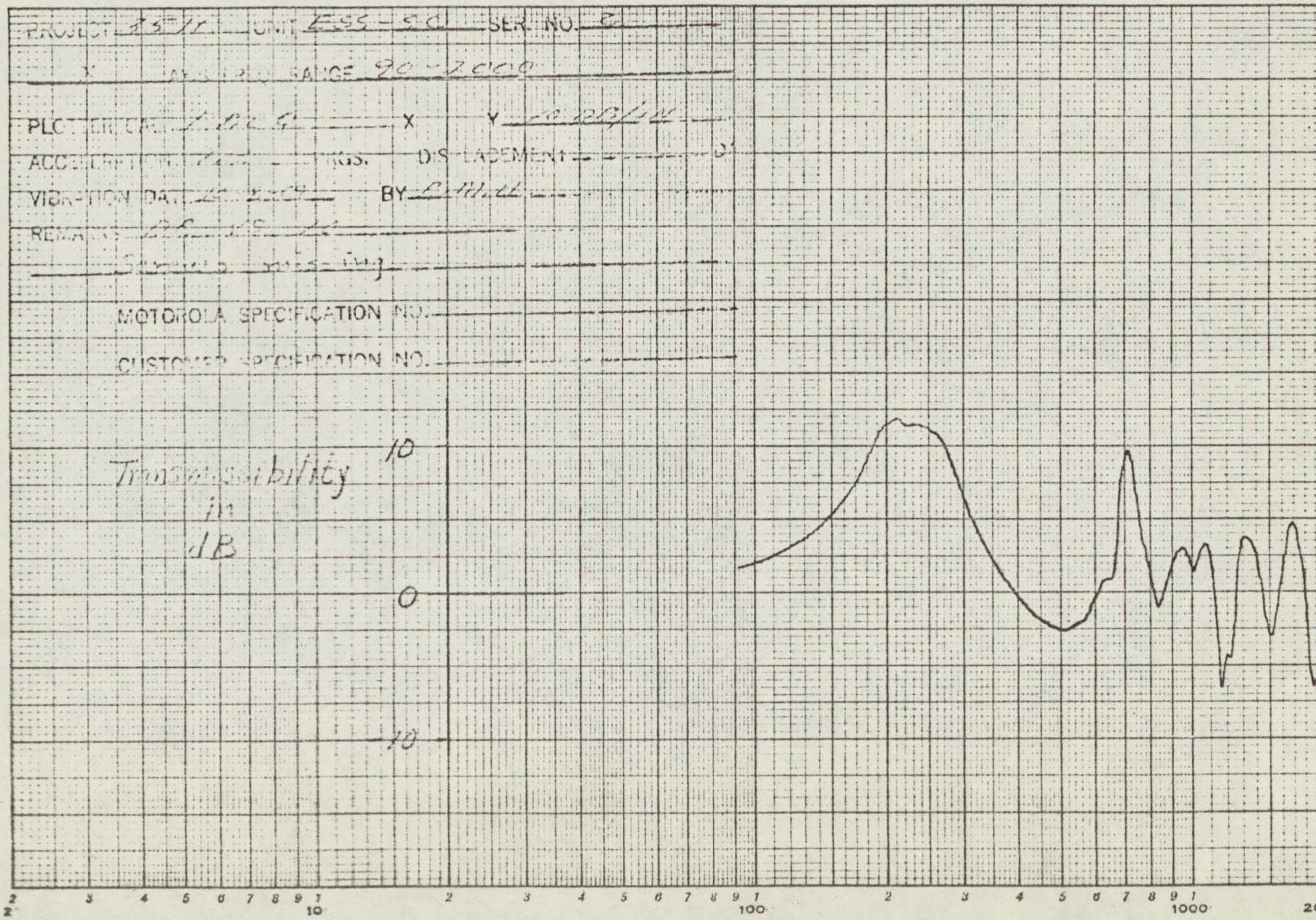
NEW LEVEL

RANDOM INPUT

NATURAL FREQ. [HZ]	-G- [RMS]	PEAK G [3-SIGMA]
5.000	.013	.039
10.000	.035	.106
20.000	.272	.815
30.000	.792	2.375
50.000	2.174	6.521
70.000	4.204	12.611
100.000	7.238	21.714
150.000	10.303	30.909
200.000	18.022	54.065
250.000	27.812	83.437
300.000	40.029	120.088
350.000	53.132	159.397
400.000	59.928	179.783
450.000	62.832	188.496
500.000	58.376	175.127
600.000	46.895	140.686
700.000	38.432	115.297
800.000	32.989	98.967
900.000	28.581	85.744
1000.000	25.413	76.238
1200.000	21.329	63.986
1400.000	18.589	55.767
1600.000	16.890	50.670
1800.000	15.614	46.843
2000.000	14.121	42.363
2500.000	12.586	37.759
3000.000	12.323	36.968
4000.000	12.112	36.335
5000.000	12.024	36.071

CALCULATION SHEET 6

AUDIO FREQUENCY 46 6882
MADE IN U.S.A.
KEUFFEL & ESSER CO.



FREQUENCY IN CYCLES PER SECOND

DATA SHEET 4

KEUFFEL & ESSER CO.

PROJECT [illegible] UNIT [illegible] SER. NO. [illegible]

Y AXIS FREQ. RANGE [illegible]

PLOTTER CAL. [illegible] X Y [illegible]

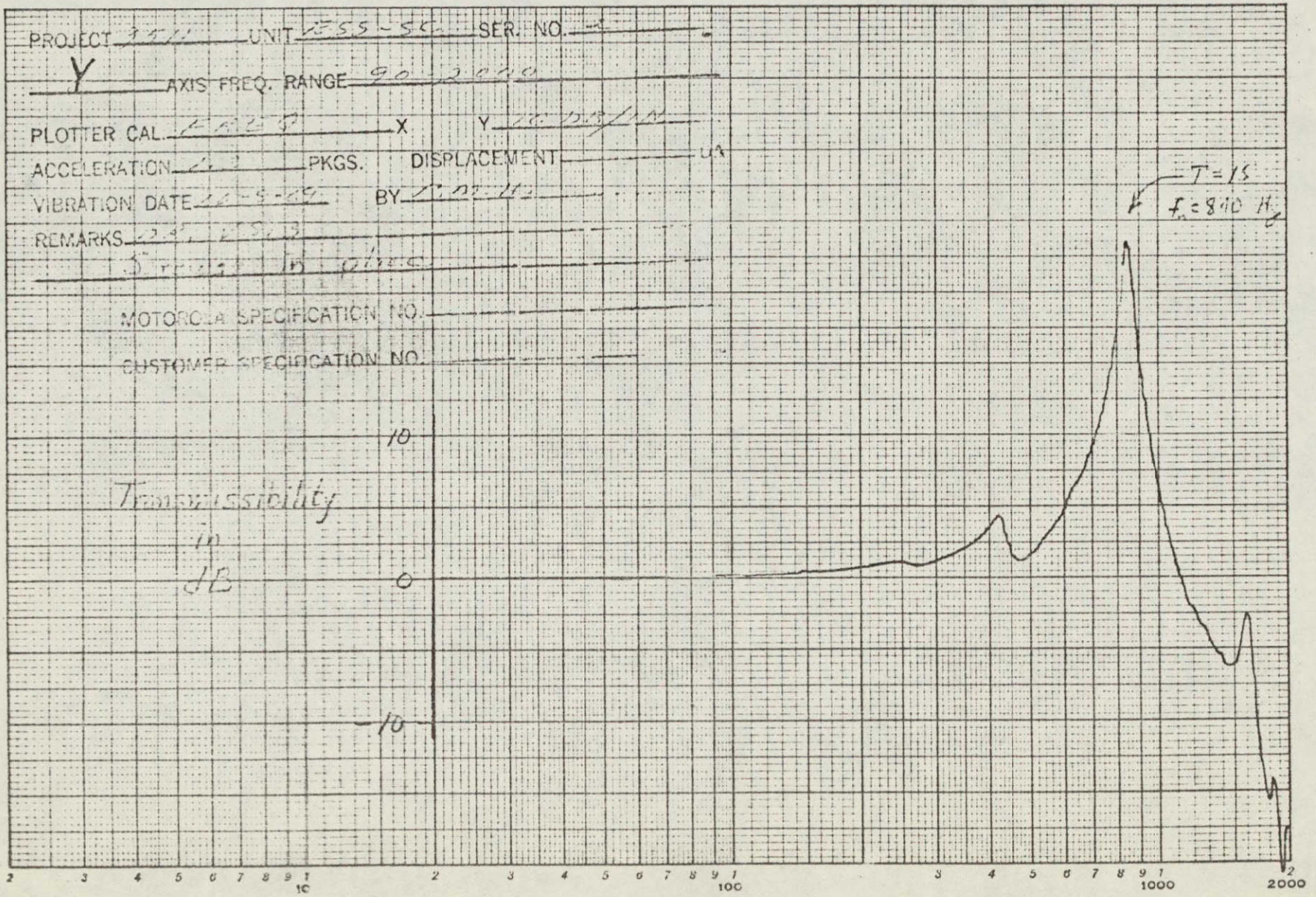
ACCELERATION [illegible] PKGS. DISPLACEMENT [illegible]

VIBRATION DATE [illegible] BY [illegible]

REMARKS [illegible]

MOTOROLA SPECIFICATION NO.

CUSTOMER SPECIFICATION NO.



DATA SHEET 5.

KEUFFEL & ESSER CO.

PROJECT [illegible] UNIT [illegible] SER. NO. [illegible]

Y AXIS FREQ. RANGE [illegible]

PLOTTER CAL [illegible] X Y [illegible]

ACCELERATION [illegible] PKGS. DISPLACEMENT [illegible] DA

VIBRATION DATE [illegible] BY [illegible]

REMARKS [illegible]

MOTORDLA SPECIFICATION NO.

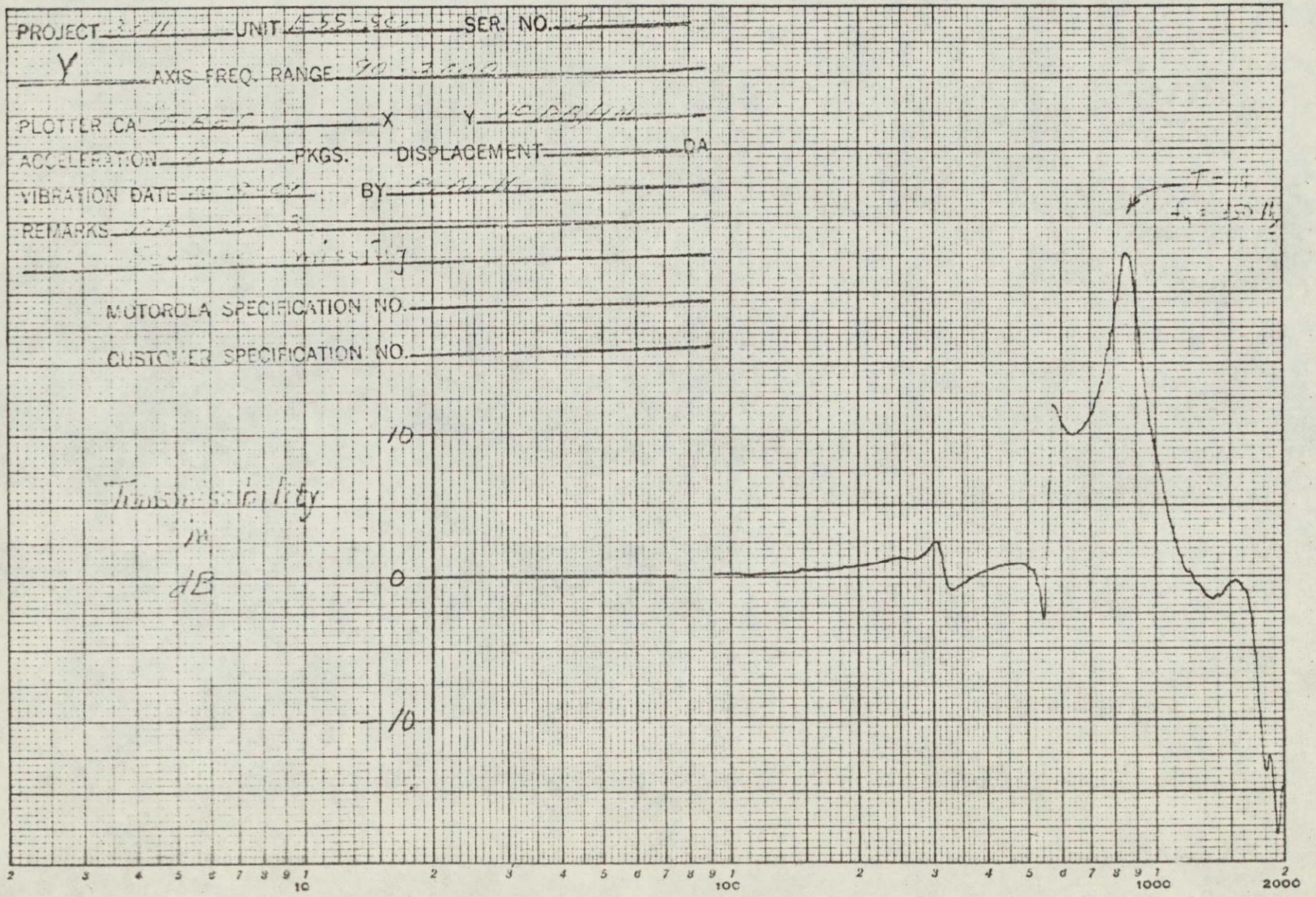
CUSTOMER SPECIFICATION NO.

Transmissibility in dB

10

0

10



FREQUENCY IN CYCLES PER SECOND

DATA SHEET 6

KEUFFEL & ESSER CO

PROJECT [illegible] UNIT [illegible] SER. NO. 2

[illegible] AXIS FREQ. RANGE [illegible]

PLOTTER CAL. [illegible] X Y [illegible]

ACCELERATION [illegible] PKGS. DISPLACEMENT [illegible] DA

VIBRATION DATE [illegible] BY [illegible]

REMARKS [illegible]

[illegible] in place

MOTOROLA SPECIFICATION NO.

CUSTOMER SPECIFICATION NO.

Transmissibility in dB

10

0

-10

T = 6.0

f_n = 620 Hz

T = [illegible]

f_n = 1420 Hz

2 3 4 5 6 7 8 9 1 10 2 3 4 5 6 7 8 9 1 100 2 3 4 5 6 7 8 9 1 1000 2 2000

FREQUENCY IN CYCLES PER SECOND

DATA SHEET 7

KEUFFEL & ESSER CO.

PROJECT [illegible] UNIT [illegible] SER. NO. [illegible]

[illegible] AXIS FREQ. RANGE [illegible]

PLOTTER CAL [illegible] X Y [illegible]

ACCELERATION [illegible] PKGS. DISPLACEMENT [illegible] DA

VIBRATION DATE [illegible] BY [illegible]

REMARKS [illegible]

MOTOROLA SPECIFICATION NO.

CUSTOMER SPECIFICATION NO.

Transmissibility in dB

10

0

-10

$T = 10$

$f_n = 310$ Hz

$T = 8.1$

$f_n = 510$ Hz

2 3 4 5 6 7 8 9 1 10 2 3 4 5 6 7 8 9 1 100 2 3 4 5 6 7 8 9 1 1000 2 2000

FREQUENCY IN CYCLES PER SECOND

DATA SHEET 8

K&E AUDIO FREQUENCY 46 6882 MADE IN U.S.A.
KEUFFEL & ESSER CO.

PROJECT [illegible] UNIT [illegible] SER. NO. [illegible]

[illegible] AXIS FREQ. RANGE [illegible]

PLOTTER CAL. [illegible] X Y [illegible]

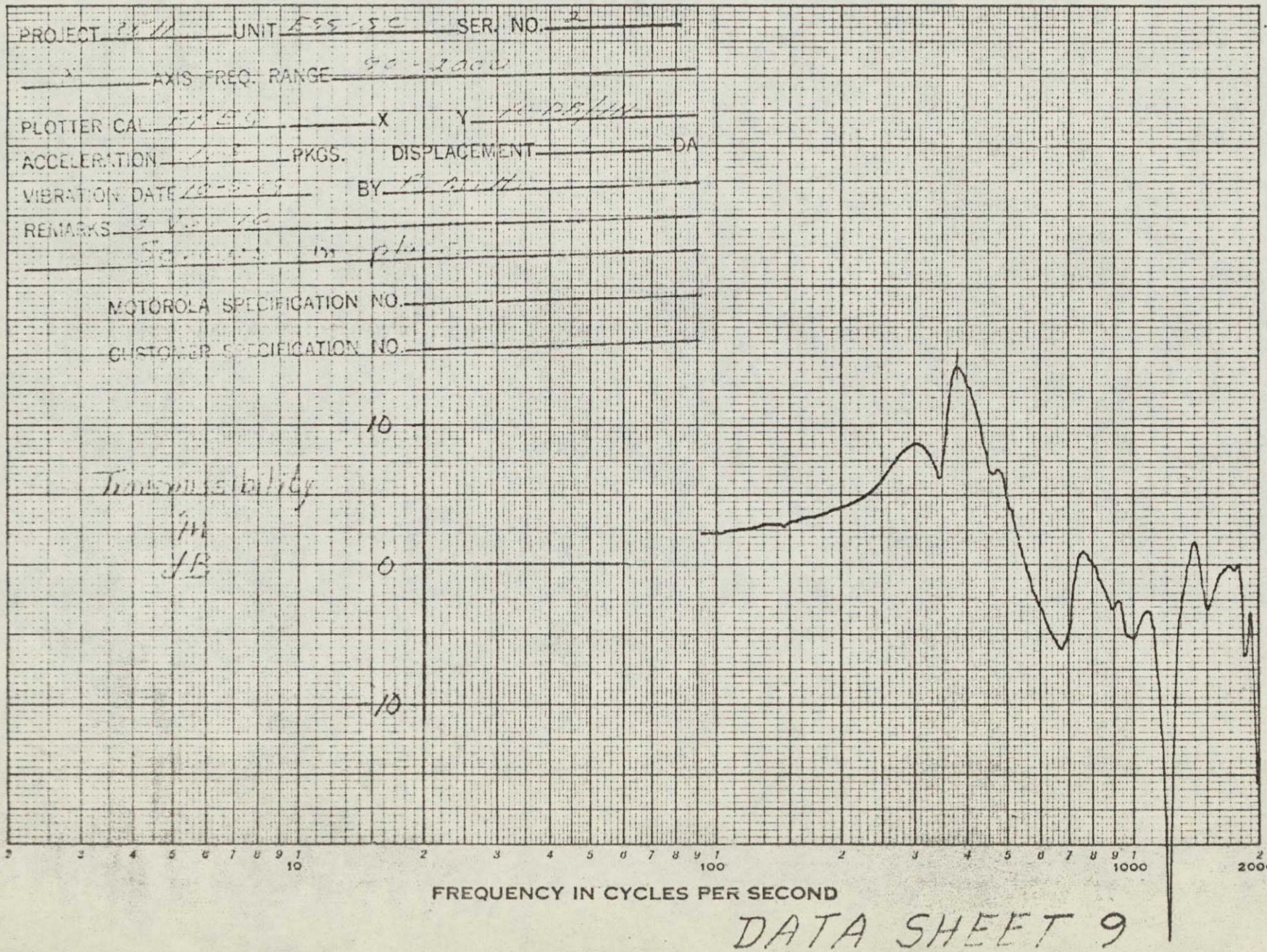
ACCELERATION [illegible] PKGS. DISPLACEMENT [illegible] DA

VIBRATION DATE [illegible] BY [illegible]

REMARKS [illegible]

MOTOROLA SPECIFICATION NO.

CUSTOMER SPECIFICATION NO.



DATA SHEET 9

K&E AUDIO FREQUENCY 46 6882
MADE IN U.S.A.
KEUFFEL & ESSER CO.

PROJECT [illegible] UNIT [illegible] SER. NO. [illegible]

X AXIS FREQ. RANGE [illegible]

PLOTTER CAL. [illegible] X [illegible] Y [illegible]

ACCELERATION [illegible] PKGS. DISPLACEMENT [illegible] DA

VIBRATION DATE [illegible] BY [illegible]

REMARKS [illegible]

MOTOROLA SPECIFICATION NO. [illegible]

CUSTOMER SPECIFICATION NO. [illegible]

10

0

-10

Y

f_n = 235 Hz

2 3 4 5 6 7 8 9 1 2 3 4 5 6 7 8 9 1 2 3 4 5 6 7 8 9 1 2

10 100 1000 2000

FREQUENCY IN CYCLES PER SECOND

DATA SHEET 10

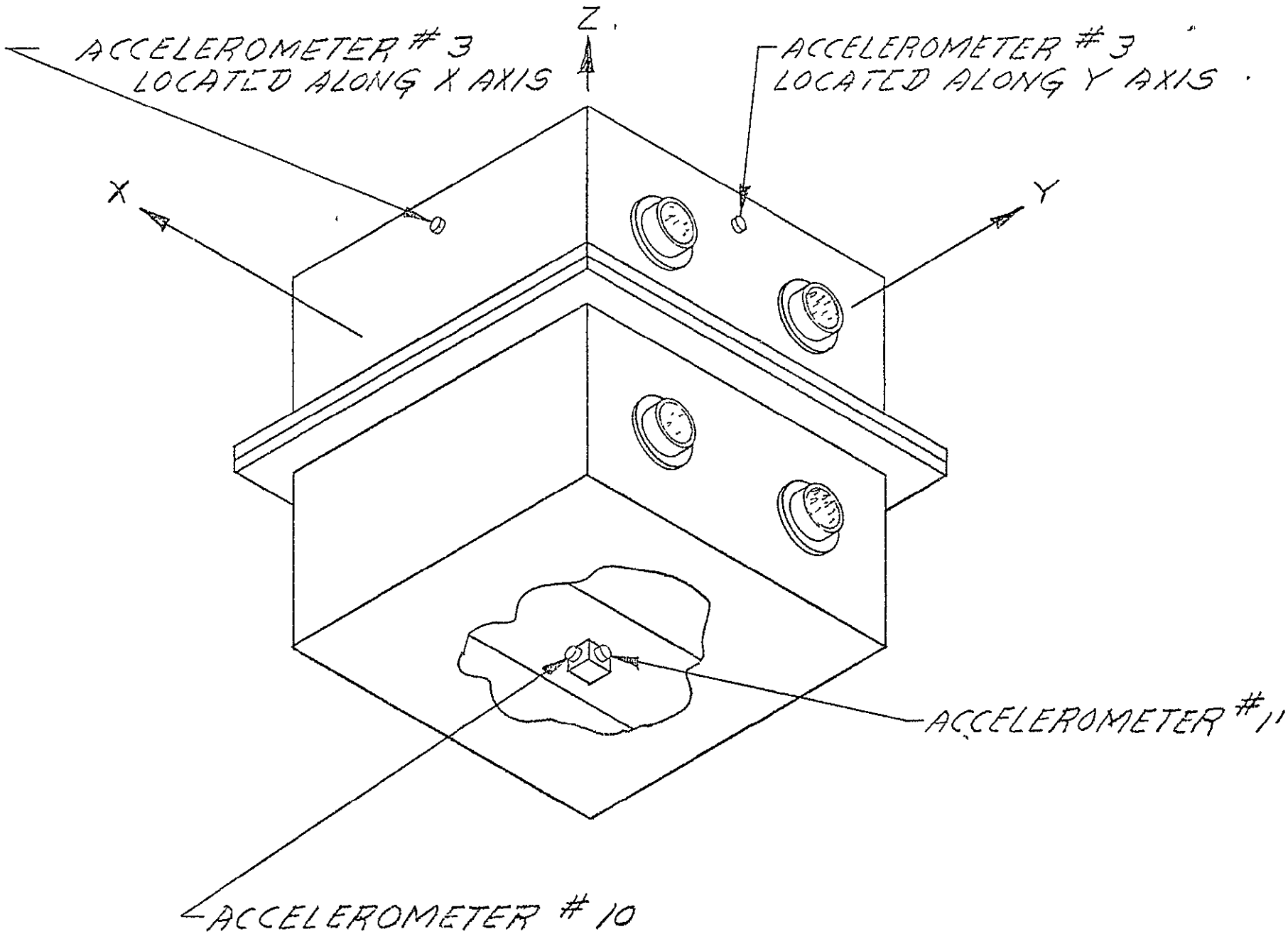
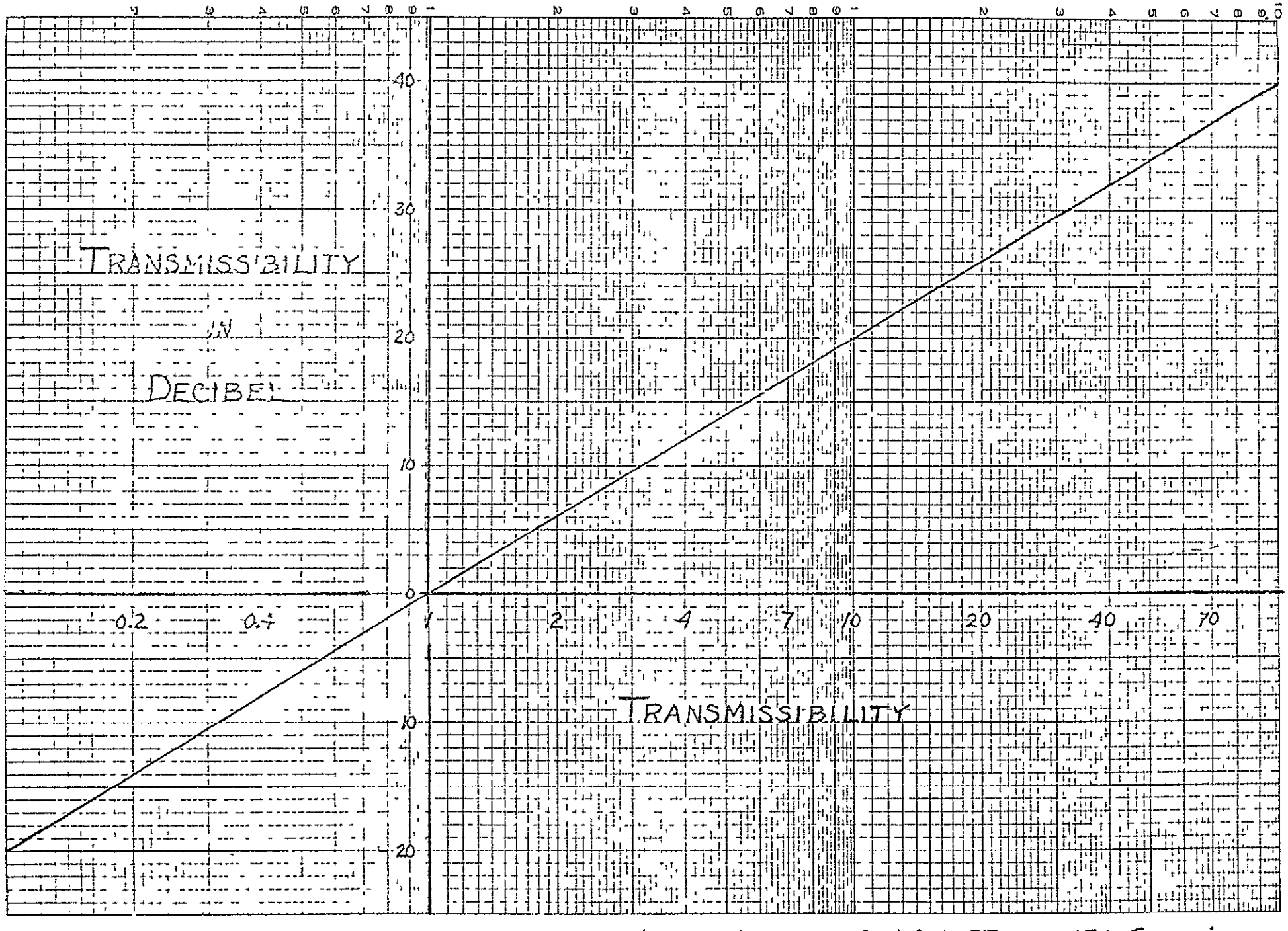

Z
ACCELEROMETER #3
LOCATED ALONG X AXIS
ACCELEROMETER #3
LOCATED ALONG Y AXIS
X
Y
ACCELEROMETER #11
ACCELEROMETER #10

FIG. 3.

SEMI LOGARITHMIC
3 CYCLES X 10 DIVISIONS PER INCH



CONVERSION CHART FIG. 4.