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# FINAL REPORT

# DIGITAL DATA SAMPLING MODULES

## PART I

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# PART I

# DIGITAL DATA SAMPLING SYSTEM

## SUMMARY

The digital data sampling system is a random access, distributed data gathering system. The system will accept data from up to 128 data modules, with each data module handling 8 channels of data for a total of 1024 remotely located data sources. The various data modules are connected along a common command-response-power cable at random intervals in party line fashion and may be addressed by a unique command data address word. Upon receipt of the proper command address word, a particular channel within a particular module will accept analog data from that data source, convert the data to digital form, transmit the response word back to a central location and present it in proper form to a central data processor (computer).

The unique features of this system are: (1) The large degree of circuit and subsystem integration, (2) the small physical size of the remote data sampling modules, (3) the low power requirements of the data modules which is achieved by special low power circuit design and a power switching scheme, and (4) the minimum number of interconnecting cables used to collect the large number of data signals.

The system concept is based upon the development of standardized interchangeable packages with a minimum physical size, minimum number of interconnecting cables, and a minimum power dissipation for each module. The system is to provide maximum flexibility by utilizing a building block approach in which all data modules are basically identical and may be connected at any remote location and addressed in a random fashion

from a central unit. The overall design objectives includes the use of multiplexing techniques to minimize system cabling requirements and the use of nearly identical circuitry for both high level and low level data modules to minimize the development of special integrated circuit arrays, provide maximum utilization of each circuit development, and reduce spare parts requirements for the system.

The design described is based on the extensive use of Metal-Oxide-Silicon Large Scale Integration (MOS LSI) techniques. The utilization of a new low threshold voltage process which has recently been developed allows the design of such a system which combines low power operation with the circuit and process simplicity of MOS transistor technology. The use of LSI-MOS technology has greatly reduced the number of circuit chips required to implement a complete data module and consequently results in reduced size and power and increased system reliability.

## II. SYSTEM ORGANIZATION

The system is organized such that one central unit will control up to 128 remotely located data modules each consisting of 8 data channels. The modules are randomly spaced along a common system cable. The central unit consists of an interface unit, System Controller (S.C.) and a central processor for controlling the remote data modules. The system has been designed to use the Digital Equipment Corporation PDP-8/L as the computer portion of the system; however, other computers may readily be interfaced with the system controller by interchanging the interface circuit boards. The System Controller receives commands from the central processor or

it may be operated under manual control. When under computer (processor) control, the S.C. converts the parallel two level address word from the computer to a serial three level data word, transmits the address word to the remote data modules, and then receives the serial three level data response word from the modules and converts the response word to a two level parallel word for use by the computer. The S.C. also provides for both sync and parity generation and detection as well as a system clock for control of all system timing.

The remote data modules consist of a high level module (0 to +5V analog data) or one of two types of low level modules (±30 MV and ±50 MV). Each of the remote units are basically identical except for the address plug which has a particular module address "wired in," and the amplifiers which control the gain of a particular module and consequently determines the type of module, and the module size in one dimension.

The system block diagram is shown in Figure 1. The command and response lines are common for all of the remote data modules as are the power lines. The command and response lines are twisted, shielded wire pairs for differential operation.

A photograph showing the system is shown in Figure 2. The photograph shows the system controller and PDP-8/L computer mounted in the chassis rack along with the teletype as the input-output device. A portion of the system cable and five high level data modules are also shown on the floor.

## III. SYSTEM OPERATION

### 1. Normal Mode

To obtain data from a particular data source or transducer, the central unit transmits serially to all modules via the command line a digital word containing two synchronization bits, the channel address of the module, the module address and a parity bit. In addition, the command word provides the clock for the data response word. Each module is capable of recognizing its own address by decoding the channel address. Upon receipt of each command word the data module is synchronized by means of the sync bits. During the receipt of the address data, the module will check the address word for proper parity, decode the channel and module addresses and enable the module if addressed. If not addressed, the module operation is inhibited and the module resets itself until the next command word is received. If the parity is correct and the module address corresponds to the "wired" address of that module, the proper circuits are activated from standby to operate mode. The operation then proceeds until the digital data word which represents the analog data from the channel addressed is processed and transmitted back to the central unit. The data response word consists of two synchronization bits, one spare bit, nine data bits, and a parity bit. The parity bit represents the parity of the data word which is transmitted by the module.

If improper parity is received by the module upon receipt of the command word, the data module responds with a special two bit response word at an earlier time than the normal response word to indicate receipt of bad parity from the command word.

The total number of bits which are transmitted for one complete data cycle is 36 bits. The clock rate for the system is variable from a few KHz to about 500 KHz; consequently, the minimum total cycle time is approximately 80 microseconds. In addition to receiving and transmitting data, the 36 bit times for command and response also allow for various internal operations such as power switching, and amplifier and multiplexer settling time.

The reduced number of interconnecting lines is achieved by the use of a three level digital command and response word. Clock, data, and synchronization information are all passed on a single line. The three level word consists of a regular train of negative pulses (module clock pulse) with data and sync pulses superimposed. A system timing diagram showing these various signals is shown in Figure 3.

Figure 3 is the system timing diagram and may be interpreted as follows: The various time slots for system operation are shown at the top of the diagram. The diagram was drawn to show command and response data along with internal module timing for two data modules (Modules A & B). The timing diagram also shows the timing for the two modes of operation, normal and interleave. The first two time lines represent the differential command lines. The top line, command line #1, is defined as a positive true command signal. For this line, the first two bits are sync bits and go from positive to ground or a one-zero-one-zero combination. The input data bits follow the sync bits. The upper portion of the bit pattern is shown shaded to represent the possibility of the data being a "1" or "0". A positive level indicates a logic one while ground level represents logic zero. Between each data bit, a negative clock bit is inserted at all times

except during each sync bit pattern. A combination of one data bit and one clock bit takes one time slot or a total bit time. The general command line bit pattern indicates that a clock bit or negative signal proceeds each data bit except during sync time. The sync bits are unique in that the normal clock time is positive rather than negative and is the only time period when a positive level is not followed by a negative level. The opposite of this is true for command line #2 or the negative true command line which is shown on the second line of Figure 3.

The module response is shown on the last two lines of the timing diagram, and as with the command line, response line #1 is positive true while response line #2 is negative. Sync, clock and data are presented in exactly the same manner as for command words.

The first half or 36 time slots of the timing diagram represent the system for interleave mode of operation and will be discussed in the next section. The second half or 36 bits show the command line output for normal operation.

Following the sync bits (time slots 1 & 2), the first three data bits are used for channel address to select one of eight data channels. The forth bit is used in conjunction with the three channel address bits to provide special control functions such as calibration. The function of each of the first four data bits is as shown below:

| Code | Function |
|---|---|
| 0000 | Zero calibrate (high level) |
| 0001 | Channel #1 |
| 0010 | Channel #2 |
| 0011 | Channel #3 |

| Code | Function |
|---|---|
| 0100 | Channel #4 |
| 0101 | Channel #5 |
| 0110 | Channel #6 |
| 0111 | Channel #7 |
| 1000 | Channel #8 |
| 1001 | Operate module addressed low level |
| 1010 | Full scale calibrate low level |
| 1011 | Zero calibrate low level |
| 1100 | Operate all modules low level |
| 1101 | Turn on module addressed |
| 1110 | Turn off module addressed |
| 1111 | Full scale calibrate (high level) |

The next seven bits following the channel address and control bits are the module address bits, these are decoded and used to select one of the 128 total possible module addresses. The next bit following the module address is the parity bit and is such that the parity of the command word is always odd. If a bad parity (even) is received by the module during the command word input, the normal output from the module is inhibited and a special two bit clock signal is outputed during time slots 21 and 22 as shown dotted on the timing diagram.

When operating in the normal mode, all bits following time slot 14 through time slot 36 are zero bits and are used only to provide clock and timing for the response word. It can be seen on the timing diagram that during normal operation, no clocks are outputed during time slots 19 and 20. This is because these time slots are used for new sync bits when operating in the interleave mode and since

clock signals are not internally generated during the sync time, it is necessary to skip these two clock bits in normal operation to insure that the system timing is correct for either mode of operation.

In summary, when operating in the normal mode, command word data is sent during the first 14 time slots followed by zeros and clocks through time slot 36 with time slots 1 & 2 being sync bits. This is then repeated every 36 bit times. The response word is outputed from time slot 23 through 36 and is proceeded by two sync bits which are identical to the command word sync bits. The parity for both command and response is odd parity. Thus, for each command word cycle of 36 bits one response word is received. A method of increasing (doubling) the data rate without changing the basic system clock and timing will now be described.

2. Interleave Mode

It is possible to operate the system such that two module responses may be received during each 36 bit time cycle. This mode of operation is called the interleave mode of operation. The one basic limitation to this mode of operation is that the same module cannot be interrogated with two successive command words. In other words, a module which is first addressed cannot again be addressed for 36 time bits; however, any other module on the line can be interrogated during the second half of the original command word or after 18 time bits. The interleave mode of operation is shown on the timing diagram of Figure 3. For the illustration shown, Module A is first addressed from time slots 1 through 18. At time slot 19 a new sync bit is transmitted

and Module B is address from time slots 19-36. The circuitry within Module A is set such that it will not receive the new sync bits at time slots 19 and 20 and, therefore, Module A will continue to operate as described in the normal mode of operation with its response being outputed during time slots 23 through 36. Following this data cycle Module A (or any other module except B) can now be interrogated again. Meanwhile, Module B has now received its command word and is proceeding in its cycle of operation. It will not accept the new sync bits at time slots 1 & 2 (which are 19 and 20 for Module B) and, therefore, it will proceed to output its data while Module A (or some other module) is receiving its command word. (Time slots 5-17 of the new command word.) Thus, it can be seen that for this operation the data rate is doubled with no change in the basic system timing. Data on the response line now is nearly continuous as compared to 14 time slots out of every 36 for normal operation. The only restriction for this operation is that the same module cannot be addressed by two successive commands when in this mode.

## IV. DATA MODULE OPERATION (HIGH LEVEL)

A block diagram of the high level data module is shown in Figure 4 and a logic diagram in Figure 5. The detailed operation of the data module in the normal mode is as follows:

The command data word (CDW) is received as a two wire input (Differential) signal by the module input circuitry which is composed of clock and data separators, and clock and sync generators. This portion of this circuitry is powered at all times. Immediately upon detection of

the sync word, power is supplied to the input timing register, data register, and multiplexer circuit by a power switching circuit. Power is applied to the input circuit, output circuit, and reference supply at all times. Upon receipt of the sync pulse the multiplexer has been designed to provide a zero signal (input shorted) to the A/D converter and it remains in this condition until the channel address is received.

The system operates with a two bit sync consisting of a 1-0-1-0 combination which is distinctly unique compared to all address commands.

As may be seen in the system timing diagram (Figure 3), the sync pulse is generated during time slot #1 (TS#1) and continues until the end of time slot #2. Clock pulses are generated as shown to provide a module clock for all subsystems within the data module. The output of the sync detector is applied to the T.R.I. flip-flop which initiates the timing register. This causes a "1" to be entered into the first stage of the timing register during time slot #2. The "1" in the first stage of the timing register will reset the sync flip-flop on the leading edge of TS#3 and cause zeros to be entered into the timing register during each succeeding clock pulse until a new sync pulse is received. The timing register thus functions as a ring counter, advancing the signal "1" down the register with each clock pulse. The timing register provides or initiates all system timing functions and keeps the status of the command word in the appropriate timing stage throughout a complete data acquisition cycle. In coincidence with sync detection, power flip-flop #1 is activated and power is applied to the timing register, data register and multiplexer.

At the beginning of time slot #3, data from the command word begins to enter a seven-bit data register and the parity detector circuit. At

the beginning of time slot #7, the 4-bit channel address word is setting in the first 4 stages of the data register. At this time the timing register will cause a transfer of the data from the data register to the multiplexer holding register and the channel address is stored in the multiplexers holding register of all modules. This will cause the multiplexer to address the appropriate channel and at the same time switch the A/D converter input from the initial zero condition to the analog input data for that particular channel. Switching the analog data to the converter input at this time allows the multiplexed data to settle before data conversion begins at time slot #25.

At the end of time slot #13, the channel address data has passed from the data register and the 7-bit module address data is present in the seven stage data register. At the beginning of time slot #14, the module address data is compared to the module address which is "wired" into the socket for the particular module. If the address does not match (which is the situation for all except one module) the compare circuit will cause an output if not addressed command to occur which resets power flip-flop #1 and removes power from the power switched circuits causing all circuits to return to their original state until the next sync pulse is received.

If a correct address is received by the data module, the parity of the command word is checked during time slot #15. If good parity exists the module continues through a normal response cycle. If a module detects a parity error in the incoming command signal, a parity error output will be placed on the response line during time slot 21 and 22 and then the power will be removed from the module with error so that it will not interfere with another responding module which may be operating normally.

The nature of the bad parity response is two clock pulses as indicated on the timing diagram.

The data module normal response begins with power being applied to the output circuits during time slot #23 and a data response sync pulse begins with time slot #23 and continues through TS#24. This is followed by a spare bit, A/D sign bit, A/D data, and response parity. A start conversion pulse is applied to the A/D converter during time slot #25. The sign bit of the A/D converter is available at the buffer output at bit time #26. For the high level module, this is normally a zero level. The most significant data bit will occur at TS#27. The response parity circuit is reset to zero in coincidence with the end of the sync word and during the response time the parity of the data word is determined so that the parity bit may be inserted at the end of the least significant bit (LSB) of the data word during time slot #35. TS#36 is used to reset all remaining circuits and remove power from the circuits which are power switched. As for the command word operations, the timing register is used to control the various events including the final reset. Only the timing register of the addressed module will proceed through all timing functions, the nonaddressed modules will be reset at time slot #14.

Power switching is utilized to achieve the lowest power requirements without sacrificing system performances. Because of complexity of design, only two power switches are used. The first switch is used to provide power to the circuitry required during receive mode. Power switch #2 provides power basically to the A/D converter which is switched on during response mode if the module is addressed. Because of the nature of the circuitry and the module requirements, the input and output circuitry are not power switched. The input circuitry cannot be power switched

because of the nature of the module requirement (must be on to receive signals) and the output circuit is complementary and thus very low power which does not appear worthwhile to power switch.

The total average power dissipation of a responding high level data module under the conditions described above is approximately 170 milliwatts. A nonaddressed module dissipates approximately half that power or about 85 milliwatts which is the operation of all but one of the modules on the line. If no commands are being sent from the system controller, the power dissipation for a module in standby operation is approximately 45 milliwatts.

The operation of the data module for interleave operation is basically the same as described above. The portion of the module which allows interleave operation is the "disable system reset" flip flop. Its operation is as follows. For every module in the system, this flip flop is reset on power-up. Following detection of the first sync pulse, all modules will proceed through the operation as previously described. During time slot #7, the output of the timing register will set the "disable system reset" flip-flop which will prevent all the modules from detecting any further sync pulses until it is again reset. As may be seen on the logic diagram (Figure 5), in addition to power-up, this flip-flop may be reset by the following signals: Output if not addressed, TS#36, command data bad and TS#23. Thus, a module which received good command data and is addressed cannot be interrogated until TS#36 when the addressed module has completed its normal response cycle. However, a module which has not been addressed will receive an output if not addressed command during TS#14 and, therefore, will be reset and available to receive a new sync

word during bit time 19 if in the interleave mode of operation. Also, if an addressed module received a bad command word and, therefore, does not respond with a normal response cycle, it will still reset the flip-flop at TS#23 and, therefore, be able to receive sync on the next data cycle. Thus, only the module which has been addressed will be inhibited from receiving sync during the second half of the command word and as previously mentioned, the addressed module can detect sync only every other command word.

The high level data module has been subdivided as shown by the dotted lines on the logic diagram. Each of these areas represent an integrated circuit chip as well as a module subsystem. The input circuit was divided into two integrated circuit chips since part of the circuitry required complementary MOS technology to achieve the desired circuit requirements. The various subsystems of the data module as outlined on the logic diagram will now be discussed in some detail.

1. Input Circuit (Complementary) S025C

The command line #1 input to the S025C chip is a tri-level signal with data information being the positive and zero portion and clock the negative. Separation of the data component from the clock is accomplished by the S025C circuitry shown in schematic diagram E-704-2050B, Figure 6.

As indicated, the complementary input inverters are referenced to ground (zero volt) potential, so the inverter Q51 and Q52 is insensitive to data and sensitive to the negative going clock. In other words, ground and +V produce the same output while -V causes

a change in output. The transition point of this input inverter is set at -3 volts to achieve both signal discrimination and optimum noise immunity. The inverter changes state when the clock signal goes more negative than the -3 volt transition level. The output voltage swing of this discriminator inverter is from ground to -V; therefore, the level changing circuit Q49 and 50 is required to obtain the +V to -V output voltage swing to be compatible with the other chips in the module. The two inverters Q47-48 and Q25-26 are output buffers required to drive the load capacitance on this clock output.

Four identical circuit sections are used to generate outputs clock, data, $\overline{\text{clock}}$ and $\overline{\text{data}}$ from the two input command lines. The required biasing on the four discriminating input inverters is defined on the referenced schematic diagram.

The ① $\overline{\text{clock}}$ output of $Q_1$ and $Q_2$ is internally connected to the $\phi 1$ and $\phi 2$ generator (Q27 through Q34) circuit. The inverter Q27 and Q28 device sizing along with diffused resistor R1 provides the proper nonoverlap of these system clocks ($\phi 1$ and $\phi 2$ cannot be negative at the same time). The buffer inverters drive the load capacitance of the clock lines.

The power switch circuitry is required to remove power from system sections when not in use. Power switch #1 (-V*) is receive power, Q39 is the switching device. Power switch #2 (-V**) is response power, Q44 is the switching device. Each of the switches is driven by two buffer inverters, which are required to drive the input capacitance of the switch devices. Input control signals for the power switches come from the S058A chip.

A summary of the S025C chips characteristics is given below:

S025C Characteristics

| | |
|---|---|
| Chip size | 58 x 66 mils |
| No. of devices | 53 |
| Supply voltages | +V = 6.5V ± 1 |
| | -V = 8.5V ± 1 |
| Maximum Power dissipation | $P_{D_{max}}$ = 35 milliwatts (at nominal voltage) |

Inputs

| Input | Pad No. | Cap. Load | Res. Load |
|---|---|---|---|
| C.L. #1 | 14 | 15 pf | 10 meg ohm |
| C.L. #2 | 1 | 15 pf | 10 meg ohm |
| P.S. #1-⑤ | 4 | 10 pf | 10 meg ohm |
| P.S. #2-⑦ | 8 | 10 pf | 10 meg ohm |

Power

| | Pad No. |
|---|---|
| -V | 9 |
| Ground | 16 |
| +V (substrate) | 11 |

| Outputs | Pad No. | Cap. Drive | Rise Time | Fall Time |
|---|---|---|---|---|
| ① $\overline{\text{Clock}}$ | 13 | 30 pf | 0.2 usec | 0.2 usec |
| ② Data | 15 | 30 pf | 0.2 usec | 0.2 usec |
| ③ $\overline{\text{Data}}$ | 3 | 30 pf | 0.2 usec | 0.2 usec |
| ④ Clock | 18 | 30 pf | 0.2 usec | 0.2 usec |
| $\phi 1$ | 12 | 50 pf | 0.3 usec | 0.3 usec |
| $\phi 2$ | 10 | 50 pf | 0.3 usec | 0.3 usec |
| ⑥ -V* | 5 | 200 pf | 1.5 usec | 2.0 usec |

| Outputs | Pad No. | Cap. Drive | Resistance | Fall Time |
|---|---|---|---|---|
| ⑧ -V** | 6 | 200 pf | 1.5 usec | 2.0 usec |
| ⑨ Output Drive | 7 | 30 pf | 0.3 usec | 0.3 usec |

2. Input Circuit (P-Channel) S058A

The S058A circuit performs the following functions within the data module:

a. Command word sync detection

b. Timing register initiate pulse generation

c. Detection of bad command word data

d. Command word parity error detection

e. Control signal generation for receive power switch

f. Control signal generation for output enable and response power switch

g. Generation of delayed data signal.

The S058A circuit schematic is shown on drawing E-704-2050 and is given in Figure 6. All device numbers mentioned in the following discussion refer to this schematic diagram.

Command word sync detection is accomplished by the three gated flip-flops (Q5-Q30). This circuit counts data pulses as they enter the flip-flops through Q5. A negative going signal on the command line will generate a clock pulse which resets the flip-flops. Each data pulse which is not followed by a negative clock will advance down the flip-flop counter such that a "1" output is produced by the circuit for a 1010 input. This occurs only during sync time for the command word. At any other time, a data bit or "1" is followed by a negative clock bit which resets the sync detector

and prevents an output. The output of the sync detector is produced as the second zero of the 1010 combination is entered into the circuit. The output of the sync detector is used for two purposes. First, it is entered in conjunction with delayed data into the nand gate (Q32-Q34) to set the power flip-flop #1 and apply receive power to the module. Second, it is entered in conjunction with delayed data and the interleave mode inhibit flip-flop output to generate a timing register initiate pulse through the nand gate formed with Q71-Q74. This pulse sets the TRI flip-flop to a state which will cause a "1" to enter the first stage of the timing register. This TRI signal will be generated every time a sync signal is present on the command line if the system is in normal mode and every other sync signal if in interleave mode. The TRI flip-flop is reset after the "1" is entered into the timing register and is fed back as output pulse TS#3 to Q92.

For proper operation, a sync pulse, a TRI pulse and a power switch #1 control signal is produced each time a normal mode sync is received and is produced during the second half of the second time slot which is when the 1010 signal enters the second zero. Both TRI and power switch #1 control signals are bootstraped push-pull output circuits to provide a low impedance output to the circuits it must drive. This drive capability is primarily to drive the capacity loading which is seen by the output.

Bad command data is detected by the circuitry of Q150 through Q183. Data on the two command lines CL#1 and CL#2 are compared every half-bit time and when they are not the exact compliments of one another, the circuit indicates reception of bad command data. For bad data,

a special output is produced at TS 21 and 22 and then both power switches are turned "OFF" at TS #23 by this bad data command. The system then holds in standby mode until a new command sequence is initiated.

A parity error in the command data information is detected by the circuit of Q97 through Q115. This circuit maintains continuous indication of the parity state (odd or even) of the received command word. The system controller normally sends an odd parity, so if even parity is received, the module indicates a parity transmission error. This error is gated with bad command data to also turn power switches "OFF" at TS #23.

The data delayed circuit is used to delay the data information sufficiently to insure that it is still negative after clock $\phi 1$ goes positive. This is accomplished by the inverter Q1 and Q2, and the output buffer circuit of Q18 through Q23.

The receive power (-V*), is controlled by the power flip-flop which consists of devices Q35-Q43. As previously mentioned, the power flip-flop is set to the power "ON" condition by receipt of the command word sync. It may be reset by one of several signals. For a normal response it is reset by the timing register at TS #36 through Q46. If the module is not addressed, the power is reset by the "output if not addressed" signal from the Data Register (S021A) through Q44. If the command data is bad the power is reset by the timing register at TS #23 through Q49. In addition to these reset signals, the power flip-flop is initially set to the off condition by the application of system power through the RC circuit into Q41.

The response power control circuit (Q116 - Q149) is used to control the output enable signal and provide power to the A/D converter (-V**)

if the module is addressed and is to respond. As with power flip-flop #1, this circuit is initially reset to "0" by means of an RC circuit during power up into the control flip-flop (Q117). The application of power to this circuit can be inhibited by means of a "turn off" command which is received from the multiplexer and applied to Q125. Once this command has been sent, the only way the module may again respond is by receipt of a "turn on" command to Q118 or by recycling power up through Q117. If a "turn off" command is not sent, the power control circuit will enable output from the module during a normal cycle at TS 23 time through Q135 and is reset at TS #36 through Q139. However, if bad command data was received the power is applied at TS 21 time through Q130 and then is turned off at TS 23 time through Q146. This allows the special two-bit bad data response signal.

The various functions described above constitute the operation of the S058A chip. One change which was made to the system during module testing was to do away with power switching of the positive voltages in the module; hence, only the control signals which provide for switching the negative voltages are used. (Q54 and Q149 are no longer connected to outputs.) The negative voltage is actually switched by the power switches in the S025 chip. The positive voltages which were power switched in the various chips are now tied permanently to the +V input power. Switching the positive voltage resulted in no power saving and only complicated the interconnect problem.

A summary of the S058A chip characteristics is given below:

| | |
|---|---|
| Chip size | 82 x 101 mils |
| No. of devices | 185 |

| | |
|---|---|
| Supply voltages | +V = 6.5 ±1 volt |
| | -V = 8.5 ±1 volt |
| Power dissipation | $P_{D_{max}}$ = 23 milliwatts (at nominal voltage) |

Inputs

| Input | Pad No. | Cap. Load | Res. Load |
|---|---|---|---|
| Turn-on | 1 | 10 pf | 10 meg ohm |
| Output if addressed | 2 | 10 pf | 10 meg ohm |
| Turn off | 3 | 10 pf | 10 meg ohm |
| TS #21 | 4 | 10 pf | 10 meg ohm |
| Data 2 | 6 | 10 pf | 10 meg ohm |
| $\overline{\text{Clock 1}}$ | 7 | 10 pf | 10 meg ohm |
| Clock 4 | 8 | 10 pf | 10 meg ohm |
| $\overline{\text{Data 3}}$ | 9 | 10 pf | 10 meg ohm |
| TS #7 | 10 | 10 pf | 10 meg ohm |
| TS #36 | 11 | 10 pf | 10 meg ohm |
| $\phi$1 clock | 12 | 15 pf | 10 meg ohm |
| TS #3 | 13 | 10 pf | 10 meg ohm |
| $\phi$2 Clock | 15 | 15 pf | 10 meg ohm |
| TS #15 | 16 | 10 pf | 10 meg ohm |
| Output if not addressed | 23 | 10 pf | 10 meg ohm |
| TS #23 | 24 | 10 pf | 10 meg ohm |

Power

| | |
|---|---|
| -V | 18 |
| Ground | 17 |
| +V (substrate) | 20 |

| | Pin No. | Cap. Drive |
|---|---|---|
| Outputs | | |
| P.S. #2 inverter - 7 | 5 | 30 pf |
| T.S. Initiate | 14 | 40 pf |
| Data Delayed | 19 | 40 pf |
| P.S. #1 inverter - 5 | 21 | 30 pf |

3. Timing Register S065

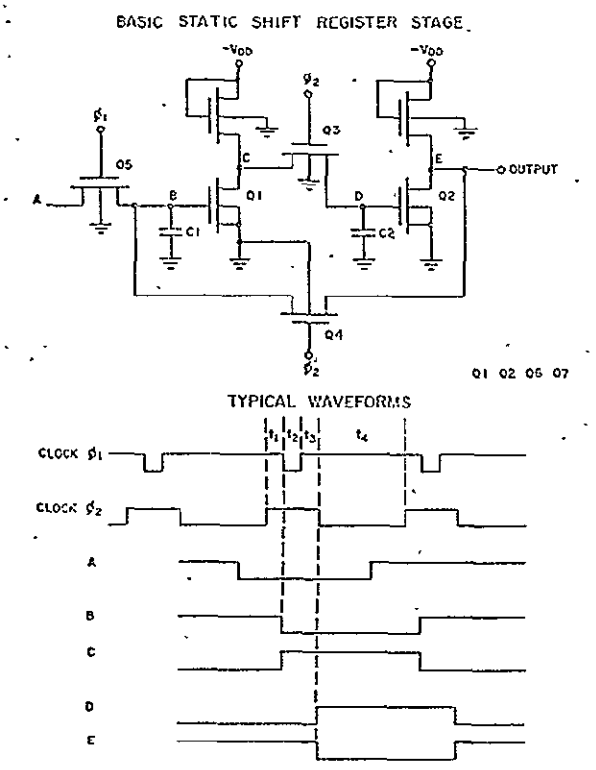
Prior to a discussion of the operation of the module timing register, a brief discussion on the basic operation of a single stage MOS shift register may be of some help in understanding the more complex timing register.

The basic shift register stage uses a regenerative d.c. stable flip-flop circuit configuration which takes advantage of the capacitive storage of the MTOS transistor. Two phase clocks are utilized to transfer data from stage to stage during each phase of clock.

Some static registers require only a single external clock into the device. However, in these cases, the other phase is generated internally. A typical shift register stage is illustrated in the following figure. The clock waveforms are shown as a timing reference.

Input data to the register appears as a negative level at point A. During $t_1$ time period, $\phi_2$ is at ground. This turns off Q3 and Q4. Information stored on capacitors C1 and C2 remains unchanged, and the register output appears at point E. During $t_2$, data is transferred to the gate of Q1 (Point B) by virtue of $\phi_1$ going negative. C1 charges to the negative input, turning on Q1. Point C now approaches ground due to the negative potential at Point B.

At $t_3$, $\phi_1$ returns to ground, cutting off Q5, but C1 remains charged negative holding the drain of Q1 (Point C) near ground. At $t_4$, $\phi_2$ goes negative, Q3 turns on bringing the gate of Q2 to the potential of the drain of Q1 (Point C). This turns Q2 off and Point E now rises to within one threshold voltage of $V_{DD}$. This voltage is coupled back through Q4, to the gate of Q1, latching Q1 in the on state. For transferring a logic "0" into the register the sequence is repeated starting with a ground signal at point A.




*Typical Static Shift Register*

A complete schematic of the timing register is given in Figure 7. Although it appears complex, the basic operation is as described for the single stage register. As previously discussed, when sync is received by the input circuit (S058) a negative signal (TRI) is applied to the input of the timing register into device #5. At this time as shown on the module timing diagram, the Phase I ($\phi 1$) clock is negative and is applied to the gate of device #5. This causes a negative voltage (logic "1") to be applied to the gate of device #7 and causes its drain to go to +V. This signal is then transfered through device #8 to the gate of device #12 as $\phi 1$ goes positive and $\phi 2$ becomes negative. Consequently at the beginning of time slot #3, the negative signal from the TRI flip-flop in the S058 chip is transfered to the output of the first stage of the timing register. This output is then applied back to the TRI flip-flop in the S058 chip and the flip-flop is reset to zero. Consequently, each succeeding clock pulse will enter a zero into the first stage of the register and shift the initial "1" which was entered one stage further down the register. Thus, the timing register functions as a ring counter shifting the single "1" down the register with each clock pulse. Outputs are taken from the timing register as parallel push-pull outputs to drive the required circuits for the required timing functions. In order to keep track of the 36 time slots of the system, 32 register stages are required. The four additional time slots are taken by the sync bits during which time no clock pulses are generated. If the module is in interleave mode, 4 sync bits are used each 36 time slots; however, for the normal mode, 2 sync bits are used and two blank time slots when no clock pulses are transmitted, consequently, for either mode

only 32 clock pulses are produced each 36 time slots.

An additional feature which was added to the timing register which is not a part of a standard shift register is a reset line. The purpose of this line is to insure that all other stages are set to zero when the first "1" is entered into the first stage. Since the chip is power switched on each data cycle, it is necessary to reset the register to insure that the latter stages do not power up in a "1" state and cause timing problems. To accomplish the reset, the TRI pulse is applied to the reset input simultaneously with the normal input through device #1. This enters the negative signal onto all of the reset transistors (devices 9, 19, 27, etc.) and forces the outputs of all stages except the first stage to a zero output. Thus, each time power up is applied to the chip during sync, it is also reset as described.

As indicated on the schematic, there are 13 output signals from the timing register. The function of each of these outputs is indicated on the timing diagram and is summarized below for convenience.

| Output | Function |
|---|---|
| TS #3 | Reset the TRI flip-flop after sync |
| TS #7 | Load multiplexer address, set interleave inhibit flip-flop |
| TS #14 | Check module address in data register |
| TS #15 | Check parity of command word |
| TS #21 | Start output for bad parity |
| TS #22 | Set response sync flip-flop in output chip |
| TS #23 | Stop output for bad parity, start output for good data |

| Output | Function |
|---|---|
| TS #24 | Reset response sync flip-flop |
| TS #25 | Start A/D converter |
| TS #26 | Output A/D sign bit |
| TS #27 | Set output data flip-flop for A/D data |
| TS #35 | Reset output data flip-flop, output response parity |
| TS #36 | Reset module, power off |

A brief summary of the timing register chip characteristics are given below:

| | |
|---|---|
| Chip size: | 58 x 94 mils |
| Number of devices: | 282 |
| Supply Voltage: | +6.5, -8.5 |
| Power Dissipation: | 40 milliwatts nominal |
| Input pads: | Input, Reset, $\phi_1$, $\phi_2$ |
| Power pads: | +V, -V, GND |
| Outputs: | 13 outputs listed above |

4. Data Register and Address Decode S021A

The basic purpose of this circuit is to accept the input data from the system controller, present the multiplexer address data to the multiplexer, accept the module address, compare it with the "hardwired" module address and determine whether or not the addresses match. A schematic of the circuit is shown in Figure 8. The register portion of the circuit consists of devices 1-57. This is a 7-stage register and functions basically the same as the timing register. The first 4 stages have push-pull outpoints such that the 4-bit multiplexer

address may be transferred to the multiplexer in parallel once it is setting in the register in the proper position. The first or least significant bit of the multiplexer address will be entered into the first stage of the data register during time slot #3 as with the timing register. By time slot #6, the first data bit is setting in the forth stage, second data bit in the third stage, etc. Consequently, the leading edge of the pulse from TS #7 is used to cause a parallel transfer of data from the data register to the holding flip-flops in the multiplexer. During the second half of TS #7 the first bit of the module addressed is entered into the data register and by TS #13, the entire 7-bit module address word is setting in the seven stage data register with the first bit in the seventh stage. At this time a bit-by-bit comparison is made by compare gates such that the hard wired level of D1 is compared to the first bit, D2 to the second bit, etc. In order for the address to match, the level at D1 must be ground or negative (not positive) if a "1" is present in the module address for the first bit. The same is true for each of the other bits. Thus, at the beginning of bit time #14, the status of each of the compare gates are checked and if every bit matches an "output if addressed" pulse is obtained. If any of the bits do not match, an "output if not addressed" pulse is obtained. This pulse is then used to turn off the unaddressed module until the next sync pulse is received. The "output if addressed" pulse is used in conjunction with turn off and turn on commands to control the turn-off and turn-on function of an addressed module.

The operation of the compare circuit for a one bit comparison is as follows: Assume a "1" was entered as the first bit and is

now setting in the seventh stage of the timing register. This causes a negative voltage to be applied to the gate of device #112 and positive to the gate of device #111. Now if this is to match, a negative voltage or ground must be applied to D1 input. If this is the situation, negative is applied to device 110 and positive to device 113. With these conditions the gate composed of devices 110-113 is off causing a negative toltage to be applied to device 116. If all other bits match, devices 116, 117, and 118 are all on and a positive voltage is then applied to device #60. This is then inverted and a negative signal is applied to device #64. With negative voltage on the gate of device 64, the gate composed of devices 64, 63, and 62 will turn on with a signal from the timing register during TS #14. This will then cause an "output if addressed" pulse at this time. If the "hard wired" data level at D1 or any other input didn't match, the opposite effect would take place and an output if not addressed is presented.

A summary of the data register-decode circuit characteristics is given below:

| | |
|---|---|
| Chip size: | 53 x 94 mils |
| Number of devices: | 128 |
| Supply Voltage: | +6.5, -8.5 ± 1.0 volt |
| Power Dissipation: | 10 milliwatts nominal |
| Inputs: | Delayed data, $\phi_1$, $\phi_2$, D1-D7 |
| Outputs: | Multiplexer data bits 1, 2, 3, and 4 |
| | Output if addressed |
| | Output if not addressed |

5. Multiplexer S018

The module multiplexer is used to select one of eight data channels and switch the analog signal from the appropriate channel to the input of the A/D converter. In addition to this, the multiplexer provides a zero calibration signal, 80 percent full scale or 4.00V calibration signal, turn on, and turn off signals.

A schematic of the multiplexer is given in Figure 9. The circuit consists of 4 holding flip-flops to accept the multiplexer data, 16 four-input logic gates to decode the multiplexer address data and 10 analog switch pairs. For the high level data module the multiplexer is operated single-ended and, therefore, the switch pairs are tied in parallel to provide a single pole switch; however, to avoid a second layout for the low level differential multiplexer, the analog switches are layed out as switch pairs and then connected in parallel for single-ended high level operation.

The operation of the multiplexer is as follows: The data register output is connected to the four input lines of the holding flip-flops. The first or least significant data bit of the multiplexer address is connected to input #4, device #34. The second bit to input #3, device 24, etc. As previously mentioned in the discussion on the data register, at the beginning of TS #7 the multiplexer address is present in the appropriate stages of the data register; therefore, as the negative TS #7 pulse is applied to the multiplexer to the gates of the input transfer transistors (4, 14, 24, 34), the data levels at the inputs are transferred into the holding flip-flops. Once the data has been entered into the flop-flops and the TS #7 pulse returns positive, the data levels at the input lines are locked out and only the data

code which was transferred is held by the input flip-flops. The only method of changing the data code is to enter another load pulse or activate the reset input. If the reset is activated, all flip-flops are returned to the zero state. During system operation, the reset line is activated each time a sync pulse is received. This returns all flip-flops to the zero state and presents a zero calibrate signal at the output of the multiplexer. At TS #7, the module address is loaded and the multiplexer switches the appropriate data channel. This operation has the effect of shorting the input of the A/D converter to zero prior to the selection of each data channel and, thus, assures that the input is never floating.

It will be noted on the schematic that the multiplexer contains 16 four-input nand decoding gates; however, only 12 of these are used in system operation. The various codes and their function are shown below:

| Multiplexer Data Code | Function |
|---|---|
| 0000 | Zero calibrate (bias) |
| 0001 | Channel #1 |
| 0010 | Channel #2 |
| 0011 | Channel #3 |
| 0100 | Channel #4 |
| 0101 | Channel #5 |
| 0110 | Channel #6 |
| 0111 | Channel #7 |
| 1000 | Channel #8 |
| 1101 | Turn on |
| 1110 | Turn off |
| 1111 | Full scale calibrate (ref.) |

It will be noted on the schematic that the circuit consisting of devices 141-145 may be used to directly control the zero calibrate or bias switch. This circuit is used to hold the output at zero when the switched voltage to the multiplexer is removed. Since the control signal ($\overline{P7}$) is the complement of the switched voltage (-V*) this circuit is activated any time the switched power is removed from the multiplexer chip. Since in normal operation, this is redundant to the reset function, this portion of the circuit need not be used and was not used in the high level data modules; however, it is available on the chip if required for other uses. The circuit does have one disadvantage, the switching time of this circuit is slightly faster than the flip-flops and decode gates; therefore, it switches the zero calibrate signal on slightly before the decode gates release the previously held analog signal and the effect is to momentarily load the addressed channel by shorting it through the bias switches to ground. For this reason, the circuit was deactivated by connecting the input to +V when it was interconnected in the module.

An example of the multiplexer operation to address channel #1 is as follows: Following receipt of the reset signal, all flip-flops are set to zero which places Q1, Q2, Q3, and Q4 positive. When the input data for channel #1 (0001) is entered, Q1-Q3 remain in this condition while Q4 is set to -V as follows: The negative signal at input #4 is transferred through device #34 to the gate of device #35 which was previously connected to +V during reset time by device #40. This negative signal is also applied to the gate of device #39. The negative signal at the gate of device #35 is inverted and a positive signal is then applied to the gate of device #36. These

complementary signals applied to opposite inputs of the holding flip-flop sets Q4 negative and $\overline{Q4}$ positive. In order to turn on Channel #1 switch (devices 121-122), it is necessary to apply a negative voltage to the gate of the analog switch. The logic gate which consists of devices 41-45 have the following inputs: Q1, Q2, Q3, and $\overline{Q4}$. Since these are all now positive, the gate is held off and a negative voltage is applied to the analog switch turning it on. All other logic gates have at least one negative input, thus, turning them on which applies a positive voltage to each respective analog switch holding it off. The selection of any other data channel is similar to that described for channel #1. The output signals for module turn-on and turn-off are taken directly from the decode logic and are negative signals when true.

A brief summary of the multiplexer characteristics are given below:

| | |
|---|---|
| Chip size: | 78 x 80 mils |
| Number of devices: | 145 |
| Supply Voltages: | +6.5, -8.5 ±1.0 |
| Power Dissipation: | 12 mw nominal |
| Switching Time: | 5 μsec nominal |
| On Resistance: | 300n (parallel switches) |
| Off Resistance: | 10 meg. min. |
| Error Contribution: | 5 mv max. |
| Inputs: | Data 1, 2, 3, 4 - load, Reset, Channels 1-8 |
| Power: | +V, -V, GND |
| Outputs: | Analog out, turn on, turn off |

6. Multiplexer Overvoltage Protection S019-B1, S019B2

Since the analog input signals to the multiplexer are from sources external to the system, it is necessary to insure that these signal sources cannot present an input which would permanently damage the data module. An input protection circuit has been incorporated into the module which will protect the module for overvoltages up to ±30 volts. This circuit consists of diffused 1 Kohm resistors and back-to-back 7 volts zener diodes. The resistors are fabricated on a separate silicon wafer and electrically isolated from the substrate of the zener diodes. This provides complete isolation for the resistors and insures that they do not conduct into their substrate. The network has been tested for the stated overvoltage with satisfactory results. No damage will occur to the module with a permament 30 volt overvoltage from a very low source impedance. The accuracy of other channels within the module are affected by positive overvoltages.

For positive overvoltages in excess of about 15 volts, the output of all channels will indicate full scale; however, the module will be fully satisfactory once the fault voltage is removed. For negative overvoltages up to -30 volts no effect is indicated on any of the nonfaulted channels.

Both resistor and zener diode network are packaged with two chips in a 16 lead flat-pac.

7. Analog-To-Digital (A/D) Converter S022

The function of the A/D converter is to accept the analog signal from the multiplexer and convert it to an 8-bit digital equivalent. The basic components of the A/D converter consist of an MOS timing-logic-switching chip (S022), a thin film D/A ladder network, a voltage comparitor and reference supply. A block diagram of the converter is shown in Figure 10. A logic diagram of the converter may be seen in Figure 5 and a schematic of the MOS logic chip (S022) is given in Figure 11.

The A/D converter is basically a 9-bit successive approximation type converter; however, only 8 bits are used for the high level data module. The 9th bit is used as the sign bit for the low level data module as will be explained later. This was done to eliminate two separate designs for the A/D converter chip. The ladder network consists of two 5-bit constant impedance type ladder network chips giving the capability of 10-bit operation; however, only 8 or 9 of the ladder bits are used in this system. The comparator and reference supply circuits are the only bipolar transistor circuitry used in the high level module. The comparator is an integrated bipolar circuit which was developed specifically for this application. Its outstanding characteristic is its very low power operation (approximately 20mw) for relatively high speed performance. A schematic of the comparator circuit is given in Figure 12. The reference supply is a hybrid circuit and consists of a precision reference zener diode, appropriate film resistors and chip capacitors and two operational amplifier chips all combined in a single 5/8" x 5/8" flat-pac. The entire A/D converter consists of only 4 flat-pacs contained on a 2" x 2" PC board.

An examination of the A/D converter block diagram, and the S022 schematic shows that the MOS chip consists of a 10 bit timing register, 9 holding flip-flops, and 9 ladder switch pairs. The output of each ladder switch is connected to the appropriate leg of a 2:1 resistive ladder network. Depending upon the state of the holding flip-flops, the ladder switches connect the ladder legs to either ground (Ref. 1) or to the positive reference voltage (Ref. 2). The nature of the ladder network is such that if the first switch (MSB) connects the MSB ladder leg to the reference voltage, and all other switches connect the ladder legs to ground, one-half the reference will be present at the ladder output which is then connected to one input of the voltage comparator. With the second switch high or at reference voltage and all others at ground, ¼ of the reference will be outputed to the comparator. First and second high and all others at ground provides 3/4 of the reference voltage, etc. Thus, it may be seen that some binary increment of the reference voltage is outputed to the comparator for each combination of switch positions. Operation of the A/D converter for one data conversion is as follows: At the start of conversion, a logic "one" is entered into the first stage of a 10-bit shift register (time register) by means of the reset input. This in turn enters a "one" into the first holding flip-flop (FF) of the data register, which results in connecting the most significant bit of the ladder network through the ladder switch to the reference voltage. As clock pulses advance the "one" down this register, 10 time intervals are generated. During each of these time intervals, one bit of the digital output is formed in the data register, starting with the most significant bit. A data bit is first set. The voltage thus produced by the ladder

network is compared to the analog input voltage by the voltage comparator. If the output of the ladder exceeds the input voltage, the data bit is reset; otherwise, it remains set. The "one" is then advanced in the shift register and the next bit is determined in a like manner. When the "one" has advanced the full length of the timing register, the binary states of the holding flip-flops in the data register represent the binary equivalent of the input signal when compared to the reference voltage. Real-time serial conversion is obtained by monitoring the state of the A/D flip-flop, which is controlled by the voltage comparator. Both the data and its compliment are available from the A/D output flip-flop. The complement data is used for the most significant bit to achieve the sign bit as specified for the bipolar A/D in the low level modules.

The specific way in which the 8-bit high level A/D is connected for the system is slightly different than discussed above. For eight bit operation, the MSB position of the ladder network is connected to the second ladder switch position of the logic chip (devices 104-105). Thus, when a start command is given and the MSB is set high, all ladder legs are still connected to ground which causes the ladder output to be zero. Since the analog input is always zero or positive, the MSB position may be used as a sign bit, but will normally indicate the same sign (positive data). The exception to this is if the voltage comparator has a significant input offset voltage, the zero output from the ladder may appear to be positive with respect to an input signal near zero. Under this condition, the sign bit would indicate a negative input signal; however, an input voltage of a few millivolts positive will reset the sign bit positive and it will remain such for

all positive input signals from approximately zero to full scale. With the ladder connected as discussed above, the first clock pulse after the start command will advance the "1" in the timing register to the second stage. This now connects the MSB of the ladder network to the reference voltage and ½ scale output is produced. The remaining operations are as discussed above. Hence, it can be seen that the only difference in the high level A/D from a standard successive approximately converter is that the first time slot actually produces an equivalent sign bit and the second time slot produces the most significant bit of the data word.

The module specification for analog input range for the high level data module requires +5 volts plus 10 percent overrange capability. To meet this requirement, the reference supply voltage was set to 5.5216 volts. With this reference supply, each bit of the 8-bit system is equivalent to an input of approximately 21.57 millivolts. Full scale output then just triggers for an input voltage of 5.489 volts with nominal mid-range full scale being 5.500 volts.

The accuracy of the high level data module is primarily dependent upon the accuracy of the A/D converter since the only other significant source of error is the multiplexer and this error is held very low by selection of multiplexer chips (<5 mv). The accuracy of the A/D converter is determined primarily by the accuracy of the ladder network and comparator. Since the ladder switch "on" resistance must be included in the ladder network, the variation of this switch resistance is the primary source of error introduced by the MOS chip. The nominal resistance for the ladder switches was designed to be 400 ohms. Consequently, the ladder network itself was specified for

10-bit accuracy (±2.5 millivolts for 5.516 full scale) with resistance legs of 10.0K and 19.6K ohms. With the 400 ohm switch resistance, the ladder network then becomes a 10K-20K 2:1 ladder. Any deviation from the 400 ohm "ON" resistance of the ladder switches then becomes a source of error. The resistance of the ladder switches depends, in addition to the original geometry design, upon the switch bias voltage which is a function of supply voltage, the temperature of the chip, and initial variations from chip to chip because of process variations.

A good portion of the last variable is removed by selection of chips. This is done by measuring the switch resistances with the nominal power supply voltages prior to connecting the chip into the circuit. A table is given below showing the measured "ON" resistance for one of the A/D logic chips for two different supply voltages.

Device #47

| Switch Position | Resistance to $R_1$-ohms | | Resistance to $R_2$-ohms | |
|---|---|---|---|---|
| | -V=8.0 | -V=9.0 | -V=8.0 | -V=9.0 |
| MSB | 415 | 375 | 425 | 390 |
| 2 | 413 | 365 | 421 | 390 |
| 3 | 400 | 360 | 408 | 365 |
| 4 | 406 | 362 | 410 | 370 |
| 5 | 410 | 370 | 405 | 365 |
| 6 | 406 | 371 | 407 | 362 |
| 7 | 415 | 374 | 408 | 361 |
| 8 | 417 | 370 | 415 | 368 |
| LSB | 360 | 325 | 325 | 300 |

As may be seen, the switch resistances have an initial variation from switch-to-switch due to processing as well as a variation due

to supply voltage; however, all of these variations when computed in terms of the total 20K ohm ladder resistance are well within the accuracy requirements of the system. The specified accuracy for the module is ±0.5 percent of full scale (±27.5 millivolts). Typical measurements of A/D accuracy indicate maximum errors of ± 1 bit or 21.6 millivolts including temperature variations of from -20 to +85°C. Each of the high level data modules were tested for accuracy by measuring the analog input which just trips the LSB of a specific code (cross-over-point) at 23 different points. These were chosen as the more critical points when the majority of the ladder switches are switching from R1 to R2 or at equal increments of analog input signals. The greatest source of error for the ladder switches are the most significant bits. Variations in the last 3 or 4 bits do not greatly effect the overall accuracy of the ladder network. A table is given below which slows the digital codes which were checked, the expected or theoretical analog input, the measured input and the error for a particular module.

| Digital Output Code | Expected Analog Input | Measured Analog Input | Error Millivolts |
|---|---|---|---|
| 00000001 | 0.01078 | .002 | -9 |
| 00000010 | 0.03235 | .024 | -8 |
| 00000011 | 0.05392 | .046 | -8 |
| 00000100 | 0.07549 | .069 | -6 |
| 00001000 | 0.16177 | .158 | -4 |
| 00010000 | 0.3343 | .332 | -2 |
| 00010111 | 0.4853 | .480 | -5 |
| 00100000 | 0.67941 | .680 | +1 |
| 00101110 | .98138 | .979 | -2 |
| 01000000 | 1.3696 | 1.373 | +3 |
| 01000111 | 1.5206 | 1.518 | -3 |
| 01011100 | 1.9735 | 1.971 | -2 |

| Digital Output Code | Expected Analog Input | Measured Analog Input | Error Millivolts |
|---|---|---|---|
| 01101000 | 2.2322 | 2.233 | +1 |
| 01110011 | 2.4696 | 2.466 | -3 |
| 01111110 | 2.7068 | 2.702 | -5 |
| 01111111 | 2.7284 | 2.725 | -3 |
| 10000000 | 2.7500 | 2.747 | -3 |
| 10001010 | 2.9657 | 2.962 | -4 |
| 10100010 | 3.4833 | 3.479 | -4 |
| 10111001 | 3.9794 | 3.973 | -6 |
| 10111001 | 3.9794 | 3.973 | -6 |
| 11010000 | 4.4755 | 4.468 | -7 |
| 11101000 | 4.9931 | 4.983 | -10 |
| 11111111 | 5.4892 | 5.478 | -11 |

As may be seen, the error for this module is well within ± ½ LSB. The majority of the error is a result of comparator offset, which could be adjusted out if provisions were made for a potentiometer on the A/D converter board. As a result of all the measurements of A/D converter accuracy, it is felt that the most desirable design change would be the addition of an offset or null potentiometer. As may be seen on the schematic diagram, the comparator does have provisions for null adjustment by external means.

In summary, the performance of the A/D portion of the module is generally very satisfactory and well within the system accuracy requirement. The operation and accuracy of the A/D converter is within the required tolerance over a bit frequency range of from a few hertz to approximately 700 KHz.

A brief description of each of the A/D converter building blocks is given below:

a. S022 Logic chip

| | |
|---|---|
| Chip size: | 54 x 80 mils |
| Number of devices: | 197 |
| Supply voltage: | +6.5, -8.5 ±1.0 |
| Power Dissipation: | 25mw nominal |
| Ladder Switch | |
| Resistance: | 400Ω nominal |
| Inputs: | $\phi_1$, $\phi_2$, start (reset), $\overline{\text{reset}}$ (for test only) Register In (for test only), Comparitor Input, Reference 1, Reference 2. |
| Power: | +V, -V, ground |
| Outputs: | Ladder switches MSB-LSB, (9 switches), serial data out, serial $\overline{\text{data}}$ out |
| Package: | 24 lead flat-pac |

A microphotograph of the S022 chip is shown in Figure 13.

b. S020 Comparator

| | |
|---|---|
| Chip size: | 30 x 60 mils |
| Devices: | 14 transistors (bipolar), 18 resistors |
| Supply Voltage: | +6.5, -8.5, +12 ±1.0 |
| Power Dissipation: | 20 milliwatts nominal |
| Switching Time: | 1 microsecond maximum |
| Inputs: | Inverting Input, Noninverting Input + Null, - Null |
| Power: | +6.5, -8.5, +12, GND |
| Outputs: | Comparator Output |
| Package: | 14 lead flat-pac |

c. SD2017 Ladder Network

| | |
|---|---|
| Chip size: | Approximately 100 x 100 mils (2 chips required) |
| Devices: | 10 resistors each chip $R_1$ = 19.6K |
| | $R_2$ = 10K |
| Voltage Range: | 0-10V |
| Power Dissipation: | Approximately 1.0 milliwatt for 5.5V reference. |
| Package: | 22 lead flat-pac (2 chips per package) |

A microphotograph of the ladder chip is shown in Figure 14.

d. Low Power Reference Supply 101535-RS1A

Since the reference supply is a hybrid circuit rather than a single integrated circuit chip, a summary of chip characteristics cannot be given as above; however, a brief description of the total hybrid package follows:

Figure 15 shows the schematic of the calibration and reference source. Positive feedback is incorporated (loop gain < 1) around A1 to constant current bias the precision, low TC, low current, zener diode CR1. This use of positive feedback effectively isolates the positive 12 volt supply and any variations from affecting the current through the zener. Amplifier A2 buffers the output circuitry, prevents loading of the zener, and also provides current drive capability. Care must be made in selecting the gain of A1 to insure that the amplifier remains in its active region. Also, proper compensation must be used to insure that -6 db/octave roll off is maintained through unity gain.

Since the amplifiers A1 and A2 input bias and zener bias

currents are low, the use of large value resistors can be used. This will then guarantee low quiescent power dissipation. Output #1 is the reference voltage for the Data Acquisition System A/D converter and output #2 provides the calibration signal. Note that excessive loading of output #2 must be prevented. In the case where loading effects must be accounted for another buffer amplifier or emitter follower stage must be added. However, in this case the calibration load was 10 megohms or greater.

The reference and calibration source was constructed using Hybrid techniques and packaged in a 5/8" x 5/8" x 0.18" 20 lead flat-pac (see Figure 16).

The original design incorporated the μA 735 operational amplifier chip for both amplifier requirements; however, because of high output impedance problems from the A/D reference output, the output amplifier was changed to a μA 741 chip. This change resulted in completely satisfactory performance. The measured characteristics of the device were very similar to those calculated in the original analysis.

Finally then, a low power precision calibration reference source has been designed, exhibiting $\leq$ 0.1% error, dissipating approximately 18 milliwatts, with excellent line regulation. Loading effects were negligible as the Output 1 voltage terminal could drive 1K ohms with no adverse loading error, and provide sufficiently low impedance at the 500 KHz switching rate of the A/D converter to achieve the overall module accuracy requirement.

Data for a typical module showing line regulation and temperature stability of the reference supply is given in the table below.

PERFORMANCE OF PRECISION CALIBRATION AND REFERENCE SOURCE

| | $V^+$(v) | $I_z$(ma) | $E_{out}$(v)#1 | $E_{out}$(v)#2 |
|---|---|---|---|---|
| T = -20°C | 11.00 | .739 | 5.510 | 3.991 |
| | 11.50 | .828 | 5.519 | 3.998 |
| | 12.00 | .838 | 5.522 | 3.999 |
| | 12.50 | .848 | 5.522 | 3.999 |
| | 13.00 | .848 | 5.522 | 3.999 |
| T = 0°C | 11.00 | .749 | 5.512 | 3.992 |
| | 11.50 | .838 | 5.521 | 3.999 |
| | 12.00 | .848 | 5.521 | 3.999 |
| | 12.50 | .848 | 5.521 | 3.999 |
| | 13.00 | .848 | 5.521 | 3.999 |
| T = 25°C | 11.00 | .843 | 5.514 | 3.994 |
| | 11.50 | .843 | 5.521 | 3.999 |
| | 12.00 | .843 | 5.521 | 3.999 |
| | 12.50 | .843 | 5.521 | 3.999 |
| | 13.00 | .848 | 5.521 | 3.999 |
| T = 50°C | 11.00 | .838 | 5.518 | 3.997 |
| | 11.50 | .848 | 5.521 | 3.999 |
| | 12.00 | .848 | 5.521 | 3.999 |
| | 12.50 | .848 | 5.521 | 3.999 |
| | 13.00 | .848 | 5.521 | 3.999 |
| T = 85°C | 11.00 | .848 | 5.521 | 3.999 |
| | 11.50 | .848 | 5.521 | 3.998 |
| | 12.00 | .848 | 5.521 | 3.998 |
| | 12.50 | .848 | 5.521 | 3.998 |
| | 13.00 | .848 | 5.520 | 3.998 |
| T = 100°C | 11.00 | .848 | 5.519 | 3.998 |
| | 11.50 | .848 | 5.519 | 3.998 |
| | 12.00 | .848 | 5.519 | 3.998 |
| | 12.50 | .848 | 5.519 | 3.998 |
| | 13.00 | .848 | 5.519 | 3.998 |

8. Module Output Circuit S056

The output circuit is a differential tri-level line driver circuit and is fabricated on a single monolythic silicon chip using complementary MOS transistor technology. A schematic of this circuit is shown in Figure 17. The circuit generates the response sync, formats output data and provides a response data parity bit. The output waveform swings between +.25 volts and a -.25 volts into a 82Ω Balance line. The positive true signal generates a +.25 volt for a logic "1", a 0.0 volt signal for logic zero and -.25 volt signal for "clock." The negative true signal swings just the opposite as shown in the Table below.

| | Data "1" | Data "0" | Clock |
|---|---|---|---|
| Positive True | +.25V | 0.0V | -.25V |
| Negative True | -.25V | 0.0V | +.25V |

There are three sources of data; Data #1, Data #2, and Parity. Data #1 is the serial data signal from the A/D converter and represents the data sign bit. This data is gated to the data buss as long as the Data #1 Enable is true. The data #1 control signal is taken from the timing register as TS #26. This allows the sign bit (MSB) of the A/D Converter to be outputed at this time.

Data #2 is gated to the data bus between the time a Data #2 start and a Data #2 stop is received. Data #2 is the serial data from the A/D converter which is the 8-bit A/D converter data.

The control signal for Data #2 start is received from the timing register as TS #27. The control signal for Data #2 stop is also received from the timing register as TS #35. It can be seen that as long as

the Data flip-flop is set, data will be outputed to the output bus. Thus, for the 8-bit data word, 8 time periods are required (TS27-TS35).

The Parity circuit in the upper left hand corner of the circuit schematic monitors the data buss and determines the parity of the data received since the last parity reset. Parity reset occurs at the beginning of the data word (TS #24) and the parity bit is outputed during TS #35. Either odd or even parity may be gated on to the data buss line; however, the system is normally odd. The data and $\overline{\text{data}}$ signals drive the large P and N channel device switches which switch one of the three voltage levels. The $\phi_1$ and $\phi_2$ clocking signals sample Data time and Clock time information for gating to the output switches. A sync signal, which indicates the start of new data, is generated by a Data "1", Data "0", Data "1", Data "0" sequence without any clock level. When the start sync signal becomes true (TS #22) the sync flip-flop is set holding the switch Q23 and Q22 on such that the positive true output is positive instead of negative during clock time. The negative true signal is negative during the clock time. The data buss is zero so both outputs are at zero volts during data time. The sync flip-flop is reset at TS #24 which stops output sync operation. The final output switches are controlled by the output enable signal which only goes true once the module has been addressed. The output enable signal is provided by the input control circuit (S058). The output is enabled during time slots TS21-22 for bad parity response and from TS23-TS35 for normal response.

A summary of the output driver chip characteristics is given below:

| | |
|---|---|
| Chip size: | 70 x 94 mils |
| No. of devices: | 76 |
| Supply Voltage: | +6.5, -8.5 ±1.0 |
| Power Dissipation: | 6 mw nominal (exclusive of line load) |
| Inputs: | Data #1 Input, Data #2 Input, Data #1 enable, Data #2 Start, Data #2 Stop, Parity reset, Parity enable odd, parity enable even, output enable, start sync, stop sync, $\phi_1$, $\phi_2$ |
| Power: | +V, -V, ground |
| Outputs: | Positive true large, positive true small, Negative true large, negative true small. |
| Package: | 24 lead flat-pac |

## V. DATA MODULE OPERATION (CIAM LOW LEVEL)

Figure 18 shows a block diagram of the CIAM low level module. Basically, each analog input to the previously described high level system has an amplifier between it and a transducer source. In order to provide a means for calibration, a special low level calibration multiplexer was designed to allow provision to calibrate each individual amplifier for full and zero scale. In addition, overload and protection circuitry was added to provide differential and common mode protection.

In addition to the above, two other slight alterations were made to the previously described high level system. The first consisted of modifying the reference supply used in the high level system to provide a low level full scale calibration signal of 30 mv or 50 mv as the gain of the amplifiers

dictated (either 83.3 or 50 respectively). Also, a bias signal of 2.755 volts for the amplifiers was necessary. The second alteration to the high level system consisted of making the A/D a 9-bit converter in order to detect the sign of the analog input voltage.

The circuitry which is different than that described for the high level module will not be discussed in some detail.

1. Overvoltage - Protection Circuitry

   Each differential input pair of analog signals are protected from both excessive common mode and differential signals by a resistive network in series with a zener diode network shown in Figure 19. Resistors R1 and R2 provide current limiting. Diodes CR5 and CR6 limit the differential input signal to less than 600 millivolts. Diodes CR1, CR3, CR2, and CR4 limit the common mode range (CMR) within $-7.0 < CMR < +7.0$ volts.

2. Calibration Multiplexer

   Figure 20 shows the schematic of the Low Level Calibration Multiplexer. It basically consists of 4 holding flip-flops that receive 4 inputs from the Data and Decode Register, decode logic to decode the four basic commands recognized by the Calibration Multiplexer, and two additional holding flip-flops which set the 48 (16 pole 3 position) MOS switches in the proper position. The table below indicates the calibration codes and their meaning.

| Name | Input #1 Input #2 Input #3 Input #4 | Output if Addressed | Q1 Q2 | Designation |
|---|---|---|---|---|
| $E_1$ | 1 0 0 1 | 1 | 11 | Operate, low level particular module |
| $E_2$ | 1 0 1 0 | 1 | 10 | Full scale calibrate particular module |
| $E_3$ | 1 0 1 1 | 1 | 01 | Zero scale calibrate particular module |
| $E_4$ | 1 1 0 0 | X | 11 | Operate, low level (all low level modules) |

The E, command requires that address of a particular module be sent along with the command to operate normally. (This command connects all data amplifiers through the calibrate multiplexer to their respective transducer.) The $E_2$ and $E_3$ commands also require that the command word states the particular address of the desired low level module. However, with these commands, the entire eight (8) amplifiers are either simultaneously connected to the full scale or zero scale calibrate voltage respectively. The $E_4$ command is used to allow all low level modules that are connected to the system to be placed in the operate mode simultaneously without stating any coded addresses for the low level modules. This command will greatly aid the programmer to follow a calibration procedure on all low level amplifiers and upon completion program one statement to connect all low level modules back to their normal analog input signals (operate). It should be noted that the flip flops designated by outputs $Q_1$ and $Q_2$ are set and remain in their set state until the next recognizable inputs to these flip flops are received. This is to say that each low level module will remain in its previous state (operate, full scale calibrate or zero scale calibrate) as long as no code commands $E_1$, $E_2$, $E_3$, $E_4$, are sent. This feature allows the individual amplifiers following the low level calibration multiplexer to be calibrated by issuances of the code commands for any desired channel to the high level multiplexer

(which is the same multiplexer used in the high level modules) immediately following the amplifiers. Thus, a calibration procedure (non-interleave mode) could be as follows:

| Time | Command Code | Remarks |
|---|---|---|
| 1st cycle | 1010 (module address) | Places addressed module to full scale calibrate |
| 2nd cycle | 0001 (module address) | Calibrate channel 1 full scale |
| 3rd cycle | 0010 (Module address) | Calibrate channel 2 full scale |
| 4th cycle | 0011 (Module address) | Calibrate channel 3 full scale |
| 5th cycle | 0100 (Module address) | Calibrate channel 4 full scale |
| 6th cycle | 0101 (Module address) | Calibrate channel 5 full scale |
| 7th cycle | 0110 (Module address) | Calibrate channel 6 full scale |
| 8th cycle | 0111 (Module address) | Calibrate channel 7 full scale |
| 9th cycle | 1000 (Module address) | Calibrate channel 8 full scale |
| 10th cycle | 1011 (Module address) | Places addressed module to zero scale calibrate |
| 11th cycle | 0001 (Module address) | Calibrate channel 1 zero scale |
| 12th cycle | 0010 (Module address) | Calibrate channel 2 zero scale |
| 13th cycle | 0011 (Module address) | Calibrate channel 3 zero scale |
| 14th cycle | 0100 (Module address) | Calibrate channel 4 zero scale |
| 15th cycle | 0101 (Module address) | Calibrate channel 5 zero scale |
| 16th cycle | 0110 (Module address) | Calibrate channel 6 zero scale |
| 17th cycle | 0111 (Module address) | Calibrate channel 7 zero scale |
| 18th cycle | 1000 (Module address) | Calibrate channel 8 zero scale |
| 19th cycle | 1001 (Module address) | Connects all 8 channels back to their respective analog sources (addressed module) |

Each succeeding low level module could be addressed with the above command code for calibration and if desired the 19th cycle could be eliminated from each particular module calibration procedure and replaced by an $E_4$ command

after all modules are calibrated.

There are a variety of ways in which the various commands discussed above may be used; however, by knowing the function which is performed by each code the exact operation must be determined by the system operator or programmer. Except for the special commands discussed above, the operation of the low level module is basically the same as described for the high level data module.

3. Low Level Amplifier (CIAM)

The low level amplifier as shown in Figure 21, consists of three low power operational amplifiers connected together in the so called "Medical Amplifier Configuration". Resistors $R_6$ and $R_7$ provide the bias current to the amplifier independent of the transducer source impedance. These resistors are 50 megohm to provide very high common-mode and differential input impedances. The input amplifiers $A_1$ and $A_2$ are cross coupled via resistors $R_1$, $R_2$, and $R_3$. They amplify the differential input signal with a gain determined by the resistor ratios $(1 + \frac{R2}{R1} + \frac{R3}{R1})$. It is interesting to note that this input network passes the common-mode signal at unity gain. The final stage (A3) and resistor network comprised of resistors R11, R13, R12, and R14, provide further gain with a single ended output, and by critically specifying accurate resistor matching yields good common mode rejection. A bias offset (2.755 volts) is introduced to provide positive output signals to the A/D converter for polarity changes in input signals. The remaining resistors and capacitors (with the exception of R4',R4", R5', and R5") provide frequency compensation and stabilization. Resistors R4', R4", R5', and R5" are adjusted during construction of the amplifier to remove the various offset voltages and their effect on the amplifier. This reduces the initial output offset voltage to less than $\pm$ 5 millivolts.

Two different gain settings are provided to handle the 30 mv and 50mv maximum input signals yet providing the same signal levels to the A/D converter. This is simply done by altering the ratios of R13/R11 and $12/R14 from 5 to 3 respectively with all other valves remaining the same. The table below lists the electrical performance characteristics of the CIAM amplifier. The component values for the amplifier schematic are given in the parts list of Figure 22.

| | Typical |
|---|---|
| Supply Voltage | ±7.5 volts |
| Power Dissipation | 4 mw |
| Differential Input Resistance | 100 megohms |
| Common-Mode Input Resistance | 25 megohms |
| Gain | 83.33±1%(50.00±1%) |
| Small Signal Bandwidth | 6 KHz |
| Slew Rate | 20 volts/millisec |
| Common Mode Rejection Ratio | 461 μvolts/5 volt |
| Power Supply Rejection Ratio | 32 μvolts/0.5 volt |
| Input Offset Voltage (including TC $V_{os}$) | 2.4 mvolt |
| TC input offset voltage | 6 μvolt/$^{o}$C |
| Input Bias Current (0 volt common mode) | 10 nano amp |
| (±5 volt common mode) | 200 nano amp |
| Noise (6 KHz Bandwidth) | 4μv RMS |

4. Low Level A/D Converter

The basic operation of the A/D converter was described in detail in another section. As was mentioned, the only difference in the high and low level A/D converter is that the high level is connected as an eight bit converter using only 8 ladder switches while the low level is connected as a 9-bit converter. The MSB of the 9 bit converter is then used as the sign bit for the low level module. The converter was designed in this manner to avoid two separate logic chip designs.

The bipolar operation of the low level module is accomplished as follows: The low level amplifiers are offset by exactly ½ the full scale reference voltage of the A/D converted. Thus, with zero input signal to the amplifiers, the output is ½ the positive reference voltage of the A/D converter. Consequently, as slight positive input to the module will cause the amplifier output to exceed ½ the reference voltage while a slight negative input signal will cause the amplifier output to become less than ½ the reference supply. Therefore, it can be seen that the MSB or first decision bit of the 9-bit A/D converter determines whether the input signal is positive or negative. From the earlier discussion, it is apparent that a positive input will leave the first bit set since the input is greater than ½ scale. This in turn would produce a "1" for the sign bit for a positive input signal with the reverse being true for a negative input signal. This is exactly opposite to the requirement for the A/D output code since the bipolar signal was to have a twos-complement code for negative inputs which requires a "1" for the sign bit of negative input signals. In order to accomplish the correct output code, the complement of

the serial output code ($\overline{\text{serial}}$ output) is used to provide sign bit information to the output circuit. With this simple change it is possible to achieve the bipolar A/D converter operation with the specified code using the same A/D converter design as was used in the high level module.

The reference supply for the low level modules contains the ½ scale offset bias voltage as well as the A/D reference voltage and a 30 or 50 millivolt calibration voltage. The reference voltage for the 9 bit A/D converter is 5.510 volts to give a nominal full scale input of 5.500 volts. The offset bias voltage is 2.755 volts. A table showing the module digital output code including parity bit is given in the table on the following page. This code is given in terms of the input voltage to the A/D converter and the 30mv low level input to the module. As may be seen the cross-over point from negative to positive sign bit occurs from -0.000065 to +0.000065 volts. The module is capable of handling ±30mv + 10% overrange or approximately ±33 millivolts input range. The accuracy of the A/D converter is well within ±1 bit which is approximately ± 10.7 millivolts. Other sources of error for the low level module include the low level multiplexer and the low level amplifiers as well as the reference bias supplied to the amplifiers from the reference supply. The overall module performance will be discussed in another section. It should be noted that if gain of 50 amplifiers are used, the input range is ±55 millivolts and the input voltages to the module are shown in the second table.

30 MILLIVOLT MODULE

LOW LEVEL A/D CONVERTER CONVERSION CHART

| DIGITAL OUTPUT CODE | | | THEORETICAL ANALOG INPUT TO A/D | THEORETICAL ANALOG INPUT TO MODULE |
|---|---|---|---|---|
| SIGN BIT | DATA BITS | PARITY BIT | VOLTS | VOLTS |
| 1 | 00000001 | 1 | 0.0054 | -0.032995 |
| 1 | 00000010 | 1 | 0.0161 | -0.032866 |
| 1 | 00000100 | 1 | 0.0376 | -0.032607 |
| 1 | 00001000 | 1 | 0.0807 | -0.032091 |
| 1 | 00010000 | 1 | 0.1668 | -0.031058 |
| 1 | 00100000 | 1 | 0.3390 | -0.028991 |
| 1 | 01000000 | 1 | 0.6834 | -0.024859 |
| 1 | 01011101 | 1 | 0.9955 | -0.021114 |
| 1 | 01111111 | 1 | 1.3614 | -0.016724 |
| 1 | 10000000 | 1 | 1.3721 | -0.016594 |
| 1 | 10000001 | 0 | 1.3829 | -0.016465 |
| 1 | 10011000 | 1 | 1.6304 | -0.013495 |
| 1 | 10111111 | 1 | 2.0501 | -0.0084[illegible] |
| 1 | 11000000 | 0 | 2.0609 | -0.008329 |
| 1 | 11011111 | 1 | 2.3945 | -0.004326 |
| 1 | 11111111 | 0 | 2.7388 | -0.000194 |
| 0 | 00000000 | 1 | 2.7496 | -0.000065 |
| 0 | 00000001 | 1 | 2.7604 | +0.000065 |
| 0 | 00011111 | 0 | 3.0832 | +0.003939 |
| 0 | 00111111 | 1 | 3.4276 | +0.008071 |
| 0 | 01011000 | 0 | 3.6966 | +0.011300 |
| 0 | 01111111 | 0 | 4.1163 | +0.016336 |
| 0 | 10000000 | 0 | 4.1271 | +0.016465 |
| 0 | 10101111 | 1 | 4.6329 | +0.022535 |
| 0 | 10111111 | 0 | 4.8051 | +0.024601 |
| 0 | 11101111 | 0 | 5.3217 | +0.030800 |
| 0 | 11111111 | 1 | 5.4938 | +0.032866 |

2

50 MILLIVOLT MODULE

LOW LEVEL A/D CONVERTER CONVERSION CHART

| DIGITAL OUTPUT CODE | | | THEORETICAL ANALOG INPUT TO A/D VOLTS | THEORETICAL ANALOG INPUT TO MODULE VOLTS |
|---|---|---|---|---|
| SIGN BIT | DATA BITS | PARITY BIT | | |
| 1 | 00000001 | 1 | 0.0054 | 0.054992 |
| 1 | 00000010 | 1 | 0.0161 | 0.054777 |
| 1 | 00000100 | 1 | 0.0376 | 0.053450 |
| 1 | 00001000 | 1 | 0.0807 | 0.053485 |
| 1 | 00010000 | 1 | 0.1668 | 0.051763 |
| 1 | 00100000 | 1 | 0.3390 | 0.048318 |
| 1 | 01000000 | 1 | 0.6834 | 0.041432 |
| 1 | 01011101 | 1 | 0.9955 | 0.035190 |
| 1 | 01111111 | 1 | 1.3614 | 0.027873 |
| 1 | 10000000 | 1 | 1.3721 | 0.027657 |
| 1 | 10000001 | 0 | 1.3829 | 0.027442 |
| 1 | 10011000 | 1 | 1.6304 | 0.022492 |
| 1 | 10111111 | 1 | 2.0501 | 0.014097 |
| 1 | 11000000 | 0 | 2.0609 | 0.013882 |
| 1 | 11011111 | 1 | 2.3945 | 0.007210 |
| 1 | 11111111 | 0 | 2.7388 | 0.000323 |
| 0 | 00000000 | 1 | 2.7496 | -0.000107 |
| 0 | 00000001 | 1 | 2.7604 | +0.000107 |
| 0 | 00011111 | 0 | 3.0832 | +0.006565 |
| 0 | 00111111 | 1 | 3.4276 | +0.013452 |
| 0 | 01011000 | 0 | 3.6966 | +0.018833 |
| 0 | 01111111 | 0 | 4.1163 | +0.027227 |
| 0 | 10000000 | 0 | 4.1271 | +0.027442 |
| 0 | 10101111 | 1 | 4.6329 | +0.037558 |
| 0 | 10111111 | 0 | 4.8051 | +0.041002 |
| 0 | 11101111 | 0 | 5.3217 | +0.051333 |
| 0 | 11111111 | 1 | 5.4938 | +0.054776 |

## VI. DATA MODULE OPERATION (CMIA LOW LEVEL)

Figure 23 shows a block diagram of the CMIA low level system. As in the CIAM system an overload and protection circuitry was used to provide differential and common mode protection. A low level differential multiplexer multiplexes one of the eight differential pairs into the common CMIA amplifier. Low level full scale calibration and zero calibration signals are also provided to calibrate the common amplifier. The CMIA amplifier is a low power fast responding amplifier that amplifies the incoming multiplexed signal to the standard voltage typical of the previously described high level system. The amplified signal is presented directly to the comparator of the A/D convertor.

As in the case of the CIAM system where the high level portion was altered, the CMIA high level system has undergone some slight changes. Basically, the CMIA high level portion is the same as the CIAM high level section with the further exception that the high level multiplexer has been removed. Thus, the high level portion of the CMIA system as distinguished from the high level system of Part IV has had: (1) the reference supply modified to provide the low level full scale calibration signals and to provide the 2.755 bias signal to the CMIA amplifier, (2) the A/D altered to a 9 bit converter and (3) the high level multiplexer removed.

The circuitry of the blocks making up the CMIA low level system will now be discussed in some detail where different from the previous described CIAM system.

### 1. Low Level Differential Multiplexer (CP073)

Figure 24 shows the schematic of the low level differential multiplexer. It is similar to the previously described high level

multiplexer with the exception that the analog channel switches have independent sources or inputs. As previously mentioned, the high level multiplexer was initially layed out with a pair of switches connected in parallel (sources connected together) such that only a slight metal mask change was necessary to provide independent sources. It might be well to mentioned that 16 decode networks were implemented internal to the circuit but only 12 were used; therefore, in order to reduce power 4 decode circuit load resistors were not internally connected. This is shown in the schematic by the open terminations of transistors 71, 76, 91, and 96. If these decode states were desired provision was allowed for a slight metal mask modification that would connect these transistors and allow for external output connection. The coding for the various channels and calibration signals remained exactly the same as the high level system, and operation of the circuit is as discussed for the high level multiplexer.

2. Low Level Amplifier (CMIA)

The low level CMIA amplifier as shown in Figure 25 consists of three operational amplifiers with moderate slew rate and power dissipation connected in the medical amplifier configuration. The operation of this amplifier is exactly the same as that described for the CIAM amplifier except for two significant characteristics. First, the amplifier is much faster responding then the CIAM version. This results from the fact that the input data to the amplifier is multiplexed at the word cycle rate from channel to channel in general. Also, the output of the amplifier must be capable of slewing to its required value and settle out before the start conversion pulse is received to the A/D convertor. Thus, upon receipt of an address

command the desired analog channel is selected and at this time (T7) the amplifier starts responding from its previous output to the new desired value. The desired value must be presented to the A/D convertor at the start conversion time slot (TS25). Because of the faster response the power dissipation characteristic of the CMIA amplifier is significantly larger than (≈10 times) the CIAM power dissipation.

A parts list for the CMIA amplifier is given in Figure 26. The table below lists the electrical performance characteristics of the CMIA amplifier.

| | Typical |
|---|---|
| Supply voltage | ±7.5 volts |
| Power dissipation | 33 mw |
| Differential Input Resistance | 100 megohms |
| Common-Mode Input Resistance | 25 megohms |
| Gain | 83.33 ± 1% |
| Small signal bandwidth | 35 KHz |
| Slew Rate | 0.5V/μsec |
| Common Mode Rejection Ratio | 471μv/5v |
| Power Supply Rejection Ratio | 32μv/0.5v |
| Input Offset Voltage (including IC $V_{os}$) | 1mv |
| TC input offset voltage | 10μv/$^{o}$C |
| Input Bias Current (0 volt common mode) | 20 nano amp. |
| | 200 nano amp. |
| Noise (35 KHz Bandwidth) | 22μv/RMS |

## VII. DATA MODULE CONFIGURATION

The basic packaging technique and module configuration of each of the module types are essentially the same and consists of mounting the integrated circuit silicon chips in flat-pac packages and then soldering the flat-pacs to a second level interconnecting printed circuit board. These printed circuit boards are then stacked and interconnected by solid bus wire stringers which form both an electrical interconnect and a mechanical support. An interfacing printed circuit board is then used at each end of the printed circuit board stack to connect the various inputs and outputs to the appropriate pins of the module connectors.

An inspection of the module packaging technique and overall configuration reveals that a considerable smaller package could be designed using the same integrated circuit flat-pacs which are presently used. The package which has been used is a compromise between a relatively small module package and a rather simple, inexpensive packaging technique which is repairable. This package was used as a convenience for system testing and evaluation without excessive expenditure of both time and money on a more elaborate microminiature package.

### 1. High Level Data Module

The high level data module is fabricated from only 12 integrated circuit flat-pacs of which two of these are used only for overvoltage protection of the analog inputs. The interconnection diagram for the twelve flat-pacs of the high level data module is given in drawing D-704-1011, Figure 27. This drawing, in addition to showing the module interconnection and pin function, shows the pin function of each of the flat-pacs used in the high level data module.

The integrated circuit flat-pacs are interconnected by means of 5 printed circuit boards. Three of these boards are used to interconnect flat-pacs, and two are used to interface the printed circuit boards with the module connectors. An assembly drawing of the high level data module is shown in Figure 28 (Drawing No. E704-3007). Photographs of the high level data module are shown in Figures 29-31. Figure 29 shows the data module looking from the transducer and address connector side with the module cover removed. Figures 30 and 31 show the module in exploded view from each end.

The distribution of the flat-pacs on the various pc boards are as follows:

HL-1 - Input circuits S025C & S058A, timing register S065, Output circuit S056A

HL-2 - A/D Converter S022; Ladder SD2017, Comparator S020B, Reference supply RS-1A 101535

HL-3 - Input protection limiting resistors S019-B1, protection zeners S019-B2, Data Register S021A, Multiplexer S018A

Photographs of each of the printed circuit boards showing the flat-pacs mounted as indicated above are given in Figures 32-36.

The printed circuit boards are interconnected by stringer wires through the 52 holes around the outside of the board. The electrical interconnect and function of each of these wires is shown on drawing E704-3007 in Figure 37. The position of hole or wire number one may be found by observing the component side of board HL-1 and noting the index point in the corner next to S065. Hole number one is the first hole counter clock wire from the index point. During assembly, all boards are aligned by this index point with the primary component

side (side A) facing the command line connector. The drawing of Figure 37 may also be used to identify the pin functions of the command line and analog connectors. In addition to input-output functions, various test points are available at the pins indicated on the command line connector (interfacing with HLB).

2. CIAM Low Level Module

The CIAM low level module incorporates most of the same circuit chips which are used in the high level module; however, in addition to these components, additional packages are required for the calibration multiplexer and the analog amplifiers. Although the same basic packing technique is used, the additional components require additional printed circuit boards which in turn increases the length of the module. The interconnection diagram of the CIAM low level module is given in Figure 38 (Drawing No. E704-4008). This drawing shows pin functions for all flat-pacs, their interconnection, and module connector pin functions. The integrated circuit flat-pacs are interconnected by means of 10 printed circuit boards. The size and general appearance of the boards are the same as those used for the high level module. As in the high level module, two of the boards are used to interface the printed circuit board stack with the module connectors. As previously noted, the only physical difference in the CIAM module compared to the high level module is the module length which increased from 1.862 to 2.743 inches.

The distribution of the circuit flat-pacs on the various printed circuit boards for the CIAM module is as follows:

module. The command line connector is identical in pin function to the high level module. The analog connector differs in that the analog inputs are two wire inputs rather than single ended as with the high level module. The pin functions for the CIAM module are given in drawing 704-4006, Figure 39 and drawing 704-4008, Figure 38.

3. CMIA Low Level Module

The CMIA low level module also uses many of the same circuit chips which are used in the high level data module. The basic difference in this module from the high level is the use of a differential protection circuit, a differential multiplexer and a CMIA amplifier package. The CMIA module uses 4 printed circuit boards for module circuitry as compared to three for the high level module. The same basic packaging technique is used for the CMIA module; in fact, the same assembly jig and housing are used for the CMIA module, consequently, the same module volume is required for this module as was required for the high level module. The extra printed circuit board is inserted in the space between HL-1 and HL-2 of the high level module assembly. This assembly is shown in the CMIA assembly drawing E704-3012, Figure 42.

As may be seen from the CMIA Interconnections Diagram, Figure 40, the CMIA module is composed of only 14 flat-pacs. The distribution of these flat-pacs on the various PC boards is as follows:

HL-1 same for all modules - Input circuits S025, S058, Timing Register S065, Output driver circuit S056

LL-2 A/D Converter S022, Ladder SD2017, Comparator S020B, Reference Supply RS2A 101549 (Same as CIAM module).

LL-9 CMIA Amplifier 101553, Data Register S021

HL-1 Input circuits S025C, S058A, Timing register S065 output circuit S056A (same as high level module)

LL-2 A/D converter S022C, Ladder SD2017, Comparator S020B, Reference Supply RS-2A 101549

LL-3 Data Register S021A, Multiplexer S018A

LL-4 Amplifier 101540 Ch. #7, Amplifier 101540 Ch. #8

LL-5 Amplifier 101540 Ch. #5, Amplifier 101540 Ch. #6

LL-6 Amplifier 101540 Ch. #3, Amplifier 101540 Ch. #4

LL-7 Amplifier 101540 Ch. #1, Amplifier 101540 Ch. #2

LL-8 Calibrate Multiplexer 062, Protection resistors S019 B1, Protection zeners 074

NOTE: Amplifiers with gain of 50 are numbered 101552

As with the high level module, the printed circuit boards are interconnected by bus wires through 52 holes around the outside of the PD boards. The function of each of the interconnecting wires is shown on the drawing E704-4006, Figure 39. The number of the interconnection wire is identified as described for the high level data module. The only basic difference between the high and low level modules is that the same hole position may carry two different interconnect functions in some places. In these instances, the interconnecting wire is cut so the two functions are not shorted together. For example, hole number two is used to connect channel #1+ from LL-7 to LL-8 and is also used to connect TS #14 from HL-1 to LL-3. The interconnecting wire is then cut somewhere between LL-3 and LL-7 to prevent the two functions from being shorted together.

Except for this sharing of functions for some interconnecting holes, the two modules are assembled as described for the high level

LL-10 Resistor Network (2) S019-B1, Zener Network 074

Differential Multiplexer 073

The same interface boards which are used in the CIAM module are used in the CMIA module, and the same pin functions are used for both modules. The PC board interconnection diagram for the CMIA module is given in Figure 41. This module requires multiple interconnect functions on only six of the interconnection wires. For these functions, the wire is clipped to prevent shorting functions together as described in the CIAM section.

## VIII. MODULE TEST RESULTS AND CONCLUSIONS

### 1. High Level Data Module

The general performance of the high level data module was satisfactory. The only problem encountered in testing the high level data modules was an accuracy problem under certain conditions. This problem was traced to noisy power supply voltages when the modules are connected along the long common system cable. Each module when tested individually was within the specified +0.5% accuracy over the entire analog input range of 0 to +5.5 volts; however, when operating at the specified frequency (450 KHz) and connected along the system cable with many other modules, errors of up to about 1½ bits or ±.8% were at times noted. If the frequency of the system controller clock was reduced to approximately 300 KHz, all modules were within the specified accuracy. It is felt that the basic problem is the power supply noise. It is, therefore, recommended that future modules should include an improved power supply decoupling network on the connector interface printed circuit board to reduce this problem. The basic design of the module at present necessitates that the negative supply be applied as a step function to each module to initiate a proper power-up state of certain control flip-flops in the S058 input chip. This, consequently, required that the negative supply could not be properly filtered or the step response would be lost. To overcome this problem for future application, the S058 chip was redesigned late in the program to include a special power-up circuit in parallel with the R-C power-up network so that the negative supply could be properly filtered at each module without hindering the power-up function in the module. The

new chip (S093) was not available in time for this program but could be incorporated in future efforts if desired. The use of this chip would require a slight redesign of the system controller such that at each initial system power-up, a special power-up command consisting of a 1-0-1-0-1-0-1-0 (two consecutive sync words) would be sent to all modules simultaneously. By using this special power-up command, extensive filtering could then be applied at the input of all power lines to all modules. This filtering could be accomplished on the connector interface printed circuit board. From all tests which were performed, it is felt that the modification would greatly improve module accuracy and make it independent of cable position or frequency.

All tests on individual modules indicate completely satisfactory performance over a wide frequency range of from a few Hertz to approximately 600 KHz. One other modification which is felt would further improve the module accuracy to within ± ½ LSB or ±0.25% is the addition of an offset adjustment to the A/D converter voltage comparator. This is presently the single largest source of error in the high level data module. If the inherent offset of each individual comparator could be adjusted after final module assembly, the present errors could very nearly be cut 50%.

Each module was tested for proper operation under computer control before final delivery. The test consisted of addressing each module on the line several million times and recording whether or not the module responded correctly. A tabulation of errors for each module was printed out the end of each system test. Any module which consistantly showed response errors was removed from the system and reworked until satisfactory operation was obtained.

In summary, it is felt that the high level data module very nearly meets all of the original program goals except for size and power. In both of these catagories, the present module is a vast improvement over presently available comparable systems. The size (2.5 x 2.5 x 1.75 approx.) could be considerably reduced by a package redesign; however, connectors are a limiting factor in size reduction. The module power consumption is about 50% higher than the original goal (150mw versus 100mw responding) however, this still represents an order of magnitude reduction in operating power compared to other electronic systems with comparable operating functions.

The large degree of circuit integration has greatly reduced manual assembly operations compared to systems using standard integrated circuit techniques, and consequently, should considerably improve reliability of such systems.

In general, it is felt by General Instrument Corporation that the high level data module development was a success and has resulted in a considerable advance in the state-of-the-art in low power miniature data sampling systems.

2. CMIA Low Level Module

In addition to the components required for the high level module, the CMIA module incorporates a low level amplifier and a low level differential multiplexer. The performance of the CMIA module is generally satisfactory; however, as with the high level module, the accuracy could be improved by both additional power supply filtering and an offset adjustment. The general operation of the module in terms of speed, power and received-respond performance is entirely satisfactory. The power dissipation is approximately 35-40 milliwatts greater than that of the high level data module which is the power required by the low level amplifier. The module will operate from a few KHz to 500 KHz; however, additional error is introduced as the frequency is increased above about 350 KHz when connected on the system cable. The module when connected by a short cable with good supply voltages is good up to 450-500 KHz.

The amplifiers themselves appear to be satisfactory except for excessive initial offset on some amplifiers. There is some additional offset when connected in the system due to noise pick-up. It appears that the optimum fix for these modules to improve accuracy would be a pot adjustment for the offset bias voltage which is supplied from the reference supply to the amplifier to enable the A/D Converter to handle bipolar signals. This pot adjust could then correct for both amplifier and comparator offset. If the adjustment is made on the module after it is placed on the system cable during zero calibrate, the accuracy could be considerably improved since the major source of error within a module appears to be an offset error.

In summary, the general performance of the CMIA module when connected

in the system appears to be good except for excessive offset error. With this error the worst case module accuracy is approximately ±0.6 mv or ±1.0% of full scale with some modules making about 0.3 mv or ±0.5% at room temperature. Temperature error is almost exclusively due to amplifier drift and can, therefore, be corrected to some extent by calibrate commands. The temperature tests indicate that absolute accuracy over temperature is approximately ±2% or 1.2 millivolts referred to the input. However, since the amplifier is still linear in this region most of the temperature drift may be calibrated out.

One of the primary problems with the low level modules has been that the hybrid amplifiers were delivered so late in the program that it has been impossible to do any redesign or even a thorough evaluation. It is felt that the performance of the CMIA module is quite good, but could be improved by a redesign incorporating additional isolation in power supplies, additional filtering in reference voltages and the addition of an offset adjustment which could be performed after the module is totally assembled.

Data was taken on 12 CMIA modules connected at random along the system cable. Zero and full scale calibration channels were interrogated by the central controller 1000 times for each channel at various system clock rates from 250 KHz to 450 KHz. The number of errors and the high and low readings for each of the modules were then tabulated by the PDP-8 computer and printed out. The results of these tests are shown in the following 5 pages along with a tabulation of maximum error. As may be seen, the majority of the error is offset error which could be adjusted out. Module address 64 is somewhat frequency sensitive and, therefore, accumulates response errors at maximum

frequency, but is satisfactory at frequencies below 400 KHz. Module address 62 has an excessive error at full scale calibrate which is apparently due to the full scale calibrate reference voltage being high. The other modules show typical errors and are within the accuracy previously discussed but could be adjusted to be considerably better by incorporation of an offset adjust pot.

More complete data for one of the modules is shown following the computer data. Accuracy tests are shown for room temperature on $+85^{\circ}C$. The results show the typical temperature effect on the module accuracy.

CMIA Low Level Module Test

```
ENTER DATA
61-72;H;0,15
X1000*
```

450 KHZ

```
TAPE?
(Y OR N) ?N
```

| MODULE | CDB | RPF | MR | RCE | NS |
|---|---|---|---|---|---|
| 0061 | 0000 | 0000 | 0000 | 0000 | 0000 |
| 0062 | 0000 | 0000 | 0000 | 0000 | 0000 |
| 0063 | 0000 | 0000 | 0000 | 0000 | 0000 |
| 0064 | 0000 | 0000 | 0000 | 2000 | 2000 |
| 0065 | 0000 | 0000 | 0000 | 0000 | 0000 |
| 0066 | 0000 | 0000 | 0000 | 0000 | 0000 |
| 0067 | 0000 | 0000 | 0000 | 0000 | 0000 |
| 0068 | 0000 | 0000 | 0000 | 2000 | 2000 |
| 0069 | 0000 | 0000 | 0000 | 2000 | 2000 |
| 0070 | 0000 | 0000 | 0000 | 0000 | 0000 |
| 0071 | 0000 | 0000 | 0000 | 0274 | 0274 |
| 0072 | 0000 | 0000 | 0000 | 0061 | 0061 |

Equivalent Input Error (MAX.)

| MODULE | CHANNEL | HIGH | LOW | MAX Error | |
|---|---|---|---|---|---|
| 0061 | 0000 | 0006 | 0006 | +6 | +.7 mv |
| 0061 | 0015 | 0356 | 0355 | +5 | +.6 |
| 0062 | 0000 | 0005 | 0004 | +5 | +.6 |
| 0062 | 0015 | 0361 | 0360 | +8 | +1.0 |
| 0063 | 0000 | 0006 | 0005 | +6 | +.7 |
| 0063 | 0015 | 0357 | 0355 | +7 | +.85 |
| 0064 | 0000 | 0000 | 0000 | no response | |
| 0064 | 0015 | 0000 | 0000 | | |
| 0065 | 0000 | 0007 | 0007 | +7 | +.85 |
| 0065 | 0015 | 0360 | 0357 | +7 | +.85 |
| 0066 | 0000 | 0003 | 0001 | +3 | +.35 |
| 0066 | 0015 | 0353 | 0351 | +2 | +.25 |
| 0067 | 0000 | 0005 | 0004 | +5 | +.6 |
| 0067 | 0015 | 0356 | 0356 | +5 | +.6 |
| 0068 | 0000 | 0000 | 0000 | no module on line | |
| 0068 | 0015 | 0000 | 0000 | | |
| 0069 | 0000 | 0000 | 0000 | no module on line | |
| 0069 | 0015 | 0000 | 0000 | | |
| 0070 | 0000 | 0004 | 0004 | +4 | +.5 |
| 0070 | 0015 | 0354 | 0353 | +3 | +.35 |
| 0071 | 0000 | 0777 | 0777 | -1 | -.1 |
| 0071 | 0015 | 0347 | 0343 | -5 | -.6 |
| 0072 | 0000 | 0776 | 0775 | -2 | -.35 |
| 0072 | 0015 | 0345 | 0345 | -3 | -.35 |

```
ENTER DATA
61-72;H;0,15
X1000*

TAPE?
(Y OR N) ??N
```

400 KHZ

| MODULE | CDB | RPF | MR | RCE | NS |
|---|---|---|---|---|---|
| 0061 | 0000 | 0000 | 0000 | 0000 | 0000 |
| 0062 | 0000 | 0000 | 0000 | 0000 | 0000 |
| 0063 | 0000 | 0000 | 0000 | 0000 | 0000 |
| 0064 | 0000 | 0000 | 0000 | 0008 | 0008 |
| 0065 | 0000 | 0000 | 0000 | 0000 | 0000 |
| 0066 | 0000 | 0000 | 0000 | 0000 | 0000 |
| 0067 | 0000 | 0000 | 0000 | 0000 | 0000 |
| 0068 | 0000 | 0000 | 0000 | 2000 | 2000 |
| 0069 | 0000 | 0000 | 0000 | 2000 | 2000 |
| 0070 | 0000 | 0000 | 0000 | 0000 | 0000 |
| 0071 | 0000 | 0000 | 0000 | 0000 | 0000 |
| 0072 | 0000 | 0000 | 0000 | 0000 | 0000 |

| MODULE | CHANNEL | HIGH | LOW | Max Error | Equivalent Input Error (MAX) |
|---|---|---|---|---|---|
| 0061 | 0000 | 0006 | 0005 | +6 | +.7 mV |
| 0061 | 0015 | 0356 | 0355 | +5 | +.6 |
| 0062 | 0000 | 0004 | 0004 | +4 | +.5 |
| 0062 | 0015 | 0361 | 0361 | +8 | +1.0 |
| 0063 | 0000 | 0004 | 0004 | +4 | +.5 |
| 0063 | 0015 | 0355 | 0354 | +4 | +.5 |
| 0064 | 0000 | 0000 | 0777 | −1 | −.1 |
| 0064 | 0015 | 0347 | 0346 | −2 | −.25 |
| 0065 | 0000 | 0006 | 0006 | +6 | +.7 |
| 0065 | 0015 | 0357 | 0356 | +6 | +.7 |
| 0066 | 0000 | 0001 | 0777 | ±1 | ±.12 |
| 0066 | 0015 | 0351 | 0347 | −2 | −.2 |
| 0067 | 0000 | 0004 | 0003 | +4 | +.5 |
| 0067 | 0015 | 0354 | 0354 | +3 | +.35 |
| 0068 | 0000 | 0000 | 0000 | No module on line | |
| 0068 | 0015 | 0000 | 0000 | | |
| 0069 | 0003 | 0000 | 0000 | No module on line | |
| 0069 | 0015 | 0000 | 0000 | | |
| 0070 | 0000 | 0002 | 0001 | +2 | +.25 |
| 0070 | 0015 | 0352 | 0351 | +1 | +.1 |
| 0071 | 0000 | 0776 | 0776 | −2 | −.25 |
| 0071 | 0015 | 0346 | 0346 | −2 | −.25 |
| 0072 | 0000 | 0774 | 0774 | −4 | −.5 |
| 0072 | 0015 | 0343 | 0343 | −5 | −.6 |

```
ENTER DATA
61-72;H;0,15
X1000*

TAPE?
(Y OR N) ??N
```

350 KHZ

| MODULE | CDB | RPF | MR | RCE | NS |
|---|---|---|---|---|---|
| 0061 | 0000 | 0000 | 0000 | 0000 | 0000 |
| 0062 | 0000 | 0000 | 0000 | 0000 | 0000 |
| 0063 | 0000 | 0000 | 0000 | 0000 | 0000 |
| 0064 | 0000 | 0000 | 0000 | 0000 | 0000 |
| 0065 | 0000 | 0000 | 0000 | 0000 | 0000 |
| 0066 | 0000 | 0000 | 0000 | 0000 | 0000 |
| 0067 | 0000 | 0000 | 0000 | 0000 | 0000 |
| 0068 | 0000 | 0000 | 0000 | 2000 | 2000 |
| 0069 | 0000 | 0000 | 0000 | 2000 | 2000 |
| 0070 | 0000 | 0000 | 0000 | 0000 | 0000 |
| 0071 | 0000 | 0000 | 0000 | 0000 | 0000 |
| 0072 | 0000 | 0000 | 0000 | 0000 | 0000 |

| MODULE | CHANNEL | HIGH | LOW | MAX Error | Equivalent Input Error (MAX) |
|---|---|---|---|---|---|
| 0061 | 0000 | 0005 | 0004 | +5 | +.6 MV. |
| 0061 | 0015 | 0355 | 0354 | +4 | +.5 |
| 0062 | 0000 | 0003 | 0003 | +3 | +.35 |
| 0062 | 0015 | 0361 | 0360 | +8 | +.8 |
| 0063 | 0000 | 0003 | 0001 | +3 | +.35 |
| 0063 | 0015 | 0354 | 0351 | +3 | +.35 |
| 0064 | 0000 | 0776 | 0776 | −2 | −.25 |
| 0064 | 0015 | 0344 | 0344 | −5 | −.6 |
| 0065 | 0000 | 0003 | 0002 | +3 | +.35 |
| 0065 | 0015 | 0353 | 0353 | +2 | +.25 |
| 0066 | 0000 | 0777 | 0774 | −4 | −.5 |
| 0066 | 0015 | 0346 | 0344 | −4 | −.5 |
| 0067 | 0000 | 0000 | 0777 | −1 | −.1 |
| 0067 | 0015 | 0351 | 0350 | −1 | −.1 |
| 0068 | 0000 | 0000 | 0000 | No module on line | |
| 0068 | 0015 | 0000 | 0000 | | |
| 0069 | 0000 | 0000 | 0000 | No module on line | |
| 0069 | 0015 | 0000 | 0000 | | |
| 0070 | 0000 | 0001 | 0000 | +1 | +.1 |
| 0070 | 0015 | 0350 | 0347 | −2 | −.25 |
| 0071 | 0000 | 0775 | 0774 | −4 | −.5 |
| 0071 | 0015 | 0345 | 0344 | −4 | −.5 |
| 0072 | 0000 | 0774 | 0773 | −4 | −.5 |
| 0072 | 0015 | 0343 | 0342 | −6 | −.7 |

300 KHz

```
ENTER DATA
61-72;H;0,15
X1000*

TAPE?
(Y OR N) ?N
```

| MODULE | CDB | RPF | MR | RCE | NS |
|---|---|---|---|---|---|
| 0061 | 0000 | 0000 | 0000 | 0000 | 0000 |
| 0062 | 0000 | 0000 | 0000 | 0000 | 0000 |
| 0063 | 0000 | 0000 | 0000 | 0000 | 0000 |
| 0064 | 0000 | 0000 | 0000 | 0000 | 0000 |
| 0065 | 0000 | 0000 | 0000 | 0000 | 0000 |
| 0066 | 0000 | 0000 | 0000 | 0000 | 0000 |
| 0067 | 0000 | 0000 | 0000 | 0000 | 0000 |
| 0068 | 0000 | 0000 | 0000 | 2000 | 2000 |
| 0069 | 0000 | 0000 | 0000 | 0000 | 0000 |
| 0070 | 0000 | 0000 | 0000 | 0000 | 0000 |
| 0071 | 0000 | 0000 | 0000 | 0000 | 0000 |
| 0072 | 0000 | 0000 | 0000 | 0000 | 0000 |

| MODULE | CHANNEL | HIGH | LOW | MAX Error | Equivalent Input Error (MAX) |
|---|---|---|---|---|---|
| | | | | | +.35 MV. |
| 0061 | 0000 | 0003 | 0002 | +3 | +.25 |
| 0061 | 0015 | 0353 | 0351 | +2 | |
| 0062 | 0000 | 0002 | 0001 | +2 | +.25 |
| 0062 | 0015 | 0360 | 0357 | +7 | +.85 |
| 0063 | 0000 | 0003 | 0001 | +3 | +.35 |
| 0063 | 0015 | 0353 | 0351 | +2 | +.25 |
| 0064 | 0000 | 0777 | 0776 | -2 | -.25 |
| 0064 | 0015 | 0346 | 0344 | -4 | -.5 |
| 0065 | 0000 | 0003 | 0003 | +3 | +.35 |
| 0065 | 0015 | 0354 | 0353 | +3 | +.35 |
| 0066 | 0000 | 0777 | 0775 | -3 | -.35 |
| 0066 | 0015 | 0347 | 0345 | -4 | -.5 |
| 0067 | 0000 | 0000 | 0777 | -1 | -.1 |
| 0067 | 0015 | 0351 | 0351 | — | — |
| 0068 | 0000 | 0000 | 0000 | no module on line | |
| 0068 | 0015 | 0000 | 0000 | | |
| 0069 | 0000 | 0003 | 0002 | +3 | +.35 |
| 0069 | 0015 | 0351 | 0351 | — | — |
| 0070 | 0000 | 0001 | 0000 | +1 | +.1 |
| 0070 | 0015 | 0350 | 0350 | -1 | -.1 |
| 0071 | 0000 | 0775 | 0774 | -4 | -.5 |
| 0071 | 0015 | 0344 | 0344 | -5 | -.6 |
| 0072 | 0000 | 0774 | 0773 | -5 | -.6 |
| 0072 | 0015 | 0343 | 0342 | -6 | -.7 |

```
61-72;H;0,15                                    250 NS
X1000*

TAPE?
(Y OR N) ?N

:  :
```

| MODULE | CDB | RPF | MR | RCE | NS |
|---|---|---|---|---|---|
| 0061 | 0000 | 0000 | 0000 | 0000 | 0000 |
| 0062 | 0000 | 0000 | 0000 | 0000 | 0000 |
| 0063 | 0000 | 0000 | 0000 | 0000 | 0000 |
| 0064 | 0000 | 0000 | 0000 | 0000 | 0000 |
| 0065 | 0000 | 0000 | 0000 | 0000 | 0000 |
| 0066 | 0000 | 0000 | 0000 | 0000 | 0000 |
| 0067 | 0000 | 0000 | 0000 | 0000 | 0000 |
| 0068 | 0000 | 0000 | 0000 | 2000 | 2000 |
| 0069 | 0000 | 0000 | 0000 | 0000 | 0000 |
| 0070 | 0000 | 0000 | 0000 | 0000 | 0000 |
| 0071 | 0000 | 0000 | 0000 | 0000 | 0000 |
| 0072 | 0000 | 0000 | 0000 | 0000 | 0000 |

| MODULE | CHANNEL | HIGH | LOW | MAX Error | Equivalent Input Error (MAX) |
|---|---|---|---|---|---|
| 0061 | 0000 | 0003 | 0003 | +3 | +.35 |
| 0061 | 0015 | 0353 | 0352 | +2 | +.25 |
| 0062 | 0000 | 0001 | 0001 | +1 | +.1 |
| 0062 | 0015 | 0357 | 0357 | +6 | +.7 |
| 0063 | 0000 | 0002 | 0002 | +2 | +.25 |
| 0063 | 0015 | 0354 | 0351 | +3 | +.35 |
| 0064 | 0000 | 0777 | 0776 | -2 | -.25 |
| 0064 | 0015 | 0345 | 0344 | -4 | -.5 |
| 0065 | 0000 | 0003 | 0003 | +3 | +.35 |
| 0065 | 0015 | 0353 | 0353 | +2 | +.25 |
| 0066 | 0000 | 0777 | 0775 | -3 | -.35 |
| 0066 | 0015 | 0346 | 0345 | -3 | -.35 |
| 0067 | 0000 | 0000 | 0777 | -1 | -.1 |
| 0067 | 0015 | 0351 | 0347 | -2 | -.25 |
| 0068 | 0000 | 0000 | 0000 | no module on line | |
| 0068 | 0015 | 0000 | 0000 | | |
| 0069 | 0000 | 0003 | 0002 | +3 | +.35 |
| 0069 | 0015 | 0351 | 0351 | — | — |
| 0070 | 0000 | 0001 | 0001 | +1 | +.1 |
| 0070 | 0015 | 0351 | 0350 | -1 | -.1 |
| 0071 | 0000 | 0776 | 0776 | -2 | -.25 |
| 0071 | 0015 | 0345 | 0344 | -4 | -.5 |
| 0072 | 0000 | 0774 | 0774 | -4 | -.5 |
| 0072 | 0015 | 0343 | 0343 | -5 | -.6 |

CMIA

9 Bit A/D Low level

Room Temp. 400KC

O = ____ -V = ____ Serial # 70

| Digital Input | Expected Analog Input | Ch #1 | Ch #2 | Ch #3 | Ch #4 | Ch #5 | Ch #6 | Ch #7 | Ch #8 |
|---|---|---|---|---|---|---|---|---|---|
| 000000001 | -32.995 | 32.476 | 33.456 | 33.473 | 33.455 | 33.445 | 33.467 | 33.472 | 33.464 |
| 000000010 | -32.866 | 33.354 | | | | | | | |
| 000000100 | -32.607 | 32.69 | | | | | | | |
| 000001000 | -32.091 | 32.570 | | | | | | | |
| 000010000 | -31.058 | 31.515 | | | | | | | |
| 000100000 | -28.991 | 29.420 | | | | | | | |
| 001000000 | -24.859 | 25.002 | | | | | | | |
| 010111101 | -21.114 | 21.596 | | | | | | | |
| 011111111 | -16.724 | 17.157 | | | | | | | |
| 100000000 | -16.594 | 17.573 | 16.912 | 16.906 | 16.911 | 16.891 | 16.930 | 16.903 | 16.913 |
| 100000001 | -16.465 | 16.989 | | | | | | | |
| 101011000 | -13.495 | 13.858 | | | | | | | |
| 110111111 | -8.458 | 8.894 | | | | | | | |
| 111000000 | -8.329 | 8.657 | | | | | | | |
| 111011111 | -4.326 | 4.745 | | | | | | | |
| 111111111 | -.194 | -.593 | -.563 | -.576 | -.565 | -.555 | -.534 | -.574 | -.572 |
| 100000000 | -.065 | -.500 | | | | | | | |
| 100000001 | +.065 | -.331 | -.322 | -.334 | -.332 | -.313 | -.332 | -.338 | -.331 |
| 100011111 | +2.929 | +.3345 | | | | | | | |
| 101011111 | +8.071 | 7.666 | | | | | | | |
| 101011000 | +11.360 | 10.942 | | | | | | | |
| 101111111 | +16.336 | 15.963 | | | | | | | |
| 110000000 | +16.465 | 16.097 | 16.031 | 16.016 | 16.020 | 16.038 | 16.026 | 16.031 | 16.012 |
| 110101111 | +22.535 | 22.142 | | | | | | | |
| 111011111 | +24.661 | 24.236 | | | | | | | |
| 111101111 | +30.800 | 30.446 | | | | | | | |
| 111111111 | +32.866 | 32.507 | 32.540 | 32.521 | 32.542 | 32.533 | 32.641 | 32.521 | 32.513 |

full scale Cal. H.L.

1/2 scale Cal. H.L. 011101010

zero Cal. H.L.

zero Cal L.L.

form 7131-5 (9-65)

# 9 Bit A/D Low level

+V = _____ -V = _____ 85° C 400kC Serial # 70

| Digital Out Bit | Expected M.V. Analog to Amp. | Ch #1 | ch #2 | Ch #3 | Ch #4 | Ch #5 | Ch #6 | Ch #7 | Ch #8 |
|---|---|---|---|---|---|---|---|---|---|
| 000000001 | -32.995 | 33.623 | 33.864 | 33.907 | 33.905 | 33.871 | 33.852 | 33.875 | 33.763 |
| 000000010 | -32.866 | 33.507 | | | | | | | |
| 000000100 | -32.607 | 33.248 | | | | | | | |
| 000001000 | -32.091 | 32.755 | | | | | | | |
| 000010000 | -31.658 | 31.669 | | | | | | | |
| 000100000 | -28.991 | 29.632 | | | | | | | |
| 001000000 | -24.859 | 25.465 | | | | | | | |
| 010101101 | -21.114 | 21.756 | | | | | | | |
| 001111111 | -16.724 | 17.329 | | | | | | | |
| 010000000 | -16.594 | 17.197 | | | | | | | |
| 010000001 | -16.465 | 17.134 | 17.273 | 17.308 | 17.304 | 17.278 | 17.253 | 17.238 | 17.178 |
| 010011000 | -13.495 | 14.124 | | | | | | | |
| 010111111 | - 8.458 | 9.093 | | | | | | | |
| 011000000 | - 8.329 | 8.923 | | | | | | | |
| 011011111 | - 4.326 | 4.945 | | | | | | | |
| 011111111 | - .194 | ——— | — | -.852 | — | -.854 | -.854 | — | -.778 |
| 000000000 | - .065 | -.798 | | | | | | | |
| 100000001 | + .065 | -.634 | -.721 | -.753 | -.734 | -.705 | -.688 | -.647 | -.614 |
| 100011111 | + 3.939 | + 2.965 | | | | | | | |
| 100111111 | + 8.071 | 7.411 | | | | | | | |
| 101011000 | + 11.300 | 10.668 | | | | | | | |
| 101111111 | + 16.336 | ——— | | | | | | | |
| 110000000 | + 16.465 | 15.497 | 15.662 | 15.675 | 15.654 | +15.693 | 15.719 | 15.768 | 15.712 |
| 110101111 | + 22.535 | 21.860 | | | | | | | |
| 110111111 | + 24.681 | 23.954 | | | | | | | |
| 111101111 | + 30.800 | 30.171 | | | | | | | |
| 111111111 | + 32.866 | 32.251 | 32.234 | 32.218 | 32.231 | 32.250 | 32.271 | 32.340 | 32.32 |

Full scale Cal. H.L

Full scale Cal. L.L. 3111e4/c1

Zero Cal. H.L. 2000c1/13

Zero Cal. L.L.

NOT REPRODUCIBLE

3. CIAM Low Level Module

The general comments and recommendations for the high level data module also apply the high level portion of the CIAM module; however, in addition, there are some unique problems with the CIAM module as a result of the additional amplifiers and calibration multiplexer. The accuracy of the CIAM module is somewhat less than anticipated or desired and again the problem is basically a noise pick up problem. The problem is most severe with the high gain (±30mv) modules as would be expected. The overall module accuracy for these modules is about ±2-3% and this was after adding decoupling resistors and capacitors on each amplifier board. Without this decoupling, operation was practically impossible. The amplifiers when tested independent of the module are generally quite satisfactory and basically meet all of the original specifications except for excessive offset on some amplifiers; however, after interconnecting the module, the operation is rather poor. In addition, the positive supply voltage required to handle the maximum positive input signals (+33 or +55 millivolts) is in excess of the system supply (approximately +7.5v compared to +6.5v available), therefore, the modules cannot operate to the full input range on the positive input signals. The decoupling resistors in the supply voltage lines are partially the cause of this, but the amplifiers themselves need approximately 1.5 - 2.0 volts of supply voltage above the maximum positive output signal (5.5 volts). This in itself is a disadvantage of the CIAM module compared to the CMIA type.

Another problem with the CIAM module compared to the CMIA approach is that the calibration procedure is not directly compatible with the

high level module procedure while the CMIA module is completely compatible. The calibration multiplexer in the CIAM module has also been somewhat of a problem due to its large size and large number of input-output pads and in general is rather poor yield. Any redesigns of the CIAM module should possibly consider doing away with the calibrate multiplexer entirely since the temperature performance of the CIAM amplifiers are good (±1% over temperature). This would simplify the module and possibly improve performance.

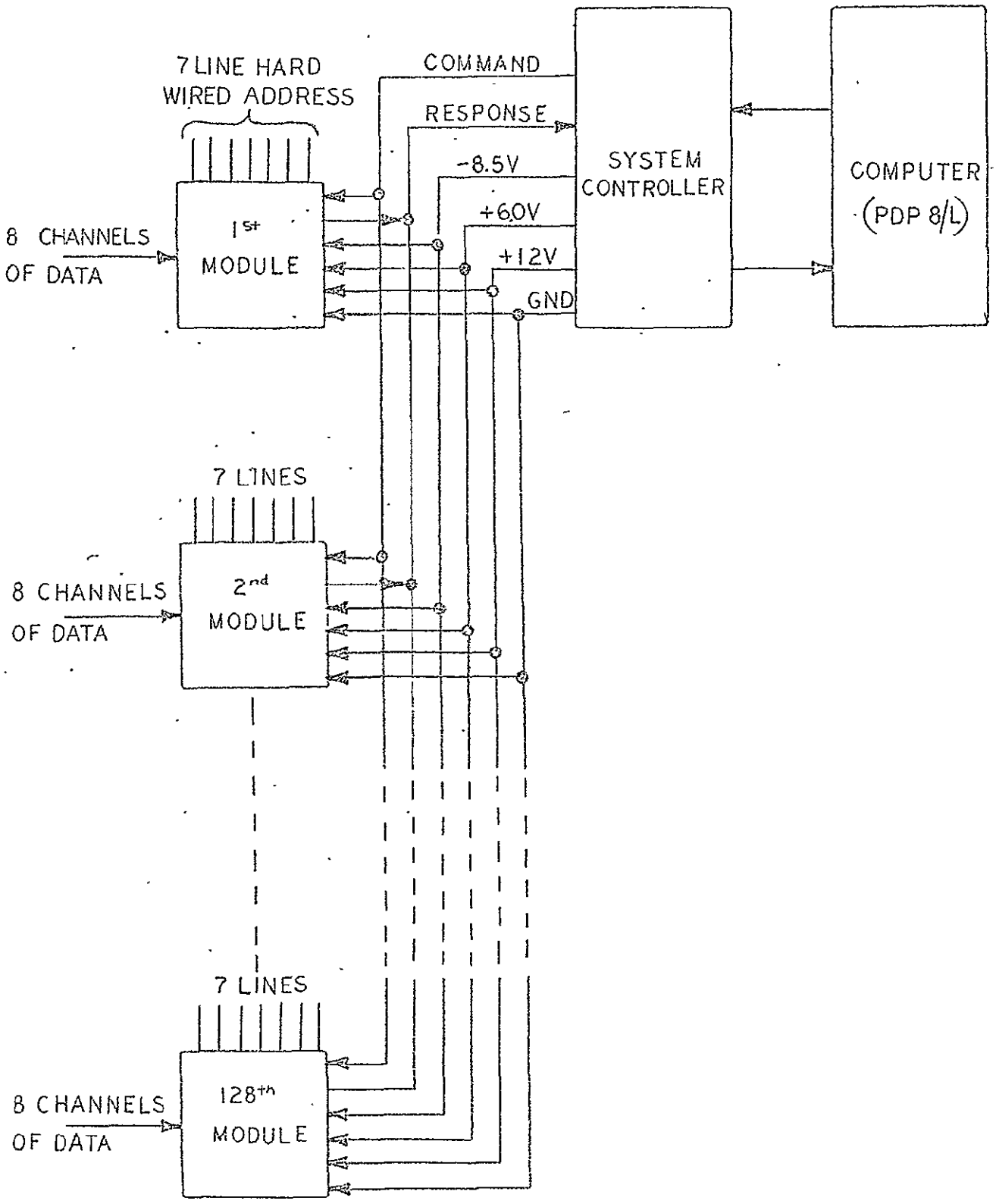
The ±50 millivolt modules are somewhat better than the ±30 millivolt units since they are more stable and less sensitive to noise pick up; however, even these units are not as satisfactory as the CMIA ±30 mvolt modules.

In summary, it can be said that in general the CMIA module is preferred over the CIAM design from the standpoint of performance, cost and ease of fabrication.

The entire low level module program suffered because of last minute deliveries of the hybrid amplifiers, leaving no time for a thorough evaluation or any redesign effort. It is felt that the CMIA modules are generally satisfactory, but could be improved with some slight redesign effort. However, the CIAM module leaves much to be desired and still requires considerably more evaluation and a major redesign to make them acceptable. The nature of the redesign would certainly involve a repackaging effort along with some electrical changes.

It is recommended that future effort along this line be directed towards the CMIA approach since it has the advantages previously mentioned. It is felt that a system using the high level modules and the CMIA

low level modules is a good system which generally meets the original goals of this program. The development effort represents a significant advance in the state-of-the-art in a small size, low power distributed data acquisition system using the most up-to-date integrated circuit techniques. The few modifications which were previously recommended would further improve system accuracy, but as is, the modules and systems provide a very acceptable system for evaluating the basic concept from both a system and a module design.




| MICROELECTRONIC DIVISION GENERAL INSTRUMENT CORPORATION SALT LAKE CITY, UTAH | | | | | REVISION |
|---|---|---|---|---|---|
| TITLE DIGITAL DATA SAMPLING SYSTEM BLOCK DIAGRAM | | | | | PROJECT NASA |
| SCALE | | | | | |
| | DRAWN | CHECKED | PROC. APP. | ENG. APP. | DWG NO |
| BY | K RAE | | | | A 704-5014 |
| DATE | 2-24-70 | | | | |

Figure 1.

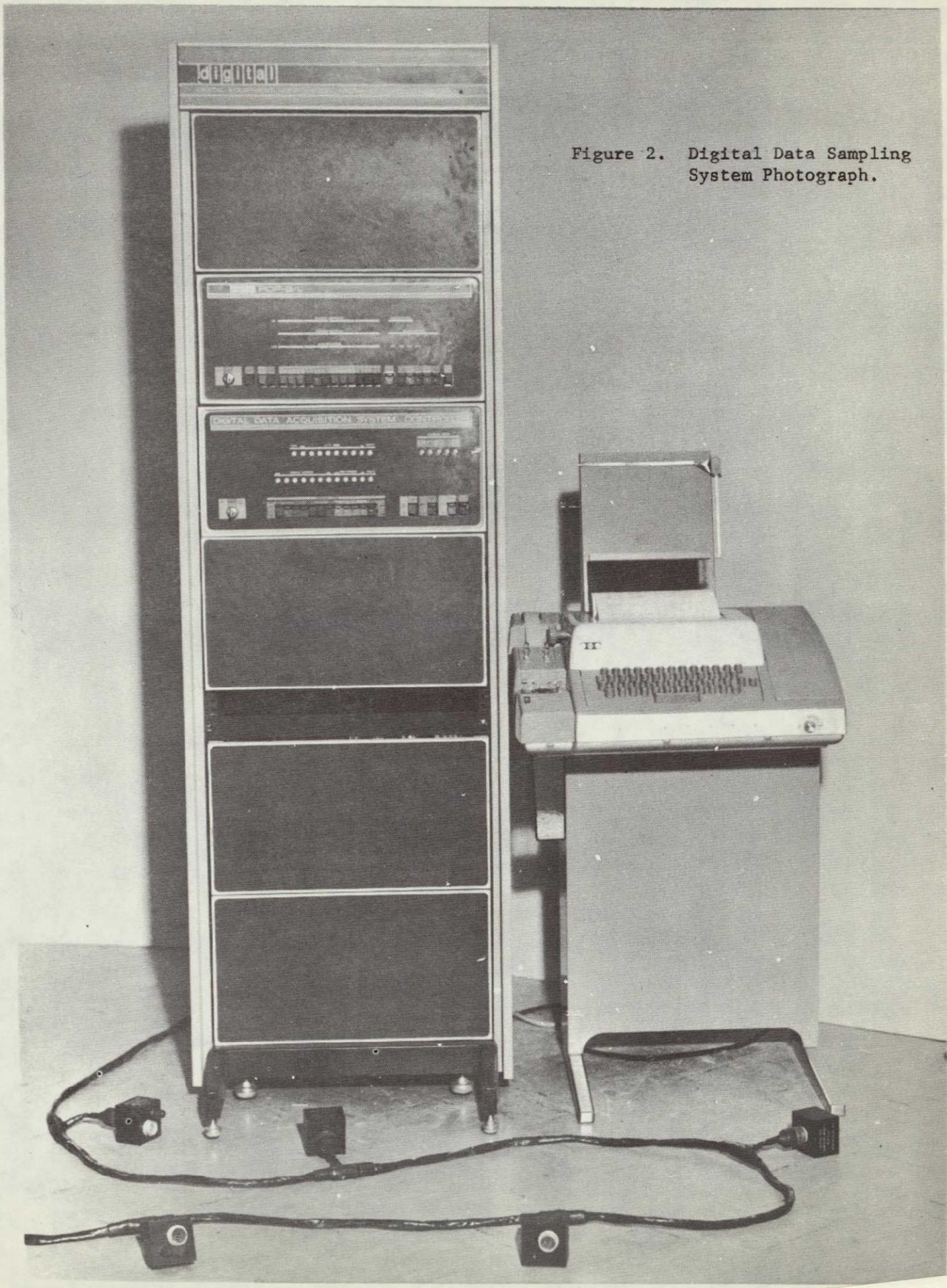
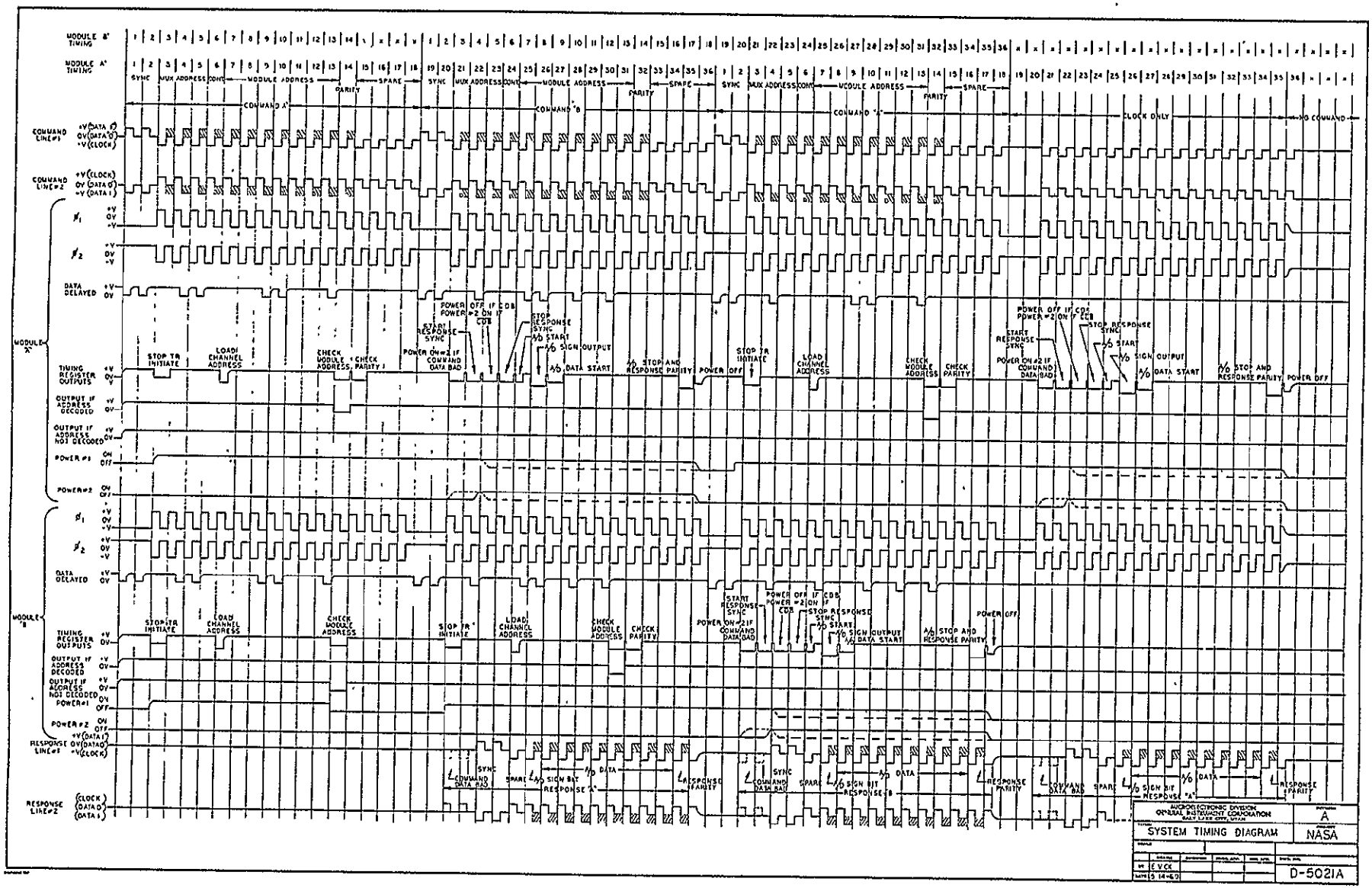



Figure 2. Digital Data Sampling System Photograph.

NOT REPRODUCIBLE




NOT REPRODUCIBLE

Figure 3.

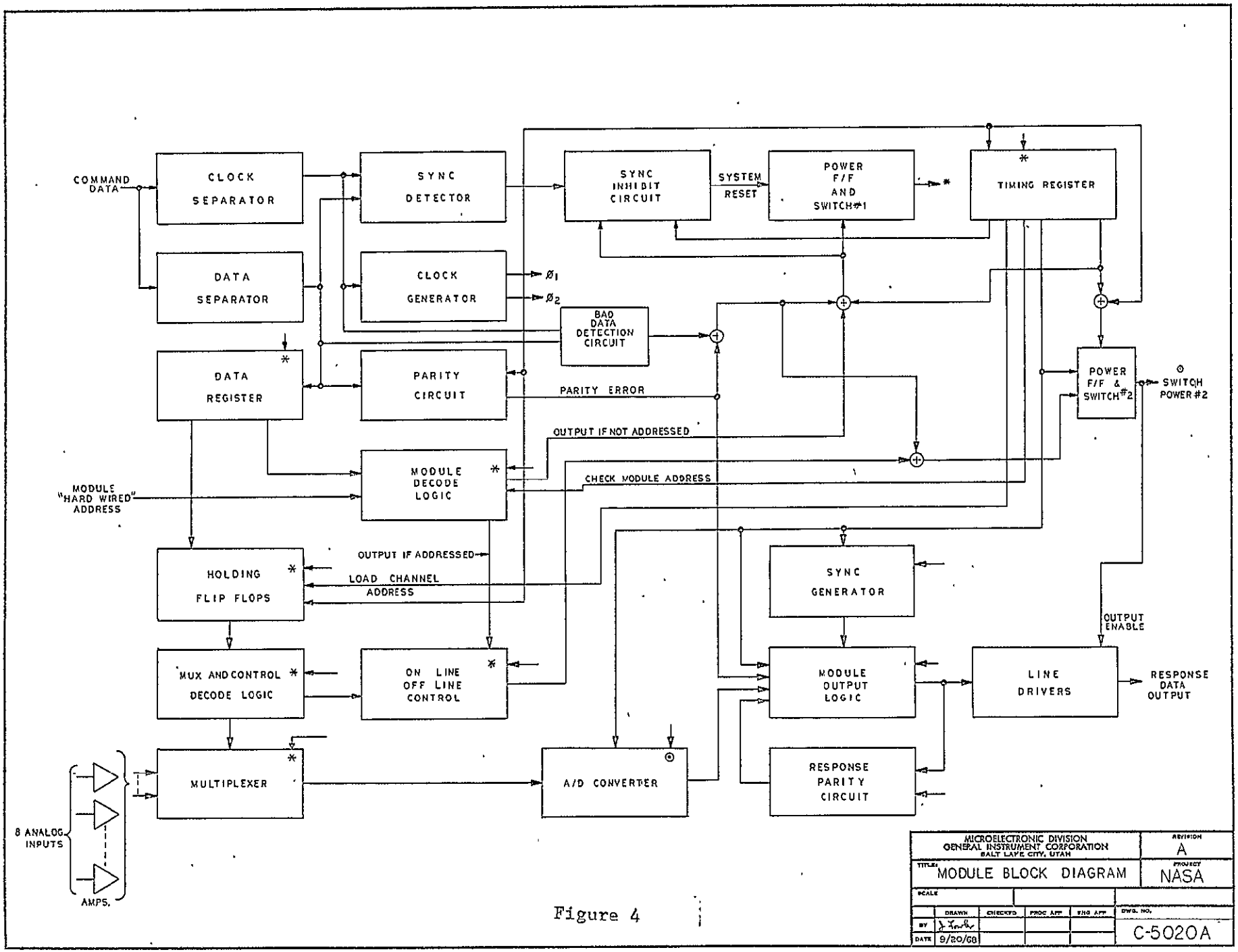



Figure 4

| | | | | | |
|---|---|---|---|---|---|
| MICROELECTRONIC DIVISION GENERAL INSTRUMENT CORPORATION SALT LAKE CITY, UTAH | | | | | REVISION A |
| TITLE: MODULE BLOCK DIAGRAM | | | | | PROJECT NASA |
| SCALE | | | | | |
| | DRAWN | CHECKED | PROC APP | ENG APP | DWG. NO. |
| BY | J. Smith | | | | C-5020A |
| DATE | 9/20/68 | | | | |

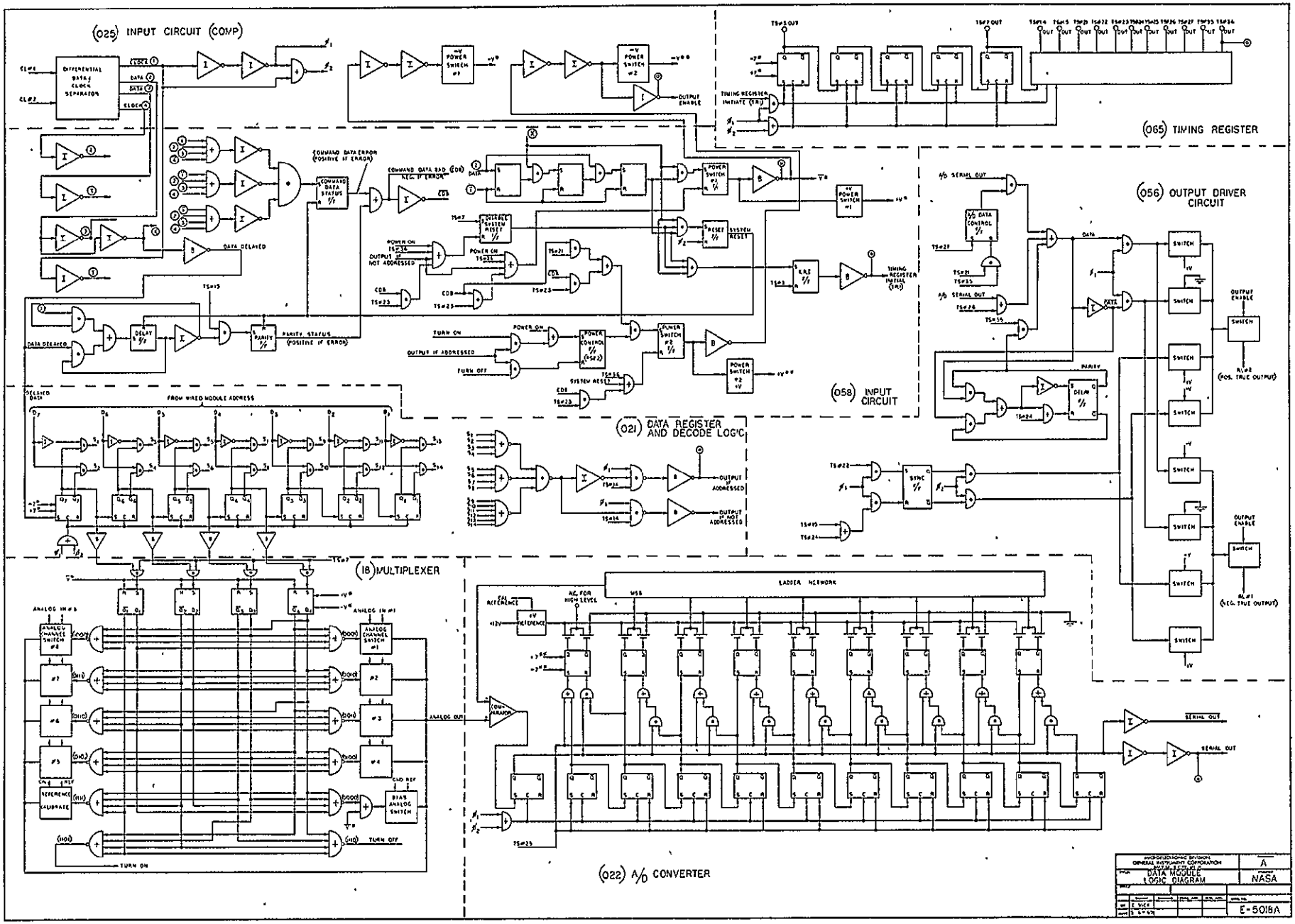

(025) INPUT CIRCUIT (COMP)
(065) TIMING REGISTER
(056) OUTPUT DRIVER CIRCUIT
(058) INPUT CIRCUIT
(021) DATA REGISTER AND DECODE LOGIC
(18) MULTIPLEXER
(022) A/D CONVERTER
DATA MODULE LOGIC DIAGRAM
NASA
E-5018A

Figure 5

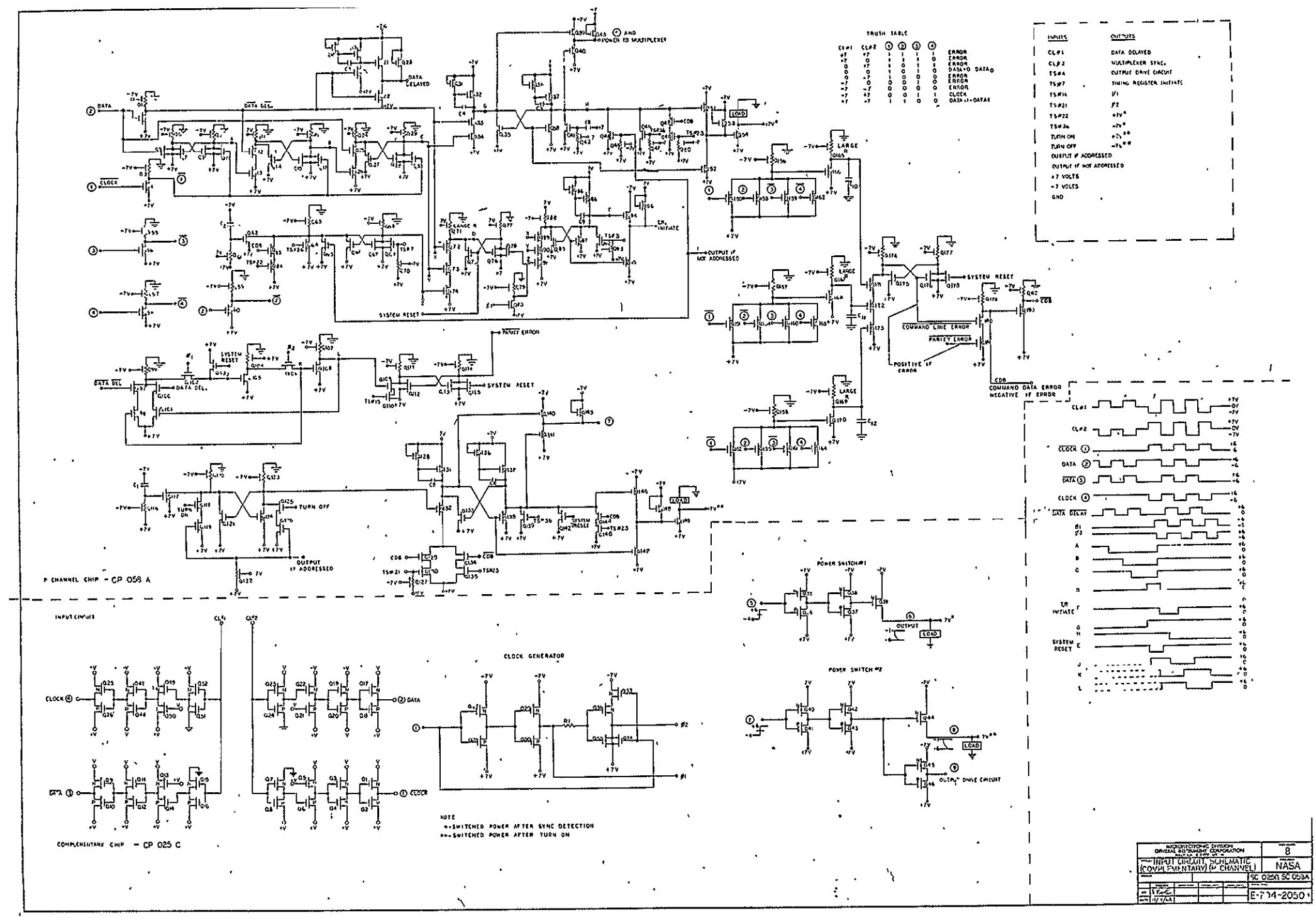

TRUTH TABLE
INPUTS
OUTPUTS
DATA DELAYED
MULTIPLEXER SYNC
OUTPUT DRIVE CIRCUIT
TIMING REGISTER INITIATE
+7 VOLTS
-7 VOLTS
GND
SYSTEM RESET
COMMAND LINE ERROR
PARITY ERROR
POSITIVE IF ERROR
COMMAND DATA ERROR NEGATIVE IF ERROR
OUTPUT IF ADDRESSED
OUTPUT IF NOT ADDRESSED
P CHANNEL CHIP - CP 059 A
INPUT CIRCUITS
CLOCK GENERATOR
POWER SWITCH #1
POWER SWITCH #2
COMPLEMENTARY CHIP - CP 025 C
NOTE
*=SWITCHED POWER AFTER SYNC DETECTION
**=SWITCHED POWER AFTER TURN ON
MICROELECTRONIC DIVISION
INPUT CIRCUIT, SCHEMATIC (COMPLEMENTARY) (P CHANNEL)
8
NASA
SC 0250, SC 059A
E-714-2050

Figure 6

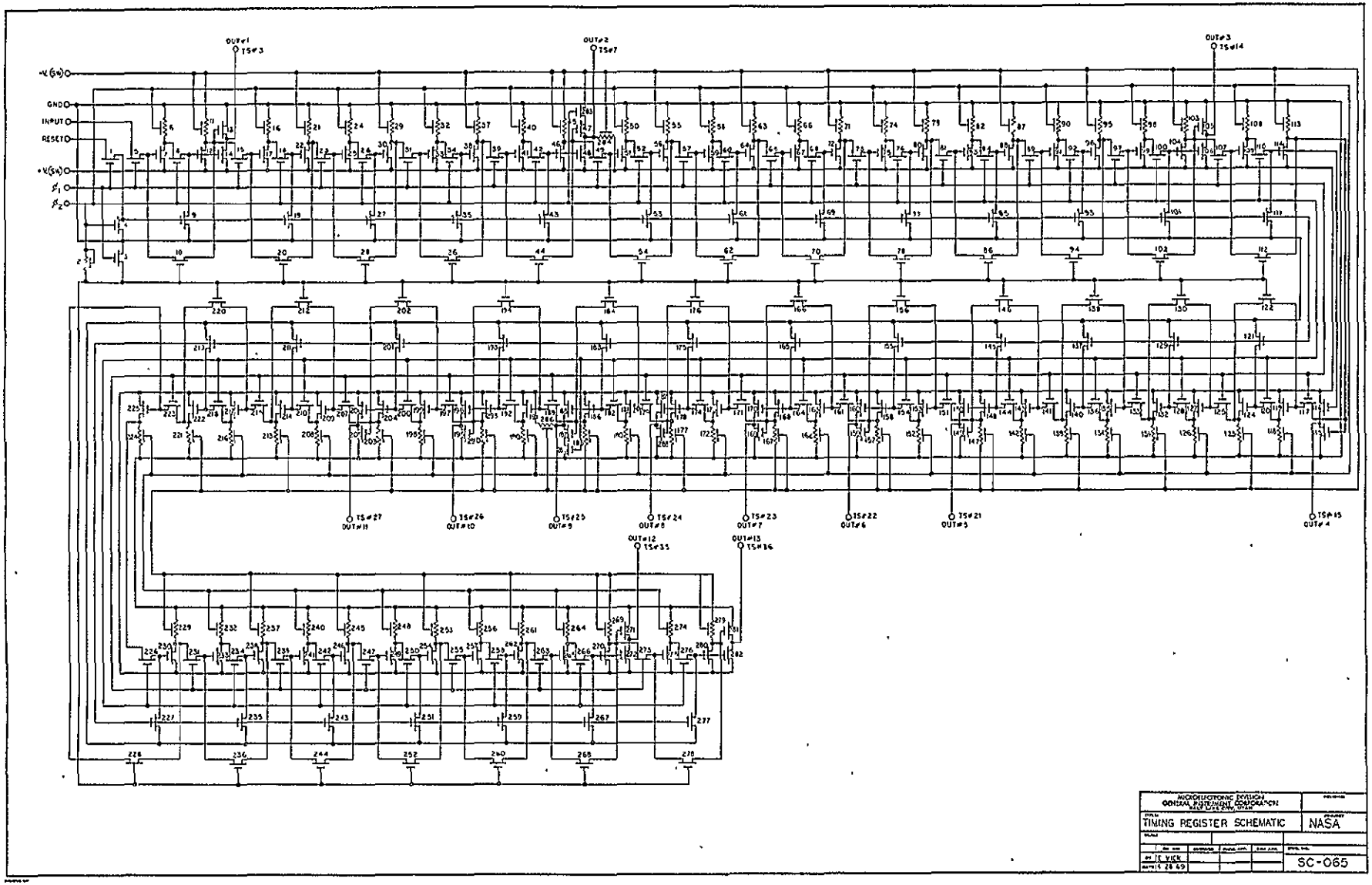



Figure 7

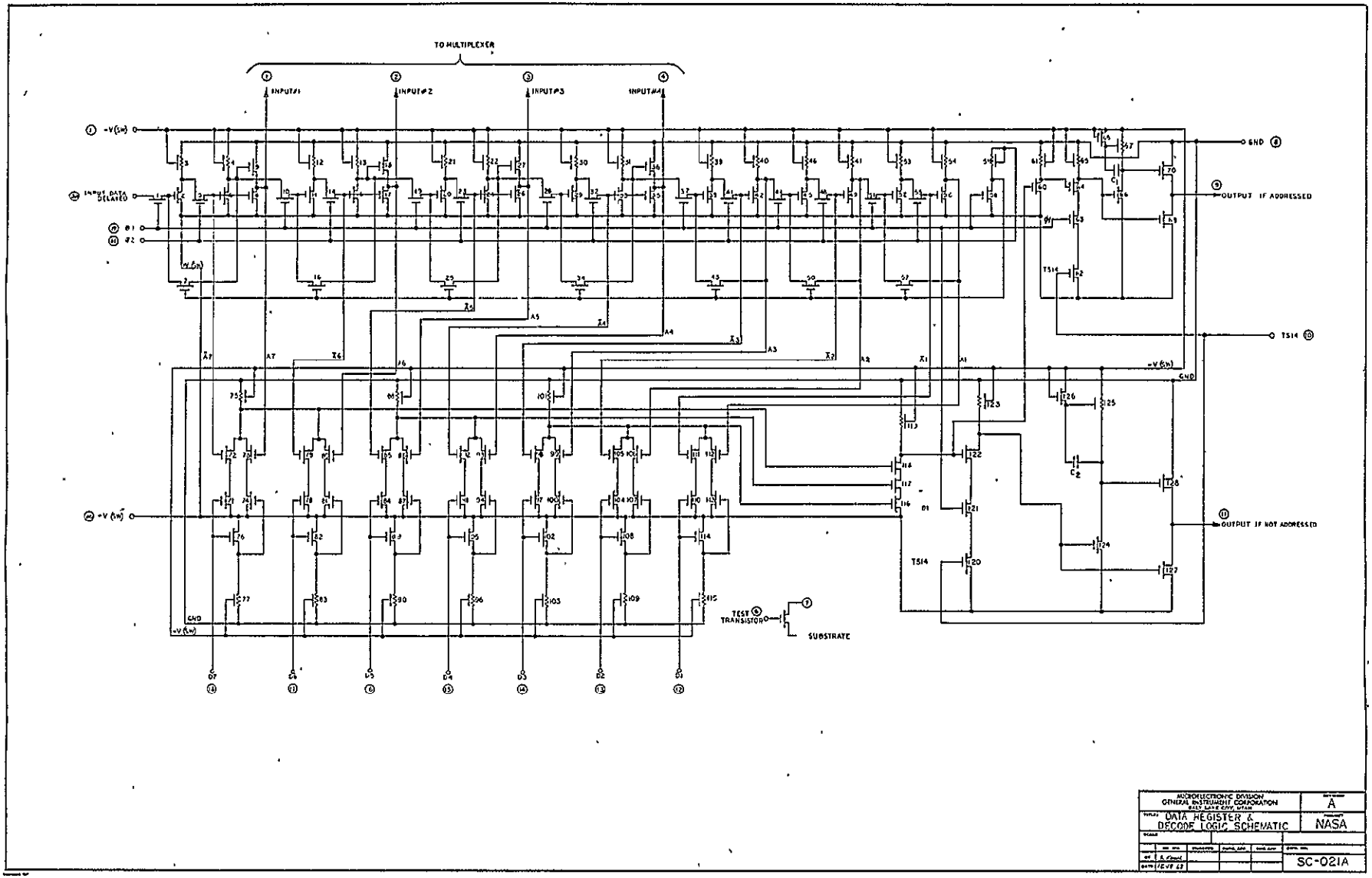

TO MULTIPLEXER
INPUT #1
INPUT #2
INPUT #3
INPUT #4
-V(SW)
INPUT DATA DELAYED
Φ1
Φ2
GND
OUTPUT IF ADDRESSED
TS14
-V(SW)
GND
OUTPUT IF NOT ADDRESSED
-V (SW)
TEST TRANSISTOR
SUBSTRATE
MICROELECTRONIC DIVISION
GENERAL INSTRUMENT CORPORATION
DATA REGISTER & DECODE LOGIC SCHEMATIC
A
NASA
SC-021A

Figure 8

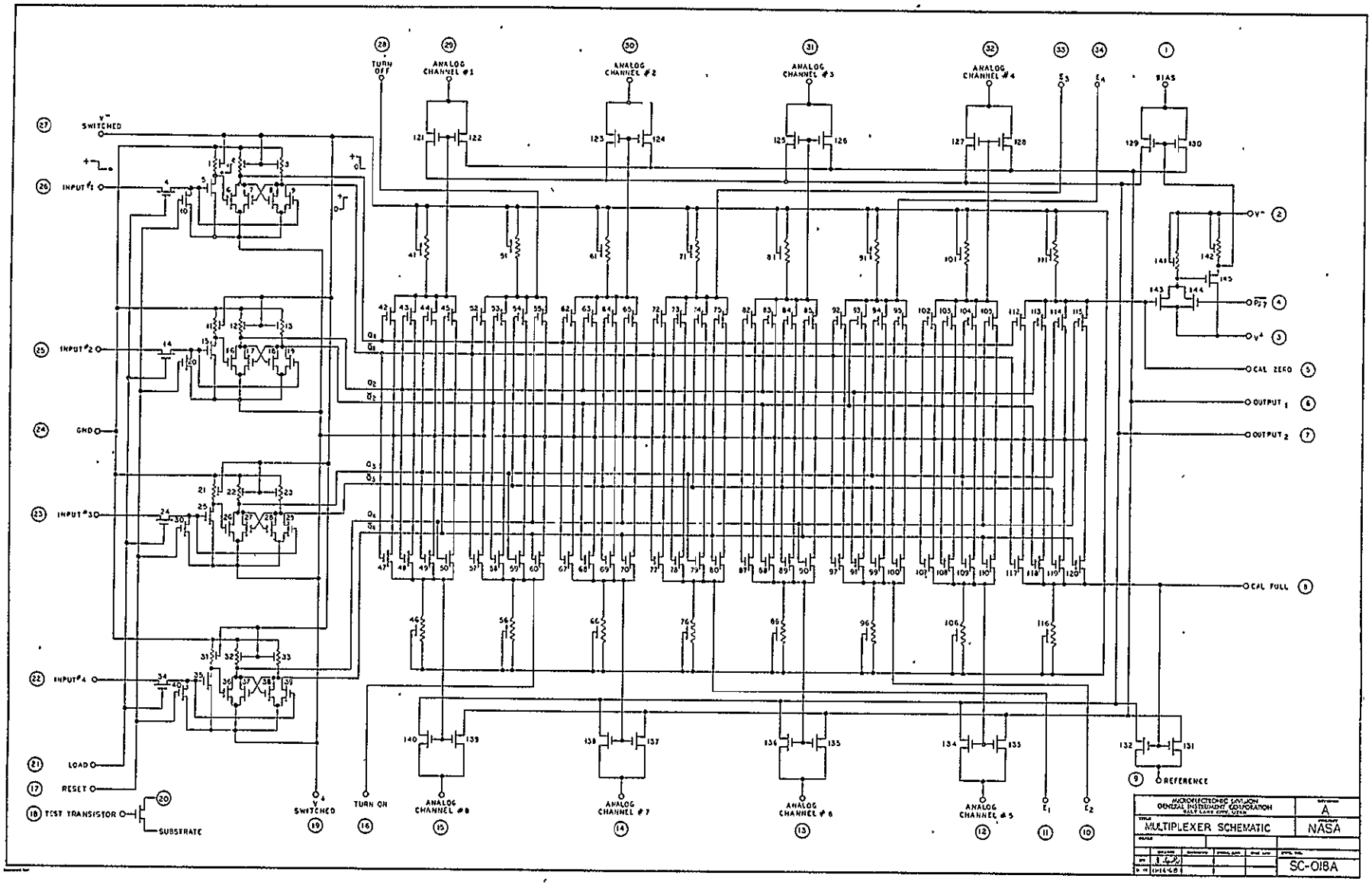
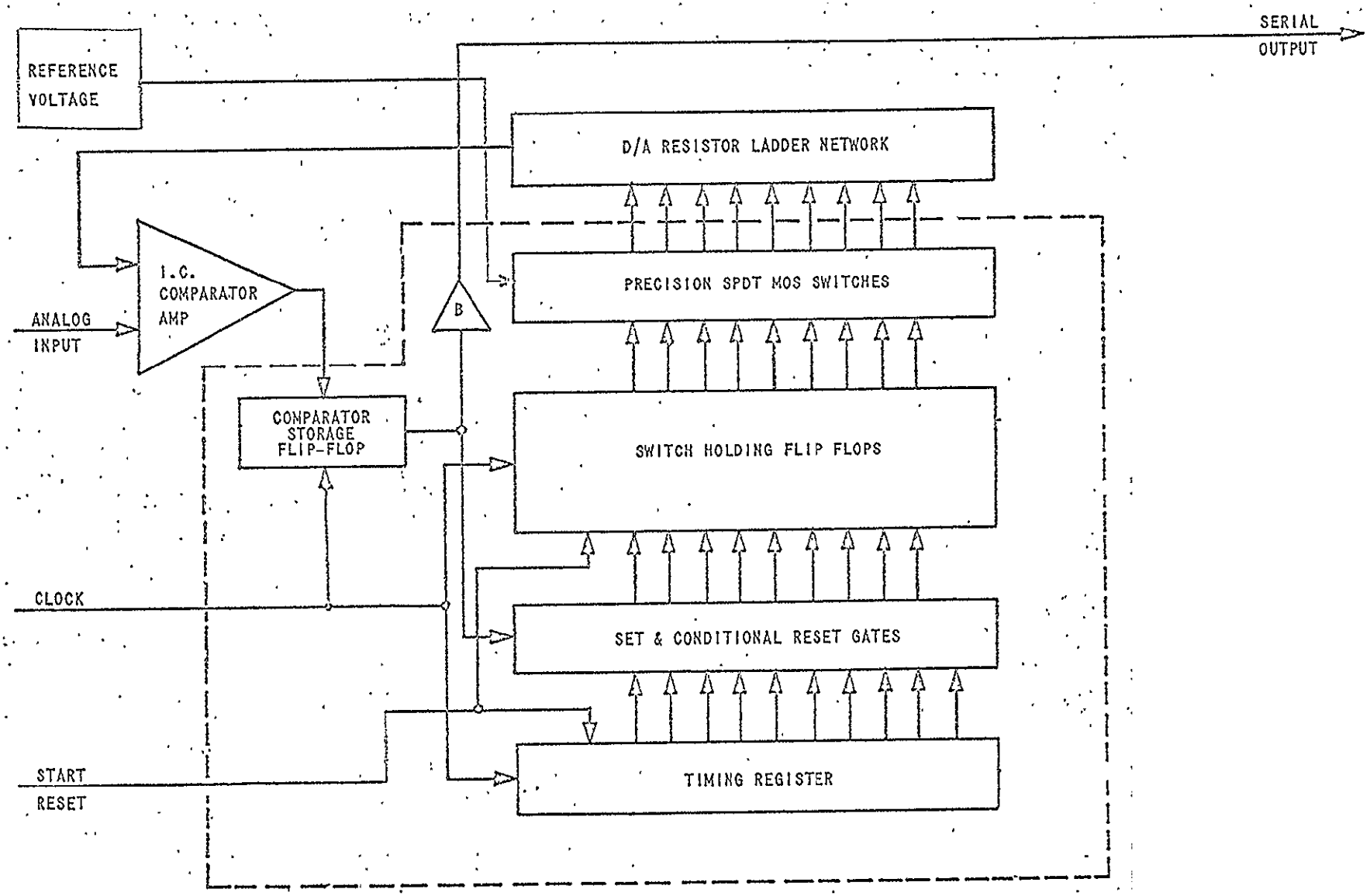

TURN OFF
ANALOG CHANNEL #1
ANALOG CHANNEL #2
ANALOG CHANNEL #3
ANALOG CHANNEL #4
BIAS
V⁻ SWITCHED
INPUT #1
INPUT #2
GND
INPUT #3
INPUT #4
LOAD
RESET
TEST TRANSISTOR
SUBSTRATE
V⁺ SWITCHED
TURN ON
ANALOG CHANNEL #8
ANALOG CHANNEL #7
ANALOG CHANNEL #6
ANALOG CHANNEL #5
V⁻
CAL ZERO
OUTPUT 1
OUTPUT 2
CAL FULL
REFERENCE
MULTIPLEXER SCHEMATIC
A
NASA
SC-018A

Figure 9




BLOCK DIAGRAM MOS A/D CONVERTER DOTTED LINE ENCIRCLES CHIP CIRCUITS

Figure 10

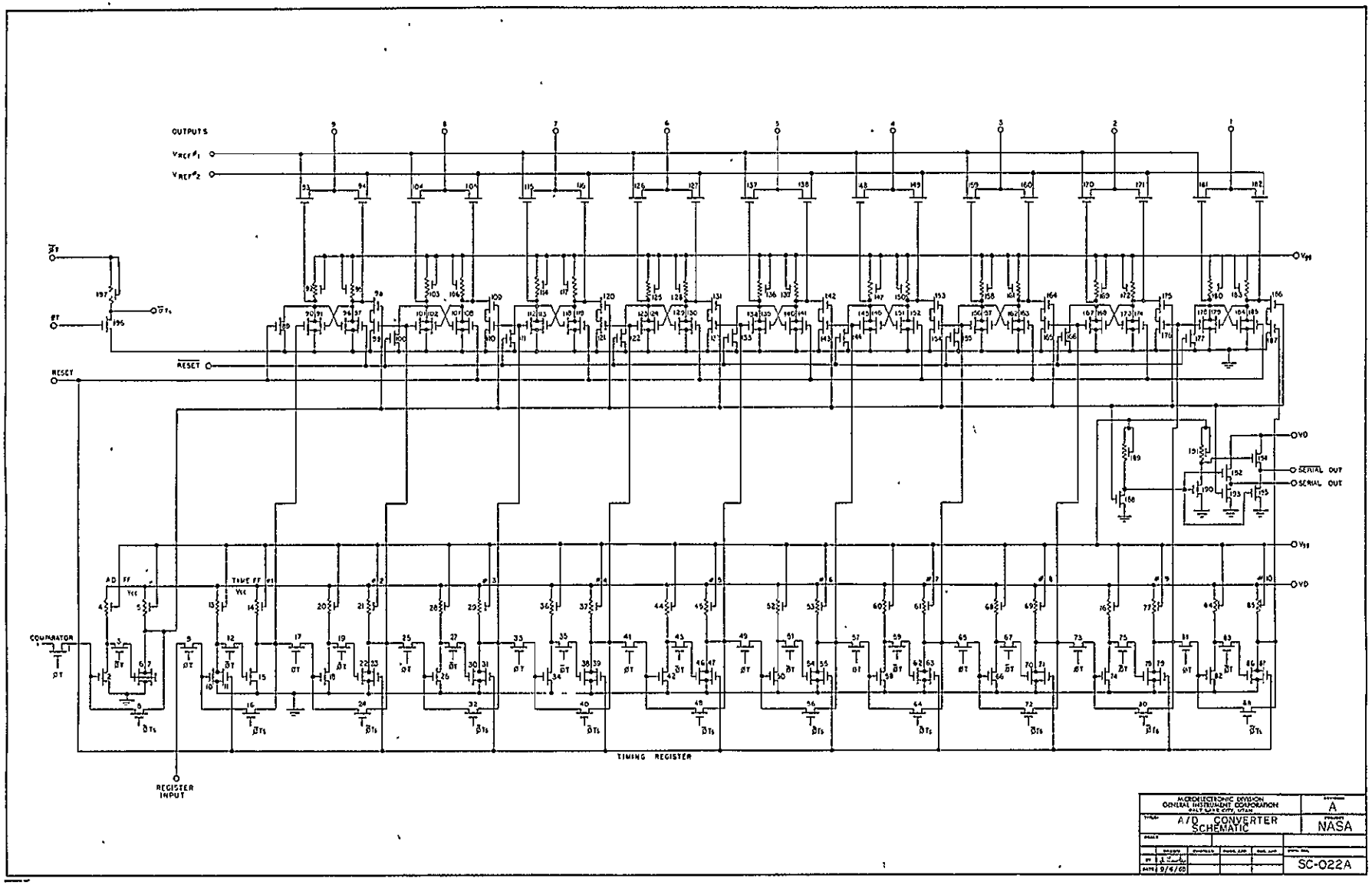
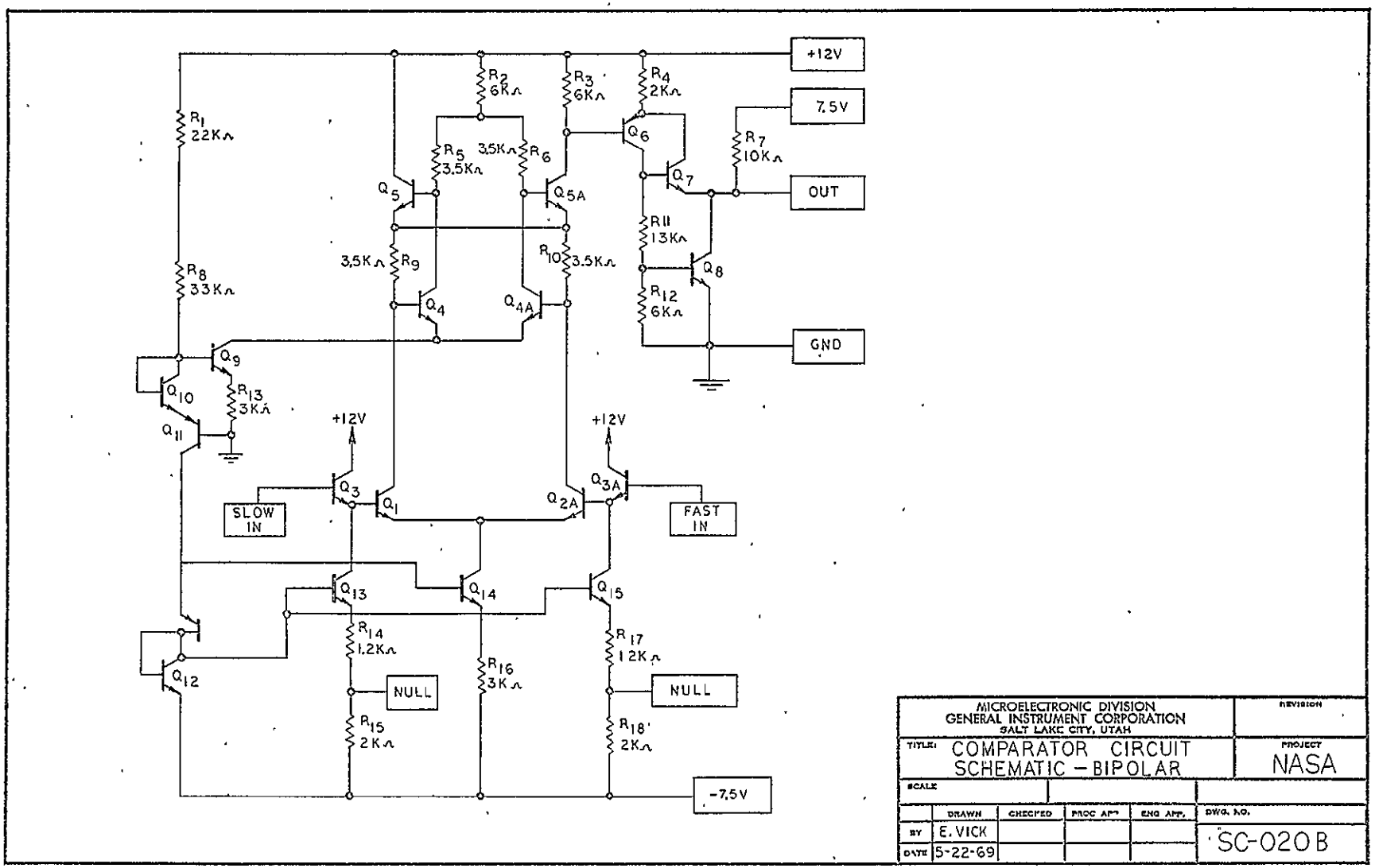

OUTPUTS
RESET
SERIAL OUT
SERIAL OUT
COMPARATOR
REGISTER INPUT
TIMING REGISTER
MICROELECTRONIC DIVISION
GENERAL INSTRUMENT CORPORATION
SALT LAKE CITY, UTAH
A/D CONVERTER SCHEMATIC
NASA
SC-022A

Figure 11




| | | | | | |
|---|---|---|---|---|---|
| MICROELECTRONIC DIVISION GENERAL INSTRUMENT CORPORATION SALT LAKE CITY, UTAH | | | | | REVISION |
| TITLE: COMPARATOR CIRCUIT SCHEMATIC – BIPOLAR | | | | | PROJECT NASA |
| SCALE | | | | | |
| | DRAWN | CHECKED | PROC APP. | ENG APP. | DWG. NO. |
| BY | E. VICK | | | | SC-020B |
| DATE | 5-22-69 | | | | |

Figure 12

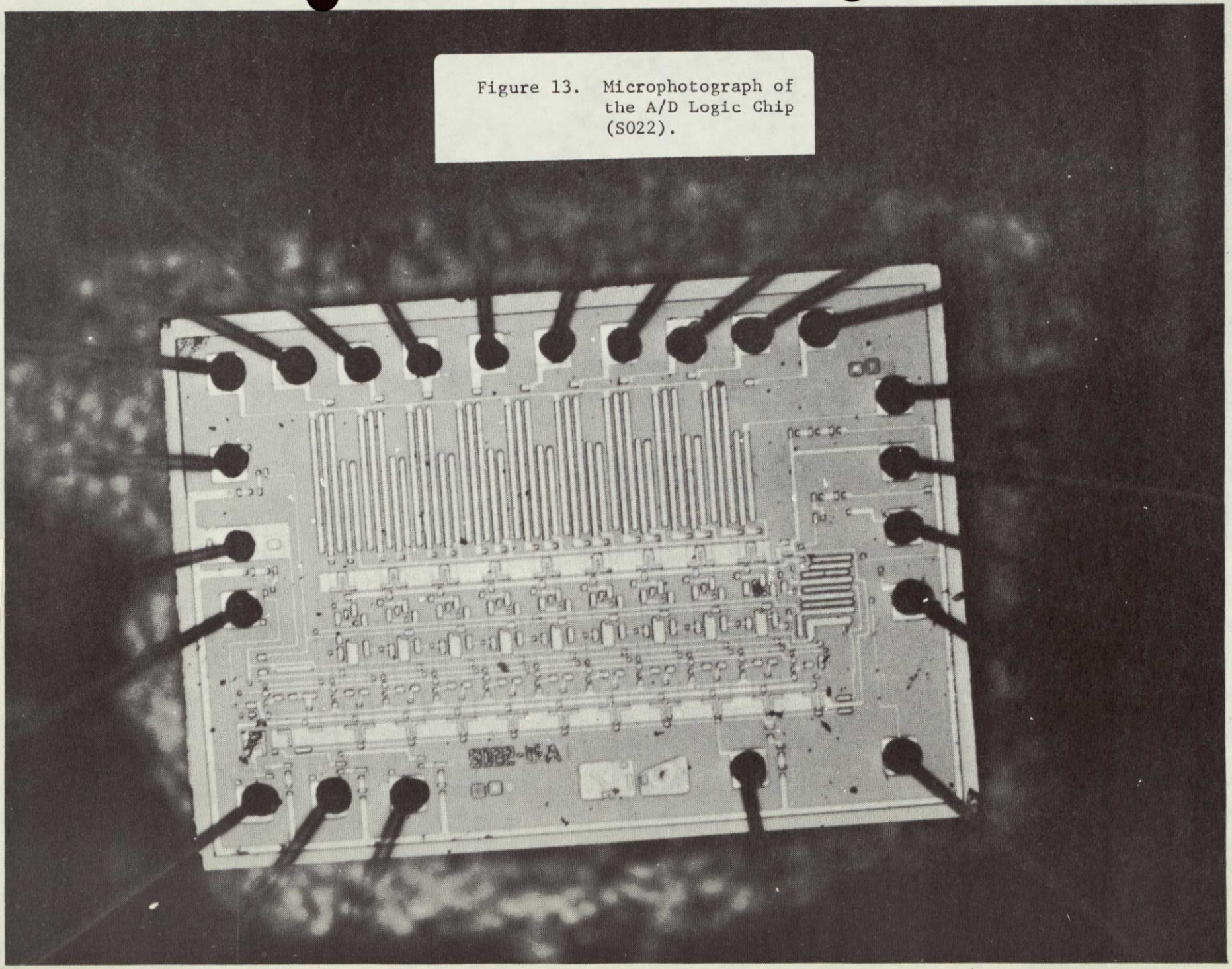


Figure 13. Microphotograph of the A/D Logic Chip (S022).

NOT REPRODUCIBLE

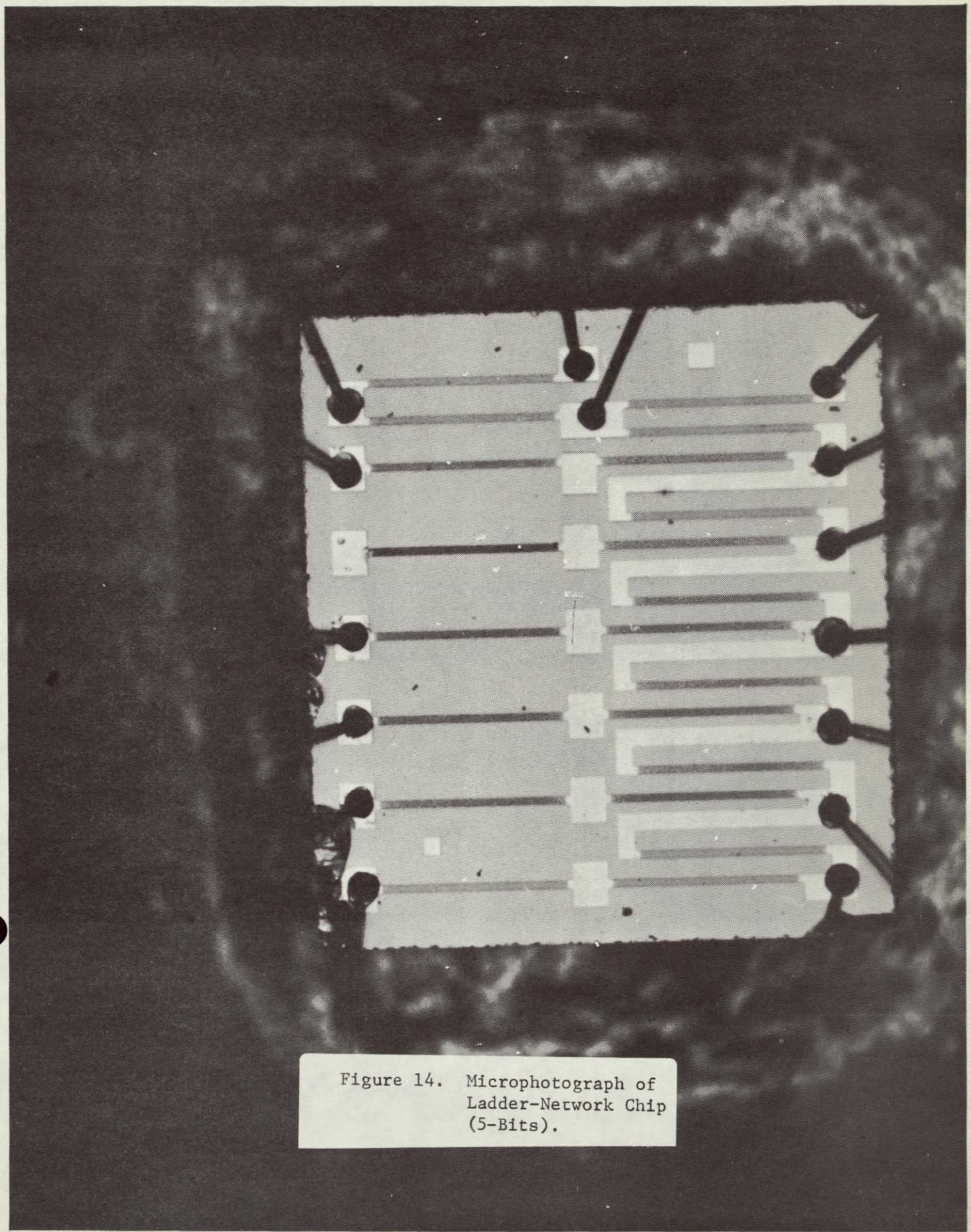
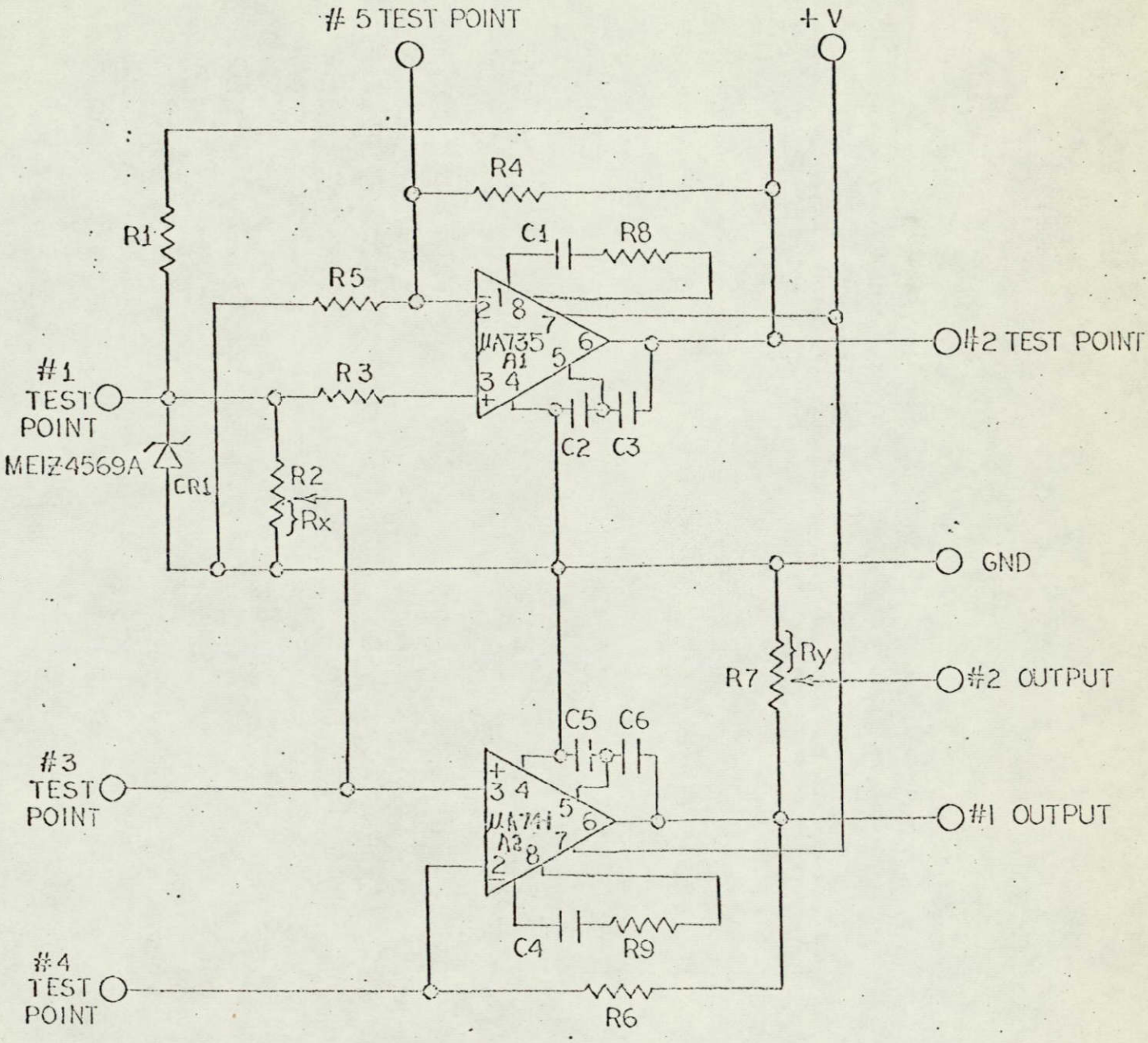


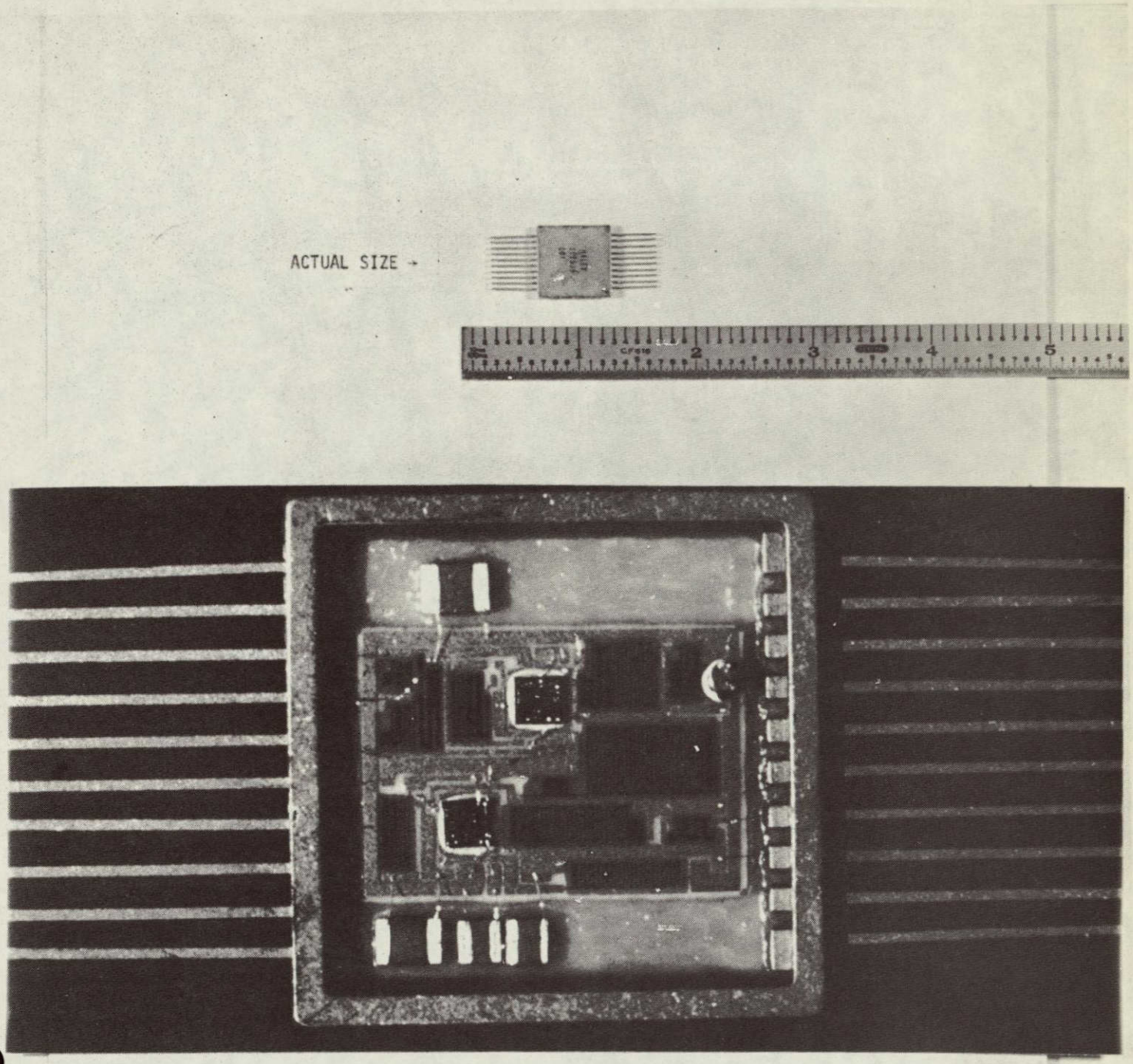
Figure 14. Microphotograph of Ladder-Network Chip (5-Bits).

NOT REPRODUCIBLE




: PRECISION CALIBRATION AND REFERENCE SUPPLY USING μA735 OPERATIONAL AMPLIFIERS.

Figure 15




HYBRID LAYOUT AND PACKAGE.

Figure 16. Reference Supply Hybrid Layout and Package.

NOT REPRODUCIBLE

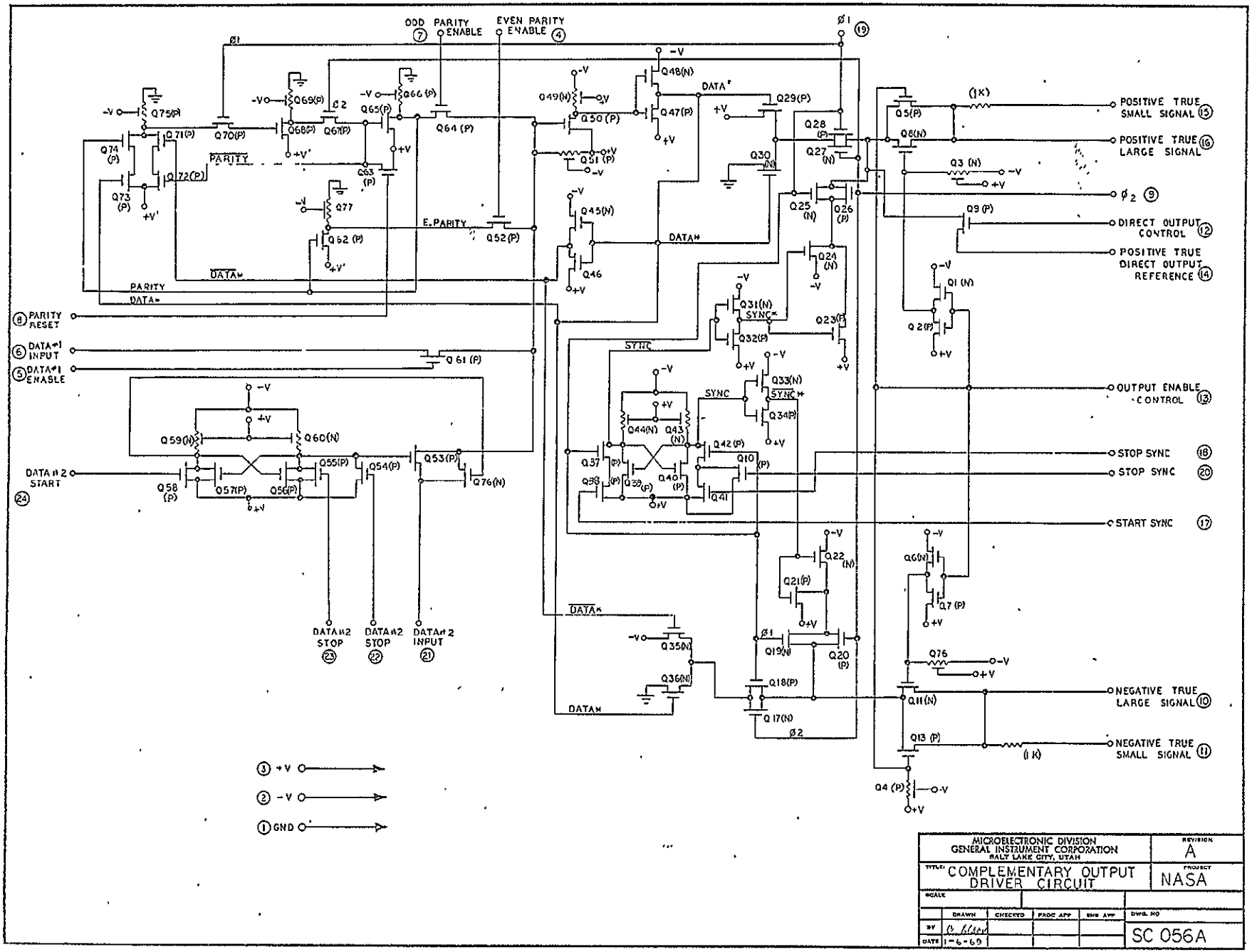
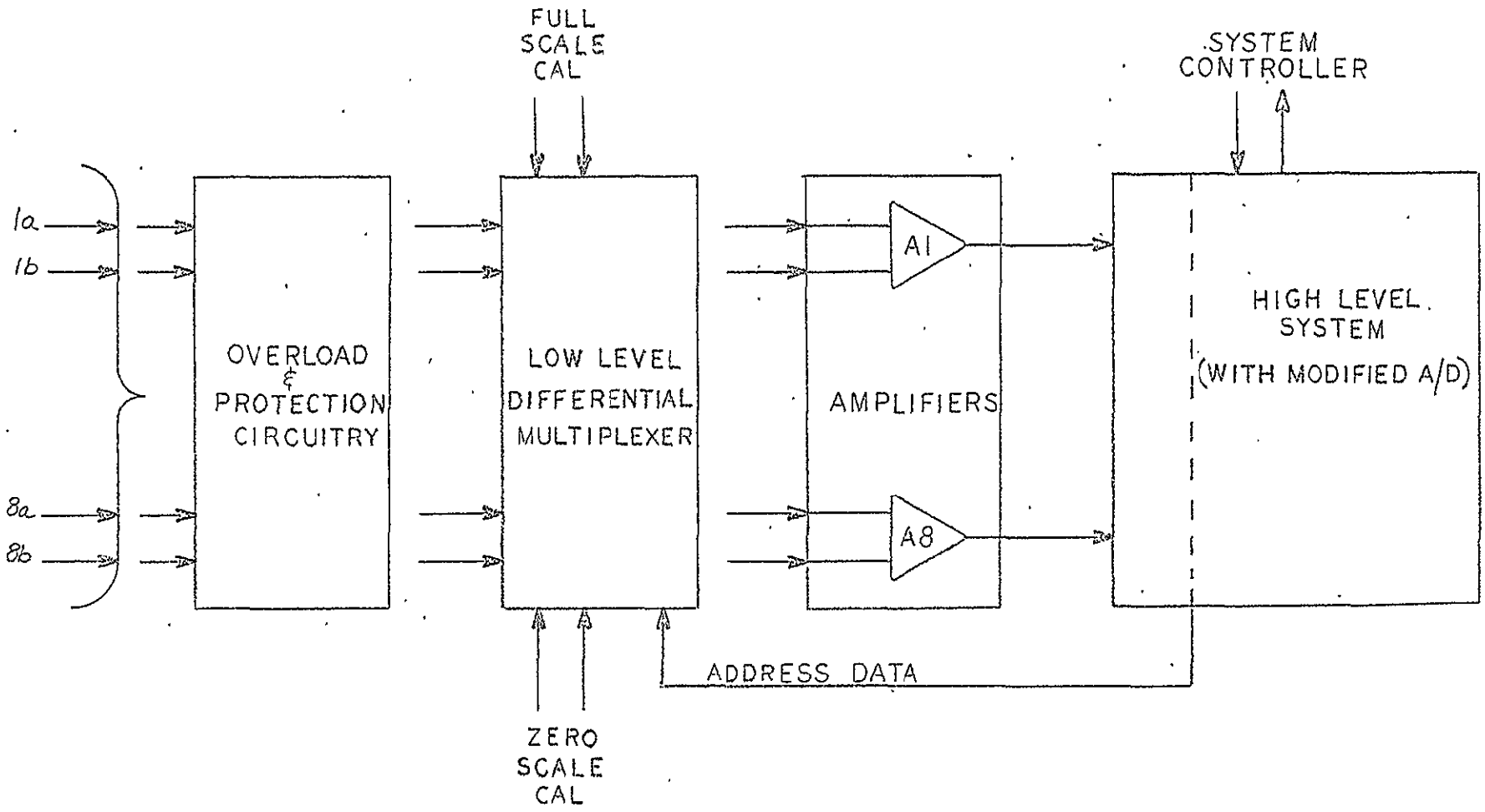
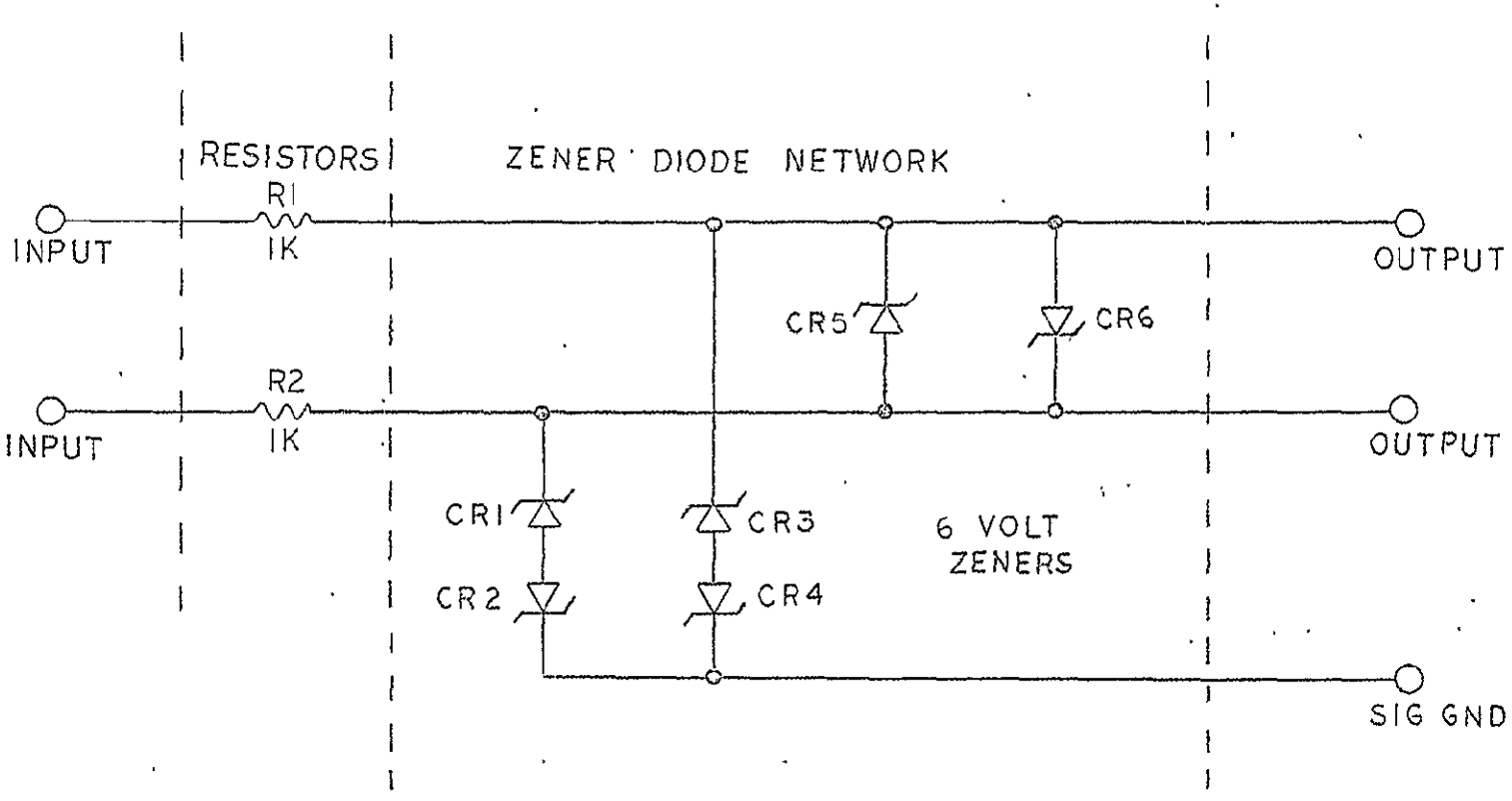

ODD PARITY ENABLE 7
EVEN PARITY ENABLE 4
Ø1 19
POSITIVE TRUE SMALL SIGNAL 15
POSITIVE TRUE LARGE SIGNAL 16
Ø2 9
DIRECT OUTPUT CONTROL 12
POSITIVE TRUE DIRECT OUTPUT REFERENCE 14
OUTPUT ENABLE CONTROL 13
STOP SYNC 18
STOP SYNC 20
START SYNC 17
NEGATIVE TRUE LARGE SIGNAL 10
NEGATIVE TRUE SMALL SIGNAL 11
8 PARITY RESET
6 DATA #1 INPUT
5 DATA #1 ENABLE
24 DATA #2 START
DATA #2 STOP 23
DATA #2 STOP 22
DATA #2 INPUT 21
3 +V
2 -V
1 GND
MICROELECTRONIC DIVISION
GENERAL INSTRUMENT CORPORATION
SALT LAKE CITY, UTAH
REVISION A
TITLE: COMPLEMENTARY OUTPUT DRIVER CIRCUIT
PROJECT NASA
SCALE
DRAWN
CHECKED
PROC APP
ENG APP
DWG. NO
BY
DATE 1-6-69
SC 056A

Figure 17




| | | | | | |
|---|---|---|---|---|---|
| MICROELECTRONIC DIVISION GENERAL INSTRUMENT CORPORATION SALT LAKE CITY, UTAH | | | | | REVISION |
| TITLE: CIAM LOW LEVEL SYSTEM BLOCK DIAGRAM | | | | | PROJECT NASA |
| SCALE | | | | | FIGURE 18 |
| | DRAWN | CHECKED | PROC APP | ENG APP. | DWG NO |
| BY | | | | | A7D-[illegible]016 |
| DATE | 3-1-71 | | | | |




| | | | | | |
|---|---|---|---|---|---|
| MICROELECTRONIC DIVISION<br>GENERAL INSTRUMENT CORPORATION<br>SALT LAKE CITY, UTAH | | | | | REVISION |
| TITLE: LOW LEVEL PROTECTION NETWORK (SINGLE CH.) | | | | | PROJECT: NASA |
| SCALE | | | | | FIGURE 19 |
| | DRAWN | CHECKED | PROC. APP. | ENG. APP. | DWG. NO. |
| BY | [illegible] | | | | A704-2062 |
| DATE | 3-17-71 | | | | |

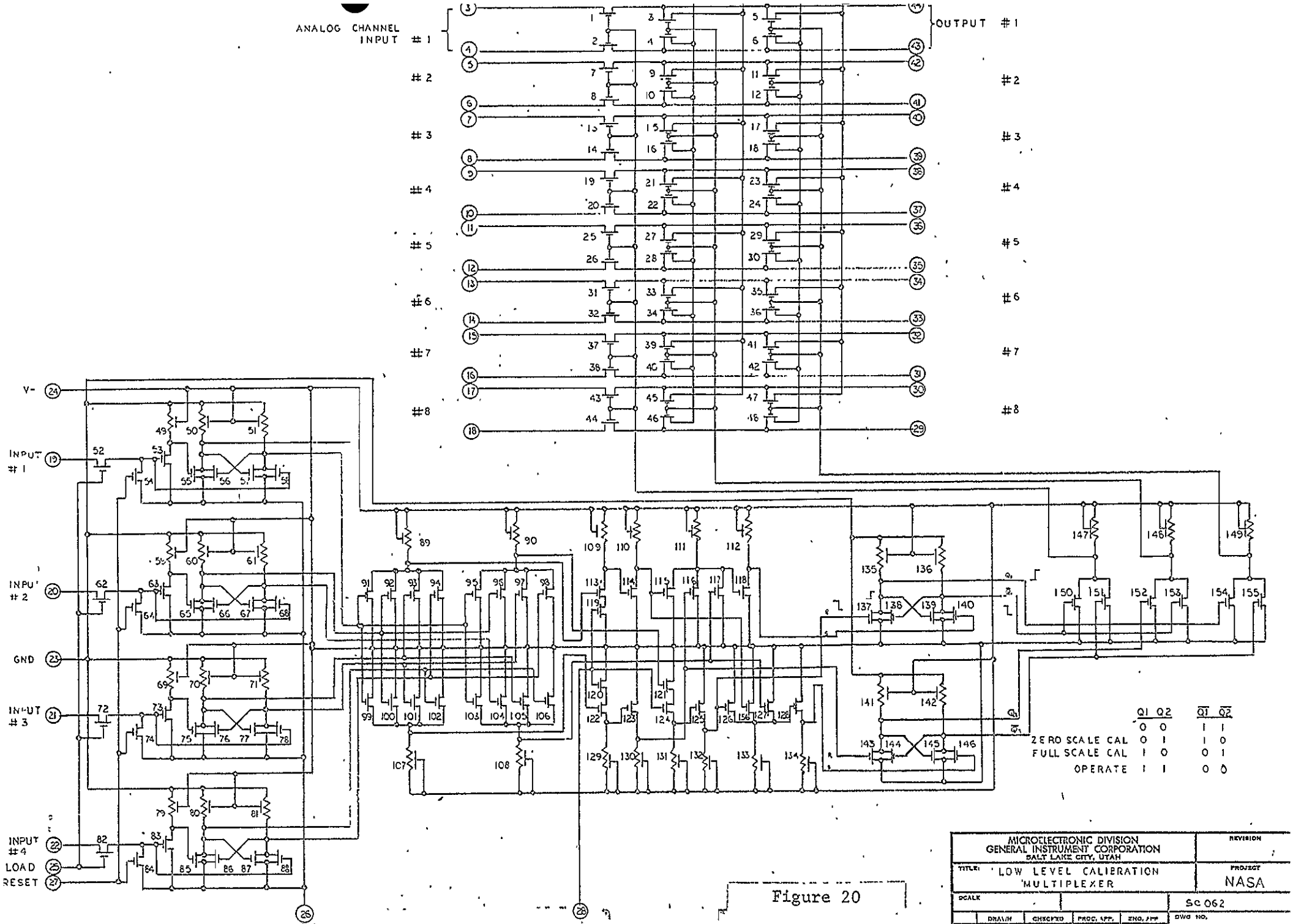
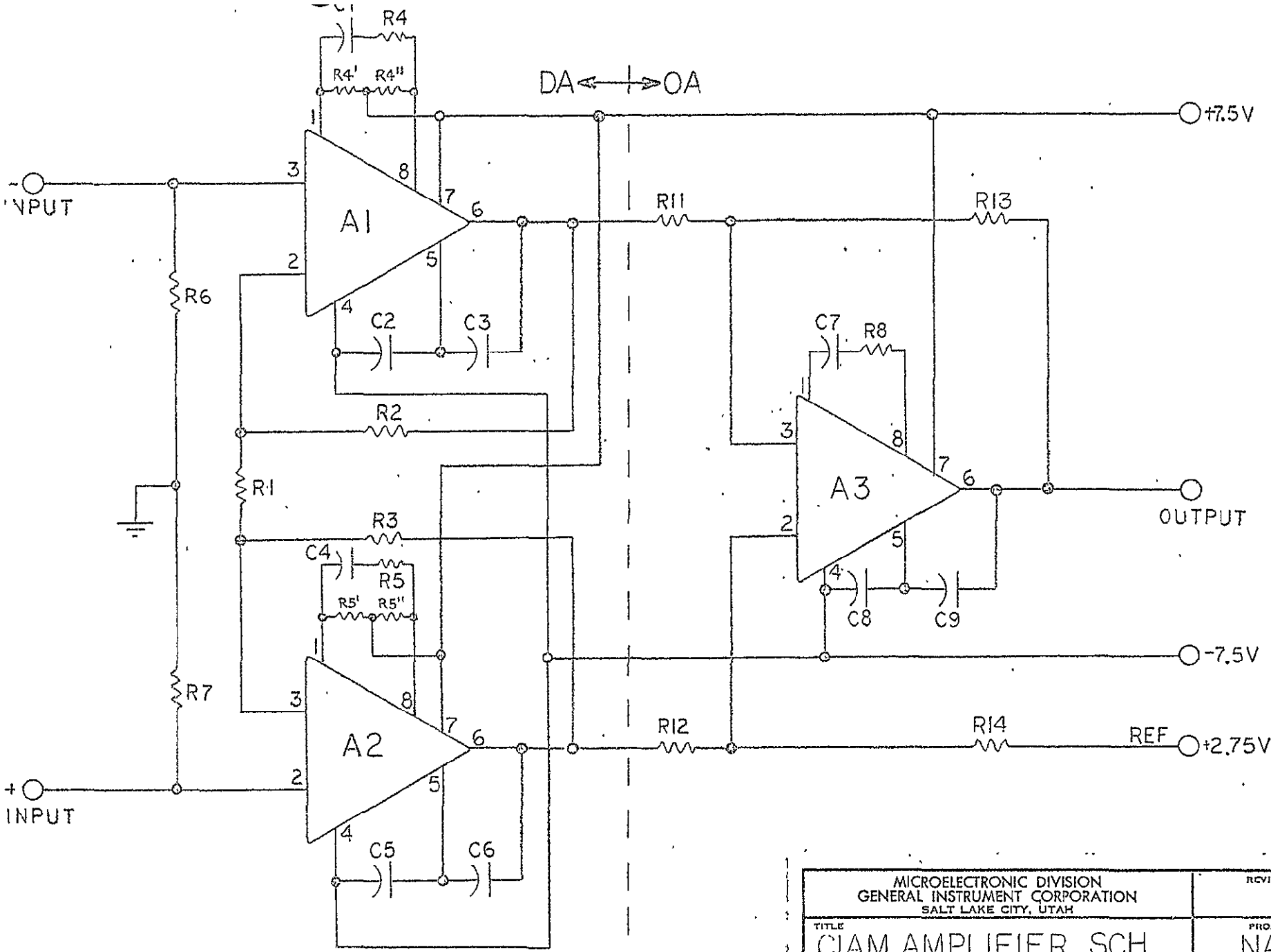



Figure 20

| | | | | | |
|---|---|---|---|---|---|
| MICROELECTRONIC DIVISION GENERAL INSTRUMENT CORPORATION SALT LAKE CITY, UTAH | | | | | REVISION |
| TITLE: LOW LEVEL CALIBRATION MULTIPLEXER | | | | | PROJECT NASA |
| SCALE | | | | | SC 062 |
| | DRAWN | CHECKED | PROD. APP. | ENG. APP. | DWG NO. |
| BY | R.E. Nelson | | | | C-704-2037 |
| DATE | 2-2-60 | | | | |




| | | | | | |
|---|---|---|---|---|---|
| MICROELECTRONIC DIVISION<br>GENERAL INSTRUMENT CORPORATION<br>SALT LAKE CITY, UTAH | | | | | REVISION |
| TITLE<br>CIAM AMPLIFIER SCH | | | | | PROJECT<br>NASA |
| SCALE | | | | | FIGURE 21 |
| | DRAWN | CHECKED | PROG. APP. | ENG. APP. | DWG. NO. |
| BY | | | | | A704 2061 |
| DATE | 11/11 | | | | |

Parts List - Single Amplifier, CIAM System

Operating temperature range: $-20^{\circ}$ to $+85^{\circ}$C

A1, A2 μA 735

A3 μA 735

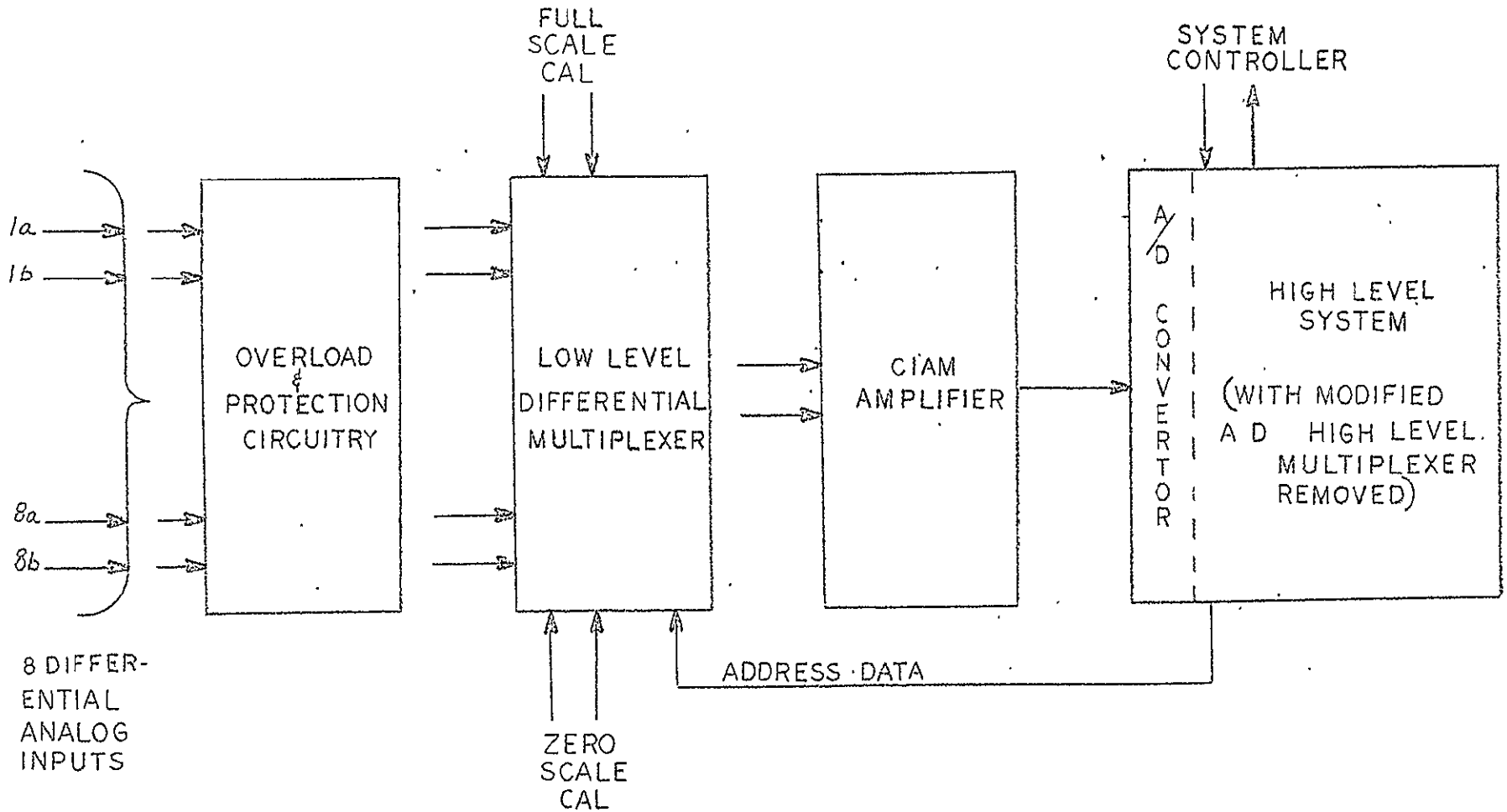
Capacitors*

| | | |
|---|---|---|
| C1, C4, C7 | 0.022μF ± 20% | 25WVDC |
| C2, C5, C8 | 0.0022μF ± 20% | 25WVDC |
| C3, C6, C9 | 180pF ± 20% | 25WVDC |

Resistors

| | | |
|---|---|---|
| R1 | 2KΩ ± 20% | |
| R2, R3 | 15.7KΩ ± 20%, matched to 5% | |
| (R2 + R3)/R1 | 15.67 ± 1% | |
| R4, R5, R8 (Comp) | 22KΩ ± 10% | $R_4' = R_4'' = R_5' = R_5''$ = 4MΩ ± 20% (adjust $R_4'$ and $R_5'$ for zero offset of A1 and A2 respectively) |
| R6, R7 | 50MΩ ± 20%, matched to 6% | |
| R9, R10 | not used | |
| R11, R12 | 50KΩ ± 20% | |
| R13, R14 | 250KΩ ± 20% | |
| R14/R12, R13/R11 | 5.00 ± 1%, matched to 0.1% | |

Figure 22.




| MICROELECTRONIC DIVISION GENERAL INSTRUMENT CORPORATION SALT LAKE CITY, UTAH | | | | REVISION |
|---|---|---|---|---|
| TITLE CIAM LOW LEVEL MODULE BLOCK DIAGRAM | | | | PROJECT NASA |
| SCALE | | | | FIGURE 23 |
| | DRAWN | CHECKED | PROG. APP. | ENG. APP. | DWG. NO. |
| BY | K. Arling | | | | A704 5015 |
| DATE | 5-17-70 | | | | |

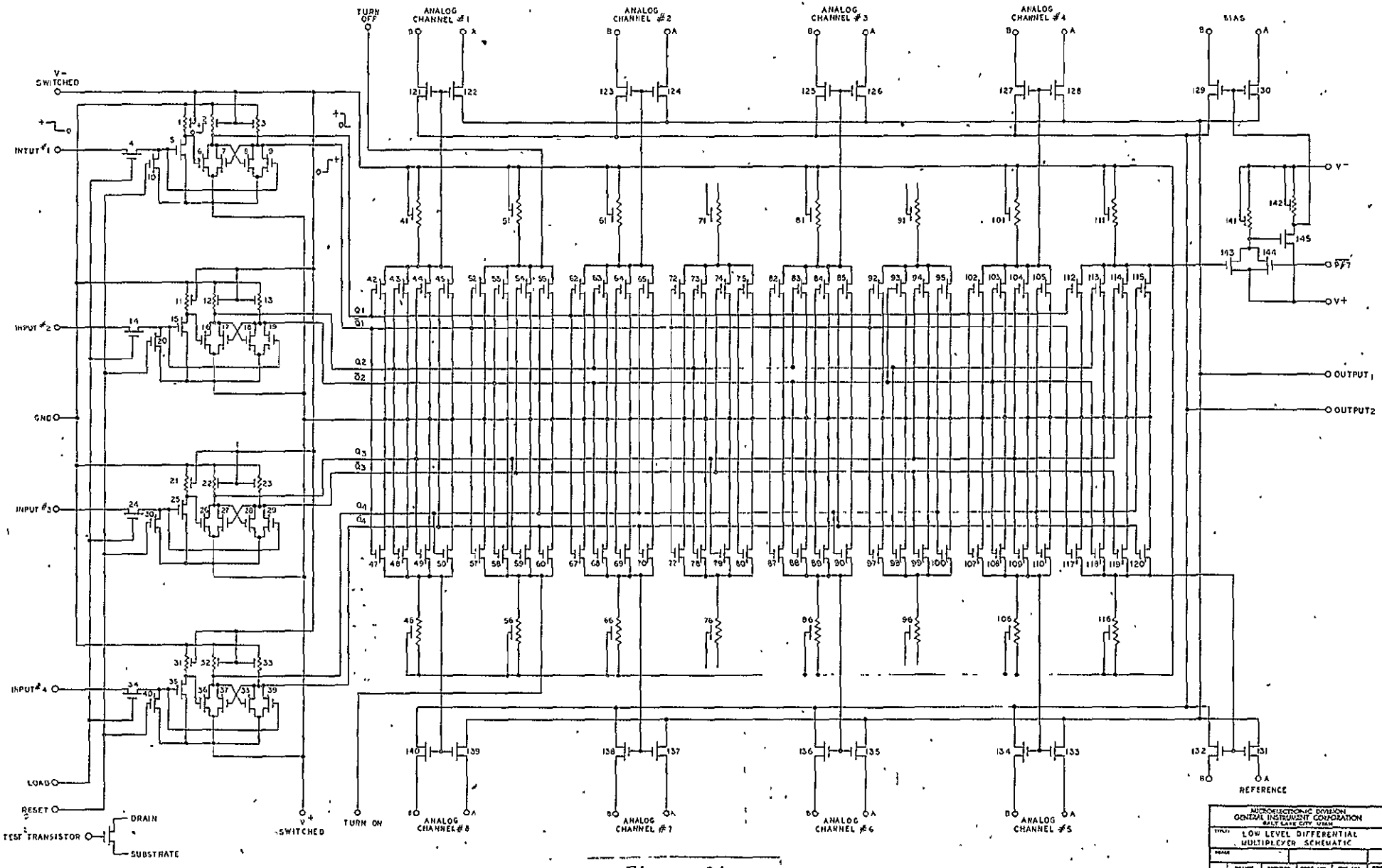
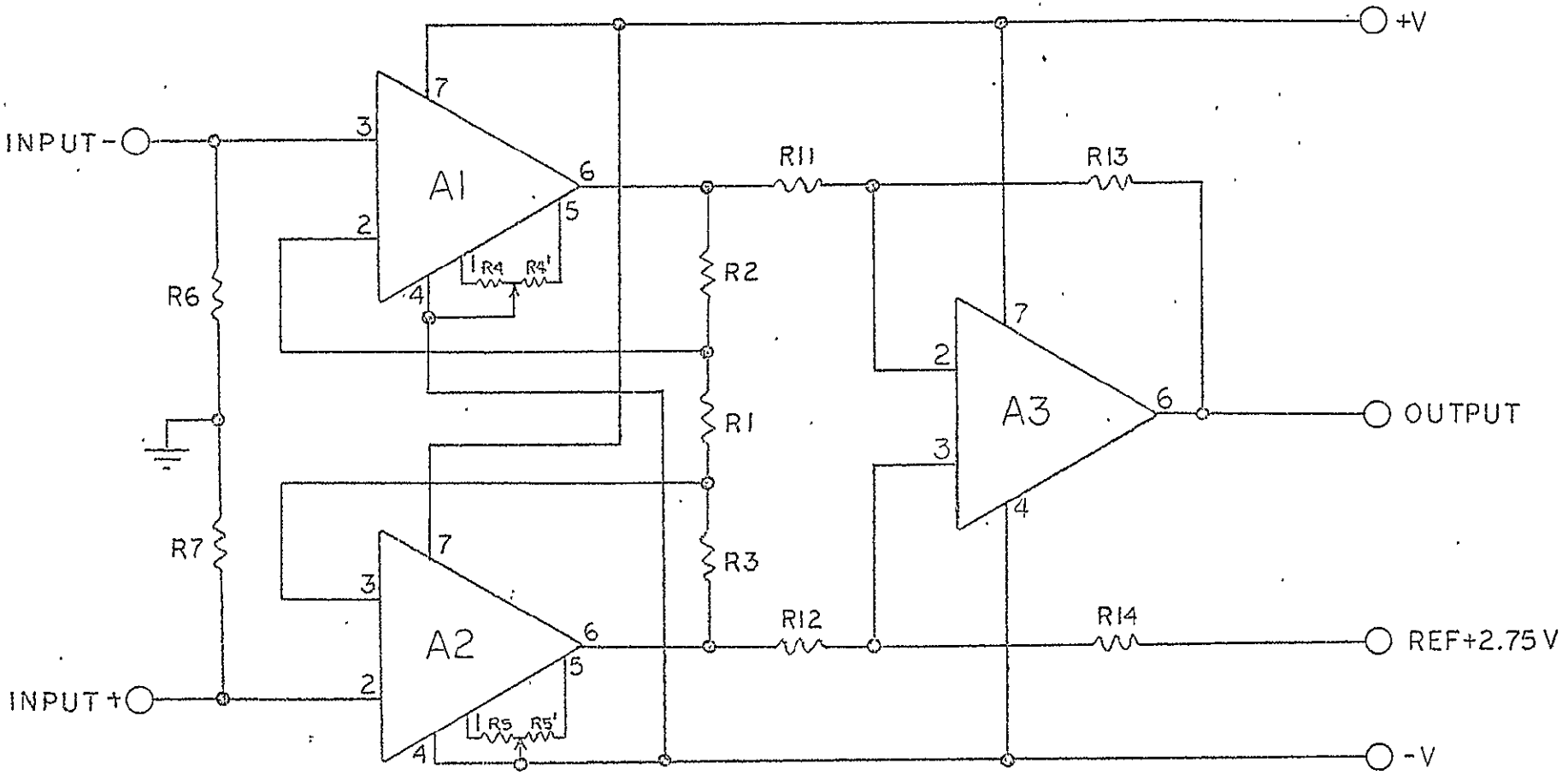



Figure 24

NOT REPRODUCIBLE




| | | | | | |
|---|---|---|---|---|---|
| MICROELECTRONIC DIVISION<br>GENERAL INSTRUMENT CORPORATION<br>SALT LAKE CITY, UTAH | | | | | REVISION |
| TITLE: SCHEMATIC OF CMIA AMPLIFER USING 3MC1556'S | | | | | PROJECT: NASA |
| SCALE | | | | | FIGURE . 25 |
| | DRAWN | CHECKED | PROC APP. | ENG. APP. | DWG. NO |
| BY | | | | | A7014-1016 |
| DATE | 3-1-77 | | | | |

Parts List - Single Amplifier, CMIA System

Operating temperature range: $-20^{o}$ to $+85^{o}C$

| | |
|---|---|
| A1, A2 | MC1556 (Motorola) |
| A3 | MC1556 |

Resistors

| | |
|---|---|
| R1 | 2K ± 20% |
| R2, R3 | 15.7K ± 20%, matched to 5% |
| (R2 + R3)/R1 | 15.67 ± 1% |
| $R_4 = R_4'$ | 5KΩ ± 20% (adjust $R_4'$ and $R_5'$ for zero |
| $R_5 = R_5'$ | 5KΩ ± 20% offset of A1 and A2 respectively) |
| R6, R7 | 50MΩ ± 20%, matched to 6% |
| R9, R10 | not used |
| R11, R12 | 50KΩ ± 20% |
| R13, R14 | 250KΩ ± 20% |
| R14/R12, R13/R11 | 5.00 ± 1%, matched to 0.1% |

FIGURE 26.

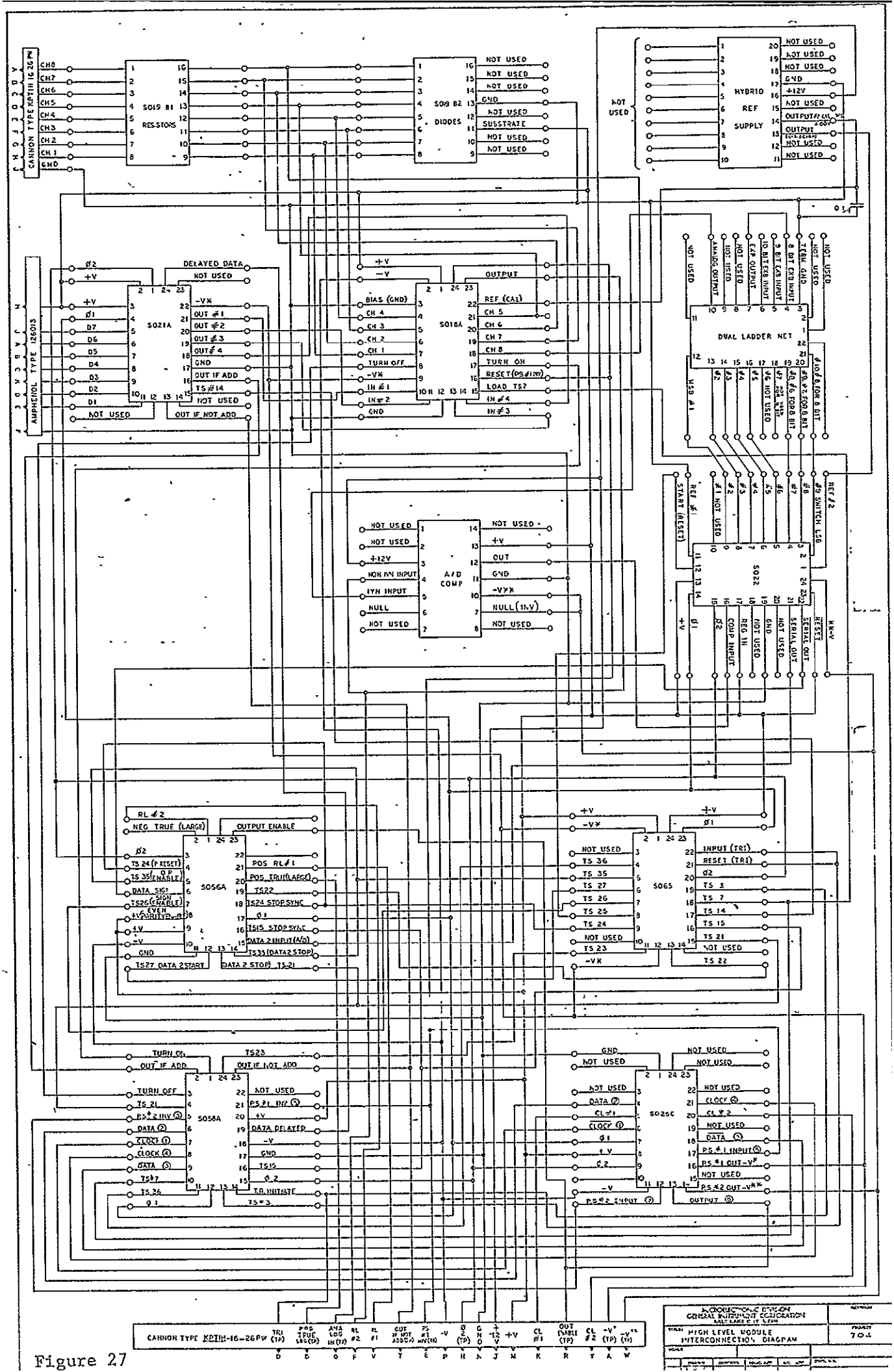
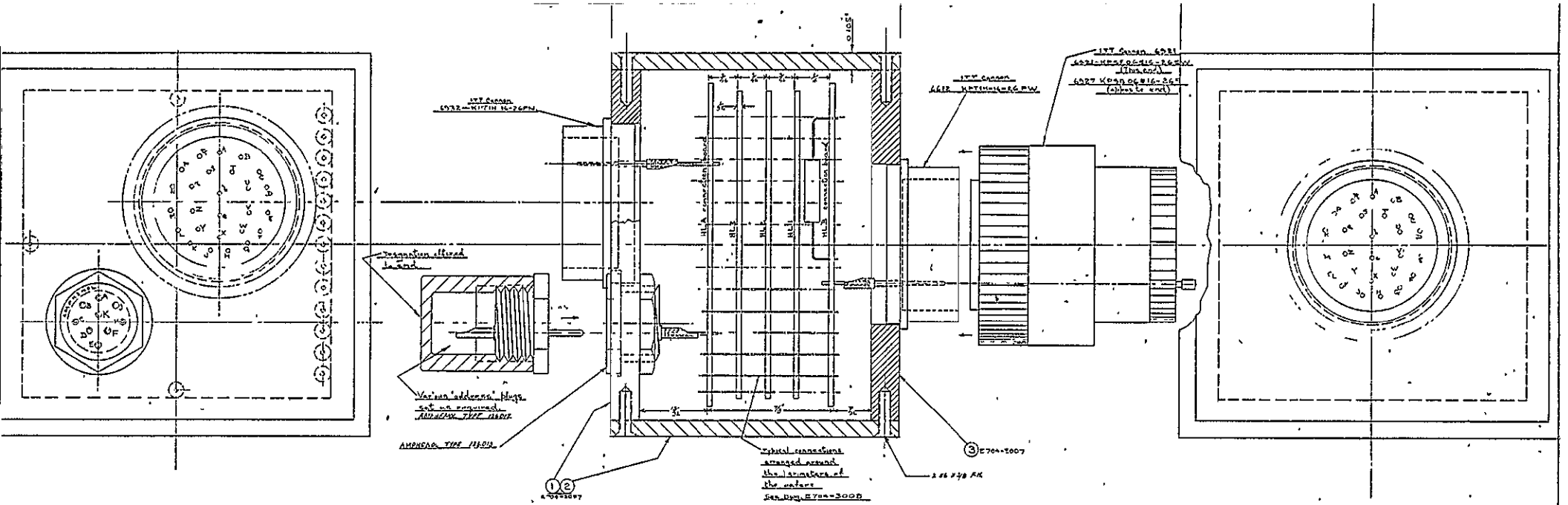
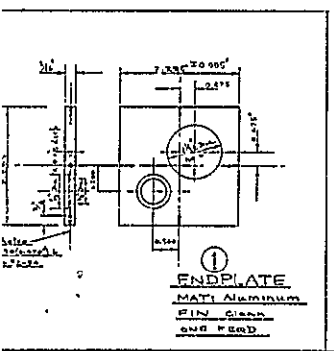
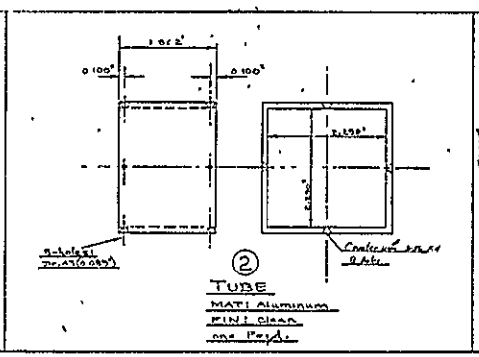

CANNON TYPE XPTH-16-26PW
SO19 B1 RESISTORS
SO19 B2 DIODES
HYBRID REF SUPPLY
DUAL LADDER NET
SO21A
SO18A
A/D COMP
SO22
SO56A
SO65
SO58A
SO26C
HIGH LEVEL MODULE INTERCONNECTION DIAGRAM
CONTROL DATA CORPORATION
GENERAL PRECISION EQUIPMENT CORPORATION

Figure 27



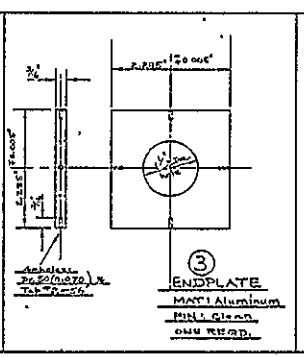




Figure 28

| Rev | Date | Description |
|---|---|---|
| 1 | 10-17-65 | 24" Cryostat 24" I.D. mag. field Default I-H's added |

ACCELERATOR DIV. ON CONTRACT E(49-18)-2000 FILED AT E.R.D.A. OAK RIDGE

High level data modules

ASSEMBLY & DETAILS

4/1

704

E704-3007

NOT REPRODUCIBLE

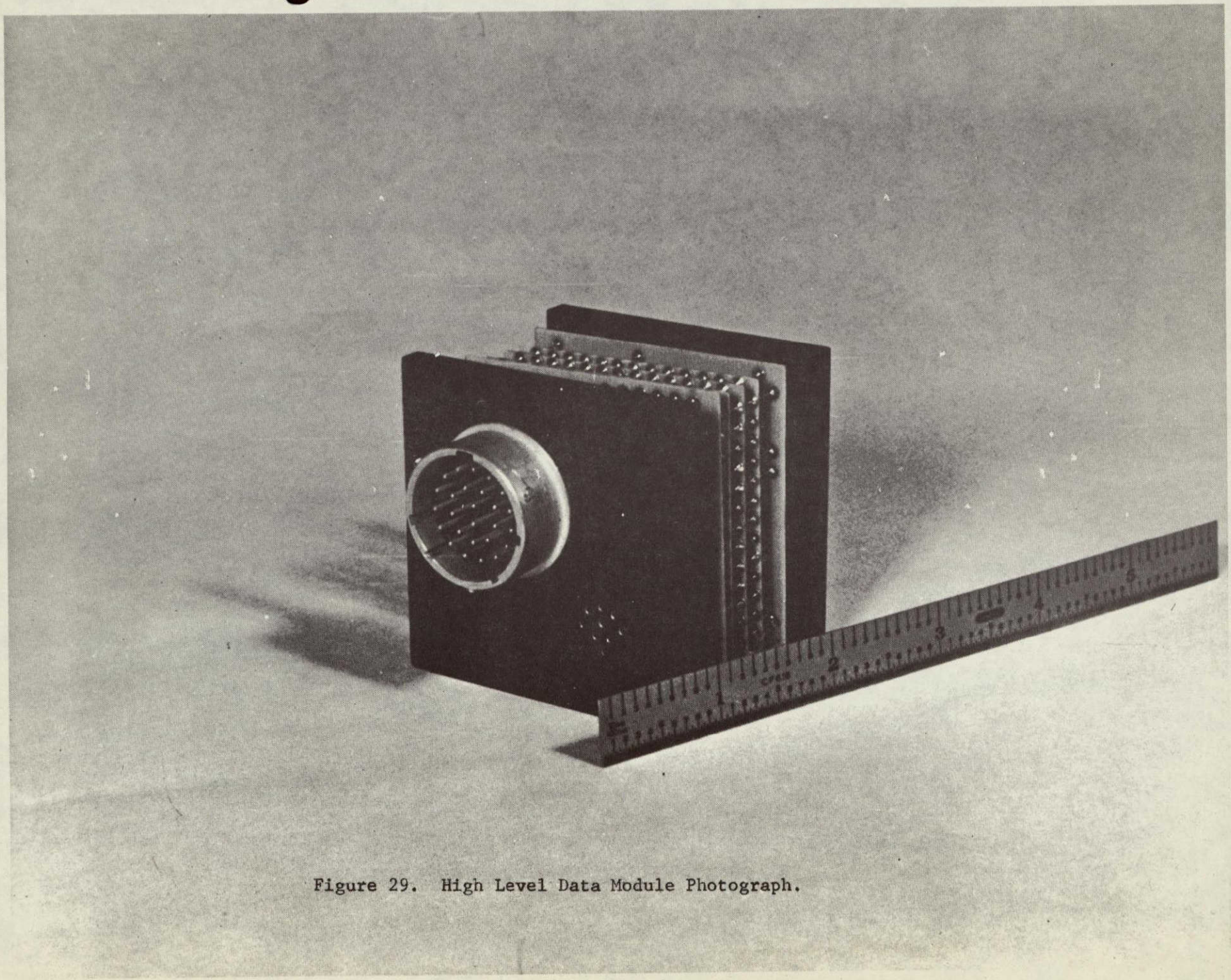


Figure 29. High Level Data Module Photograph.

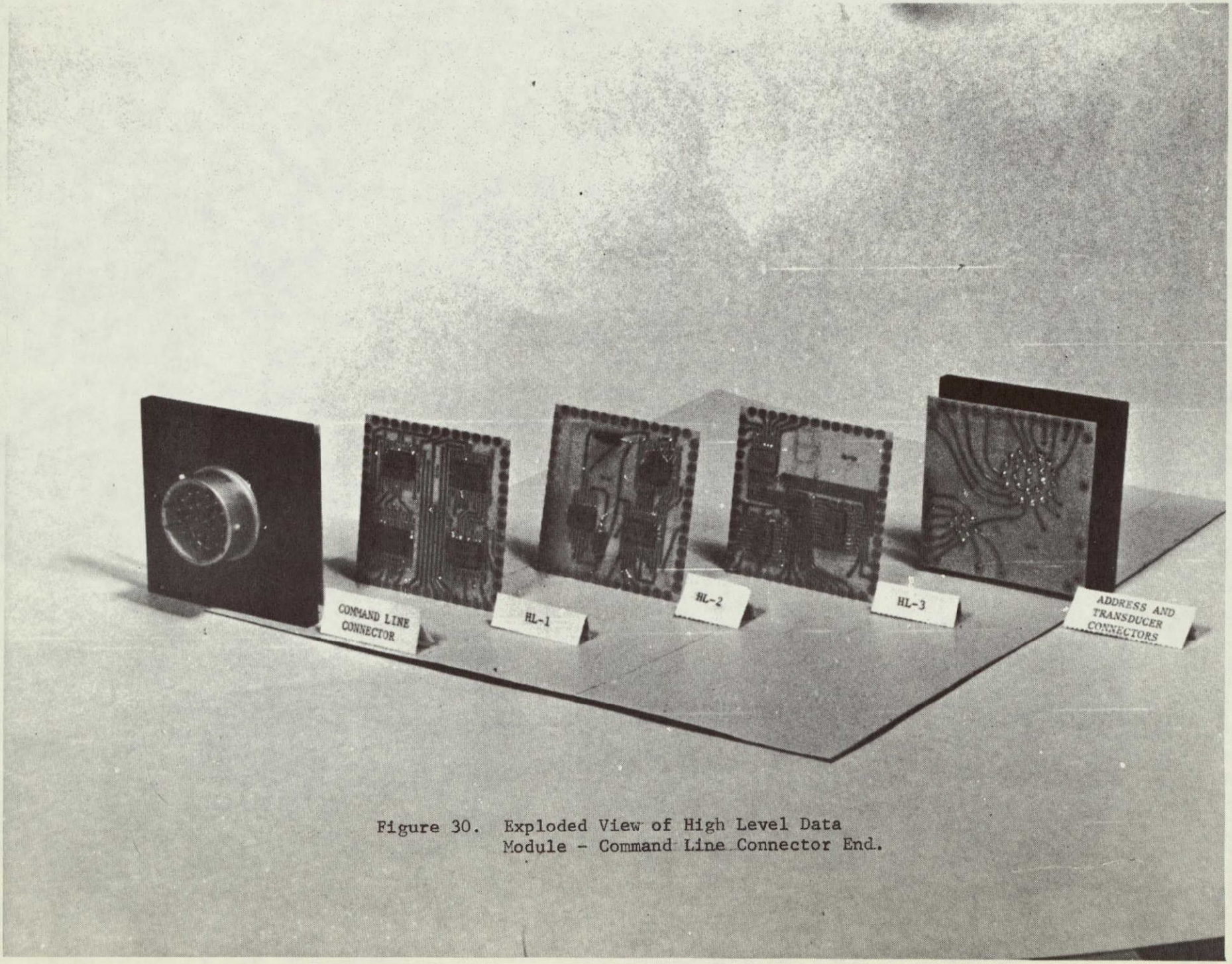



Figure 30. Exploded View of High Level Data Module - Command Line Connector End.

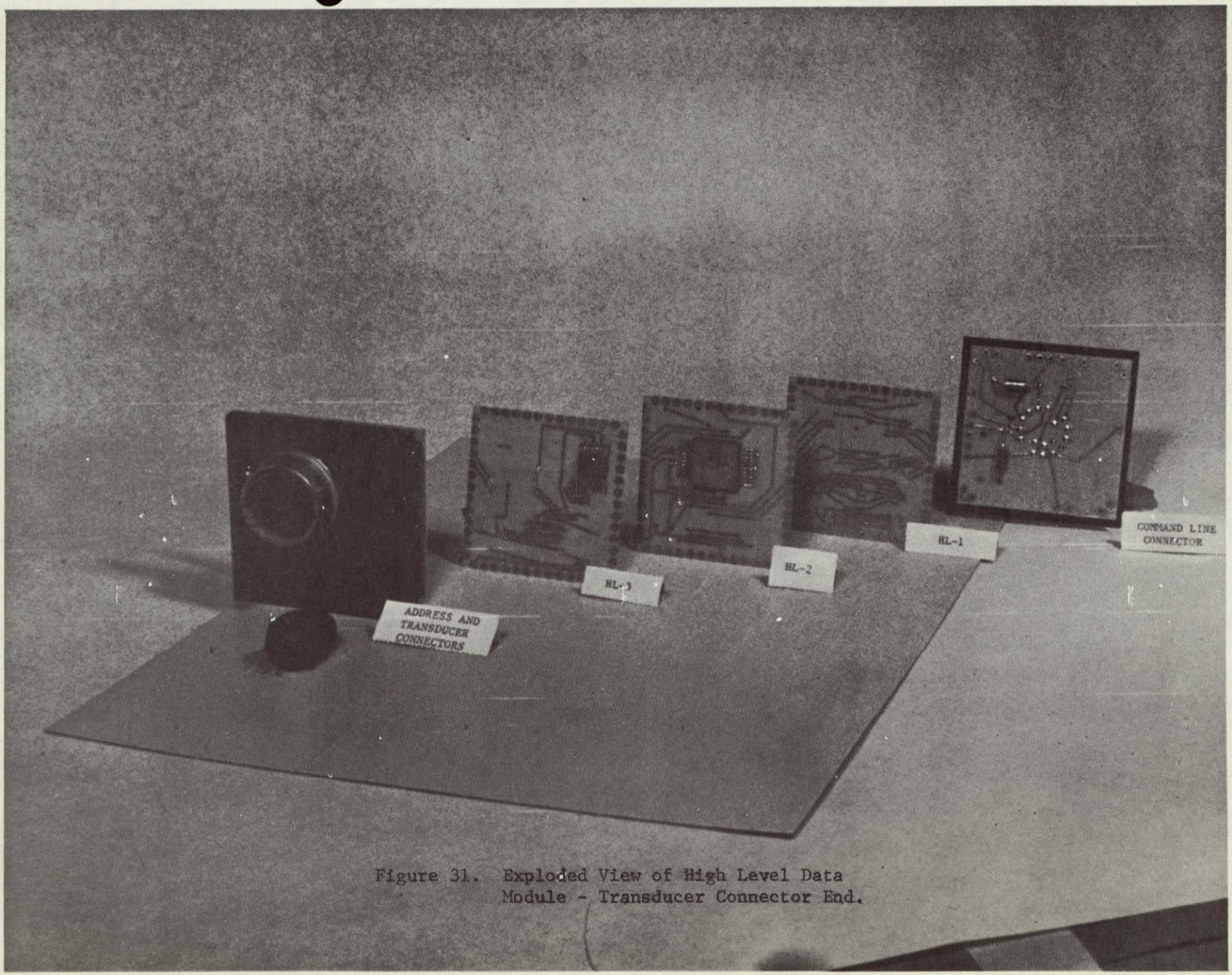



Figure 31. Exploded View of High Level Data Module - Transducer Connector End.

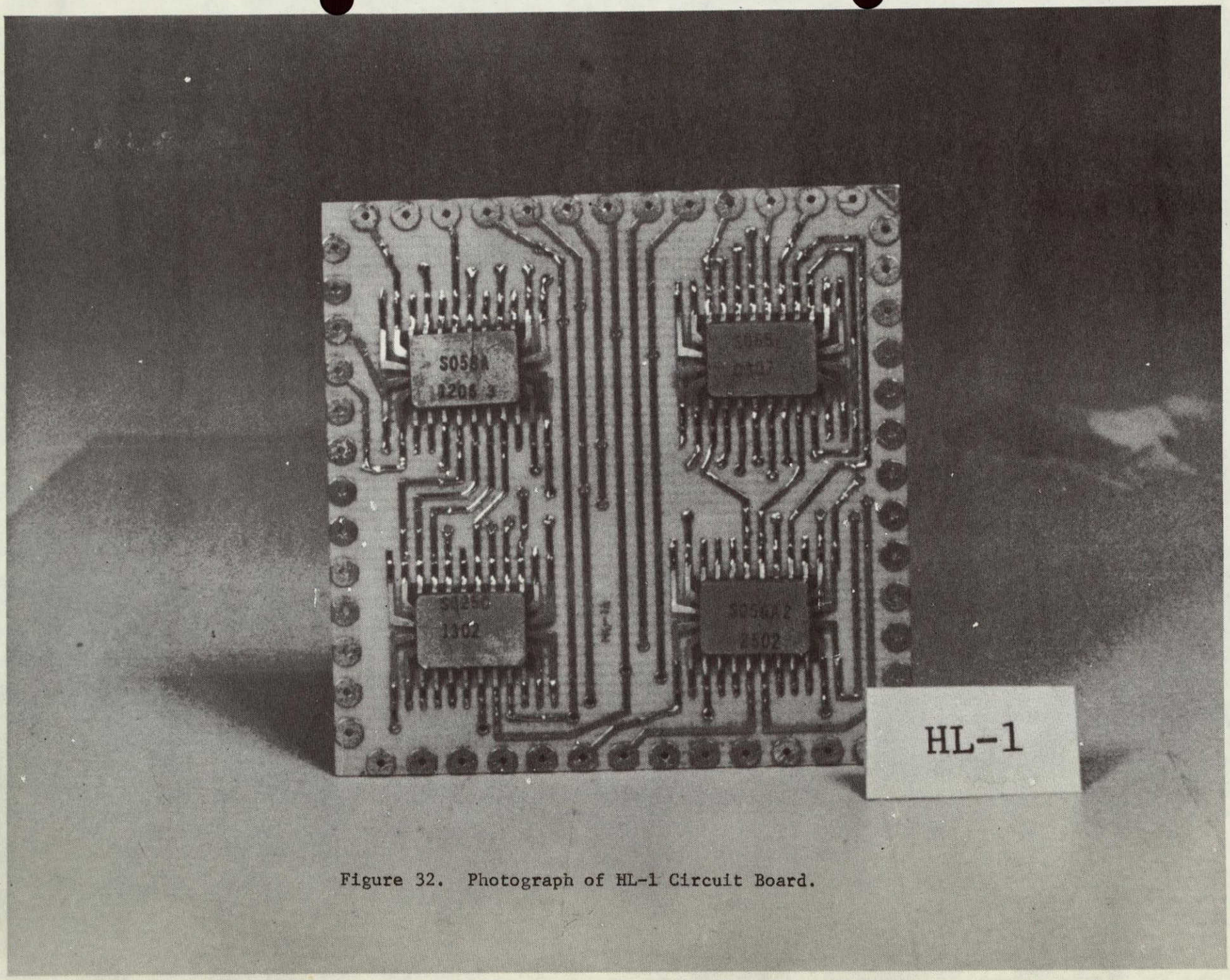



Figure 32. Photograph of HL-1 Circuit Board.

NOT REPRODUCIBLE

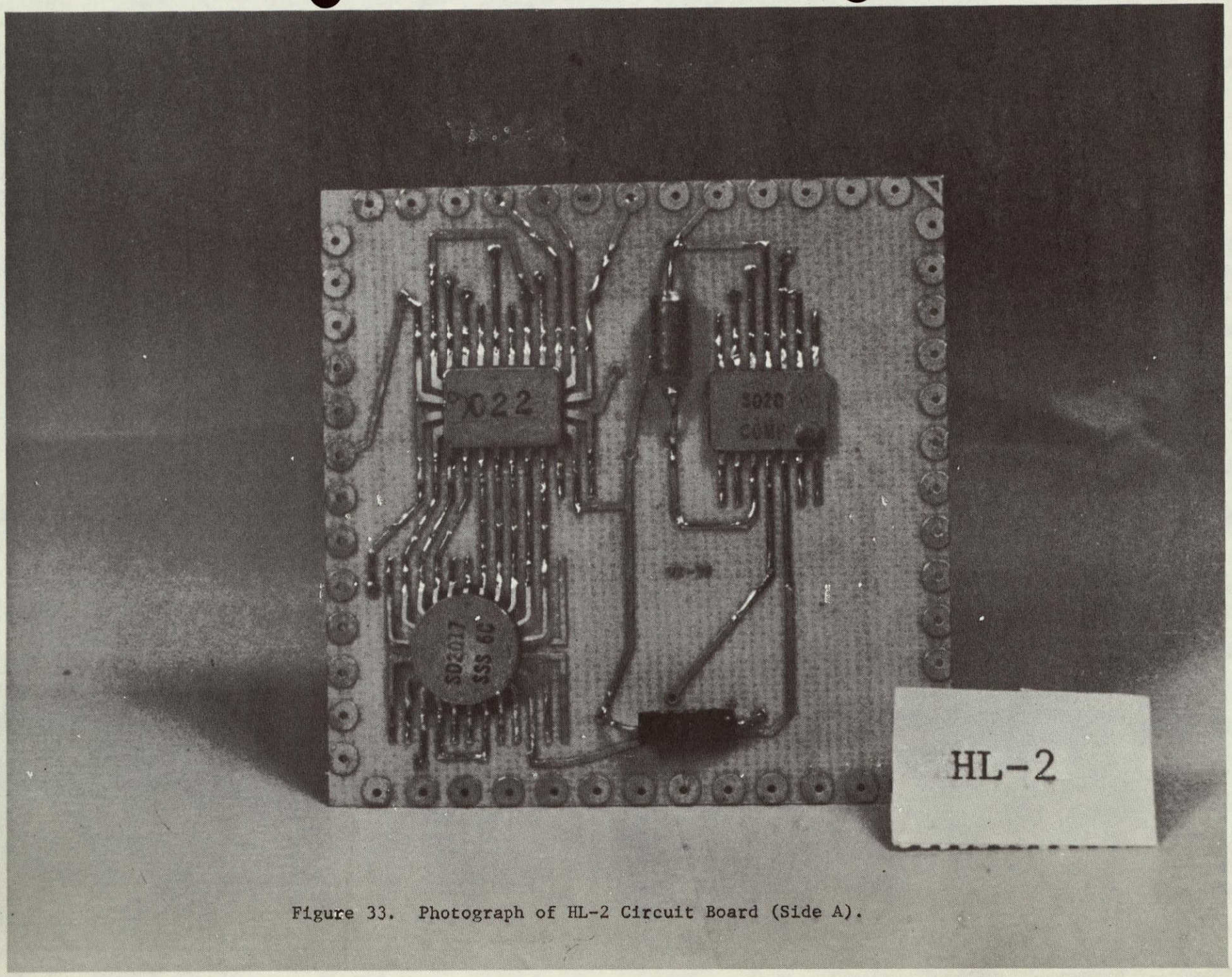



Figure 33. Photograph of HL-2 Circuit Board (Side A).

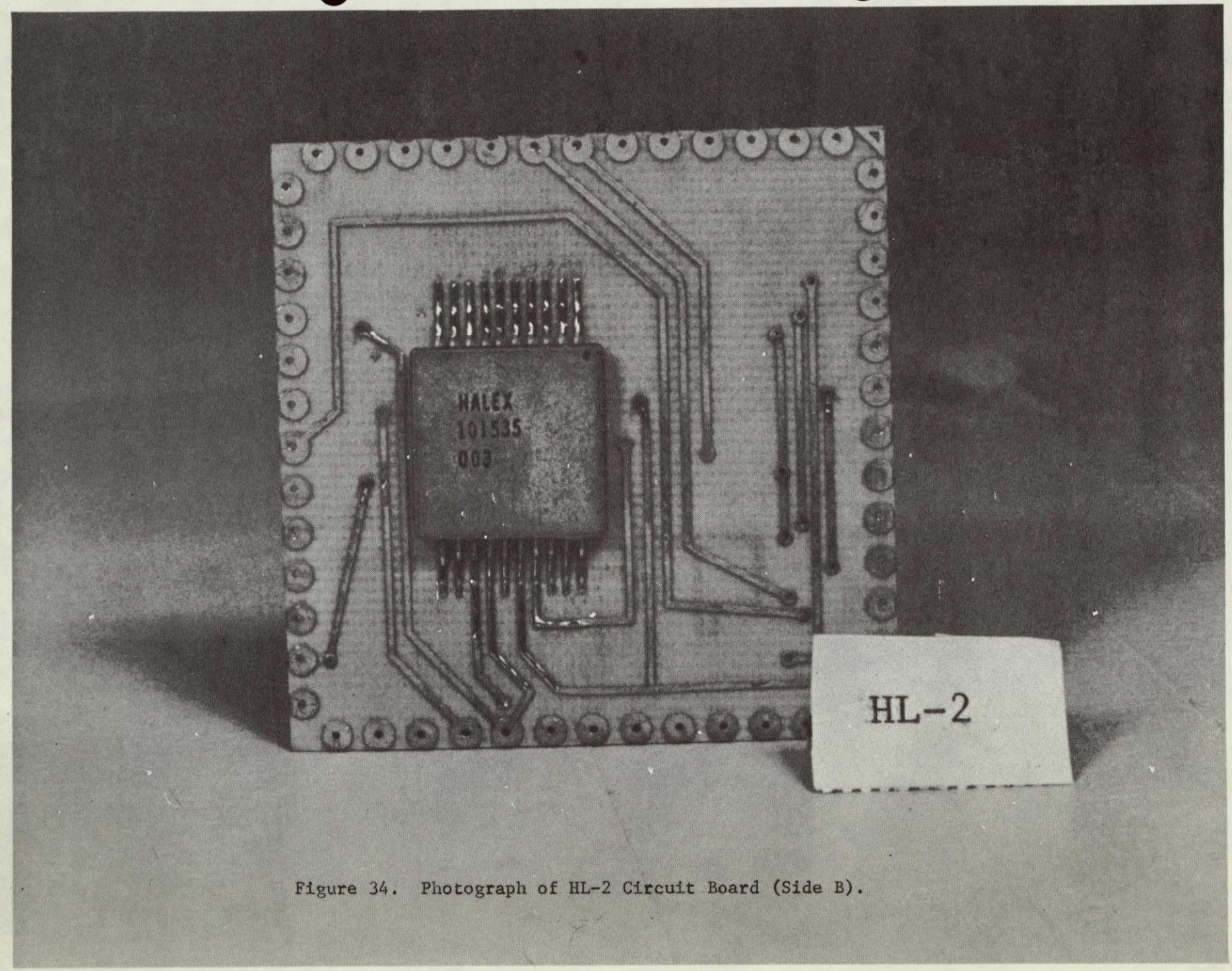



Figure 34. Photograph of HL-2 Circuit Board (Side B).

NOT REPRODUCIBLE

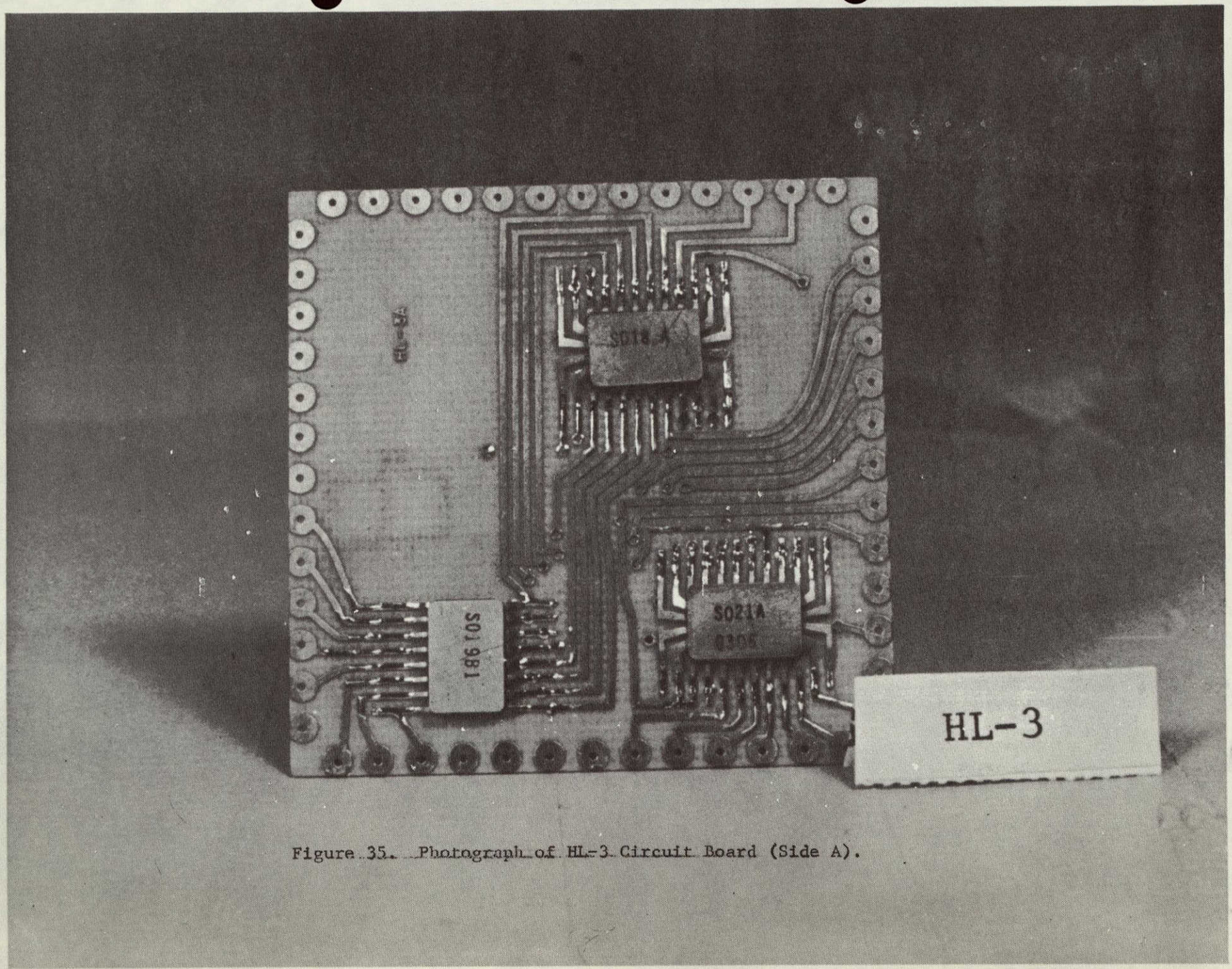
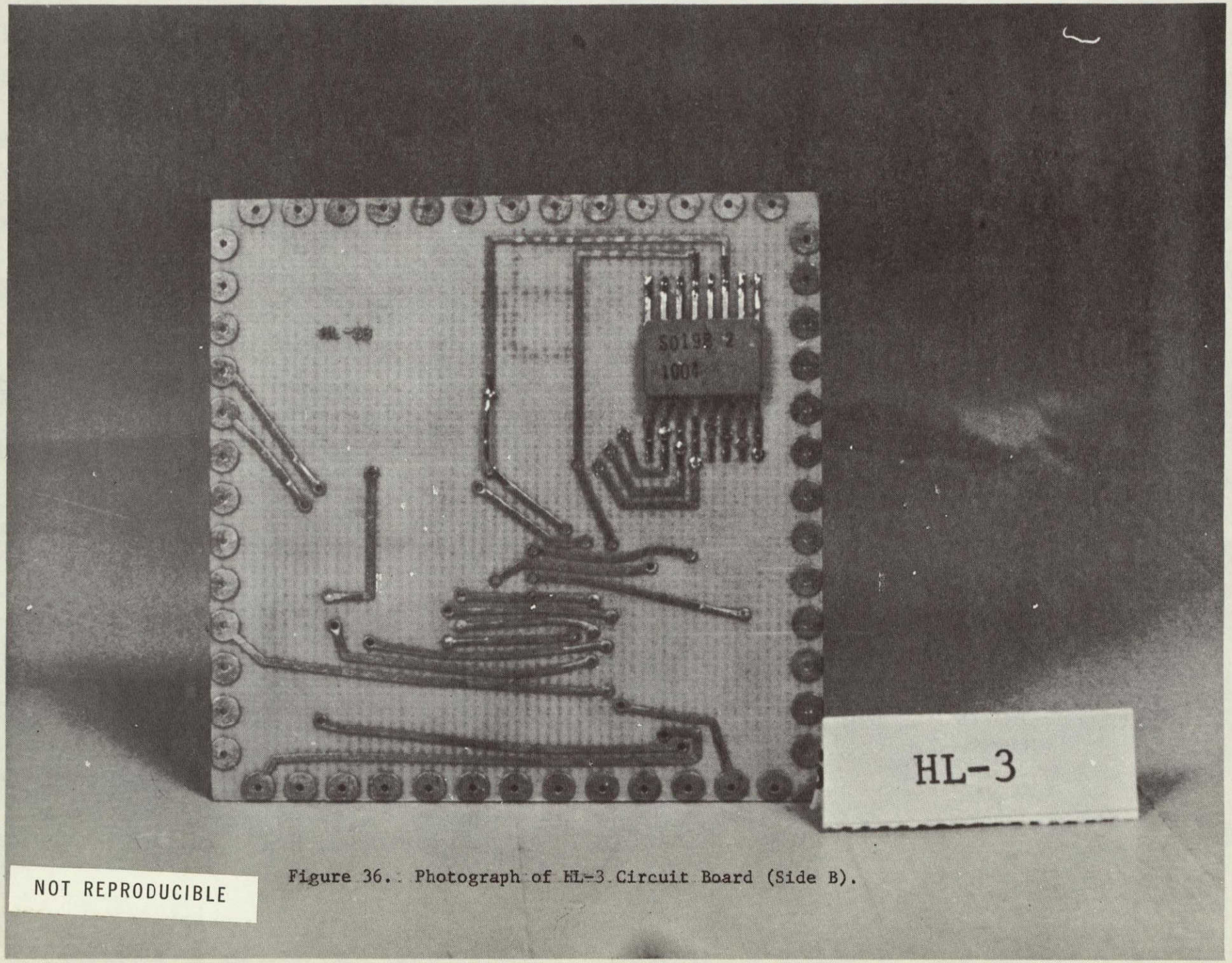



Figure 35. Photograph of HL-3 Circuit Board (Side A).

NOT REPRODUCIBLE




NOT REPRODUCIBLE

Figure 36. Photograph of HL-3 Circuit Board (Side B).

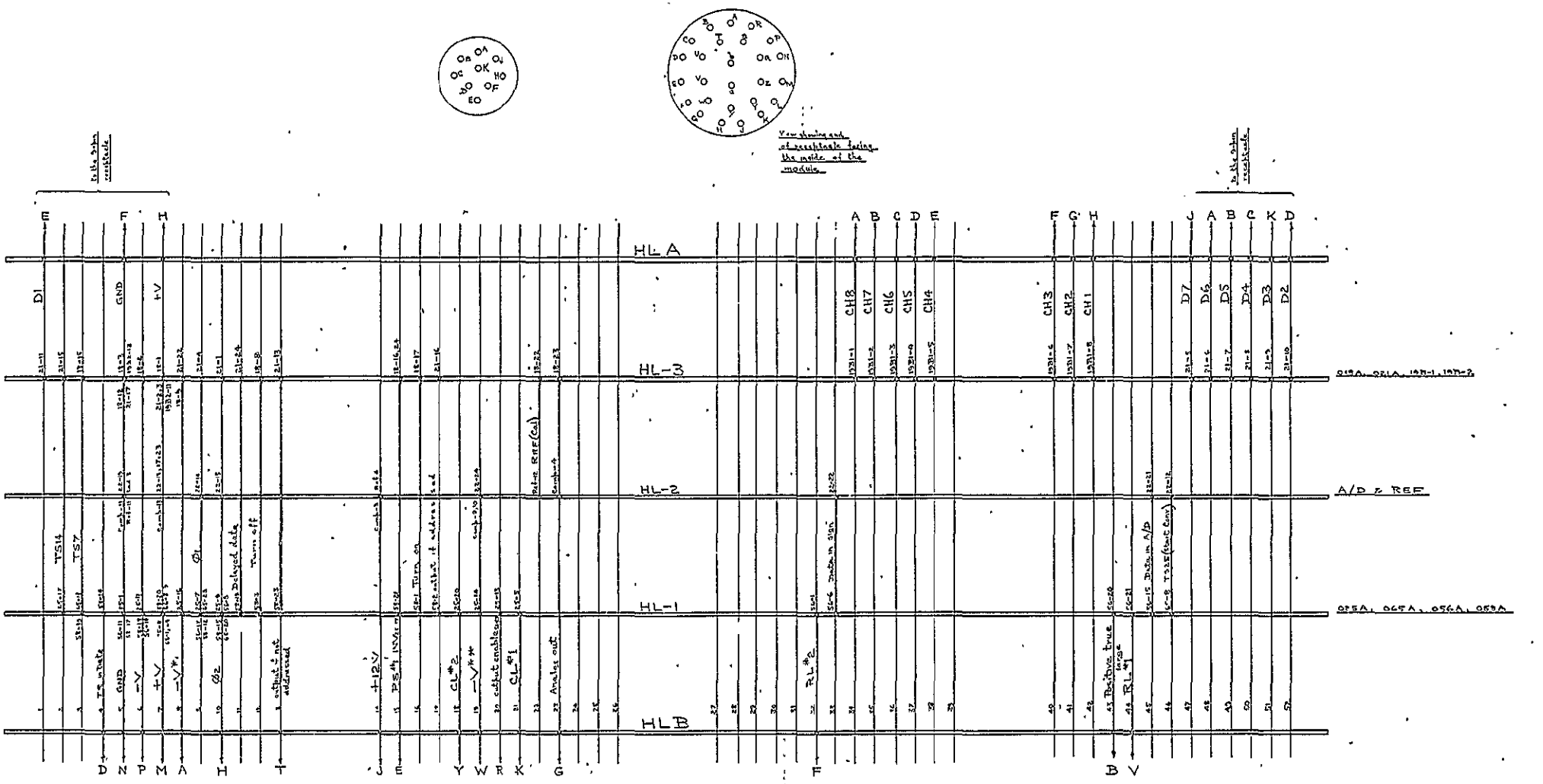



Figure 37

| | |
|---|---|
| WARPER INTERCONNECTIONS | 704 |
| E704-3009 | |

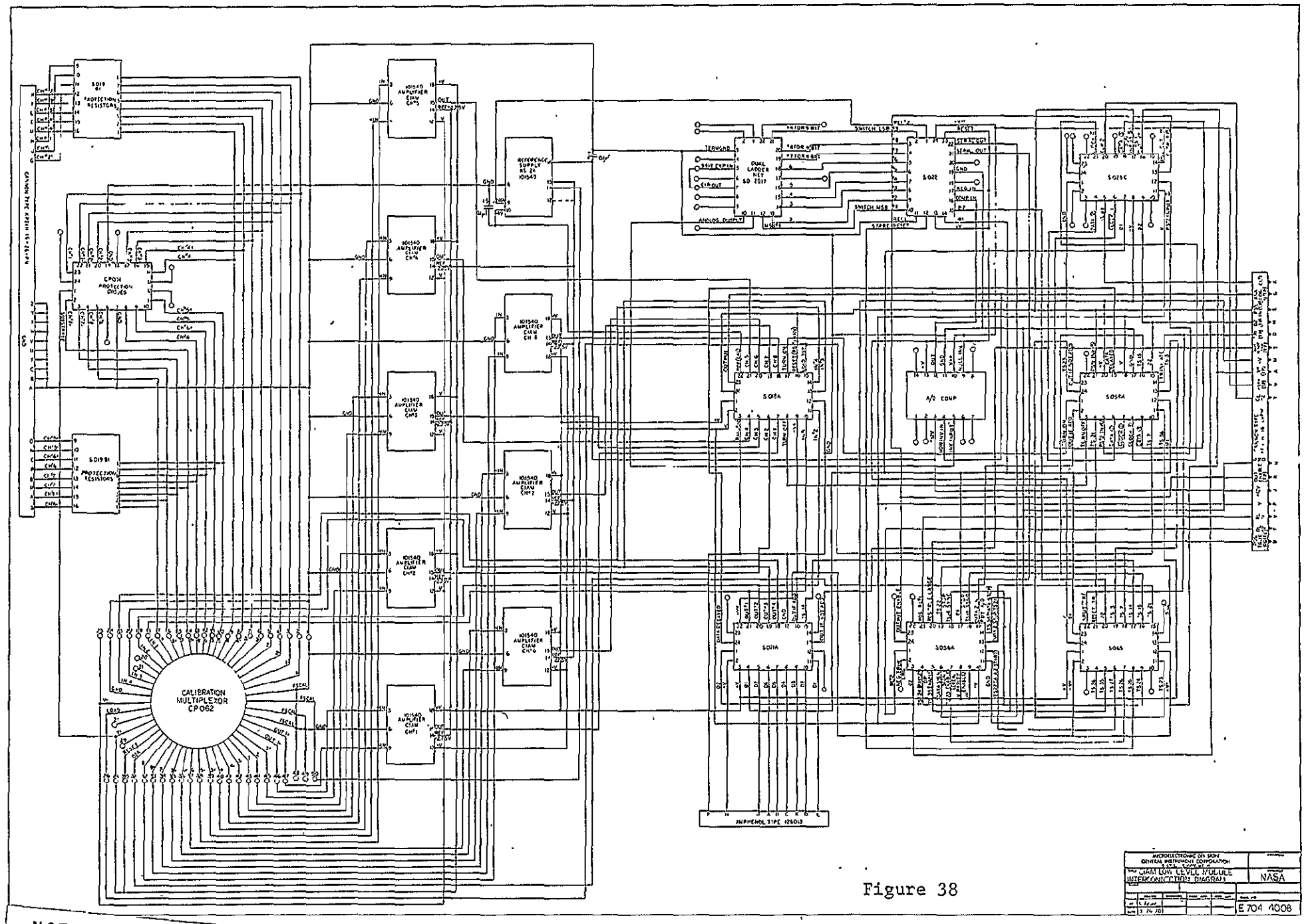
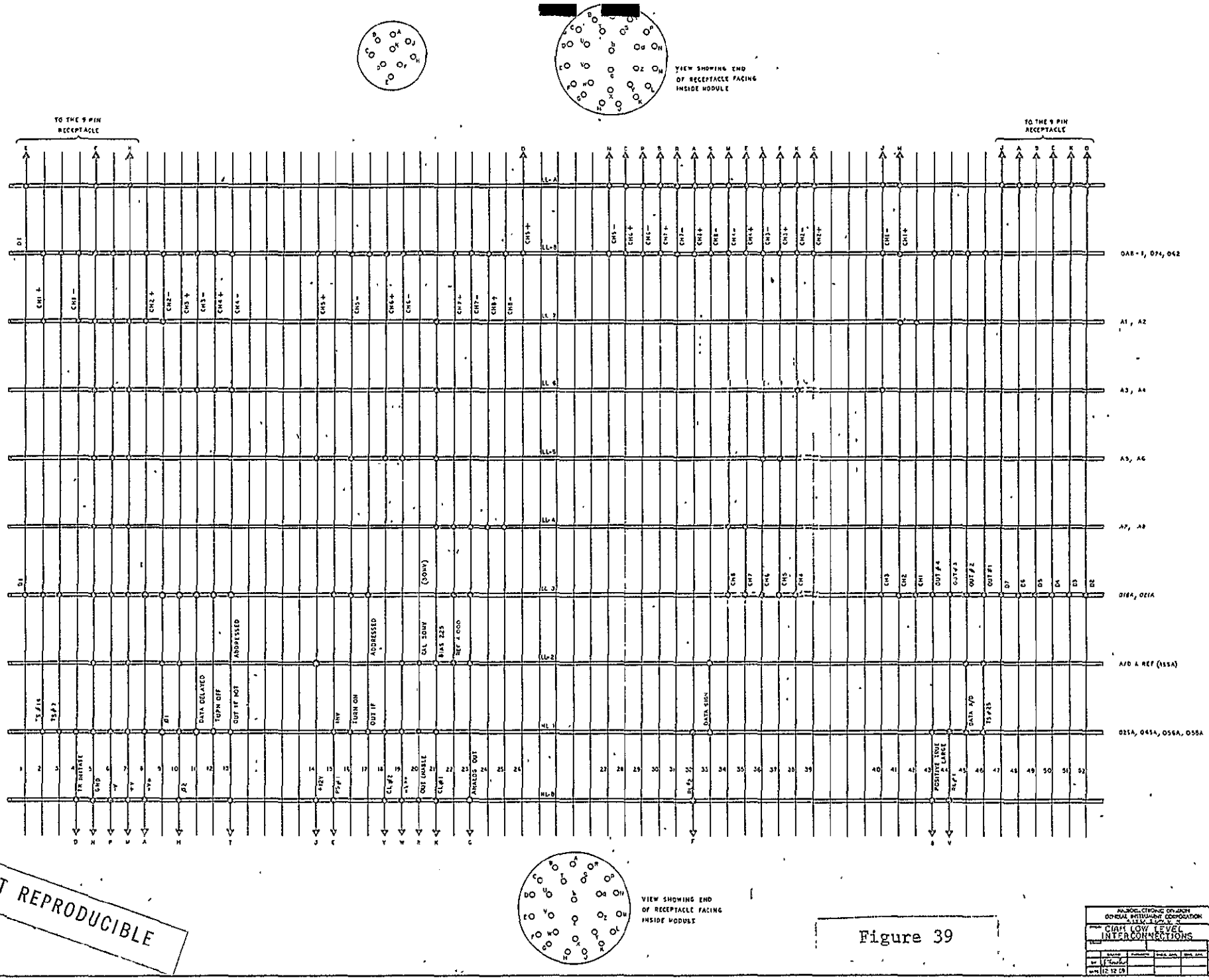



Figure 38

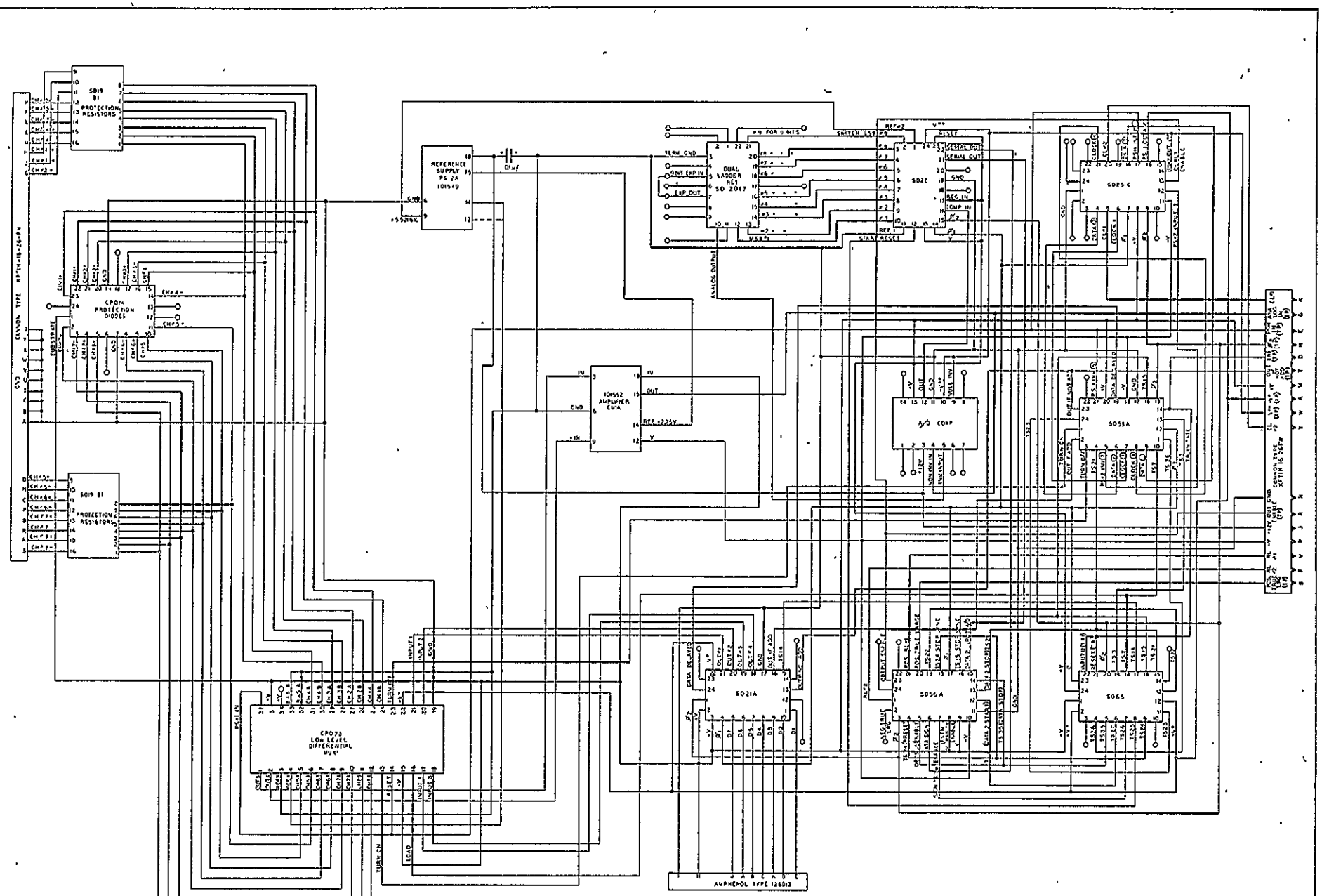
NOT REPRODUCIBLE




NOT REPRODUCIBLE

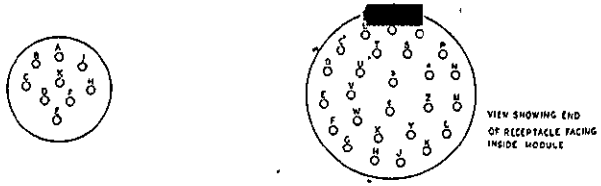
Figure 39

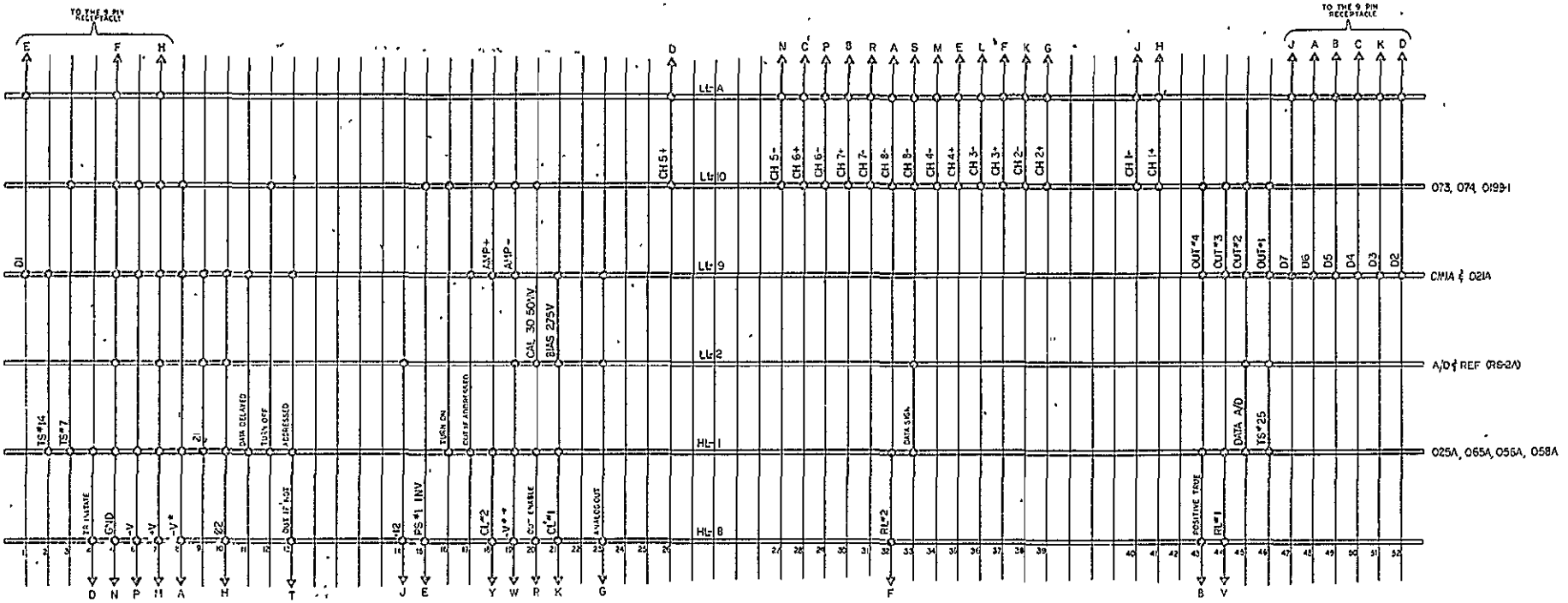
| | |
|---|---|
| RAYTHEON COMPANY, GENERAL INSTRUMENT CORPORATION, CIAM LOW LEVEL INTERCONNECTIONS | 704 |
| | E704-4005 |




NOT REPRODUCIBLE

Figure 40




NOT REPRODUCIBLE

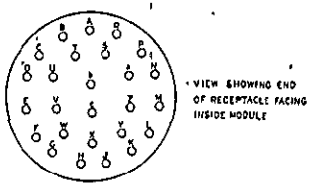
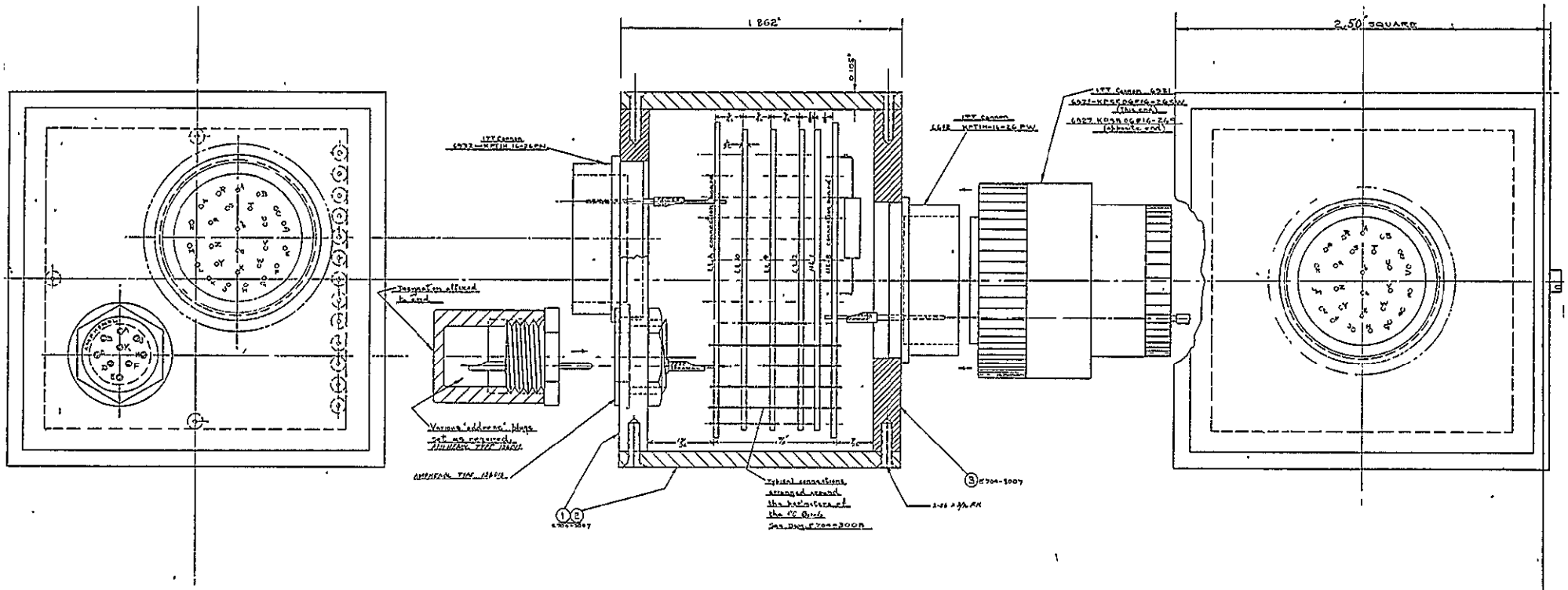
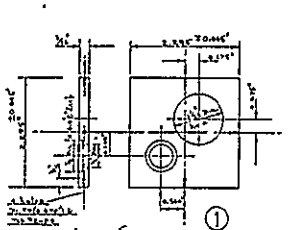



Figure 41

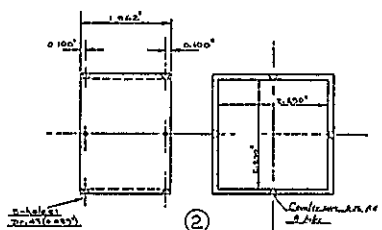
MICROELECTRONIC DIVISION
GENERAL INSTRUMENT CORPORATION
CMIA LOW LEVEL INTERCONNECTIONS
704
E 704-4007



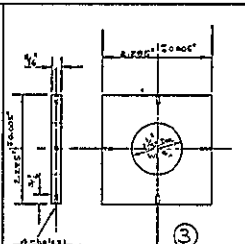

NOT REPRODUCIBLE



① ENDPLATE
MAT'l Aluminum
FIN' Clear
ONE REQD



② TUBE
MAT'l Aluminum
FIN. Clear
ONE Reqd.



③ ENDPLATE
MAT'l Aluminum
FIN' Clear
ONE REQD

Figure 42

| Rev | Date | Description | By |
|---|---|---|---|
| 2 | 3-23-70 | Changed from high level to CMIA Low Level Module | CL |
| 1 | 10-17-69 | 2.50" sq. was 2.25" sq. Dim. "B" was 1.810 | RS |

AEROJET-GENERAL CORPORATION
A SUBSIDIARY OF THE GENCORP
CMIA Low Level Module
ASSEMBLY DRAWING
1
704
E704-3012