NASA CR-102705

FINAL REPORT

DIGITAL DATA SAMPLING MODULES

PART II - SYSTEM CONTROLLER

CONTRACT NO. NAS 8-30003

Submitted to:

NASA
George C. Marshall
Space Flight Center
Huntsville, Alabama

Submitted by:

General Instrument Corporation
Microelectronic Division
Advanced Development Center
Salt Lake City, Utah 84115

PART II. SYSTEM CONTROLLER OPERATION

I. GENERAL DESCRIPTION

The System Controller (S.C.) receives command data words from the computer and generates a differential trilevel command signal to the modules (up to 128). See System Diagram (Figure 1). The addressed module responds with a differential trilevel response word which the S.C. converts to a parallel data word for the computer. The computer can be programmed to generate command words as desired depending on the data collection required. The Computer can be programmed to analyze the response data and output test results. The test program furnished is used to test the modules and verify that the system is working correctly. See Section VIII.

The System Controller can also operate "OFF LINE" (independent of the computer). The command word bits are selected by the front panel controls and the response word is displayed on the panel.

The System Controller block diagram is shown in Figure 2. Command data words are stored in command data Register A by a decoded instruction from the computer (load command word A) command data is transferred from Register A to Register B as the data from Register B is used. The command line multiplexer selects the data from command data register B or data from the manual entry switches and generates a serial data word. The serial data word is used by the command line generator to generate a differential tri-level signal. The sync generator provides the data "1", data "0", data "1" data "0" sync pattern for the command line.

The timing and control logic monitors the Front Panel Switches, decoded signals from the computer, and the timing registers and generates control

signals for the S.C. The timing and control logic also decides from its inputs whether another command word should be generated or not. If another command word is required, then a logic "1" is loaded into the command timing register.

The Command Timing Register generates "1 bit time" long signals for use throughout the SC. Note that command word timing is divided into 36 bit times. See System Timing Diagram Figure 3.

Each of the modules monitor the command word and the addressed module responses with small amplitude (.5V pp) trilevel response word. The S.C. receives the response signal through a differential amplifier. The signal is then split into clock and data signals. The sync detector logic recognizes the data "1", data "0", data "1", data "0" pattern uninterrupted by a clock signal.

The sync is used to start the Response clock counter and enable the response clock generator. The response clock causes the shift register to load the response data.

If the response clock counter counts 12 clocks, no error is recorded; otherwise, a response clock error is stored in the Status Storage register. No Sync, Command Data Bad, Response Parity Fail, Multiple Response are the remainder of the Status bits which are stored in the Status Storage register.

The data is transferred from the Serial to Parallel Shift Register to Register B as soon as B is available. The transfer from B to A is also made on an availability basis.

The Data/Status selector determines whether Response data or the status bits are loaded into Response Data Register B.

The Special Computer Interface Logic decodes signals from the computer

and causes command data to be loaded from the computer, and Response data to be inputed to the Computer.

II. SYSTEM CONTROLLER PACKAGING

The System Controller is contained in a Digital Equipment Company Module Drawer (H925). See Figures 4 and 5. The Four System power supplies are mounted in the Drawer. Six DEC type card connectors provide 24 double card connections. Single and double size circuit cards are used to implement the logic. Inputs from the computer and signals from the Front panel terminate at the card connector with a special printed circuit card connected to flat cable. A small maintenance panel for adjustment of the Master Clock is included inside the chasis.

III. FRONT PANEL

The System Controller Front Panel controls the operation of the Data Acquisition System. See Figure 4 and Figure 6. The switches from left to right on the panel will not be discussed. The twelve switches labeled COMMAND WORD control the command word when the SC is in OFF LINE operation. The first seven bits select the module address (0-127); the next four select the MUX address or control function. All switches select a "1" when in the "up" position. When the PARITY switch is in the "up" or ODD position, the parity bit is made a "1" or "0" such that the total number of bits at logic "1" is odd. This is the normal position. If the PARITY switch is placed in the down position, even command word parity is generated. The address module, in this case, should respond with a

command data bad signal. See Figure 3.

The System Controller operation switch selects whether the SC operates with the computer or from the front panel controls. When in ON-LINE operation, the System Controller uses output data from the computer to generate command words, and inputs responses to the computer. The OFF-LINE operation uses the control switches for command words. The ONL* and OFL* signals are -V or open from the switch; however, a pull resistor to +V is on the receiving PC card.

The MODE switch selects whether the command word is generated in the INTERLEAVE mode or NORMAL. See Figure 3 for definition of INTERLEAVE or NORMAL.

The MAN. (Manual) control switch in the ON position stops the generation of any command words. The pressing of the CMND INIT. (Command initiate) switch causes one and only one command word to be generated. The MAN. switch in the "up" position allows command word to be generated automatically.

The A/D DATA indicator lamps display the last received response word (What's in Response Data Register B). The RESPONSE STATUS indicators if "lit" indicates a failure. Refer to Figure 18 for the exact meaning of the status bits.

The command word indicators indicate the command word in Register B. (The command data that will be used next.)

IV. POWER SUPPLIES

The power key switch turned to the off position turns all power off including power to the computer, System Controller and modules. The second position of the switch turns power on to the computer and the cabinet fan. See Figure 7. The third position turns power to the whole

system. The four SC power supplies should be maintained at the following voltages:

Power Supply No.	Voltage Setting
(1)	+6.5 ± .25VDC
(2)	-8.5 ± .25VDC
(3)	+12V ± .5VDC
(4)	-13V ± .5VDC

Each power supply has a crowbar protection device attached to it, (Sorenson VP1) which set to clamp the power supply if it exceeds .5 volts above its nominal setting. If the clamping to (0V) is caused by a transient, turning the System power on and off is all that is necessary.

V. PRINTED CIRCUIT TYPES AND CARD LAYOUT

Figure 8 shows the top view (wiring side) of the card connector chasis. The maintenance panel has the clock controls on it. The switch on the left when in the INT position allows the internal oscillator to determine the Master Clock frequency. The HI-LOW switch selects the frequency range. The control on the top allows for continuously varying the frequency from approximately 10KC - 750 KC. Puting the control to EXT allows for an external generator to be plugged into the rear of the chasis and set the command word clock frequency.

The System Controller is packaged on single and double size circuit cards. The logic implemented on each card performs a unique function. The following is a list of the PC cards used in the System Controller.

NAME	GI NO.	Number Required per System
Response Receiver	366A	1
Command Line Gen.	367A	1
Command Line Multiplexer	368A	1
Command Data Register	369A	1
Computer Interface Decode	370	1
Timing and Control Logic	371A	1
Response Data Register A	372	1
Response Data Register B	373A	1
Lamp Driver	374	4
Response Status	375A	1
Power Relay	376	1
Computer Interface Logic	377A	1

The location of each PC card is shown in Figure 8. Three panel cable connectors and 4 computer cable connector locations are also shown.

VI. LOGIC ELEMENTS

The System Controller logic is implemented with the nine devices shown in Figure 9. Each is made using complementary MOS technology with the exception of S016 which is P-channel MOS. In all cases, the -V input is a logic "1" and +V is a logic "0". With the exception of computer input/outputs all logic levels within the SC is as just described.

1. Logic Gates

The HEX Inverter, (S081) Quad Two Input NOR (S080) and Dual Four Input NOR (S079) are negative true logic gates.

2. RST FLIP/FLOP

The S071-1 flip-flop provides an and-or gating to the set and reset inputs of the flip-flop. The S071-2 provides two flip-flops in a 16 pin dual-in line package. The S071-3 and S071-4 provide for 3 bits of storage. Each bit is loaded when its clock goes negative.

3. Shift Register

S016 is a 9 bit serial to parallel shift register that can be reset to logic "0". The Reset input going negative causes each of the nine bits to be set to logic "0" with ϕ_1. The data at the input during ϕ_1 time is transferred from the data input to bit 1 during ϕ_2 time and so forth down the register.

4. Oscillator and Two Phase Clock Driver

S030A includes an internal oscillator. The duration of ϕ_1 is determined by the value of R1 and C while the duration of ϕ_2 (negative) is determined by R_2 and C. Pins 8-9 and 5 can be tied together with only one R and C if ϕ_1 and ϕ_2 need not be independently adjusted. When the internal clock enable is negative, the internal oscillator drives the two phase clock driver; If positive ϕ_1 and ϕ_2 follow the External Clock Source. The internal clock can be stopped or started at anytime by the STOP clock or START clock controls going negative.

VII. DETAILED FUNCTIONAL DESCRIPTION

1. System Controller Wiring Diagram

Figure 10 shows all the wiring between printed circuit cards, the front panel, the computer to the left, and the Data/Power

Cable connector to the modules to the right. Each card performs a certain logic function and a discussion of each follows.

2. Response Line Receiver - GI 366

The circuit shown in Figure 11 shows the System Controller Response receiver, which receives a low power differential trilevel signal and generates data and clock information. The differential receiver comprising transistors 1-6 reduces the common mode noise by at least 30db and amplifies a trilevel signal approximately +6db. The amplified trilevel signal drives three Fairchild 710 comparators. Comparator A reference is adjusted such that the output swings negative as the input goes above the adjusted positive voltage level. The output of the comparator A then becomes data. Transistors 7 and 8 are used as level changers to generate $\overline{\text{Data}}$ (negative true) at the +6, -8 volt levels used in the System Controller. Figure 12 shows the response line inputs and the $\overline{\text{Data}}$ and $\overline{\text{Clock}}$ output waveforms.

The Reference of comparator B is adjusted to a negative voltage such that a negative signal below the reference causes the output to go negative. Figure 13 shows the response signal into the comparators along with the Receiver output signals. The Data and Clock reference voltage is adjusted so that the nominal amplitude response signal has greatest noise immunity.

If a module malfunctions and decodes the address wrong, there can be more than one module responding at a time. The right hand part of Figure 13 shows a response signal with two modules responding. The outputs from each module add algebraically. The slight stairstep effect is caused by the difference in distance from the System

Controller. The Multiple response reference is set above the largest single-response signal and below the smallest double response signal. The response signal is attenuated by about 2db by 300 feet of cable so there is about 2db difference in the response signals received.

The multiple response signal is passed on to the Computer by the System Controller, where the Computer, under program control, can take appropriate action.

3. Command Line Generator - GI 367A

The Command Line Generator receives serial data, clocking and control signals and generates the differential trilevel command signal, see Figure 14. The Output Circuit (S056A2) is also used in each module. Refer to Part I, Section IV-7 for S056A2 operation and schematic. The START SYNC (TR0) and STIP SYNC (TR3) cause the data "1", data "0", data "1" data "0" sync pattern to be generated. The signals at S056A2 pin 20 (LARGE POSITIVE TRUE signal) and pin 2 (LARGE NEGATIVE TRUE signal) are similar to the response signals from the modules. ϕ_1 and ϕ_2 control the generation of clock and data outputs. The DATA #2 START (TR3) causes the serial data stream to be gated onto the Data bus. The DATA #2 STOP (TR14) prevents the serial data signal from getting to the Data bus. As the serial data stream is passing through the S056A2 circuit, the number of data "1" bits is counted. Either ODD PARITY ENABLE or EVEN PARITY ENABLE is true during TR14 time. A data bit either logic "1" or logic "0" is generated by S056A2 at Parity time (TR14). If the number of data bits generated since the start of the command word is even and the ODD PARITY ENABLE is true, the parity bit output will be a logic "1". Likewise, an odd number of data bits and ODD PARITY ENABLE cause

a parity bit of logic "0"; for the EVEN PARITY ENABLE signal the opposite is true. The System Controller normally generates odd parity. The Even Parity is used only to check command word Parity detection of each module. DATA #1 ENABLE (TR15) causes +V (logic "0") to be gated onto the bus. The two signal outputs of the S056A2 are clamped to ground by the two MOS devices 1 and 2 whenever OUTPUT ENABLE is false (+V).

The positive and negative true command line signals are amplified by identical circuits. Only the positive true amplifier will be discussed. The S056A2 has a limited voltage and current driving capability the 82Ω balanced line must be driven to the +V, -V levels. Devices 19 and 20 split the trilevel signal into a clock and data components. The emitter of device 20 should follow the data part of the signal, the emitter of 19 the clock part. Devices 3 and 5 invert the signal twice and shorten the rise and fall time of the data signal. Devices 4 and 6 perform the same function for the clock signal.

The signals at the collectors of device 5 and 6 swing from +12V to -13V. Devices 7 and 8 form a push pull emitter follower type driver. When data is true, device 7 is on. The voltage at pin A is the result of a voltage divider between 51Ω and the 82Ω line $\frac{82}{51 + 82}$ (12V) ≅ 7.4 volts. The on resistance of device 7 lowers the voltage slightly. When data is logic "0" both device 7 and 8 are off. The 82Ω terminating resistor pulls pin A to ground. When clock is true, device 8 is on and the line is pulled negative. The zener from base to emitter prevents the emitter base breakdown voltage from being exceeded. The 5Ω and 2.2μf capacitor isolate the current spiking from the power

supply. During the switching time both devices 7 and 8 can be on causing high current surges.

4. Command Line Multiplexer - GI 368A

The Command Line Multiplexer converts the paralleled data from command Data Register A to a serial data stream, see Figure 15. If the System Controller is in the off line mode, the command word set by the front panel switches is used for the parallel word. Two 9-bit shift registers S016 R, P generate the timing signals $\overline{TR3}$ through $\overline{TR13}$ for the multiplexer. The logic for the DATA INPUT signal is:

$$\text{DATA INPUT} = \overline{(TR3\cdot\overline{C11}+TR4\cdot\overline{C10}+\ \ldots\ +TR13\cdot\overline{C01})ONL} + (TR3\cdot\overline{S011}+TR4\cdot\overline{S010}+\ \ldots\ +TR13\cdot\overline{S01})$$

Note that up until the final inverter output, the signal is the timing signal times the data bit "barred". The final inversion causes the each data bit to appear at the DATA INPUT signal point at the proper time to generate the command word.

5. Command Data Register - GI 369A

The command data register stores the command word information from the computer, see Figure 16. The 12 bit information is translated from the 0, 5V levels to a -7, +7 levels by the input level changer (ILC) circuit as shown below:

Input		Output
0V (Logic "0")	→	-7V (Logic "1")
5V (Logic "1")	→	+7V (Logic "0")

Thus, the ILC is shown as an inverter since it logically inverts the signal. The Command Data Register A is built from four S071-4

(3 bit inverting latches). The twelve data bits from the Data Output Buss (BAC) are loaded into Register A whenever the LOAD COMMAND DATA REGISTER A signal is negative (Logic "1"). Register B uses the non-inverting (S071-3) 3 bit register. The data is transferred from register A to register B by the LOAD COMMAND DATA REGISTER B signal. The data in register B is used to generate command word.

6. Computer Interface Decode - GI 370

The Computer Interface Decode circuit decodes the "BMB" lines and generates the "616", "615", "$\overline{614}$" signals. These signals are used by the Computer Interface Logic (GI 377A) for decoding computer instructions. Refer to Figure 17. Note that each of the seven System Controller instructions begin with 614, 615, or 616. See Figure 18. The input level changer converts the +5V, 0V logic to -V, +V, logic of the System Controller. The logic translation is thus:

Input	Output
+5V (Logic "1")	+V (Logic "0")
0V (Logic "0")	-V (Logic "1")

7. Timing and Control Logic - GI 371A

The timing and control logic provides all the control signals for generation of the Command word, see Figure 19. The frequency of master two phase clock generator is controlled by the R-C network shown. By adjusting the potentiometer and selecting the low and high position, the clock frequency can be varied from ~10KC to 750KC. Also, an external source can be used as the frequency source. The input connector is on the rear of the cabinet and the selection switch on the card chassis. The two phase clock is amplified by the Hex inverter for distribution to the rest of the system Controller.

The command Timing Register is composed of five S016, 9 Bit Shift registers. A logic "1" is inserted into the timing register each time a new command word is to be generated by the start Ring counter signal. The "1" bit is shifted down the register generating the successive "TRXX" bit times. The logic equation for the generation of the start ring counter is:

START RING COUNTER = (OFL+ONL·CIR)(NORM·TR35+INLV·TR17)
+ ASYCHRONOUS START

where OFL - off line
ONL - on line
NORM - normal mode
INLV - interleave mode
TRXX - timing register count

Whenever the logic detects the fact that no command word is being generated (no "1" in the timing register) and a new command word should be generated, the ASYCHRONOUS START signal is generated. The ASYCHRONOUS START flip-flop is set by the following logic. Set ASYCHRONOUS START = COMMAND INITIATE + CDOF (OFL + ONL·CIR)

where

CDOF - Command Data Off

CIR - Computer Interface Ready

The Command Data Off flip-flop is set by either a power up signal (R-C network) or $\overline{TRO} \cdot \overline{TR18} \cdot TR36 \cdot \phi_2$. This indicates that timing

register is at TR36 (command word has just been finished) and there is not a new command started (TR0) or one in progress (TR18).

The Output Enable signal prevents the command word from getting onto the line and clamps both positive and negative signals to ground. This occurs whenever the command word is no longer being generated or when words are being generated in the INTERLEAVE MODE. Note that in the NORMAL mode, the command word (both positive and negative true) must be clamped to ground between during TR19 and TR20 time. Therefore, the logic for setting the OUTPUT ENABLE flip-flop is:

$$\text{SET OUTPUT ENABLE} = \text{START RING COUNTER} + \overline{\text{INLV}} \cdot \phi_1 \cdot \text{TR20}$$

$$\text{RESET OUTPUT ENABLE} = \text{END COM. DATA} + \overline{\overline{\text{INLV}}} \cdot \phi_1 \cdot \text{TR18}$$

8. Response Data Register A - GI 372

The Response Data Register A stores the Response Data word until the computer can accept the response word, see Figure 20. Each S071-4 stores and inverts three bits of data to form register A. The LRDRA (load Response Data Register A) signal is generated whenever Response Register B is full and A is empty, see 377A for details. The LRDRA signal transfers the Response data word from B to A.

The PDP-8L computer has a "party line IO" so whenever the computer decides a word can be accepted an INPUT RESPONSE DATA (IRD) instruction is issued, see 370 and 377A for further details. The decoded IRD instruction generates the $\overline{\text{ENABLE RESP. DATA}}$ signal which gates the response data on the Data input buss. The logic gating for each bus is: $\overline{\text{ACOO}} = \overline{\text{COO} \cdot \text{ENABLE RESP. DATA}}$ Note the logic internal to the System Controller is:

+7 logic "0"

-7 logic "1"

on DATA BUS the logic levels are

+5 logic "1"

0V logic "0"

$\overline{\text{Data}}$ is set on the Data Buss.

9. Response Data Register B - GI 373A

The Response Data Register B circuit card shifts the DATA (DELAYED) and parallel loads the response data into RESPONSE DATA REGISTER B, refer to Figure 21. The S016 (L) and (H) provides the shift register. The data from the shift register is loaded into RESPONSE DATA REGISTER B by LRDRB (load Response data Register B) which happens at TR38 time. The gating on bits 3-5 load either the three status bits into Register B or the sign and two MSB's of the Response data into register B. The logic for bit 3 is:

SIGN·$\overline{\text{RESP. STATUS ENABLE}}$ + MULTIPLE RESPONSE GATED·RESP. STATUS ENABLE

The logic for bits 4 and 5 are similar. Note that the rest of the response data is loaded into register B even if one of the status bits are true. This simplifies the logic since the computer will ignore that part of the status word.

10. Lamp Driver - GI 374

Each GI 374 has six lamp drivers. Any of the MOS logic circuits will drive the lamp drivers. The schematic is shown in Figure 22. The logic is:

-V (logic "1") - lamp on

+V (logic "0") - lamp off

The lamp is connected between the emitter and +V.

11. Response Status - GI 375A

The Response Status Logic receives $\overline{\text{CLOCK}}$ and $\overline{\text{DATA}}$ signals from the Response Receiver (366) circuit and records any data transmission errors (STATUS). See Figure 23.

The Sync Detector circuit detects the "1", "0", "1", "0" sync pattern. The series of B, C, D S080 2 input NOR gates form four latches with gating. Each latch in succession stores the fact that the next part of the sync pattern has occurred. If a clock signal is detected the latches are reset and the sync pattern must be repeated for a sync detection.

The sync output is loaded into the Response Clock Counter. TS25, the first bit out, resets the sync detector. S016 (M) and (N) are shift registers that count the response time periods (TS25 through TS37) from the response clocks. If the correct number (12) of response clocks are received, the shift register will indicate TS36 time at the end of the response signal.

The Response Clock $\overline{\text{Error}}$ flip-flop is reset just prior to the end of the response word and set if TS36 is true at TR38* time. TR38* is two clock periods after the completion of the command word clocking output. Since the 300 foot maximum module distance can cause approximately 900ns round trip delay, the later command word timing is used to set the Response clock $\overline{\text{ERROR}}$ flip-flop.

The flip-flop not getting set indicates that the logic detected too many or not enough clocks from the response. S071-2 (L) delays the $\overline{\text{Data}}$ signal so that it is the right time with respect to clock for loading into the Response Shift Register, see 373A (Response Data

Register).

The two phase response clock (ϕ_1, ϕ_2) is gated on by SYNC and off by TR38*. This inhibits noise from shifting the data before its loaded into Response Data Register B.

The response parity detection circuit is implemented by S071-1 (H and J) and three S080(F) 2 input gates. The flop-flops provide a one bit delay. The feedback logic is:

$$(\overline{PAR} + \overline{DATA\ DELAY})(PAR + DATA\ DEL) = \overline{PAR}\cdot DATA\ DEL + PAR\cdot\overline{DATA\ DEL}$$

This effectively counts the number of ones received. The flip-flops are reset by the SYNC signal. If the signal at pin AP is negative at the completion of the response signal, an even number of "1's" have been received (response parity failure).

Two S080 2-input gates form the No Sync latch. TR21 (the time period just before an expected sync signal) sets the latch. If a SYNC signal is received it resets the latch.

The multiple response latch is mechanized the same way. Figure 18 shows the data status word format. Note that if any one of three status bits (MULTIPLE RESPONSE, RESPONSE CLOCK ERROR, or NO SYNC) are set, the status bits are gated into Response Register B instead of the Response Data. The three status bits are "ored" together to provide the RESP. STATUS ENABLE signal.

If the module detects any fault in the command word, such as even instead of odd parity, the module generates a negative (clock like) signal early, see the System timing diagram. The COMMAND DATA BAD flip-flop is reset at TR18 and set if CLOCK is true at TR22 time.

The COMMAND DATA BAD and RESPONSE PARITY FAIL status bits are loaded in Response Register B with the Response Data, see GI 373A.

12. Power Relay - GI 376

The Power Relay delays the -V to the modules, see Figure 24. This assures the Power up reset circuitry in the Module will work. The Delay from the time the system Controller receives power till the -V is on to modules is approximately 1 second. There is also a delay in the T & C logic (GI 371A) such that no command word is sent for the first few seconds.

13. Computer Interface Logic - GI 377A

The Computer Interface logic decodes computer control signals and generates transfer signals for the storage registers and status signals for the computer, see Figure 25.

When a "6146" (Input Response Data) is executed in the computer, the AC CLEAR and ENABLE RESPONSE DATA signals are generated, see Figure 26 for waveforms. The last number of the instruction refers to "IOP" signals generates; i.e., "6146" causes an IOP4 and IOP2 to be generated, "6151" causes only an IOP1 to be generated. For the "6146" (IRD) the Accumulator of the computer must be reset prior to loading a response word. The $\overline{\text{AC CLEAR BUS}}$ generated by an IOP2 and 614 clears the accumulator of the computer. The IOP4 that follows generates the ENABLE RESPONSE DATA signal. This causes Response data register A to be gated onto the Accumulator Buss lines (ACXX). See GI 372, (Section VII, 8).

The Read Command Instructions "6514" causes a LOAD CDRA signal to be generated in the SC which loads data from the BAC lines into the command data register A. See GI 369A and Figure 26.

The $\overline{\text{INT REQUEST BUS}}$ signal is set to 0V (Interrupt), whenever a command word is needed or a Response word ready for input. The interrupt is inhibited, if the computer has put the SC in the WAIT mode. A "616" and IOP4 puts the SC in the WAIT mode. A "616" and IOP2 allows the SC to continue operation.

Whenever an interrupt is made, the computer will generate a series of "skip commands." The SC decodes SKIP ON RESPONSE FLAG and SKIP ON COMMAND FLAG, see Figure 18. If the $\overline{\text{SKIP BUS}}$ goes to GND (SKIP) the computer then skips the next instruction. This is used to get the computer to the correct interrupt service routine. The logic for generating a SKIP is as follows:

$$\overline{\text{SKIP}} = \text{IOP1}\cdot\text{"614"RDRAF}\ \overline{\text{WAIT}} + \text{IOP1}\cdot\text{"615"}\cdot\text{CDRAE}\cdot\overline{\text{WAIT}}$$

where RDRAF - Response Data Register A Full

CDRAE - Command Data Register A Empty

The logic in the lower half of Figure 25 stores the fact of whether the two command registers and the two response registers are full or empty and generates two asynchronous load signals. The S030A (N) provides two phase clock signals for use only on 377A.

A "616" and IOP1 provides a INIT (initialize) signal to set the Register state (empty or full) to the empty condition. The interrupt F/F is also reset with the initialize signal.

Upon start up, the four empty/full status flip-flops are set to empty. The SC interrupts the computer and generates a skip when a SKIP ON COMMAND FLAG (SCF) is issued. This causes a READ COMMAND DATA to be issued which generates a LOAD CDRA signal loading the first

command word in Register A. Next a latch is set. The logic for setting the latch is:

$$LCDRB = \overline{CDRAE} \cdot \overline{CDRBF} \cdot \phi_1^*$$

As soon as ϕ_2^* is true, LCDRB is generated. The latch is used to prevent a race condition. The LCDRB signal transfers the command word from command Register A to B. The COMMAND DATA REGISTER A EMPTY F/F is set true with LCDRB. This causes the INTERRUPT to be set again and another Command word transferred from the Computer to Register A.

The COMP. INTERFACE READY logic is:

$$\text{COMP. INTERFACE READY} = \overline{RDRAF} \cdot RDRAE \cdot CDRBF \cdot \overline{CDRAE}$$

This allows the first command word to be generated. (Two command registers full, two empty response registers.)

TR15 is shortened to approximately 500ns by the two gate "one shot." TR15 must not be negative when LCDRB is negative. At TR15 time the command word has been generated and CDRB is then considered empty. At that time, register A is transferred to B and another command word is requested. At TR38 time the command word is transferred from the serial in parallel out shift register to Response data register B. The RDRBE (empty) is reset false. If register A is not full (RDRAE false) then a LRDRA signal is generated through the "race preventing latch." The data is RD register A causes an interrupt and eventually an ENABLE RESPONSE DATA, which transfers the data to the computer.

VIII. NASA DATA SYSTEM EXERCISE PROGRAM (NADSEP)

This program is written in Macro 8 for Digital Equipment Corporation's PDP-8L. It is intended for use with the NASA Digital Data Acquisition System Controller.

This program is written to accept input data in a convenient format, either from the teletype keyboard or the teletype paper tape reader. The data is then assembled into a series of command words for the System Controller. Once the command words are assembled, all modules are turned on and all unselected modules are turned off.

At this time each command word is issued and each module response is stored. While command words are being issued, the computer is analyzing the list of response words. The valid data responses are analyzed and the high and low value for each tested module and channel is stored. If the response is an error, the module error counter for the appropriate error type is advanced by 1.

The complete list of command words may be issued a predetermined number of times, or until manually stopped by entering any character from the keyboard.

After the test is completed, the results are printed. The data consists of the number of errors of each type for each module tested and the high and low data limits for each module channel tested.

The rate at which command words are issued is controlled by the System Controller. When the rate is low enough, the computer can analyze the response data between issuing command words. If the computer is unable to analyze the data as it comes in, the data is stored in memory. When the storage area is full, the computer stops issuing command words until the data is analyzed.

The command word data has the following format:

$$M_1, M_2\text{-}M_3; T; C_1\text{-}C_2, C_3$$

This means that modules M_1 and M_2 through M_3 will be given identical tests. As many module groups as desired may be placed in this list, as long as they are all the same type of module. T signifies the module type

H for hi level

L_1 for low level CMIA

L_2 for low level CIAM

The channels tested are C_1 through C_2, and C_3. As many channel groups as desired may be contained in the list. Thus, channels C_1 through C_2 and C_3 will be exercised for modules M_1 and M_2 through M_3. All modules are of Type T.

There may be as many data statements as necessary to define the system being tested. The computer will print a diagnostic statement if something is wrong with the data list.

Two additional statements may be included in the data list. The statement X1000 indicates that the command word list is to be issued 1000 times. The number is decimal and may be between 1 and 4095 inclusive.

If this statement is not included, the test runs until any character is entered on the keyboard.

The second statement is $I. This controls the way the command word list is assembled from the data list. Its purpose is to assemble command words in a sequence suitable for the interleave mode of operation. To

illustrate, consider the data list:

1, 5, 3-5; H; 1-3, 7

If $I is not used, the command word sequence would access modules and channels in the following order:

Module	Channel
1	1
1	2
1	3
1	7
5	1
5	2
5	3
5	7
3	1
3	2
3	3
3	7
4	1
4	2
4	3
4	7
5	1
5	2
5	3
5	7

Note that a module is accessed 4 times before the next module is considered.

Now consider the case for the same data but with the $I statement.

```
1, 5, 3-5; H; 1-3, 7
$I
```

This generates the command word sequence as follows:

Module	Channel
1	7
5	7
3	7
4	7
5	7
1	3
5	3
3	3
4	3
5	3
1	2
5	2
3	2
4	2
5	2
1	1
5	1
3	1
4	1
5	1

In this case, no module is accessed for two consecutive command words. Thus, proper interleave operation is achieved.

Note that the data list can be formed to access certain modules more often than other modules.

If an error is made in entering data, "rubout" will delete characters one at a time from the end of the list. A carriage return and line feed is considered as one character. The rubout prints a back slash (\) for each character deleted.

The input list is terminated with an asterisk (*). When the * is sensed, the operator has the option of prepunching a paper tape of the test data. This may be used for data entry on future tests of that configuration.

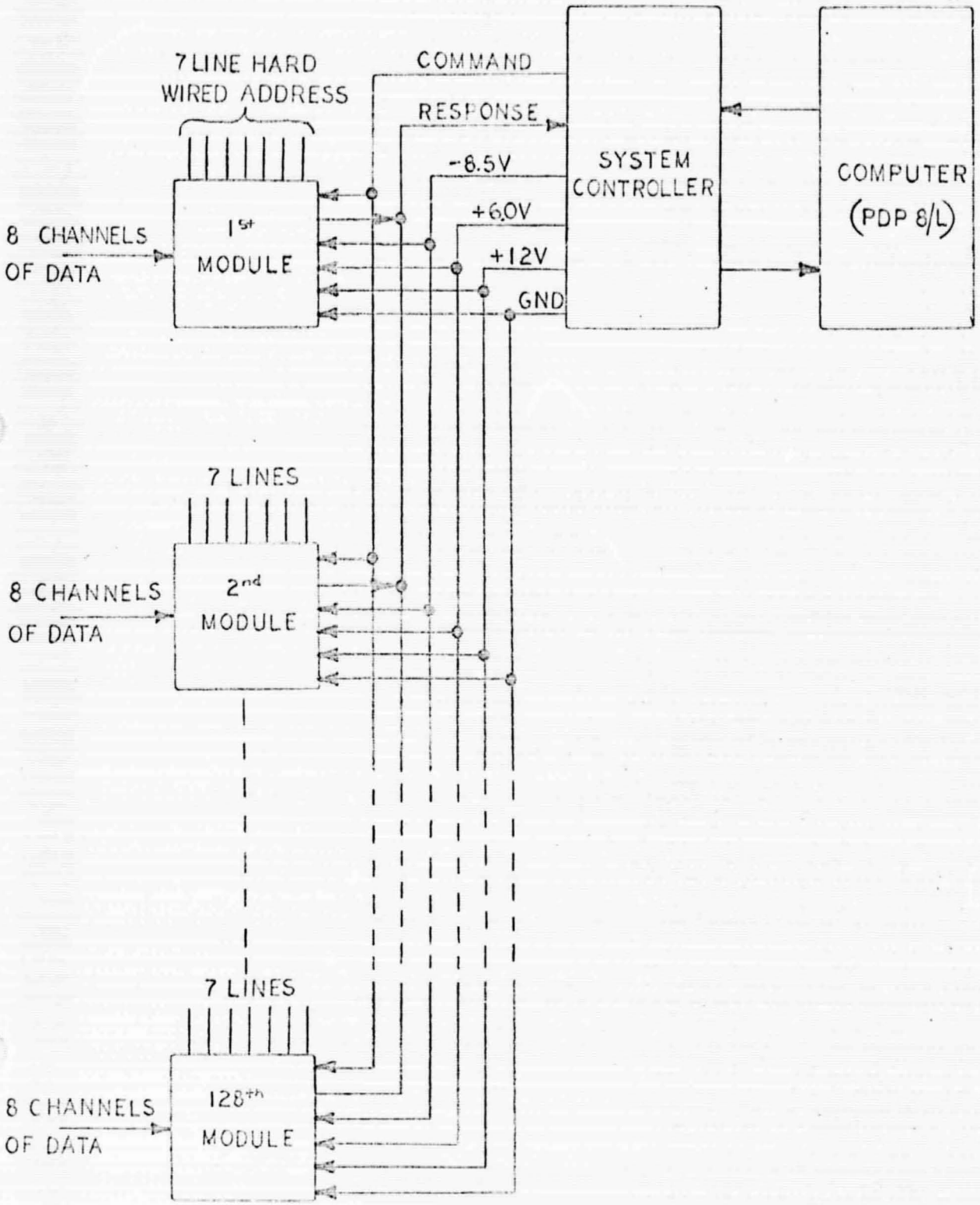
The system test begins as soon as the tape is punched. Test results are printed as soon as the test is completed.

All numbers in the test results are decimal except the high and low data values. These are octal presentations of the data bits including sign as received from the system modules.

Following are the results of a typical test sequence.

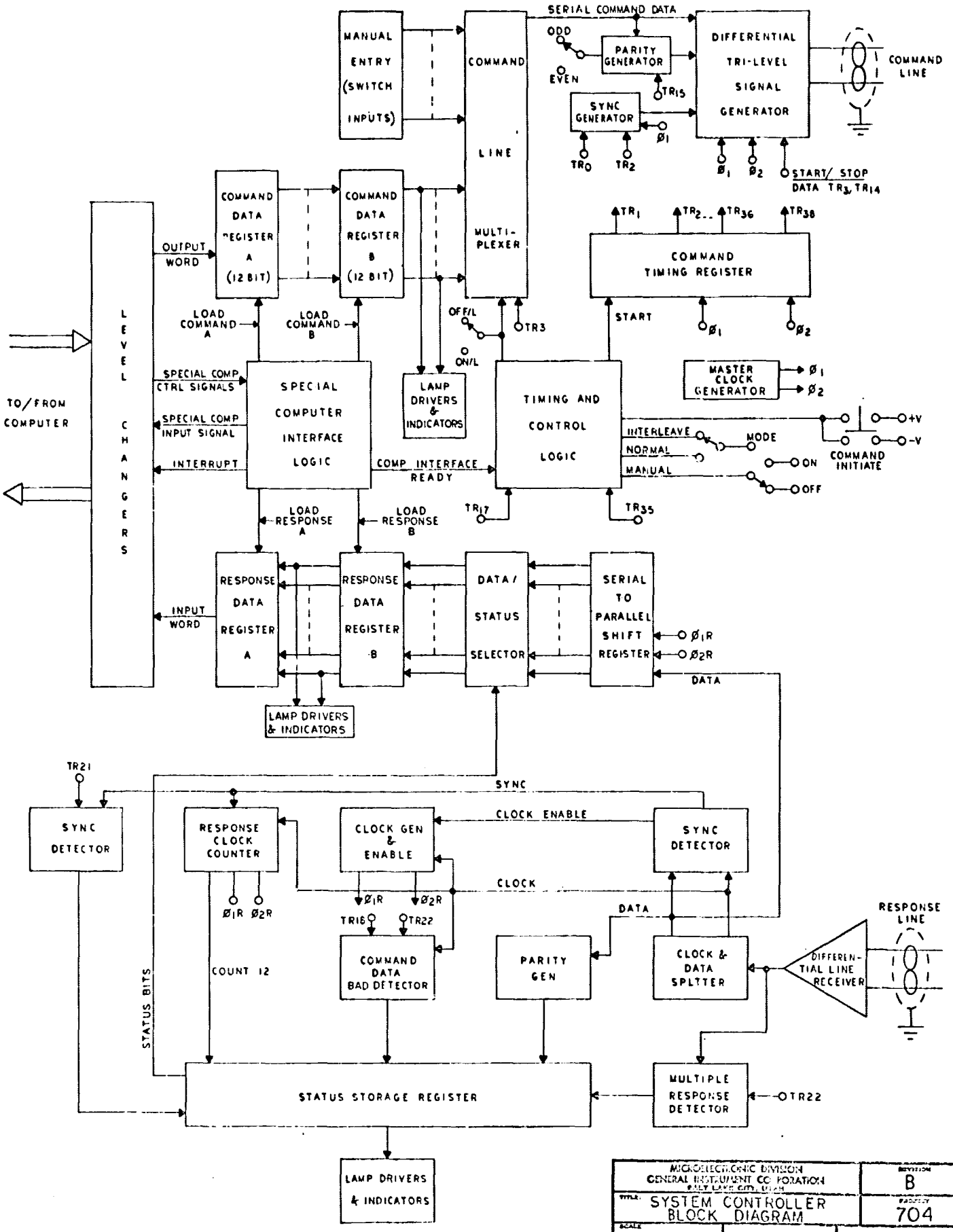
```
ENTER DATA

56,61-63,68-69;H;0,1,15
N\X1000*

TAPE?
(Y OR N) Y
56,61-63,68-69;H;0,1,15
X1000*


MODULE     CDB    RPF    MR     RCE    NS
 0056     0000   0000   0000   3000   3000
 0061     0000   0000   0000   0000   0000
 0062     0000   0000   0000   0000   0000
 0063     0000   0000   0000   0000   0000
 0068     0000   0000   0000   3000   3000
 0069     0000   0000   0000   3000   3000

MODULE   CHANNEL   HIGH    LOW
 0056     0000     0000   0000
 0056     0001     0000   0000
 0056     0015     0000   0000

 0061     0000     0006   0005
 0061     0001     0377   0400
 0061     0015     0356   0352

 0062     0000     0004   0003
 0062     0001     0377   0377
 0062     0015     0361   0360

 0063     0000     0004   0003
 0063     0001     0377   0400
 0063     0015     0354   0351

 0068     0000     0000   0000
 0068     0001     0000   0000
 0068     0015     0000   0000

 0069     0000     0000   0000
 0069     0001     0000   0000
 0069     0015     0000   0000


ENTER DATA
```

```
ENTER DATA

56,61-63,68-69;H;0,1,15
N\X1000*

TAPE?
(Y OR N) Y
56,61-63,68-69;H;0,1,15
X1000*


MODULE     CDB    RPF    MR     RCE    NS
 0056     0000   0000   0000   3000   3000
 0061     0000   0000   0000   0000   0000
 0062     0000   0000   0000   0000   0000
 0063     0000   0000   0000   0000   0000
 0068     0000   0000   0000   3000   3000
 0069     0000   0000   0000   3000   3000

MODULE   CHANNEL   HIGH   LOW
 0056     0000     0000   0000
 0056     0001     0000   0000
 0056     0015     0000   0000

 0061     0000     0006   0005
 0061     0001     0377   0400
 0061     0015     0356   0352

 0062     0000     0004   0003
 0062     0001     0377   0377
 0062     0015     0361   0360

 0063     0000     0004   0003
 0063     0001     0377   0400
 0063     0015     0354   0351

 0068     0000     0000   0000
 0068     0001     0000   0000
 0068     0015     0000   0000

 0069     0000     0000   0000
 0069     0001     0000   0000
 0069     0015     0000   0000


ENTER DATA
```



MICROELECTRONIC DIVISION GENERAL INSTRUMENT CORPORATION SALT LAKE CITY, UTAH					REVISION
TITLE: DIGITAL DATA SAMPLING SYSTEM BLOCK DIAGRAM					PROJECT NASA
SCALE					
	DRAWN	CHECKED	PROC. APP.	ENG. APP.	DWG. NO.
BY	K Raine				A 704-5014
DATE	2-24-70				

Figure 1.



MICROELECTRONIC DIVISION GENERAL INSTRUMENT CORPORATION SALT LAKE CITY, UTAH	REVISION B
TITLE: SYSTEM CONTROLLER BLOCK DIAGRAM	PAGE 704
SCALE	
BY	
DATE 12/19/69	DWG. NO. C-704-500

Figure 2.

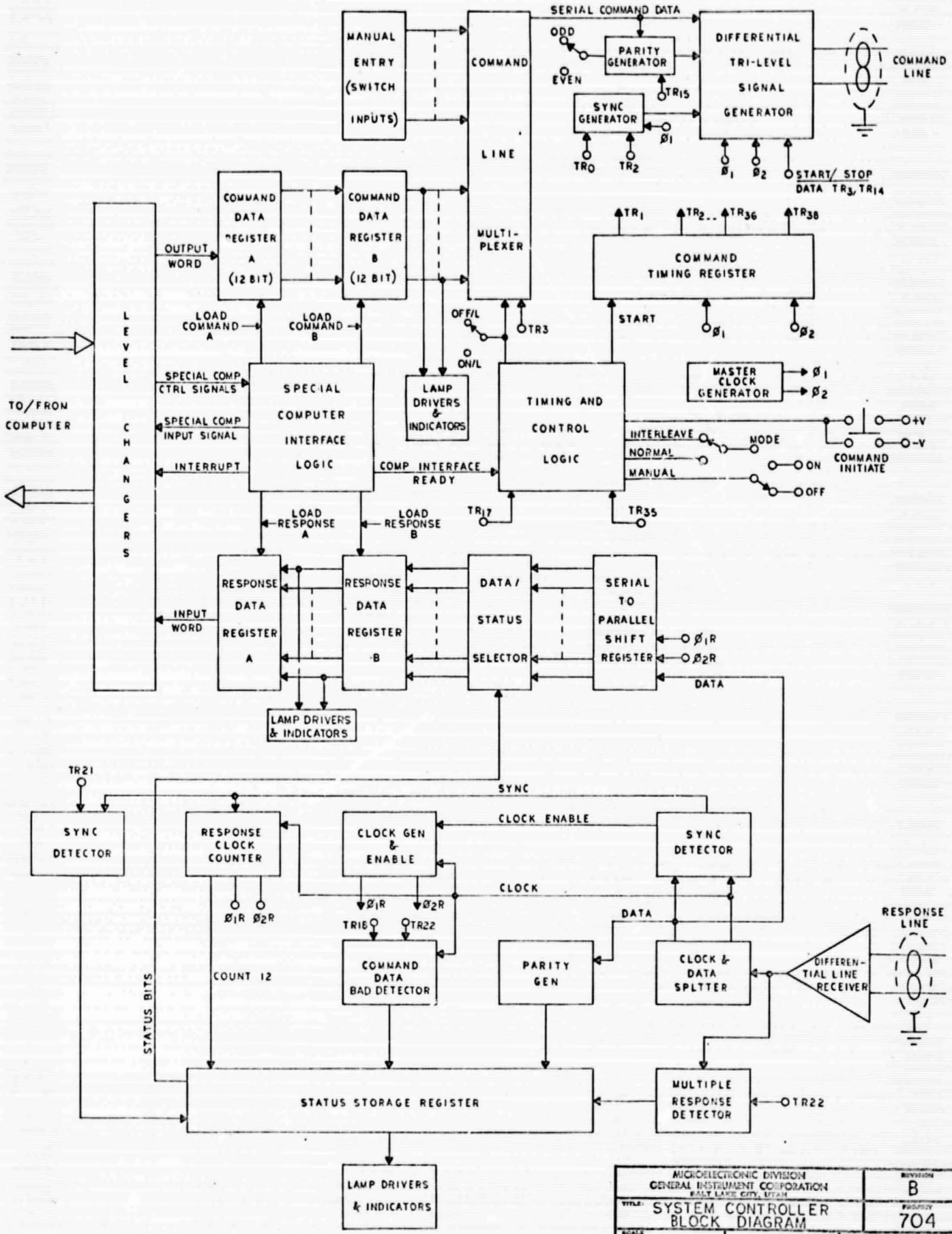


Figure 2.

MICROELECTRONIC DIVISION GENERAL INSTRUMENT CORPORATION SALT LAKE CITY, UTAH		DIVISION B
TITLE: SYSTEM CONTROLLER BLOCK DIAGRAM		PROJECT 704
SCALE		
	DRAWN	DWG. NO.
BY	J Hardy	C-704-500
DATE	12/10/69	

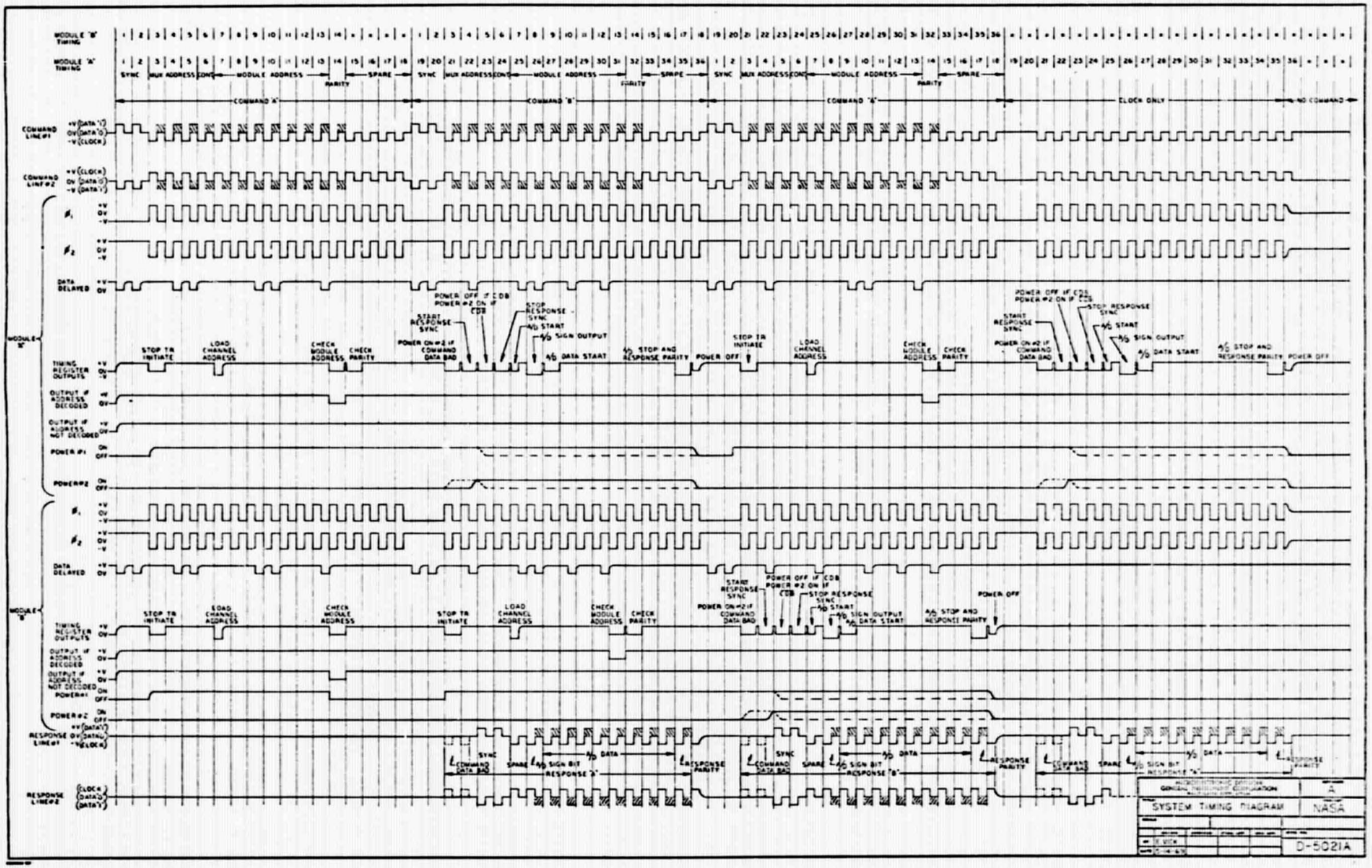

MODULE 'B' TIMING
MODULE 'A' TIMING
SYNC
MUX ADDRESS
CONT
MODULE ADDRESS
PARITY
SPARE
COMMAND 'A'
COMMAND 'B'
COMMAND 'A'
CLOCK ONLY
NO COMMAND
COMMAND LINE #1
COMMAND LINE #2
DATA DELAYED
MODULE 'A'
TIMING REGISTER OUTPUTS
STOP TR INITIATE
LOAD CHANNEL ADDRESS
CHECK MODULE ADDRESS
CHECK PARITY
START RESPONSE SYNC
POWER ON #2 IF COMMAND DATA BAD
POWER OFF IF CDB
POWER #2 ON IF CDB
STOP RESPONSE SYNC
½ START
½ SIGN OUTPUT
½ DATA START
½ STOP AND RESPONSE PARITY
POWER OFF
OUTPUT IF ADDRESS DECODED
OUTPUT IF ADDRESS NOT DECODED
POWER #1
POWER #2
MODULE 'B'
RESPONSE LINE #1
RESPONSE LINE #2
COMMAND DATA BAD
SIGN BIT
DATA
RESPONSE PARITY
RESPONSE 'A'
RESPONSE 'B'
SYSTEM TIMING DIAGRAM
NASA
D-5021A

Figure 3.

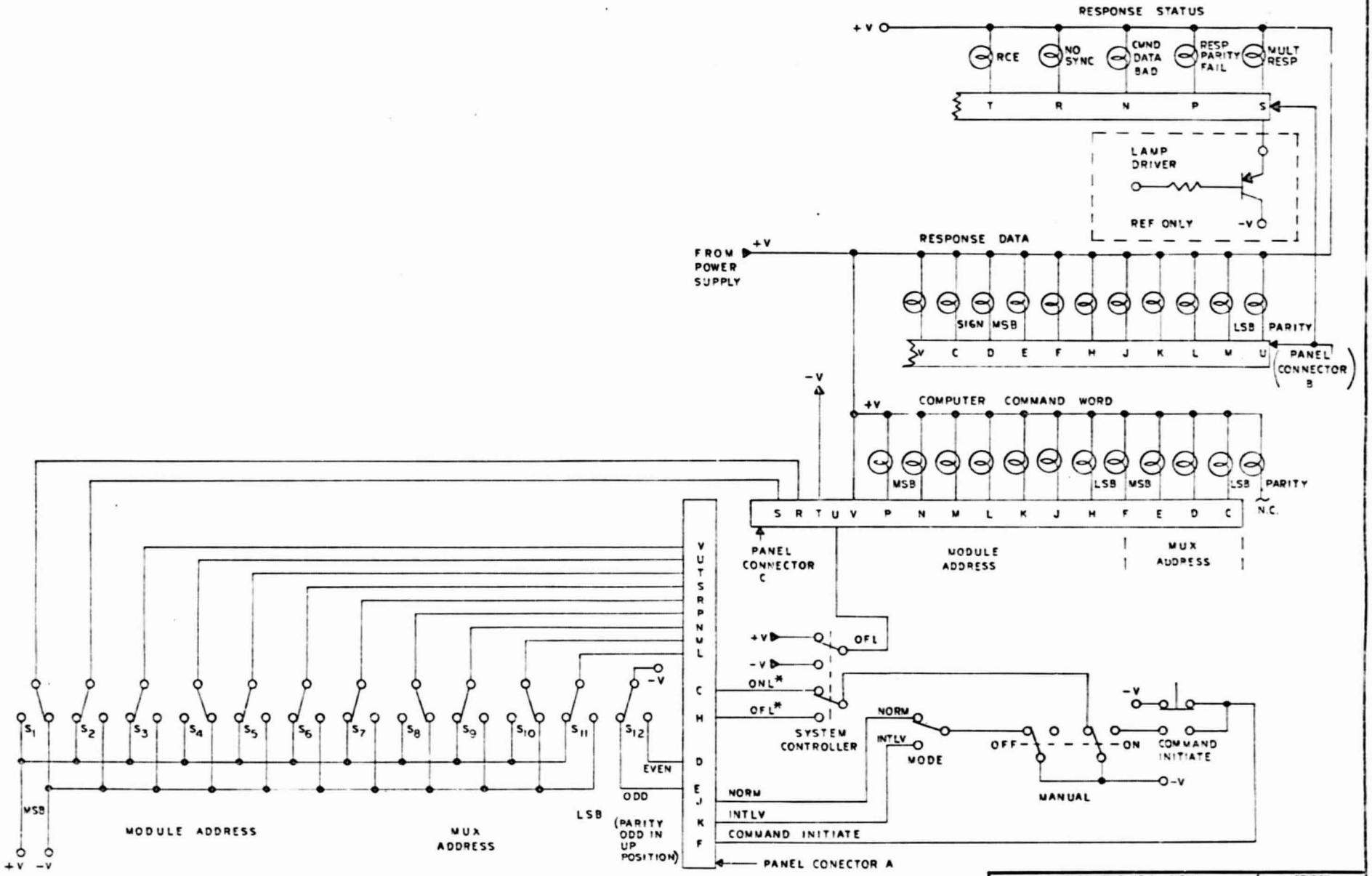
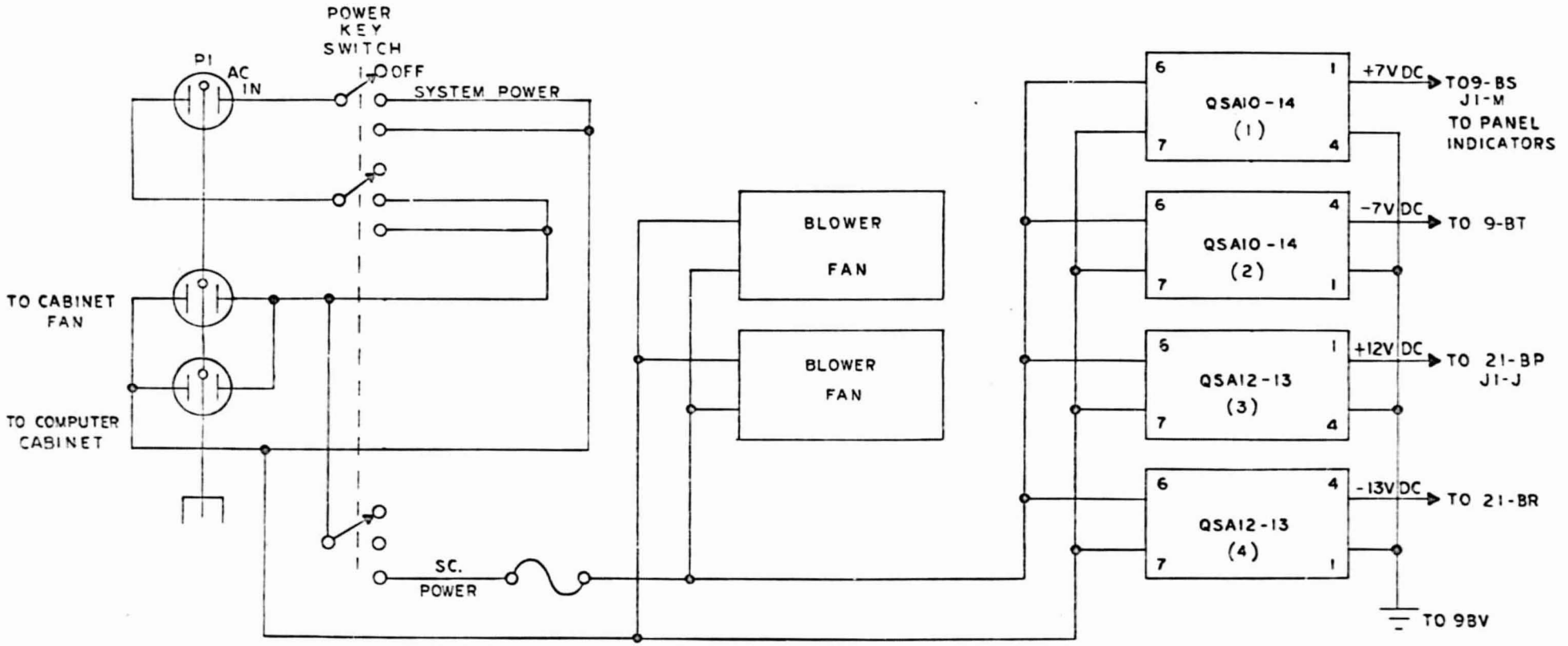
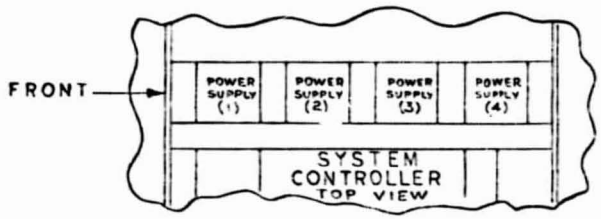

REVISIONS
LTR DATE E.C.N. DESCRIPTION BY CH PROG APP
RESPONSE STATUS
+V
RCE
NO SYNC
CMND DATA BAD
RESP PARITY FAIL
MULT RESP
T R N P S
LAMP DRIVER
REF ONLY
-V
RESPONSE DATA
FROM POWER SUPPLY
+V
SIGN MSB
LSB PARITY
V C D E F H J K L M U
PANEL CONNECTOR B
-V
COMPUTER COMMAND WORD
+V
MSB
LSB MSB
LSB PARITY
N.C.
S R T U V P N M L K J H F E D C
PANEL CONNECTOR C
MODULE ADDRESS
MUX ADDRESS
V U T S R P N M L C H D E J K F
+V
OFL
-V
ONL*
OFL*
SYSTEM CONTROLLER
NORM
INTLV
MODE
OFF
ON
COMMAND INITIATE
-V
MANUAL
NORM
INTLV
COMMAND INITIATE
PANEL CONECTOR A
S1 S2 S3 S4 S5 S6 S7 S8 S9 S10 S11 S12
-V
EVEN
ODD
(PARITY ODD IN UP POSITION)
LSB
MSB
MODULE ADDRESS
MUX ADDRESS
+V -V
NOTE: WHEN SWITCH IN +V (UP) POSITION = "1"
ODD PARITY = -V (UP)
EVEN PARITY = +V (DOWN)
MICROELECTRONIC DIVISION
GENERAL INSTRUMENT CORPORATION
SALT LAKE CITY, UTAH
REVISION
TITLE: FRONT PANEL SYSTEM CONTROLLER
PROJECT NASA
SCALE
DRAWN CHECKED PROG APP ENG APP
DWG. NO.
BY J. Fowler
DATE 12/9/69
C704-3011

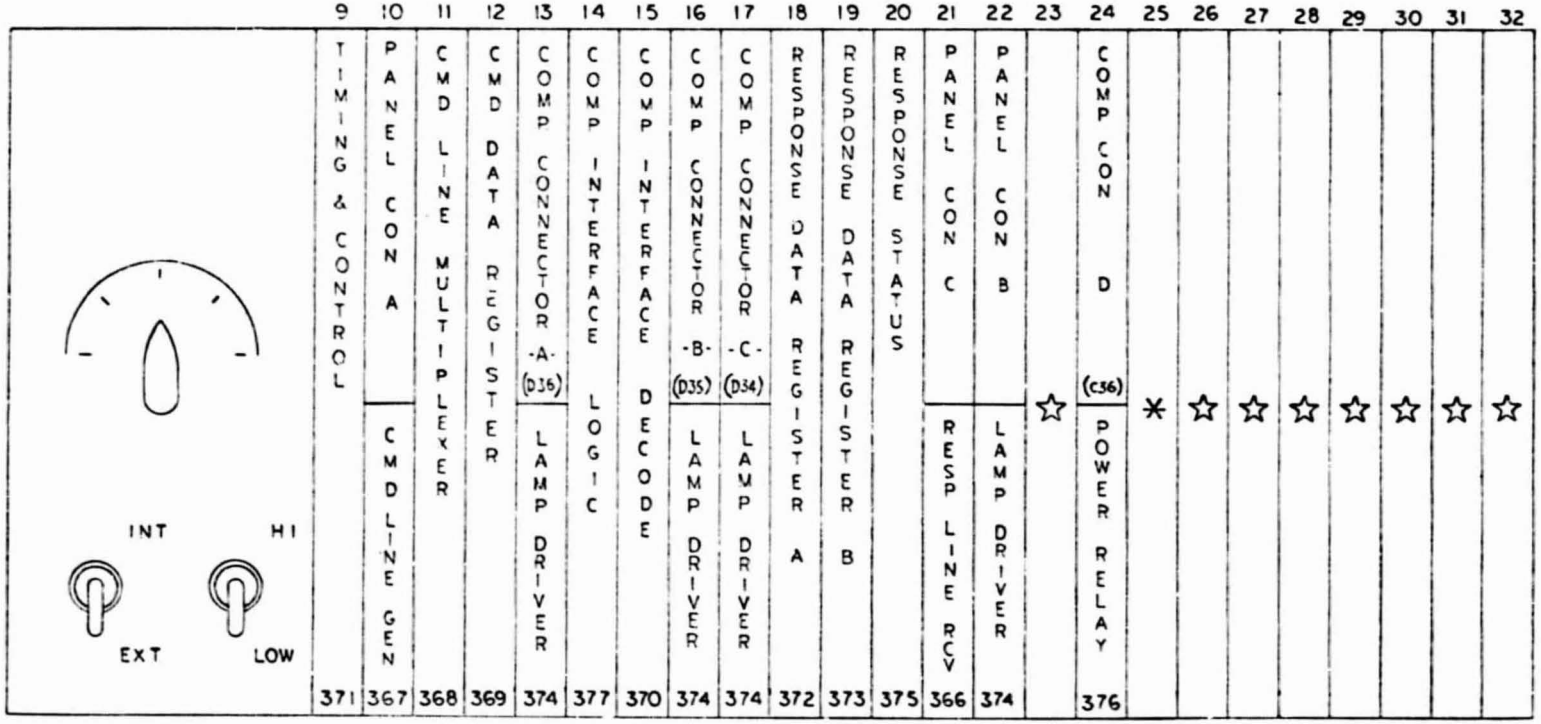
Figure 6.





MICROELECTRONIC DIVISION GENERAL INSTRUMENT CORPORATION SALT LAKE CITY, UTAH		REVISION
TITLE: NASA SYSTEM CONTROLLER AC DISTRIBUTION & POWER SUPPLY WIRING		PROJECT 704
SCALE		
	DRAWN / CHECKED / PROC. APP. / ENG. APP.	DWG. NO.
BY	J Fowler	B704-5013
DATE	12-22-69	

Figure 7.



NOTES:

* DO NOT USE

☆ SPARE

REVISIONS

SYM.	DAT E	E.C.N.	DESCRIPTION	DY	CK	PROG	APP.

MICROELECTRONIC DIVISION
GENERAL INSTRUMENT CORPORATION
SALT LAKE CITY, UTAH

REVISION

TITLE: SYSTEM CONTROLLER PC CARD LAYOUT

PROJECT 704

SCALE

	DRAWN	CHECKED	PROG. APP.	ENG. APP.	DWG. NO.
BY	J Fowler				B-704-5011
DATE	12·12·69				

Figure 8

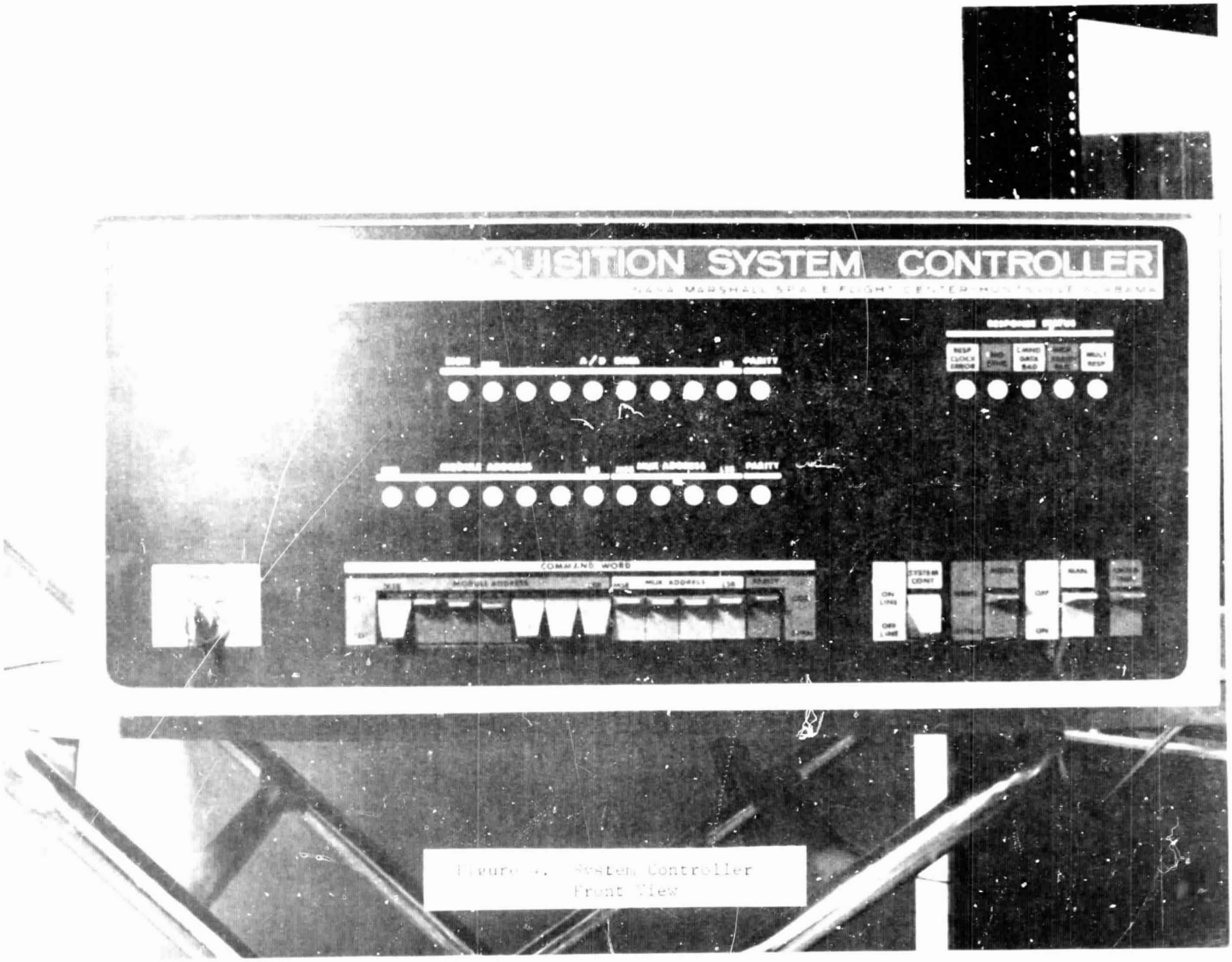


Figure 4. System Controller
Front View

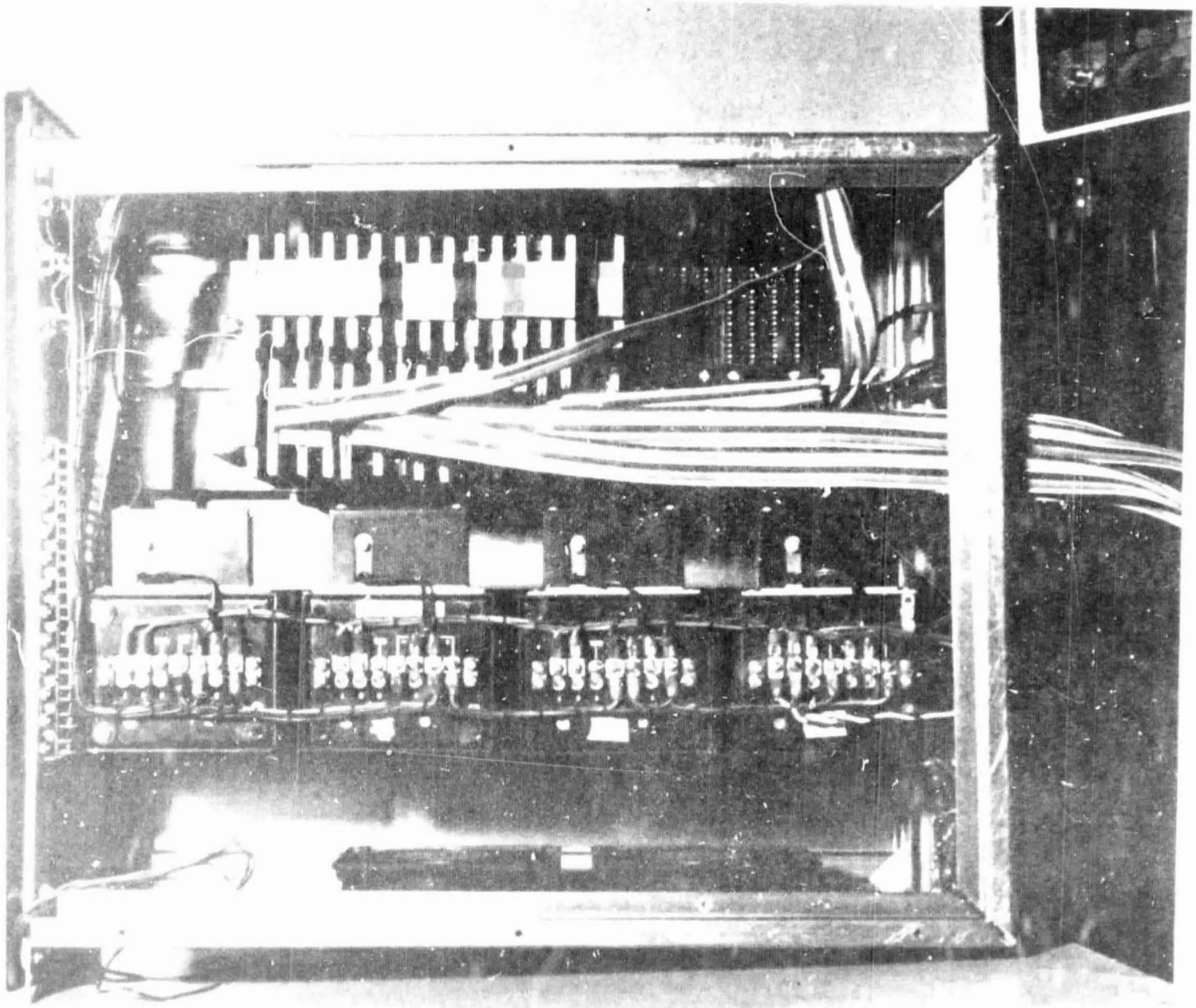


Figure 3. System Controller
Bottom View

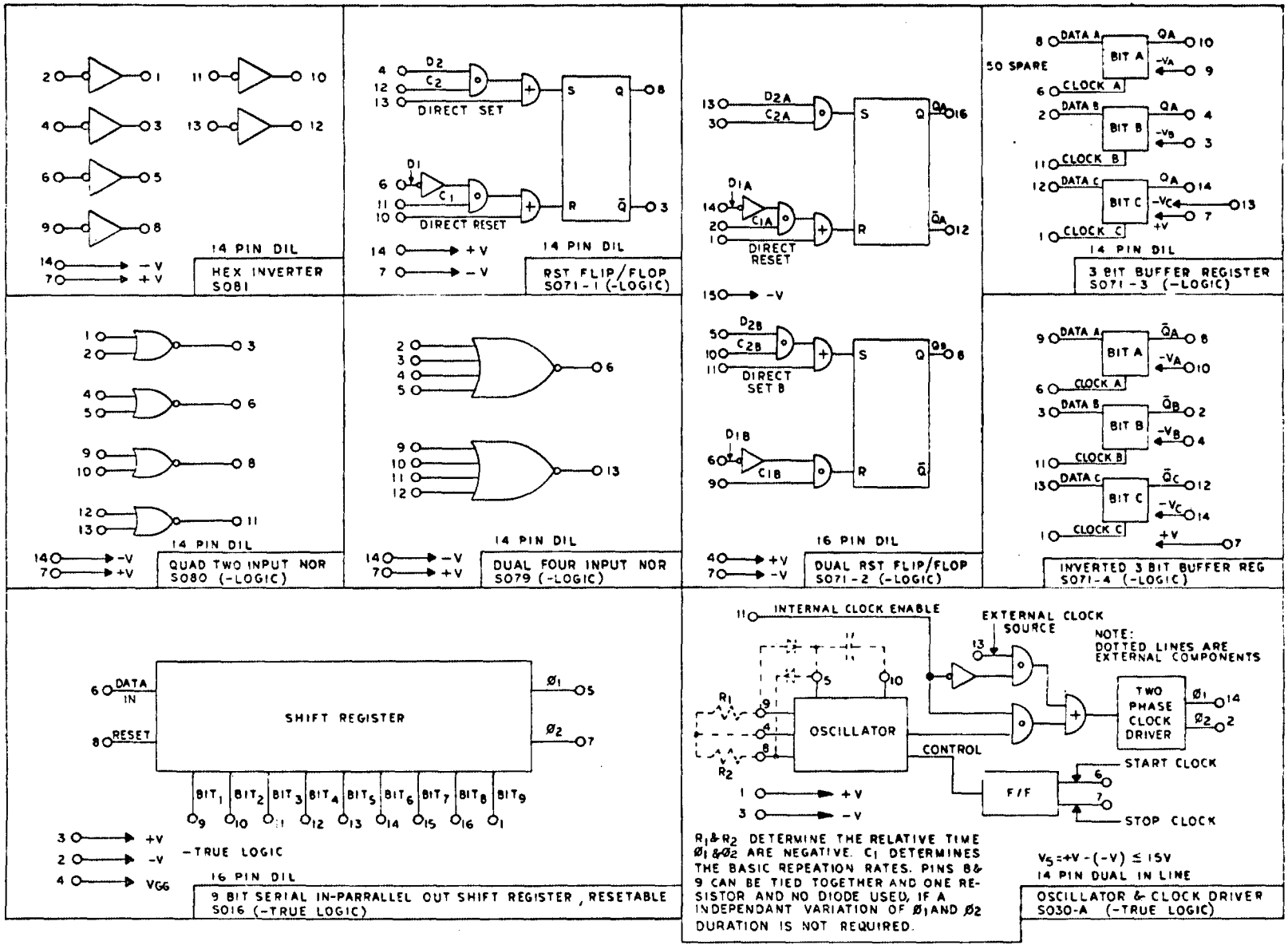


Figure 9

MICROELECTRONIC DIVISION GENERAL INSTRUMENT CORPORATION SALT LAKE CITY, UTAH					DIVISION
TITLE: COMPONENT DIAGRAMS PIN CONFIGURATIONS					PROJECT 704
SCALE					
	DRAWN	CHECKED	PROD. APP.	ENG. APP.	DWG. NO. C704-1014
BY	B Fowler				
DATE	12-19-69				

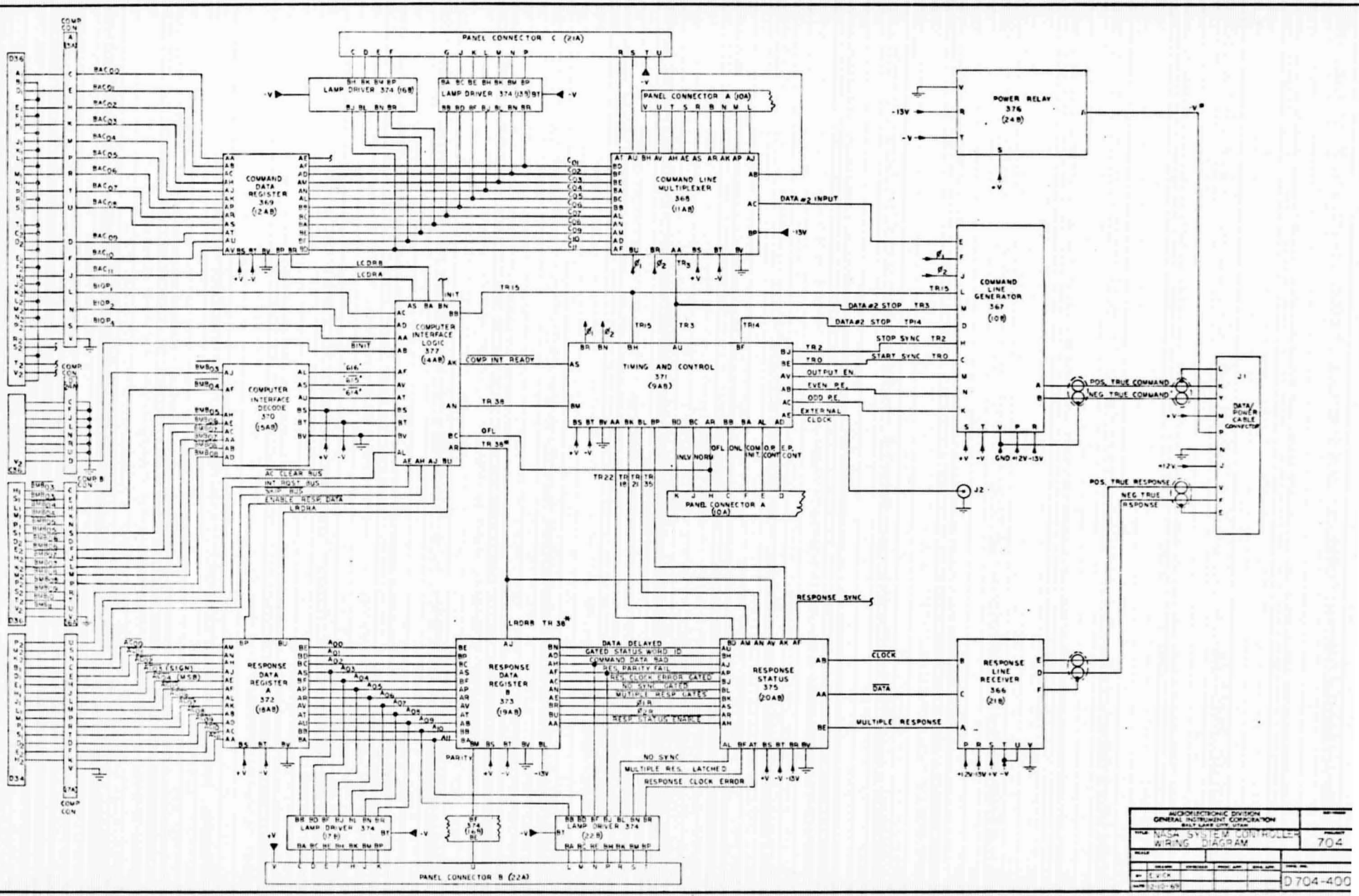

PANEL CONNECTOR C (21A)
LAMP DRIVER 374 (16B)
LAMP DRIVER 374 (13B)
PANEL CONNECTOR A (10A)
POWER RELAY 376 (24B)
COMMAND DATA REGISTER 369 (12AB)
COMMAND LINE MULTIPLEXER 368 (11AB)
DATA #2 INPUT
COMMAND LINE GENERATOR 367 (10B)
COMPUTER INTERFACE LOGIC 372 (14AB)
COMPUTER INTERFACE DECODE 370 (15AB)
TIMING AND CONTROL 371 (9AB)
POS. TRUE COMMAND
NEG. TRUE COMMAND
DATA/POWER CABLE CONNECTOR J1
POS. TRUE RESPONSE
NEG. TRUE RESPONSE
RESPONSE DATA REGISTER A 372 (18AB)
RESPONSE DATA REGISTER B 373 (19AB)
RESPONSE STATUS 375 (20AB)
RESPONSE LINE RECEIVER 366 (21B)
RESPONSE SYNC
MULTIPLE RESPONSE
NO SYNC
MULTIPLE RES. LATCHED
RESPONSE CLOCK ERROR
PANEL CONNECTOR B (22A)
MICROELECTRONIC DIVISION GENERAL INSTRUMENT CORPORATION
NASA SYSTEM CONTROLLER WIRING DIAGRAM
704
D 704-400

Figure 10

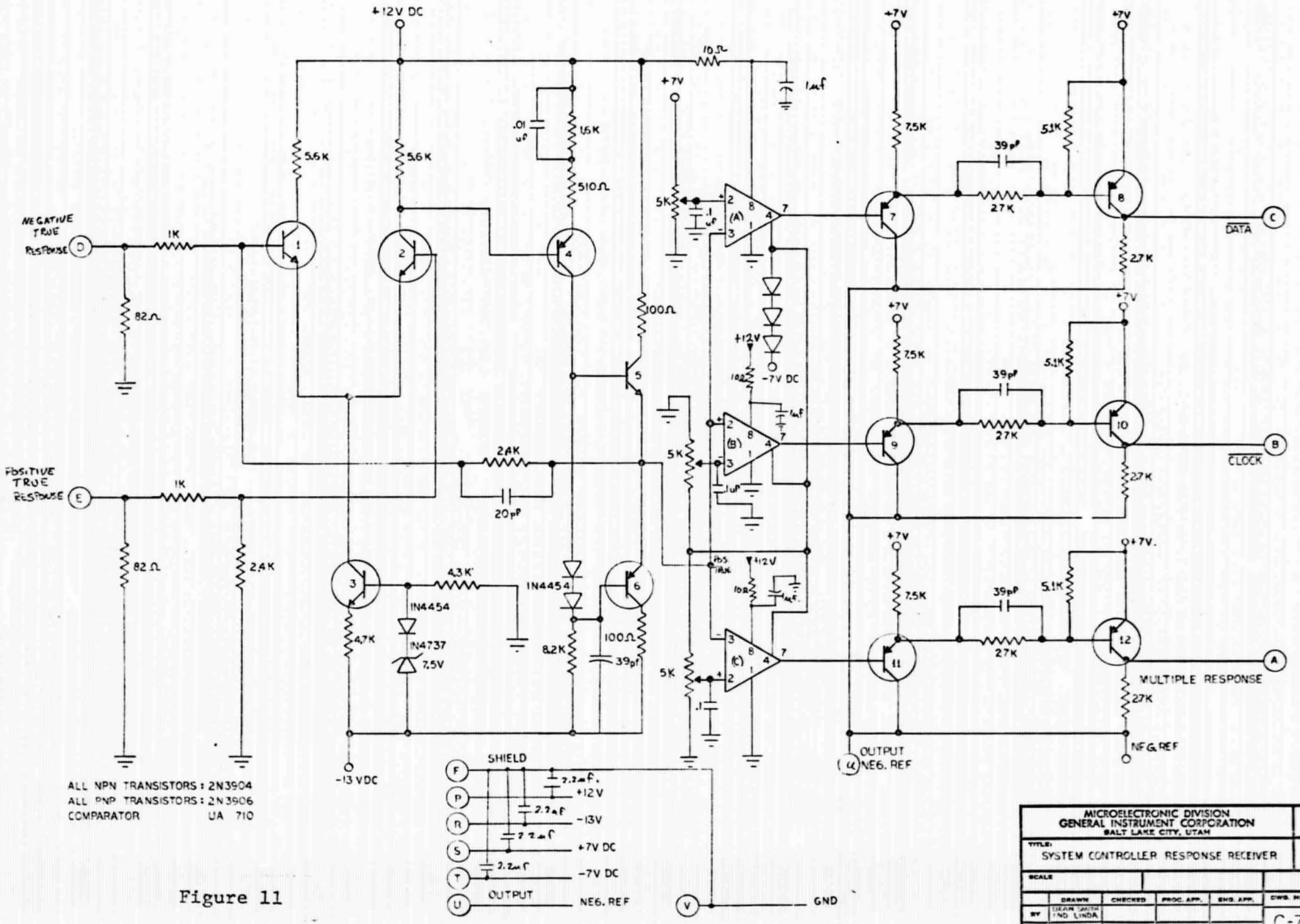


Figure 11

REVISIONS

SYM	DATE	E.C.N.	DESCRIPTION	BY	CHK'D/PROC	APP'D

MICROELECTRONIC DIVISION GENERAL INSTRUMENT CORPORATION SALT LAKE CITY, UTAH			REVISION
TITLE: SYSTEM CONTROLLER RESPONSE RECEIVER			PROJECT NASA
SCALE			GI 366A
	DRAWN	CHECKED / PROC. APP. / ENG. APP.	DWG. NO.
BY	DEAN SMITH AND LINDA		C-704-2001
DATE	12. 3/69		

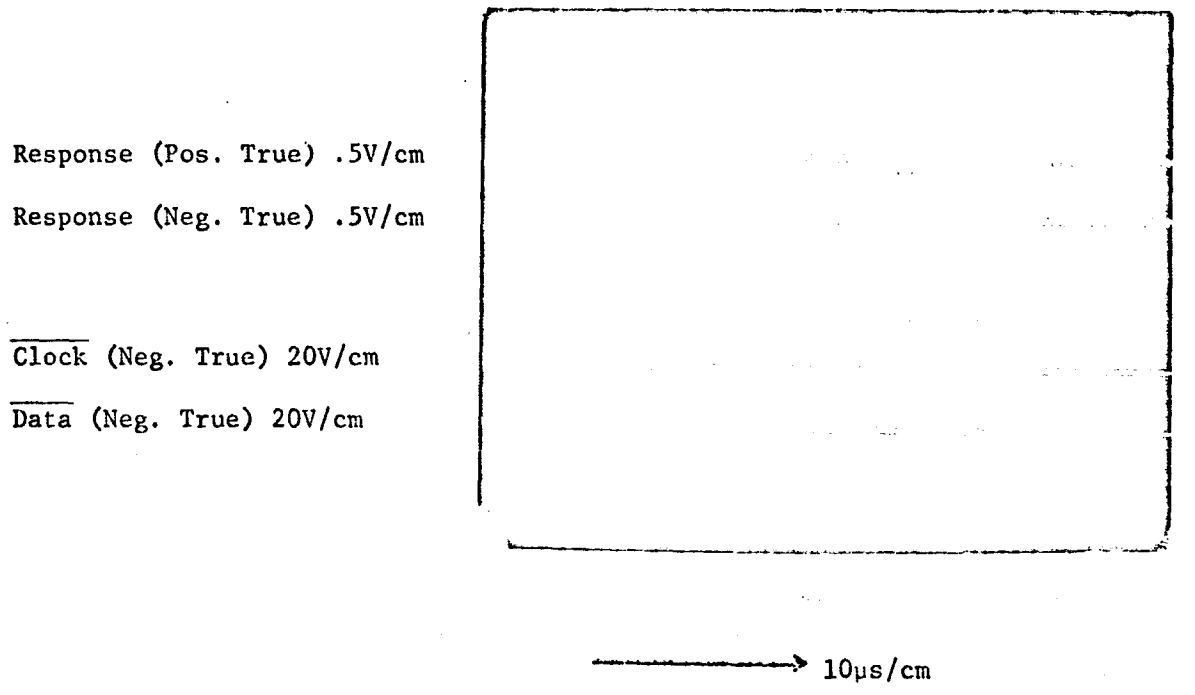


Figure 12. Receiver Waveforms.

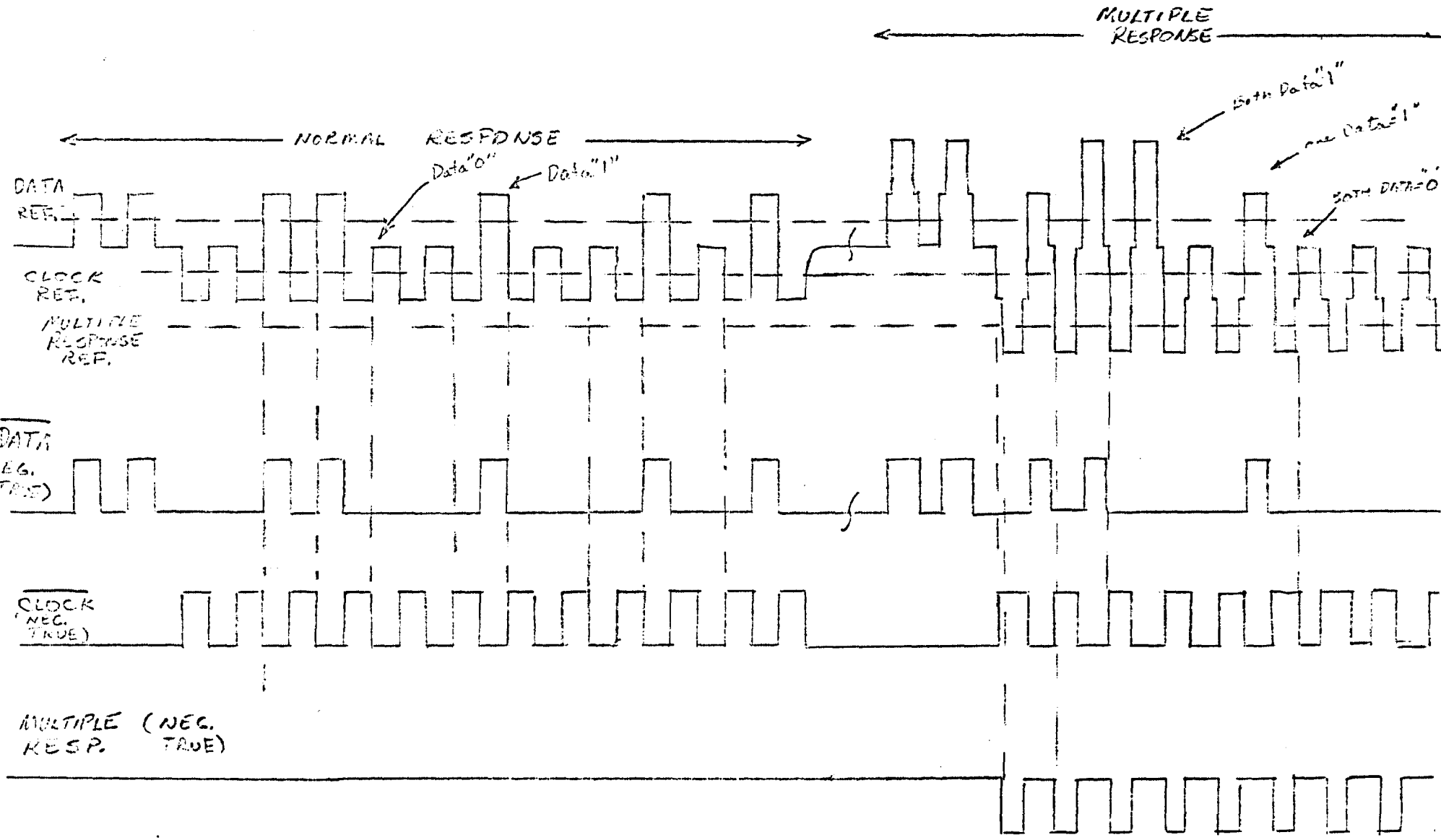


FIGURE 13 — RECEIVER WAVEFORMS.

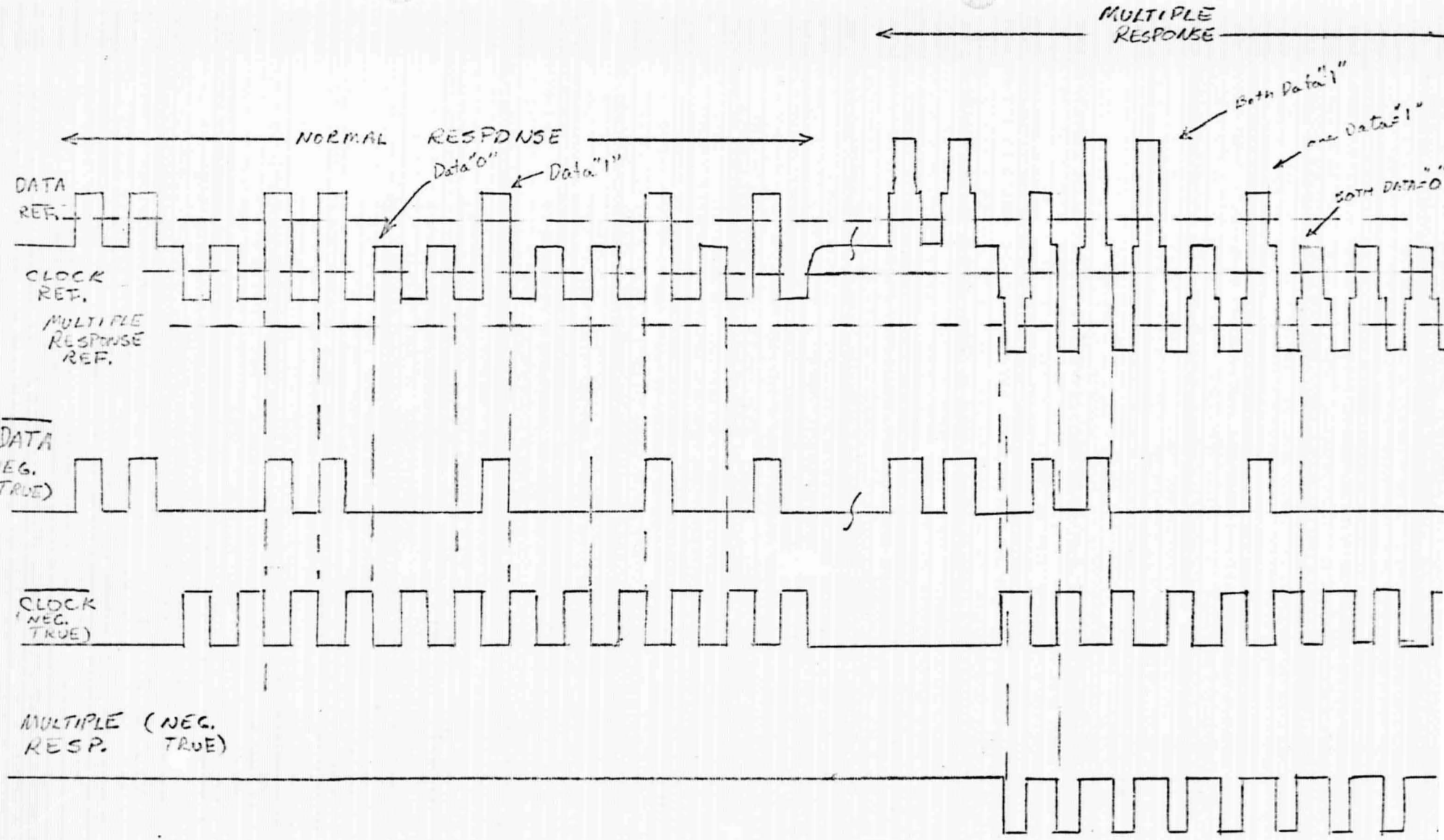
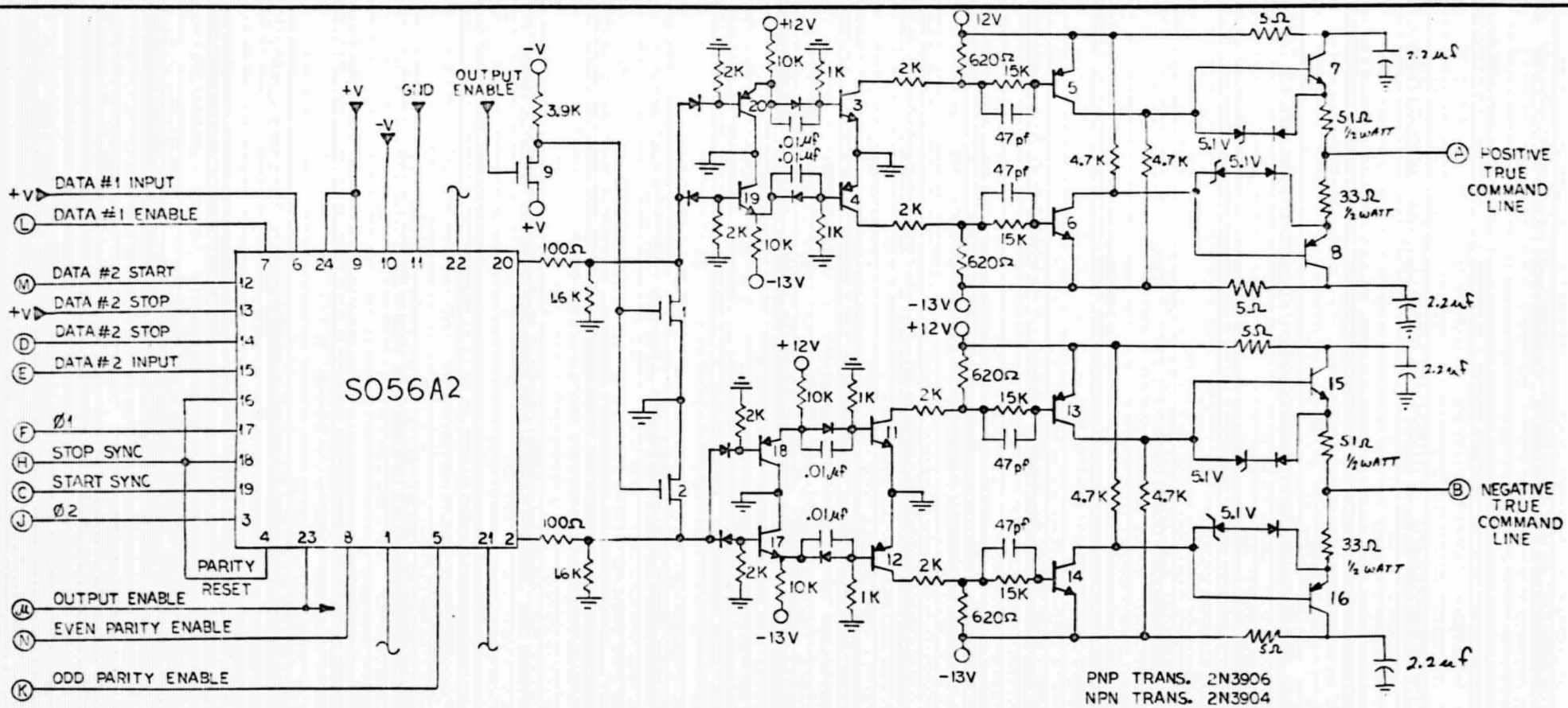


FIGURE 13 — RECEIVER WAVE FORMS.



REVISIONS							
SYM	DATE	E.C.N.	DESCRIPTION	BY	CK.	PROC.	APP.
	10/3/69		MINOR CORRECTION	SW			
	11/21/69		OUTPUT RESISTORS CHANGED	RG			

MICROELECTRONIC DIVISION
GENERAL INSTRUMENT CORPORATION
SALT LAKE CITY, UTAH

REVISION

TITLE: SYSTEM CONTROLLER COMMAND LINE GEN.

PROJECT: NASA

SCALE

GI 367A

	DRAWN	CHECKED	PROC. APP.	ENG. APP.
BY	Linda			
DATE	6/26/69			

DWG. NO. B-704-2013

Figure 14

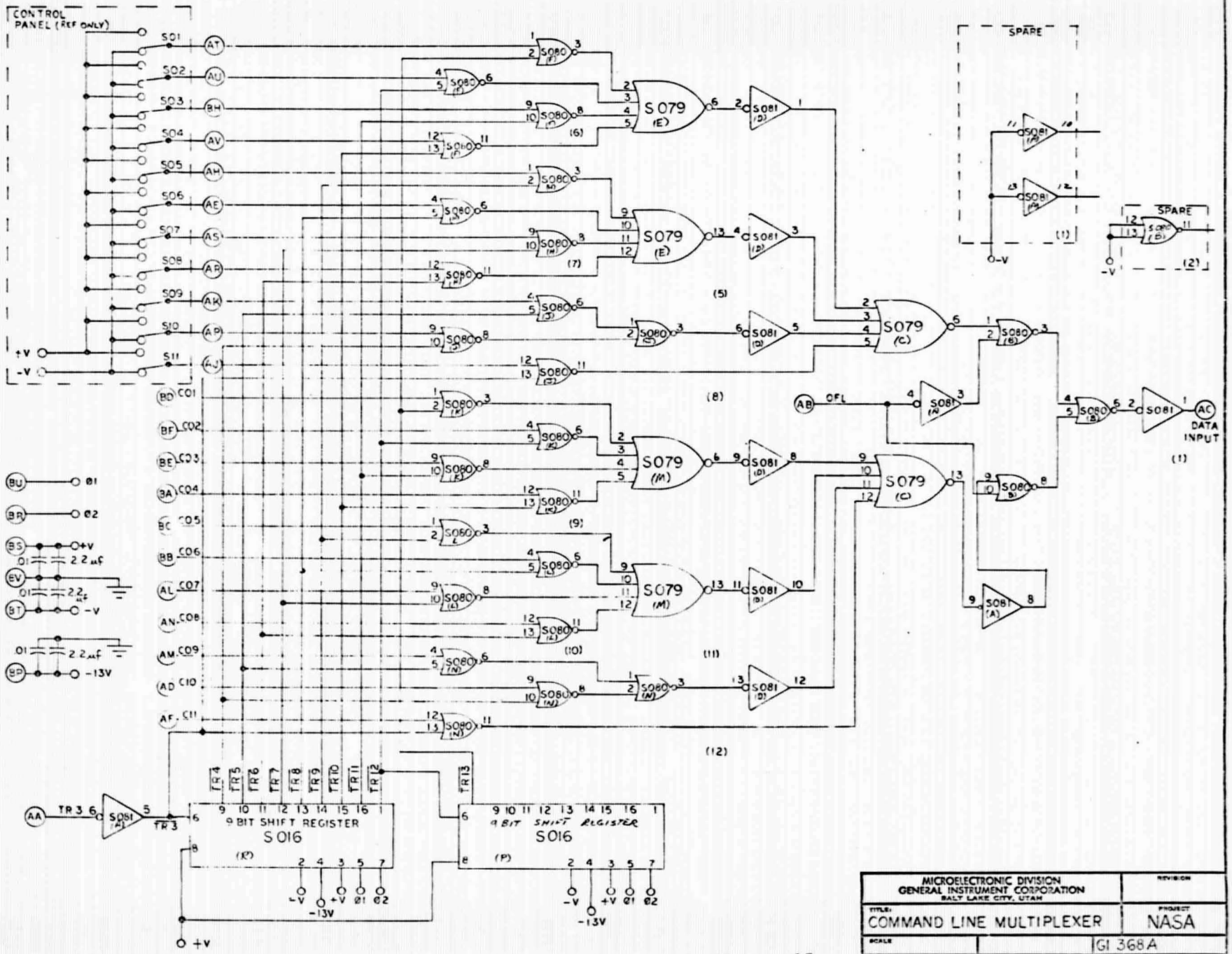


Figure 15

MICROELECTRONIC DIVISION GENERAL INSTRUMENT CORPORATION SALT LAKE CITY, UTAH	REVISION
TITLE: COMMAND LINE MULTIPLEXER	PROJECT: NASA
SCALE	GI 368A
DRAWN / CHECKED / PROG. APP. / ENG. APP.	DWG. NO.
BY / DATE 12-3-69	C-704-1009

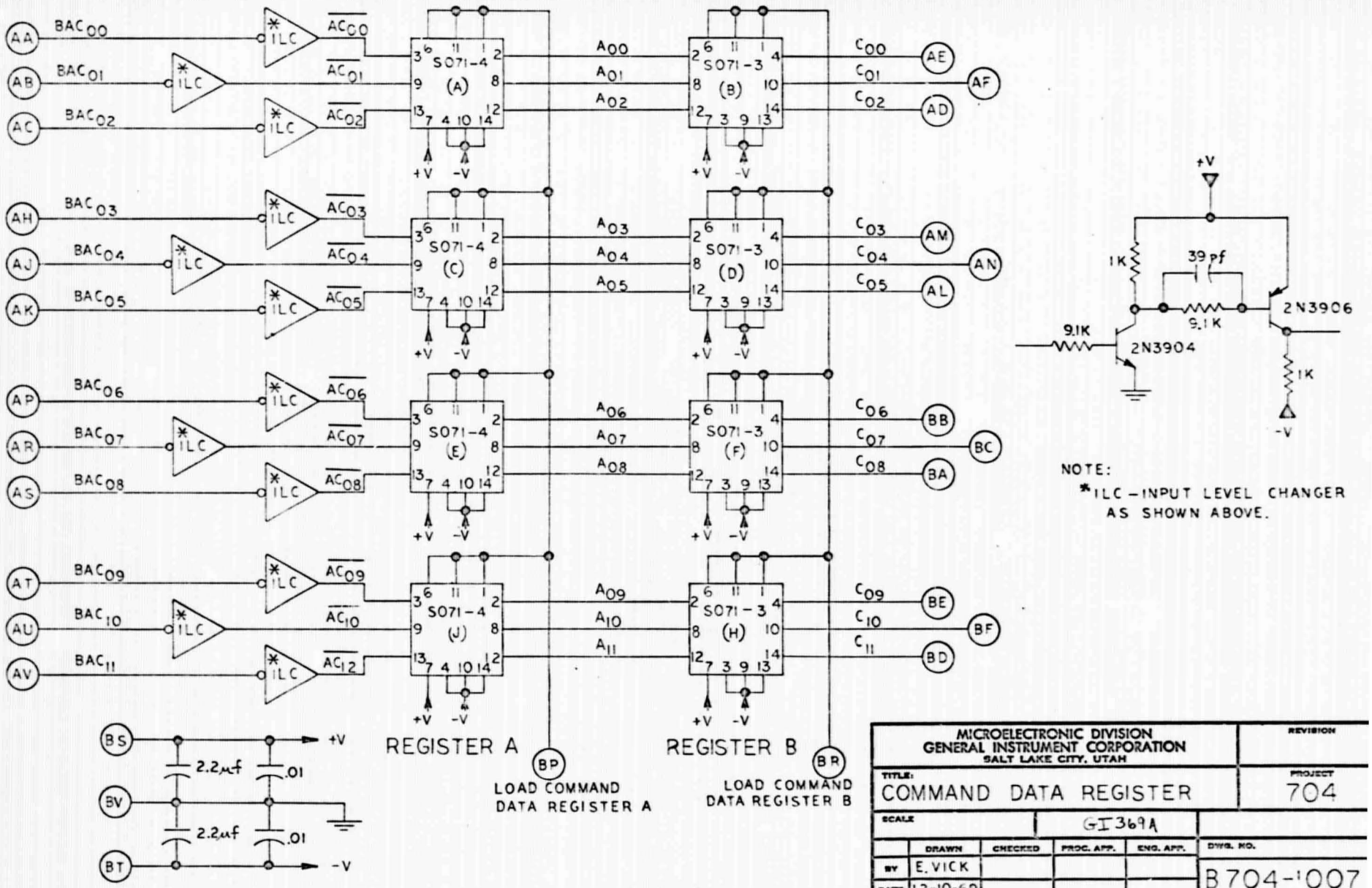
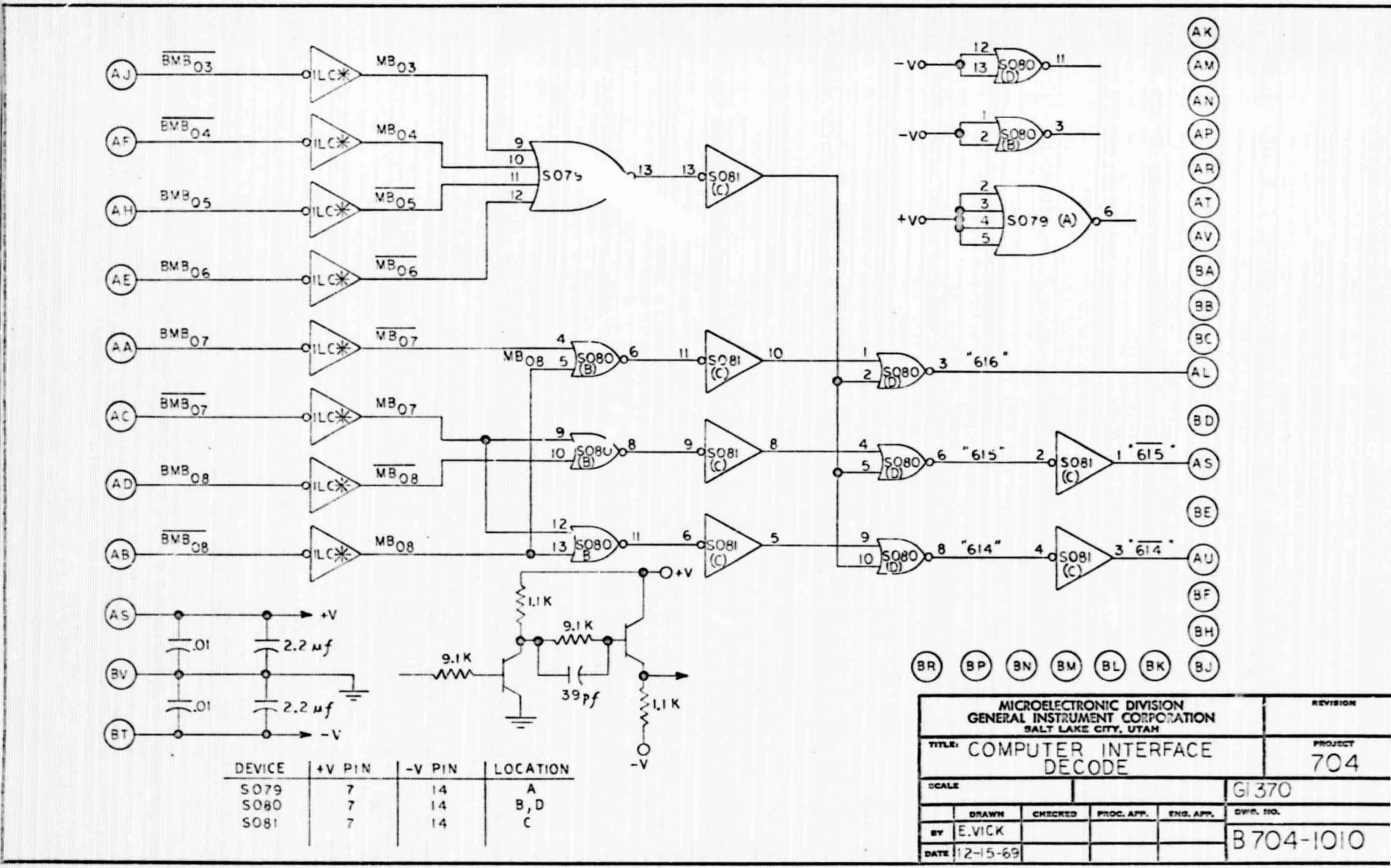

AA
AB
AC
AH
AJ
AK
AP
AR
AS
AT
AU
AV
BAC00
BAC01
BAC02
BAC03
BAC04
BAC05
BAC06
BAC07
BAC08
BAC09
BAC10
BAC11
*ILC
AC00
AC01
AC02
AC03
AC04
AC05
AC06
AC07
AC08
AC09
AC10
AC12
SO71-4
(A)
(C)
(E)
(J)
SO71-3
(B)
(D)
(F)
(H)
+V
-V
A00
A01
A02
A03
A04
A05
A06
A07
A08
A09
A10
A11
C00
C01
C02
C03
C04
C05
C06
C07
C08
C09
C10
C11
AE
AF
AD
AM
AN
AL
BB
BC
BA
BE
BF
BD
BS
BV
BT
2.2μf
.01
REGISTER A
REGISTER B
BP
BR
LOAD COMMAND DATA REGISTER A
LOAD COMMAND DATA REGISTER B
1K
39 pf
9.1K
2N3906
2N3904
NOTE:
*ILC - INPUT LEVEL CHANGER AS SHOWN ABOVE.
MICROELECTRONIC DIVISION
GENERAL INSTRUMENT CORPORATION
SALT LAKE CITY, UTAH
REVISION
TITLE:
COMMAND DATA REGISTER
PROJECT
704
SCALE
GI369A
DRAWN
CHECKED
PROC. APP.
ENG. APP.
DWG. NO.
BY
E. VICK
DATE
12-10-69
B704-1007

Figure 16



DEVICE	+V PIN	-V PIN	LOCATION
S079	7	14	A
S080	7	14	B, D
S081	7	14	C

MICROELECTRONIC DIVISION
GENERAL INSTRUMENT CORPORATION
SALT LAKE CITY, UTAH

REVISION

TITLE: COMPUTER INTERFACE DECODE

PROJECT 704

SCALE

GI 370

	DRAWN	CHECKED	PROC. APP.	ENG. APP.
BY	E.VICK			
DATE	12-15-69			

DWG. NO. B 704-1010

Figure 17

	0	1	2	3	4	5	6	7	8	9	10	11
Command (Output) Word	Spare	MSB	Module Address					LSB	MSB	MUX * Address		LSB
Response Data Word (Input)	Word ID "0"	Com. Data Bad	Resp. Parity Fail.	SIGN	MSB	A/D Data						LSB
Response Status Word (Input)	Word ID "1"	Com. Data Bad	Resp. Parity Fail.	Mul. Resp.	Res. Clock Error	No Sync	Spare					

Word Format

NOTES: *The MUX address is decoded by the module as follows:

MSB			LSB	
0	0	0	0	Zero Cal- (High level)
0	0	0	1	Analog Channel #1
0	0	1	0	Analog Channel #2
0	0	1	1	Analog Channel #3
0	1	0	0	Analog Channel #4
0	1	0	1	Analog Channel #5
0	1	1	0	Analog Channel #6
0	1	1	1	Analog Channel #7
1	0	0	0	Analog Channel #8
1	0	0	1	Operate-(Low Level - Particular Module)
1	0	1	0	Full Scale Cal-Low Level
1	0	1	1	Zero Cal-Low Level
1	1	0	0	Operate Low Level-All Modules
1	1	0	1	Turn on
1	1	1	0	Turn off
1	1	1	1	Full Scale Cal (High Level)

SYSTEM CONTROLLER PROGRAM INSTRUCTIONS (PDP-8L)

Input Response Data (IRD)

Octal Code: 6146
(Output Response Data)

Read Command Data (RCD)

Octal Code: 6154
(Load Command Data)

Skip on Response Flag (SRF)

Octal Code: 6141
S.C. generates skip signal if response data is ready

Skip on Command Flag (SCF)

Octal Code: 6151
S.C. generates skip signal if command data is required

Go to Wait Mode (GWM)

Octal Code: 6164
S.C. stops interrupting computer

Go to Operate Mode (GOM)

Octal Code: 6162
S.C. starts requesting input and output word transfers

Initialize (GIZ)

Octal Code: 6161
S.C. initializes all logic. Note that it can be combined with 6162 and 6154.

MICROELECTRONIC DIVISION GENERAL INSTRUMENT CORPORATION SALT LAKE CITY, UTAH					REVISION
TITLE: NASA System Controller PDP-8L Word Format and Program Instructions					PROJECT 704
SCALE					
	DRAWN	CHECKED	PROC. APP.	ENG. APP.	DWG. NO.
BY	J Fowler				B704-6009
DATE	1/13/69				

Figure 18

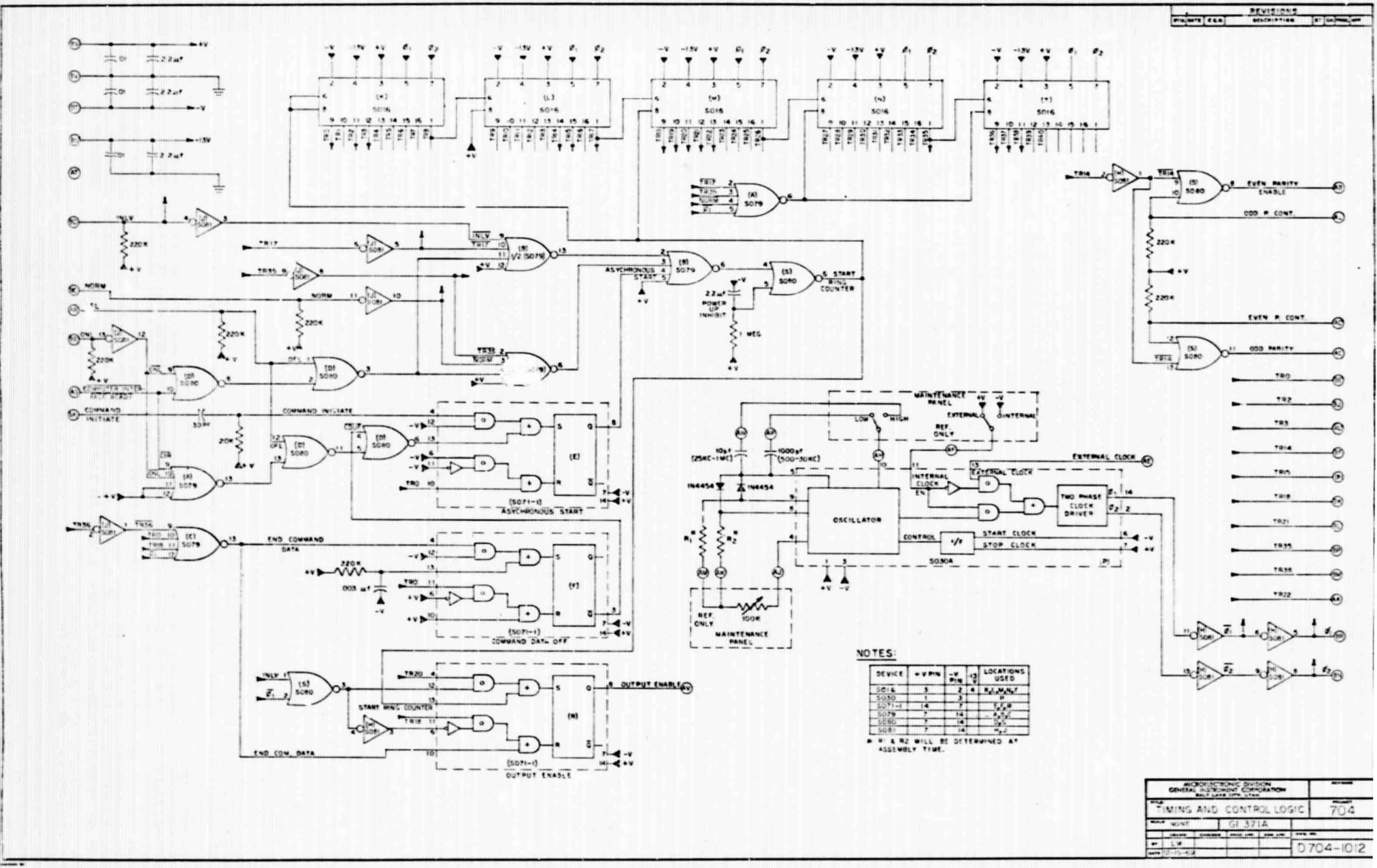
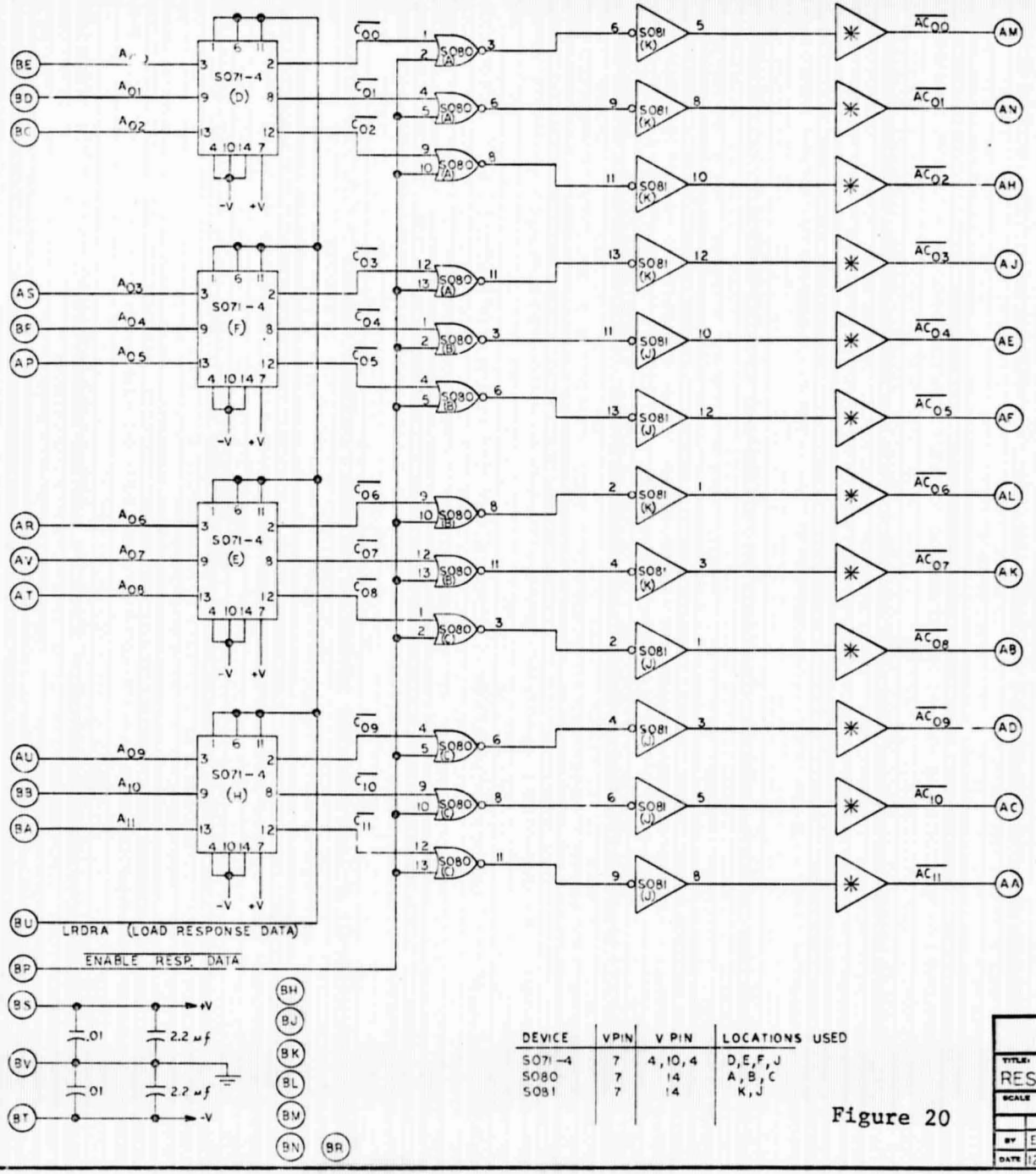
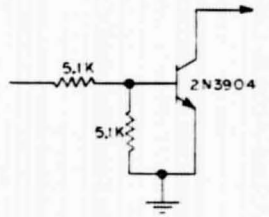

REVISIONS
NOTES:
DEVICE
+V PIN
-V PIN
+3 V
LOCATIONS USED
SO16
SO30
SO71-1
SO79
SO80
SO81
R1 & R2 WILL BE DETERMINED AT ASSEMBLY TIME.
MICROELECTRONIC DIVISION
GENERAL INSTRUMENT CORPORATION
TIMING AND CONTROL LOGIC
704
GI 371A
D704-1012

Figure 19



NOTE:

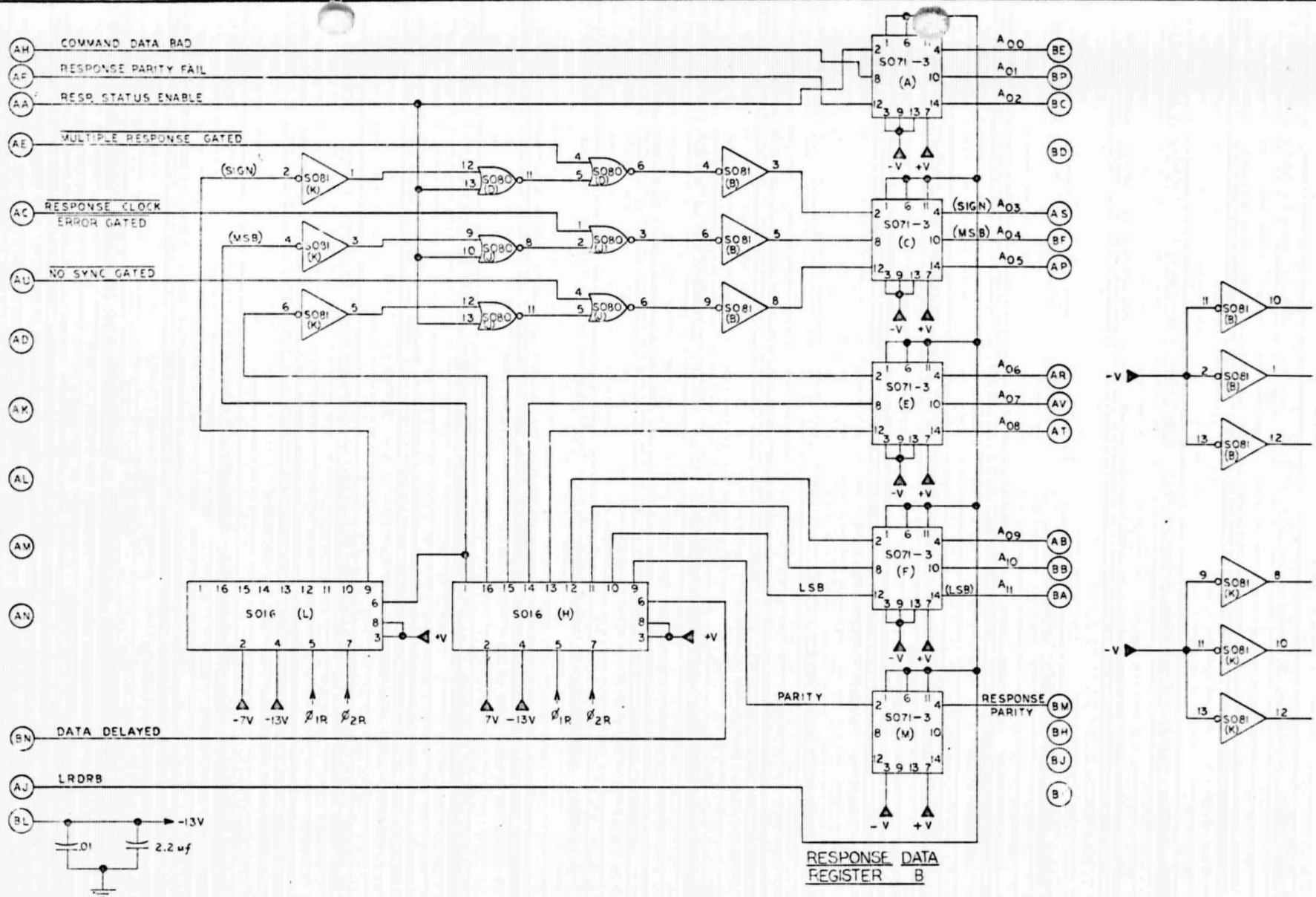
✳ OLC = OUTPUT LEVEL CHANGER



DEVICE	VPIN	V PIN	LOCATIONS USED
S071-4	7	4,10,4	D,E,F,J
S080	7	14	A,B,C
S081	7	14	K,J

Figure 20

MICROELECTRONIC DIVISION GENERAL INSTRUMENT CORPORATION SALT LAKE CITY, UTAH					REVISION
TITLE: RESPONSE DATA REGISTER A					PROJECT 704
SCALE					GI 372
	DRAWN	CHECKED	PROC. APP.	ENG. APP.	DWG. NO.
BY	E. VICK				C704 1006
DATE	12-11-69				

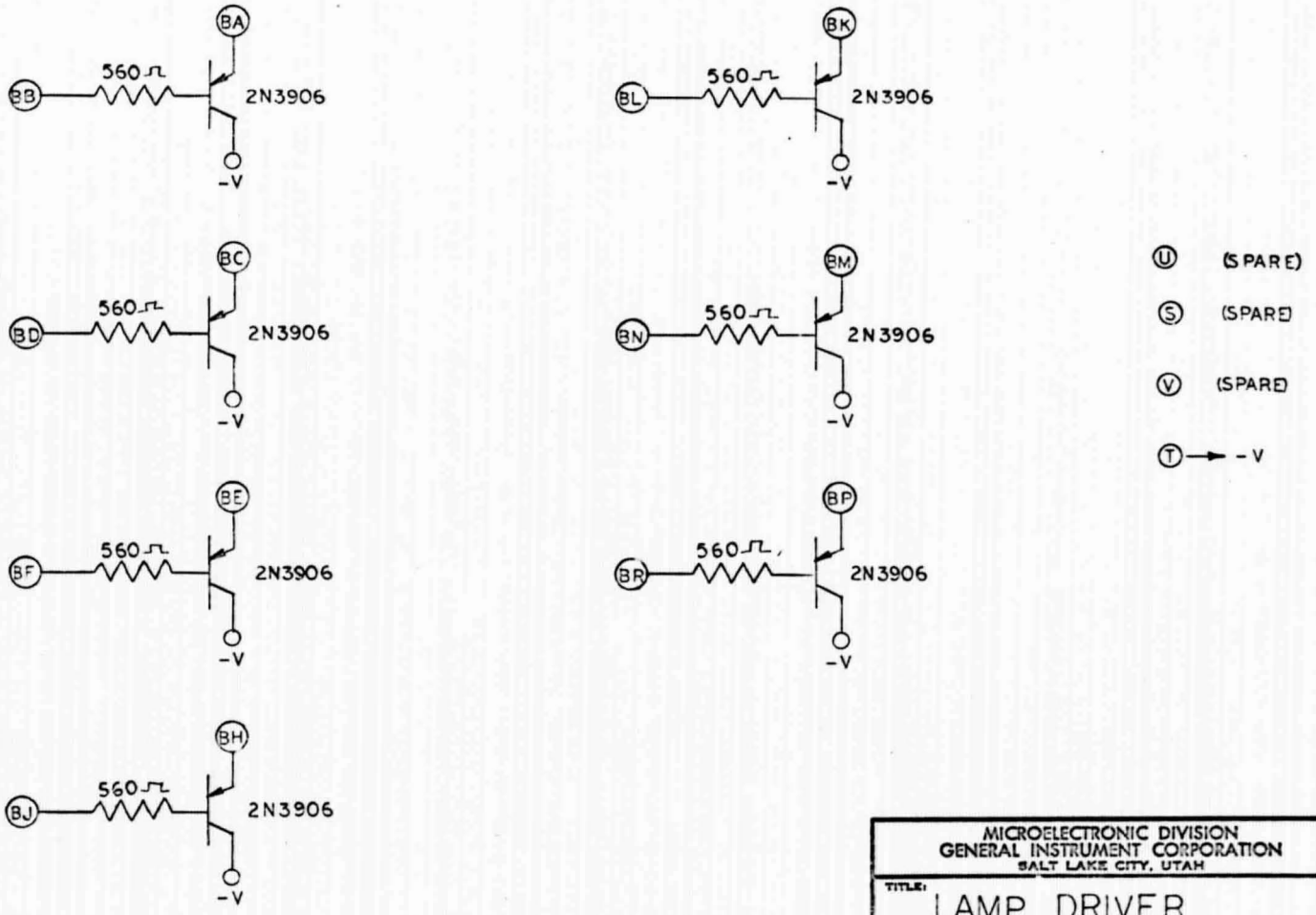


RESPONSE DATA REGISTER B

DEVICE	-13V PIN	+V PIN	-V PIN	LOCATIONS USED
SO16	4	3	2	H, L
SO80	—	7	14	D, J
SO81	—	7	14	B, K
SO71-3	—	7	3,9,13	A, C, E, F, M

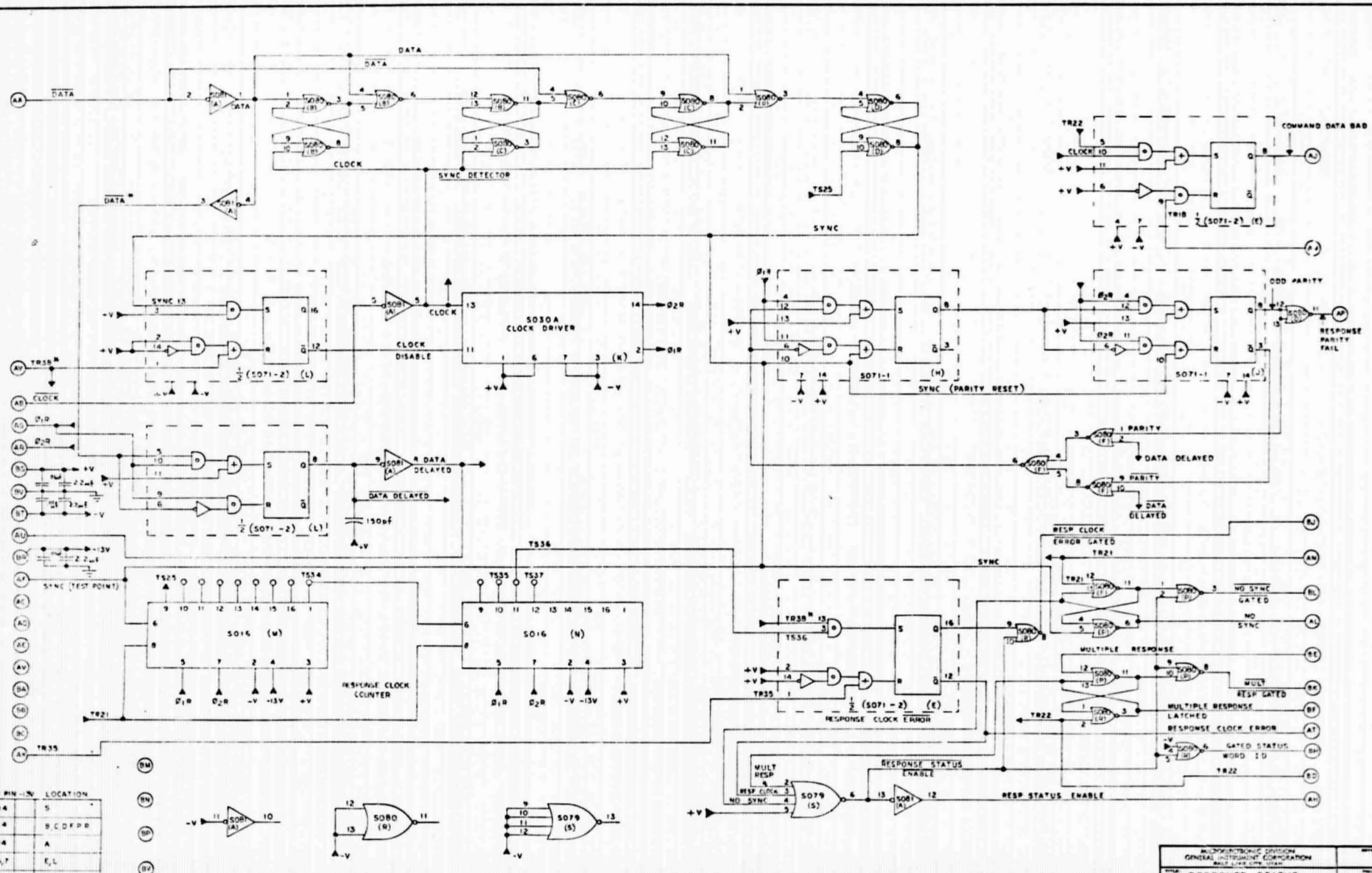
Figure 21

MICROELECTRONIC DIVISION GENERAL INSTRUMENT CORPORATION SALT LAKE CITY, UTAH				REVISION
TITLE: REPONSE DATA REGISTER B				PROJECT 704
SCALE				GI 373 A
	DRAWN	CHECKED	PROG. APP.	ENG. APP.	DWG. NO.
BY	E VICK				C 704-1008
DATE	12-12-69				



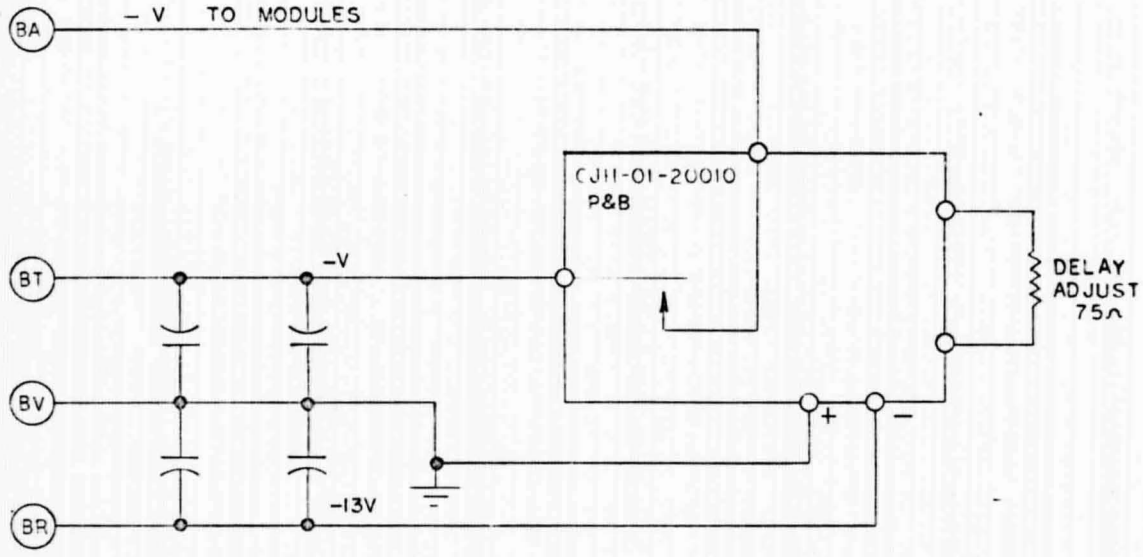
MICROELECTRONIC DIVISION GENERAL INSTRUMENT CORPORATION SALT LAKE CITY, UTAH					REVISION
TITLE: LAMP DRIVER					PROJECT NASA
SCALE		GI 374			
	DRAWN	CHECKED	PROG. APP.	ENG. APP.	DWG. NO.
BY	S.WEST				B704-2058
DATE	9/11/69				

Figure 22



DEVICE	+V PIN	-V PIN	-13V	LOCATION
S079	7	14		S
S080	7	14		B,C,D,F,P,R
S081	7	14		A
S071-2	4	15,7		E,L
S071-1	14	7		J,H
S016	3	2	4	M,N
S030A	1,6	7,3		K

MICROELECTRONICS DIVISION GENERAL INSTRUMENT CORPORATION	
RESPONSE STATUS	704
	GI 375A
	D704-10



MICROELECTRONIC DIVISION GENERAL INSTRUMENT CORPORATION SALT LAKE CITY, UTAH					REVISION
TITLE: POWER RELAY					PROJECT 704
SCALE					GI 376
	DRAWN	CHECKED	PROC. APP.	ENG. APP.	DWG. NO.
BY	P. Vick				B 704-205
DATE	2-4-70				

Figure 24

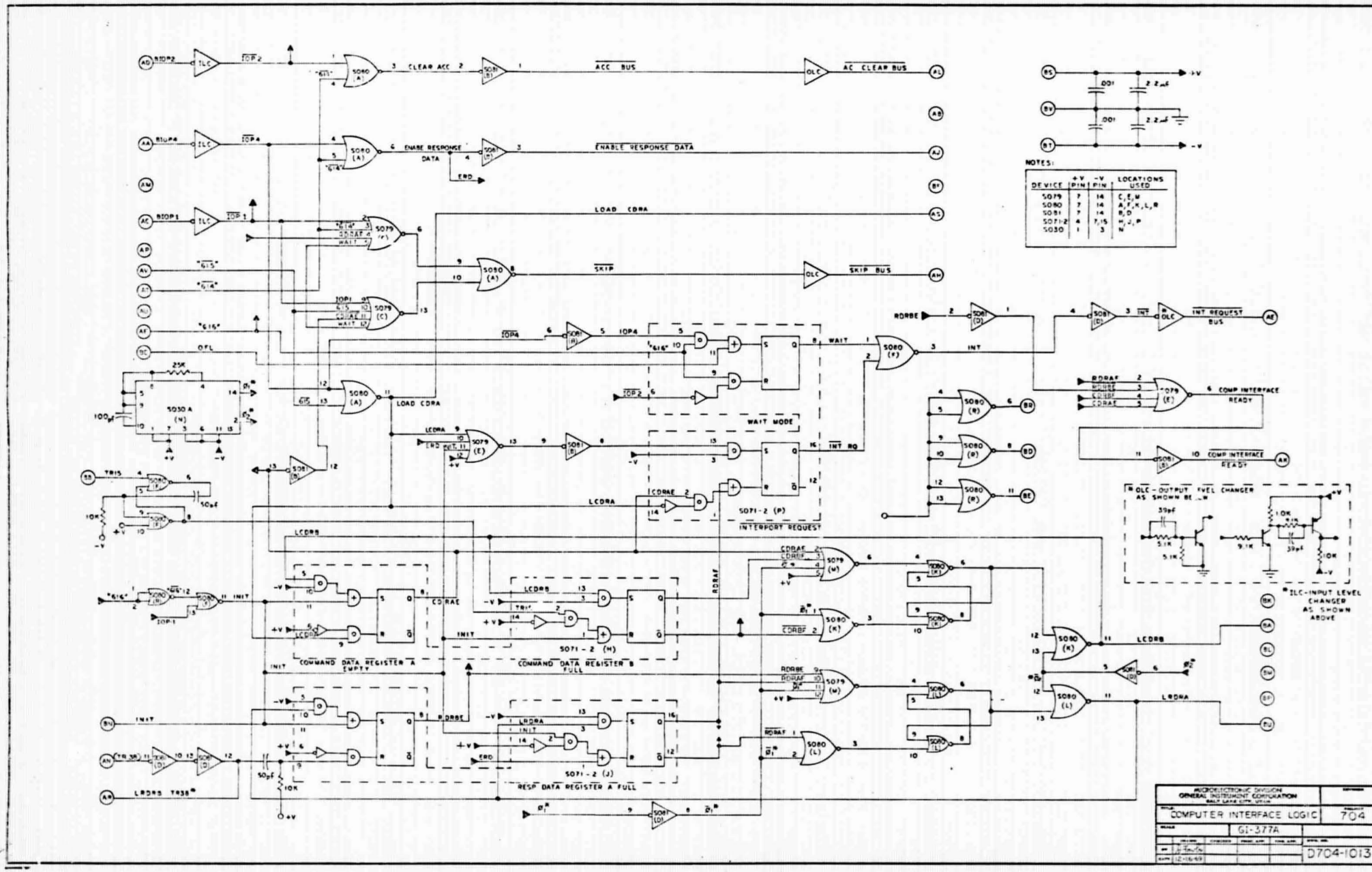
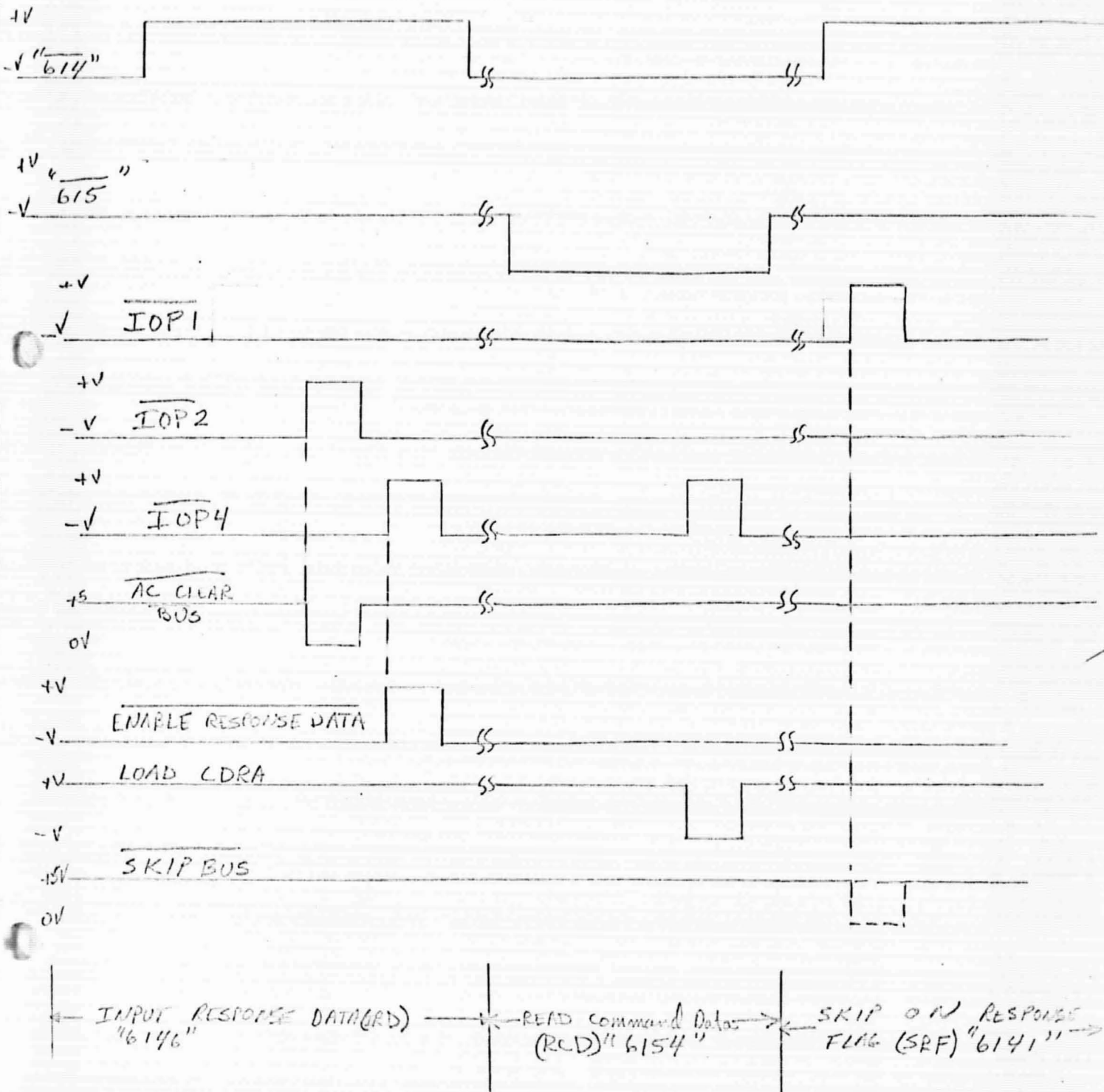

ACC BUS
AC CLEAR BUS
ENABLE RESPONSE DATA
LOAD CDRA
SKIP
SKIP BUS
WAIT MODE
INTERPORT REQUEST
INT REQUEST BUS
COMP INTERFACE READY
COMMAND DATA REGISTER A EMPTY
COMMAND DATA REGISTER B FULL
RESP DATA REGISTER A FULL
NOTES:
COMPUTER INTERFACE LOGIC
704
GI-377A
D704-1013

Figure 25



NOTE: SEE PDP-8L USER'S MANUAL PAGE 11 FOR EXACT TIMING

FIGURE 26 — COMPUTER INTERFACE TIMING DIAGRAM