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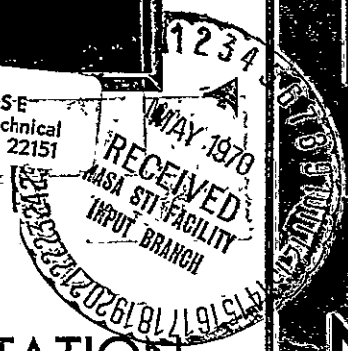

ENGINEERING EXPERIMENT STATION

AUBURN UNIVERSITY

AUBURN, ALABAMA

CR-102746

DESIGN AND CONSTRUCTION OF A PULSE-WIDTH-MODULATED SIGNAL GENERATOR

PREPARED BY

AMPLIFYING SYSTEMS LABORATORY

ANNUAL REPORT
(Part I)
March 20, 1970

CONTRACT NAS8-11344
GEROGE C. MARSHALL SPACE FLIGHT CENTER
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
HUNTSVILLE, ALABAMA

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FOREWORD

This report is a technical summary reporting the results of a study conducted by the Amplifying Systems Laboratory of the Electrical Engineering Department, Auburn University, under the auspices of the Engineering Experiment Station. The report is submitted in partial fulfillment of the requirements in NASA Contract No. NAS8-11344.

DESIGN AND CONSTRUCTION OF A PULSE-WIDTH-MODULATED SIGNAL GENERATOR

M. A. Honnell, R. O. Pettus and J. L. Tibbits, Jr.

ABSTRACT

The programmable pulse-width modulated signal generator described was designed and constructed to serve as a versatile source of various types of pulse-width-modulated signals. Typical signals generated are unipolar and bipolar PWM signals with single-edge, or double-edge, modulation. This signal generator can be used as a driver for the development of PWM power amplifiers, or as a source of PWM signals for studies of their spectral content and of filter requirements for low-distortion signal recovery.

The basic characteristics of unipolar and bipolar PWM amplifiers and signals are discussed. The design of the circuit modules utilized in the signal generator is presented. All of the modules are built on plug-in circuit boards.

The signal generator incorporates an active low-pass filter with a Butterworth characteristic having a roll-off of 6, 12 or 18 db per octave. The cut-off frequency is variable from 1 kHz to 50 kHz. The triangular carrier signal frequency is variable from 10 kHz to 1 MHz and can be modulated with input signals from DC to 50 kHz.

The system is conveniently arranged for the application of negative feedback to assist in stability studies and to study the effect of negative feedback on signal distortion and on carrier ripple. The unfiltered carrier output signal can supply 200 mA to a 50-ohm load which is sufficient to drive high-power switching-mode output amplifier stages.

A complete circuit diagram and a parts list are included. Photographs of typical signals generated are presented.

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I. INTRODUCTION

At present, pulse-width-modulated (PWM) amplification systems are utilized in many applications where high efficiency is essential. In order to design and improve PWM amplifiers many parameters and subsystems must be optimized and tested. A rigorous mathematical analysis of PWM systems is very complicated [1]. For this reason a purely mathematical approach to optimization is tedious. Hence a tool is needed to aid the designer in his work. The programmable pulse-width-modulated amplifier system described here was developed to serve as a versatile pulse-width-modulated amplifier suitable for making studies on PWM systems, for use as a signal generator, and for spectral analyses of PWM signals.

In general, a PWM amplifier operates with either single-edge or double-edge modulation. In both of these cases the amplitude of a square pulse is kept constant while the width is varied in accordance with the amplitude of the input signal. This permits the amplifier stages to be operated from cut-off to saturation yielding high efficiency.

II. GENERAL DESCRIPTION

The programmable pulse-width modulated amplifier described here generates the two types of output signals illustrated in Figure 1. To avoid confusion, the circuitry needed to generate these waveforms is classified as Type A and Type B as labeled in Figure 1.

A. Type A PWM System

A block diagram for a basic Type A PWM system is shown in Figure 2 [2].

The input signal is first linearly amplified (or attenuated) in the input amplifier to obtain the required level for optimum modulation. The signal is then summed with the triangular carrier signal in the resistive adder, R_1 and R_2. The resultant sum, e_1, is applied to the comparator. Since the comparator is referenced to ground, in the absence of an input signal E_{in}, the comparator toggles at the carrier frequency. The signal at the unfiltered output is a square wave. A signal applied at the input appears at the comparator summed with the carrier signal as illustrated in Figure 3. The comparator output is positive when the sum signal, e_1, is positive and negative when e_1 is negative. The width of each pulse at the output of the comparator is therefore proportional to the amplitude of the input signal at that instant, as illustrated in Figure 3.

The signal information is recovered by filtering the output signal

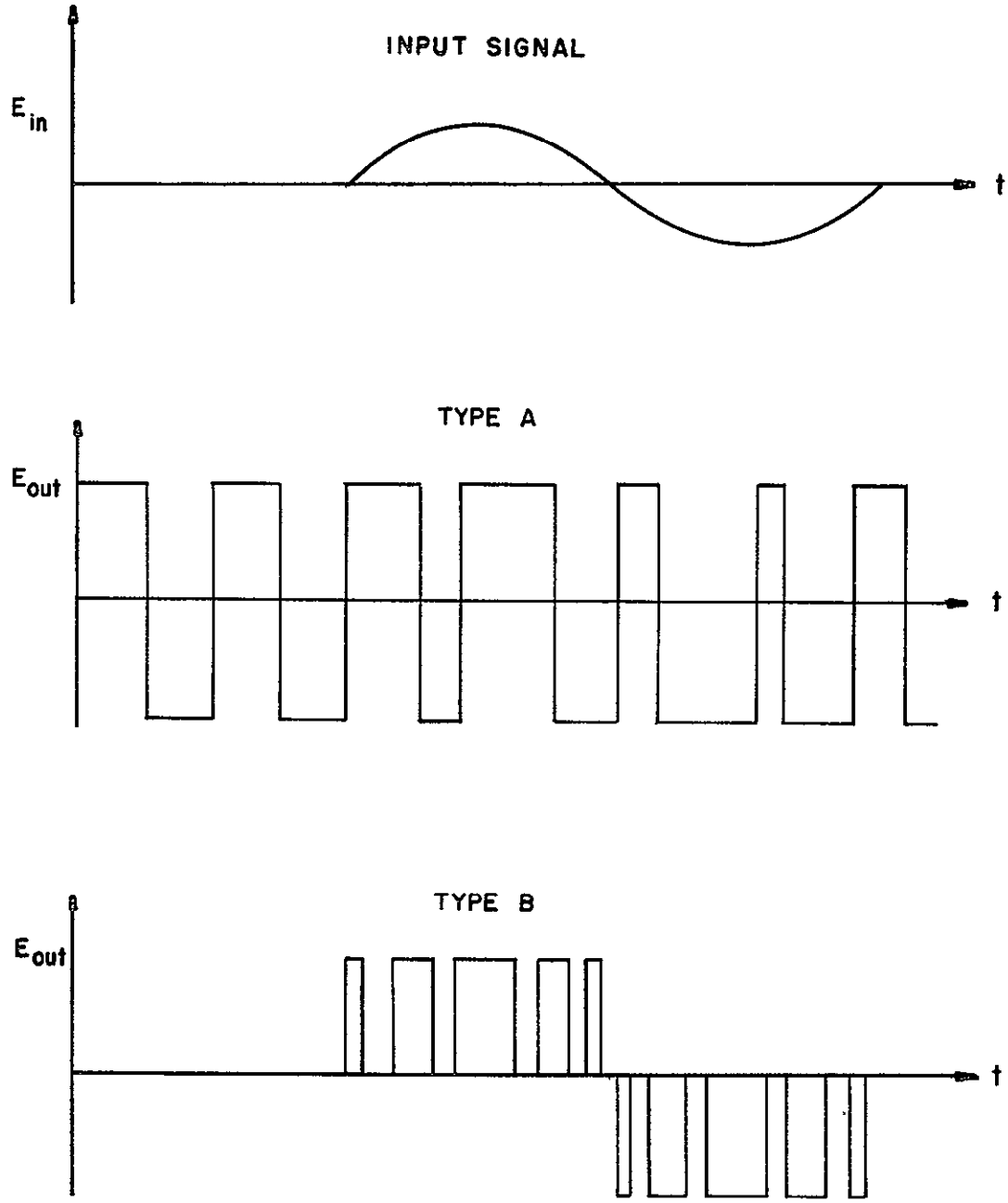


Figure 1. - Type A and Type B output waveforms.

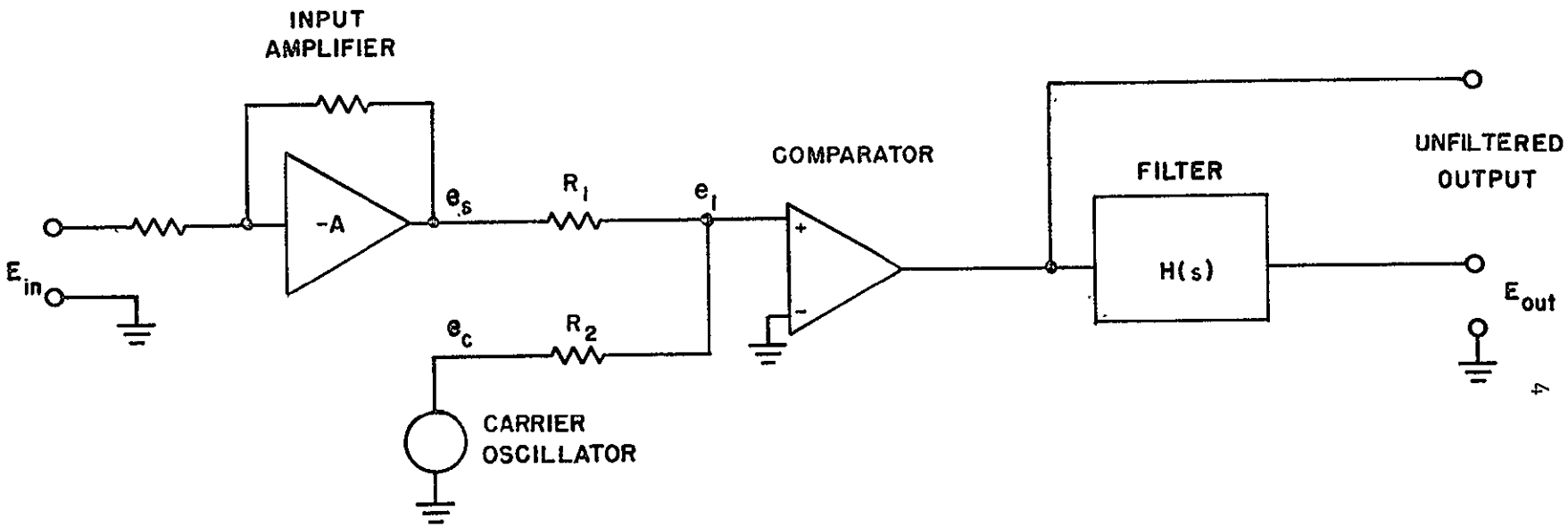


Figure 2. - Block diagram of Type A PWM system.

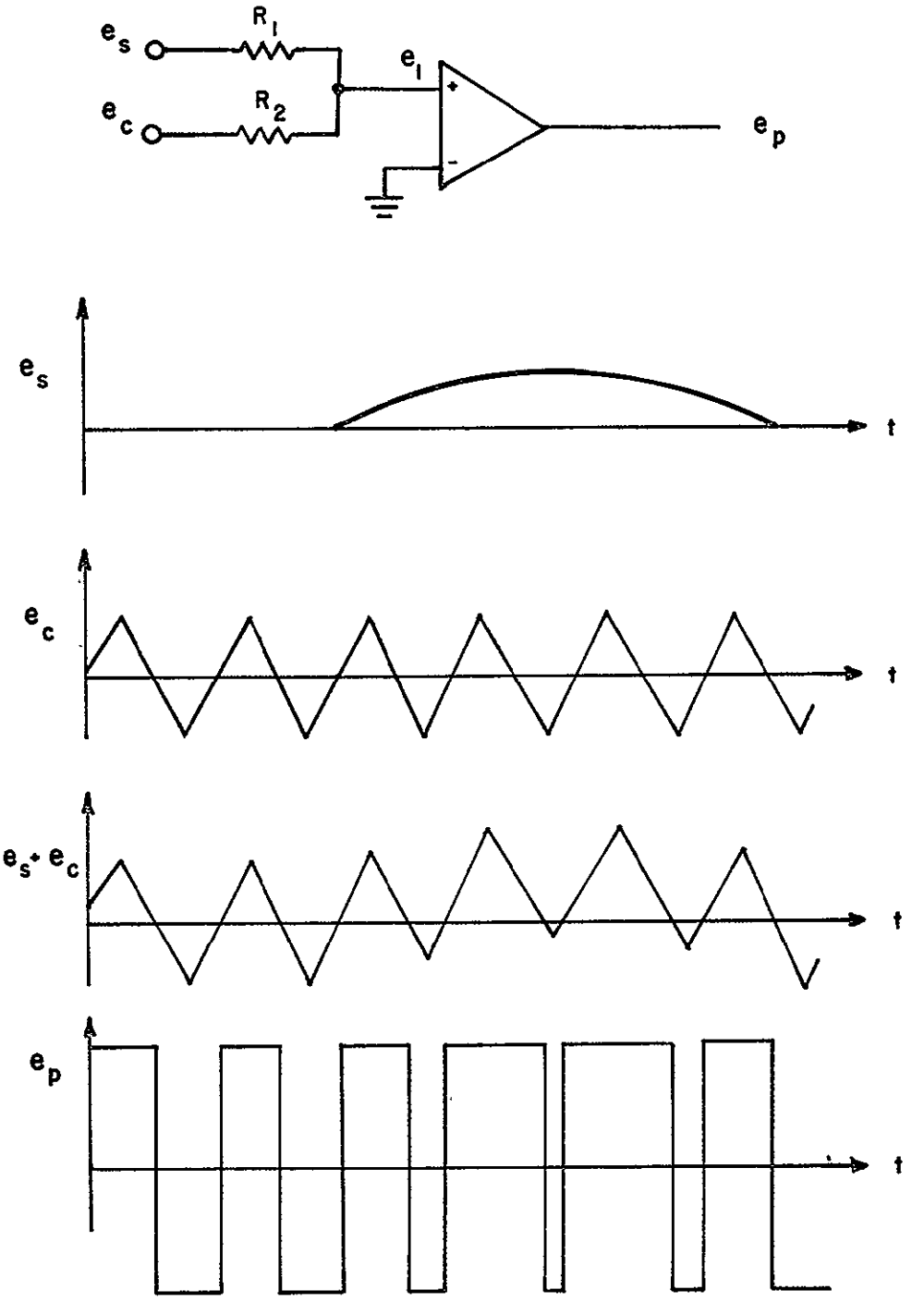


Figure 3. - Waveforms associated with Type A PWM system.

from the comparator. The undesired frequency components in the output may be minimized through the proper choice of carrier frequency and filter characteristics.

B. Type B PWM System

A block diagram for a basic Type B PWM amplifier is shown in Figure 4. The operation of this system is quite similar to that of the Type A system with the exception that two separate channels are employed. The P channel is modulated for positive input signals and the N channel is modulated for negative input signals. The signals from these two channels must be combined and filtered.

The comparator for the P-channel is referenced (biased) to the peak positive amplitude of the carrier signal. For zero input signal the P-comparator output remains constant since the voltage at its positive input never exceeds the reference potential biasing its negative input.

When the applied input signal goes positive, it appears summed with the carrier signal at the positive input of the P-comparator. Whenever this sum is more positive than the reference level, the comparator switches to an "on" state. The resultant output of the P-comparator is a train of pulses as shown in Figure 5. The width of each pulse is proportional to the amplitude of the input signal at that instant. If the applied input signal goes negative it subtracts from the carrier signal and, hence, the signal at the positive input of the P-channel comparator never exceeds the reference voltage. Therefore the comparator output remains constant.

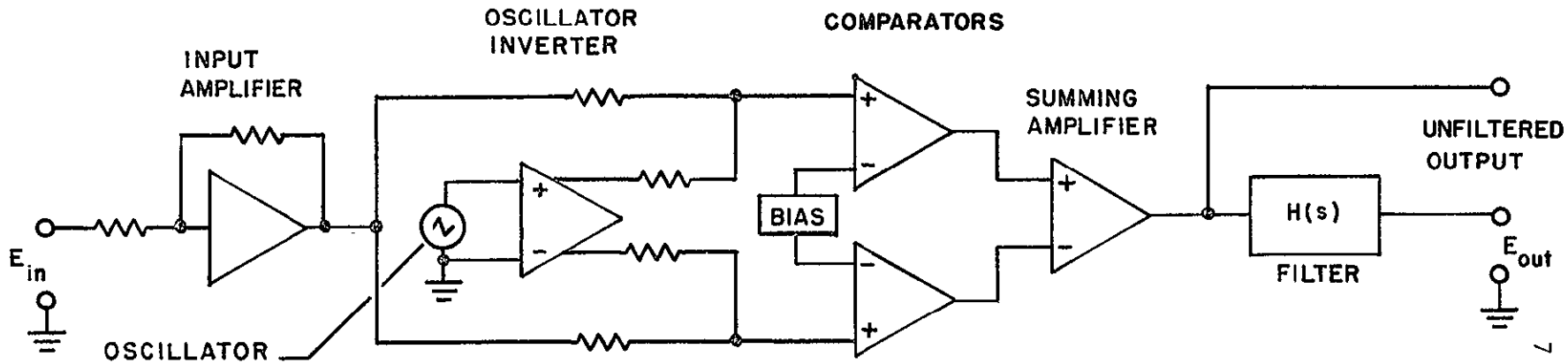


Figure 4. - Block diagram of Type B PWM system.

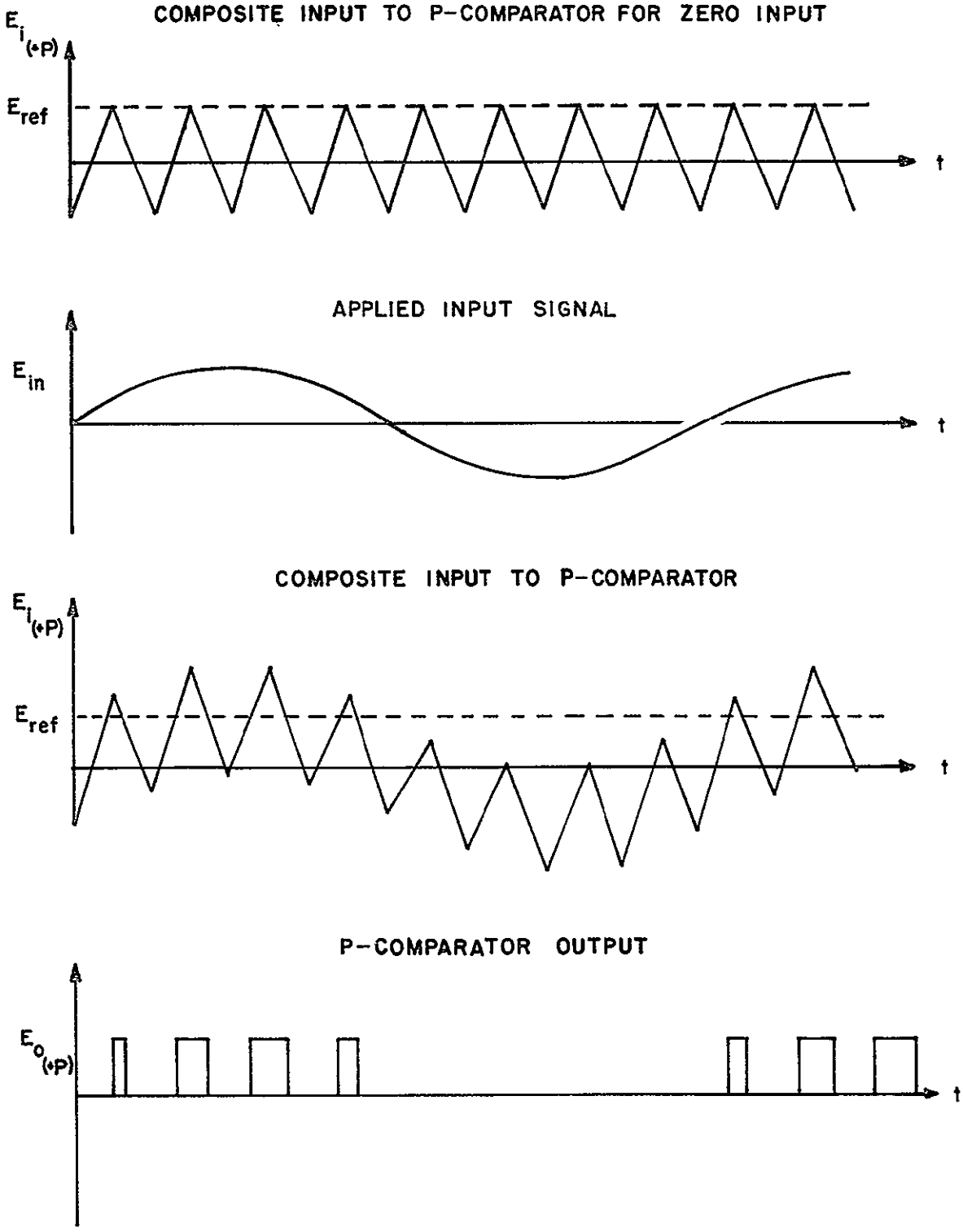


Figure 5. - Waveforms associated with Type B PWM system.

The N-channel comparator is referenced to the negative peak amplitude of the carrier signal. It performs a complementary operation to the P-channel.

The signals from the two comparators are added in the summing amplifier and the resulting waveform is filtered with a low-pass filter to recover the desired signal components.

It is to be noted that when the carrier is a sawtooth wave, the output signal is single-edge modulated. On the other hand, if the carrier is a symmetrical triangular wave, such as a pyramid, the output wave is double-edge modulated.

III. DESIGN

In this chapter the actual designs of the various modules of the programmable pulse-width-modulated amplifier are presented. The performance required of the system dictates the performance required of each of the individual subsystems. For each of the subsystems the specifications are listed under the heading of Design Criteria.

Some fundamental design considerations which were taken into account in developing the individual circuits for the programmable PWM amplifier are discussed in Appendix A.

A. The Comparator

1. Design Criteria

1) High gain (less than 50 mv hysteresis)
2) High speed (less than 20 ns rise or fall time)
3) Low input bias current
4) $\pm$10 volt output across 50 Ω loads shunted by 100 pF.
5) Differential input
6) Large input differential and common-mode voltage range.
7) Saturating output

The comparator developed is shown in Figure 6. The performance met, or exceeded, all of the design criteria. A stage-by-stage discussion of the circuitry follows. Circuit values are listed in Appendix B.

2. The Output Stage

Using the minimum specifications given in the design criteria the minimum slew rate of the comparator may be calculated to be

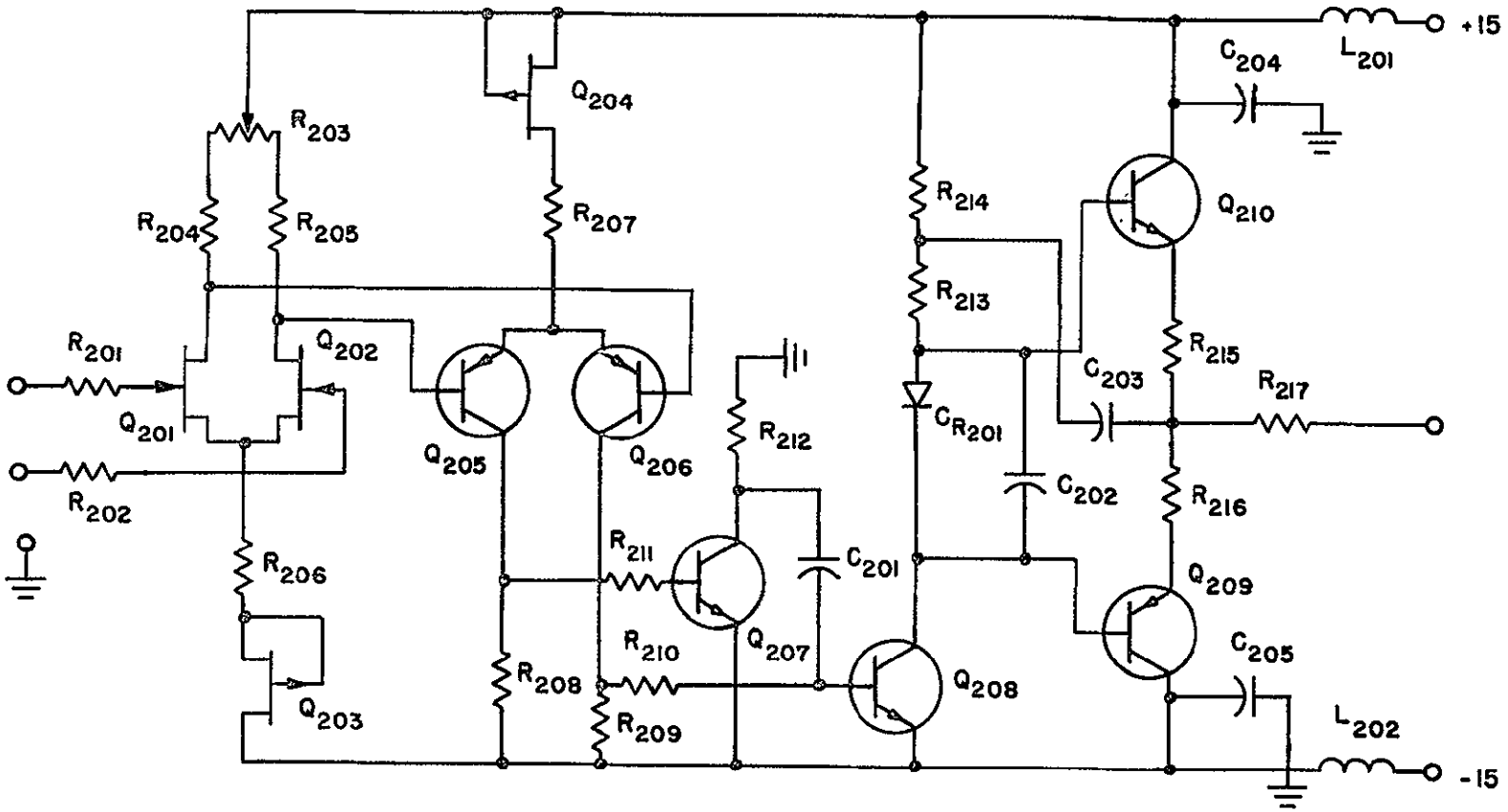


Figure 6. - Schematic diagram of comparator.

$$S_{min} = \frac{\Delta V}{\Delta T} = \frac{20v}{20ns} = 10^3 \frac{v}{\mu s} \quad (1)$$

Because of the high value of dv/dt at the output, the output stage must be able to deliver relatively high currents of either polarity. The minimum slew rate produces a current of 100 mA in a 100 pF capacitor. When the 200 mA of resistive current is added, the comparator must be able to supply at least $\pm$300 mA. This figure is well within the ratings of the 2N2219/2N2905 series of complementary transistors employed. A push-pull configuration is used to provide balanced output impedances. Emitter resistors, R_{215} and R_{216}, protect against thermal runaway and provide short-circuit protection. The bias diode, CR_{201}, is a dual diode designed specifically for complementary biasing applications. The delay time was reduced by maintaining a non-zero quiescent collector current in the output transistors.

3. The Driver Stage

The driver stage is a common-emitter amplifier. This configuration is employed for several reasons:

1) This configuration gives high voltage and power gain.
2) It is possible to drive both of the output transistors into "soft" saturation.
3) When used in conjunction with the differential input stages, satisfactory operation is obtained over a wide range of supply voltages.

A value of 390 ohms was chosen for collector load resistors, R_{213} and R_{214}. This was an optimum compromise, giving a good value for the active-region time constant, τ_A (see Appendix A), while keeping the

collector current of Q_{208} in a favorable region. Q_{208}, a 2N3227 transistor, determines the switching time of the comparator because most of the voltage swing is developed here. A low value of τ_s is necessary in order to drive this stage into hard saturation. The 2N3227 transistor satisfies both criteria. In addition, this transistor offers higher gain and voltage ratings than most other transistors of equivalent speed. The higher voltage rating is especially important because the required output voltage swing makes operation from $\pm$ 15-volt power supplies necessary. This means that the 2N3227 is operated beyond its voltage ratings. However, a number of samples of this transistor were checked and all were found to give satisfactory operation with supply voltages of $\pm$ 18 volts. If a more conservative rating is desired, other transistors or lower supply voltages could be used with a corresponding sacrifice in performance.

4. The Input Stage

To fulfill design criteria #5 and #6 a differential configuration is used for the input stage. High input impedance (low input bias current) is achieved through the use of field-effect transistors. A second differential stage proved to be necessary in order that sufficient drive be available for the class-A driver. The second differential pair acts as an impedance-matching device, thus allowing the input stage to operate with much higher gain.

The choice of FET's used in the first differential stage is discussed in Appendix A. A constant bias current of 6 mA for the sources

is obtained from the zero-gate-voltage drain current, I_{DSS}, of an FET, Q_{203}. This current must be slightly less than the I_{DSS} value of either Q_{201} or Q_{202}. This prevents the gate from becoming forward biased when the input signal goes positive. A balance potentiometer, R_{203}, alleviates the need for perfect matching of Q_{201} and Q_{202}. The quiescent voltage drop across the drain resistors, R_{201} and R_{202}, must be at least 5 volts to insure that the second stage current source, Q_{204}, will operate properly. The resistors, R_{201}, R_{202}, and R_{203} are employed to suppress parasitic oscillations.

5. The Second Stage

The second stage of the comparator is also composed of a differential pair, Q_{205} and Q_{206}. This circuit configuration yields low propagation delay and provides a convenient signal for the speed-up amplifier transistor, Q_{207}. A six decibel increase in gain is realized by utilizing the differential output available from the input differential stage. A 6-mA current source is used to bias transistors Q_{205} and Q_{206} at a favorable operating point with respect to β and f_t. The collector load resistors, R_{208} and R_{209}, bias the bases of the driver transistors, Q_{207} and Q_{208}, to approximately 0.7 volts with respect to their emitters.

6. The Speed-Up Amplifier

Because the second differential pair is unable to provide the overdrive to Q_{208} necessary for fastest switching, a speed-up amplifier is employed. The speed-up transistor, Q_{207}, is operated as a class-A amplifier which capacitively couples a large signal to the base of

transistor, Q_{208}, which is overdriven in order to reduce the switching times. The collector of Q_{207} is returned to ground to lower the V_{CEO} requirement. The collector resistor, R_{212}, yields a short active region time constant, τ_A (see Appendix A), yet limits the saturation current to a safe value.

B. The Oscillator

1. Design Criteria

1) Triangular and sawtooth output.
2) Repetition rate from 1 kHz to 1 mHz
3) Less than 1% non-linearity
4) Good short-term frequency and amplitude stability.

2. The Basic Oscillator

The basic circuit configuration for the oscillator is shown in Figure 7 [3]. The operation of the oscillator is as follows. The positive feedback supplied through R_1 and R_2 drives the comparator to saturation. If the comparator is in the positive state, the output is at $+V_o$. Then diode CR_1 is reverse-biased and the current flowing into the integrating capacitor, C is given by

$$I_c^+ = I_p - I_N = 2I - I = I \tag{2}$$

The capacitor is then charged by a constant positive current, giving a positive-going ramp at the output. When the capacitor voltage exceeds the voltage at the positive input, the comparator toggles. The voltage is designated V_T^+ and is given by

$$V_T^+ = + V_o \left(\frac{R_2}{R_1 + R_2}\right) \tag{3}$$

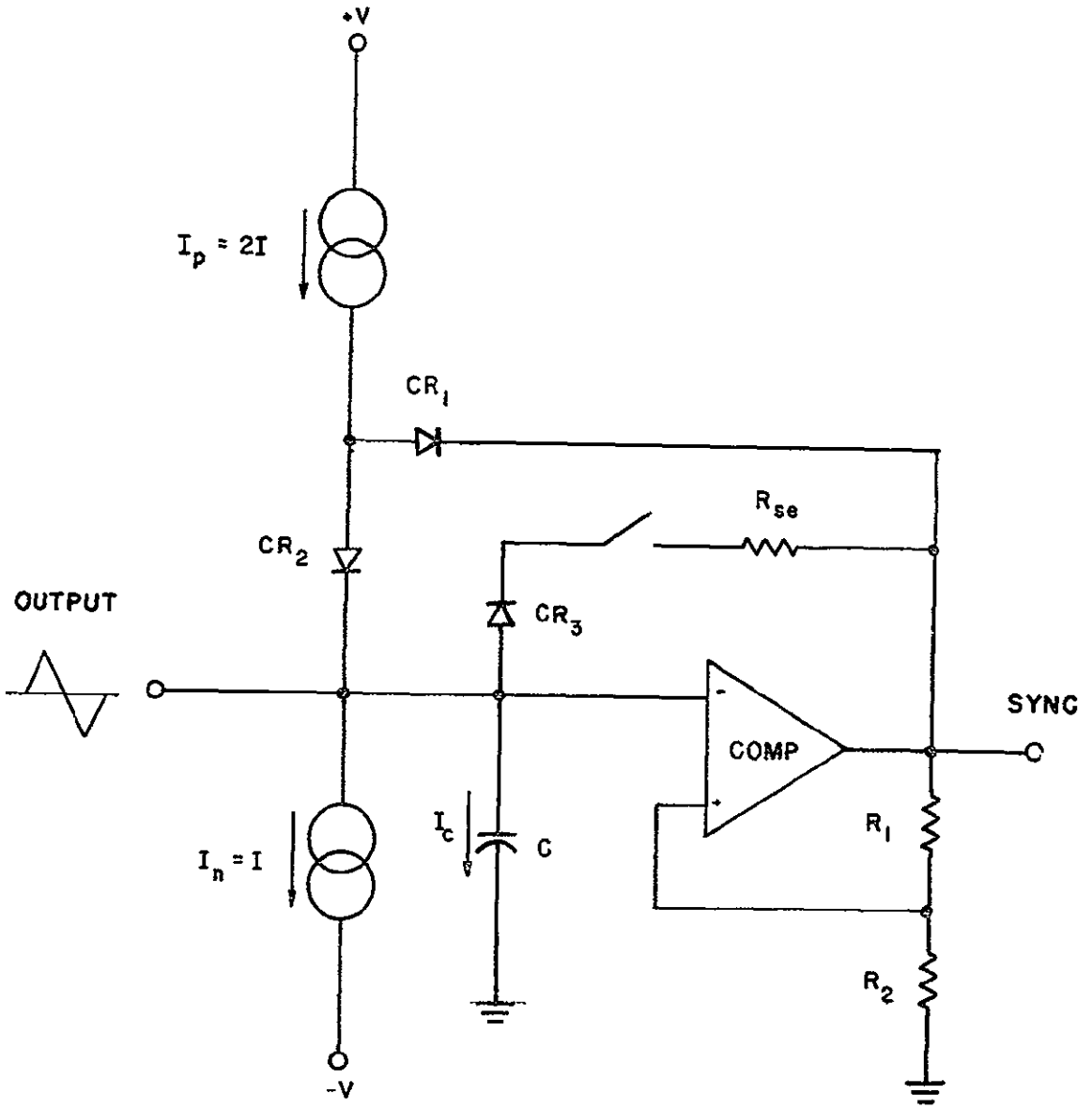


Figure 7. Basic circuit configuration of oscillator.

After the comparator toggles, diode, CR_1, becomes forward-biased and the comparator acts as a sink for I_p. Therefore, the negative current source discharges the integrating capacitor. Diode CR_2 isolates the negative current source and C during this interval. If $I_p = 2I_N$ as given, the positive and negative slopes will be of equal magnitudes, thus producing a symmetrical triangular output waveform. The equation for the negative toggle voltage, V_T^-, is of the same form as Eq. 3 and has the same magnitude as V_T^+ if the comparator has symmetrical saturation voltages. When these conditions are met, the period, T, is given by

$$T = \frac{4V_oCR2}{I(R_1 + R_2)} \tag{4}$$

The oscillator generates a sawtooth at the output if switch, S, is closed. When the comparator output goes negative, the comparator discharges the integrating capacitor through diode CR_3. Because of the low-impedance discharge path, the capacitor discharges in a small fraction of the period. When the comparator is in the positive state, CR_3 is reverse-biased and the output waveform is not affected. The period of the sawtooth generated is given by

$$T = \frac{2V_oCR_2}{I(R_1 + R_2)} \tag{5}$$

3. High-Frequency Operation

At high carrier frequencies (above 75 kHz) the amplitude of the

output waveform increases. This is caused by the delay time of the comparator and the switching time of CR_1. When the output voltage reaches the toggle voltage, there is a time lag before the current sources are gated. The output continues to advance during this time, thus increasing the amplitude.

In order to maintain a constant output amplitude, an automatic level control (ALC) is used as shown in Figure 8. The peak value of the output signal is sensed by the peak detector and summed with a reference voltage, V_{REF}. The resultant error signal, ε, is amplified and drives a voltage-dependent resistor which adjusts the toggle voltage of the comparator. The polarities are chosen to drive ε to zero. If sufficient loop gain is provided, good amplitude stability is achieved. Because the output is capacitively coupled to the peak detector, only the positive peak of the output waveform is sampled.

Using the ALC the equations for the period become

$$T = \frac{4C\ V_{REF}}{I} \tag{6}$$

for the symmetrical triangular wave and

$$T = \frac{2C\ V_{REF}}{I} \tag{7}$$

for the sawtooth wave. V_{REF} represents the reference voltage.

4. The Comparator

The circuit for the comparator used in the oscillator is shown in

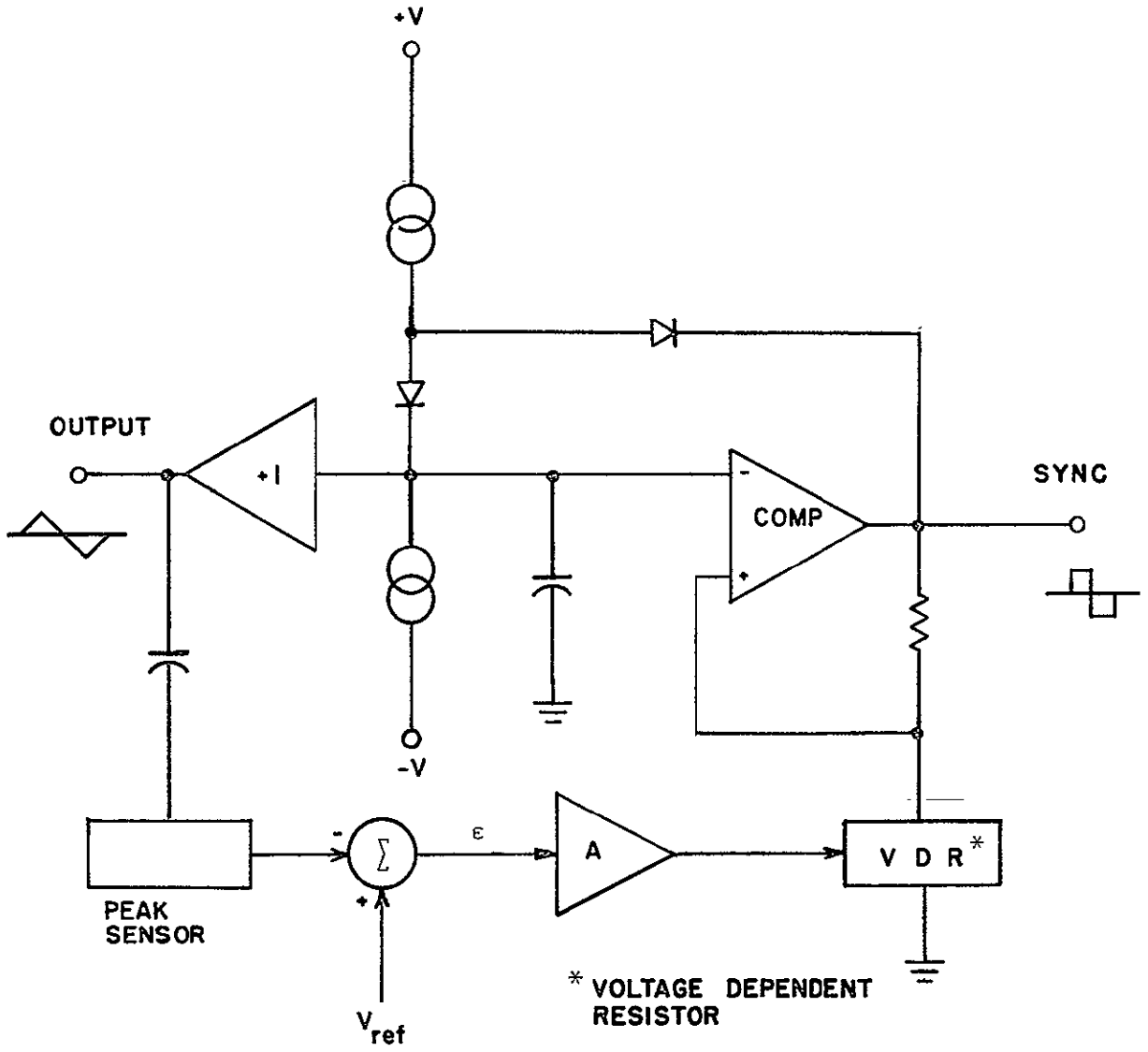


Figure 8. - Automatic level control block diagram.

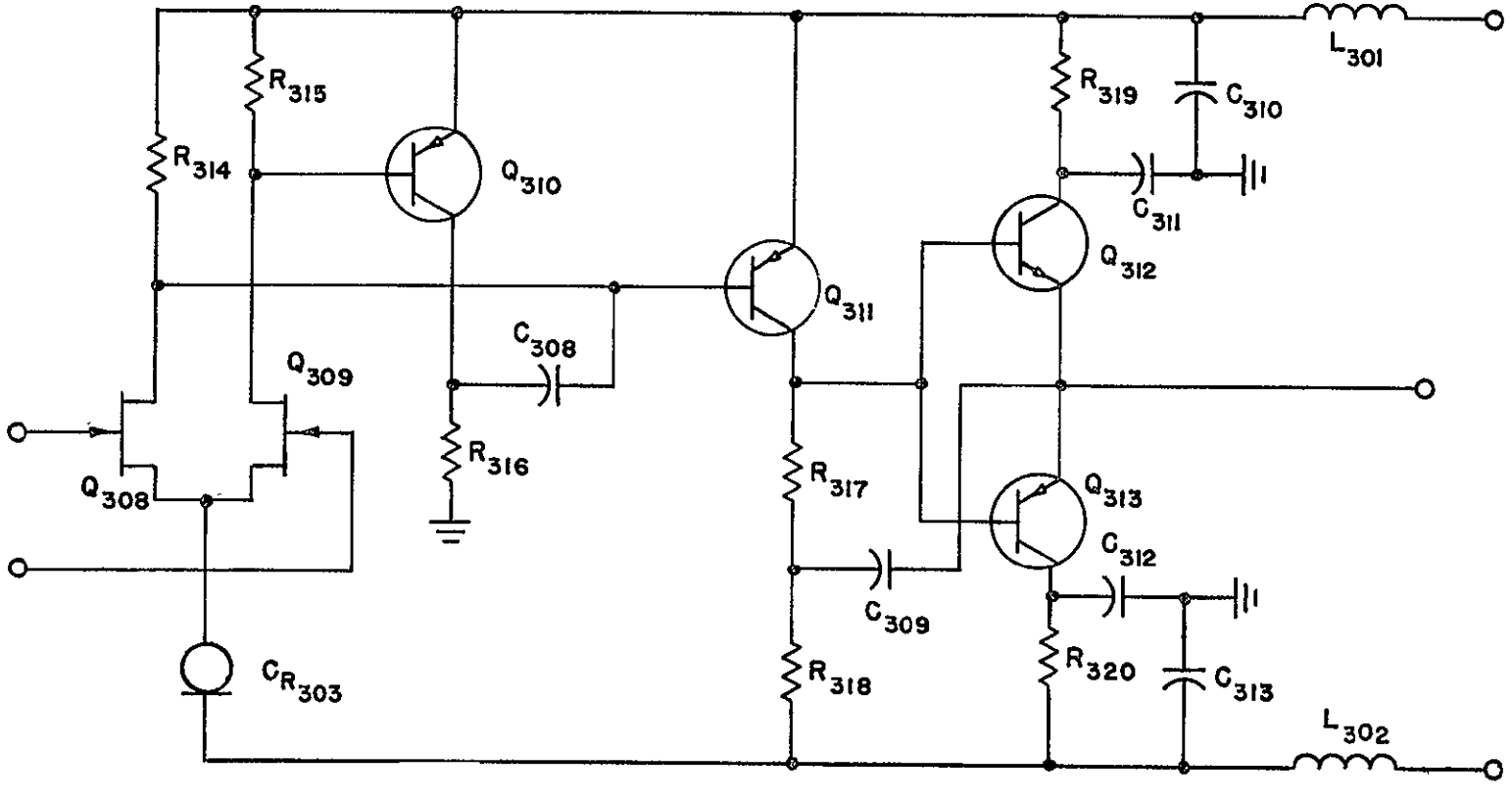


Figure 9. - Oscillator comparator schematic.

Figure 9. This circuit is similar to the comparator of Figure 6, with the exception that the second differential pair is eliminated. Therefore, the performance of these comparators is similar.

5. The Current Sources

High-impedance current sources are used to assure high-linearity waveforms. Variable repetition rates are provided by varying the magnitude of the currents with precise tracking controls, S_{301}, as shown in Figure 10.

Transistors, Q_{303} and Q_{304}, with their associated circuitry form the positive and negative current sources, respectively. Transistors, Q_{301} and Q_{302}, supply a constant current to the resistive divider, R_1 through R_{20}. Constant bias voltage increments for Q_{303} and Q_{304} are selected by S_{301} which serves as a frequency selector. Diodes, CR_{301} and CR_{302}, cancel the V_{BE} drops in the current source transistors. The current supplied by Q_{303} can be approximated as follows

$$I_p = \frac{20 - V_B}{R_{301}} \tag{8}$$

Similar calculations for Q_{304} are valid. The following criteria was used to determine the values for R_{301} and R_{302}.

A peak value of two volts for the triangular wave is used to assure compatibility with the peak detector used in the ALC circuitry. This leaves an 18-volt range for each of the current sources. A ten-volt maximum bias voltage for each of the current sources allows a minimum

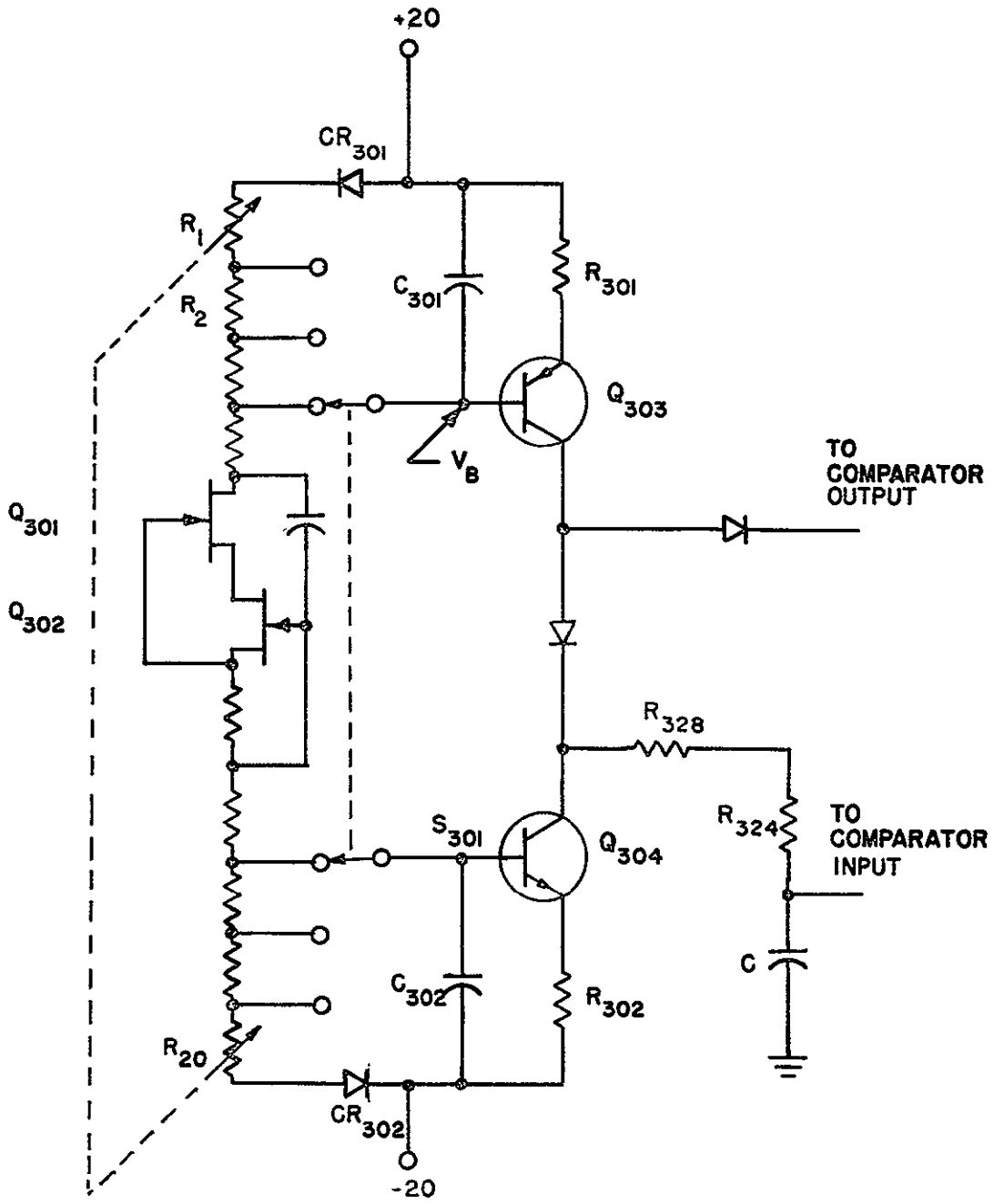


Figure 10. - Schematic diagram of current sources.

V_{CE} of 8 volts. The high bias voltages used provide linearity of control and good repeatability of frequency. The minimum V_{CE} of 8 volts is not critical but should be large enough to insure good linear operation of transistors, Q_{303} and Q_{304}. The maximum safe charging current determines the value of the integrating capacitor needed for operation at the highest frequency. The integrating capacitor should be much larger than the stray circuit capacitance. With equal bias voltages, the positive current source dissipates twice the power of the negative current source. To avoid dissipation problems, a maximum positive current of approximately 18 mA is used. R_{301} and R_{302} are calculated as follows

$$R_{301} = \frac{V_{CC} - 10}{I_P} \left(\frac{\beta}{\beta + 1}\right) = 0.55 \text{ k}\Omega \tag{9}$$

$$R_{302} = 2\, R_{301} = 1.10 \text{ k}\Omega \tag{10}$$

The bias current source utilizing FET's, Q_{301} and Q_{302}, is of standard design. Since the voltage across this current source remains essentially constant, the current available is limited to 15 mA by the dissipation capacity of the FET's. The ten milliamperes of bias current selected determined the value of the divide resistors, R_1 through R_{20} to be 100 Ω each.

The values of the integrating capacitors were calculated using Eq. 6 and Eq. 7. Small resistors are placed in series with the integrating capacitors to suppress parasitic oscillations.

For single-edge waveforms (sawtooth) two new factors must be considered. The current surges which occur during transitions are limited by R_{SE} to protect the comparator. Also, the abrupt transitions magnify the high-frequency amplitude problem beyond the range of the ALC circuitry. This is remedied by changing the toggle voltage during the transition with a diode placed in parallel with the voltage-dependent resistor.

6. The Impedance Converter

The output waveform is buffered by the unity-gain impedance converter shown in Figure 11. This circuit consists of a common-source FET amplifier in cascade with a common-emitter bipolar amplifier. Unity negative feedback sets the gain and gives wide bandwidth. The current regulator diode, CR_{304}, is used as a load for the impedance converter to reduce the effects of power-supply voltage variations. R_{310} provides short-circuit protection.

7. The Automatic Level Control

The automatic level control (ALC) circuitry is shown in Figure 12

a. The Peak Detector

An LM306 comparator which has high gain and high speed is used in the peak detector. C_{303} is large enough to eliminate ripple at low frequencies. The accuracy of the peak detector is within one percent at one megahertz.

b. The Error Amplifier

An LM301A operational amplifier is used for the error amplifier. Chief considerations in the selection of this amplifier are low input-

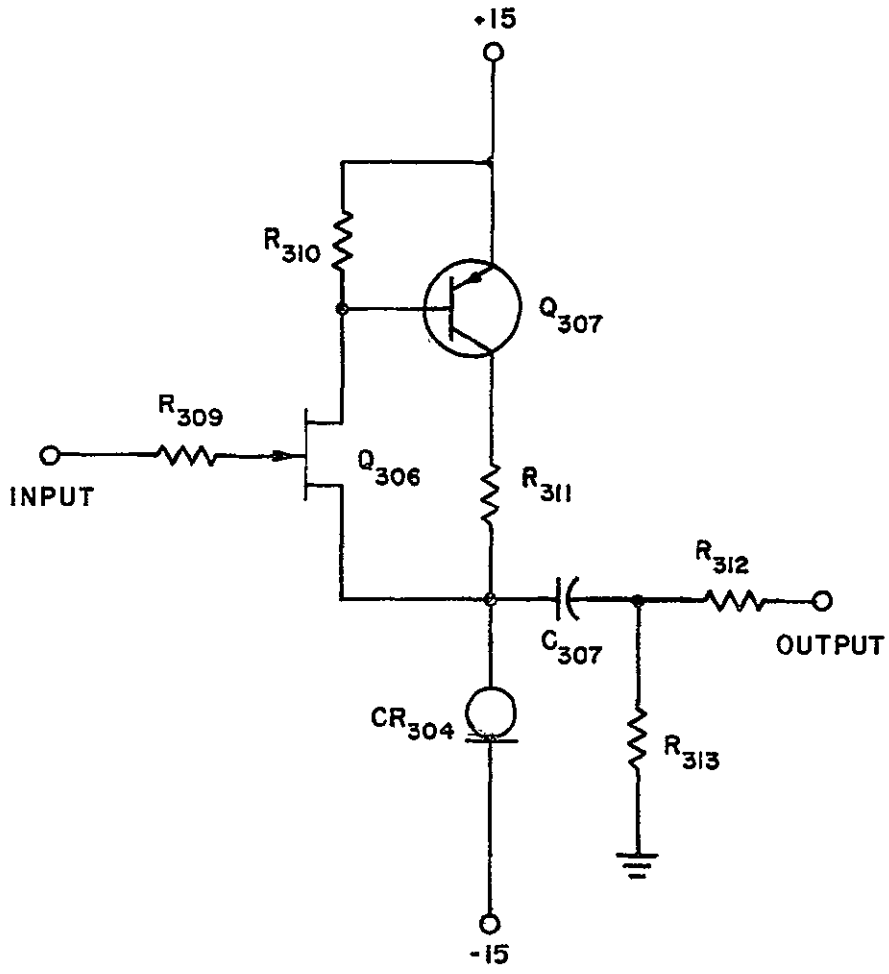


Figure 11. Schematic diagram of impedance converter.

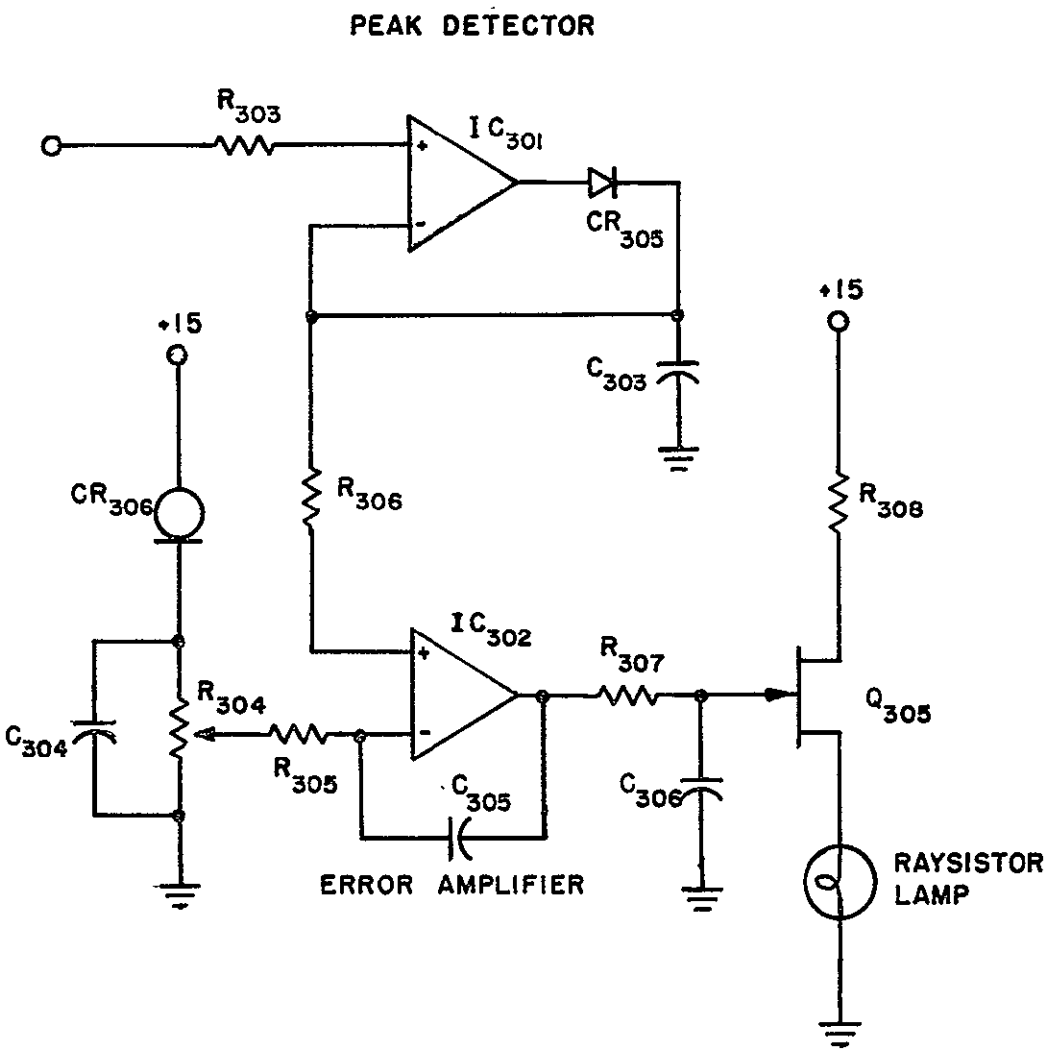


Figure 12. - Schematic diagram of ALC.

offset voltage and high DC gain. Frequency-dependent negative feedback is applied through C_{305}. This provides a dominent pole to stabilize the ALC loop. Values for C_{305} and R_{305} were determined experimentally. A current-regulator diode is used to obtain the reference voltage.

c. The Voltage-Dependent Resistor

A Raysistor (Raytheon trademark) is used for the voltage-dependent resistor because it affords excellent isolation through optical coupling An FET is used to drive the Raysistor lamp. R_{307} and C_{306} remove any spikes present at the output of the error amplifier.

C. The Carrier Amplifier

1. Design Criteria

1) Differential output
2) Less than 5 ns differential delay
3) Less than 1% differential gain error
4) Less than 20 ns rise time for ±5 volt output
5) Gain ≐5
6) Level control

The carrier amplifier circuit is shown in Figure 13. Two cascaded differential amplifiers feed a pair of emitter followers. This configuration yields balanced outputs with low output impedance.

2. Application of Negative Feedback

Negative feedback is employed to insure that the gains for each output will be equal. This is done with resistors: R_{101}, R_{102}, R_{401}, R_{402}, R_{408}, and R_{412}. In order to avoid instability problems, this wide-bandwidth amplifier is designed to be absolutely stable without

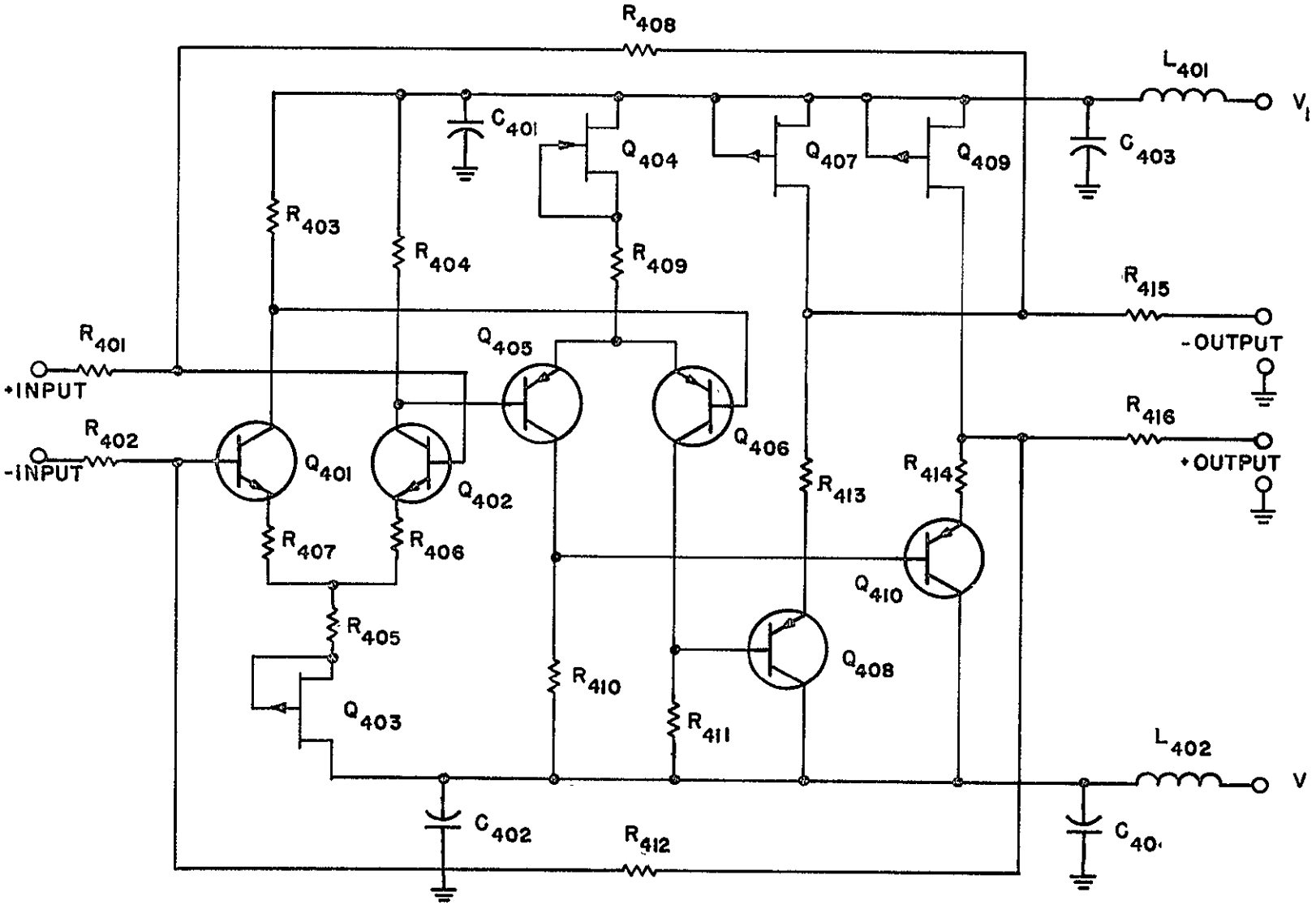


Figure 13. - Schematic diagram of carrier amplifier.

compensation. The general form of the open-loop frequency response is illustrated in Figure 14. Each of the stages contributes one break point. Other break points due to second-order effects occur at sufficiently high frequencies to be ignored.

To insure absolute stability it is desirable for the open-loop gain curve to cross the zero-decibel axis before or near the second break point. This provides an adequate phase margin. For the curve shown, this requires that two of the break points occur at a substantially higher frequency than the first as shown by the dotted response in Figure 14. This gives the same "dominant-pole" effect as the addition of a compensating network.

The input stage is designed to have the lowest cutoff frequency of the three stages for the following reasons:

1) The signal swings are smallest in the input stage, thus slew-limiting is minimized.
2) High-frequency overloading of the following stages is minimized.
3) The necessary DC levels permit this stage to have the highest gain.

3. The Input Stage

The values for R_{403} and R_{404} are made as small as possible without causing the input bias currents to become excessive. A matched pair of 2N2219 transistors is used for Q_{401} and Q_{402}. The input stage is biased by Q_{303} which is used as a constant-current regulator of 6 mA.

4. The Second Stage

In order to get sufficient bandwidth, the second stage is operated at a current of approximately 15 mA per transistor. This value is

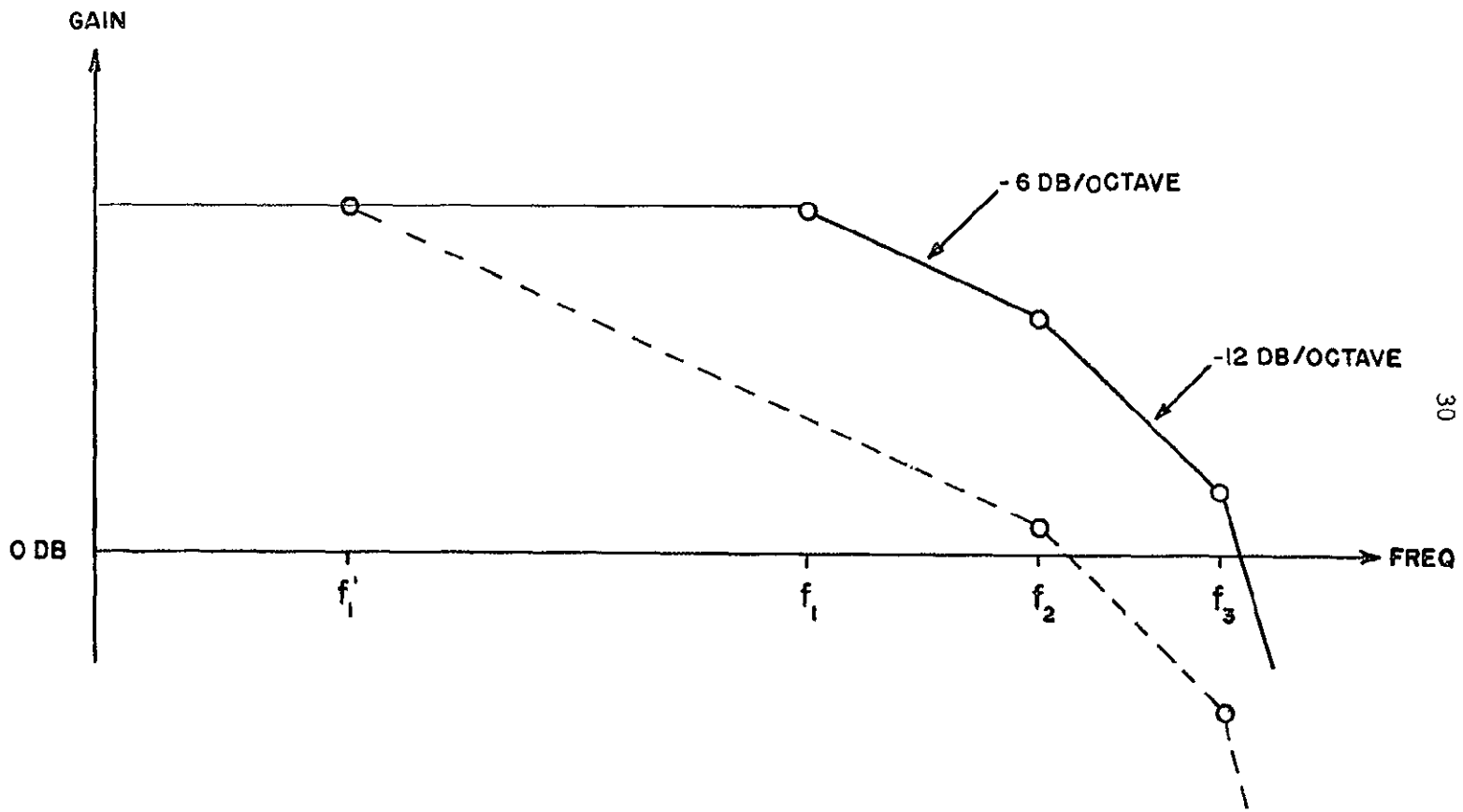


Figure 14. - General form for the open-loop frequency response of the carrier amplifier.

limited by the dissipation allowable for Q_{405} and Q_{406}, a pair of 2N2905 transistors. R_{410} and R_{411} were chosen to be 1.2 kilohms in order to get proper output offset with the 15 ma bias current previously determined.

5. The Output Stages

Two emitter-follower amplifiers are used as output stages. One serves as a buffer amplifier for the non-inverted signal and the other, for the inverted signal. Each stage consists of a 2N2905 transistor with a 2N5461 FET in the emitter circuit to serve as a constant-current device. Resistors, R_{413} and R_{414} limit the current under fault conditions.

6. Stability and Gain

The overall gain of the two channels is determined by the driving-source impedances and resistors: R_{401}, R_{402}, R_{408}, and R_{412}. The resistors in the emitters of the input-stage transistors are used to set the open-loop gain to a value which provides unconditional stability.

7. The Gain Control

The gain control, R_{103}, is isolated from the carrier amplifier by an emitter-follower amplifier to avoid upsetting the gain balance between the two channels of the carrier amplifier. This circuitry is shown in Figure 15. R_{102} is adjusted to compensate for the output impedance of the emitter-follower amplifier.

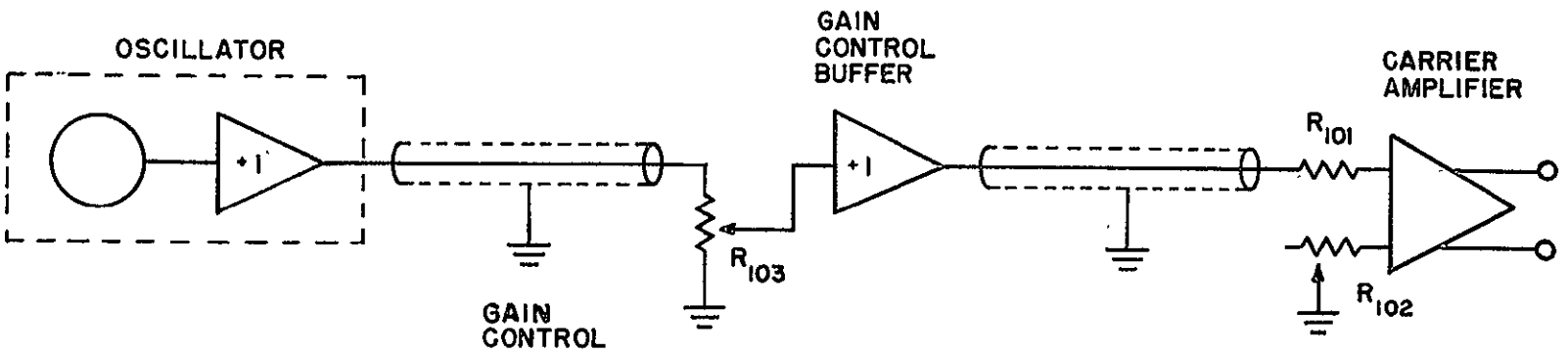


Figure 15 - Gain control circuitry.

D. The Input Amplifier

1. Design Criteria

1) Gain from 0-10
2) AC and DC coupling
3) Bandwidth of at least 100 kHz
4) Low distortion
5) Slew rate $\geq$ 50

2. Circuit Description

All of the design criteria are met with a commercially available operational amplifier, the Burr-Brown Model 1510. Because the input amplifier must also be able to attenuate the signal, the inverting mode is used as illustrated in Figure 16. The gain is continuously adjustable through the use of the feedback network consisting of potentiometer, R_{21}, and the incremental steps provided by R_{22} through R_{32}.

The values selected for R_{in} and R_f compromise between input impedance and offset. C_{in} and C_{out} are large, non-polarized electrolytic capacitors. R_{in} and C_{in} produce a low-frequency breakpoint at about one hertz.

E. The Output Amplifier

1. Design Criteria

1) Add P and N channel signals
2) $\pm$ 20 volt output
3) High-speed response
4) Three output states (+20,0,-20)
5) Protected for any load impedance

2. Circuit Description

The output amplifier shown in Figure 17 serves as a summing amplifier and provides gain. AC coupling is used to facilitate design. This

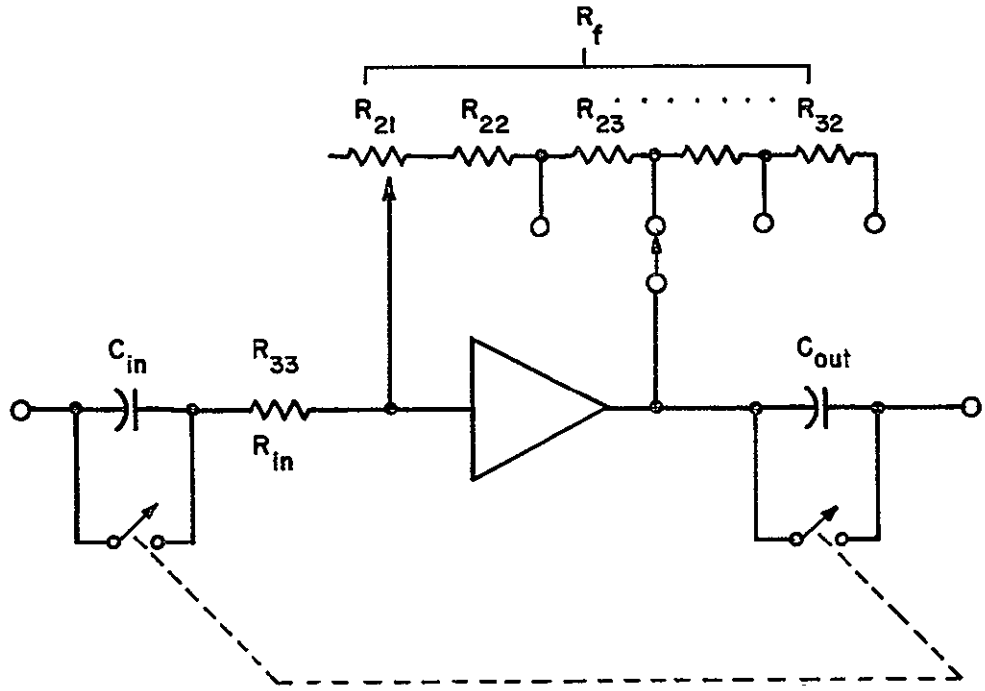


Figure 16. - Input amplifier schematic diagram.

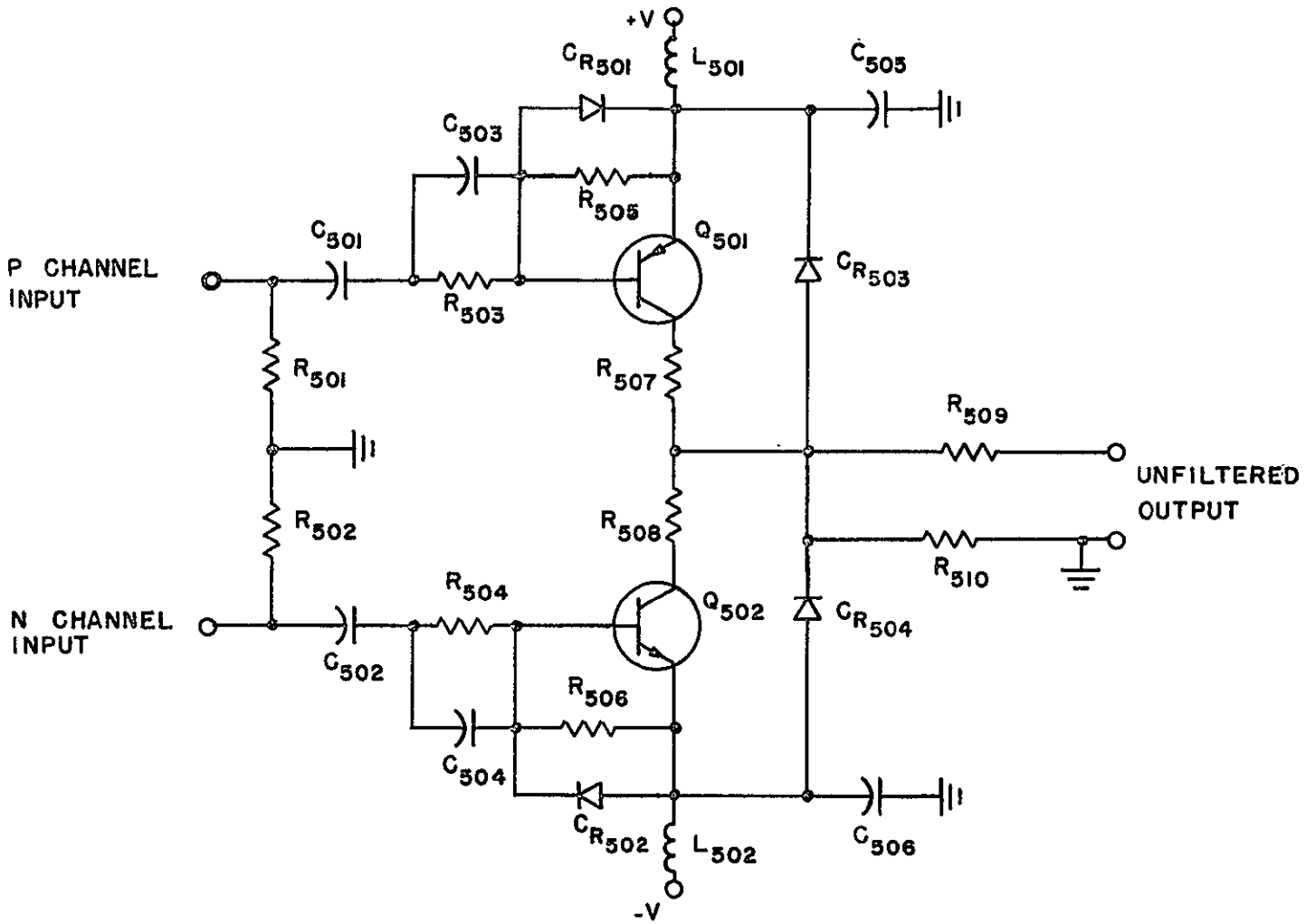


Figure 17. - Output amplifier schematic diagram.

amplifier operates in the switching mode from cut-off to saturation. The switching times are reduced through the use of the speed-up techniques discussed in Appendix A.

Resistors from the bases to the emitters of Q_{501} and Q_{502} hold them off in the absence of an input signal. Since the leakage currents are not equal, the output is held near zero potential by R_{510} when the load is removed.

In the abnormal event that input signals should turn-on both transistors simultaneously, a large common-mode current would flow from the positive supply to the negative supply. This would demand excessive dissipation of one or both of the output transistors. Resistors, R_{507} and R_{508}, serve to limit this current and, hence, the dissipation under these conditions.

When the amplifier is used to drive inductive loads such as a transformer, high-voltage transients may be generated. The output transistors are protected from these by the diodes, CR_{503} and CR_{504}.

F. The Active Filters

1. 1) Low-pass Butterworth characteristics.
   2) One, two, and three-pole filters.
   3) Cut-off frequencies in kHz: (1, 2, 5, 10, 20, 50)

2. Circuit Description

The active filter circuitry shown in Figure 18 is of conventional design. The two buffer amplifiers are integrated voltage-followers. Due to the limited output swing of these amplifiers, the waveform

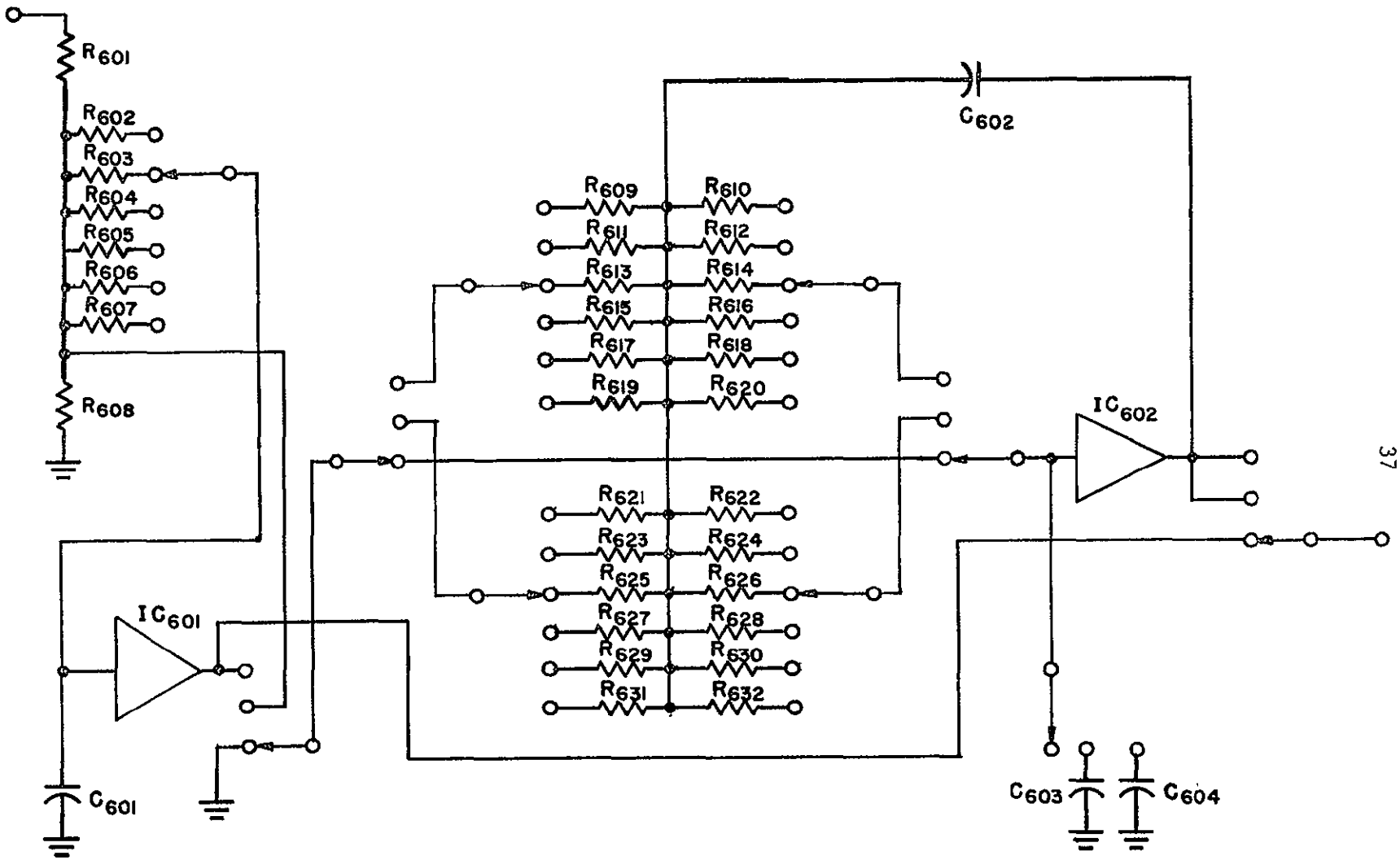


Figure 18. - Schematic diagram of active filters.

from the output amplifier is attenuated 6 dB by resistors, R_{601} and R_{602}. The values for the frequency-selective components were calculated using a digital computer.

G. The Power Supplies

1. Design Criteria

1) Provide $\pm$ 20 volts and $\pm$ 15 volts
2) Ripple $\leq$ 10 mv. at full load.
3) Regulation $\leq$ 1% at full load.

2. Circuit Description

Since all of the circuit modules of the amplifier are designed for good stability, voltage regulators of simple design are employed in the power supply. A transformer is utilized in the power supply to provide isolation from the power line. The circuitry for the power supply which utilizes Zener diodes for regulation is shown in Figure 19.

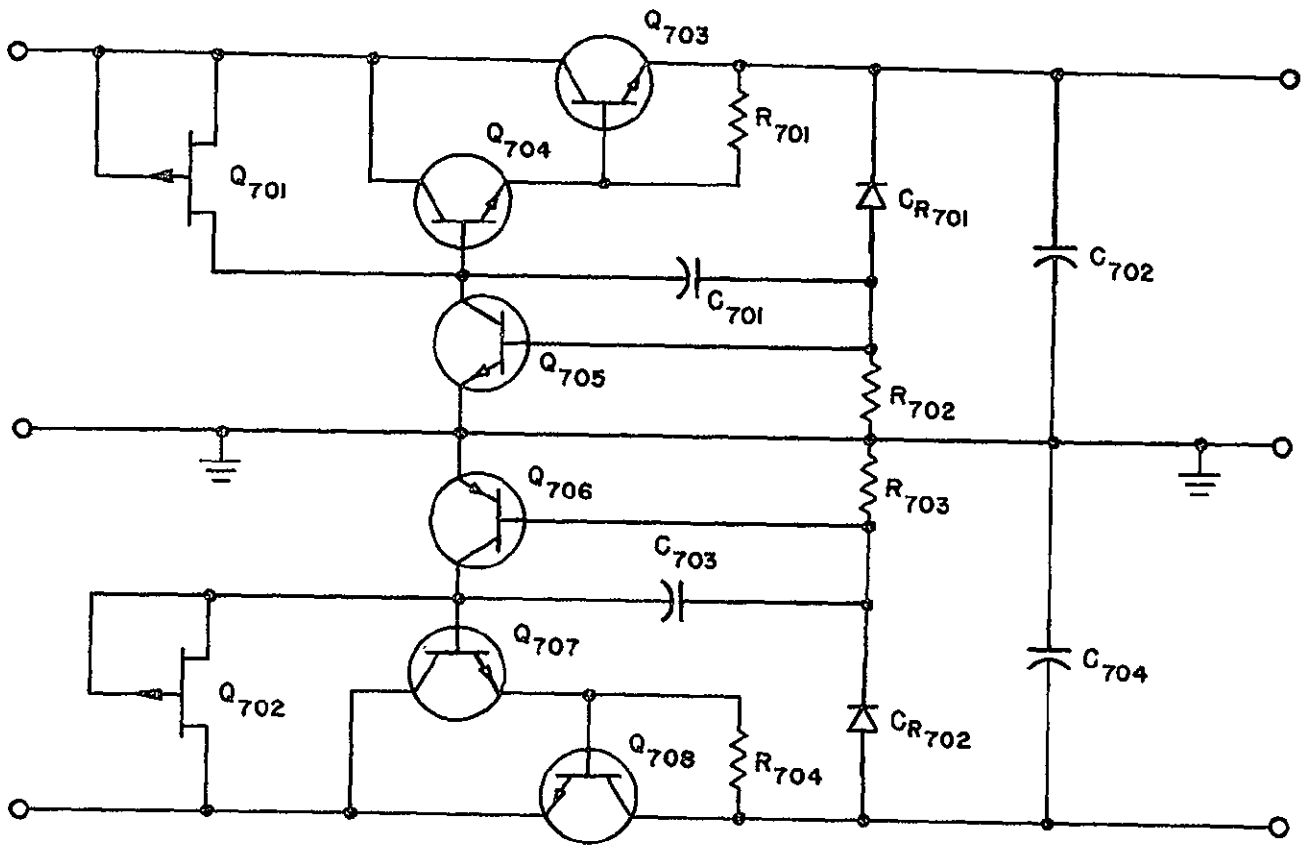


Figure 19. - Power supply schematic diagram.

IV. PERFORMANCE

Each of the circuit modules for the PWM amplifier was constructed and tested. The composite PWM amplifier performs quite well at carrier frequencies up to 100 kHz. At higher carrier frequencies the output summing amplifier limits the performance. The high-frequency operation was improved by the use of a passive output summing stage. It is recommended that future research be directed in this area.

The open-loop performance of the programmable PWM amplifier is illustrated in Figures 20 through 25.

Figure 20 illustrates typical Type A operation while Figure 21 shows typical Type B operation. In both cases the carrier is a 50 kHz triangular wave, the input is a 5 kHz sinusoid, and the filters are set for a 12 db/octave roll-off at 5 kHz. The figures show both the unfiltered and filtered outputs. It is noted that the filtered output for Type B operation is less distorted than the filtered output for Type A operation.

Figure 22 illustrates the response of the PWM amplifier to a square wave. The carrier frequency is 50 kHz. The input is a 1 kHz. square wave and the filters are set for a 12 db/octave roll-off at 10 kHz. The overshoot in the response is characteristic of the low-pass Butterworth filter of two or more poles.

A good illustration of the recovery of the signal from the

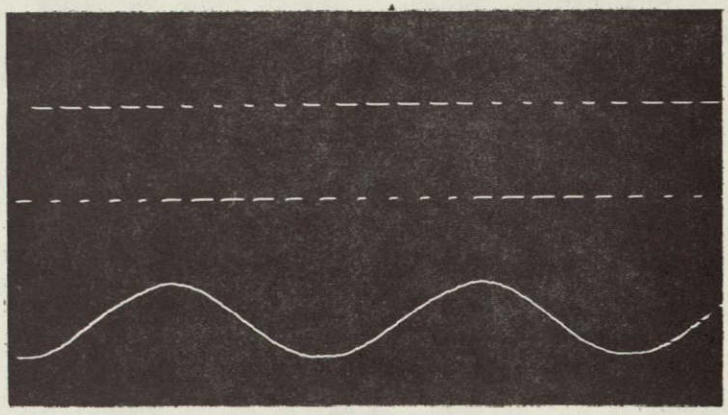


Figure 20. - Waveforms associated with Type A operation.
(f_c = 50 kHz, f_f = 5 kHz, f_{signal} = 5 kHz)

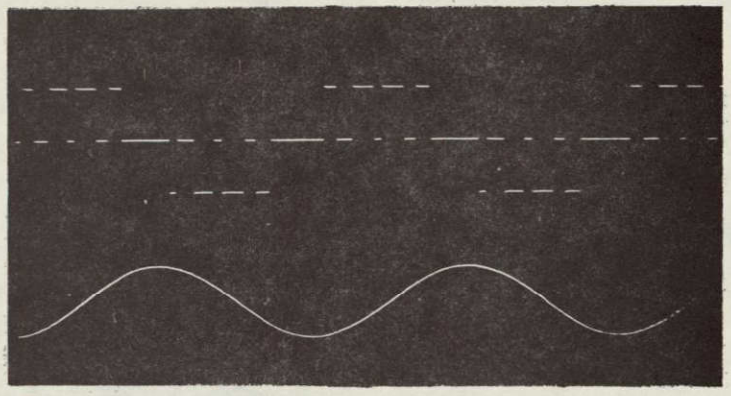


Figure 21. - Waveforms associated with Type B operation.
(f_c = 50 kHz, f_f = 5 kHz, f_{signal} = 5 kHz)

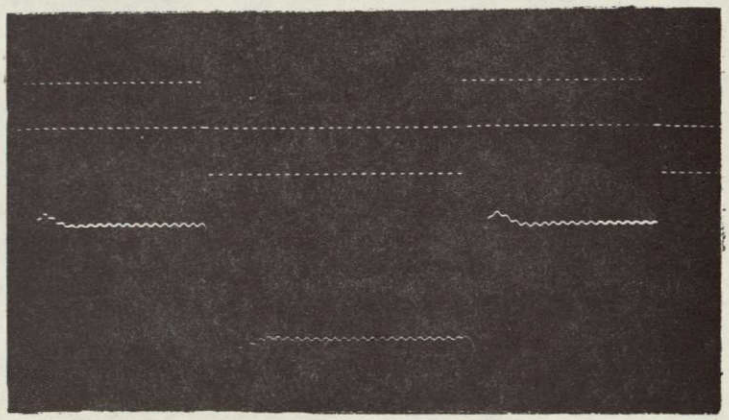


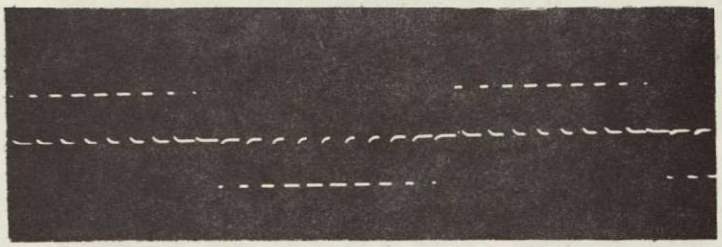
Figure 22. - Square wave response.
(f_c = 50 kHz, f_f = 10 kHz, f_{signal} = 1 kHz)

modulated output is seen in Figure 23. In this case the carrier frequency is 20 kHz and the signal is a 1 kHz sinusoid. The filter is set for 12 db/octave roll-off at 50 kHz. The signal is progressively filtered by switching the break-frequency of the filters to lower and lower frequencies.

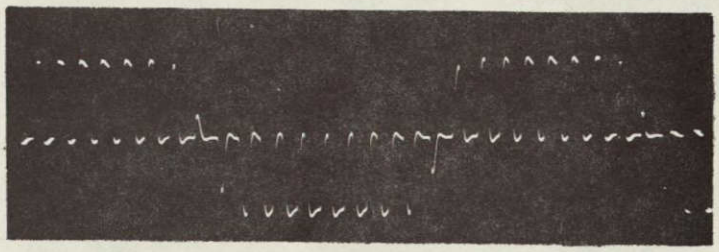
Figure 24 indicates the linearity of the amplifier. The gain was changed for each of the curves shown to prevent the curves from falling on top of each other.

The quality of the oscillator signal and the performance of the comparators is illustrated in Figure 25. For both waveforms the frequency is 100 kHz. The square wave produced by the comparator is 30 volts peak-to-peak.

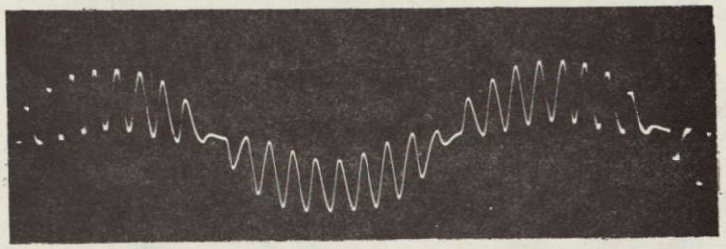
One problem with the system becomes apparent whenever the amplitude of the carrier signal is changed. The bias voltages must be reset each time the carrier amplitude is changed because the bias voltage applied to the comparators is dependent on the peak value of the carrier signal. This adjustment is quite critical for Type B operation. For these reasons it would be desirable to have a circuit to automatically set the bias voltages. It is suggested that work be done in this area in the future.



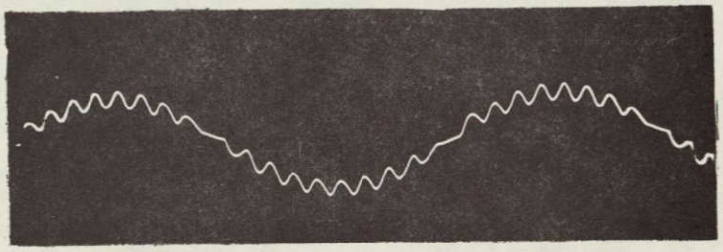
Unfiltered output.



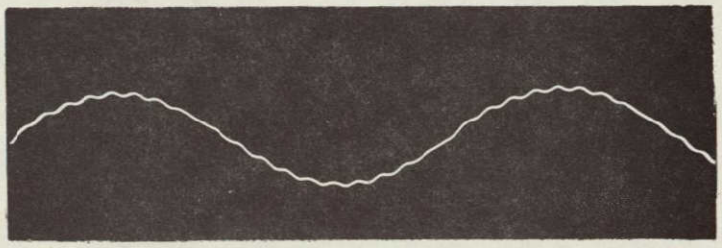
Filter Cutoff = 50 kHz



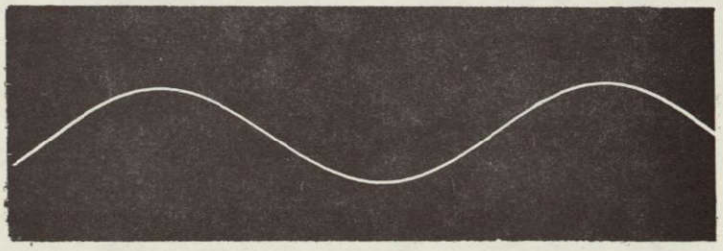
Filter Cutoff = 20 kHz



Filter Cutoff = 10 kHz



Filter Cutoff = 5 kHz



Filter Cutoff = 2 kHz

Figure 23. - Sequential filtering of the output waveform with 12 dB/octave roll-off. (f_c = 20 kHz, f_{signal} = 1 kHz)

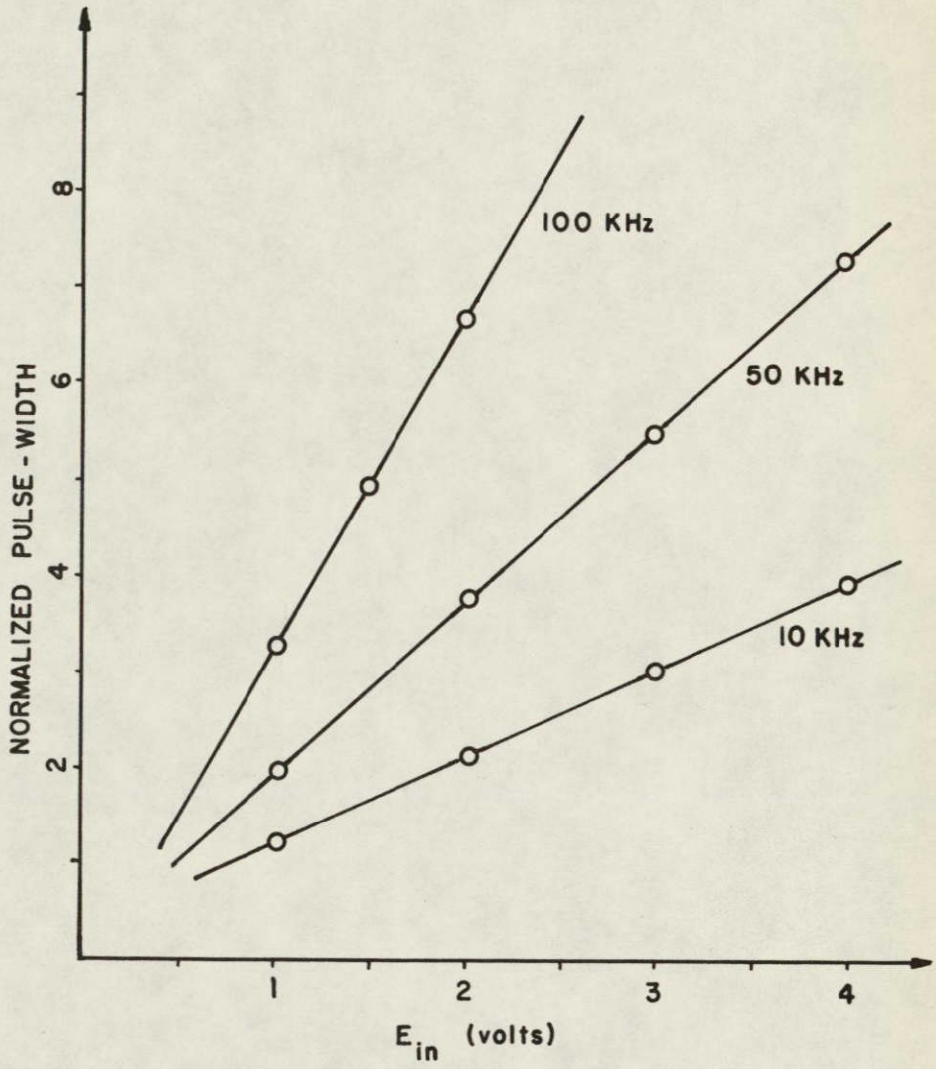


Figure 24. - Amplifier linearity.

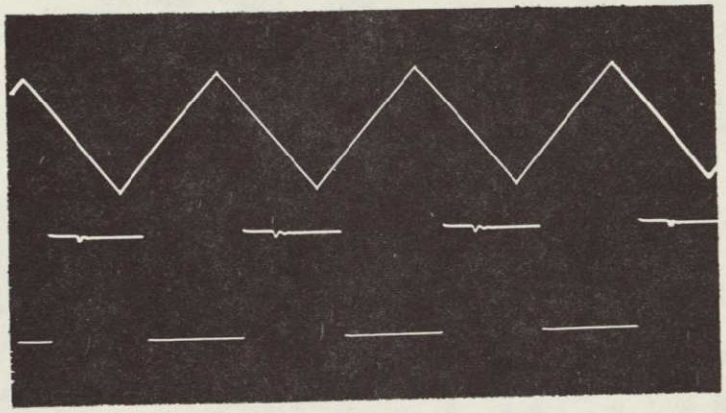


Figure 25. - Triangular wave and comparator output at 100 kHz.

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2. M. A. Honnell et. al., A Low-Distortion Switching-Mode Amplifier, Engineering Experiment Station, Auburn University, Auburn, Alabama, May, 1968.

3. Hewlett-Packard Journal, Hewlett-Packard Company, 1506 Page Mill Road, Palo Alto, California, June, 1969.

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APPENDIX A

I. GENERAL SWITCHING RELATIONS

Because many of the functions of the PWM amplifier involve switching, it is necessary to obtain the proper criteria for the design of switching circuits. Rather than show the computations for each individual device, the general relations are covered here. In many instances values of components, or bias values, were chosen empirically. The following design equations were very useful in determining the proper configurations and range of values to use [4].

A. Rise Time

The rise time of the transistor shown in Figure 26 is given by

$$t_{on} = \tau_A \ln\left(\frac{K_{on}}{K_{on}-1}\right) \tag{11}$$

where τ_A is the active-region time constant and K_{on} is the input overdrive factor. The active-region time constant is given by

$$\tau_A = \frac{\beta_o (1 + \alpha R_L C_{ob} \omega_t)}{\omega_t} \tag{12}$$

and the turn-on overdrive factor may be computed from

$$K_{on} = \frac{\beta_o I_{B(on)} R_L}{V_{cc}} \tag{13}$$

The base current, I_B, is given by

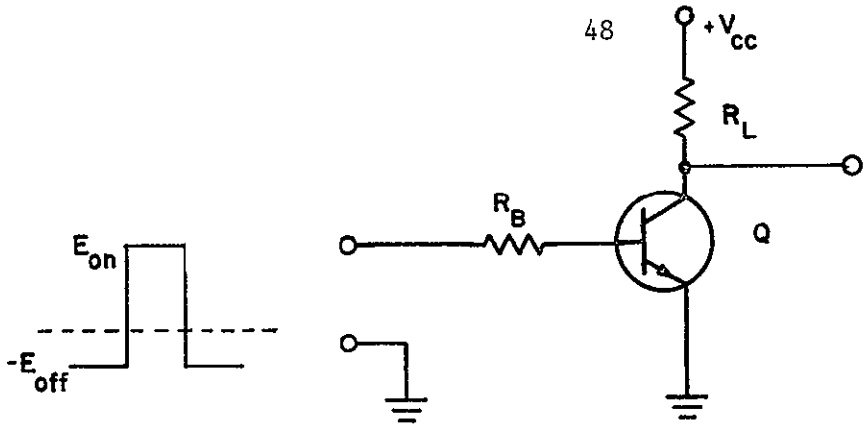

Figure 26. - Basic transistor switch.

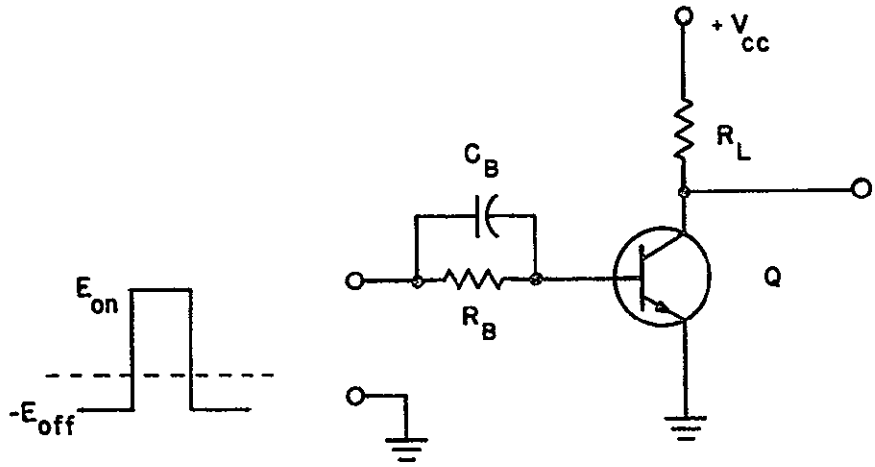

Figure 27. - Transistor switch with speed-up network.

$$I_{B(on)} = \frac{E_{on} - V_{BE(sat)}}{R_s} \tag{14}$$

Equation 11, shows that the smaller R_L and C_{ob} are, the faster the switching time. For this reason a low value of C_{ob} is a prime criteria in the selection of transistors. Once an optimum choice of R_L is made, the amount of overdrive necessary may be calculated.

B. Fall Time

The fall time for the switch of Figure 26 is given by

$$t_{off} = \tau_A \ln\left(\frac{K_{off} + 1}{K_{off}}\right) \tag{15}$$

The turn-off overdrive factor, K_{off}, is given by

$$K_{off} = \frac{V_{cc}}{R_L I_{B(off)} \beta_0} \tag{16}$$

where

$$I_{B(off)} = \frac{-E_{off} + V_{BE(sat)}}{R_s} \tag{17}$$

C. Delay and Storage Times

Saturation storage time is given by

$$t_s = \tau_s \ln \frac{I_{B(on)} - I_{B(off)}}{I_{B(sat)} - I_{B(off)}} \tag{18}$$

where τ_s is the recombination time, a parameter of the transistor. Unfortunately, the conditions which lead to good rise time,

$I_{B(on)} >> I_{B(sat)}$, also result in relatively long storage times. Where possible the emitter-coupled (differential) configuration was used to keep the transistors from going into saturation. Where this was not possible, transistors with very low τ_s values were chosen. In this manner it was possible to avoid compromising either of the switching times.

The turn-on delay time is given by

$$t_d = R_s C_{B'C} \ln\left(\frac{E_{on} + E_{off}}{E_{on} - V_{BE(sat)}}\right) \tag{19}$$

A similar problem arises here in that one switching time may be improved at the expense of another. In this instance a large value of turn-off voltage, giving good fall times, results in increased delay times. This problem is handled in much the same manner as storage time.

D. Speed-Up Capacitors

In those cases where R_s is an external resistor it is possible to improve the switching performance by the use of a speed-up capacitor, C_B, as shown in Figure 27. The value of C_B may be calculated by

$$C_B = \frac{1}{R_s \tau_A} \tag{20}$$

II. SELECTION OF SEMICONDUCTORS

Due to the nature of the waveforms generated by the programmable PWM amplifier many of the circuits require very wide bandwidth. For this reason the semiconductor devices used were carefully selected to achieve the performance desired from each of the circuits.

A. Bipolar Transistors

The bipolar transistors used may be grouped into three separate catagories:

1) general purpose switching and amplifier transistors
2) high-speed saturated switching transistors
3) miscellaneous low-frequency transistors

Transistors from the first group perform all of the signal related operations. These transistors must have sufficient current, voltage, and power capabilities, as well as the ability to operate at high frequency. To simplify design this group was narrowed to include one basic NPN type (2N2219) and one basic PNP type (2N2905). These transistors have excellent switching times as well as the capacity to handle the voltages and currents associated with both high- and low-level stages.

When a transistor is driven into hard saturation, low storage and delay times are a prime consideration. For the second group of transistors, the 2N2369-2N3227 family was chosen. These transistors exhibit extremely low storage time and are capable of total switching

times of 25 nanoseconds or less. Because of the special doping used in the manufacture of these transistors, their voltage ratings are substantially lower than those of the first group.

The third group of bipolar transistors employed is composed primarily of power-supply devices. Due to the nature of these tasks, the primary selection criteria was simply that of sufficient ratings.

B. Field-Effect Transistors

Where high input impedance or low bias currents were desired, FET's were used. Other than the obvious need for adequate voltage ratings, the primary parameters of interest were zero-gate-voltage drain current, I_{DSS}, and the input and transfer capacitances, C_{iss} and C_{rss} respectively. To achieve high bandwidth these capacitances should be as low as possible. The FET's chosen were from the 2N4220 family. These FET's are available in a wide range of I_{DSS} values, simplifying design.

C. Diodes

1N914 diodes are used in the high-speed switching circuits. A large number of current sources were used in the modulator. Where small size or very high dynamic impedance was required, current regulator diodes were used. For many of the current sources the FET's with their gates shorted to their sources as shown in Figure 28 were employed.

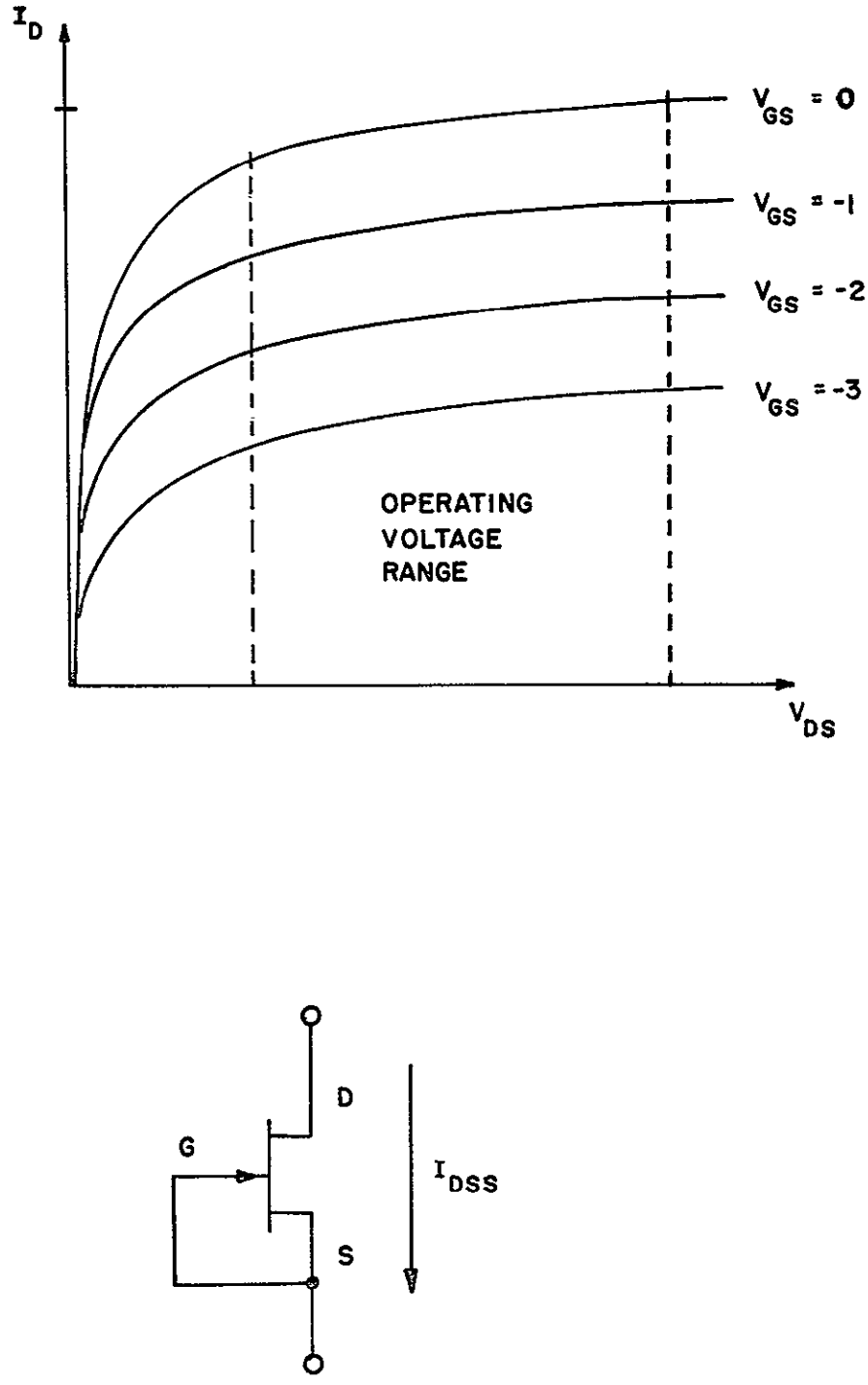

Figure 28. - Constant current characteristic of FET

III. GENERAL CIRCUIT PROBLEMS

Circuits designed to generate or amplify high-frequency waveforms must include protective measures to suppress oscillations. Many of the circuits used in the PWM amplifier respond to frequencies in excess of twenty megahertz. The following circuit techniques were employed to prevent potential problems. Power supply decoupling and bypassing is used to reduce the AC impedance of the power supply. Decoupling prevents the supply leads from acting as stray signal paths. Figure 29 shows the networks used for most of the modules. Where convenient, commercial feed-through filters were also used in power supply lines. Electrolytic capacitors are not effective as bypass elements above a few megahertz. This was remedied by additional bypassing with ceramic capacitors.

The second technique is the use of parasitic suppressors in high-impedance signal paths. Sometimes stray lead inductance forms a resonant circuit with circuit capacitance. The addition of a small noninductive resistor in a signal path lowers the Q of such a resonant circuit thus preventing oscillation, or ringing. Since stray parameters are difficult to measure, the value of resistor required was usually chosen empirically.

The last technique deals with circuit layout. Signal leads were kept as short as possible. Also an effort was made to keep input and

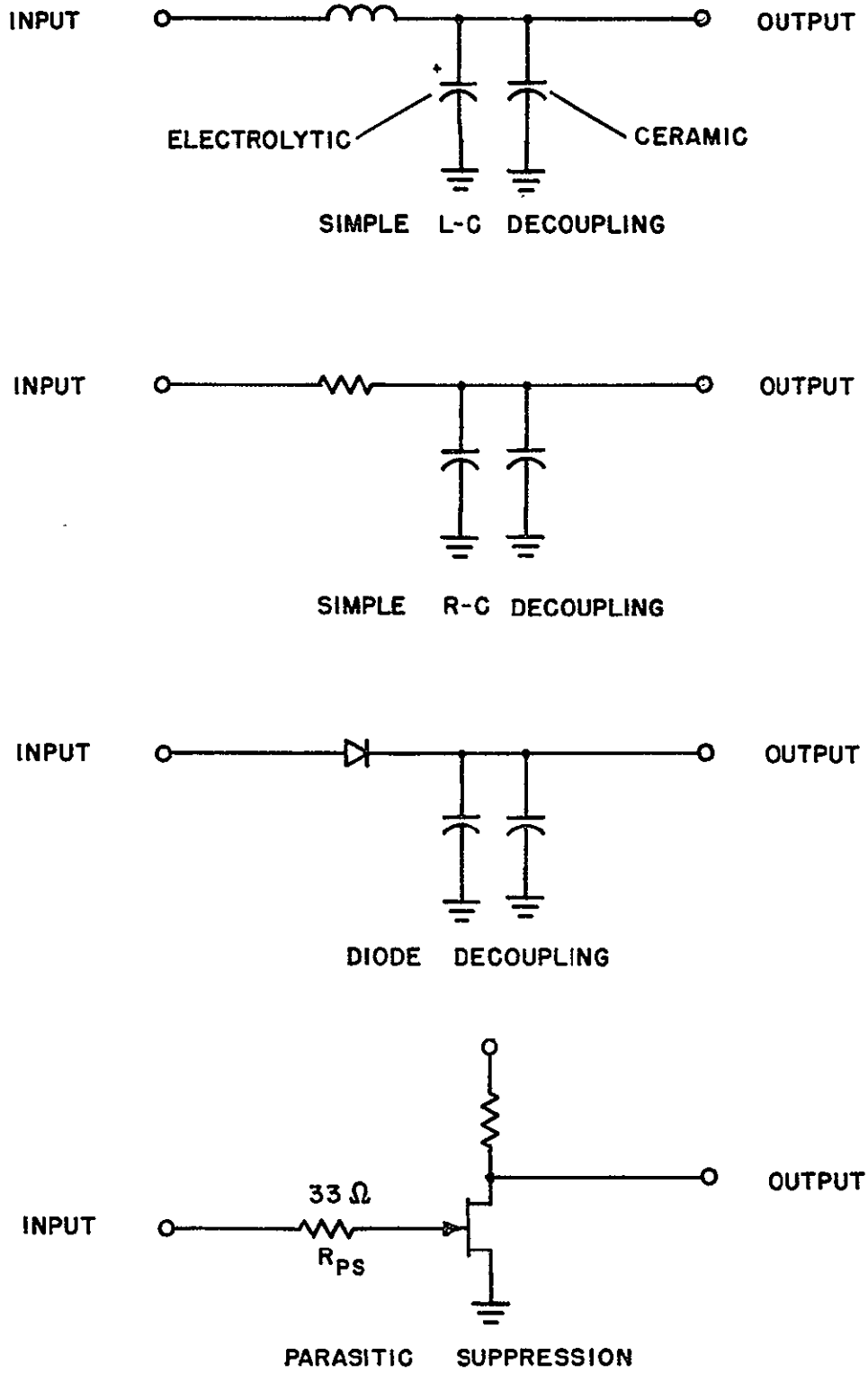

Figure 29. - Decoupling networks and parasitic suppression.

output circuitry as far apart as possible.

APPENDIX B

COMPLETE PARTS LIST

OF THE

PULSE-WIDTH-MODULATED

SIGNAL GENERATOR

CHASSIS MOUNTED PARTS

SYMBOL	VALUE	COMMENTS
R-1	100 Ω	Pot., ganged with R-20
R-2 thru R-19	97.3 Ω	1/2 w, 1%
R-20	100 Ω	Pot., ganged with R-1
R-21	10 kΩ	Pot.
R-22 thru R-33	10 kΩ	1/4 watt, 1%
R-34	12.4 kΩ	1/2 watt
R-35	10 kΩ	Pot., 10-turn
R-36	17.5 kΩ	1/2 watt
R-37	12.4 kΩ	1/2 watt
R-38	10 kΩ	Pot., 10-turn
R-39	17.5 kΩ	1/2 watt
R-40 thru R-45	680 Ω	1/2 watt
R-46	150 kΩ	1/4 watt
R-47 thru R-50	5490 Ω	1/2 watt, 1%
R-51	150 kΩ	1/4 watt
C-1	5500 μF	40 v
C-2	5500 μF	40 v
C-3 thru R-14	0.1 μF	100 v
C-15	6.8 μF	35 v
C-16	6.8 μF	35 v

CHASSIS MOUNTED PARTS (continued)

SYMBOL	VALUE	COMMENTS
C-17	20 µF	30 VNP
C-18	500 µF	10 VNP
C-19	430 pF	1000 v
C-20	.0068 µF	400 v
C-21	.015 µF	400 v
CR-1 thru CR-4	IN5061	600 v, 1 amp
F-1	1/2 amp	fuse
T-1	Pri: 117 VAC SEC: 43 VCT	UTC - S77
AMP-1	Model 1510	
S-1	SPST	
S-2	DPDT	
S-3	5 position	5 poles
S-4	6 position	5 poles
S-5	3 position	4 poles
S-6	10 position	1 pole

COMPARATOR PARTS LIST

SYMBOL	VALUE	COMMENTS
R-101	40.2 Ω	1/4 watt
R-102	40.2 Ω	1/4 watt
R-103	1 kΩ	Pot., 10-turn
R-104	2 kΩ	1/4 watt
R-105	2 kΩ	1/4 watt
R-106	40.2 Ω	1/4 watt
R-107	10 Ω	1/4 watt
R-108	316 Ω	1/4 watt
R-109	316 Ω	1/4 watt
R-110	100 Ω	1/4 watt
R-111	10 Ω	1/4 watt
R-112	1 kΩ	1/2 watt
R-113	390 Ω	1/2 watt
R-114	390 Ω	1/2 watt
R-115	12 Ω	1/2 watt
R-116	12 Ω	1/2 watt
R-117	47 Ω	1/2 watt
C-101	1 μF	100 v
C-102	1 μF	100 v
C-103	1000 pF	1000 v

COMPARATOR PARTS LIST (continued)

SYMBOL	VALUE	COMMENTS
C-104	.1 μF	100 v
C-105	.1 μF	100 v
L-101	18 μH	
L-102	18 μH	
CR-101	MZ2361	
Q-101	2N4222	FET
Q-102	2N4222	FET
Q-103	2N5461	FET (Selected for I_{DSS} = 6ma.)
Q-104	2N5461	FET (Selected for I_{DSS} = 6ma.)
Q-105	2N2905 A	
Q-106	2N2905 A	
Q-107	2N2369 A	
Q-108	2N3227	Selected for $V_{CEO} \geq 30$ volts
Q-109	2N2905	
Q-110	2N2219	

Note: The comparator with 200 designations uses same parts as listed above.

OSCILLATOR PARTS LIST

SYMBOL	VALUE	COMMENTS
R-301	887 Ω	1/4 watt, 1%
R-302	1.77 kΩ	1/2 watt, 1%
R-303	56 Ω	1/2 watt
R-304	1 kΩ	Pot., 10-turn
R-305	47 kΩ	1/4 watt
R-306	130 Ω	1/4 watt
R-307	1 MΩ	1/2 watt
R-308	1 kΩ	1/2 watt
R-309	35 Ω	1/2 watt
R-310	825 Ω	1/2 watt
R-311	40.2 Ω	1/4 watt
R-312	33 Ω	1/2 watt
R-313	22 kΩ	1/2 watt
R-314	680 Ω	1/4 watt
R-315	680 Ω	1/4 watt
R-316	1.5 kΩ	1/2 watt
R-317	390 Ω	1/2 watt
R-318	390 Ω	1/2 watt
R-319	47 Ω	1/2 watt
R-320	47 Ω	1/2 watt
R-321	97.6 Ω	1/2 watt
R-322	220 Ω	1/2 watt

OSCILLATOR PARTS LIST (continued)

SYMBOL	VALUE	COMMENTS
R-323	35 Ω	1/2 watt
R-324 and R-328	56 Ω	1/2 watt
R-325	9311 Ω	1/4 watt
R-326	1300 Ω	1/2 watt
R-327	22 Ω	1/2 watt
C-301 thru C-303	22 μF	15 v
C-304	4.7 μF	20 v
C-305	10 μF	30 v
C-306	0.1 μF	100 v
C-307	33 μF	50 v
C-308 thru C-313	0.1 μF	100 v
C-314	390 pF	1000 v
C-315	360 pF	1000 v
C-316	100 μF	35 v
C-317	100 μF	35 v
C-318	22 μF	15 v
C-319	22 μF	15 v
L-301	24 μH	
L-302	24 μH	
CR-301	1N4001	

OSCILLATOR PARTS LIST (continued)

SYMBOL	VALUE	COMMENTS
CR-302	1N4001	
CR-303	1N5305	
CR-304	1N5308	
CR-305	1N914	
CR-306	1N5308	
CR-307 thru CR-309	1N914B	
CR-310	MZ2361	
CR-311	MZ2361	
Q-301	2N3971	FET
Q-302	2N3971	FET
Q-303	2N2905	
Q-304	2N2219	
Q-305	2N3971	FET
Q-306	2N4222	FET
Q-307	2N2905	
Q-308	2N4222	FET
Q-309	2N4222	FET
Q-310	2N2905	
Q-311	2N2905	
Q-312	2N2219	
Q-313	2N2905	

OSCILLATOR PARTS LIST (continued)

SYMBOL	VALUE	COMMENTS
IC-301	LM306	
IC-302	LM301 A	
RAY-301	CK1116	(Raytheon)
S-301	10 positions	2 poles
S-302	3 positions	2 poles

CARRIER AMPLIFIER PARTS LIST

SYMBOL	VALUE	COMMENTS
R-401	953 Ω	1/4 watt
R-402	953 Ω	1/4 watt
R-403	1.1 kΩ	1/2 watt
R-404	1.1 kΩ	1/2 watt
R-405	316 Ω	1/4 watt
R-406	113 Ω	1/2 watt
R-407	113 Ω	1/2 watt
R-408	9311 Ω	1/4 watt
R-409	10 Ω	1/4 watt
R-410	1.2 Ω	1/2 watt
R-411	1.2 Ω	1/2 watt
R-412	9311 Ω	1/4 watt
R-413	40.2 Ω	1/4 watt
R-414	40.2 Ω	1/4 watt
C-401	0.1 μF	100 v
C-402	0.1 μF	100 v
C-403	33 μF	50 v
C-404	33 μF	50 v
L-401	24 μH	

CARRIER AMPLIFIER PARTS LIST (continued)

SYMBOL	VALUE	COMMENTS
L-402	24 μH	
Q-401	2N2219	
Q-402	2N2219	
Q-403	2N5461	FET (Selected for I_{DSS} = 5 ma.)
Q-404	2N3971	FET (Selected for I_{DSS} = 30 ma.)
Q-405	2N2905	
Q-406	2N2905	
Q-407	MPF 153	FET
Q-408	2N2905	
Q-409	MPF 153	FET
Q-410	2N2905	

OUTPUT SUMMING AMPLIFIER PARTS LIST

SYMBOL	VALUE	COMMENTS
R-501	10 kΩ	1/2 watt
R-502	10 kΩ	1/2 watt
R-503	1 kΩ	1/2 watt
R-504	1 kΩ	1/2 watt
R-505	4.7 kΩ	1/4 watt
R-506	4.7 kΩ	1/4 watt
R-507	33 Ω	1 watt
R-508	33 Ω	1 watt
R-509	33 Ω	1/2 watt
R-510	1.5 kΩ	1/2 watt
C-501	22 µF	35 v
C-502	22 µF	35 v
C-503	120 pF	1000 v
C-504	120 pF	1000 v
C-505	0.1 µF	100 v
C-506	0.1 µF	100 v
L-501		Ferrite Bead
L-502		Ferrite Bead
CR-501 thru CR-504	1N914 A	

ACTIVE FILTER PARTS LIST

SYMBOL	VALUE	COMMENTS
R-601	1 kΩ	1/2 watt
R-602	107 kΩ	1/4 watt, 1%
R-603	53.6 kΩ	1/4 watt, 1%
R-604	21 kΩ	1/4 watt, 1%
R-605	10.7 kΩ	1/4 watt, 1%
R-606	5.36 kΩ	1/4 watt, 1%
R-607	2.1 kΩ	1/4 watt
R-608	1.0 kΩ	1/2 watt
R-609	158 kΩ	1/4 watt, 1%
R-610	158 kΩ	1/4 watt, 1%
R-611	80.6 kΩ	1/4 watt, 1%
R-612	80.6 kΩ	1/4 watt, 1%
R-613	31.6 kΩ	1/4 watt, 1%
R-614	31.6 kΩ	1/4 watt, 1%
R-615	15.8 kΩ	1/4 watt, 1%
R-616	15.8 kΩ	1/4 watt, 1%
R-617	8.06 kΩ	1/4 watt, 1%
R-618	80.6 kΩ	1/4 watt, 1%
R-619	3.16 kΩ	1/4 watt, 1%
R-620	3.16 kΩ	1/4 watt, 1%

ACTIVE FILTER PARTS LIST (continued)

SYMBOL	VALUE	COMMENTS
R-621	226 kΩ	1/4 watt, 1%
R-622	226 kΩ	1/4 watt, 1%
R-623	113 kΩ	1/4 watt, 1%
R-624	113 kΩ	1/4 watt, 1%
R-625	45.3 kΩ	1/4 watt, 1%
R-626	45.3 kΩ	1/4 watt, 1%
R-627	22.6 kΩ	1/4 watt, 1%
R-628	22.6 kΩ	1/4 watt, 1%
R-629	11.3 kΩ	1/4 watt, 1%
R-630	11.3 kΩ	1/4 watt, 1%
R-631	4.53 kΩ	1/4 watt, 1%
R-632	4.53 kΩ	1/4 watt, 1%
C-601	0015 µF	600 v
C-602	0014 µF	600 v
C-603	470 pF	1000 v
C-604	200 pF	1000 v
IC-601	LM302	
IC-602	LM302	

VOLTAGE REGULATOR PARTS LIST

SYMBOL	VALUE	COMMENTS
R-701	68 Ω	1/2 watt
R-702	150 Ω	1/2 watt
R-703	150 Ω	1/2 watt
R-704	68 Ω	1/2 watt
R-705	68 Ω	1/2 watt
R-706	68 Ω	1/2 watt
R-707	150 Ω	1/2 watt
R-708	150 Ω	1/2 watt
C-701	0.1 µF	100 v
C-702	500 µF	30 v
C-703	0.1 µF	100 v
C-704	500 µF	30 v
C-705	0.1 µF	100 v
C-706	500 µF	30 v
C-707	0.1 µF	100 v
C-708	500 µF	30 v
CR-701	15 v	ZENER, 400 mw
CR-702	15 v	ZENER, 400 mw
CR-703	20 v	ZENER, 1 watt

VOLTAGE REGULATOR PARTS LIST (continued)

SYMBOL	VALUE	COMMENTS
CR-704	20 v	ZENER, 1 watt
Q-701	2N5461	FET
Q-702	2N5461	FET
Q-703	2N3713	
Q-704	2N3053	
Q-705	2N4400	
Q-706	2N4402	
Q-707	2N4890	
Q-708	2N3713	
Q-709	2N5461	FET
Q-710	2N5461	FET
Q-711	2N3713	
Q-712	2N3053	
Q-713	2N4400	
Q-714	2N4402	
Q-715	2N4890	
Q-716	2N3713	

CARRIER TRAIN PARTS LIST

SYMBOL	VALUE	COMMENTS
R-801	51 Ω	1/2 watt
R-802	200 Ω	Pot., 10-turn
R-803	2.5 kΩ	Pot.
R-804	1.5 kΩ	1/2 watt
R-805	4 kΩ	1/4 watt
R-806	39 kΩ	1/4 watt

APPENDIX C

DIAGRAMS

OF THE

PULSE-WIDTH-MODULATED

SIGNAL GENERATOR

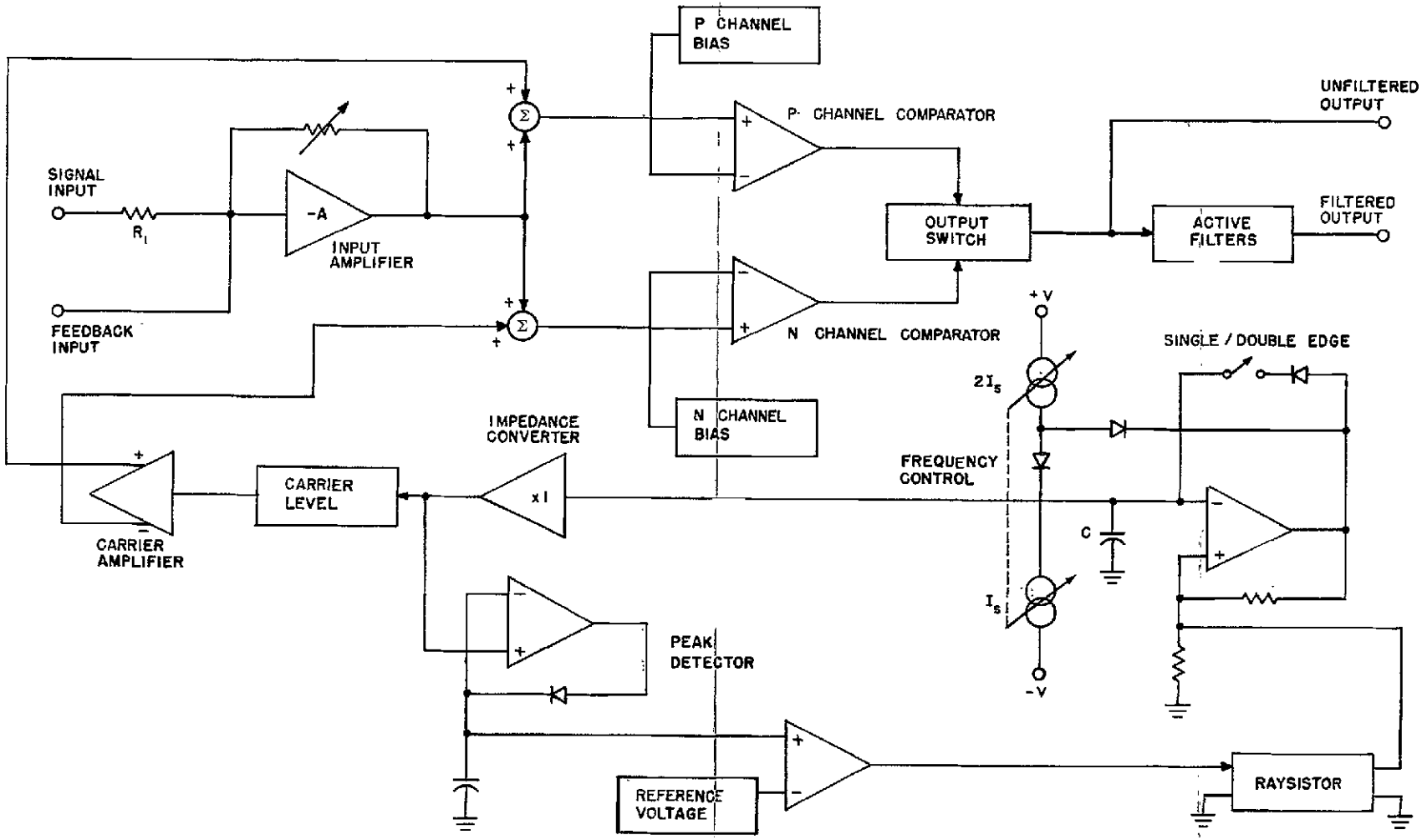

Fig. 30. Complete Block Diagram

FOLDOUT FRAME

FOLDOUT FRAME

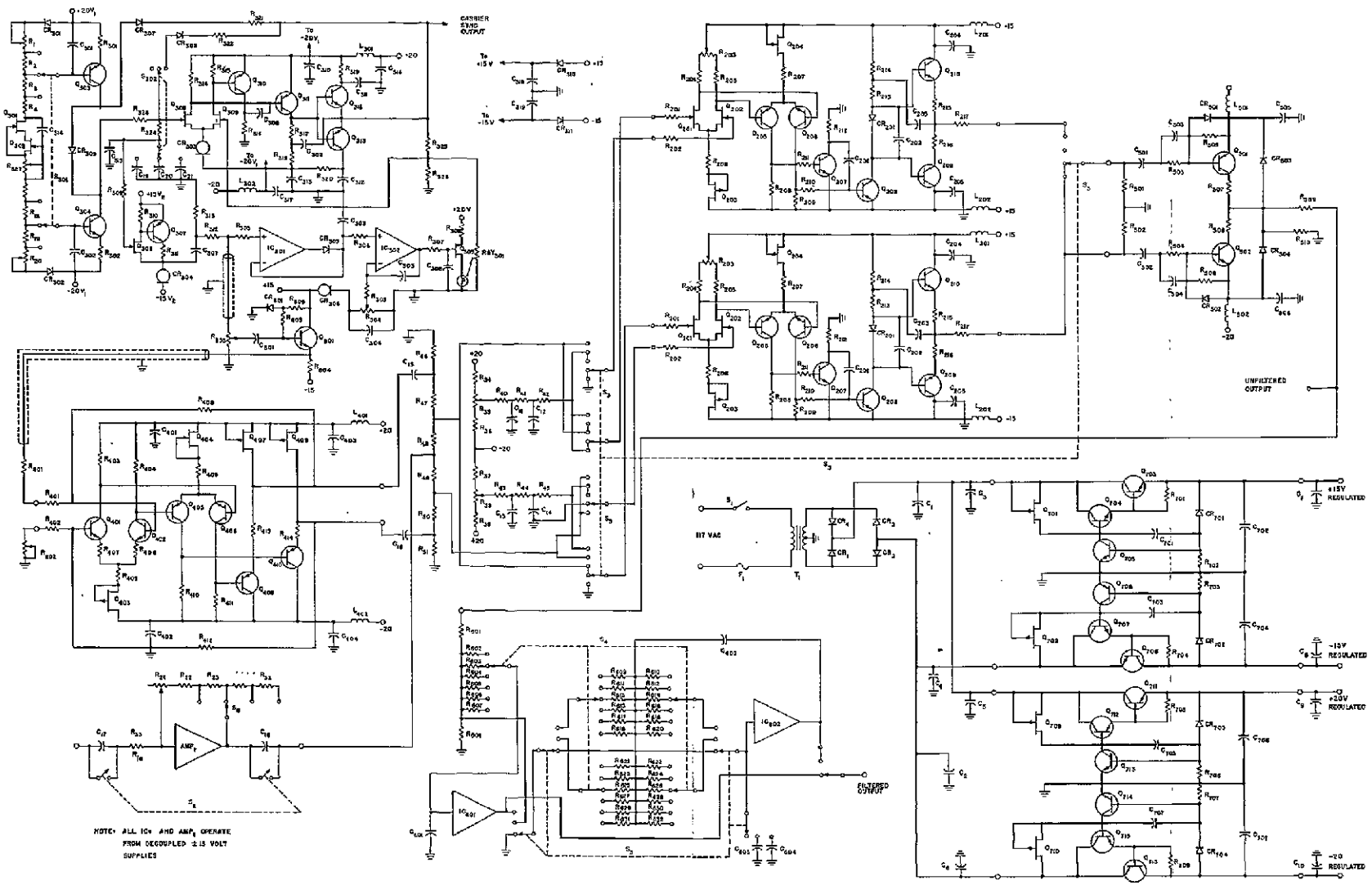

Fig. 31. Complete Schematic Diagram

FOLDOUT FRAME

FOLDOUT FRAME 2