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DEVELOPMENT AND EVALUATION OF A HIGH-EFFICIENCY POWER INVERTER

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16. Abstract

After a brief review of state-of-the-art power conversion techniques, a design and design methods are presented to derive a high-efficiency solid-state inverter in the range of 2 to 5 kilowatts. Complementary transistor circuits are used in all logic. The resulting power matrix configuration is scrutinized for major failure modes. The resulting inverter matrix is further improved by the application of special circuits that reduce the transient effects of the switching elements. A final evaluation is presented, and efficiency curves are plotted over a wide load range.

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SUMMARY

With efficiency as the prime requisite, a power inverter was designed and evaluated. A critical review of state-of-the-art supporting circuitry was conducted by using complementary transistor logic techniques. Since failure modes were of prime concern, the results of circuit tests under the influence of a variety of loads are reported. Transient suppression was shown to be a major problem, and a circuit to suppress the transient effects on the commutation of the inverter matrix is presented. Efficiency was both measured and calculated, and a critical review of the effort is presented.

INTRODUCTION

The term "inverter" is used to describe a device that converts dc voltage or power to ac voltage or power. In most practical applications, however, ac voltage is available at an undesired frequency. For this study, an ac source was assumed, and some of the decisions made early in the study were influenced by this assumption.

Most commercially available inverters employ transistors as the power control elements. If the desired output voltage is higher than transistor operating specifications allow, an output transformer is used. Generally, the output transformer is also employed as a feedback and tuning device to control output frequency. Inverters of this type seldom achieve efficient operation in excess of 50 to 60 percent. In order to increase the efficiency of the inverter, power dissipating elements, such as resistors and transformers, must either be eliminated or changed and the overall philosophy altered. Removal of the output transformer necessitates a new frequency control and a higher working voltage for the power control elements. Higher working voltage makes the transistor less desirable for this purpose, and the consideration of another switching element is in order. The

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silicon-controlled rectifier (SCR) is the obvious replacement as it has higher gain, current, and voltage ratings than the power transistor. The design presented is, therefore, a transformerless SCR matrix.

SYMBOLS AND ABBREVIATIONS

A,B,C,D	Boolean variables or flip-flop outputs
b	base (transistor)
C	capacitance or capacitor
D	diode
e	emitter
FF	flip-flop
f_c	natural frequency of commutating components
G	gate or gate pulse
g(X),h(X)	parametric functions of X
I	steady-state value of current
i	instantaneous current
L	inductance or inductor
N	NOR gate
P	power
P_c	commutating power loss
P_d	driver-amplifier power loss
P_l	logic-circuit power loss

P_p	peak power
Q	transistor
R	resistance or resistor
R_b	base resistor
SCR	silicon-controlled rectifier (thyristor)
T	transformer
t	time
t_o	time interval
UJT	unijunction transistor
V	voltage
W	energy
X	ratio of currents
Z	impedance
τ	time constant
ω	angular velocity

Subscripts:

c	commutation
i	di/dt protection
L	load
max	maximum

min	minimum
rms	root mean square
SCR	silicon-controlled rectifier
t	timing
v	dV/dt protection

A prime refers to a three-phase configuration.

DESIGN CONSIDERATIONS

Waveform

Although a sinusoidal waveform would be the most desirable for the variety of loads that might normally be encountered, it is certainly not the only useful waveform. The development of a sinusoidal wave might well be complex and expensive and result in an unnecessary loss in system efficiency. The prime use for ac power is for motor loads, and the selection of 400 Hz as the power frequency was influenced by existing hardware technology at that frequency.

Test data (ref. 1) have shown that the loss in efficiency of a motor operating with a square or quasi-square wave input, rather than a sine wave input, can be held to only 3 to 5 percent. The loss is dependent upon motor design and the dwell angle of the waveform. Dwell angle is defined as the period between the positive and negative parts of the wave, as illustrated in figure 1. The results of dwell-angle variation upon harmonic content of the quasi-square wave, which can be readily calculated by using Fourier series, is shown graphically in figure 2 (ref. 2). Harmonic content of a wave plays an important role in the production of torque. Harmonic currents in polyphase induction motors may produce forward rotating fields (in the same direction as the fundamental), backward rotating fields, or stationary pulsating fields, depending upon the order of the harmonic. The torquing effects of harmonics are shown in table 1. Since a square wave contains no even harmonics and, as can be seen in figure 2, the third harmonic can be eliminated with a 60° dwell angle, this quasi-square wave is a good choice for motor loads. In the analysis of any waveform for possible use as an output phase-to-neutral voltage, the resulting phase-to-phase voltage wave must also be considered. If the square wave of figure 1(a) is produced from phase-to-neutral, the resultant phase-to-phase voltage will be a quasi-square wave with 60° dwell angle. If the phase-to-neutral waveform is instead the quasi-square wave of figure 1(b), the phase-to-phase resultant is a six-step wave.

The latter waveforms (fig. 1(b)), whereas only slightly more complicated to produce, offer significant advantages. A three-phase output using a square wave, if produced by switching from a dc source, presents an uneven loading on that source. Also, any single-phase loads are subject to all the odd harmonics present in the square wave. On the other hand, the three-phase quasi-square wave of figure 1(b) results in a continuous sequential power demand from the dc source and presents essentially the same harmonics to both single-phase and three-phase loads. While it is obvious that the more steps there are in a quasi-square waveform, the more closely it may approximate a sine wave, it should also be realized that more steps require more complex control and switching circuitry. The quasi-square wave with a 60^{o} dwell angle, developed as a phase-to-neutral voltage, has significant advantages with minimum complexity to justify its use.

Inverter Configuration

In general, an SCR inverter is described by the commutation method employed. The term "commutation" is used to denote the transfer of current from one conducting element to another in rectifier or SCR circuits. Generally, commutation involves a series of events which may occur concurrently or in sequence. Providing for reliable commutation is the most difficult design problem and is dealt with in many publications. The commutation method depends to some extent on the configuration of the inverter conducting elements and in many cases on the load.

Since efficiency is of prime concern, minimizing the number of power absorbing elements in the main current path is desirable. The efficiency of the power handling section of the inverter is a function of voltage drop and the rms current. The voltage drop across an SCR is nominally 1.2 volts and is reasonably independent of current. Because the current is the controlling parameter, a higher supply voltage results in a lower current for a given power level, and therefore, a higher efficiency is effected for a given load.

The most efficient configuration with the above points in mind would be direct rectification of the ac source to a high-voltage dc bus. Both a positive and negative bus thus obtained can then be switched to the load alternately. (See fig. 3.) Thus, both input and output transformers have been eliminated, energy storage can be provided at the dc busses, and transients created by the switching process are buffered from the ac supply. These requirements are met by the three-phase McMurray inverter of figure 4, which requires no starting circuitry, no output transformer, and an absolute minimum of dissipative elements in series with the load. Commutation is accomplished by an impulse of current to the load which briefly reverses the voltage on the conducting SCR and allows it to turn off. The impulse is formed by an inductance-capacitance (L-C) network. The remainder of this paper is devoted to this circuit.

When the load is reactive, the feedback diodes D1 and D2 conduct during part of each half-cycle to return power from the load to the dc supply. Refer to the phase A section of figure 4, and assume that power has just been applied and that C_C has no initial charge. The controlled rectifiers SCR2 and SCR3 are gated on, and current flows from the dc supply to the load and charges C_C. As C_C becomes charged, the current through SCR2 will decrease until it is below the value necessary to maintain conduction of the device, and SCR2 will cut off. In order to commutate SCR3 off, SCR1 is fired. The discharge current pulse through SCR1, C_C, and L_C builds up to exceed the load current and the current through SCR3 diminishes to zero. The excess commutating current flows through the feedback diode D1 to the dc supply. A charge of reverse polarity is built up on C_C, and the forward voltage drop of D1 appears as inverse voltage across SCR3 and turns it off. To obtain the negative half-cycle, SCR1 and SCR4 are fired, and current flows from the negative dc supply to the load. The controlled rectifier SCR4 is commutated by the firing of SCR2 and the action of the L-C circuit as described above. To provide the commutation energy, the following energy balance equation (ref. 3) must be evaluated:

$$\frac{1}{2} CV^2 = \frac{1}{2} LI^2 \tag{1}$$

The amount of current that can be commutated is

$$I = V\sqrt{\frac{C}{L}} \tag{2}$$

The time constant that must be considered is

$$\tau = 2\pi\sqrt{LC} \tag{3}$$

Since the circuit will supply power to motors, the inductance of the motor will enter into the time constant of the commutation circuit. From equation (2), it is obvious that an increase in L reduces the current that can be commutated. If C is increased to compensate for the increase in L, the time constant may become excessively long.

The Silicon-Controlled Rectifier

When first introduced, the silicon-controlled rectifier was heralded as the answer to many problems in power switching and control. In practical applications the device has two major failings, both of which are termed "rate effect." Either of these rate effects, if not considered in either the device construction or the circuit design or both, can cause failure of the device or the circuit.

The first of the rate effect parameters is the current rate, or the di/dt rating. Even though a particular SCR may have a rated maximum direct-current carrying

capability of several amperes, the device can be destroyed at much lower values. When a gate signal is applied, the gate-cathode junction becomes forward biased, and the buildup of current takes place. The junction bias change results from carriers being injected through the gate lead. A finite amount of time is required for the entire junction to be affected by the injected carriers. The change in potential spreads across the junction from the gate lead connection. If the anode-to-cathode current builds up too rapidly before the complete cathode junction becomes forward biased, the current density in the immediate vicinity of the gate lead connection becomes excessive. Localized heating caused by high current density results in destruction of the junction.

The second rate effect parameter is referred to as the dV/dt characteristic. It is possible to force an SCR into a conducting state by rapid application of voltage without exceeding the forward blocking voltage. This parameter is measured with the gate open-circuited, and if the circuit configuration is such that the cathode of the SCR is connected to a fixed voltage point such as a dc bus or ground, the dV/dt rating has meaning. The rating is meant to denote the maximum rate at which forward voltage can be applied. There are many circuit configurations for which the dV/dt rating is misleading, and the McMurray inverter is such a circuit. Several SCR manuals circulated by manufacturers describe a negative gating technique wherein the device is gated into conduction by driving the cathode negative with respect to the gate, as opposed to the more popular concept of a positive pulse to the gate lead with respect to the cathode. Each of the SCR's in the McMurray configuration has a cathode connection other than system ground. (See fig. 5.) The controlled rectifier SCR1 is connected at point I, the potential of which varies with the output waveform. The cathode of SCR3 is the output terminal, and the cathodes of SCR2 and SCR4 are connected to the negative dc bus. The gating signals, however, are developed with respect to the system ground and, therefore, must be coupled to the SCR's through pulse transformers. This transformer connection from gate to cathode places the SCR in the general configuration for negative gating, which can occur through normal action of the circuit. The controlled rectifiers SCR1 and SCR3 can be negative gated by the normal conduction of SCR2 and SCR4, respectively. The controlled rectifiers SCR2 and SCR4 can be negative gated upon initial application of the negative dc bus voltage to the SCR matrix. Hence, although the voltage changes at points I and II may not exceed the dV/dt rating of the SCR, negative gating can occur and the consequences are the same. Under the conditions described, negative gating will occur if the dc bus voltages are sufficiently high. Even if the more advanced SCR designs are employed in the circuit, negative gating can occur at dc working voltages of 80 to 100 volts. Negative gating protection is discussed in a subsequent section.

The inductors L_i of figure 5 limit the di/dt of each controlled rectifier to an acceptable value for the device. The diodes D_i provide a path for reactive current for each inductor.

The resistance-capacitance (R-C) network across each SCR serves as dV/dt protection. A good approximation for C_V can be calculated as follows (ref. 2):

$$\tau = \frac{0.632 \times \text{Rated SCR voltage}}{\text{dV/dt capability}} \tag{4}$$

The time constant τ should be chosen so that

$$\tau = R_L C_V \tag{5}$$

The damping resistor R_V should be selected on the basis of limiting the peak capacitor discharge current during the SCR turn-on interval to a value within the capability of the device. For best results, the network should be placed in proximity to the SCR to minimize inductive effects.

Logic

A basic logic circuit that combines high efficiency, low output impedance, and fast transition times can be constructed by using complementary transistors. The switch of figure 6 uses a complementary p-n-p transistor as a variable collector resistance for the control transistor Q1. This circuit can drive loads returned either to ground or to the supply voltage. When a positive signal is applied to the input, transistor Q1 saturates and pulls the output to ground while the same input cuts off Q2. Since Q2 is open-circuited, no power is drawn from the supply. For a negative or zero input, the states of Q1 and Q2 are reversed. Transistor Q2 is saturated and delivers full power to the load while no power is lost in the cutoff transistor Q1. Theoretically the power-transfer efficiency of this circuit is 100 percent. In practice, values above 90 percent can be obtained.

The basic concept illustrated can be extended to provide a variety of logic circuits. Figure 7 shows a complementary transistor flip-flop, with a conventional steering circuit, designed for use with a 28-volt supply. The inherent low output impedance permits the system logic level to remain constant with a wide load variation. These circuits are extremely tolerant of leakage currents. If the OFF transistor is not turned off completely, the ON transistor has only to conduct that much more current. It is, therefore, possible to design circuits of this type with no reverse-bias supply. The only power losses are in the base drive circuit and the collector saturation voltage drop, both of which are small compared with output capability.

DEVELOPMENT

Logic

The following procedures are aimed at the design of a system of logic to provide the necessary gating signals for the SCR matrix. The desired inverter output is three phases of quasi-square waves 120^{o} apart at a frequency of 400 Hz. As can be seen in figure 8, the minimum number of separate timing pulses needed in one 400-Hz time period is six. Digital techniques are easily employed to count down from a reference oscillator and to gate the proper SCR at the desired time.

The unijunction transistor (UJT) relaxation oscillator of figure 9 is simple and efficient. The circuit has excellent temperature stability and low power dissipation. Design procedures can be extracted from various texts. (See ref. 4.)

A UJT oscillator and flip-flop comprise the system clock whose output is 6×400 Hz and represents the binary "one." These pulses are fed to a train of three flip-flops which are connected to divide by 6. The Boolean expressions for the pulses t_1 to t_6 can be written directly from the diagram in figure 8 and are presented in the appendix.

The logic diagram is shown in figure 10. The NOR gates are utilized to provide sufficient isolation from and current drive to the gate amplifiers.

Gate Amplifiers

The requirements of the SCR gate circuit are dictated by the type of SCR employed. In order to conserve power, the gate pulse should be of short duration. The controlled rectifiers SCR1 and SCR3 (fig. 5) are positioned in the circuit so that their cathode potentials are of changing polarity, and the cathodes of SCR2 and SCR4 are connected to the negative supply voltage. Isolation from the logic circuitry is provided by pulse transformers. If negative gating or dV/dt breakdown is allowed to occur, a short circuit is created from the positive supply to the negative supply through two SCR's.

To prevent negative gating, another SCR can be connected in the secondary of the pulse transformer, and the blocking characteristic is used to provide an effective open circuit unless a trigger pulse is applied from the logic. The gate amplifier of figure 11 provides isolation and blocking for the negative gating phenomenon. The square pulse on the input appears as a short positive spike on the secondary of T1 to provide a gate potential for the blocking SCR. At the same time, T2 provides anode voltage across the blocking SCR and current to the gate lead of the power SCR and can provide any width pulse desired, up to the width of the input logic signal. To any cathode transients, the gate is an open circuit.

Commutation

In order to provide adequate commutation, the commutation current must exceed the load current I_L for an interval of time t_o which is longer than the turn-off time of the SCR. Three alternate commutation pulse shapes are shown in figure 12. (See ref. 3.) The parameter X is the ratio of the maximum current to be commutated I_{max} to the load current I_L. The maximum current to be commutated must be considered to be the peak current that can occur during any half-cycle of operation. When motors are to be started, this current can be high when compared with the current drawn when the motor is running at rated speed. For resistive loads, the maximum load current to be commutated is

$$I_L = \frac{P_p}{V_{min}} \tag{6}$$

where

P_p peak instantaneous power output

V_{min} minimum supply voltage

The dc voltage necessary to supply 115 volts rms to the load by using a quasi-square wave with a 60^o dwell angle is approximately 141 volts.

The optimum commutating pulse is the one which requires the least energy. For the analysis which follows (ref. 3), the commutating circuit is assumed to have low losses so that these losses may be neglected. From figure 12

$$I_L = I_{max} \cos \omega t \tag{7}$$

where $t = \frac{t_o}{2}$ or

$$\cos \frac{\omega t_o}{2} = \frac{I_L}{I_{max}} = \frac{1}{X} \tag{8}$$

where

$$\omega = \frac{1}{\sqrt{L_c C_c}} \tag{9}$$

Therefore, by substituting equation (9) into equation (8)

$$\frac{t_o}{\sqrt{L_c C_c}} = 2 \cos^{-1} \frac{1}{X} \equiv g(X) \tag{10}$$

The energy W that must be supplied by the commutating circuit to accomplish SCR turn-off is

$$W = \frac{1}{2} C_c V_c^2 \tag{11a}$$

or

$$W = \frac{1}{2} L_c I_{max}^2 \tag{11b}$$

Multiplying equations (11a) and (11b) gives

$$W = \frac{1}{2} V_c I_{max} \sqrt{L_c C_c} \tag{12}$$

By substituting equations (8) and (10) into equation (12)

$$W = \frac{1}{2} \left(\frac{t_o}{2 \cos^{-1} \frac{1}{X}} \right) V_c I_L X \tag{13}$$

By expressing equation (13) as a function of X

$$\frac{W}{V_c I_L t_o} = \frac{X}{4 \cos^{-1} \frac{1}{X}} \equiv h(X) \tag{14}$$

The functions $g(X)$ and $h(X)$ are plotted in figure 13. (See ref. 3.) When $X = 1.5$, $h(X)$, a function of the commutating energy W, is at a minimum value of 0.446. The value of $g(X)$ at this point is 1.68. To determine the values for the commutating circuit components, the values of V_c, I_L, t_o, and X pertaining to the maximum load and minimum supply voltage must be used. By combining equations (11) and (13), the required values of C_c and L_c are

$$C_c = \frac{X}{g(X)} \frac{I_L t_o}{V_c} = 0.893 \frac{I_L t_o}{V_c} \tag{15}$$

$$L_c = \frac{1}{X\, g(X)} \frac{V_c t_o}{I_L} = 0.397 \frac{V_c t_o}{I_L} \tag{16}$$

By using the optimum values for the numerical constants

$$X = 1.5 \tag{17}$$

$$g(X) = 1.68 \tag{18}$$

The natural frequency of the commutating circuit is

$$f_c = \frac{1}{2\pi \sqrt{L_c C_c}} = \frac{g(X)}{2\pi\, t_o} = \frac{0.267}{t_o} \tag{19}$$

and the pulse width is

$$\pi\sqrt{L_c C_c} = \frac{\pi t_o}{g(X)} = 1.87t_o \tag{20}$$

RESULTS

Operational evaluation of the circuit illustrated in figure 5 led to several conclusions. The rapid turn-on and turn-off times of the SCR's produced a square wave with steep sides. The results of this fast switching, aside from a nearly perfect quasi-square output waveform, were some adverse transient conditions within the circuit matrix. These transients, due to the normal switching operations, produced extremely short voltage rise times (dV/dt), current buildup (di/dt), and false gating signals. Without protective networks, operation was limited to dc supply voltages in the range of ±50 volts, even though the best available SCR's were employed. Even at this limited voltage, operation was sensitive to load changes and turn-on sequences involving supply voltage application and logic.

Two types of circuit failures were considered. The first was the simultaneous conduction of two series-connected SCR's and resulted in the activation of supply current limiting devices, such as fuses or circuit breakers. The other was the destruction of an SCR from di/dt burnout. Other failures were not considered as it was realized that random failures and the prevention thereof are not within the scope of this work. Hence, the term "failure" is only used to indicate one of the two prevalent types described.

Rate Protection

Since square voltage waveshapes were present at nearly every point in the inverter, di/dt failure was always possible. To protect the SCR's against di/dt failure, a small inductance was connected in series with the device. A value was approximated by using the maximum supply voltage and the di/dt rating of the device.

Breakdown failure, which occurs when two series SCR's conduct simultaneously, can be the result of dV/dt breakdown of one SCR due to the turn-on of a series SCR. The use of R-C networks connected in parallel with each device effects a softening of dV/dt. To operate successfully in the ±150-volt range, a minimum capacitance in the range of 0.5 μF was required. The current limiting resistor also became large, and the overall result was a considerable dissipation of power. If circuit efficiency is of little concern, this power loss may be tolerated. For the application discussed herein, the loss of 30 to 40 watts could not be justified.

Before dV/dt protection is used, the cause of breakdown should be pinpointed. This can be done by triggering the SCR's manually in the proper sequence with all gate leads open except for the SCR being triggered. If a failure does not occur, dV/dt

breakdown can be ruled out as a failure mode, and the R-C protective networks may be omitted. In this application, a dV/dt rating of 200 V/μsec proved to be sufficient to prevent dV/dt breakdown at working voltages up to ±200 volts dc.

Negative Gating

Even though dV/dt breakdown was shown to be absent, high dV/dt was still the major problem in the circuit because it produced negative gating signals. These false gating signals were the result of a negative SCR (SCR connected to negative dc bus) being triggered into conduction and thereby connecting either point I or point II (fig. 5) to the negative supply bus. Since the gate circuits of the positive SCR's were transformer coupled to the trigger amplifiers, the gate-to-cathode impedance was such as to allow this transient, negative-going cathode voltage to be interpreted as a gating pulse. A similar condition existed for the negative SCR's at the moment of application of dc power.

In order to have any degree of stable and reliable operation, the transient effects had to be blocked or reduced drastically. The blocking pulse gate amplifier was designed to utilize the blocking characteristics of one SCR in order to open-circuit the gate lead of the power SCR effectively. (See fig. 11.) The blocking SCR was selected for high dV/dt capability and low maximum average current capacity. The latter parameter was necessary in order to minimize junction capacitance. The pulse leakage was thereby held to a low value. The leakage pulse amplitude was proportional to the transient amplitude and rise time, as well as the total p-n junction capacitance. If care is taken in the selection of the blocking SCR, the amplifier of figure 11 can improve the maximum allowable matrix supply voltage from 3 to 5 times that possible with conventional transformer coupling.

Efficiency

While the inverter design has taken into account various load conditions, overall efficiency was measured at unity power factor. Efficiency measurements were taken for the single-phase configuration and were projected for the three-phase configuration. The power consumed by the logic and gate amplifiers was taken into account, but it should be noted that R_V and C_V, as shown in figure 5, were removed. Table 2(a) shows the measurements taken from the single-phase configuration at five output levels. The power dissipated by the logic P_l is constant and is the same for single-phase and three-phase operation. Power loss from the SCR is a function of the nearly constant voltage drop across the device and the current through it. This loss will triple for the three-phase calculation. Power consumption in the driver circuits P_d will also triple. The remaining losses are due to the increase in commutation energy P_c and protection-device loss. This figure will also triple. In general, table 2 shows the breakdown of various component losses. The total loss can be approximated by

$$\Delta P = P_{in} - P_{out} = P_l + P_d + P_{SCR} + P_c \tag{21}$$

A set of curves can now be calculated for the three-phase inverter by using the values in table 2(a).

$$\Delta P' = P_l + 3P_d + 3P_{SCR} + 3P_c \tag{22}$$

$$\text{Efficiency} = \frac{P_{out}}{P_{out} + \Delta P} \tag{23}$$

Figure 14 is the result of measurements taken on the single-phase inverter. From these values the curves of figure 15 were calculated. A comparison of efficiency for both the single-phase configuration and the three-phase configuration is shown in figure 16.

CONCLUDING REMARKS

The deficiencies of the McMurray inverter circuit configuration are, in fact, deficiencies of the silicon-controlled rectifier (SCR) itself. The SCR is a handy tool and can be reliable when used in applications involving sinusoidal waveforms. The square-wave application serves to bring out the shortcomings and faults inherent to the device. Although there has been a great deal of improvement in SCR's over the past few years, little attention has been given to the gating connection.

Even now, some manufacturers are reluctant to admit that a real problem exists. The user, however, can easily prove to himself that in nearly any application, the gating circuit will require much consideration and protection before reliable operation can be obtained.

If the circuit could be used without excessive protective components, it would be an important contribution to the inverter art. Every extra component dissipates power and increases weight and cost.

The circuit has the following problems:

1. Two principal inherent failure modes which result from characteristics of the silicon-controlled rectifier:

Failure due to current rate
High transients which can produce false gating signals that result in circuit failure

2. Appreciable radiation of energy resulting from step transient conditions

However, problem areas can be reduced by:

1. Employing current rate inductors, which dissipate very little power, in series with each silicon-controlled rectifier

2. The use of blocking devices to improve the characteristics of the external gating circuitry

With proper design, the McMurray inverter can meet the requirements of high efficiency and medium power output. Good reliability can be accomplished only through a large reduction of efficiency. Reliability and efficiency may be increased if the "rate effect" characteristic in the silicon-controlled rectifier can be improved. Even with improved SCR's, the reliability may still be questionable, because of the intolerance of the design to rapid load changes and leading power factor loads, which produce voltage transients and increase the current rate factor.

Langley Research Center,
National Aeronautics and Space Administration,
Hampton, Va., April 30, 1970.

APPENDIX

BOOLEAN DEVELOPMENT OF LOGIC CIRCUITRY

In figure 8 it can be seen that a timing pulse is required for each turn-off of the SCR switches used for the three-phase output. These can most easily be obtained from the direct selection of the logic flip-flop outputs through AND and NOR gates.

$$t_1 = A\overline{B}C\overline{D} = A\overline{BD} \qquad \bar{t}_1 = \overline{A} + B + D$$

$$t_2 = ABC\overline{D} = AB\overline{D} \qquad \bar{t}_2 = \overline{A} + \overline{B} + D$$

$$t_3 = A\overline{BC}D = A\overline{BC} \qquad \bar{t}_3 = \overline{A} + B + C$$

$$t_4 = AB\overline{C}D = AB\overline{C} \qquad \bar{t}_4 = \overline{A} + \overline{B} + C$$

$$t_5 = A\overline{B}CD \qquad \bar{t}_5 = \overline{A} + B + \overline{C} + \overline{D}$$

$$t_6 = ABCD \qquad \bar{t}_6 = \overline{A} + \overline{B} + \overline{C} + \overline{D}$$

From the discussion of the SCR matrix, the pulses required for each gate can be written:

Phase A	Phase B	Phase C
$G_1 = \bar{t}_3 + \bar{t}_4$	$G_5 = \bar{t}_5 + \bar{t}_6$	$G_9 = \bar{t}_1 + \bar{t}_2$
$G_2 = \bar{t}_1 + \bar{t}_6$	$G_6 = \bar{t}_2 + \bar{t}_3$	$G_{10} = \bar{t}_4 + \bar{t}_5$
$G_3 = \bar{t}_1$	$G_7 = \bar{t}_3$	$G_{11} = \bar{t}_5$
$G_4 = \bar{t}_4$	$G_8 = \bar{t}_6$	$G_{12} = \bar{t}_2$

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2. Gutzwiller, F. W., ed.: Silicon Controlled Rectifier Manual. Third ed., Gen. Elec. Co., c.1964.

3. Bedford, B. D.; and Hoft, R. G.: Principles of Inverter Circuits. John Wiley & Sons, Inc., c.1964.

4. Cleary, J. F., ed.: Transistor Manual. Seventh ed., Gen. Elec. Co., c.1964.

TABLE 1.- STARTING TORQUE CHARACTERISTICS OF HARMONICS

Two-phase machine

Torque direction		
Positive	Negative	Zero
Fundamental	3	2
5	7	4
9	11	6
13	15	8
		10
		12

Three-phase machine

Torque direction		
Positive	Negative	Zero
Fundamental	2	3
4	5	6
7	8	9
10	11	12
13	14	15

TABLE 2.- POWER MEASUREMENTS AND CALCULATIONS

(a) Single-phase matrix

Measured					Calculated			
P_{out}, W	P_{in}, W	I_{rms}, A	P_l, W	P_d, W	ΔP, W	P_{SCR}, W	P_c, W	Efficiency, percent
100	118.0	0.87	7.5	7	18.0	1.04	2.45	84.7
200	222.5	1.74	7.5	7	22.5	2.09	5.91	89.9
325	351.6	2.83	7.5	7	26.6	3.40	8.70	92.4
600	635.5	5.22	7.5	7	35.5	6.26	14.7	94.4
1000	1050.4	8.7	7.5	7	50.4	10.4	25.5	95.2

(b) Three-phase matrix
(Calculated from curves)

P_{out}, kW	P_l, W	$3P_d$, W	$3P_{SCR}$, W	$3P_c$, W	ΔP, W	$3P_{in}$, kW	Efficiency, percent
0.3	7.5	21	3.13	7.35	39.0	0.339	88.5
.6	7.5	21	6.26	17.7	52.5	.652	92.0
.975	7.5	21	10.2	26.1	64.8	1.04	93.7
1.8	7.5	21	18.8	44.2	91.5	1.89	95.2
3.0	7.5	21	31.3	76.4	136	3.14	95.7

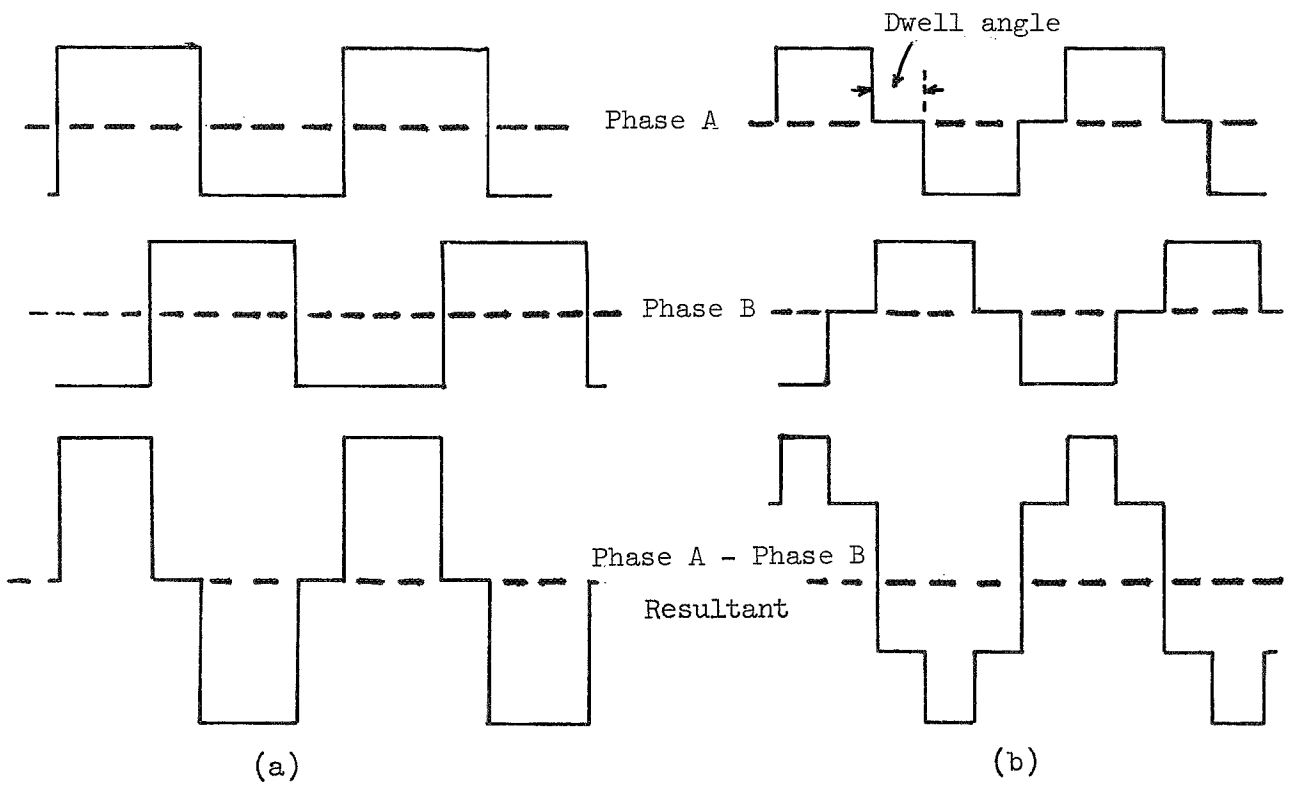

Figure 1.- Square-wave phase relationships.

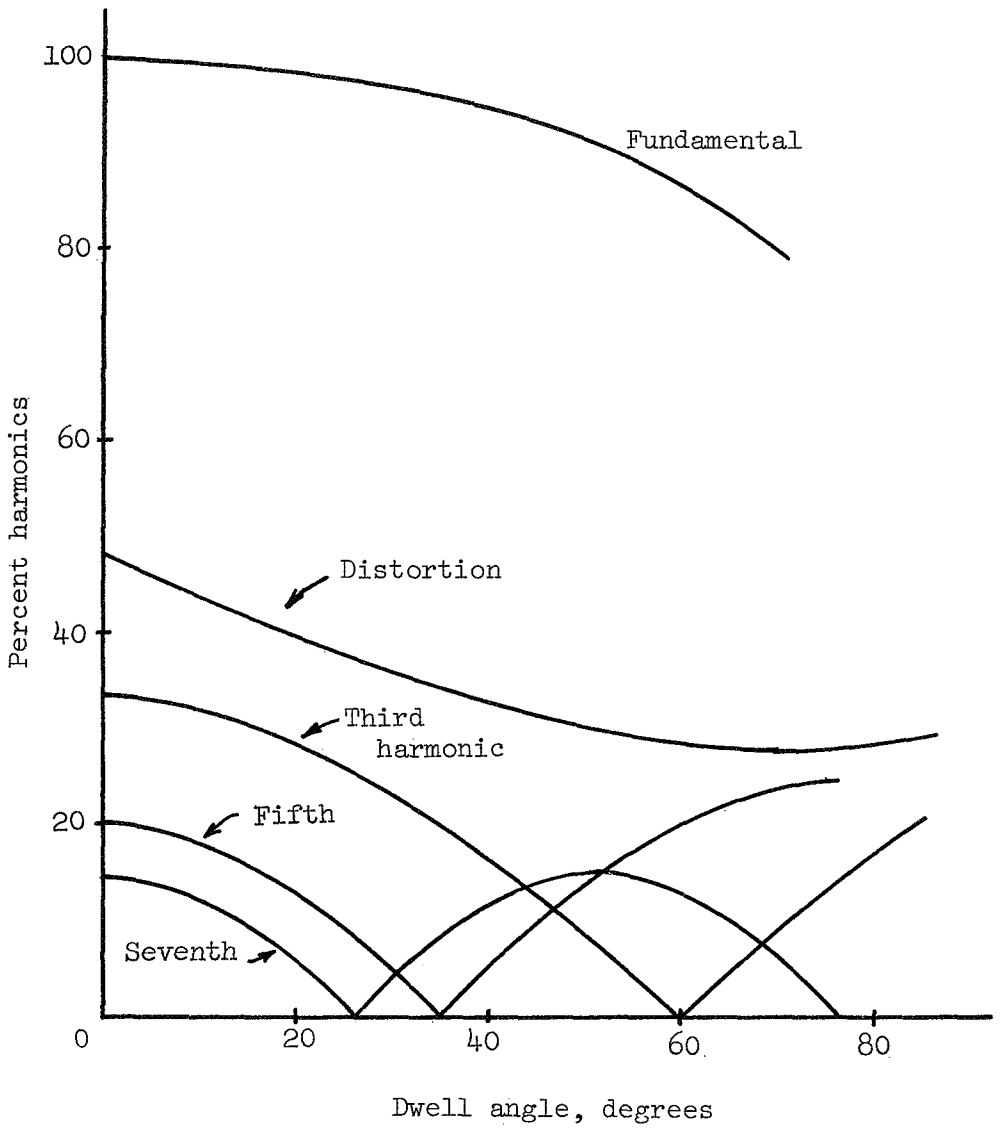

Figure 2.- Harmonic content of quasi-square wave.

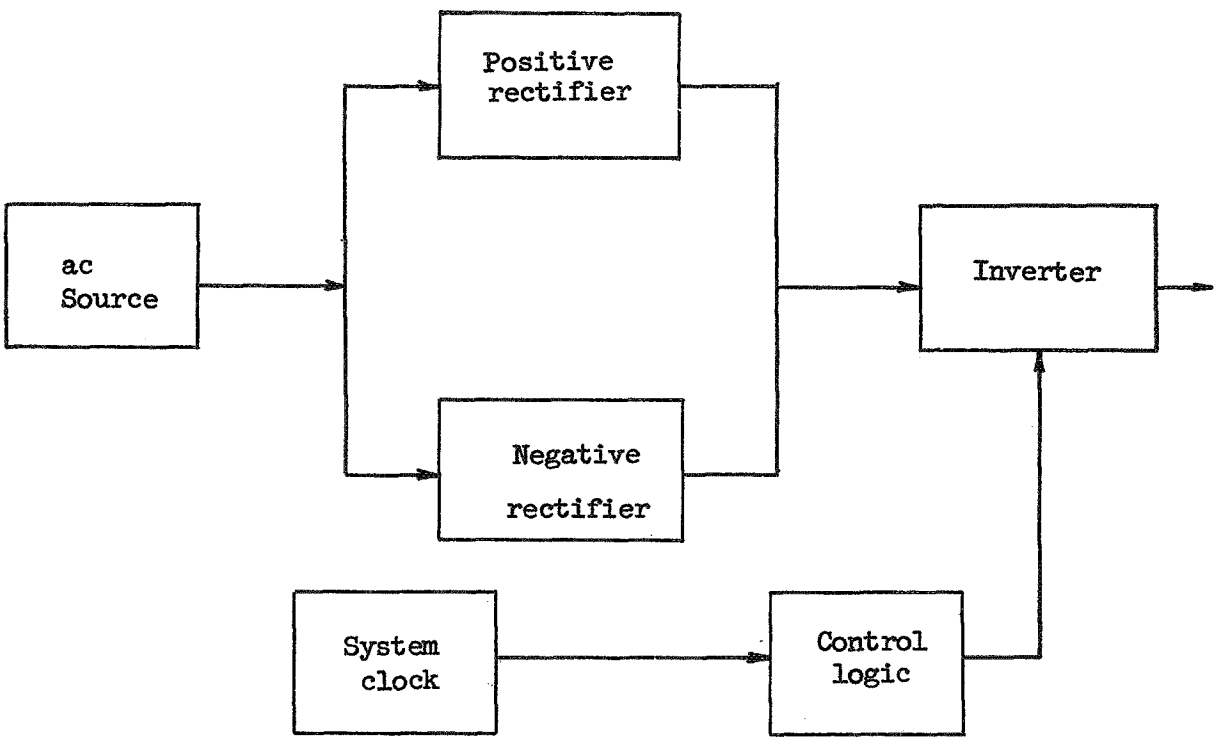

Figure 3.- Block diagram of basic rectifier-inverter system.

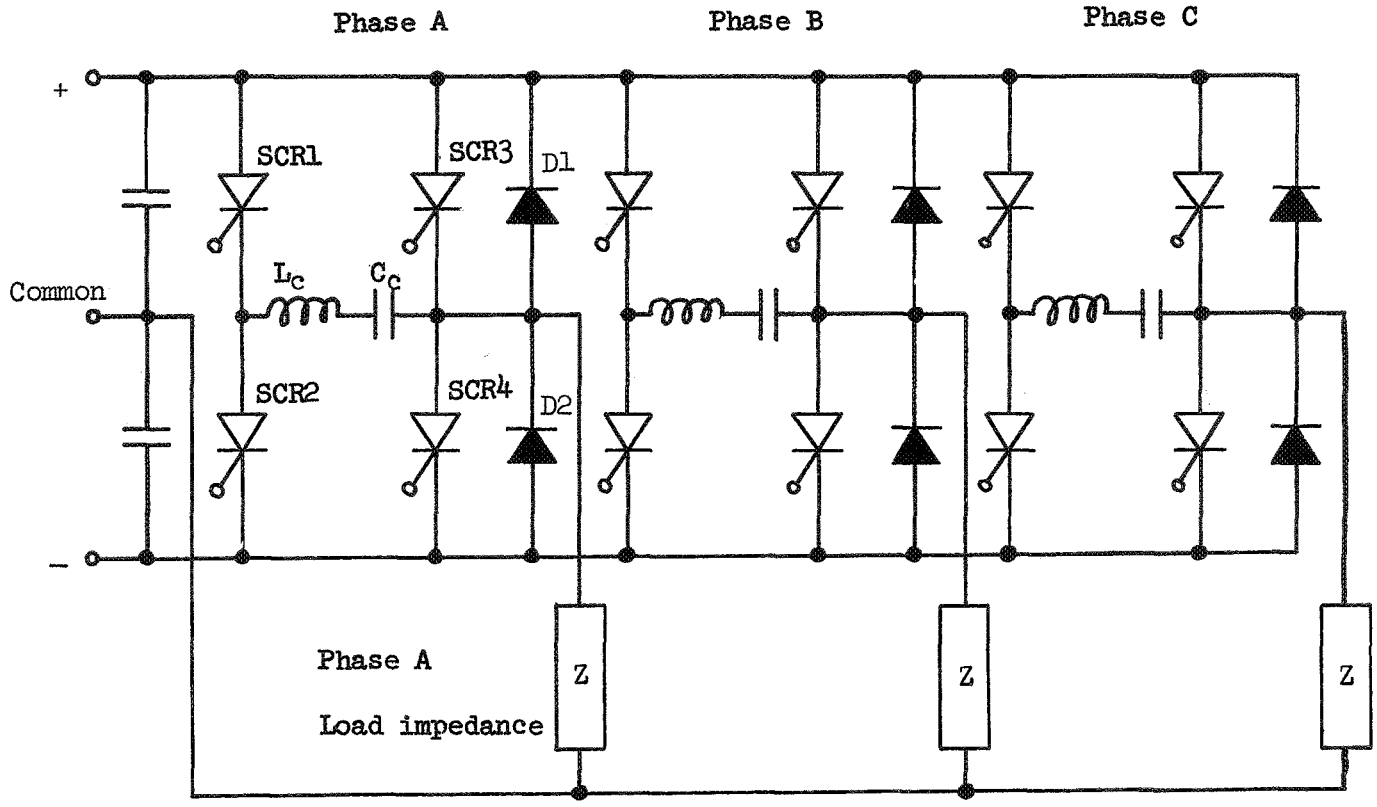

Figure 4.- Three-phase McMurray inverter.

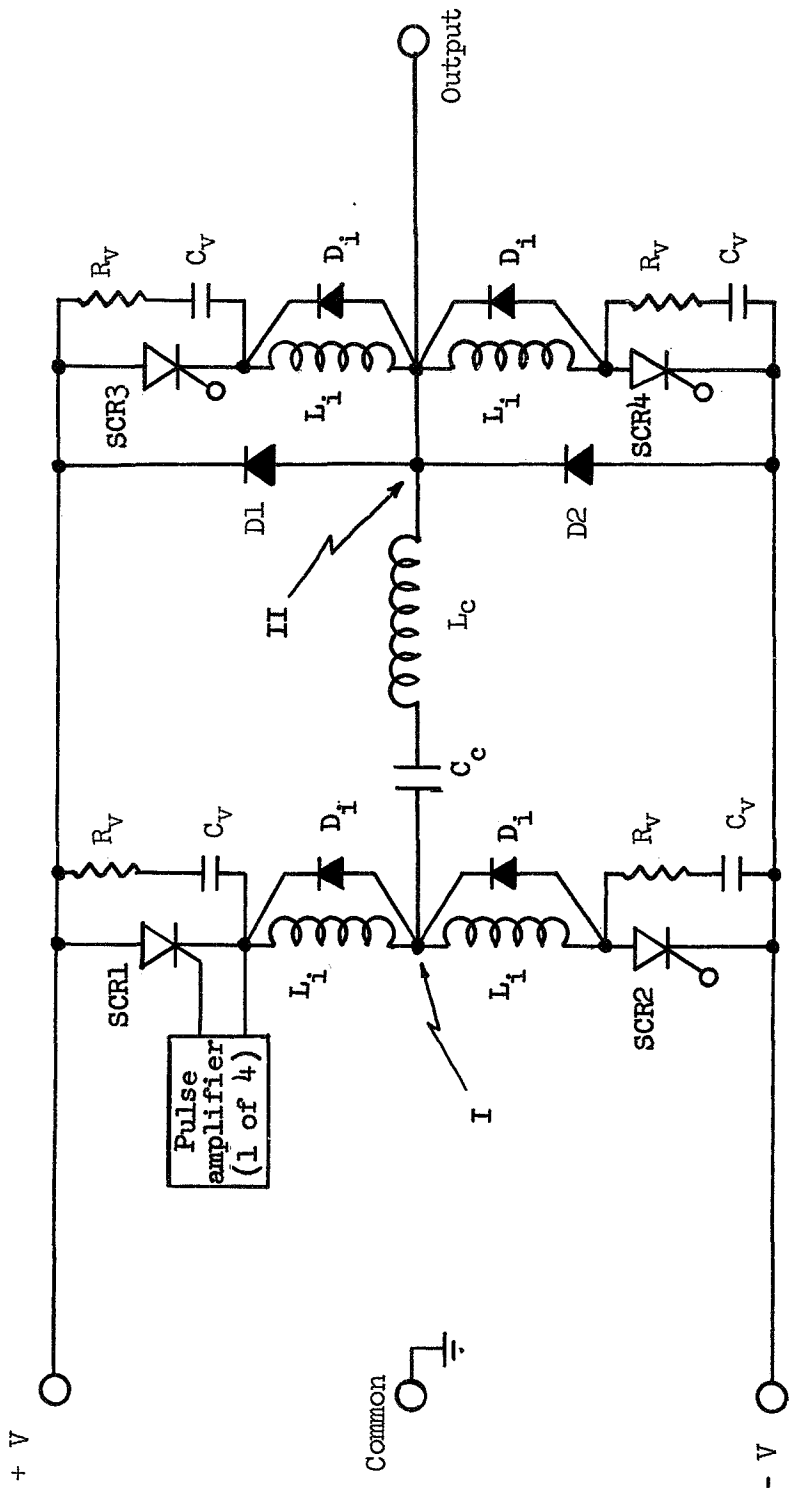

Figure 5.- Single-phase McMurray inverter with rate protection networks.

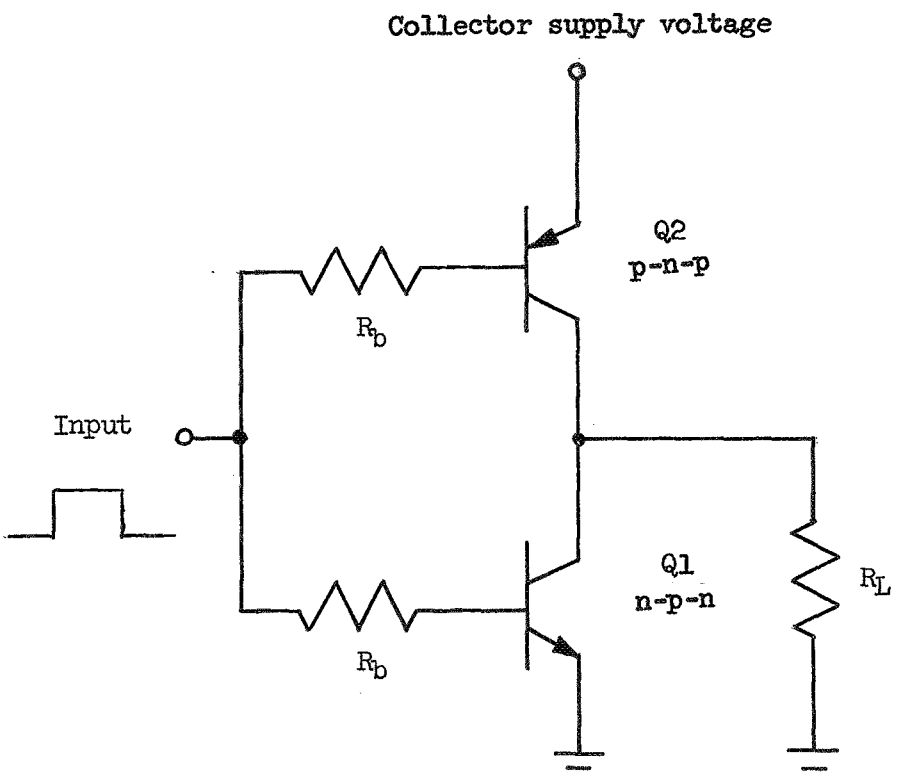

Figure 6.- Complementary transistor switch.

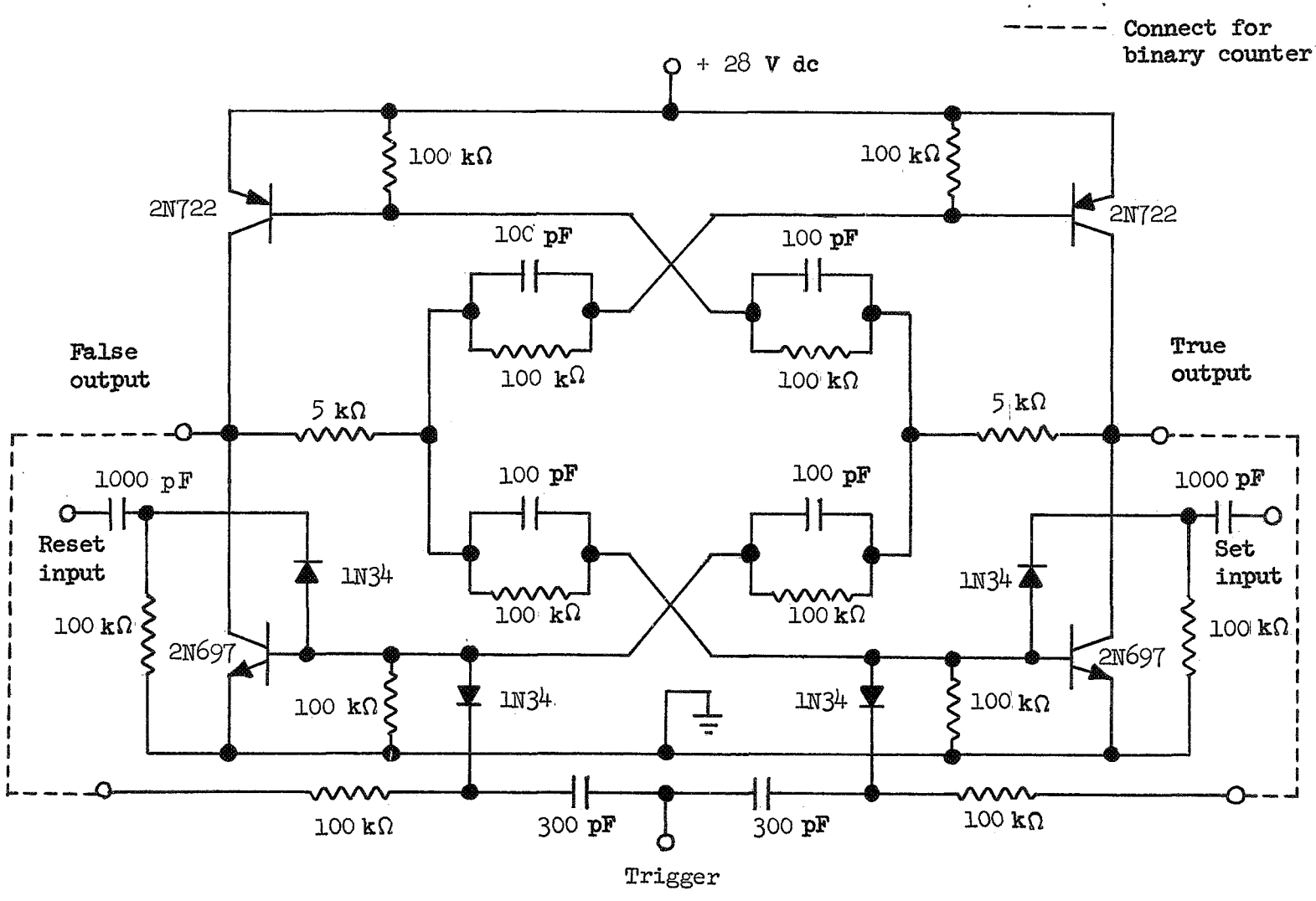

Figure 7.- Complementary transistor flip-flop designed for 28 V dc.

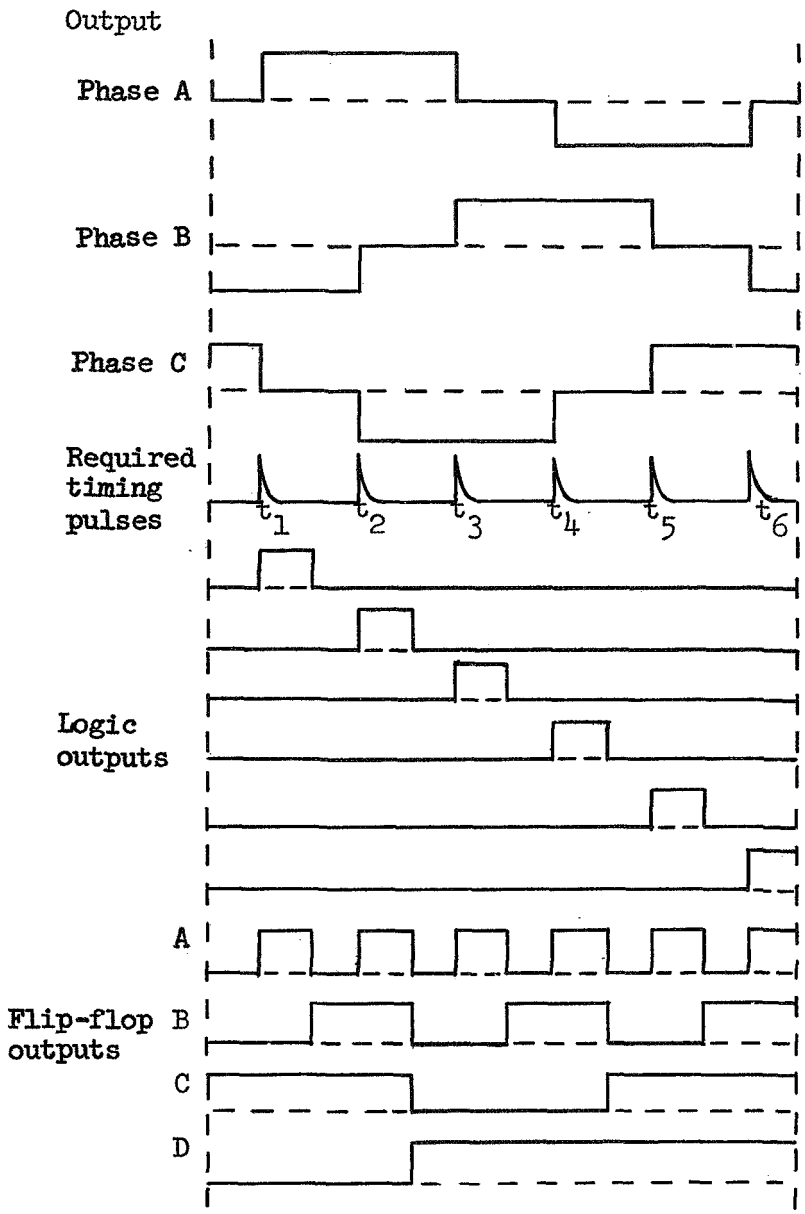

Figure 8.- Timing-pulse relationships.

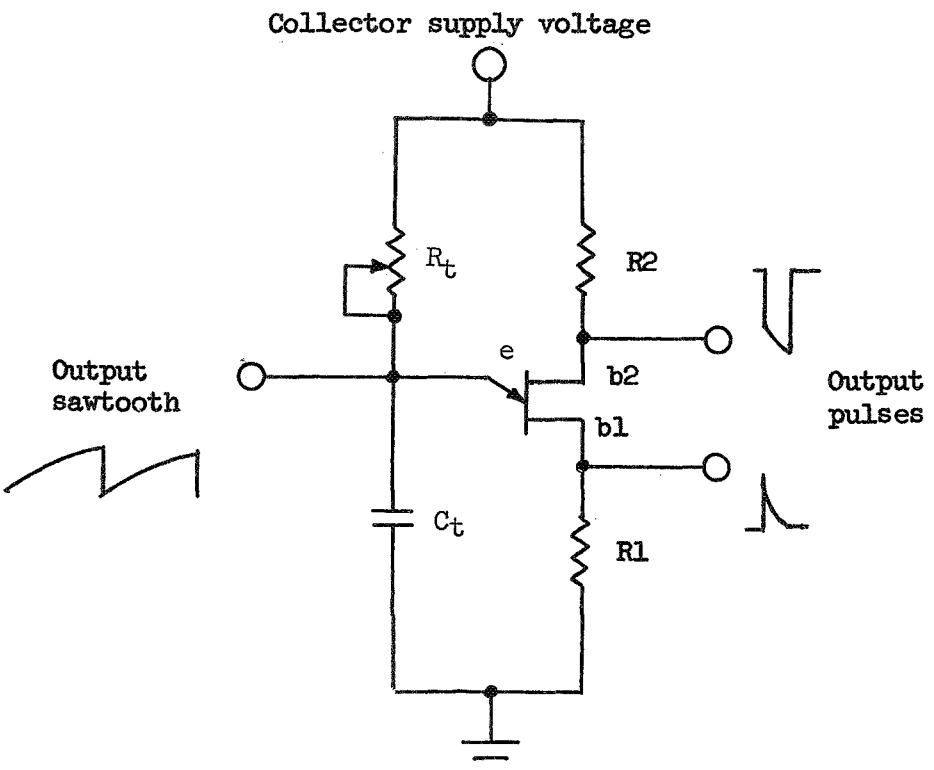

Figure 9.- Unijunction transistor relaxation oscillator.

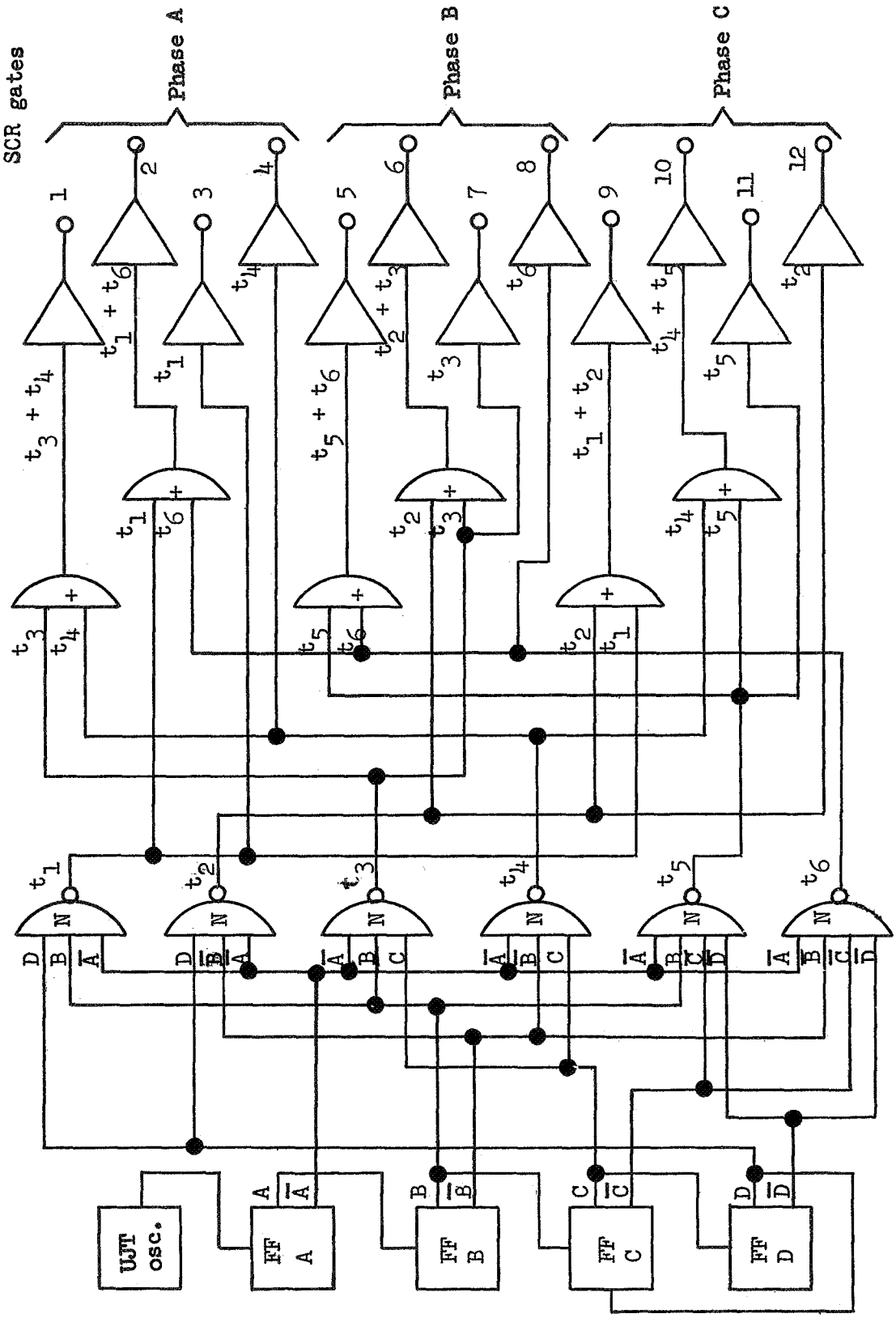

Figure 10.- Logic block diagram.

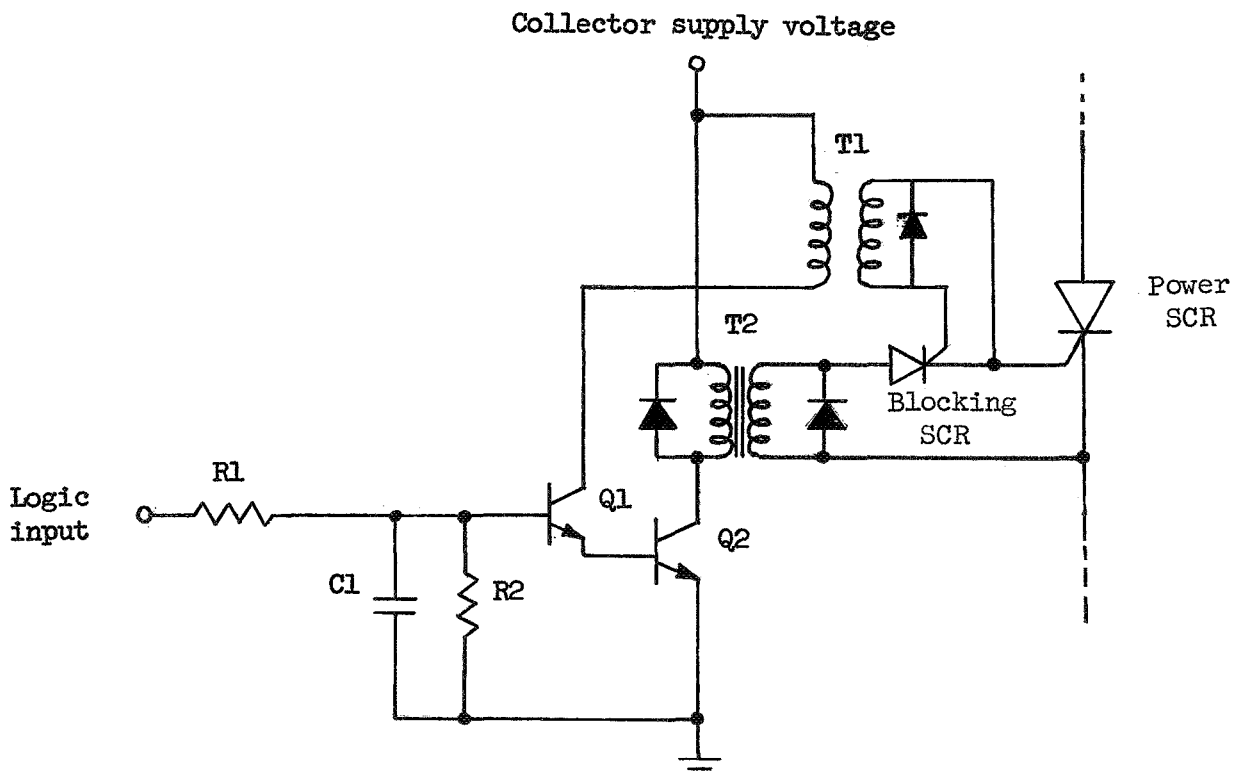

Figure 11.- Blocking pulse gate amplifier.

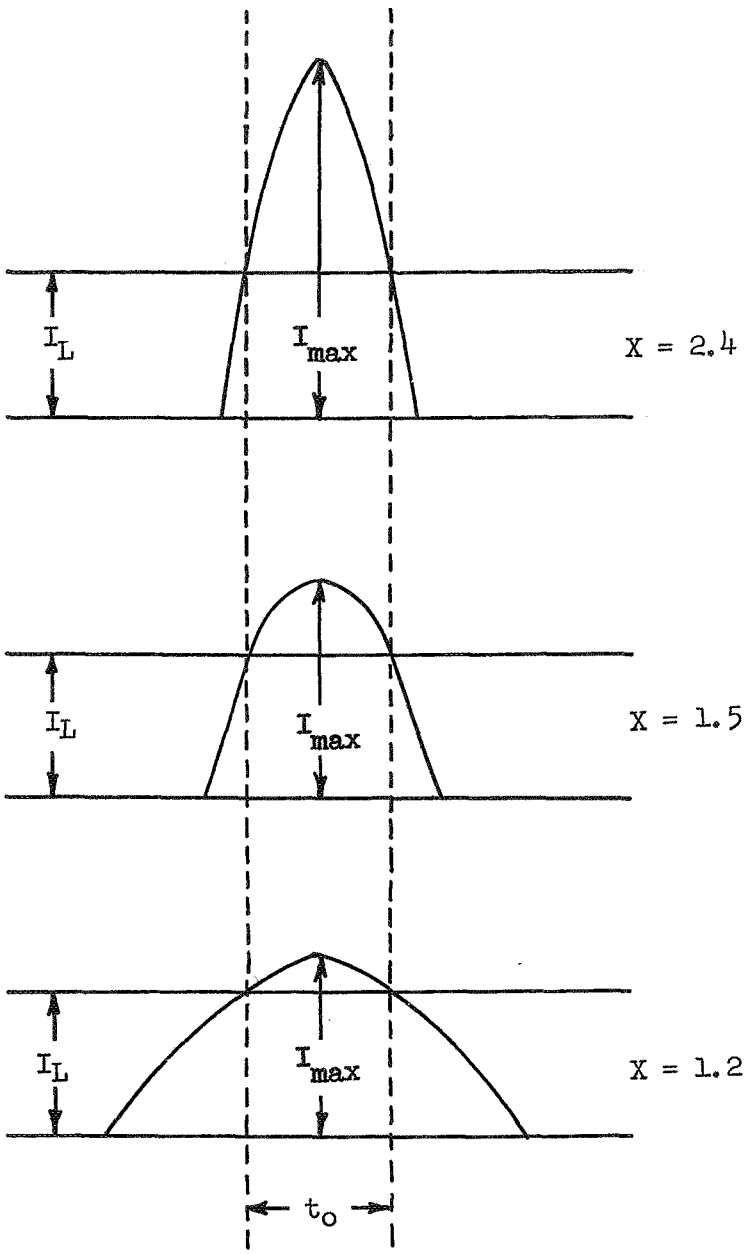

Figure 12.- Commutating current pulses.

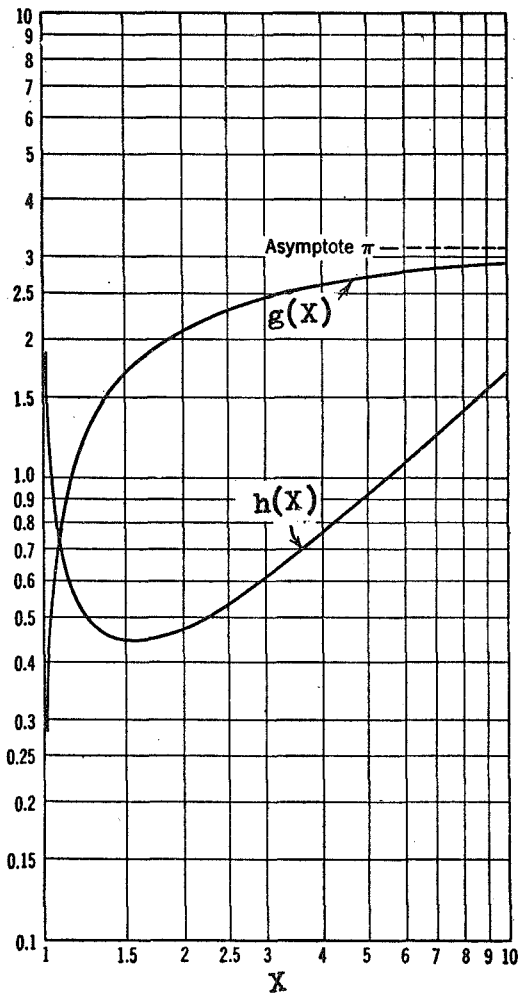

Figure 13.- Commutation parameters g(X) and h(X).

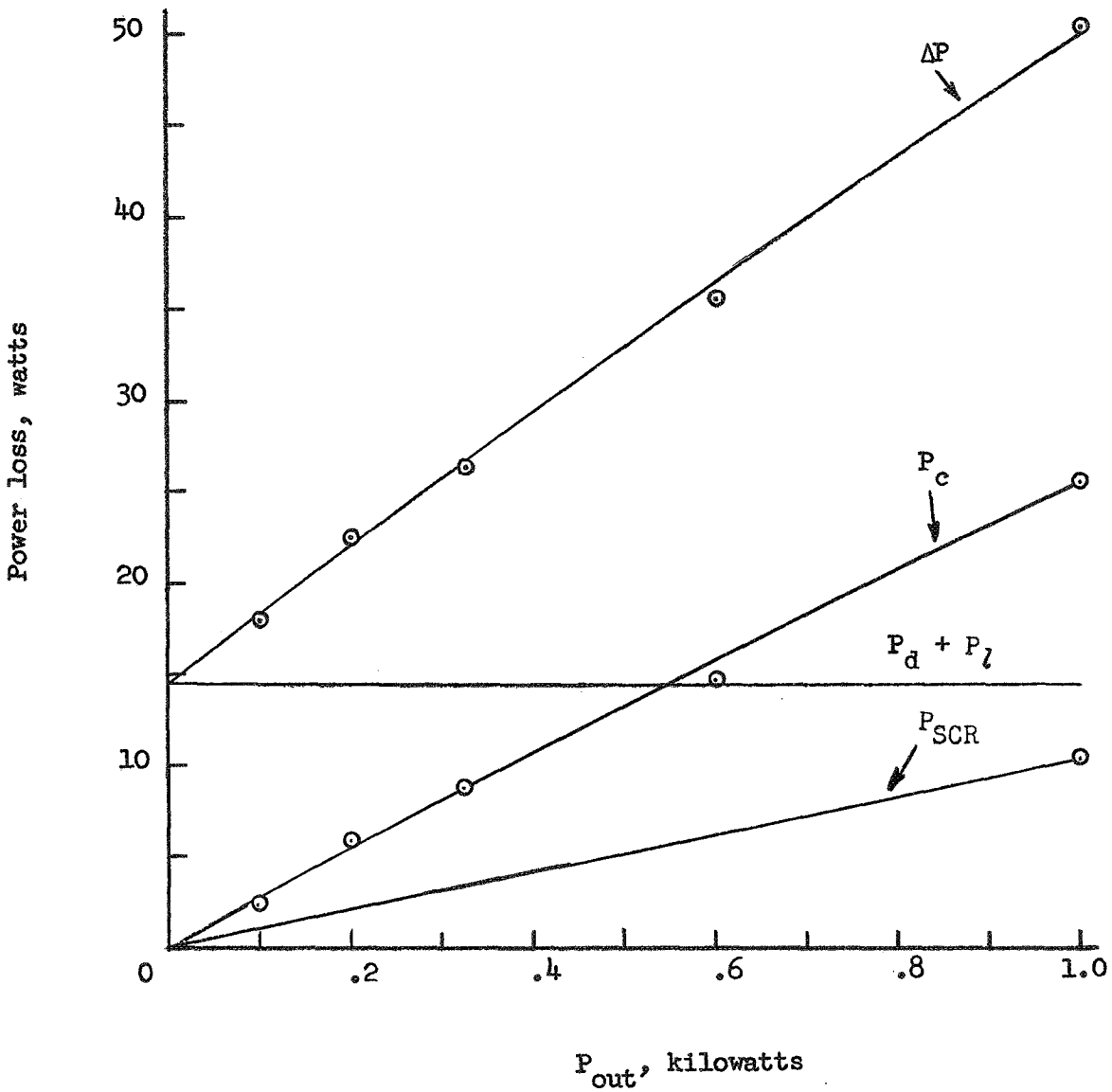

Figure 14.- Power loss breakdown for single-phase inverter.

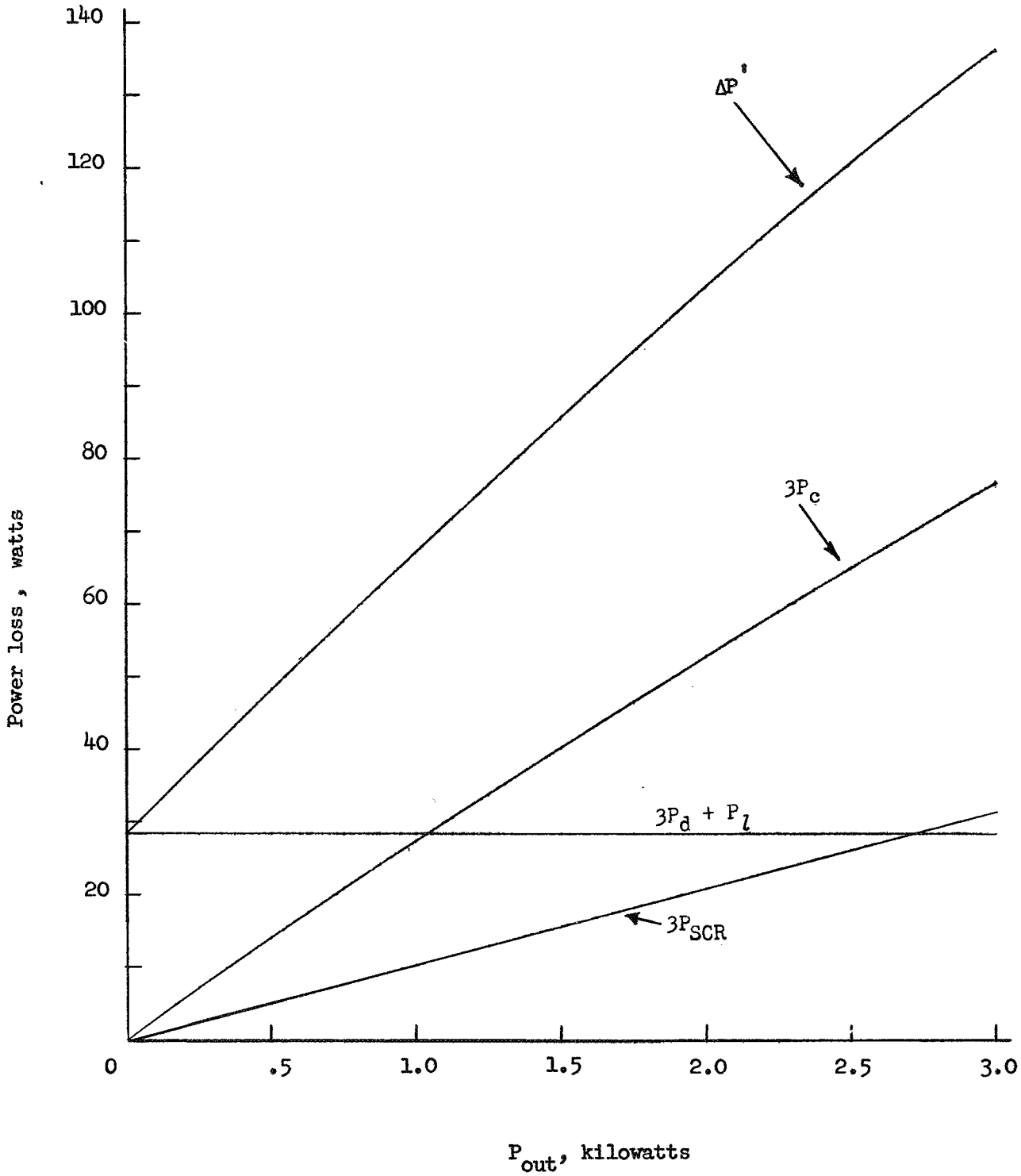

Figure 15.- Calculated losses for three-phase inverter.

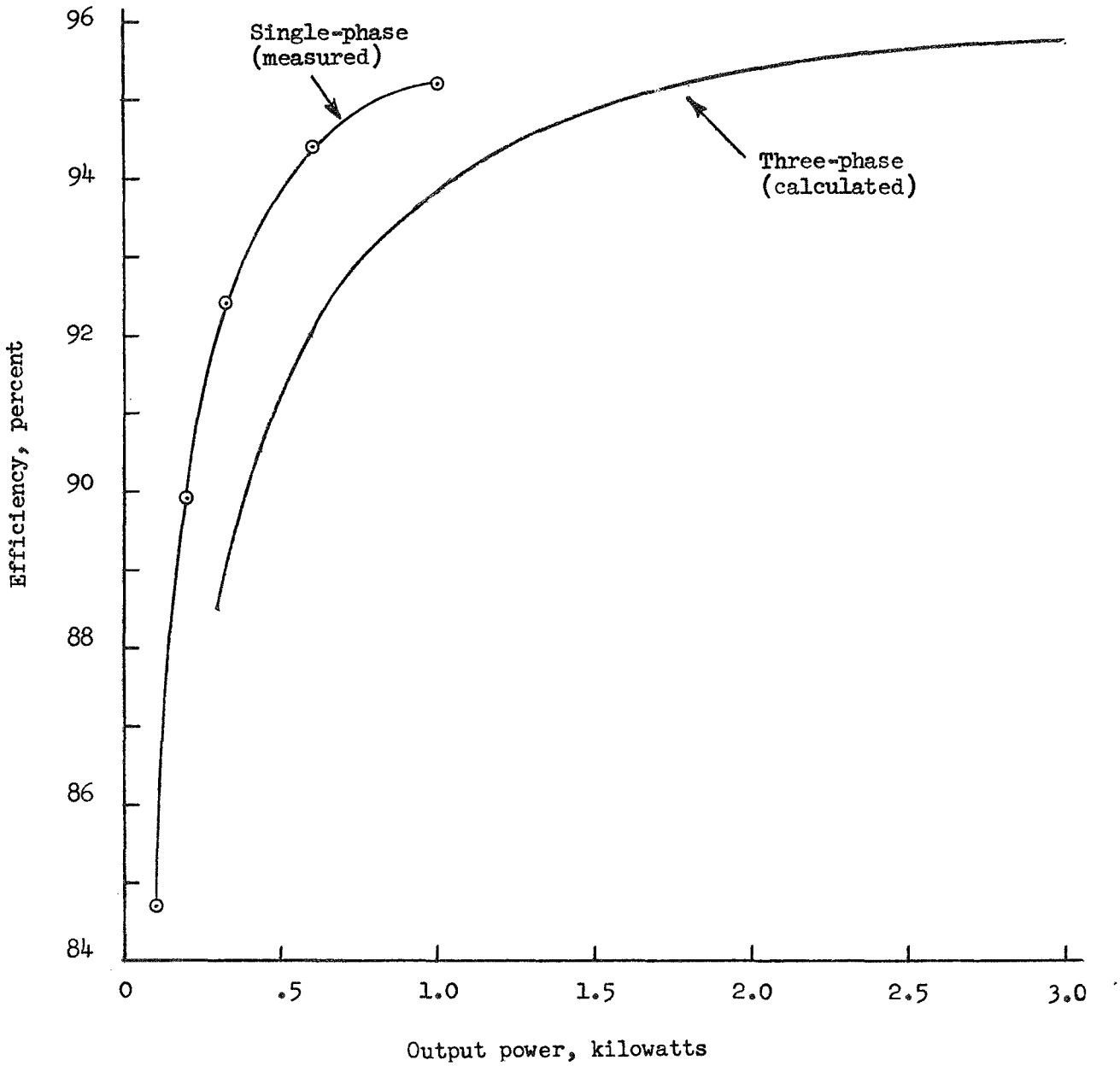

Figure 16.- Power efficiency curves.

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