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VALIDATION OF MONOLITHIC CIRCUIT TEST STANDARDS THROUGH AN INTEGRATED COS/MOS MULTIPLEXER

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Prepared Under Contract NAS 8-21440
by

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GEORGE C. MARSHALL SPACE FLIGHT CENTER
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

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FINAL REPORT

for

GEORGE C. MARSHALL SPACE FLIGHT CENTER
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

This report describes studies performed in accordance with Contract No. NAS 8-21440, dated June 25, 1968. This report covers work performed between June 25, 1968 and December 31, 1969.

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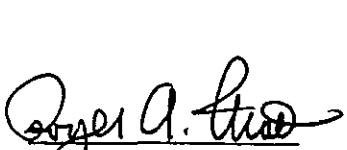

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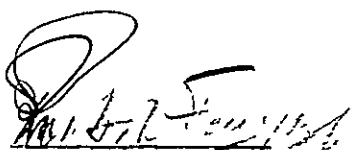

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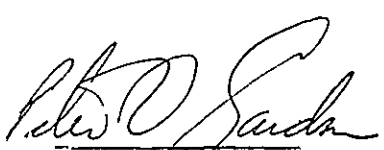
Principal Investigators

Approved by:



Peter D. Gardner
Project Manager

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SECTION I
INTRODUCTION

The objective of this program has been to validate proposed NASA test standards for process control and testing of monolithic circuits. The proposed tests are to be used in the process for actual fabrication of a complementary-symmetry MOS (COS/MOS) 16-channel multiplexer circuit.

Achievement of program objectives was keyed to the following developments:

a. Validation of the proposed NASA test standards by applying suitable tests at appropriate steps in the COS/MOS process.

b. Design and development of a COS/MOS 16-channel multiplexer circuit.

c. Fabrication of the 16-channel COS/MOS multiplexer, using the RCA COS/MOS process.

SECTION II
TECHNICAL DISCUSSION

A. PROCESSING

The multiplexer described in this report (Figure 1) was fabricated on a silicon chip 130 mils by 110 mils. The right portion of the chip is occupied by the clock and enable inverters and the four stages of the up-counter with the random-access addresses (Inputs 1, 2, 3 and 4). The decoder is in the center of the chip; the multiplexer switches with their inverters and the blanking and reference gates are on the periphery. Inside the chip, four testing pads are provided for diagnostic purposes for evaluation of the performance of the counter and of the decoder. On the chip are also two test transistors, marked n and p for testing the respective threshold voltages and transconductance. In the left lower portion, a capacitor is provided to evaluate the cleanliness of the processing of the oxide and metal system. Figure 2 shows a C-V plot obtained during processing of the multiplexer.

Standard RCA COS/MOS processes, reported elsewhere[1] are used in processing the multiplexers. In Figures 3 through 8 are photographs of the masks used during processing of the well, p^+ diffusion, n^+ diffusion, channel, contacts. and metalization.

The multiplexers are packaged in an RCA 28-lead ceramic flat package (Figure 9). This package is 1/2 by 3/4 by 3/16 inch. In Table I is listed the bonding pattern of the multiplexer.

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(1) Solid-to-Solid Diffusion Techniques to Improve Reliability in LSI Circuits, NASA Contract NAS 12-2026, Final Report.

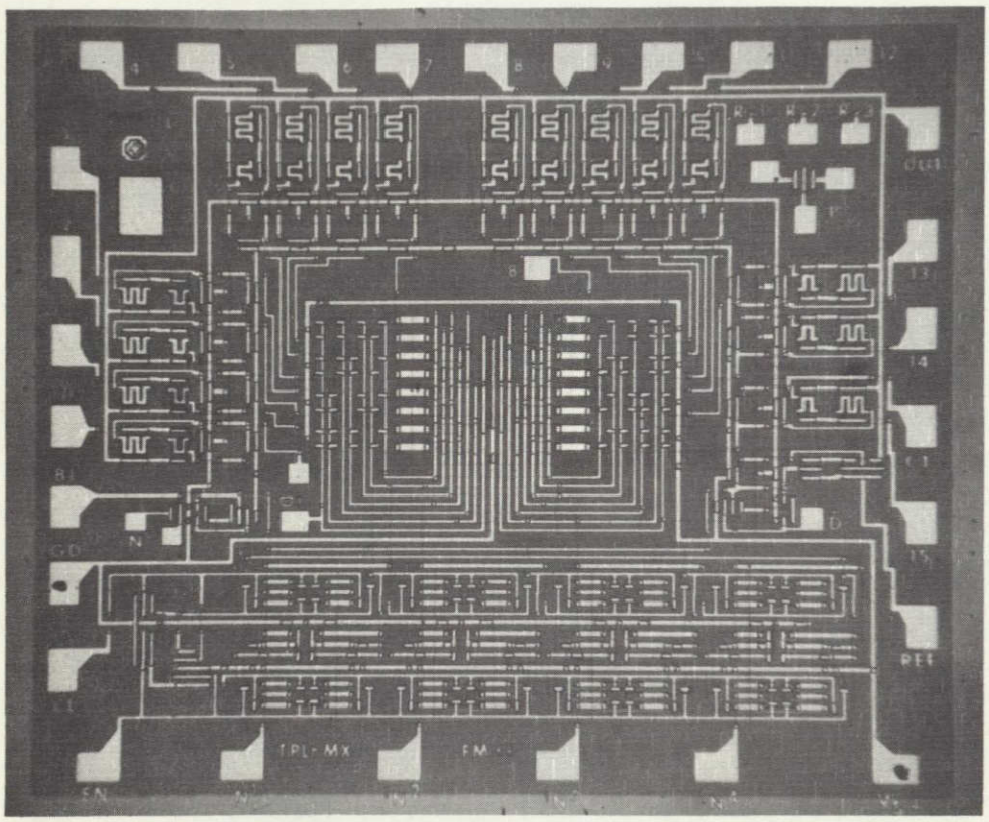

Figure 1. Multiplexer Fabricated on 130- by 110-Mil Chip

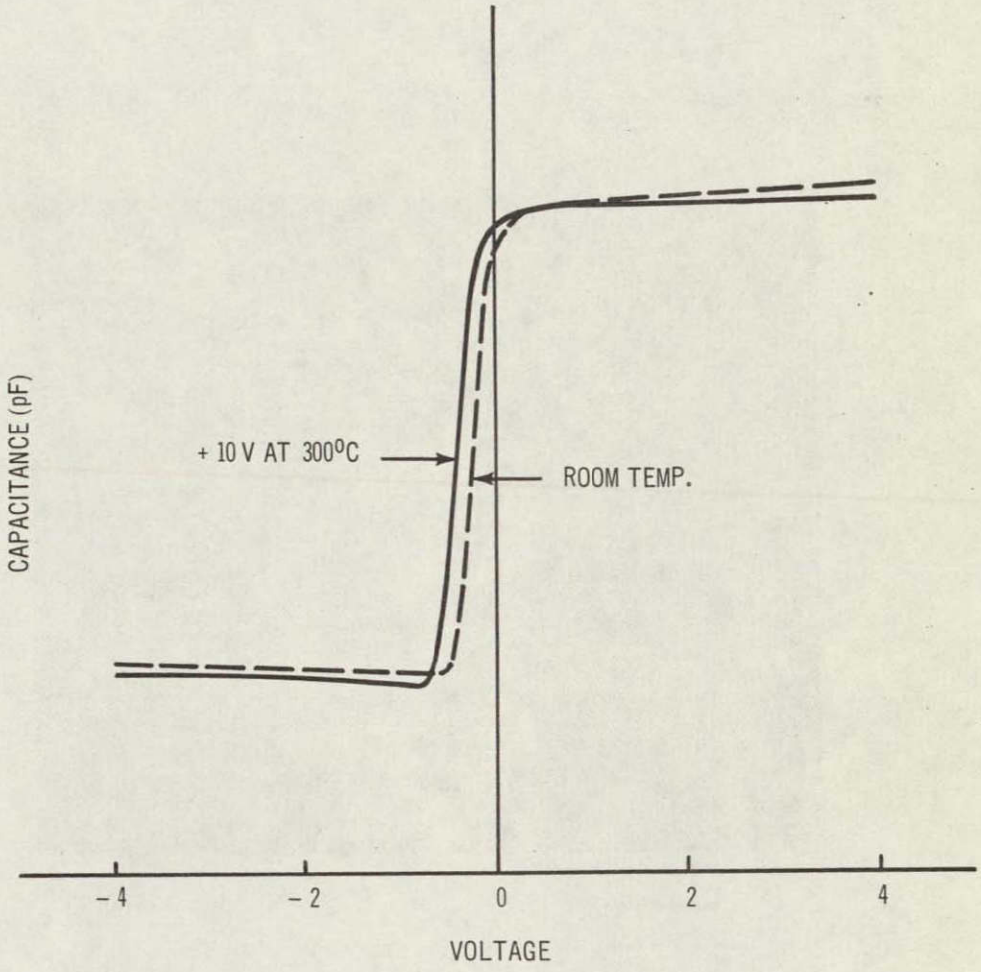

Figure 2. Capacitance-Voltage Plot of Multiplexer Devices (Lot No. MC-12)

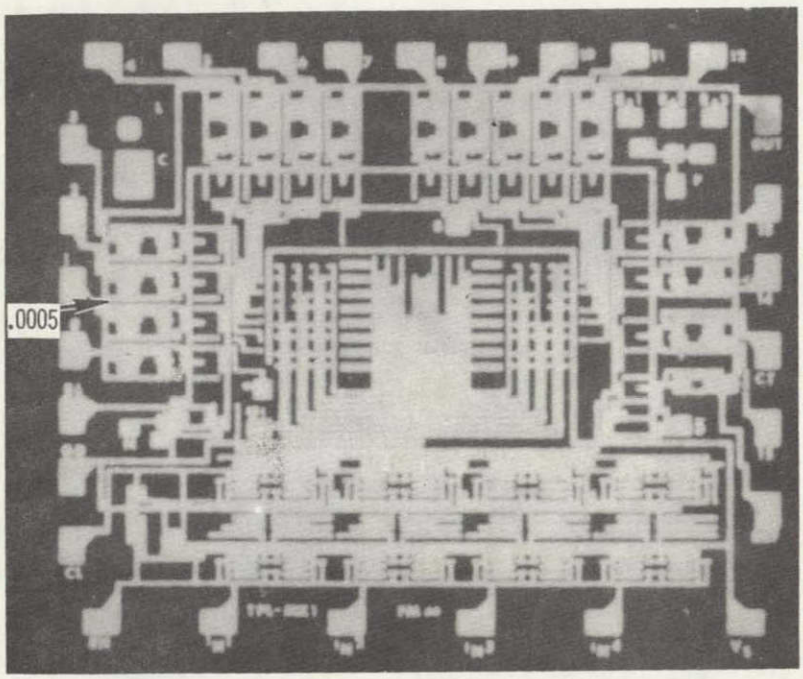

Figure 3. Metalization Pattern Photomask

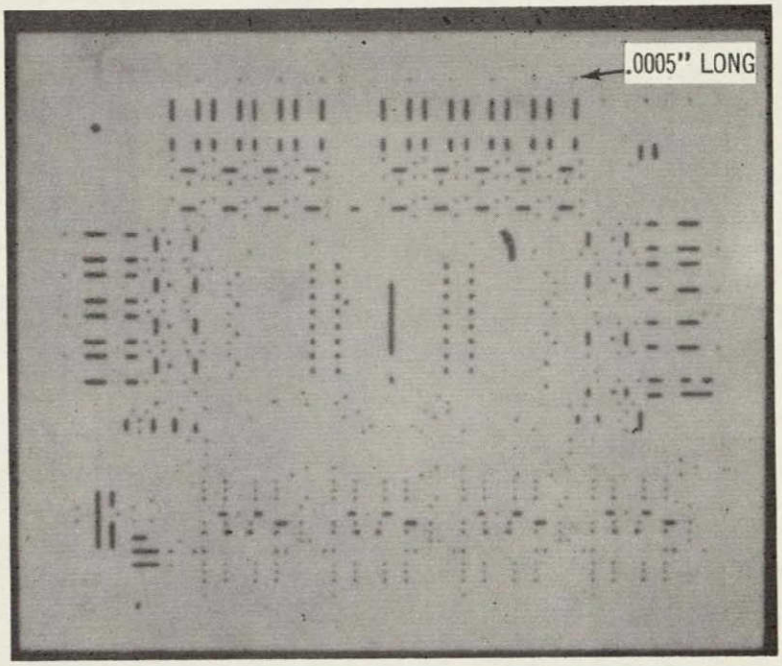

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Figure 4. Contact Photomask

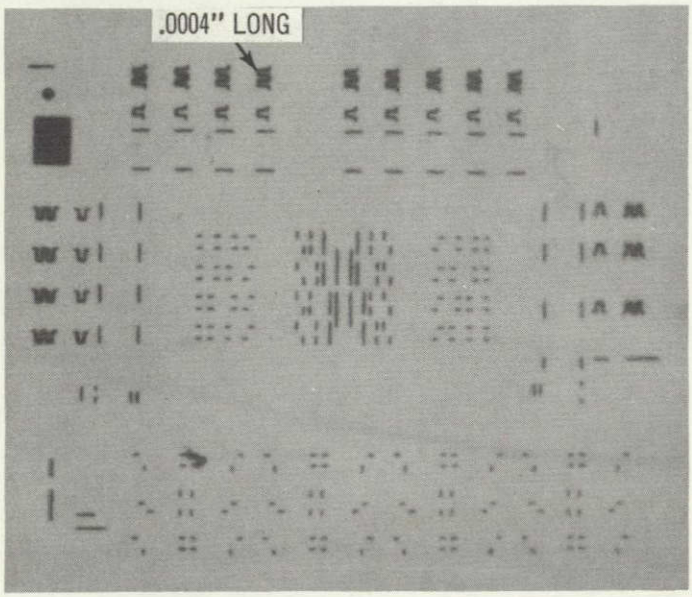


Figure 5. Channel Photomask Pattern

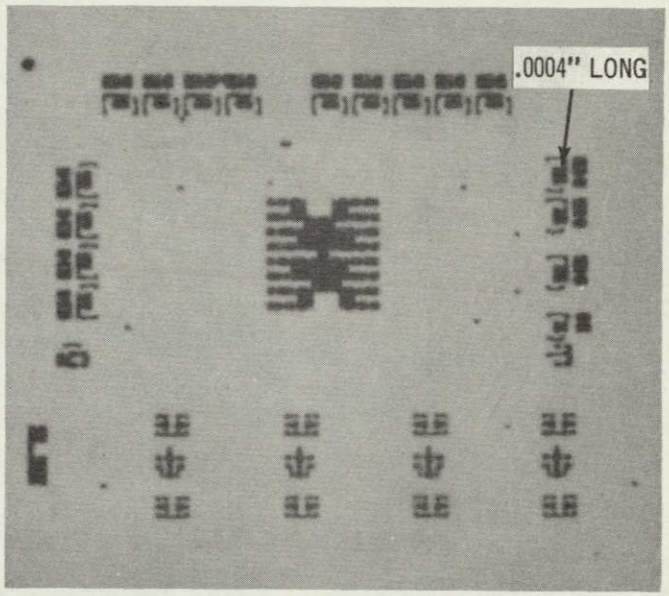


Figure 6. n^+ Diffusion Photomask Pattern

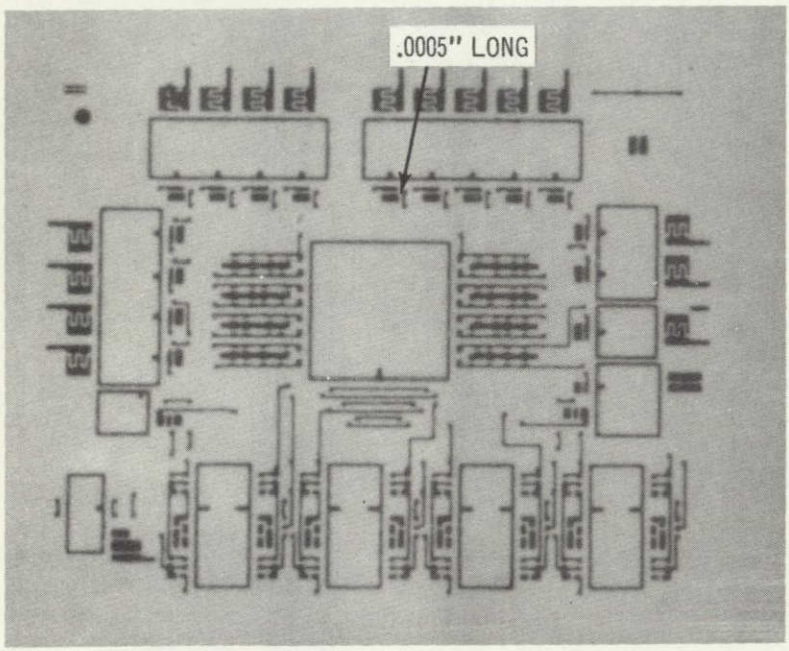


Figure 7. p^+ Diffusion Photomask Pattern

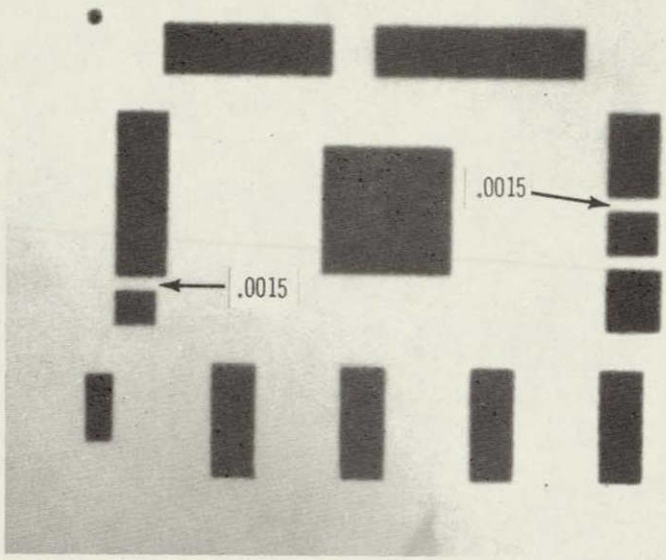


Figure 8. Well Photomask Pattern

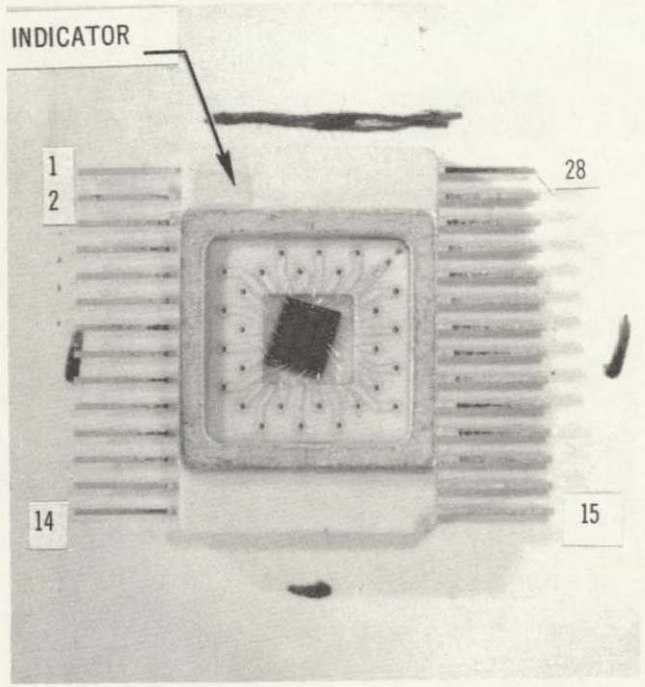


Figure 9. Photomicrograph of Multiplexer Pellet in 28-Lead Package

TABLE I. BONDING PATTERN OF THE MULTIPLEXER

Pin No.	Masking (Fig. 3)	Function
1	GD	Ground
2	CL	Clock
3	EN	Parallel Address Enable
4	In 1	Parallel Address Inputs
5	In 2	" "
6	In 3	" "
7	In 4	" "
8	V_S	Supply Voltage
9	REF	Reference
10	15	Input Channel 15
11	CT	Sync. Output
12	14	Input Channel 14
13	13	" " 13
14	Out	Output Channel
15	12	Input Channel 12
16	11	" " 11
17	10	" " 10
18	9	" " 9
19	8	" " 8
20	7	" " 7
21	6	" " 6
22	5	" " 5
23	4	" " 4
24	3	" " 3
25	2	" " 2
26	1	" " 1
27	0	" " 0
28	BL	Blank input

B. SIXTEEN-CHANNEL MULTIPLEX SYSTEM

Figure 10 shows the block diagram of the COS/MOS 16-channel multiplexer unit. The multiplexer provides a means of time sharing 16 parallel analog inputs on a single common output channel. The input channels can be operated in either a random-access mode or a sequential-access mode. The random-access mode is activated by putting a logical 1 on the parallel address enable input and entering the desired address into the parallel address inputs. All counter stages of the four-stage up-counter can be reset to 0 by means of the random-access mode.

The multiplexer provides a sync output to drive other multiplex units. Another feature is a blank input that disconnects all 16 channels of the multiplexer and connects a reference channel to the output when a logical 1 is applied. The reference channel can be set at any level for purposes of calibration.

The functions used in the multiplexer and the device quantities are listed below.

Functions	Device Quantity
Input Inverters to 1st Counter Stage	4
Four-stage Up-counter (24 per stage)	96
Blanking Gates	8
Tree Decoder (30 n's, 64 p's)	94
Multiplex Switches with Inverters	68
Total	270

1. COUNTER CIRCUIT

Figure 11 shows the circuit of one counter stage out of the four used in the multiplexer. The counter is essentially a T flip-flop using master-slave loops. For convenience, positive logic (0, +V) will be used to describe the operation of the circuit rather than using the actually applied symmetrical logic (-5.0V, + 5.0V). If the counter is to be used in the sequential-access mode the parallel address enable input E is set to 0. Switches (transfer gates) S7 and S8 are open and switches S5 and S6 are closed.

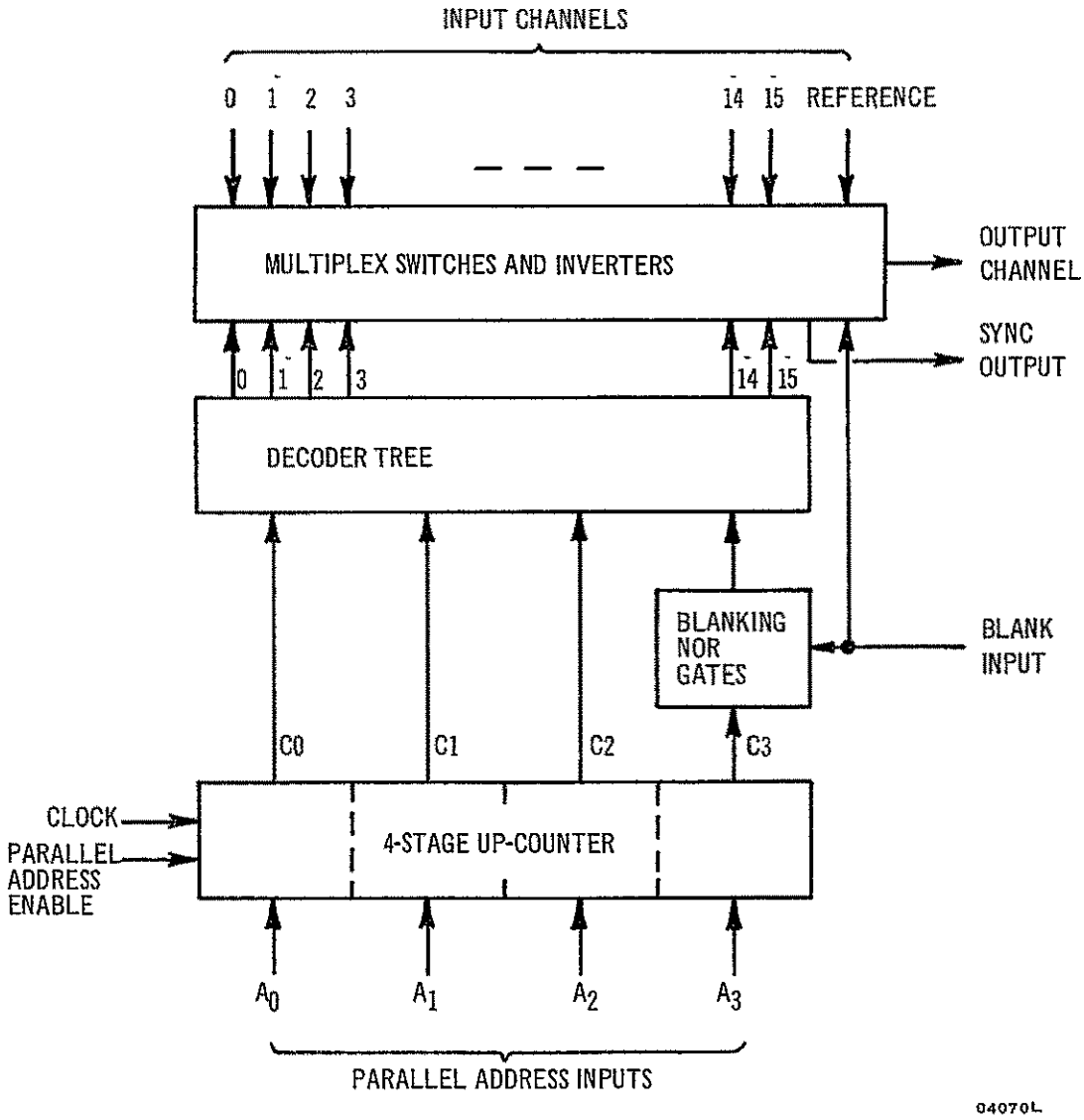


Figure 10. 16-Channel Random-Sequential Access Multiplexer, Block Diagram

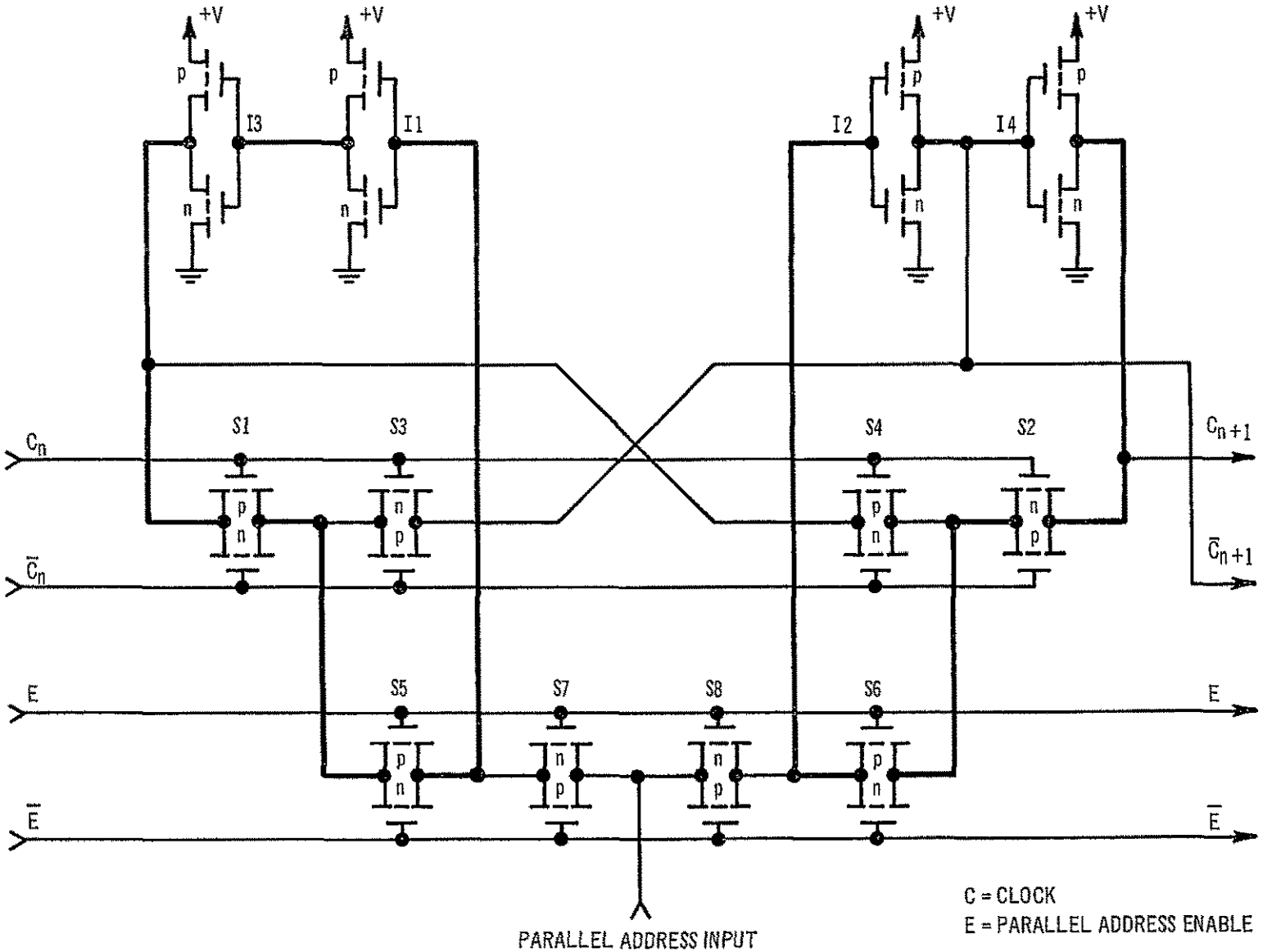


Figure 11. Circuit of Up-Counter Stage

The operation of the counter in this mode can be broken into four periods, shown in Figure 12. During period T1, clock signal C_n is set to 0 and the input of inverter I1 is chosen to be 0. Since switches S1 and S5 are closed 0 at input I1 is locked into the left loop. The left loop forces this state into input I2, via S4 and S6, so that the output C_{n+1} is at 0.

During the transition from period T1 to T2 (i.e., when C_n changes from 0 to 1), the right loop will lock to the 0 at input I2 because S2 is closing. Since the left loop is now unlocked by S1, input I1 is forced to go to 1 by the right loop via closed switches S3 and S5. The output C_{n+1} still remains at 0 during period T2.

For the transition from period T2 to T3, the left loop will lock to the 1 at input I1 because S1 is closing. Since the right loop is now unlocked by S2, input I2 is forced to go to 1 by the left loop via closed switches S4 and S6. Output C_{n+1} is forced to be at 1 for period T3.

During the transition from period T3 to T4 the right loop will lock to the 1 at input I2 because S2 is closing. Since the left loop is now unlocked by S1, then input I1 is forced to go to 0 by the right loop via closed switches S3 and S5. The output C_{n+1} remains at 1 during period T4. The cycle is repeated as the clock signal C_n continues.

For the counter to operate in the random-access mode, enable input E is set to 1. This action opens switches S5 and S6 opening their respective loops. The desired address is then forced through closed switches S7 and S8 and into the inputs of inverters I1 and I2. During the transition period, when E changes from 1 to 0, the information is held by the gate capacitances of the MOS transistors used in inverters I1 and I2. When E finally reaches a value of 0, the information will lock into either the left loop, if C_n is 0, or into the right loop, if C_n is 1.

The photograph in A, Figure 13 shows the input clock signal and the output of each stage of the up-counter. The counter was initially set to 0000 by entering a 0 at each parallel address input and initiating the parallel address enable input. In B, Figure 13 shows an input address 1010

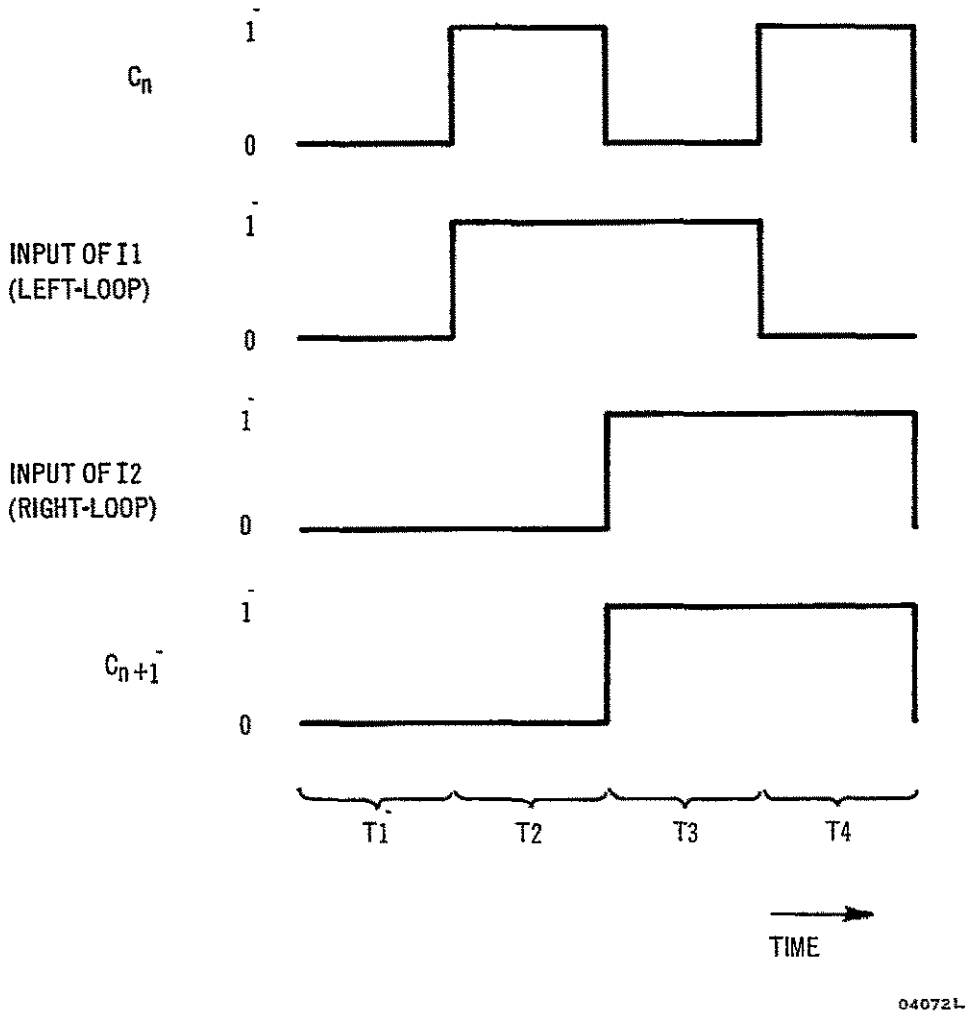
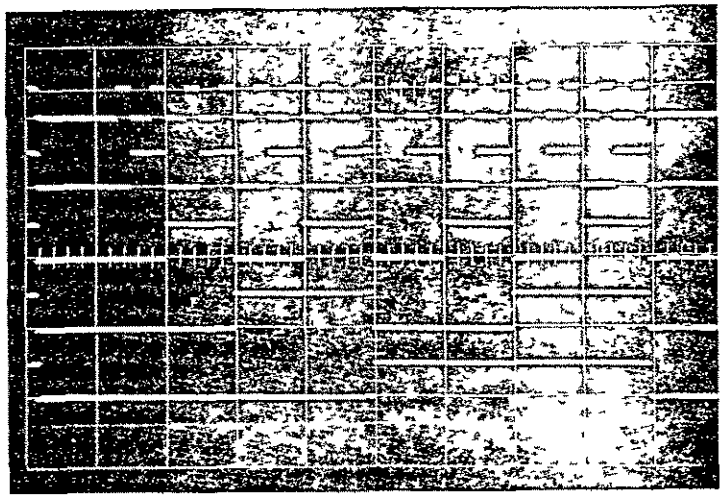
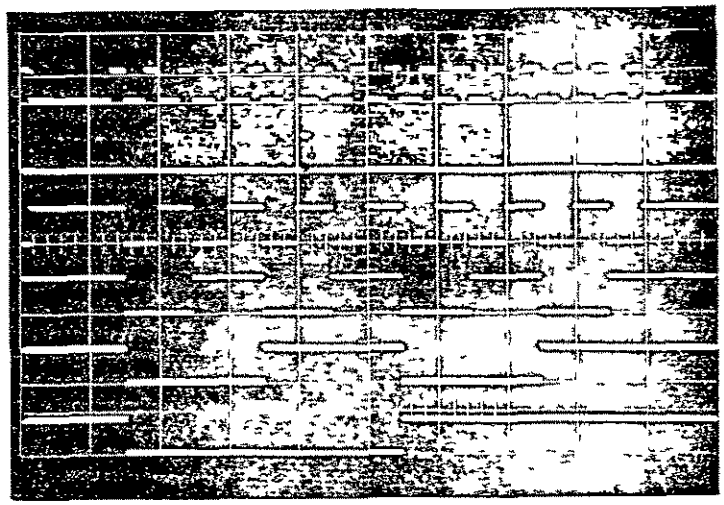


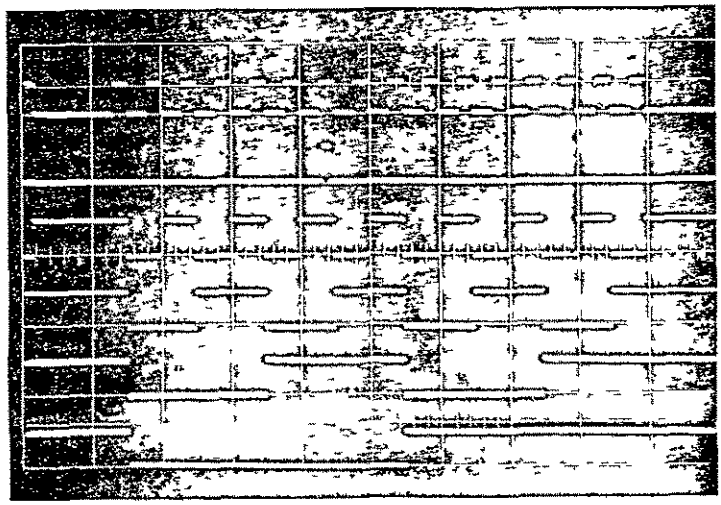
Figure 12. Operational Signal Sequence of One Counter Stage



A. INPUT AND OUTPUT CLOCK SIGNALS



B INPUT ADDRESS 1010 ENTERED WHEN ENABLE = 1 CLOCK INPUT = 1



C INPUT ADDRESS 1010 ENTERED WHEN ENABLE = 1 CLOCK INPUT = 1

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Figure 13 Up-Counter Signal Pulses

being entered into the counter stages when the enable pulse E goes to 1. In C, Figure 13 it is shown that the address can be entered without ambiguity with the enable pulse in the other half of the clock period.

2. DECODER AND BLANKING CIRCUITS

The decoding network is shown in Figure 14. The decoder tree is essentially 16 COS/MOS NAND gates, except that the n-channel devices are subtly combined to reduce their numbers. Each tree decoder NAND gate is coded in such a manner with the normal and inverted signals from the up-counter that only one output is activated at a time. The binary signal from the up-counter activates the corresponding output, and each up-date of the up-counter by the clock produces a sequential sweeping of the decoder output. A typical output (number 7) is shown in the photograph in Figure 15.

The intermediate circuit shown in Figure 16 is used to blank or open the multiplex switches when the blanking signal is set to a logical one. This scheme was chosen since the alternate scheme of placing a common series-blanking switch (transfer gate) with the 16 multiplex switches would require the use of unreasonably large MOS devices to provide the 1000-ohm switch resistance. The circuit consists of two NOR gates. The gate inputs are connected to the last counter stage and to the blank input. When the blanking signal is at 0 the NOR gates act as regular inverter stages. When the blanking signal is at 1, the outputs of both NOR gates are at 0 so that the decoder is disabled.

3. MULTIPLEX SWITCHES AND ASSOCIATED INVERTERS

Figure 17 shows the circuit diagram of the multiplex switches and their associated inverters. The inverters are required because the switches use complementary devices. Single-channel devices cannot provide a full operating range, as described in Section B4a. In Figure 15 is shown a photograph of an input sinusoidal being sampled by switch number 7. The multiplexer has in addition a 17th switch that closes when the blank input goes to logical 1. The regular multiplex switches are opened by the logic described in Paragraph 2, above. The reference switch can be connected to some voltage level for the

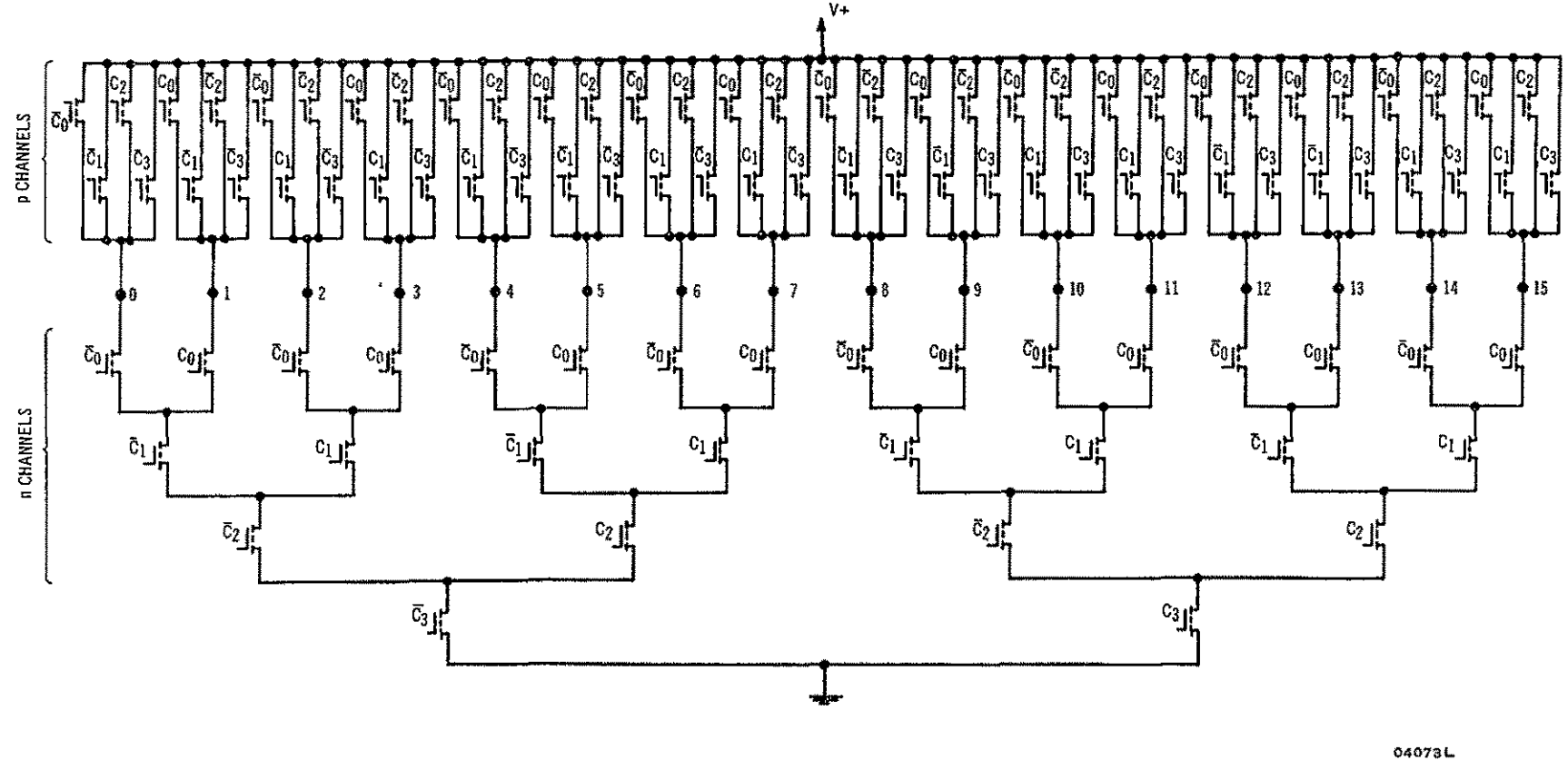

Figure 14. Circuit of Decoder Tree Used in Multiplexer

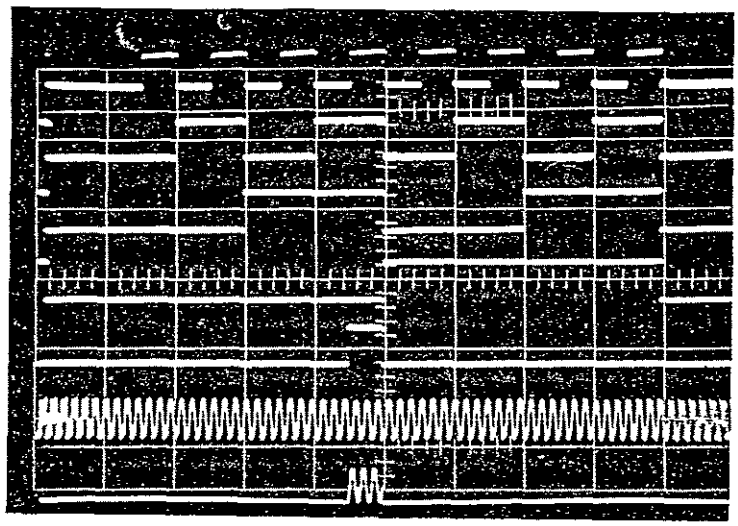

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Figure 15 Typical Decoder and Switch Output

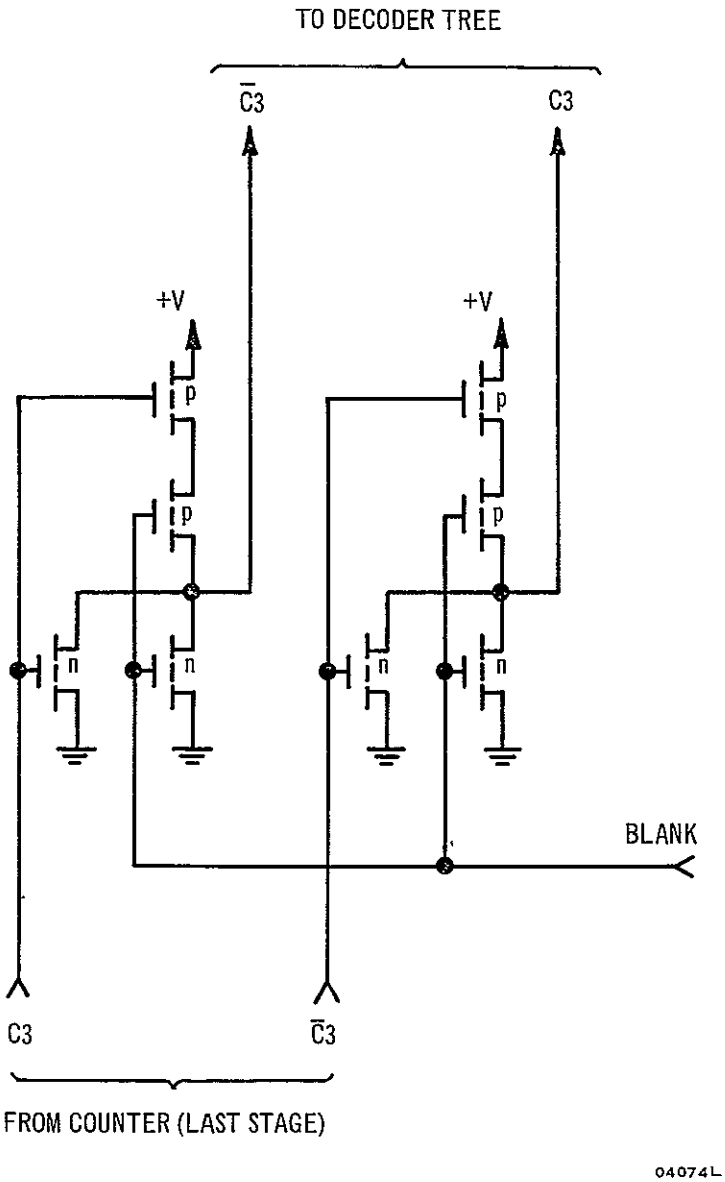


Figure 16 NOR Gates Used for Blanking in Multiplexer

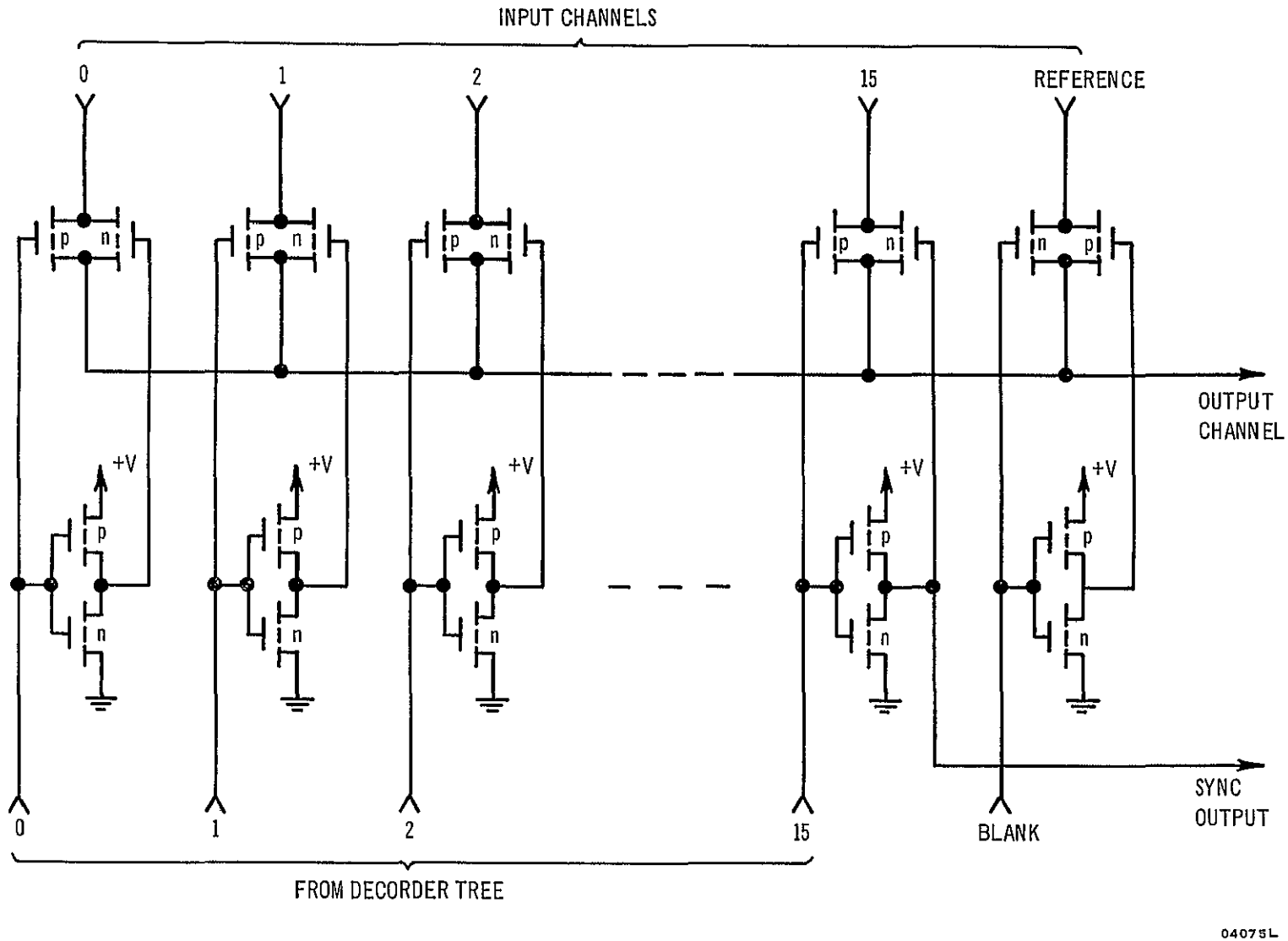


Figure 17. Circuit of Multiplex Switches with Associated Inverters

purpose of calibration. The sync output provided at output 15 of the multiplexer can either truncate the count of the up-counter or drive another multiplexer.

The ON resistance of the multiplex switches are specified to be at least 1000 ohms. With this value of resistance the width of the MOS devices can be calculated. Figure 18 shows the characteristic curve for an MOS device. The MOS switch operates within the lower portion of the curve in the triode region. The triode region is represented by equation 1.

$$I_D = -\beta\left[\left(V_{GS} - V_{GST}\right)V_{DS} - 0.5\,V_{DS}^{2}\right] \quad \ldots\ldots\ldots\ldots \quad (1)$$

where

$$\beta = \mu\,\frac{W}{L}\,\frac{\varepsilon_{ox}}{t_{ox}}$$

ε_{ox} = permittivity of silicon oxide (35.4×10^{-14} F/cm)

L = length of channel (0.3 mil)

T_{ox} = thickness of oxide (1000 Å)

μ = surface mobility +175 $cm^2/V \cdot S$ for p-channels

-350 $cm^2/V \cdot S$ for n-channels

V_{DS} = drain-to-source voltage

V_{GS} = gate-to-source voltage

V_{GST} = threshold voltage

W = width of channel (in mils)

The drain-source conductance (slope of the characteristic curve) is obtained by differentiating equation 1.

$$g_{ds} = \frac{\partial I_D}{\partial V_{DS}} = \beta(V_{GS}-V_{GST})-V_{DS} \quad \ldots\ldots\ldots\ldots\ldots \quad (2)$$

Since the resistance is due to two switches in parallel so that $r_{ds} = 1/2g_{ds}$ (both switches are on even though one switch limits in the source follower mode), and assuming that the load resistance is at least 10 times larger than the switch resistance so that $|V_{DS}| \ll |V_{DS} - V_{GST}|$ equation 2 reduces to equation 3.

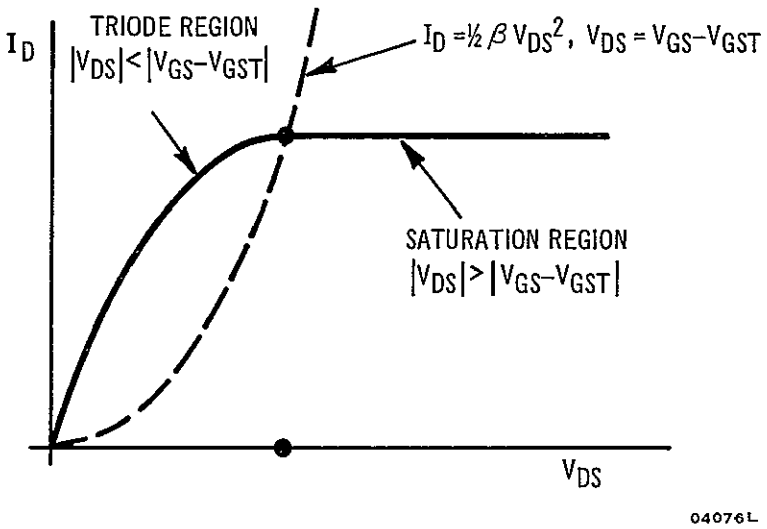


Figure 18 Characteristic Curves of MOS Transistor

$$r_{ds} = \frac{1}{-2\beta\,(V_{GS} - V_{GST})} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (3)$$

With $r_{ds} = 1000$, $V_{GS} = V_{LL} = -6V$, $V_{GST} = -4.00V$ (compensated by substrate effect), and using the values of the auxiliary parameters of equation 1, the width of the p channel is calculated to be about 12 mils. The width of the n channel is half of this value since the only differing parameter is the surface mobility. The multiplexer switches were designed with these values.

Although the widths of the p-channel and n-channel devices are unequal, the capacitance due to the overlap of the gate-to-source and drain-to-source diffusions were made equal for both devices. This is required so that the feed-through spikes occurring as a result of the logic level transitions are canceled as much as possible.

4. MULTIPLEX OUTPUT SWITCHES

The basic multiplex system consists of a number of electrically activated switches, the inputs to which may be connected to n quantity of desired signals, as shown in Figure 19. The switches are turned on sequentially. Each input signal is sampled and appears sequentially at the output. The sampling rate is assumed to be at least twice that of the highest frequency component of the incoming signal. The transmitted output signal, therefore, may be reconverted into the original input signals. The reconversion process is accomplished by a similar synchronous switching.

The following discussion consists of a qualitative part (Sections B4 through B5) and a more quantitative part (Sections B6 through B9).

a. Single p-Channel MOS Switch

Figure 20 shows a single p-channel device used as a switch. Assume the switch resistance is much smaller than the load resistance R_L. The voltages shown (input voltage V_I, output voltage V_O, gate voltage V_G, and substrate voltage V_B) are all measured with respect to ground.

The MOS is a bilateral device for which source and drain designa-

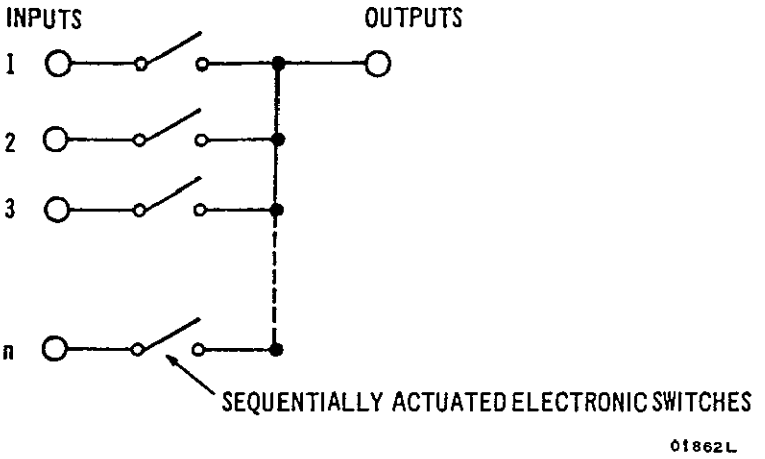


Figure 19 Basic Multiplex System

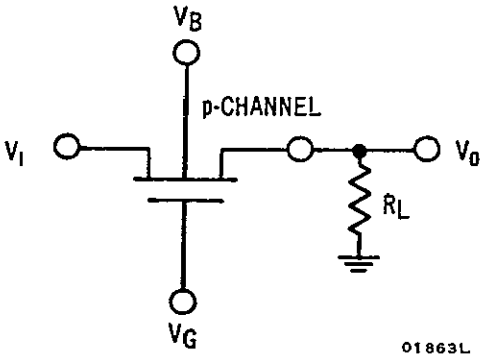


Figure 20. Single MOS Multiplex Switch (p-Channel)

tions are determined by the direction of current flowing through the device. For a p-channel MOS unit, current flowing into the device defines the source terminal; current flowing out from the device defines the drain terminal. The convention is opposite for an n-channel device. When an MOS unit is used as a mutliplex switch, input voltage V_i can be considered to swing negative or positive around zero bias; consequently, the source will shift from the input terminal to the output terminal. This action is shown in A, Figure 21 for a p-channel device and in B, Figure 21 for an n-channel device. When the source is located at the output terminal (i.e., terminal nearest to load resistor R_L), the switch is in the source-follower mode. If the source is located at the input terminal, the switch is in the common-source mode. The modes are inverted for an n-channel device, compared to a p-channel device, relative to coordinate axis V_1.

The transfer characteristic (i.e., V_i vs. V_o plot) of a typical single p-channel MOS switch in the on condition is shown in A, Figure 22. The MOS device used and the voltage values of the gate-to-ground voltage V_G and the substrate-to-ground voltage V_B are selected to provide linear operation within the linear operating range of $\pm$ 5 volts. Note that it is expected that the gate of the MOS switch must be overdriven (10 volts in this case) to provide the desired operating linear range. It will be shown subsequently that complementary MOS switches (i.e., n- and p-channel devices in parallel) do not require overdriven gates that need asymmetrical supply voltage.

The on transfer characteristics can be broken into four distinct regions, i.e. region 1 ($V_1 > 5.7$, common-source mode), region 2 ($0 < V_1 < 5.7$, common-source mode), region 3 ($-5.0 < V_1 < 0$, source-follower mode), and region 4 ($V_1 < -5.0$, source-follower mode). In region 1 the input voltage V_1 exceeds the substrate voltage V_B so that current flows through the source p^+ diffusion-to-substrate junction of the p-channel device. Although the drain p^+ diffusion-to-substrate junction is back biased, current flows to the load resistor by two mechanisms: (1) the p^+ diffusions are spaced so close that some p-n-p junction transistor action occurs, and (2) MOS action occurs since the surface below the gate is greatly inverted forming a good channel. Note that damage to the device can occur if the signal ventures within this region, since the

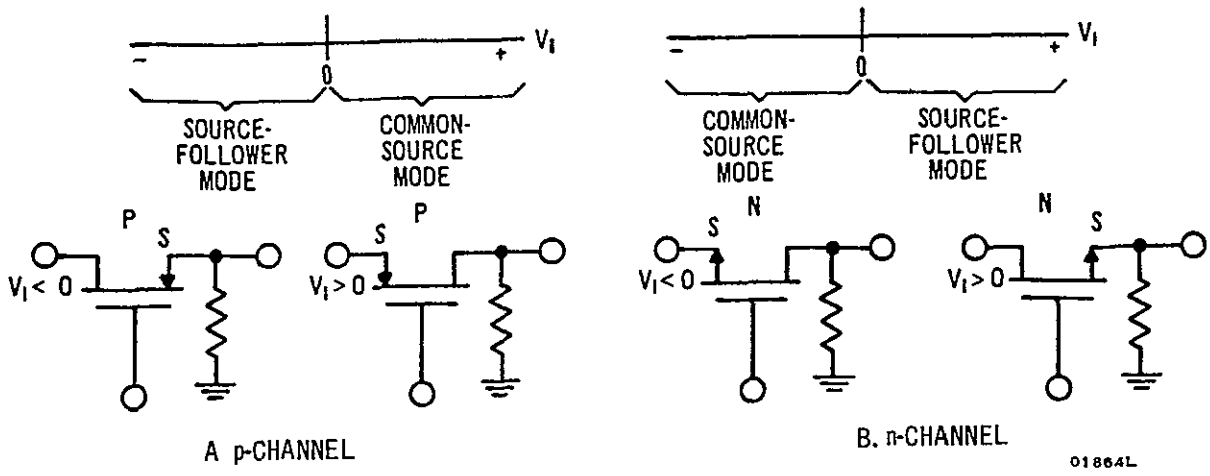


Figure 21 Definition of Modes of Operation

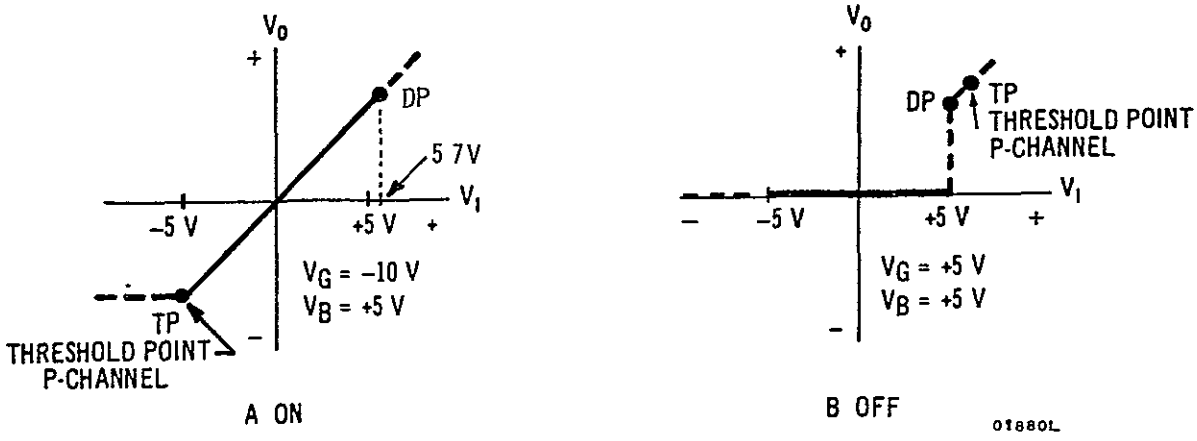


Figure 22 ON and OFF Transfer Characteristics of Single MOS Switch

source p^+ diffusion-to-substrate junction is forward biased so that a large and distructive current can flow unless limited by a series resistor. Note that the voltage V_B must be finite (± 5 volts in this case) to offset this diode turn-on mechanism so that the ± 5 volt half of the linear operating range of ± 5 volts is maintained. In region 2 conduction occurs only due to MOS action. In region 3 the MOS switch and load resistor combination operate as a source-follower with the gate-to-source voltage V_{GS} still below the threshold voltage V_{GST} of the device. Conduction of the MOS switch is still sufficient so that $R_{switch} << R_{load}$, and transfer characteristic linearity is maintained. In region 4 the gate-to-source voltage V_{GS} just about equals the threshold voltage V_{GST} independently of the input voltage V_1 so that V_o limits. This limiting action is described by classical source-follower action, i.e., the output voltage (V_o in this case) follows the input voltage (V_G in this case, but V_G is constant) and is independent of the supply voltage (V_i in this case, V_i varies).

In general, the four regions are distinguished by three points, i.e., the diode point of the p-channel device (DP), the origin, and the threshold point of the p-channel device (TP). The diode point (DP, and Dn for an n-channel device) is defined to be the point at which the source-diffusion-to-substrate junction becomes forward biased. The origin separates the modes of operation (i.e., common source-follower modes). The threshold point (TP, and Tn for an n-channel device) is defined to be the point at which the gate-to-source voltage V_{GS} just equals the threshold voltage V_{GST}. The term threshold point should not be confused with threshold voltage, since the threshold point applies only to the transfer characteristic (V_1 vs. V_o) of the switch and depends not only on the threshold voltage, but upon the gate-to-ground voltage V_G and substrate-to-ground voltage V_B as well. This will be shown in the OFF transfer characteristic.

In B, Figure 22 is shown the OFF transfer characteristic of the p-channel switch. As shown, the threshold point (TP) has moved above the diode point (DP) since the gate-to-ground voltage V_G is now ± 5 volts. Below the diode point (DP) the gate-to-source voltage of the MOS device is above the threshold voltage so that the device is cut off. Above the diode point

the switch turns on by the junction transistor action described previously. Above the threshold point both p-n-p junction transistor action and MOS transistor action are in effect. It must be noted that V_G or V_{GST} or both can be selected so that Tp can lie somewhat below DP. The resulting OFF transfer characteristic will be similar, even though MOS action occurs first, since the switch is operating in the common-source mode.

b. Complementary MOS Switch

The problems encountered in overdriving the single-channel MOS switch can be eliminated by using a complementary MOS arrangement. The arrangement consists of a p-channel device and an n-channel device in parallel, as shown in Figure 23. Output-versus-input characteristics are shown in A, Figure 24 for a single p-channel device, in B, Figure 24 for a single n-channel device, and in C, Figure 24 for a composite device (both devices in parallel). Resistance R_L again is assumed to be large compared to the MOS ON resistance. The composite characteristics are obtained by adding the output voltages V_o, from the individual devices for a given input voltage V_i. The ON characteristic shows that one device is on even when the other device is limiting. The logic levels used to drive the gate (-5 volts in this case) have the same maximum and minimum voltage excursions as those used at the signal-input terminal.

The OFF transfer characteristics for the complementary switch are shown in Figure 25. The composite characteristics (C, Figure 25) are obtained by the procedure described above for the ON condition. The OFF characteristics show that no problems arise when the threshold points are outside the diode points. The junction transistor mechanism mentioned for the single p-channel switch dominates if both units are enchancement types with greater than 0.7 volt. The operating limit for the off condition is +5.7 volts and -5.7 volts.

It has been observed that threshold point T_n of some n-channel devices may be below threshold point Tp of a p-channel device. This condition is shown by Figure 26. This difference in effect creates a dead region, or source of nonlinearity, in the ON transfer characteristics of the comple-

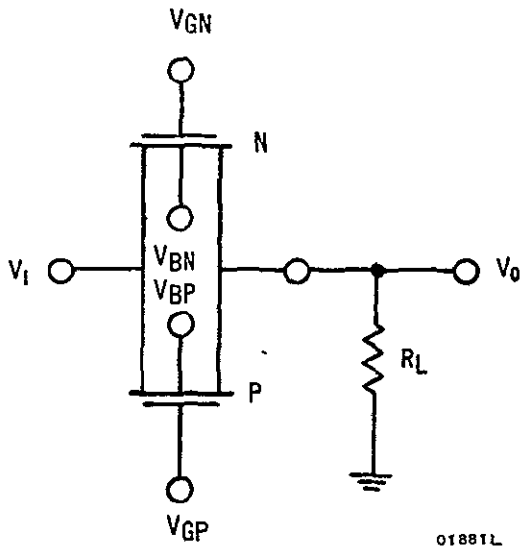


Figure 23. Complementary MOS Multiplex Switch

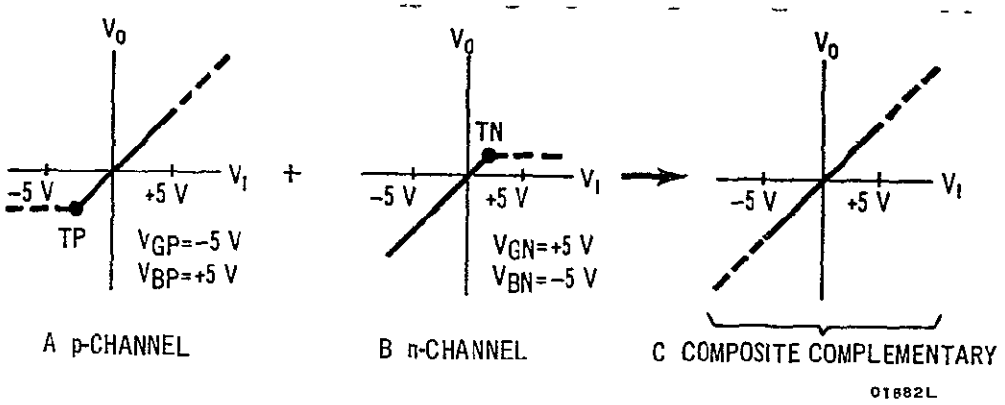


Figure 24 On Transfer Characteristics of Complementary MOS Switch

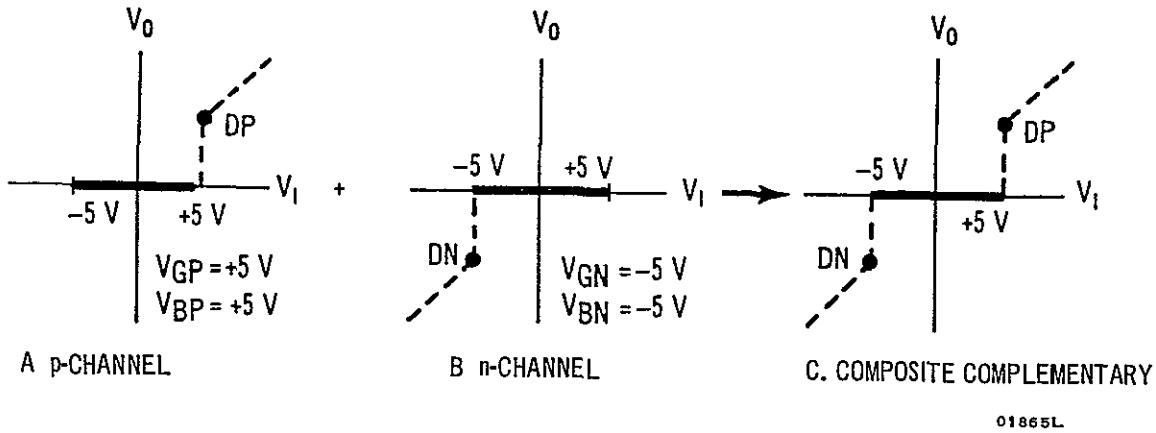


Figure 25 OFF Transfer Characteristics of Complementary MOS Switch

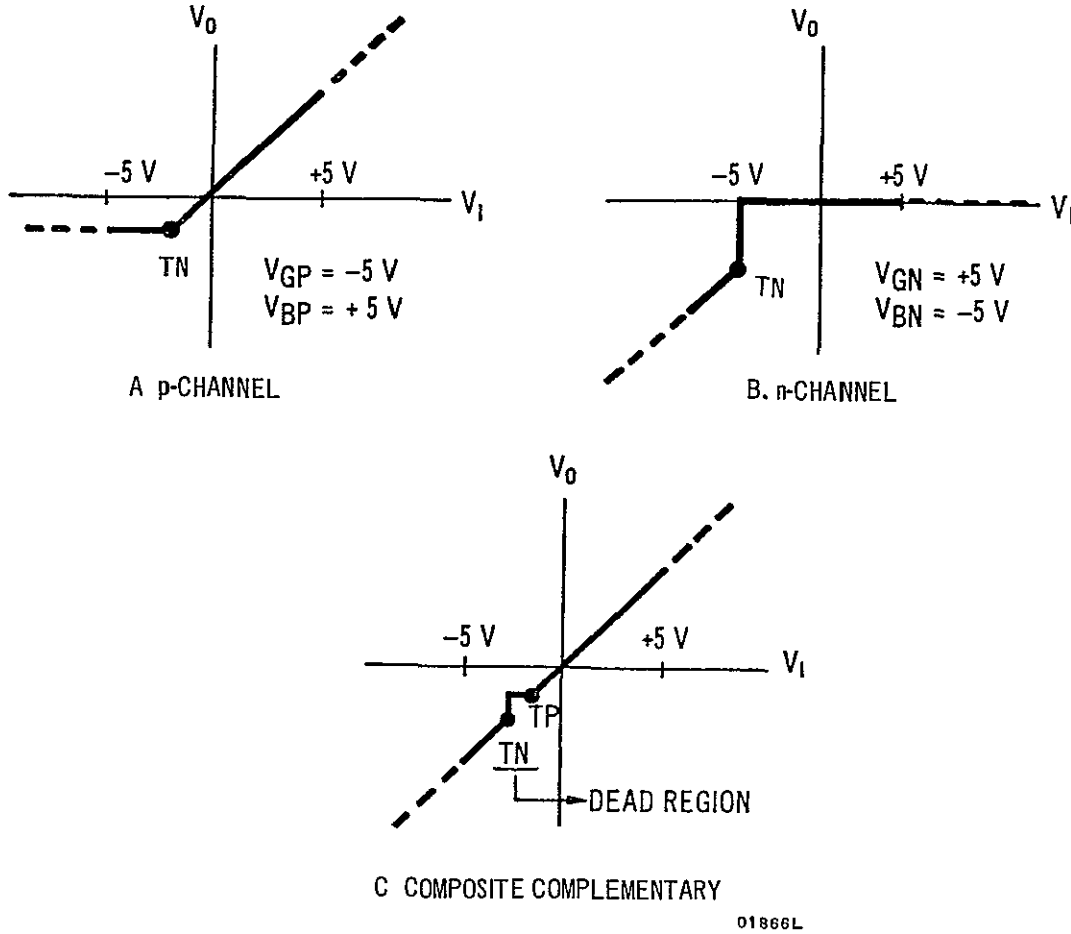


Figure 26. Possible Dead Region in ON Characteristics

mentary switch. This problem can be eliminated by controlling the parameters of the MOS devices. The problem is analyzed in more detail in sections B6, B7, B8, B9, and B10. This condition is related to the threshold voltages of the p-channel and n-channel MOS units, which, in turn, are related to the initial threshold voltage and the substrate-to-source voltage.

5. MULTIPLEX CIRCUITS

The circuits involved in the complementary multiplex system are shown in Figure 27. Four complementary MOS switches are shown upper left in the figure. The gates of the p-channel devices are connected directly to the control inputs, while the gates of the n-channel devices are connected to the inverter. The inverters are connected to the appropriate control input. The complementary inverters supply the addtional inverted logic level needed to drive the complementary MOS switches. The transfer characteristics of these inverters are shown in Figure 28.

6. SUBSTRATE EFFECT

The threshold voltage, V_{GST}, of an MOS device is not constant; it is a function of substrate-to-source voltage V_{BS}. This variation is shown in Figure 29 for both an n-channel device and a p-channel device. The functional relationship of this curve, which was derived from a physical model of the device, seems to agree very closely with an actual device. The substrate-effect relationship is given by equation (4) and equation (5) for an n-channel device and a p-channel device, respectively. Letters n and p in the subscripts denote n-channel and p-channel transistors, respectively.

$$V_{GSTn} = V_{GSTOn} + K_n\left(\sqrt{-V_{BSn} + \phi_{Sn}} - \sqrt{\phi_{Sn}}\right) \quad \ldots\ldots\ldots\ldots (4)$$

$$V_{GSTp} = V_{GSTOp} - K_p\left(\sqrt{V_{BSp} - \phi_{Sp}} - \sqrt{-\phi_{Sp}}\right) \quad \ldots\ldots\ldots\ldots (5)$$

Quantities V_{GSTOn} and V_{GSTOp} are the threshold voltages that apply for zero substrate-to-source voltage. These quantities are functions of the thickness and permittivity of the silicon-oxide layer and of the surface charge of the oxide. Quantities K_p and K_n are constants whose values depend upon the thickness and permittivity of the silicon oxide as well as the concentration and

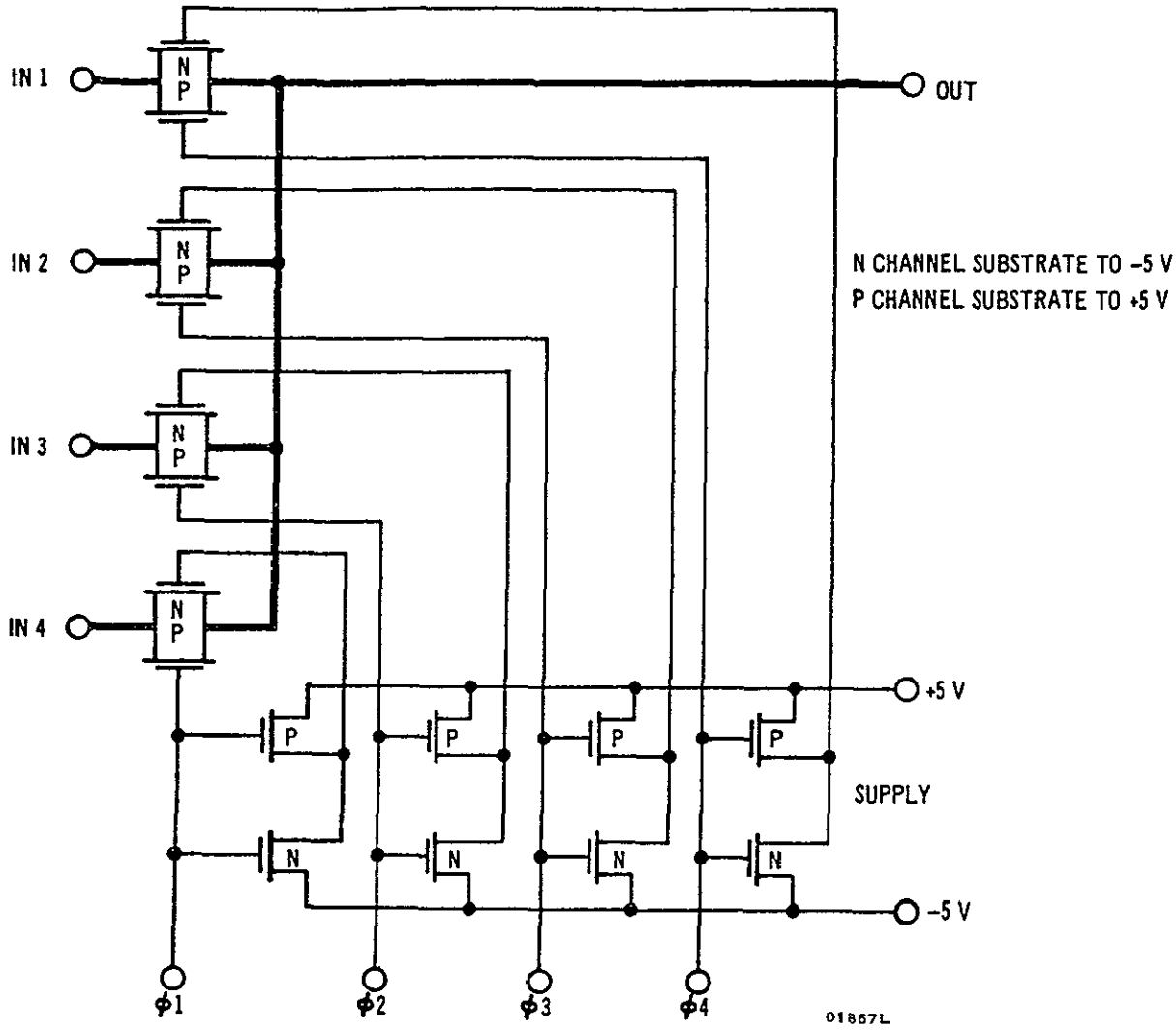


Figure 27. MOS Complementary Multiplex System

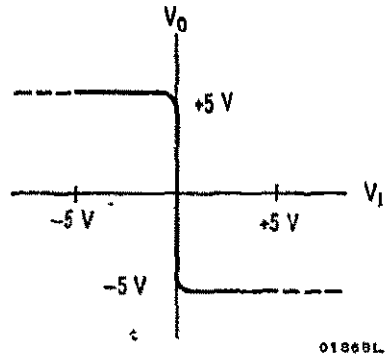


Figure 28. Transfer Characteristics of Complementary Inverter

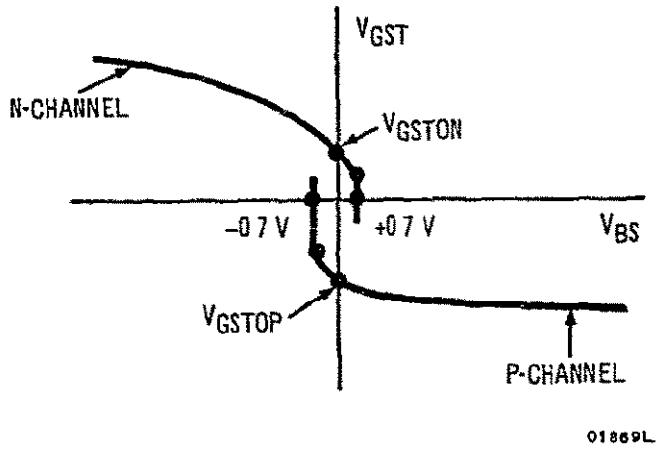


Figure 29. Substrate-Effect Curves

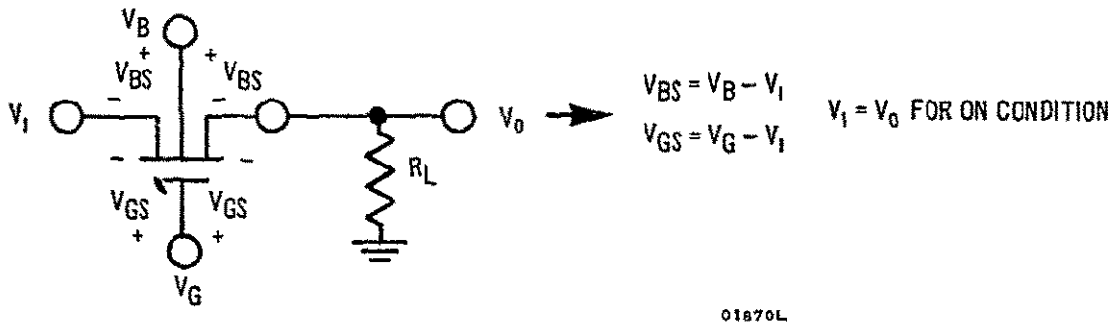


Figure 30. Kirchoff's Voltage Law Applied to MOS Device

permittivity of the silicon substrate. Quantity ϕ_S is twice the change in the Fermi potential, which depends upon the doping concentration. The physical parameters are described in Section B. When $V_{BSn} \geq +0.7$ volt and $V_{BSp} \leq -0.7$ volt, the substrate-to-source junction diode conducts, and the MOS device turns on by the junction transistor mechanism described previously.

7. THRESHOLD POINT ON TRANSFER CHARACTERISTICS

The threshold points shown on the transfer characteristics of Figures 24 and 25 may be obtained either graphically or mathematically if the substrate effect curve is available (either from measurements made on an actual device or from equations (4) and (5). Applying Kirchoff's voltage law to the MOS device shown in Figure 30, equations (6) and (7) are obtained.

$$V_i = V_G - V_{GS} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (6)$$

$$V_i = V_B - V_{BS} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (7)$$

These equations are valid for either an n-channel device or a p-channel device.

Figure 30 shows that voltages V_{GS} and V_{BS} can appear either at the input terminal or the output terminal of the switch. This condition occurs because the source of the device may switch from the input terminal of the MOS to its output terminal, depending upon the direction of current flow through the device. Figure 21 describes graphically the regions in which the two possible modes exist (i.e., common-source mode or source-follower mode) for both p-channel and n-channel devices. Assuming that load resistance R_L is large compared to the ON resistance of the device, output voltage V_o equals input voltage V_i when the MOS is turned on. Equations (6) and (7) are valid, therefore, for the ON condition until the device becomes cut off.

Equations (6) and (7) can be combined to eliminate input voltage V_i. The result is given by equation (8):

$$V_{GS} = V_{BS} + (V_G - V_B) \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (8)$$

To obtain a graphical solution for the value of threshold point T_n, equation (8) is plotted with the substrate-effect curve, which is shown in A,

Figure 31 for an n-channel device. Threshold point T_n occurs at the intersection of both curves. The threshold point on the transfer characteristics (i.e., plot of V_o versus V_1) is obtained by substituting the coordinate value of V_{BSn} (A, Figure 31) into equation (4) and determining the value of V_{1Tn}. The V_{1Tn} can be found by substituting V_{GSTn} into equation (4) for V_{GS}. Threshold point Tp can be found as shown in B, Figure 31.

The threshold point also can be obtained mathematically by susbstituting equation (8) for the appropriate type of channel device into equations (4) and (5). The results are equations (9) and (10) for n-channel and p-channel devices, respectively.

$$V_{GSTn} = V_{GSTOn} - K_n K_n' + K_n \sqrt{(K_n')^2 + ((V_{Gn} - V_{Bn}) - V_{GSTOn})} \quad \ldots (9)$$

where

$$K_n' = \left(\tfrac{1}{2} K_n + \sqrt{\phi_{Sn}} \right)$$

$$V_{GSTp} = V_{GSTOp} + K_p K_p' - K_p \sqrt{\left(K_p'\right)^2 - \left(\left(V_{Gp} - V_{Bp}\right) - V_{GSTOp}\right)} \quad \ldots (10)$$

where

$$K_p' = \left(\tfrac{1}{2} K_p + \sqrt{-\phi_{Sp}} \right)$$

The threshold point on the transfer characteristics can be obtained by substituting the value of V_{GSTn} or V_{GSTp} from equations (9) and (10) for V_{1Tn} and V_{1Tp} in equation (11).

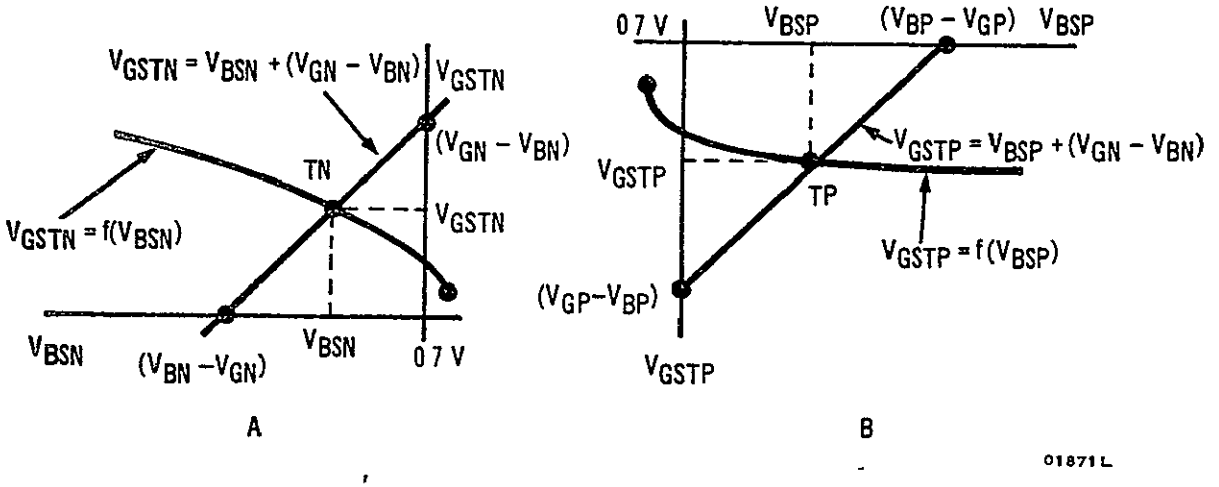


Figure 31. Obtaining Threshold Point for n-Channel Device

8. CRITERION FOR NO DEAD REGION

A problem that can arise on the conducting (ON) transfer characteristics is the formation of a dead region, as shown in C, Figure 26. This discontinuity occurs when the threshold point of the n-channel (T_n) lies below the threshold point of the p-channel (T_p). The discontinuity can be avoided if point T_n lies above or at point T_p; stated mathematically,

$$V_{iTn} \geq V_{iTp} \quad \ldots \quad (11)$$

This criterion can be achieved either by controlling the device parameters or by picking an appropriate logic level. It is the aim of this discussion to obtain a graphic method to show the range under which the aforementioned criterion holds.

In a multiplex system using two symmetrical voltage levels (i.e., V_{LL} and $-V_{LL}$) to drive the gates of the complementary MOS switches, gate voltage V_G, and substrate voltage V_B for the ON condition can be defined for both channel devices as follows:

$$V_{LL} \triangleq V_{Gn} \triangleq -V_{Gp} \triangleq -V_{Bn} \triangleq V_{Bp} \quad \ldots \quad (12)$$

Methods of obtaining the threshold point from the substrate-effect curves when applied to the device were described in Section B. This graphic procedure is shown again, for convenience, for an n-channel device in A, Figure 32. When equation (12) is applied to the graph, a new graph is obtained, as shown in B, Figure 32. From equation (9) ($V_{iTn} = V_{Gn} - V_{GSTn}$) and using the appropriate definition stated by equation (12),

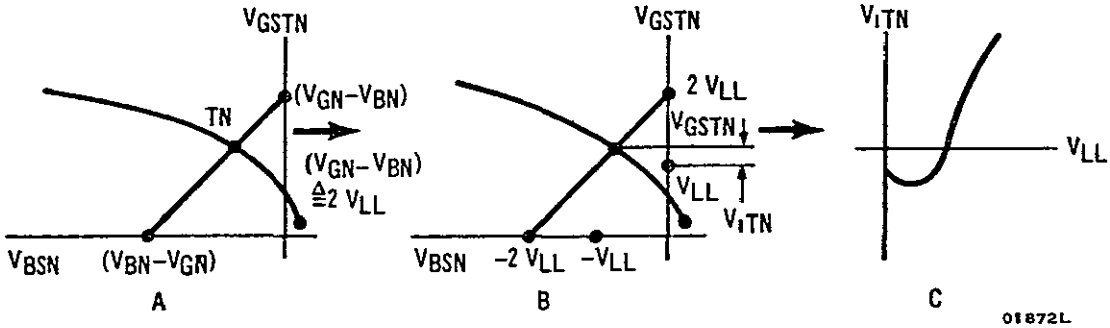


Figure 32. Obtaining Characteristics of Threshold Point versus Logic Level for n-Channel Devices

$$V_{iTn} = V_{LL} - V_{GSTn} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (13)$$

Equation (13) can be interpreted graphically as shown in B, Figure 32. Values of V_{iTn} (threshold point) can be obtained from B, Figure 32, as a function of V_{LL} (logic level) and the results are plotted as shown in C, Figure 32. This curve also can be obtained mathematically using equations (9) and (13) and the appropriate definition given by equation (12). The results are given by equation (14):

$$V_{iTn} = V_{LL} - V_{GSTOn} + K_n K_n' - K_n \sqrt{(K_n')^2 + (2V_{LL} - V_{GSTOn})} \quad \ldots \quad (14)$$

where

$$K_n' = \tfrac{1}{2} K_n + \sqrt{\phi_{Sn}}$$

The curve that equation (14) represents in C, Figure 32, consists of two components that depend on V_{LL}. The first component is linear term V_{LL}, the second term is square-root term $-K_n \sqrt{(K_n'^2) + (2V_{LL} - V_{GSTOn})}$. The curve shows that the square-root term dominates for small values of V_{LL}, however, the linear term becomes dominant as V_{LL} increases. The significance of this relationship will be mentioned subsequently. For convenience, the location of the minima on the plot is given by equation (15):

$$V_{LL} = \tfrac{1}{2} \left(V_{GSTOn} + K_n^2 - (K_n')^2\right) \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (15)$$

The general procedure for an n-channel device applies also to a p-channel device. The characteristics of A, Figure 33, and equation (12) can be used to obtain the characteristics of B, Figure 33. From equation (6) and the definitions given by equation (12), equation (16) is obtained, which is represented graphically in B, Figure 33.

$$V_{iTp} = - V_{LL} - V_{GSTp} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots \quad (16)$$

The threshold voltage V_{iTp} now can be plotted as a function of logic level V_{LL}, as shown in C, Figure 33. The curve also can be obtained mathematically by using equation (16), equation (10) and equation (12) The result is equation (17):

$$V_{iTp} = - V_{LL} - V_{GSTOp} - K_p K_p' + K_p \sqrt{(K_p')^2 + (2V_{LL} + V_{GSTOp})} \quad \ldots \quad (17)$$

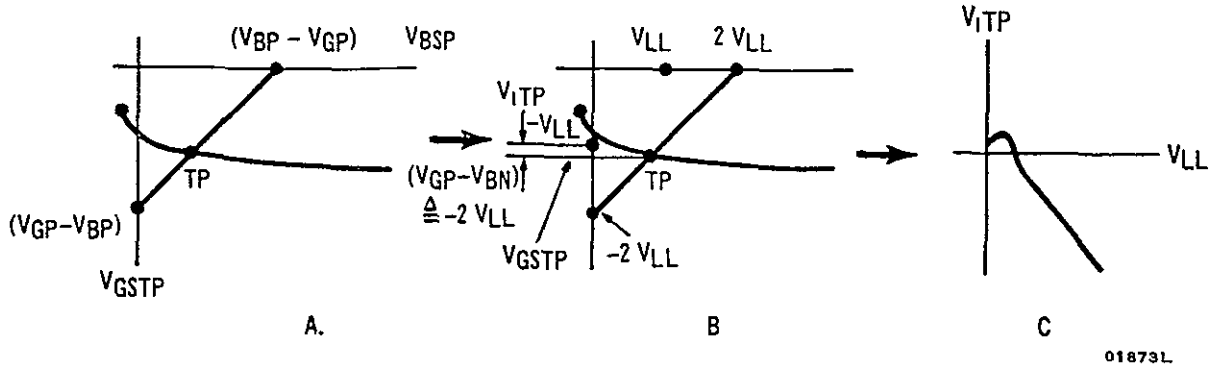


Figure 33. Obtaining Characteristics of Threshold Point versus Logic Level for p-Channel Devices

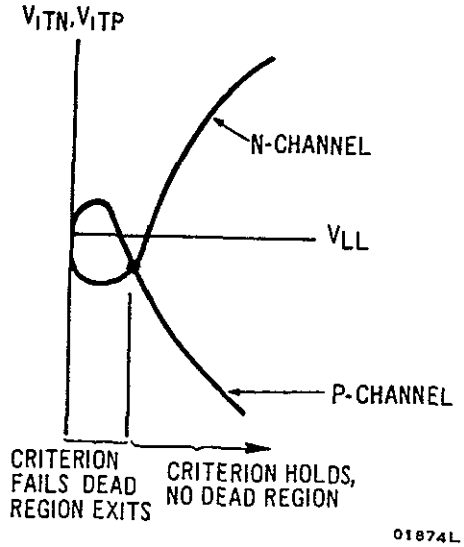


Figure 34. Characteristics of Threshold Point versus Logic Level for Complementary Devices

where

$$K_p' = \tfrac{1}{2} K_p + \sqrt{-\phi_{Sp}}$$

The location of the maxima of equation (17) is given by equation (18)

$$V_{LL} = \tfrac{1}{2}\left(-V_{GSTOp} + K_p^2 - (K_p')^2\right) \quad \ldots\ldots\ldots\ldots \quad (18)$$

The criterion given by equation (11) may be applied when the curves of C, Figure 32, and C, Figure 33 are plotted on the same coordinates (Figure 34). The right of the intersection of the resulting curves shows when the criterion of equation (11) holds. Operation with V_{LL} in this region results and there is no dead region on the transfer characteristics. If a smaller value of V_{LL} is used, a dead region would result the size of which is determined between the two values represented by the curves for V_{LL}. Device parameters (e.g., V_{GSTO} and K) determine the intersection or minimum logic level. At a sacrifice in logic-noise-level immunity, the intersection can be moved to the left for operation by changing substrate resistivities, thus lowering device thresholds.

9. DEFINITIONS OF DEVICE PARAMETERS FROM PHYSICAL PARAMETERS

The minimum logic level that can be used depends upon device parameters V_{GSTO} and K. These parameters depend upon certain physical parameters that are associated with the MOS transistor. Device parameters are given in terms of the physical parameters in the following equations for both p-channel and n-channel devices.

For a p-channel device, the threshold voltage V_{GSTOp} and parameter K_p are given as:

$$V_{GSTOp} = -\frac{\sigma_{Bp}}{C_{ox}} + \phi_{Sp} - \frac{\sigma_{SSp}}{C_{ox}} + \phi_{MSp} \quad \ldots\ldots\ldots\ldots \quad (19)$$

$$K_p = \frac{\gamma_p}{C_{ox}} \quad \ldots\ldots\ldots\ldots \quad (20)$$

where

$$C_{ox} = \frac{\varepsilon_{ox}}{T_{ox}}$$

$$\sigma_{Bp} = +\gamma_p \sqrt{-\phi_{Sp}}$$

$$\gamma_p = \sqrt{2q\epsilon_S N_D}$$

$$\phi Sp = -2\frac{kT}{q}\ \ell n\ \frac{N_D}{n_1} \quad \text{(twice the change in the Fermi level)}$$

$$\sigma_{SSp} = q\ N_{SSp}$$

$$\phi_{MSp} = -0.6 - \frac{1}{2}\phi_{SP} \quad \text{(for aluminum metalization)}$$

ϵ_S = permittivity of Si (104×10^{-14} F/cm)

ϵ_{ox} = permittivity of SiO_2 (35.4×10^{-14} F/cm)

k = Boltzmann's constant ($1\ 38 \times 10^{-23}$ J/^oK)

n_1 = intrinsic concentration of Si (1.45×10^{10} cm^{-3} at 300^oK)

N_D = doping concentration of substrate (cm^{-3})(donor)

N_{SSp} = surface state concentration (cm^{-2})

q = electric charge (1.602×10^{-19} coulombs/electron)

T = temperature (^oK)

T_{ox} = thickness of oxide

For an n-channel device, the threshold voltage V_{GSTOn} and the parameter K_n are given as

$$V_{GSTOn} = -\frac{\sigma_{Rn}}{C_{ox}} + \phi_{Sn} - \frac{\phi_{SSn}}{C_{ox}} + \phi_{MSn} \quad \ldots \quad (21)$$

$$K_n = \frac{\gamma_n}{C_{ox}} \quad \ldots \quad (22)$$

where

$$C_{ox} = \frac{\varepsilon_{ox}}{T_{ox}}$$

$$\sigma_{Bn} = -\gamma_n \sqrt{\phi_{Sn}}$$

$$\gamma_n = \sqrt{2q\varepsilon_S N_A}$$

$$\phi_{Sn} = 2 \frac{kT}{q} \ell n \frac{N_A}{n_i} \quad \text{(twice the Fermi level)}$$

$$\sigma_{SSn} = q N_{SSn}$$

$$\phi_{MSn} = -0.6 - \frac{1}{2} \phi_{Sn} \quad \text{(for aluminum metalization)}$$

N_A = doping concentration of substrate (cm^{-3})(acceptor)

N_{SSn} = surface state concentration (cm^{-2})

10. COMPUTER ANALYSIS TO DETERMINE DEAD REGIONS

In Section B8 the equations (Eqs. 14 and 17) representing threshold points of the p- and n-channel devices as a function of logic level (V_{LL}) and device parameters (V_{GSTO}, K, K') were developed. Figure 34 shows a rough plot of those equations and gives information as to the minimum logic level, $V_{LL\ min}$ needed to ensure no dead regions, and the size of the dead regions if logic levels are used below this minimum logic level. In Section B9 the device parameters were defined in terms of the physical parameters (e.g., T_{ox}, N_D, N_A, N_{SSp}, and N_{SSn}). With this information a numerical family of threshold point vs logic level curves can be established,as a function of the physical parameters. The curves are shown in Figures 35, 36 and 37.

By examining the family of curves, certain trends can be established as to how the multiplexer IC should be processed. Figures 35, 36 and 37

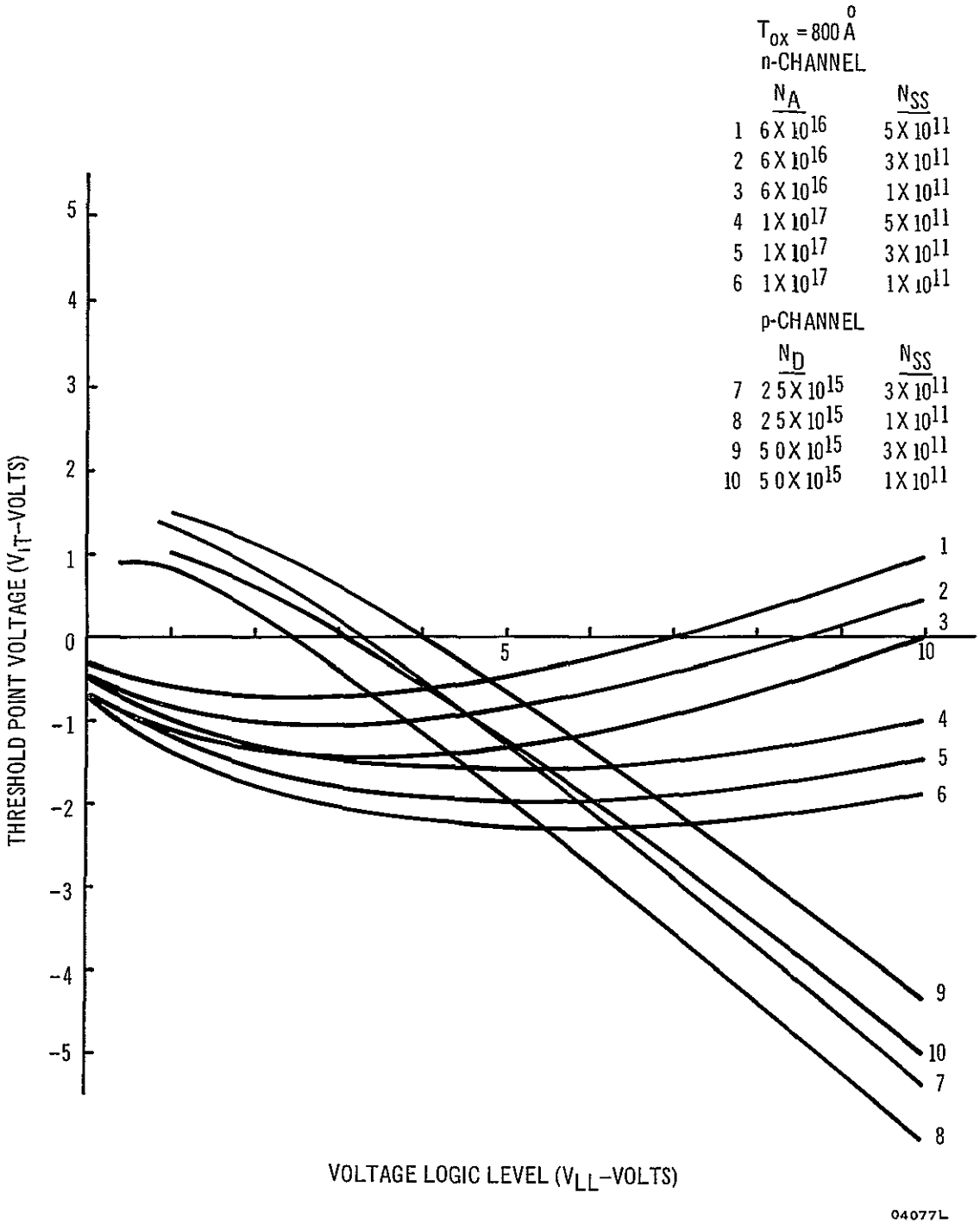


Figure 35. Family of Threshold Point vs. Logic Level Curves (T_{ox} = 800 Å)

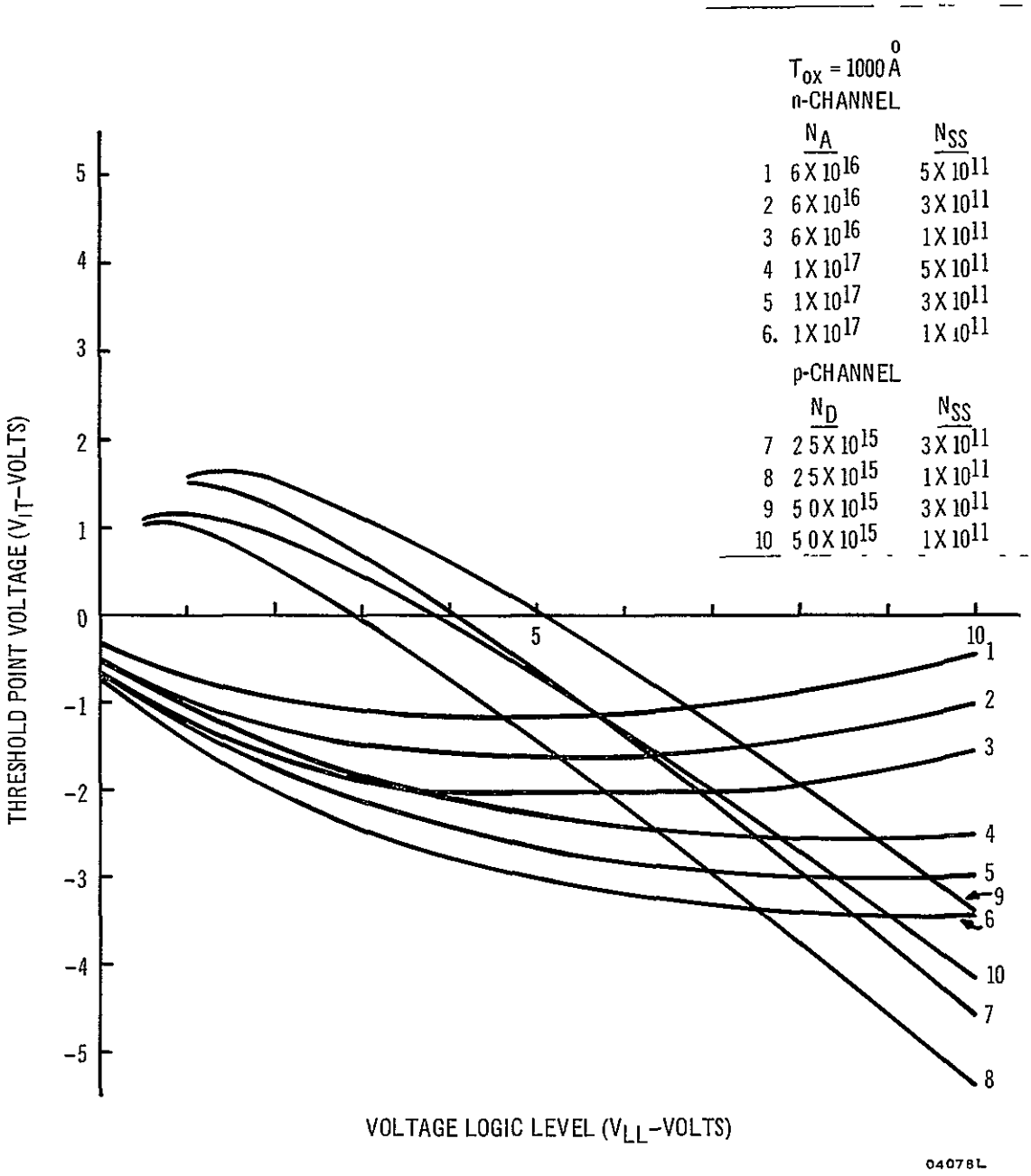


Figure 36. Family of Threshold Point vs. Logic Level Curves (T_{ox} = 1000 Å)

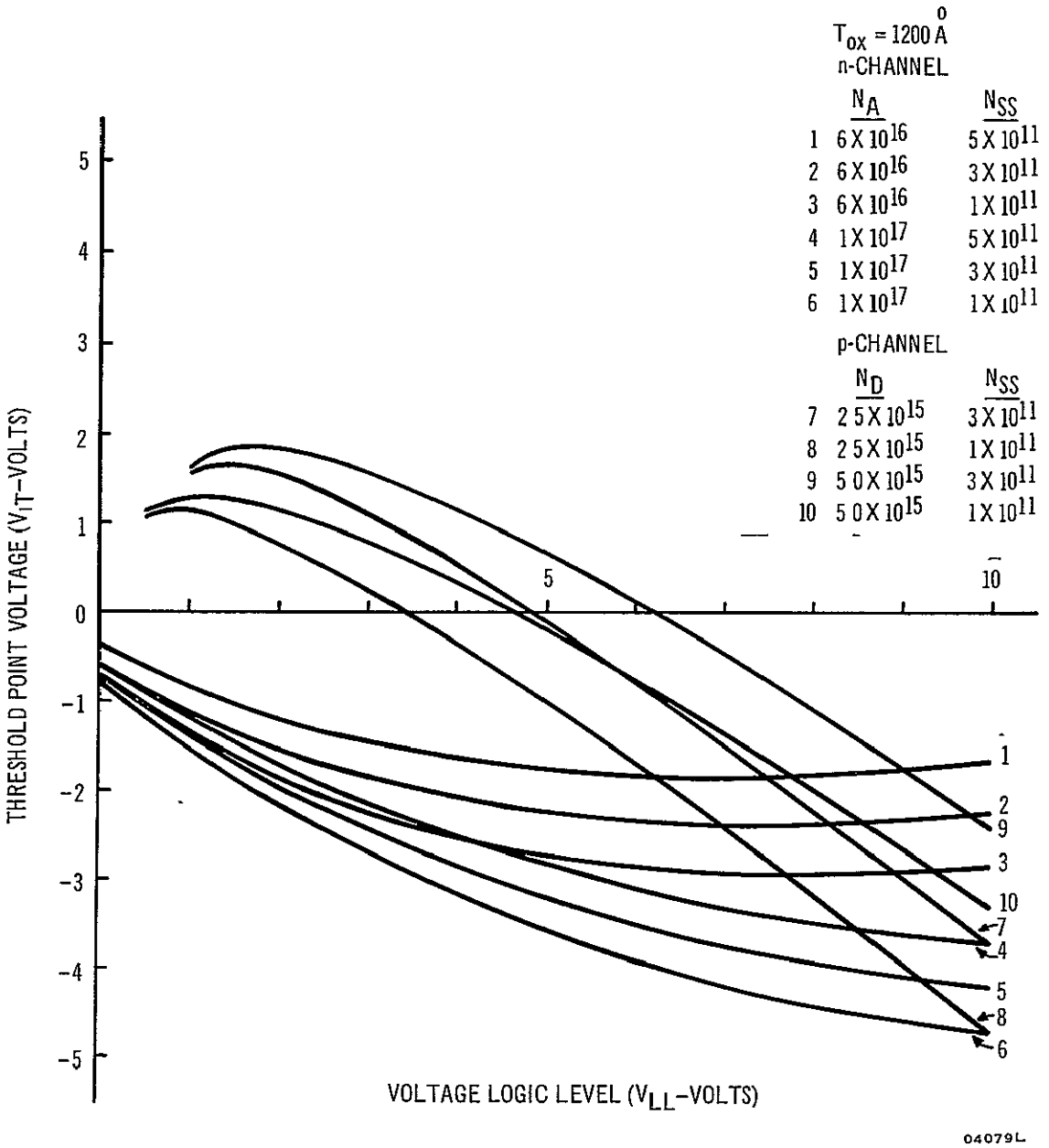


Figure 37 Family of Threshold Point vs Logic Level Curves (T_{ox} = 1200 Å)

show that curve 8 (p-channel device, $N_D = 2.5 \times 10^{15}$ cm^{-3}, $N_{SSp} = 1 \times 10^{11}$ cm^{-2}) and curve 1 (n-channel device, $N_A = 6 \times 10^{16}$ cm^{-3}, $N_{SSn} = 5 \times 10^{11}$ cm^{-2}) produces the lowest minimum logic level and the lowest dead region size compared to any other combination of curves. It can be concluded from this that the substrate doping level (N_A and N_D) should be kept as low as possible, that the p-channel surface state concentration (N_{SSp}) be kept low, and that the n-channel surface state concentration be kept high. From measurements made on actual integrated MOS devices it is found that the p-channels have surface-state concentrations much lower than the n-channel surface-state concentrations. The higher surface-state concentration for the n-channel, although desirable for the multiplexer switch is undesirable for the logic circuits in the multiplexer. The reason for this is that the n-channel threshold voltage will decrease with an increase of surface-state concentration, thus lowering the noise immunity of the logic circuits. In general, surface-state concentrations should be kept as low as possible to ensure good device stability. Noise immunity also decreases with a decrease of substrate doping concentration since the threshold voltage (V_{GST}) is proportional to doping concentration. Figures 33, 34, and 35 (T_{ox} = 800 Å, 1000 Å, and 1200 Å, respectively) shows that the minimum logic level point, for curve 8 and curve 1, increases with oxide thickness. Due to this relationship the oxide thickness should, therefore, be kept as thin as possible.

It can be concluded that the minimum practical logic level established for an overall good and consistent MOS performance must compromise the minimum logic level. Technological developments, however, can alter the degree of this compromise.

C. EVALUATION OF INTEGRATED MULTIPLEXER

Figures 38 and 39 show statistical plots of current for multiplexers tested early (lots 1 to 6. 24 units) and for later units (lots 7 to 8: 13 units). Each lot was measured dynamically in the sequential access mode at a supply voltage of 10 volts (symmetrical logic level of 5 volts) with a clock frequency of 10 kilohertz. The units used were selected on the basis that· (1) all four counter stages were operative under the sequential access mode at 10 kilohertz, (2) all four counter stages could be initiated by means of an

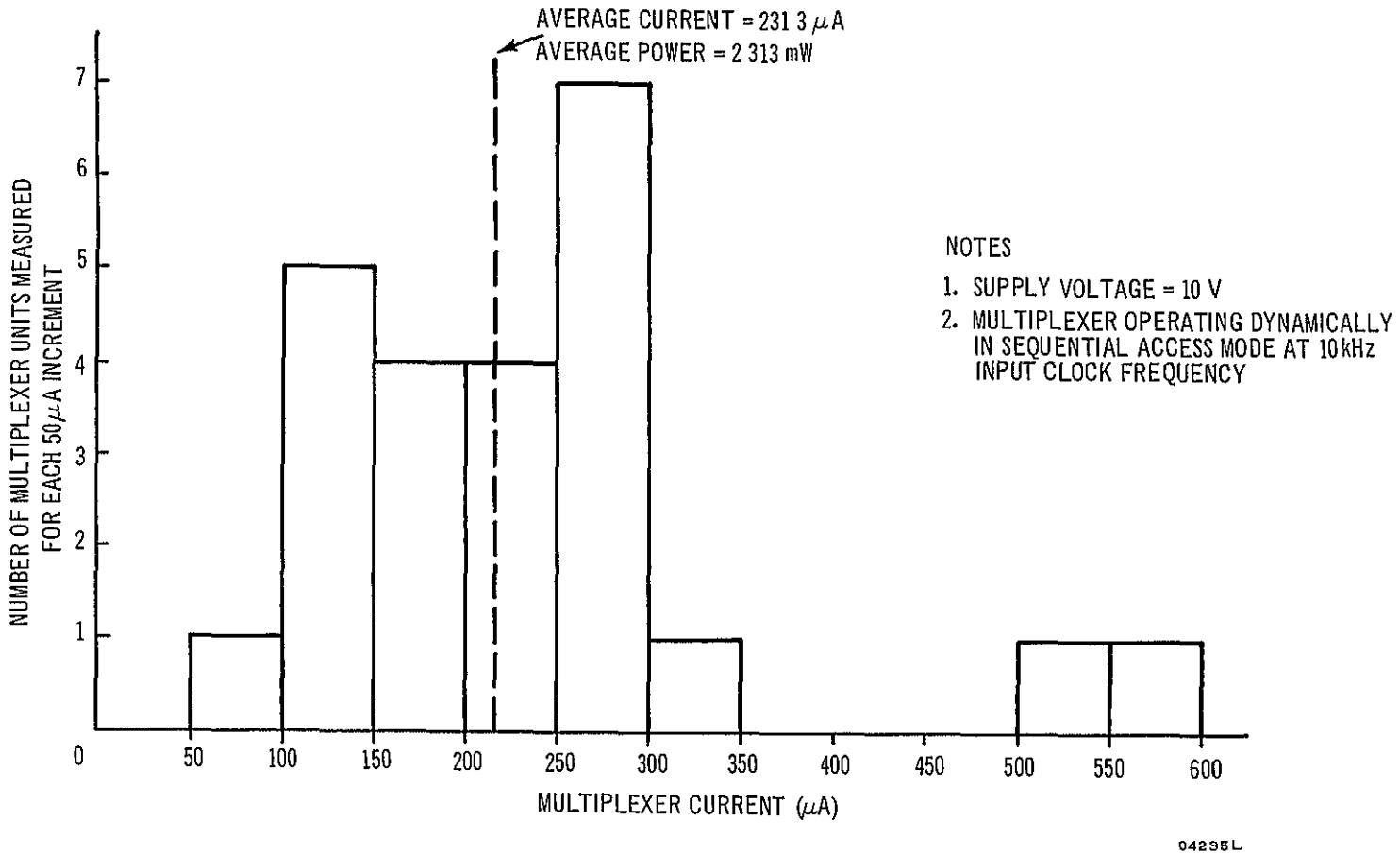


Figure 38. Statistical Plot of Multiplexer Current for 24 Units (Lots 1 to 6)

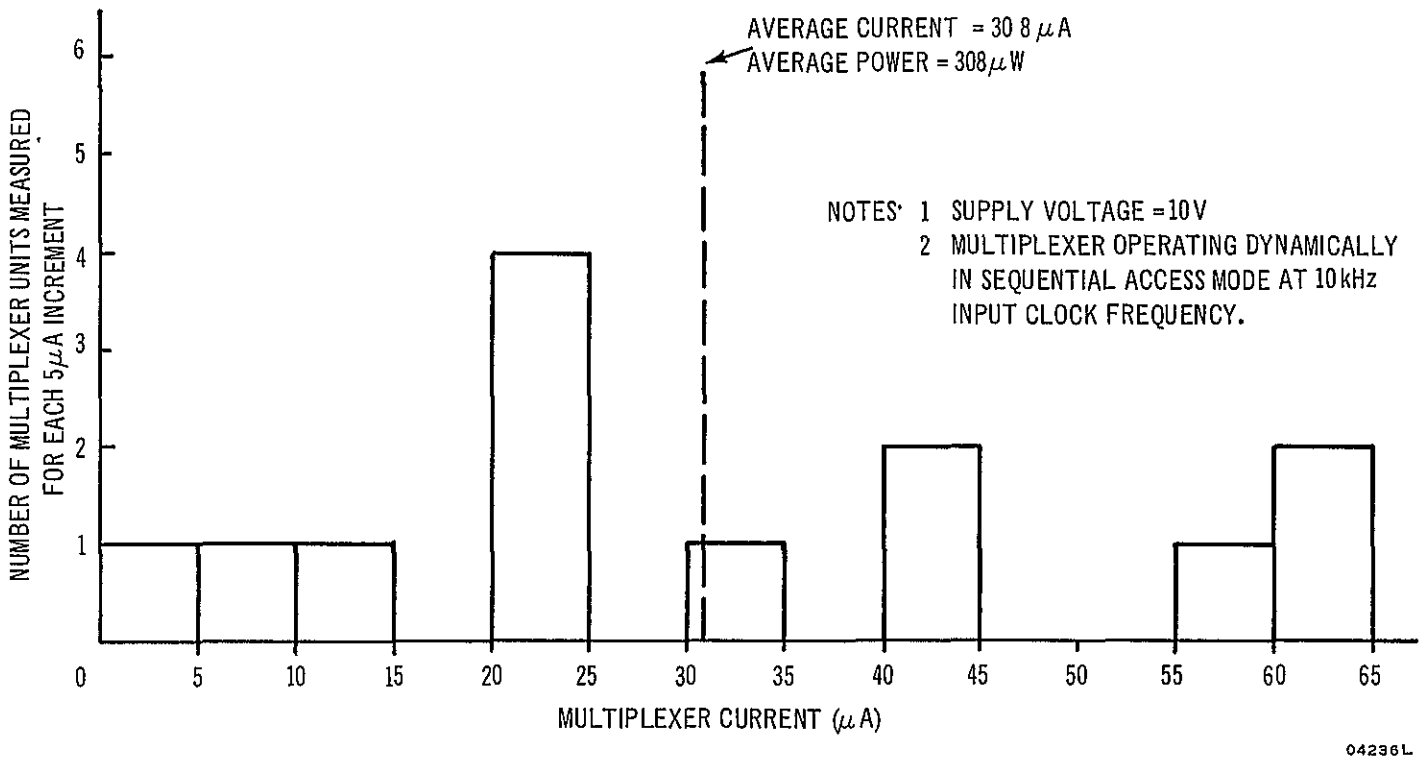


Figure 39. Statistical Plot of Multiplexer Current for 13 Units (Lots 7 to 8)

enable pulse to the binary input addresser C$_D$C$_1$C$_2$C$_3$ = 1000, 0100, 0010, 0001 (3) there were at least 13 operating multiplexer switches; and (4) multiplexer currents did not deviate so drastically as to be statistically meaningless. Two plots were used rather than incorporate the results into one plot, since a significant improvement in multiplexer current was noted in the later lots. As shown, the early lots had a statistical average current of 231.3 microamperes (power was 2.313 milliwatts), while the later lots had a statistical average current of 30.8 microamperes (power was 0.308 milliwatts). The lowest current observed for a totally operative unit was 6 milliamperes at 10 volts, and the largest current observed for a totally operative unit was about 3 milliamperes at 10 volts.

The greatest clock frequency that could provide a proper counting operation in the counter stage was measured to be 2 megahertz at 10 volts Operation was observed to improve with increasing supply voltage. Although 2 megahertz was the greatest clock frequency observed, it is not a practical sampling rate for the multiplexer in the sequential access mode. Practical maximum input clock frequencies ranging from 250 to 500 kilohertz are felt to be reasonable (the variation is due to differences in processing from lot to lot). The counter is designed to be used down to DC.

The ON resistance of a multiplexer switch at a given supply voltage (V_{SUP} = 2 V_{LL}; V_{LL} = logic level voltage) was measured with the test setup shown in Figure 40. The sinusoidal generator provided a signal having a peak-to-peak value equal to V_{SUP} and having a frequency of 100 hertz for this test. The oscilloscope depicts the V_{DS} vs. I_D (= V_O/R_L) characteristic of the switch where the slope of the curve represents the resistance of the switch. Since the characteristic is nonlinear a generalized technique is used to measure the overall resistance of the switch. In this method, a convenient V_O/V_{DS} ratio (i.e., 1/1, 1/10, or 1/100) is selected representing the amount of voltage drop that is desired to appear across the switch (in practice V_O/V_{DS} should be as small as possible). The characteristic is then adjusted to fit an imaginary 45 degree line intersecting the origin by varying the load resistor R_L. The switch resistance R_{DS} can be calculated, since V_O/V_{DS} is selected, R_L is measured, and from the circuit $V_O/V_{DS} = R_L/R_{DS}$. Figure 41 shows the

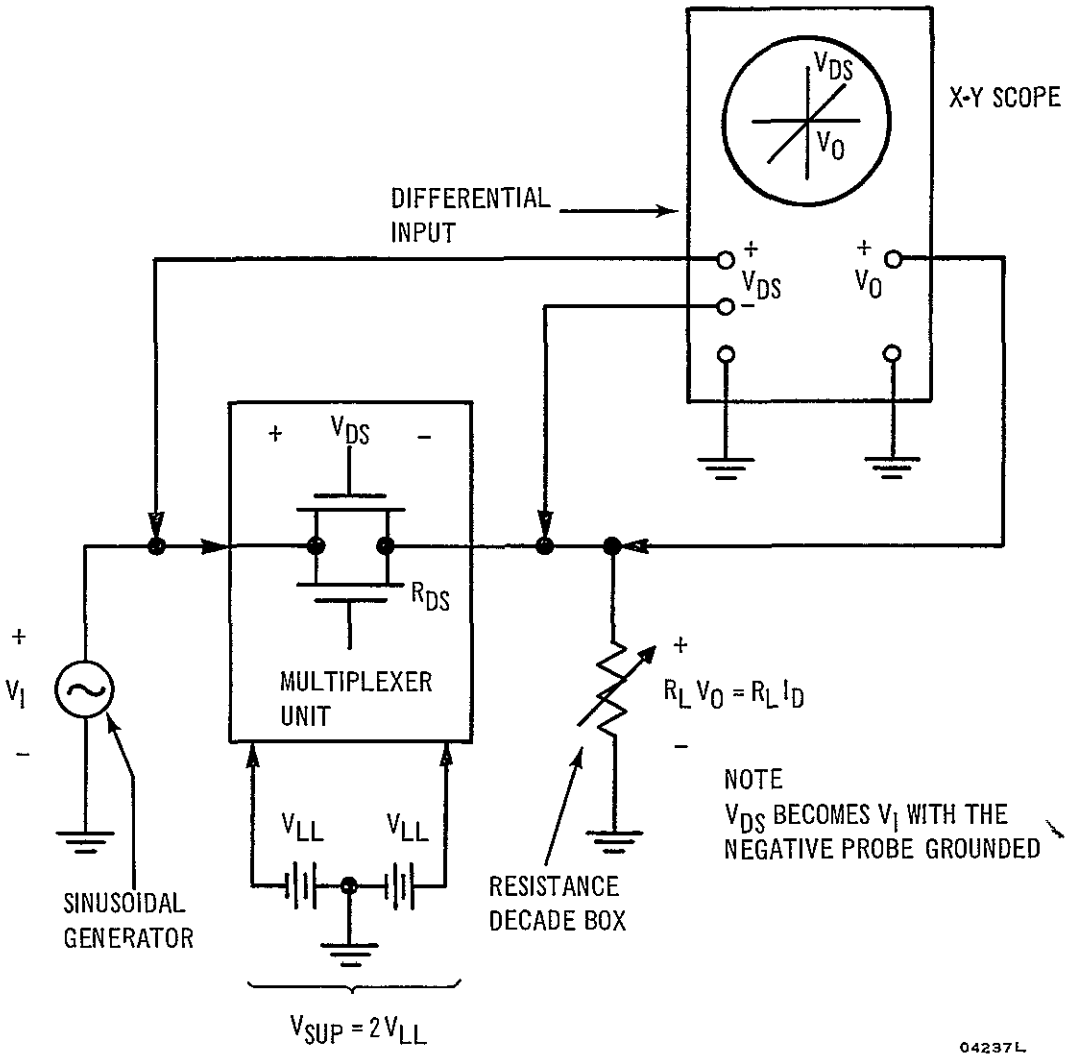
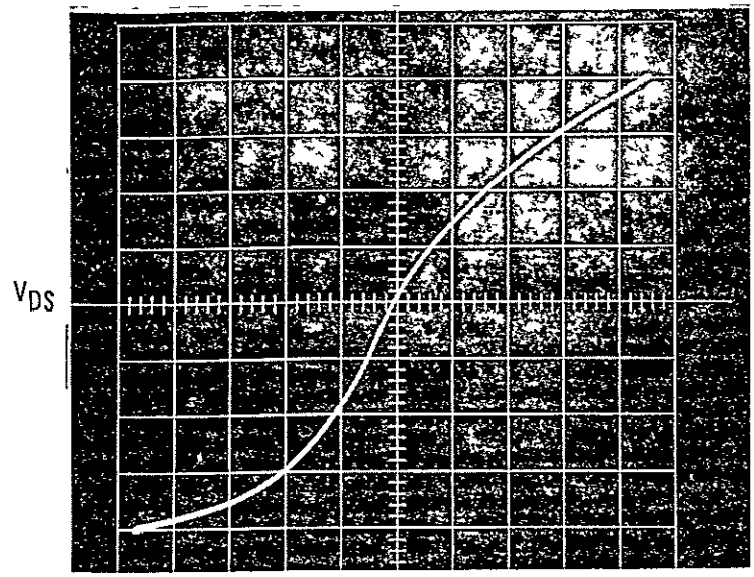


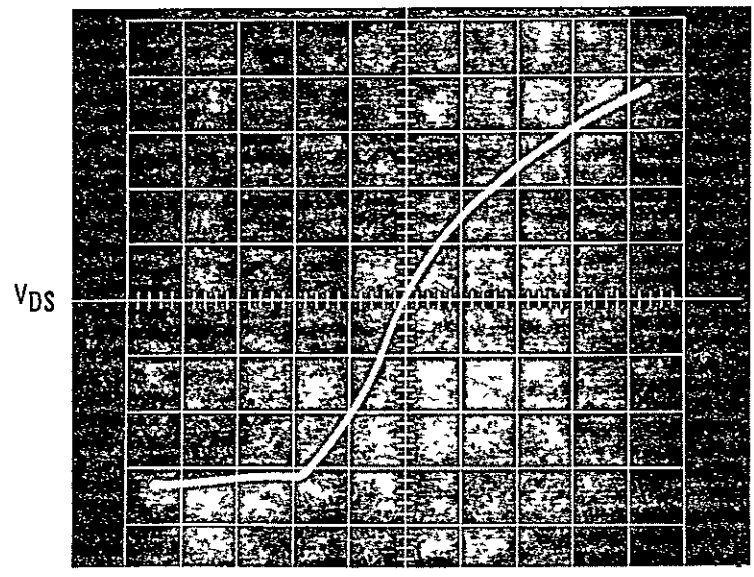
Figure 40 Test Set-up for Measuring Multiplexer Switch On Resistance



04245P

NOTE V_D, I_D = 0 5 V/DIV , 270 μA/DIV
V_{DS} = 0 5 V/DIV

Figure 41 V_{DS} vs I_D Characteristic of Multiplexer Switch



04233P

NOTE V_O, I_D = 1 V/DIV., 55 5 μA/DIV.
V_{DS} = 0 1 V/DIV

Figure 42. V_{DS} vs I_D Characteristic of Multiplexer Switch

characteristic for a V_O/V_{DS} ratio of 1 (i.e., the voltage drop between R_{DS} and R_L is 1:1) for a 45-degree line fitting. From the load resistor decade box, R_L is read out to be 1,800 ohms for this 45-degree line fitting, so that R_{DS} has an average resistance of about 1,800 ohms. Figure 42 shows the characteristic for a V_O/V_{DS} ratio of 1/10 for a 45-degree line fitting. From the load resistor decade box, R_L is read out to be 18,000 ohms, so that R_{DS} has an average resistance of about 1,800 ohms. It is to be noted that although the extent of nonlinearities are different for both cases, the switch ON resistance R_{DS} is about the same. Figure 43 shows a graph of R_{DS} as a function of the supply voltage V_{SUP} for two typical multiplexer units out of two lots. It is seen that as V_{SUP} increases R_{DS} decreases in anticipation of Eq. (3) The reference switch on the multiplexer was designed with MOS device widths half the size of the regular multiplexer switches so that the ON resistance is twice as large.

A sequence of photographs showing the V_{DS} vs. I_D (= V_O/R_L, R_L = 100 kΩ) characteristic of a multiplexer switch in the ON condition are given in Figure 44, views A1, B1, C1, D1, E1, and F1. As shown in the sequence, an increase of supply voltage (V_{SUP}) (i.e., from 4 volts to 9 volts) results in characteristics that approach the characteristic of an ideal switch. (The last picture shows the OFF characteristic in addition to the ON characteristic.) For low values of V_{SUP} a high resistance valley occurs due to the dead region described in Section B8 and shown in the corresponding sequence of photographs in Figure 44 Figure 44, views A2, B2, C2, D2, E2, and F2, shows a sequence of photographs illustrating the transfer characteristics (V_O vs. V_I) of the multiplexer switch for the same increases of supply voltage Note that the coordinate axes are interchanged (flipped around) from those depicted in the figures of Section B8 due to the arrangement of the test setup (Figure 40) The transfer characteristics show the migration and size reduction of the dead region (until it disappears) that occur with increasing supply voltage. The last photograph shows, for all practical purposes, an idealized ON transfer characteristic of the multiplexer switch (45-degree line) and, for completeness, an OFF transfer characteristic (vertical line).

From such transfer characteristics the dead region (in terms of the n- and p-channel threshold points) may be plotted as a function of logic level voltage

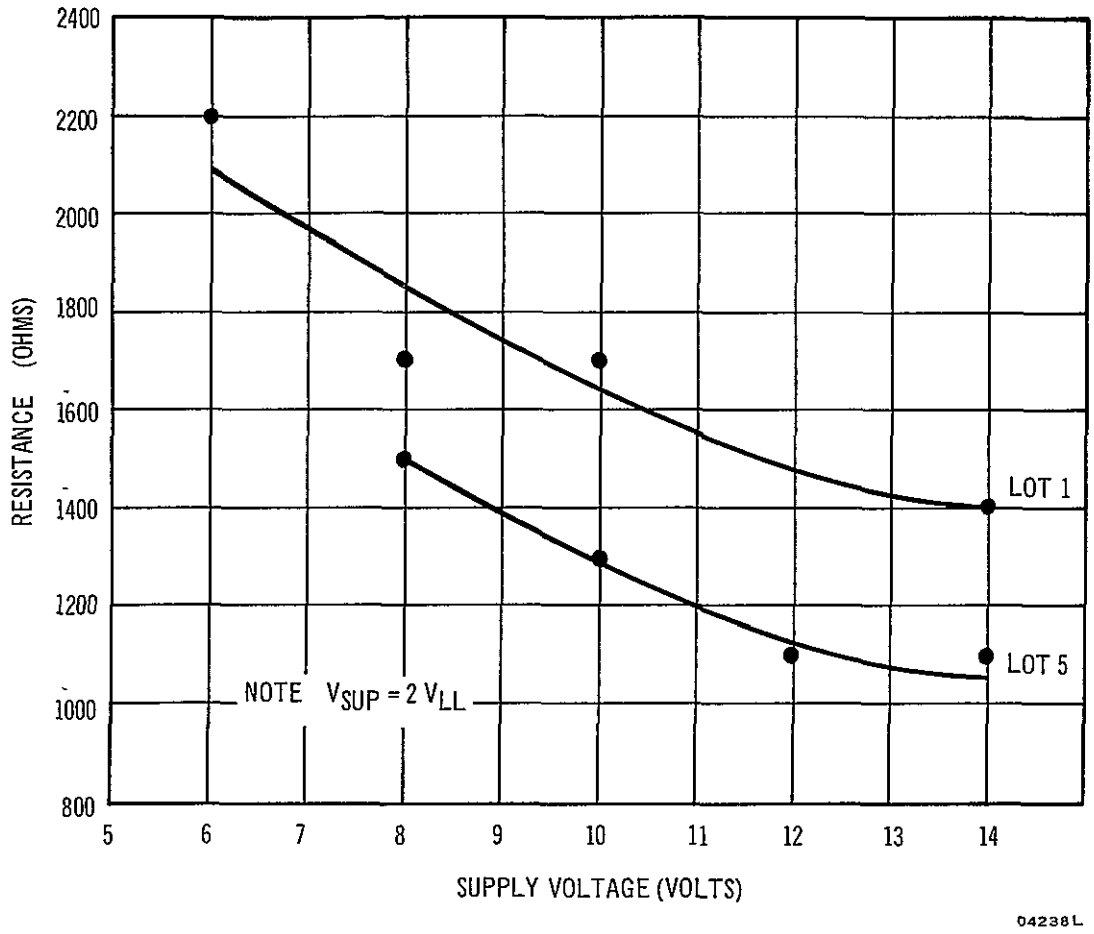
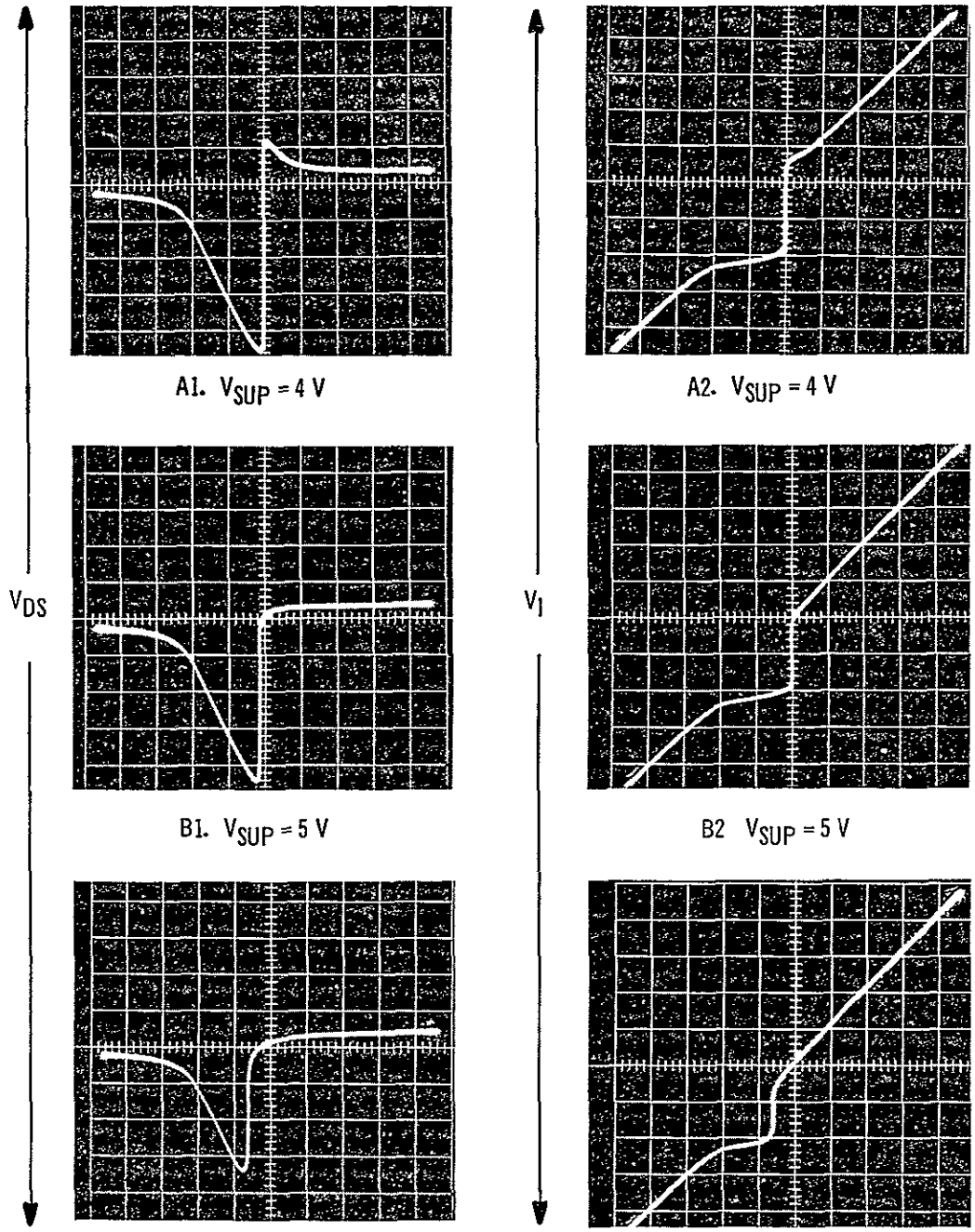


Figure 43 Multiplexer Switch on Resistance (R_{DS}) vs Supply Voltage (V_{SUP})



NOTES 1 V_O, I_D = 0 5 V/DIV , 5μA/DIV , V_{DS} = 0.2 V/DIV.

2 V_O = 0 5 V/DIV , V_I = 0 5 V/DIV

04225P

Figure 44 Voltage and Current Characteristic of Multiplexer Switch in On Condition (Sheet 1 of 2)

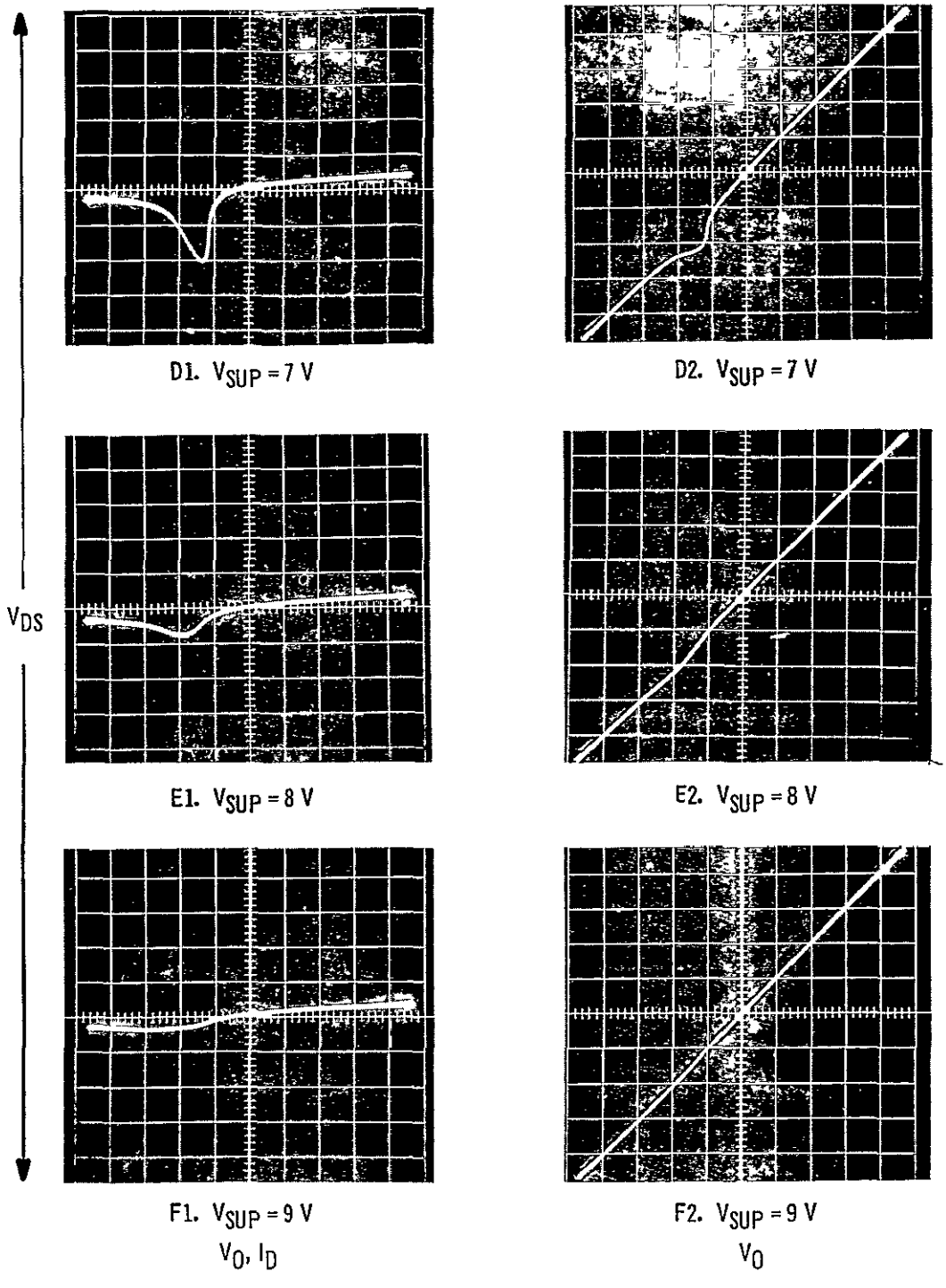


Figure 44 Voltage and Current Characteristic of Multiplexer Switch in On Condition (Sheet 2 of 2)

(V_{LL} = 0.5 V_{SUP}) and is shown plotted in Figure 45 for two multiplexer units designated as lot 1 and lot 5. A comparison can be made between these measured curves and the theoretical curves shown in Figure 36 for identical oxide thickness of 1000 Å. For lot 5 in Figure 45 the p-channel portion of the curve fits for all practical purposes with curve 8 of Figure 36, so that the doping concentration and surface state concentration would be very close to 2.5 x 10^{15} cm^{-3} and 1 x 10^{11} cm^{-2}, respectively. The p-channel portion of lot 1 shows that the shape and slope of the curve is the same but shifted downward compared to the lot 5 curve, which indicates the same doping concentration but a lighter surface state concentration. The n-channel portion of the lot 1 and lot 5 curves show that a greater variation in doping concentration occurs, and compares respectively to curve 1 (6 x 10^{11} cm^{-3}) and curve 4 (1 x 10^{17} cm^{-3}) of Figure 36. The surface state concentration for the n-channel devices in both lot 1 and 5 are roughly the same (i.e., 5 x 10^{11} cm^{-2}). The uniformity in doping concentration for the p-channels and the variation for doping concentration for the n-channels are expected, since the p-channels are processed in the uniformly doped substrate while the n-channels are processed in wells diffused into the substrate in a later phase of the COS/MOS process. The surface state concentration of the n-channel devices are higher than that of the p-channel device since more process steps are required to produce the n-channel devices. As mentioned in Section B8 the dead region can be reduced by having lightly doped substrate and well concentrations while p-channel surface state concentration is small and n-channel surface state concentration can be large.

The distortion that results in the output wave shape of a multiplex switch can be attributed to two factors, (1) the square law characteristic of the n- and p-channel devices and (2) the dead region (shown in Figure 44, views A2, B2, C2, D2, E2, and F2. The distortion due to the square law characteristics can be reduced by increasing the load resistor R_L (it is recommended that R_L be greater than 10 times the switch ON resistance R_S), since a smaller voltage drop (V_{DS}) appears across the multiplex switch providing a more linear operation. The distortion due to the dead region (for a given process) can be eliminated by operating the multiplexer unit beyond the minimum logic level (in Figure 45, minimum logic level for lot 1 is 4 volts for a supply voltage

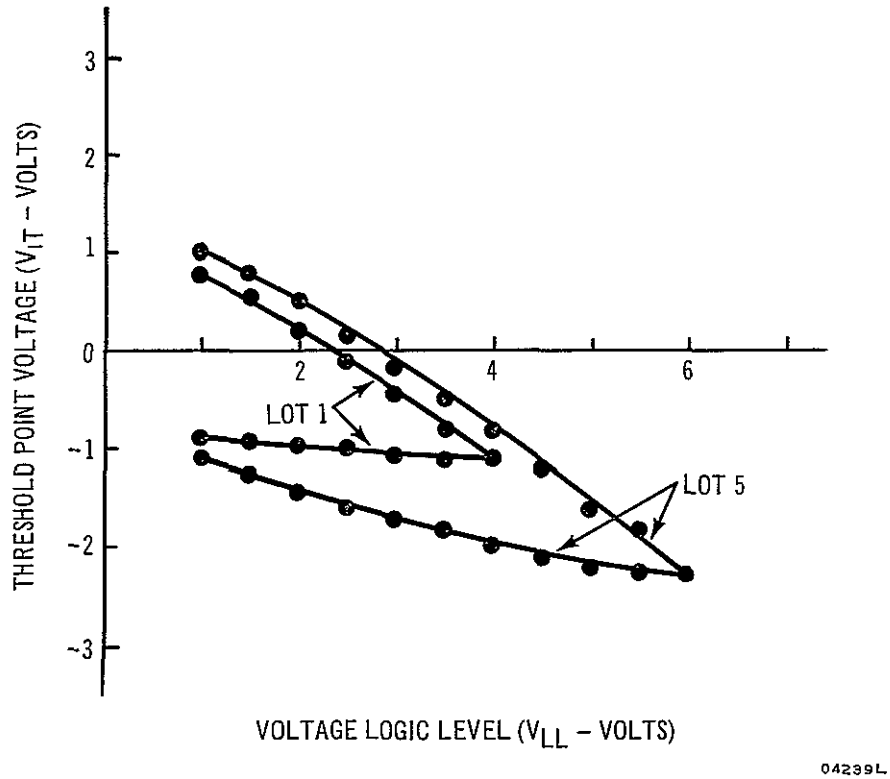


Figure 45 Threshold Point vs Logic Level Curves Measured From the Multiplexer Switches

of 8 volts). The distortion (i.e., the percentage of harmonic content in the output signal compared to the fundamental component) from a lot 5 multiplex unit was measured as a function of load resistance R_L and supply voltage V_{SUP}, as shown in Figure 46. The distortion from the sinusoidal signal generator was measured to be about 0.1 percent, which can be subtracted from the multiplexer switch distortion measured at larger values of load resistances.

The amount of input signal that feeds through to the output when the multiplexer switch is turned off was measured as a function of frequency and load resistance for a given supply voltage. From the results, shown subsequently, the circuit component that gives rise to this feedthrough is capacitive in nature. Figure 47 shows a lumped parameter model of the multiplexer unit with associated load where C_S is the capacitor of the multiplexer switch (including package and test jig feedthrough capacitors), R_L is the load resistor, C_L is the load capacitor (including multiplexer output capacitor, and package and test jig output capacitors). The multiplexer was connected such that the common bus to all multiplexer switches was used as the input terminal and the individual switch lead of a switch was used as the output terminal. The circuit equation of the model is obtained from the circuit and is given by Eqs (23), (24), and (25).

$$\frac{V_o}{V_1} = \frac{f/f_2}{\sqrt{1 + (f/f_1)^2}} \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (23)$$

where

$$f_1 = 1/2\pi\,(C_L + C_S)\,R_L \quad \text{(break frequency)} \quad \ldots\ldots\ldots \quad (24)$$

$$f_2 = 1/2\pi\,C_S\,R_L \quad \text{(zero crossover frequency)} \quad \ldots\ldots\ldots \quad (25)$$

For values of frequency f smaller than and greater than the break frequency f_1, Eq (23) reduces to Eqs. (26) and (27) respectively.

$$\left.\frac{V_o}{V_1}\right]_{f<f_1} = \frac{f}{f_2} = (2\pi\,C_S\,R_L)f \quad \text{(linear)} \quad \ldots\ldots\ldots \quad (26)$$

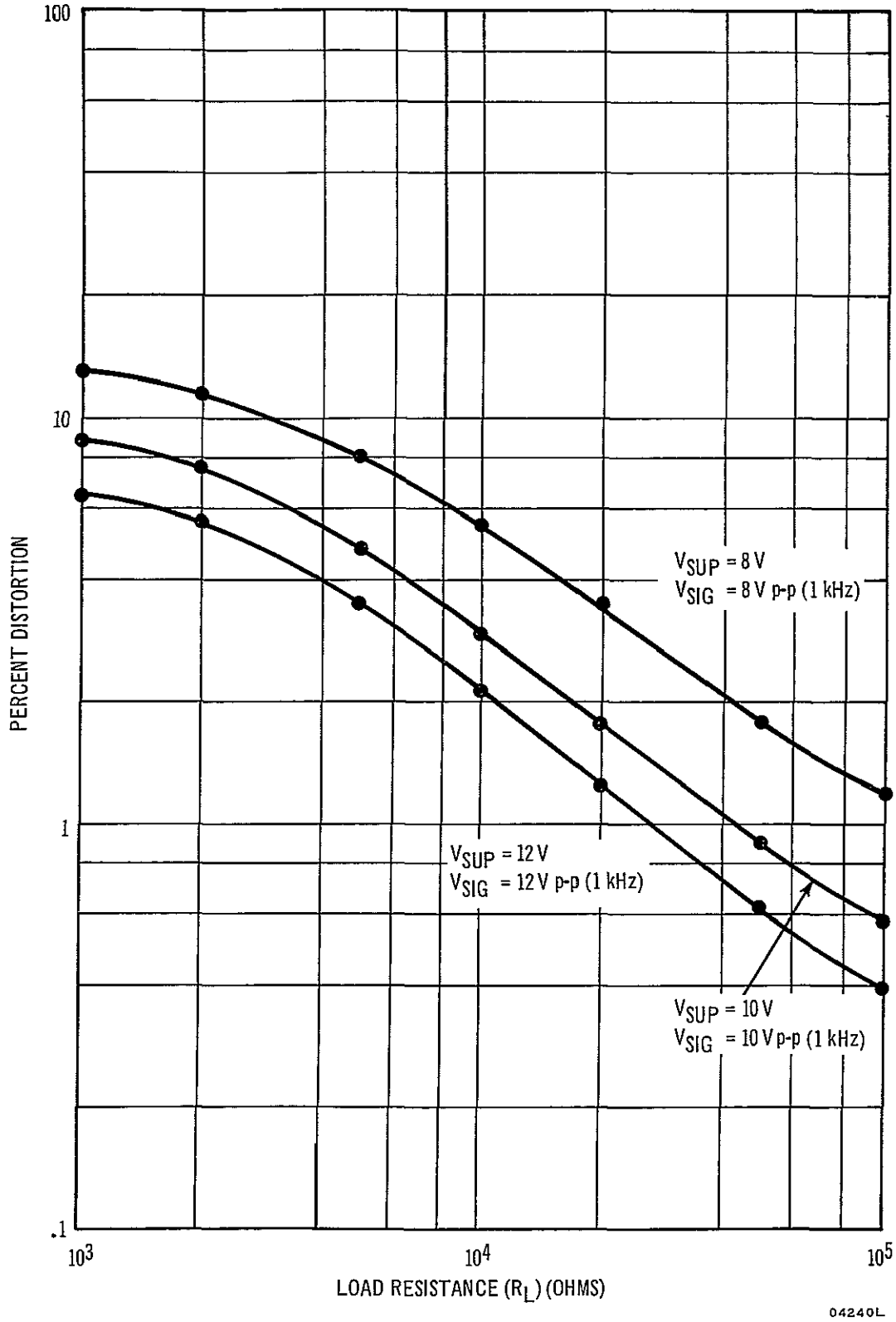


Figure 46 Percent Harmonic Distortion vs Load Resistance and Supply Voltage

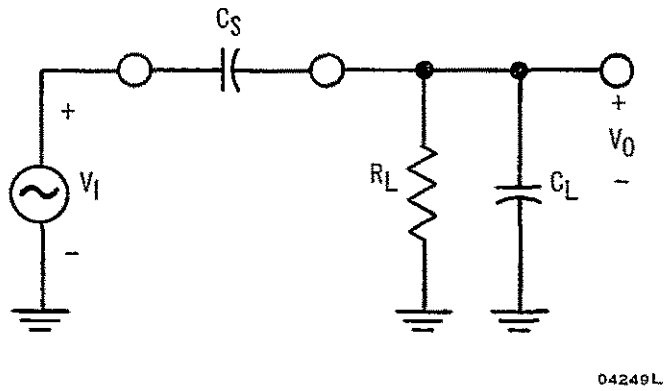


Figure 47 Lumped-Parameter Model of Multiplexer Unit (Switch Open) and Associated Load

$$\left.\frac{V_o}{V_1}\right]_{f>f_1} = \frac{f_1}{f_2} = \frac{C_S}{C_L + C_S} \text{ (constant)} \quad \ldots\ldots\ldots\ldots \quad (27)$$

By taking the $\log_{10}$ of Eq. (23), resulting in Eq. (28), the frequency response of the model is illustrated by an asymptotic plot, shown in Figure 48.

$$\log_{10}\left(\frac{V_o}{V_1}\right) = \log_{10}\left(\frac{f}{f_2}\right) - \frac{1}{2}\log_{10}\left(1 + \left(\frac{f}{f_1}\right)^2\right) \quad \ldots\ldots \quad (28)$$

The first term of Eq. (28) is asymptotically drawn in Figure 48 as curve 2 (dashed line), the second term of Eq. (28) is asymptotically drawn as curve 1 (dashed line), and the composite (algebraic sum) is drawn as curve 3 (solid line) Curve 3 is linear below the break frequency f_1 (increasing at one voltage-ratio decade per frequency decade) showing that the resistive component of the load dominates, and it becomes constant above f_1 showing that the capacitance component of the load dominates Figure 49 shows curves obtained from results measured from a typical multiplexer unit (solid lines) and associated asymptotes (dashed lines) for different load resistors and load capacitors, for a supply voltage of 10 volts DC, and a signal voltage of 10 volts peak to peak The value of the capacitor C_S may be calculated by using the break frequency f_1, feedthrough $(V_o/V_1)_{f>f_1}$, and the known load resistance for a particular curve, and by using Eqs. (24) and (27). An alternate method uses the zero crossover frequency f_2 and the known load resistance for a particular curve by using Eq (25). Using either method the value of C_S is calculated to be about 1.74 picofarads. The capacitor C_S contains the jig capacitance as well as the package and actual multiplexer switch capacitance Figure 50 shows a feedthrough vs. frequency plot of the jig. Using the above systems and the information from the curves the jig apparatus C_J is obtained in a similar manner and is calculated to be 0 14 picofarad. Subtracting C_J from C_S, the feedthrough capacitance of the multiplexer switch and associated package is 1 6 picofarad. It must be noted that feedthrough varied from switch to switch but did not exceed in value from the feedthrough measured and plotted.

The feedthrough calculated above is associated with the signal and can be termed "signal feedthrough", but another form of feedthrough also exists which

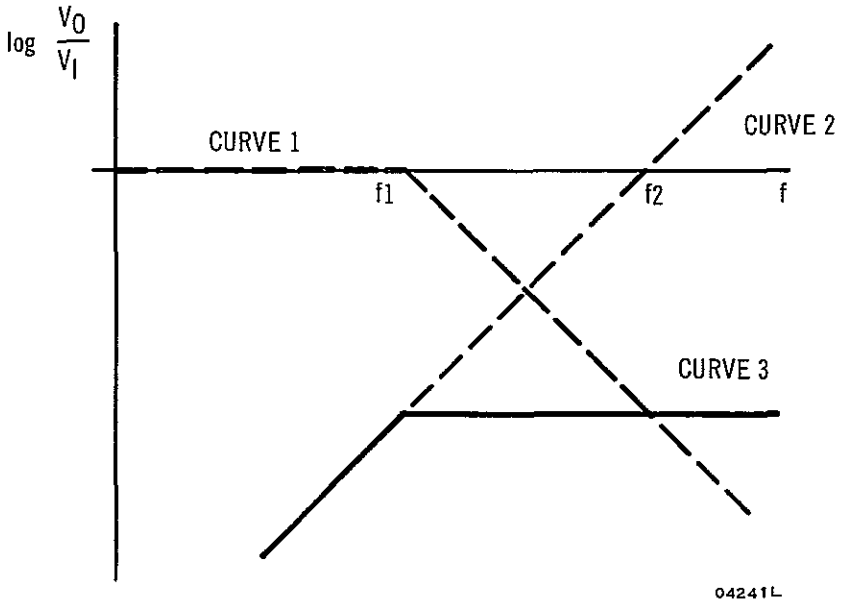


Figure 48. Frequency Response of Model of Multiplexer Unit

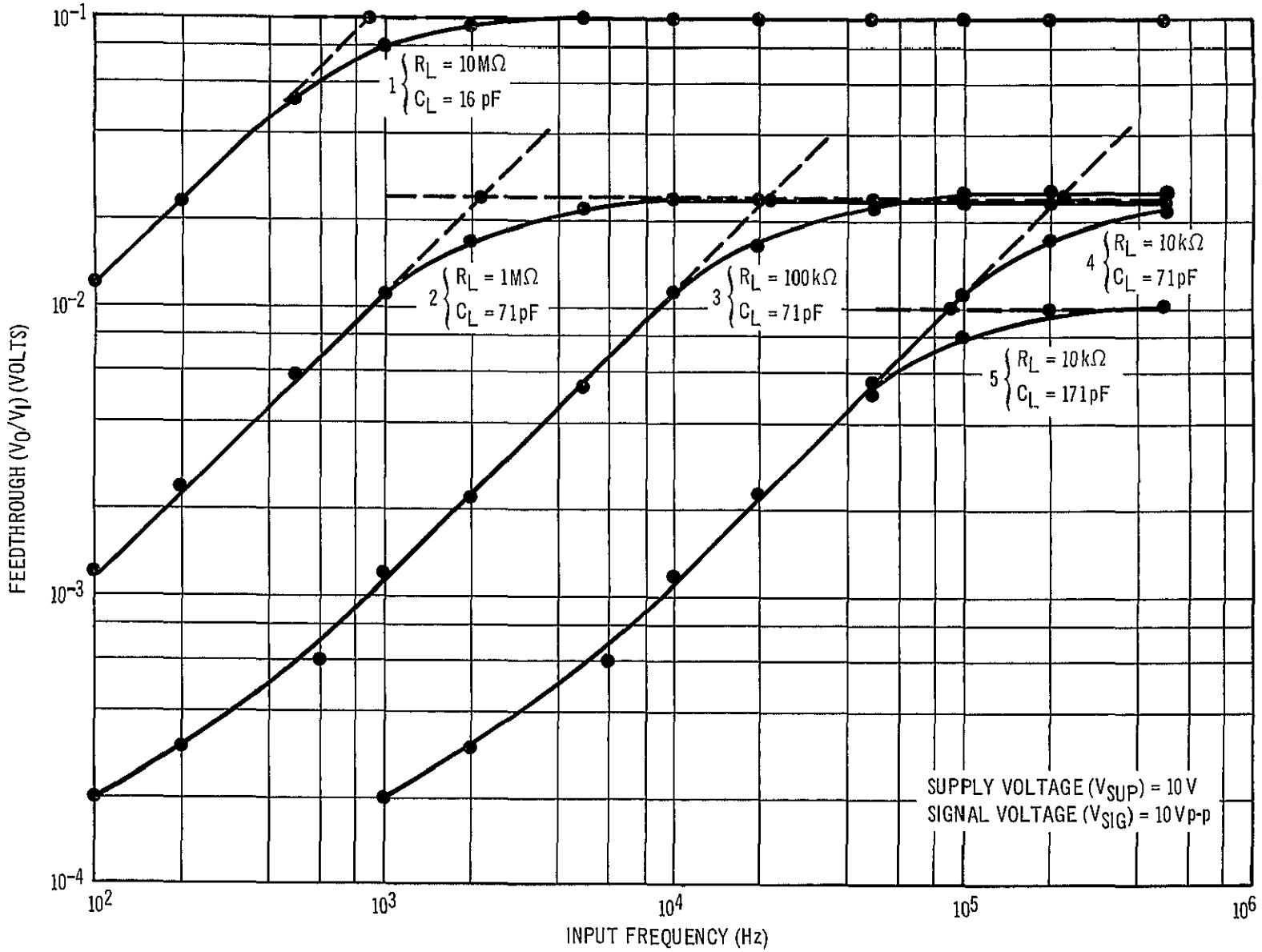


Figure 49 Feedthrough (Output Voltage / Input Voltage) vs. Frequency for a Multiplexer Switch

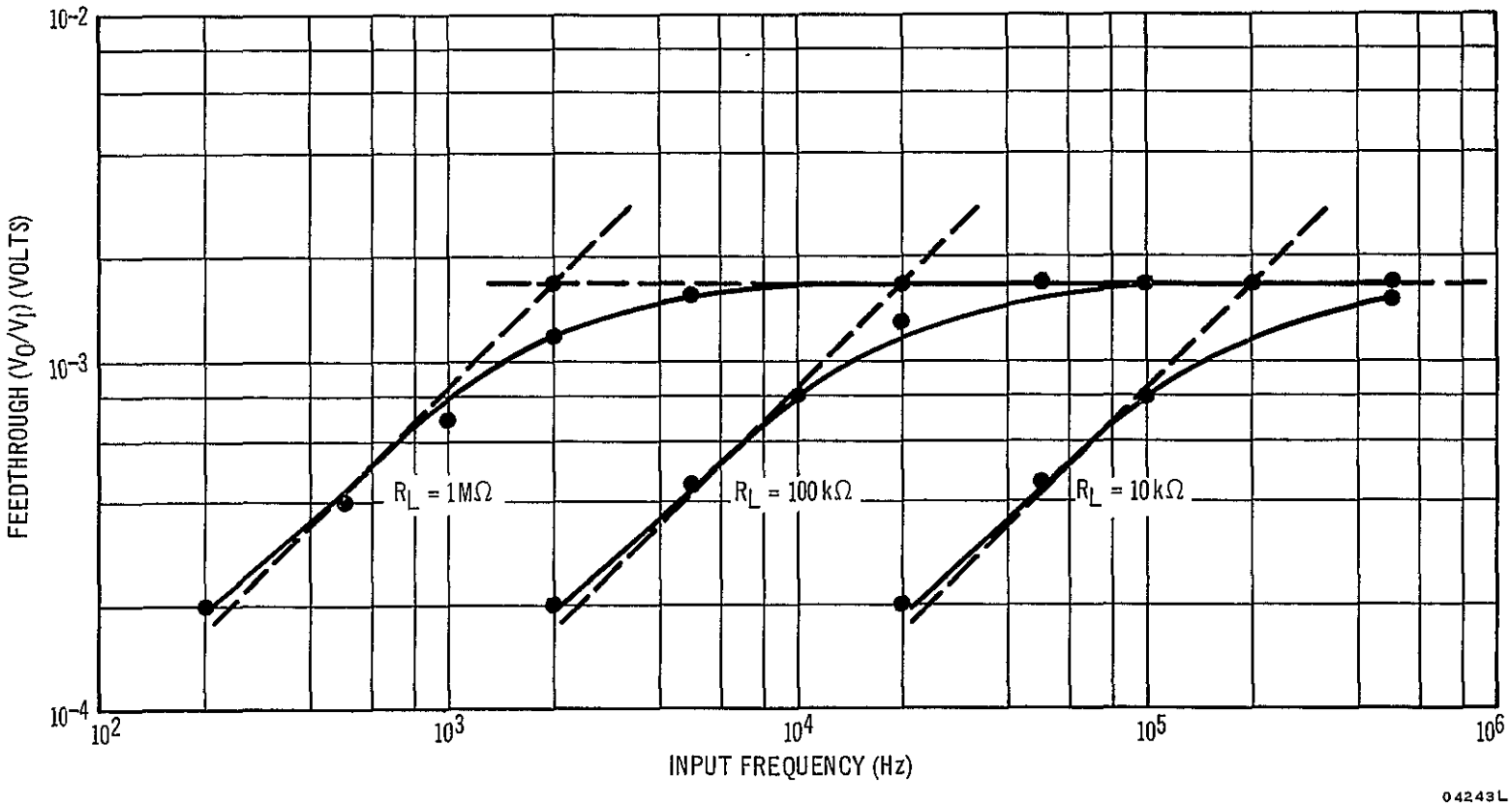


Figure 50 Feedthrough (Output Voltage / Input Voltage) vs. Frequency of the Multiplexer Jig

can be termed 'logic feedthrough". Signal feedthrough was measured with no clock signal applied to the multiplexer (i e., used in random access mode) and was shown to depend upon the drain-source switch and package capacitors of the multiplexer unit Logic feedthrough, on the other hand, was measured with a clock signal applied to the clock input of the multiplexer unit (i.e., used in sequential access mode), and depends upon the gate-to-diffusion (drain or source) capacitor on the output (load) terminal of the multiplexer unit. Since the switches on the multiplexer unit are complementary and have complementary logic signals, the switches were designed so that the gate metalization overlapping both the n- and p-channel diffusions (source and drains) were made equal in area (providing equal logic feedthrough capacitors) so that the logic feedthrough from each device would cancel. Figure 51 is a photograph showing the clock and enable inputs and logic feedthrough of a typical multiplexer switch (number 0) with the three decoders disabled (i.e., the blanking input is at 1 so that no logic signal reaches the switch). The feedthroughs in this case are only due to feedthroughs of the clock and enable pulses since the feedthrough pulses align with the edges of those signals. Figure 52 is a similar photograph except that the blanking input is set to 0 thus adding the tree decoder. In this case the influence of the logic to the switch is clearly seen in terms of the spikes; but no pulse-like feedthrough, that would occur in single-channel devices, is seen to occur. The measurement was made with a supply voltage of 10 volts, a load resistance and capacitance of almost 10 kilohms and 71 picofarads, respectively, and the input terminal shorted to ground. It must be noted that low signal feedthrough is sacrificed at the expense of having low signal feedthrough, and vice versa, since the finite overlapping of the gate metalization diffusion is needed for logic feedthrough cancelation and provides a larger source-drain capacitor which increases the signal feedthrough.

Figure 53 shows a picture of normal output pulses (on outputs 0, 2, 4, 6, . ., and 14) produced with a constant input voltage, and what appears to be logic feedthrough (small spikes). The spikes follow the amplitude of the input signal (constant in this case) so that the spikes can only be attributed to a momentary turn-on of the switches. The cause is the small discrepancies in the rise and fall times of the coded signal coming from the four-stage

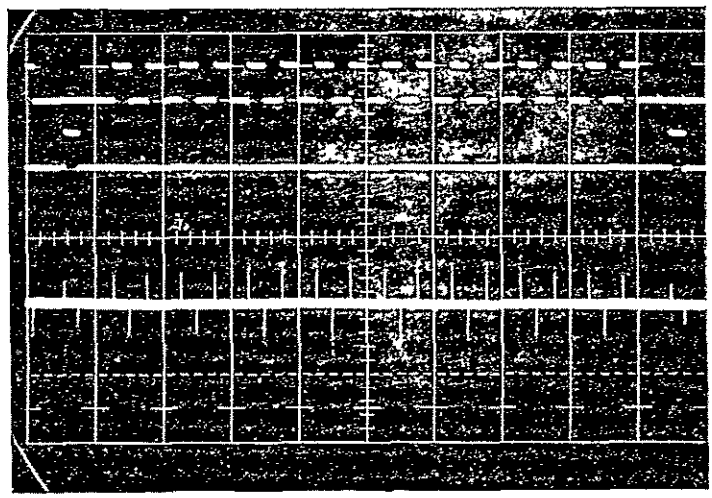


Figure 51. Logic Feedthrough (Blanking Input at 1)

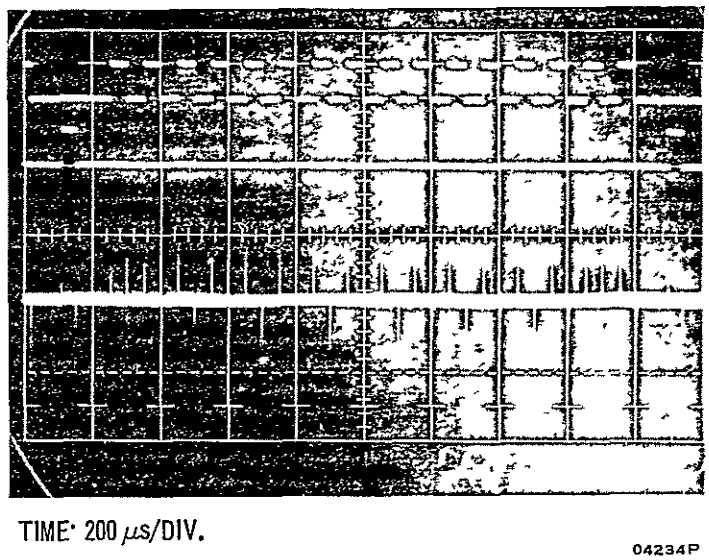


Figure 52. Logic Feedthrough (Blanking Input at 0)

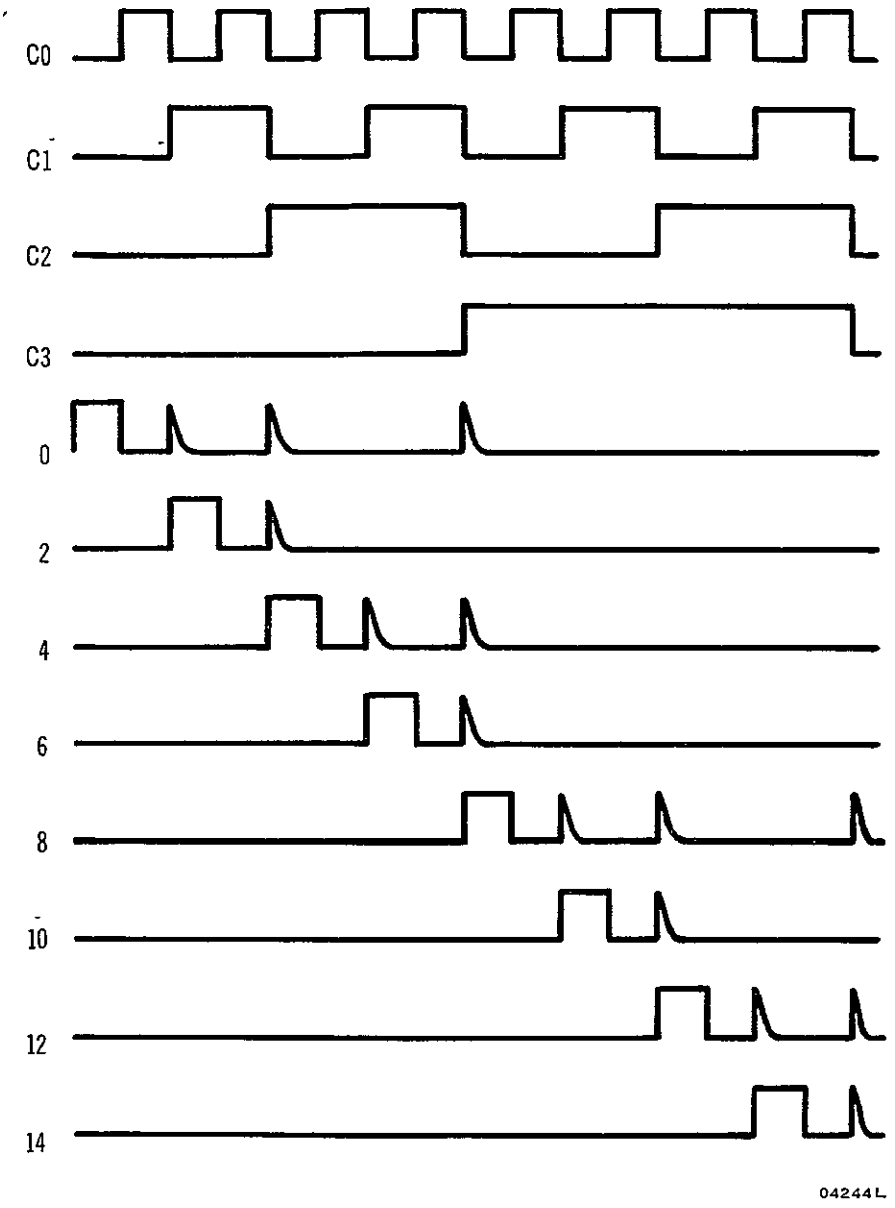


Figure 53. Switch Turn-on Spikes

counter into the decoder tree. The small discrepancies provide a delay that gives an erronious code of short duration and turns on the switch for which that code is designated. The differences in rise and fall time can be attributed to the sizes of the devices used in the counter (they were designed 1 to 1 rather than 1 to 2 for n- and p-channel devices, respectively, to conserve space). The 1 to 2 size difference is preferred since it accounts for the 2 to 1 surface mobility differences (assuming equal threshold devices). It is to be noted that only the even number outputs had this spiking problem and that no spiking was observed for the odd numbered switches The duration and amplitude of the spikes can be reduced (even to the point of being eliminated) if large supply voltages are used. It was observed that some units did not have spiking. A method of eliminating the turn-on spikes is to tie the reference input to ground and apply a blanking pulse (logical "1") during the transition (edge) periods.

D. VALIDATION OF TEST STANDARDS

The multiplexers described in this report were used as a vehicle to test the validity of the proposed NASA test standard (NASA-STD-XX-3) that was designed for process control and testing of monolithic circuits. This standard is a compilation of test methods selected from various programs for NASA's Microelectronics Line Certification program. From this standard, the 6000-series test methods were applied to the multiplexer. Ninety-three tests from this series were checked out and are included in the outline of the test that is included in the following pages.

In general, the recommended procedures were entirely satisfactory, and in a few instances contribute significantly to techniques of in-process control. In these cases, the tests were rated good or excellent.

In the test outline that follows, suggestions are included that could improve the effectiveness of some of the tests. These suggestions arise from practical experience in processing the multiplexers. Occasionally, the tests were found to be unclear and liable to misinterpretation.

VALIDATION OF TEST STANDARDS FOR MICROCIRCUITS
MICROELECTRONICS SUBCOMMITTEE
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

VALIDATION REPORT

6000 Measurement of Water Purity

6000.1 Good. The standard should mention that in spite of precautions, bacteria grow in the water distribution system. These do not show as ionizable impurities; hence are not detected by resistivity measurement.

6001A Measurement of Resistivity of Deionized Water

Good.

6001B Water Resistivity

Good.

6002A Determination of Total Solids in High Purity Water

2.0 100 mℓ silica dishes are too small for the 100 mil sample required.

3.0 Procedure: The dish must be kept covered with a quartz clock glass during evaporation to avoid dust pick-up.

General Comment: The sensitivity of this method is 2 to 5 ppm. too poor to be applicable to "high purity water".

6002B Water Solids

Particle Count: Method is good, but some guide as to interpretation is required. Suggest dark field may help identification.

6003 Determination of Organic Impurity

Good.

6004 Water Bacteria Count

Good.

6010 Lifetime Measurement

6010.1 Lifetime measurement is critically affected by the metallurgical history of the silicon wafer or crystal. In addition, the oxygen content also plays a part in the actual value of lifetime measured. A warning is in order, that this method is best applied to crystals obtained by similar methods of preparation and thermal history.

6011A Resistivity - Monolithic Microcircuits

5.2 Sheet Resistivity: This is unclear.

5.3 The measurement should be carried out with the specimen fully shielded from light. The polarity should be reversed after each measurement, as described in 6011B, 41.6.

The upper limits for applied current must be specified. Too high a current causes heating and invalidates the measurement.

It is good practice to clean the sample in hydrofluoric acid just before measurement.

6011B Substrate Bulk Resistivity

Same comment as given for 6011A 5.3 above.

6012 Orientation of Substrate with Reference to Crystal Plane

Good.

6012B Substrate Orientation

Good.

6013A Dimensional Evaluation

.4 It is often desirable to reject the wafers used as samples, (especially if the orientation was (100)), because even relatively light pressure causes surface damage. A differential etch should be used periodically on the inspected wafer to determine whether the measuring instrument causes damage.

6013B Substrate Thickness

Good, except for caution as in A.

6013C Substrate Parallelism

Good, except for caution as in A.

6013D Substrate Flatness

This method does not distinguish between distortion and edge rounding or pillowing. The latter may be acceptable.

b6013E Substrate Width

Good.

6014 Oxygen Content of Silicon Substrates

A caution about heat treatment is necessary oxygen compounds precipitate during heat treatment and the absorptivity of the 9-μm band changes even though the total oxygen content remains unchanged.

6015A Dislocation Density, Lineage and Slip & 6015B Substrate Crystal Perfection

Neither method is applicable to (100) oriented substrates. Etch patterns observable on other low index planes are difficult to interpret.

6016 Inclusions

Good.

6017A Conductivity Type

.4 The sample should be etched in hydrofluoric acid just before use. This is especially important when high resistivity and polished samples are to be tested.

6018A Surface Roughness

Attention should be drawn to the method of interpreting step height from the recorded tracing. A base line (average) is drawn and peak height determined as the vertical component not normal to a sloping base line.

6018B Substrate Surface Finish

It is useful to view this reflection of a fine-line pattern.

6020A Viscosity

Good.

6020B Photoresist Viscosity (ASTM)

Good.

6020C Photoresist Viscosity (Torque)

Good.

6021A Determination of Solids in Photoresist Materials

Good.

6021B Photoresist Solids Residue

Sample should be prepared as 6021A 3.2.1.

6022 Photoresist Surface Tension

.4 Preparation of sample as in 6021A 3.2.1. Temperature must be specified.

6030A Thickness of Epitaxial Layer

.2 Reference to "Method #22" is obscure.

.4 It should be indicated that the stated limits apply to epitaxial layer thickness ranges of >5 μm. Also the method is only applicable to samples with homogenous deposits, i.e., no "pockets" and where the doping difference between substrate and layer is greater than about 1.5 orders of magnitude; also, note that only carrier density, not type, matters.

6030B Thickness of Epitaxial Layer (Stacking Fault)

Good.

6030C Thickness of Epitaxial Layer (IR) EIR

Some cross reference to 6030A should be made to establish their relationship.

6030D Thickness of Epitaxial Layer (Normarsky)

Good.

6031 Resistivity of Epitaxial Layer (Four-Point Probe)

.4 If the wafers have been stored, a dip in hydrofluoric acid is desirable. The point of measuring the probe spacing (set at 0.040" in 6031.21) is obscure as virtually all epitaxial layers are considerably thinner It is more important to check that the points are in line Also, the check wafer must be rejected because of damage by the test.

6032 Epitaxial Defects

Excellent.

6033A Susceptor Temperature Monitoring

Reference to "Methods #11 & 12" are obscure. A note on the emissivity correction and a warning about absorption losses due to films on the reactor wall is desirable.

6033B Epitaxial Process (Substrate Temperature)

Same as in 6033A above.

6040A Oxide Thickness & 6040B Thickness of Passivating Layer

Why is there no mention of the ultra violet reflection method?

6040C Thickness of Passivating Layer (Polychromatic)

This is true only for SiO_2 of known refractive index. Does not apply to undensified deposited oxides, doped oxides, glasses Si_3N_4, etc. The accuracy given is very optimistic in the region 3000° to 4500°.

6041A Oxide Stability & 6041B Stability of Passivating Layer (C-V Curves)

Some standardization is required on the applied voltage stress in terms of field, i.e., it may be 10^6 volt/cm. The methods given here allow a variation of at least a factor of 2

Also, note that the flatband voltage is different for different crystal orientations. No allowance of the metal work function effect is made.

6050A Measurement of Line Width

Good.

6050B Photoresist Process (Minimum Line Width)

Good.

6051A Photoresist Film Thickness

Good.

6051B Photoresist Process (Thickness of Film)

A note describing how to obtain the refractive index of various photoresists and how it varies with processing, age, and temperature is needed (ellipsometry, U.V.reflectance).

6052A Oxide and Photoresist Pinhole Determination

Some standardization of a metal thickness, e.g.,not less than 3000Å is desirable because very thin metal over a defect can burn out locally and rapidly, and may not give rise to a short.

6052B Photoresist Process (Pinholes in Film)

It is very doubtful whether this method is capable of finding any but the most gross defect, the ± 10% accuracy is too optimistic.

6053A Photoresist Process (Light Intensity)

Good. Reference to "Method 18" is obscure.

6053B Photoresist Exposure Control

Good.

6060A Junction Depth

.3 The junction stain is given as HF. This is not usual, it should be $HF-HNO_3$ or $HF-HNO_3$-HOAC as in 6060B.4.1.10 at seq.

6060B Junction Formation (Depth)

Good.

6061A Impurity Concentration Profile

Good.

6061B Junction Formation (Sheet Resistance)

Good.

6062A Diffusion Furnace Profiling

Good.

6062B Junction Formation (Temperature Profile)

Good.

6062C Junction Formation (Gas Profile)

Good.

6065A Measurement of Isolation

Good.

6065B Diode Isolation (Breakdown Voltage)

The stated "purpose" is an inadequate description of the test objective.

4.5 This should state what to do when the voltage does or does not change.

6065C Dielectric Isolation (Breakdown Voltage)

Good.

6066 Isolation Leakage

4.1 Some standardized surface treatment after the 4.1 etching step would be useful if low leakage currents, e.g., 10^{-12} to 10^{-9} amperes, are to be read. Also, the test set atmosphere should be controlled, for example, dry N_2.

6070A Metalization Thickness

Good.

6070B Metalization Thickness (Tolansky)

Good.

6070C Metalization Thickness (Sheet Resistance)

This method rests on the assumption that evaporated metal has the same density and conductivity as bulk aluminum. It is doubtful that $\pm$ 10% accuracy can be achieved.

6071A Metalization Adherence

2.0 A. As the adhesive force apparatus of tape varies with the adhesive, which in turn varies with the nature of the tape, some standardization on type number is desirable.

B. The adhesive properties of tape are also influenced by storage time, temperature, and ambient humidity. Again, the parameters can be defined. It may help to order the tape to be delivered in airtight containers. After opening, they should be resealed--possibly "tropical packs" can be obtained.

6071B

Good, but see 6071A (B)

6072A Metalization Stability

I Good. Scale indication in fig 1 and 2 of the NASA report would be useful.

II Excellent

6072B Stability of Metalization

It is not clear whether this test is carried out on sealed or just mounted units. The ambient RH should be defined.

6073 Specific Reactivity of Metalization

Good.

6074A,B Quality of Ohmic Contract

Good.

6075A Cross Section Uniformity of Metalization

Not sufficiently detailed.

6075B Cross Sectional Uniformity of Metalization

Good.

6080 Pneumatic Impact Test

Good

6081 Push Test

Supply details.

6091 Measurement of Bond Conductivity

Good. Probe positioning may be difficult. The chip should be rejected after the test.

6100A Moisture Content of Enclosed Gases

Good. Title is not accurate.
Moisture content of sealing atmosphere would seem more to the point.

6100B Moisture Content (Dry Box Sealing)

Good.

6100C Moisture Content (Belt Furnace Sealing)

Good.

6101A,B,C Leak Detection

Good.

6102A Evaluation of Defect in Glass Package

3.1 Magnification of 30X is preferred (see 6102 B)

6102B Sealing Defects in Glass

Good.

6102C Sealing--Defect in Glass (Flat Package)

2.1 Magnification of 30X is preferred.

6500 Electrical Parameter Measurement of Bipolar Transistors in Monolithic Integrated Circuit Technology

Good

6501 Stored Charge, Bipolar Transistor (Q_{BX})

Good.

6600 Metal-Dielectric-Semiconductor Field Effect Transistors (MOSFET)

Good. In all test setups battery polarity will depend on whether transistor is n or p channel.

6601 Breakdown Voltage (BV_{DSS})

Unclear. Substrate should be tied to source. Note I not shown. Bipolar and MOSFET terminology mixed.

6602 Breakdown Voltage, Source to Gate (BV_{GSS})

Unclear. Substrate should be tied to source.

6603 Drain-to-Source Cutoff Current I_{DSS})

Unclear. Bipolar terminology mixed with MOSFET terminology. Substrate should not be floating. Only condition C seems to yield a measurement of I_{DSS}.

6604 Source-to-Gate Cutoff Current (I_{GSS})

Unclear. Bipolar terminology mixed with MOSFET terminology.

6605 Gate-to-Source Threshold Voltage (V_{GST})

This measurement should be made at constant current density in order to be compatible amoung units of different dimensions, or better yet, threshold should be measured at I_o=0.0 amperes. Substrate should be tied to the source.

6606 Gate Leakage Resistance (R_{GS})

This measurement is very difficult and requires special probe setups if it is to be made at all.

6607 Dynamic Drain-to-Source Resistance (Rd on)

Substrate must be tied to the source; otherwise good.

6608 Static transconductance (gm)

Substrate must not be floating, otherwise good.

6609 Direct Inter-terminal Capacitance (G_{GS}, C_{GD}, C_{DS})

3. Definitions are incorrect.

SECTION III
CONCLUSIONS

A sixteen-output multiplexer with the requisite counter and decoder circuits was constructed using the COS/MOS processing technique. The processes used were standard except that stoppers were not employed. The only problems encountered during the term of the project resulted from errors in the preparation of the complex multiplexer masks. These errors were painstakingly found and corrected, and circuit fabrication became a smooth operation.

During circuit manufacture the monolithic test standards outlined in NASA-STD-XX-3 were tested and, on the whole, found to be thoroughly satisfactory, although a few of the tests required refinement or change. The adoption is recommended of the 6000 series of the test standards, including the changed outlined.

SECTION IV
NEW TECHNOLOGY

Listed below is the new technology that was developed during the course of the program. A reference is provided to the pages in this report on which a description of each item of new technology appears.

a. Manufacture of a 16-output COS/MOS multiplexer (see page 3).

b. Design and fabrication of the counter circuit (see pages 14 and 16).

c. Design and fabrication of COS/MOS decoder tree (see pages 20 and 21).

d. Method of calculating material characteristics of well from COS/MOS transfer characteristics (see pages 36 through 40, and 42 through 44).

e. Validation of monolithic test standards (see pages 73 through 82).