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for

THE DEVELOPMENT OF QUALITY STANDARDS FOR BIPOLAR LSI

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ABSTRACT

Work performed under this contract is summarized in two volumes. Volume One reports on the work performed during the period of the contract and Volume Two contains recommended guidelines for reliability engineers or prospective LSI users, which can be used to formulate meaningful Quality Assurance specifications for procurement of LSI devices.

Various test programs were initiated to identify failure mechanisms and this resulted in finalization of the package design and multilevel metallization techniques.

In conclusion, areas of further work in the development of quality standards and inspection criteria for Bi-polar LSI devices are also suggested.

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SECTION I

INTRODUCTION

This report is volume one of two volumes of the final report on NASA contract No. NAS8-21319, prepared for the George C. Marshall Space Flight Center, Huntsville, Alabama. Volume one covers the work performed during the calendar period from 15 April 1968 to 15 April 1969.

Three quarterly reports were written in compliance with this contract. The first quarterly report, TI Report No. 03-68-55, the second quarterly report, TI Report No. 03-68-88 and the third quarterly report, TI Report No. 03-69-19 were completed in July 1968, October 1968 and January 1969 respectively. During the above period, 8 monthly reports were also submitted.

The objectives of this program were:

1) To identify and interpret the cause of failure in large scale integrated circuits (LSI) with particular emphasis on discretionary routed array (DRA) technology.

2) To develop standards and controls to prevent the occurrence of failures in devices to be used in high reliability applications.

As mentioned above, this final report is contained in two volumes. Volume Two contains recommended guidelines for reliability engineers or prospective LSI users, which can be used to formulate meaningful quality assurance specifications for procurement of LSI devices.

Although various technological approaches which can be used to produce LSI devices are described, it should be emphasized that essentially all the work performed in conjunction with this contract was based on TI's DRA technology. For this reason the reader should be alert to differentiate between those comments applicable to LSI generally, and those specifically oriented to DRA technology only.

Major contributors to this program have been: Mssrs. Carl J. Benning, Boyd Plott, Bryan E. Zimmerman, S. Radhakrishnan, and W. E. Spencer, under the guidance of Mr. Dave C. Mueller, the Program Manager.

SECTION II

TECHNICAL DISCUSSION

A. LSI CONCEPT

The technological base of the electronics industry has undergone dramatic change in the past 20 years, largely related to the expansion of the use of materials technology. With the invention of the transistor in 1948, semiconductor materials processing provided the technology for an entirely new class of electronic devices. The invention of the monolithic integrated circuit in 1958, extended the use of materials technology to the formation of complete circuit functions on chips of semiconductor. The semiconductor industry is now entering another phase of the expansion of materials technology, in which complete equipment subsystems are processed on slices or large chips of silicon which are then packaged as a single device.

This phase has been given several names, some of which are "large scale integration" (LSI), "computer on a slice" and "array technology". The term "large scale integration" is the most descriptive. The concept of LSI is actually nothing new; it is a natural and logical extension of the monolithic integrated circuit.

In the past, criteria such as the number of gates, size of the chip, and/or components per slice centimeter have been used to classify LSI devices. Consequently, LSI has been defined by some as "a monolithic IC that contains the equivalent of 100 or more gates". However, in a more general way, large scale integration may be defined as: the incorporation of a large number of active and/or passive components on a single silicon chip or wafer connected in such a way as to function as an electronic system or subsystem. Two active device structures that are in use for LSI applications are the bipolar transistor and the MOS transistor. Various LSI approaches based on bipolar technology are described in the following section.

B. BIPOLAR TECHNOLOGY

The preparation of a typical bipolar device starts out with a slice of P-type (or N-type) silicon which is polished and used as the original substrate. An N-type layer is epitaxially grown on the substrate. A passivation oxide layer is grown on top of the N layer as shown in Figure 1. Selected areas of the oxide layer are etched away as shown in Figure 2 and the slice is subjected to a P-type diffusion process. This step results in the formation of N-type islands in the epitaxial layer which are isolated by the diffused P-type regions.

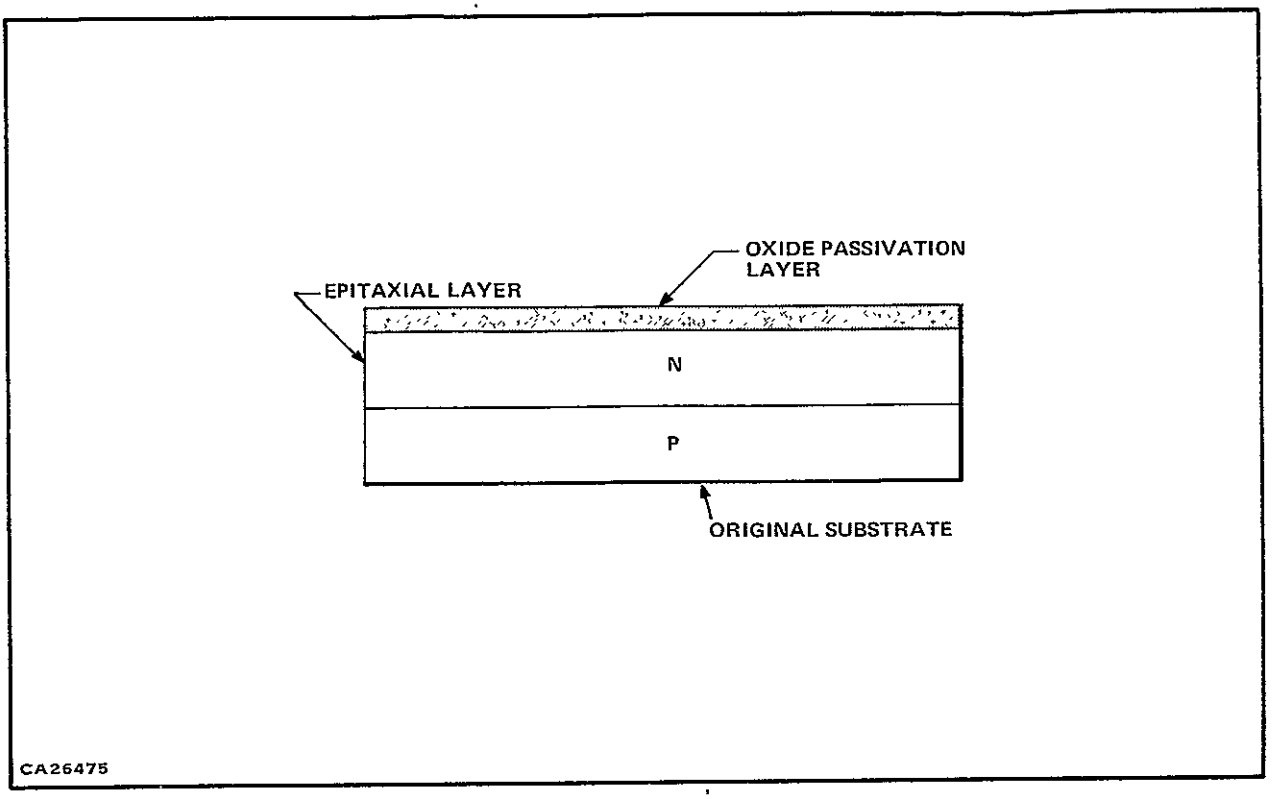


Figure 1. Planar Epitaxial IC Before the First Diffusion Step

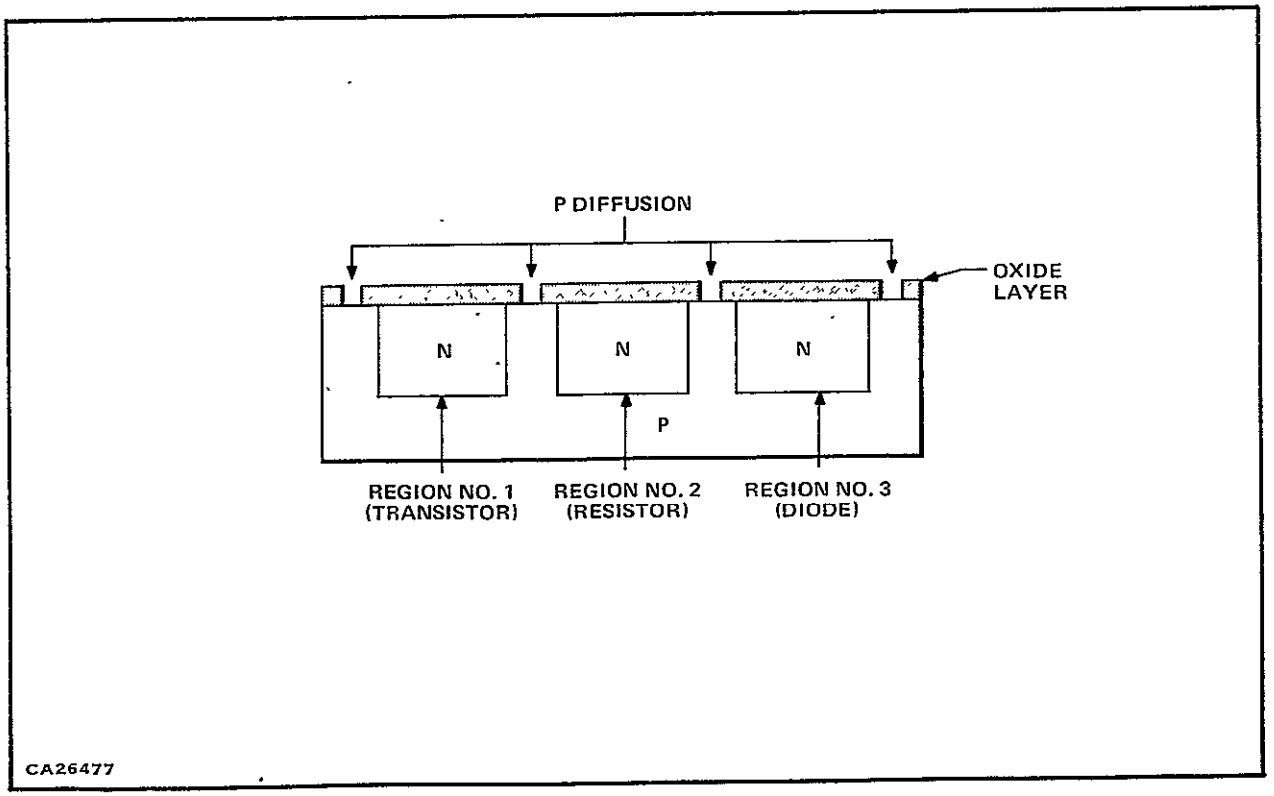


Figure 2. First Diffusion for Isolation

During the first P-type diffusion that created isolated N-type regions the wafer is reoxidized; subsequently, it is coated with a layer of photoresist. A mask containing the transistor base and the resistor patterns is positioned on the wafer. A second process of exposure, development, and etching takes place in a similar manner as the first step, although different areas of the silicon surface are now exposed. A second P-type diffusion results in the wafer profile as shown in Figure 3.

Subsequently, after the second diffusion, another photoresist, expose, etch cycle results in a third pattern for emitter diffusion over the wafer, and the wafer is subjected to an N-type diffusion. Figure 4 shows the wafer profile at the end of the third diffusion step.

On completion of the third diffusion step, selected spots are etched away on the reoxidized wafer for making metal contacts to the various circuit elements which have been diffused into the silicon substrate. After the conducting material has been deposited, another mask, which contains the circuit conductor pattern, is positioned over the wafer, and the photoresist expose, etch cycle is again repeated. Each slice now contains an array of circuits or cells which can now be interconnected to perform complex logic functions.

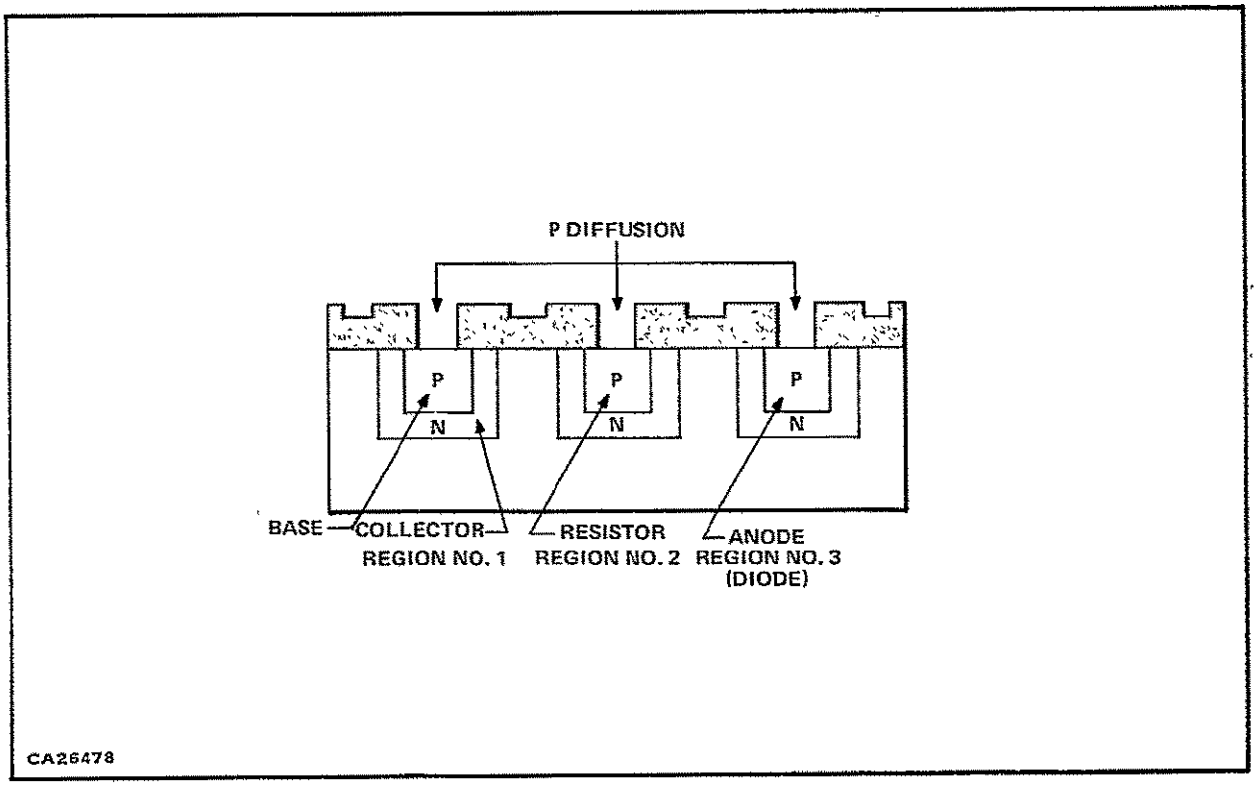


Figure 3. Second Diffusion for Transistor Base and Resistor

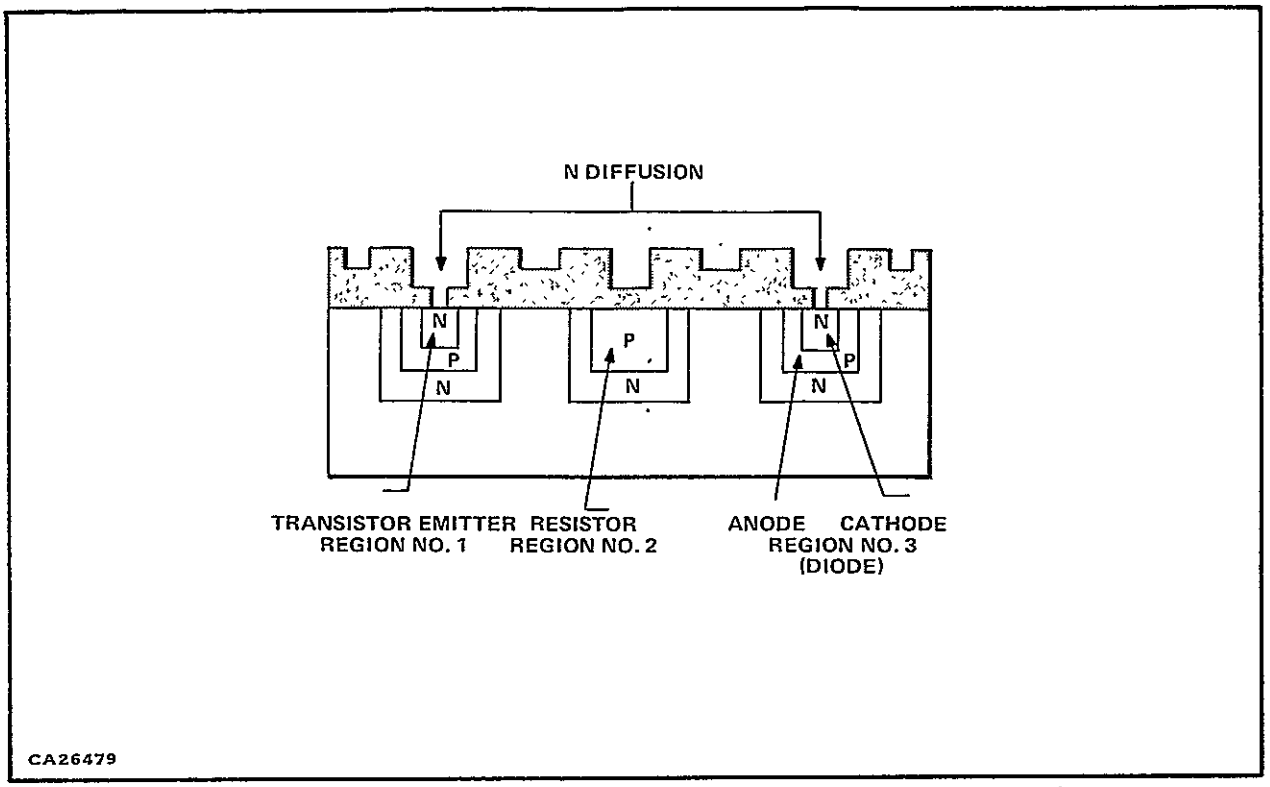


Figure 4. Third Diffusion for Transistor Emitter

As the complexity of IC interconnections is increased, one limitation is the routing of interconnections. This routing statistically becomes increasingly more difficult without numerous crossovers. To reduce the number of crossovers, inter-element spacing can be increased, but this results in larger chips with lower yield. To overcome this difficulty, techniques for using multiple levels of interconnection have been developed.

C. DISCRETIONARY ROUTING TECHNOLOGY

Current discretionary routing techniques involve repeating TTL building blocks (gates and flip-flops) over the entire silicon slice. Realizing that a minimum amount of imperfections will always show up in every slice, a method called "discretionary wiring" has been developed.

Figure 5 is a simplified block diagram of the principal steps in the fabrication of an LSI unit by the discretionary wiring approach. In this system a first level of metallized pattern interconnects groups of circuit components thereby creating unit cells (as discussed previously). The metallized pattern also includes a number of test pads so that a series of functional tests can be conducted on each cell individually. Also the first-level metallization makes use of all the devices on the chip, whether they are good or bad. The next step consists of functionally testing each cell by means of a conventional IC tester using the multiprobe method. The coordinate information on the location of

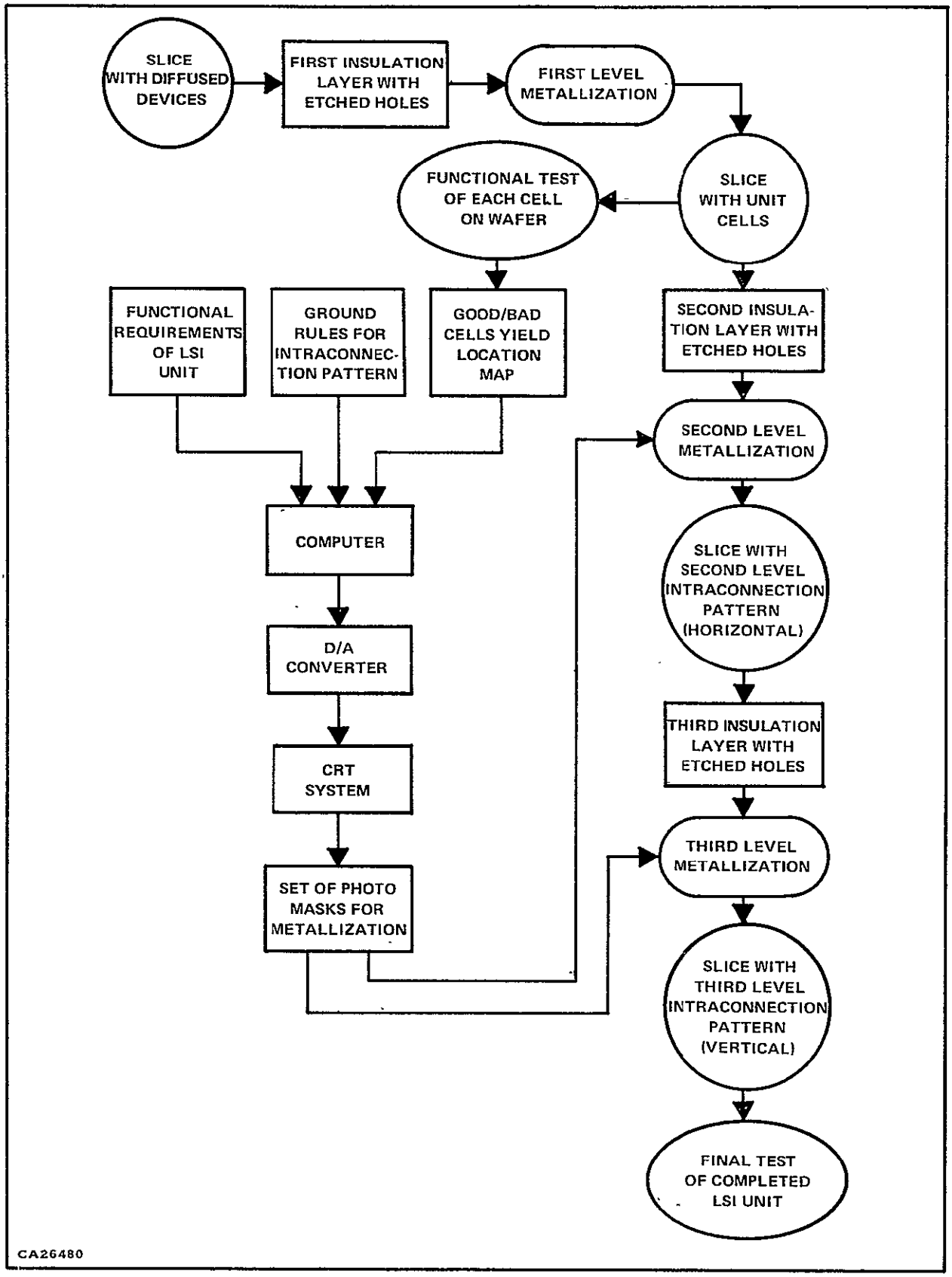


Figure 5. Block Diagram of Principal Steps in Discretionary Wiring

the good and the unacceptable cells is fed into a computer. The functional requirements and the ground rules concerning the intraconnection pattern are also fed into the computer. The computer generates the metallization pattern and feeds it into a high-resolution cathode-ray tube system via a digital-to-analog converter. The pattern generated on the face of the CRT is then projected on a photosensitive material from which a photomask is made. A set of masks is thus prepared for the second and third levels of metallization.

After the first level of metallization, which intraconnects the devices on the chip into cells, is deposited, the slice is covered with a layer of insulation. At appropriate places, holes are etched through to the first-level metallization pattern. A horizontal intraconnection pattern, which was developed by the computer, is now deposited on top of the insulation layer and makes contact with the first-layer metal through the etched holes. Another layer of insulation is now applied on top and holes are etched at appropriate places to the second-level metallization. A third level of vertical metallization pattern, also generated by the computer, is now deposited on top of the insulation and contact is made to the second-level pattern through the holes. This completes the intraconnection on the wafer.

One unique feature of this approach is that no two LSI chips fabricated by discretionary wiring will have the same intraconnection pattern even though the functional output of the two units may be identical. In other words, each LSI unit will have its own unique intraconnection pattern.

Although individual testing of cells as outlined above is a time-consuming and expensive operation, these costs are justified on two counts:

1) Regardless of the method employed for intraconnections, the final testing of an LSI unit is a formidable task. With the DRA approach, the pre-intraconnection testing of individual cells offers added confidence in the LSI unit at final test.

2) The pre-intraconnection testing of the individual cells identifies the parametrically and functionally good cells. Thus, as the array's intraconnections are fabricated, only the good cells will be included in each array, and resultant unit performance is enhanced.

D. FIXED INTRACONNECTION PATTERNS

This system uses a library of standard cells that can be intraconnected in various combinations in order to obtain the desired LSI array. A cell is either a circuit such as a logic gate or a flip-flop of higher functional complexity. A computer complex has direct access to the cell library.

The computer-aided design phase starts with an analysis of the functional requirements. The designer calls for the various cells from the library and these are visually displayed on the CRT console. By using the typewriter and the light pen the designer can rearrange the cell positions until a satisfactory arrangement is obtained.

The next phase starts out when the computer specifies the data needed for the processing of the basic slice. It also generates the interconnection pattern. Because of the greater accuracy provided and elimination of test cells, arrays of significantly smaller geometries are obtained. Generally, only one layer of metallization is required to connect the various devices within each cell to give the basic logic circuits, and also to interconnect the cells to satisfy the functional requirements of the LSI device. This is a 100-percent yield approach. Essentially no electrical tests are made either on the devices or the cells during processing; parametric and functional tests are performed after the interconnection of the cells is completed. Thus, if one cell is bad, the entire array has to be discarded.

E. HYBRID WIRING

Another approach in interconnection is the assembly of several chips onto a ceramic substrate which contains a thick-film pattern that interconnects the chips into the required functional circuit. Each chip may contain 10 to 20 gates, interconnected into convenient subsystems. The wiring pattern on the ceramic can be formed by either thin- or thick-film techniques. To allow crossovers, two levels can be used by applying a glass slurry over the first level of connections and firing. Then the second level of connections is screened over the top. The IC chips are mounted in prepared locations using one of several possible methods: mounted face up with connections made by ball bonding, assembled face down with all connections made simultaneously and directly to the chip (flip-chip assembly), or fabricated with gold beam leads with connections made by welding. The assembled unit can be tested before final encapsulation and any faulty chips replaced.

A distinct advantage of this approach is that standard IC chips can be assembled for medium levels of complexity. Also, this arrangement is very flexible in that combinations of different IC chips can be used, for example, combinations of MOS and bipolar chips. On the debit side are the special test procedures necessary to identify faulty chips, and the high content of skilled labor involved in both the initial assembly and the rework to replace faulty chips.

SECTION III

TEST PROGRAM

The test program was intended to generate data and enable one to draw meaningful conclusions about the capability of the device over a range of stresses and environments. Since relatively few devices were available during the program period, only the following tests and test conditions, which cover a wide range of stresses or environments, were chosen.

1) Life Tests (device evaluation)

2) Shock (storage test, package evaluation)

3) Multi-Level Evaluation

   a) T/H Test

   b) Interfacial leakage test

From the above test data, meaningful conclusions concerning the MTBF of LSI circuits, LSI package design weaknesses and multi-level metallization problems were drawn.

A. LIFE TESTS

The objectives of the life tests were:

1) To isolate failure mechanisms which are time dependent

2) To obtain data on performance degradation as a function of time.

Life tests can be classified into the following groups:

1) Static Bias

2) Storage

3) Operating.

Normally these are specified to be performed at a particular ambient or case temperature. Life testing at elevated temperatures is a useful tool to accelerate device failure mechanisms. The

elevated temperatures enable useful long-term reliability data, applicable to devices operated at ambients of approximately 25°C, to be generated. If the tests to evaluate devices at 125°C are run at 25°C, a time lapse of approximately 10 times longer would be required.

With the above concepts in mind the life tests were carried out at elevated temperatures. The results of the tests would also be used to evaluate bond integrity, package/seal integrity, etc. However, primary attention was focused on only evaluation of the semiconductor devices themselves, together with their multi-level metallization intraconnection patterns.

1. **Static Bias and High Temperature Test**

Objective—The above test was aimed at determining the effect of static bias and high temperature on

1) Multilevel metallization
2) Ball bonds
3) Repair wiring
4) Performance

Test Vehicle—The E-17 device which was used as the test vehicle is a high-speed monolithic two-bit binary counter consisting of two master slave flip-flops internally connected to provide a divide-by-two and a divide-by-four counter. The E-17, 1/2 of an E-30(see Figure 6), contains 12 gates and two flip-flops. The E-17 circuits are completely compatible with TI series 54/74 TTL and DTL logic families.

Characteristics

V_{CC} . . . . . 7.0 V max
Input Voltage . . . . . 5.5 V max
Operating Temperature . . . . . .70°C max
Normalized fan-out from each output is 10 with fan-out to normal 54/74 loads.

Procedure—Two E-17 units were subjected to the following test conditions. A static bias voltage of 2.4 volts was applied to all input pins on the top section(see Figure 6), i.e., input pins whose number designation is greater than 52. V_{CC} was set at 5.0 volts. These were then subjected to 85°C for 500 hours. Followed by another 500 hours at 125°C for a total of 2000 device hours. Both the devices passed the Simplified Array Test System (SATS) functional test before and after the application of the temperature and static bias stresses.

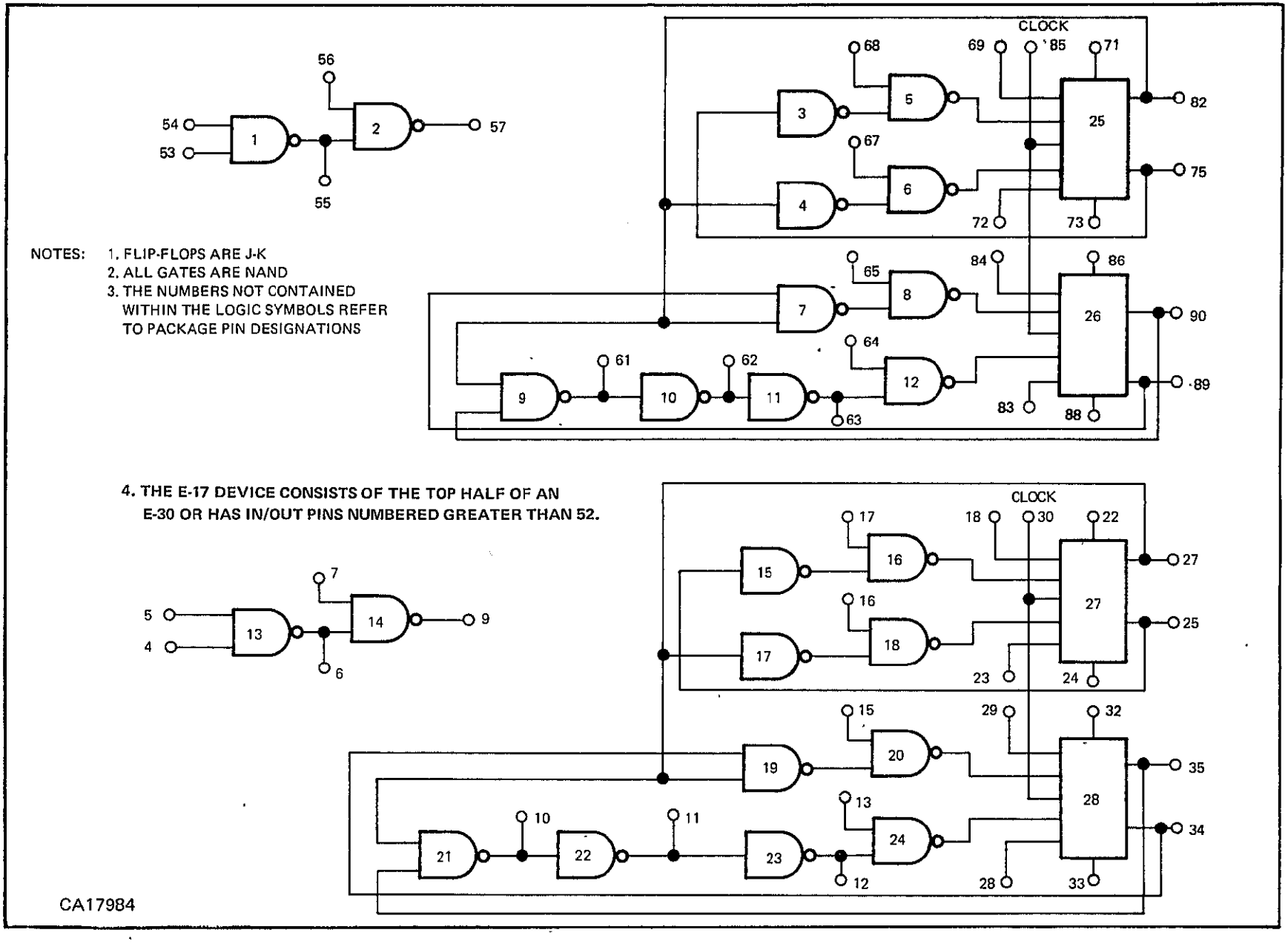


Figure 6. E-30 Logic Diagram

2. High-Temperature Storage Test

Purpose—The purpose of this test is to evaluate the effects of high temperature on the performance of LSI circuits.

Test Vehicle—Two E-17 slices identical to those used in the static bias and high-temperature test were used in this test.

Procedure—The two E-17 slices were subjected to 125°C in an oven with no bias applied and were removed every week for a functional test.

The V_{OFF} and V_{ON} (with load) measurements were taken on each indicated pair with a digital voltmeter (DVM) shunted by a constant 20,000 OHM resistance to ground. This moderate shunting was to allow a desirable current to stabilize the output voltage of the array.

3. Operating Life Test

Purpose—The operating-life test was performed in order to:

1) Isolate failure mechanisms which depend on time
2) Obtain data on performance degradation as a function of time
3) Predict failure rate (MTBF) of the devices

Test Vehicle—Five TA00050 units and six E-30 units were used for this test.

The E-30 consists of two separate sections which are electrically and logically identical (each identical section being an E-17, see Figure 6). The TA00050 is a 100-bit bipolar monolithic serial-in/serial-out dual shift register compatible with standard TI series 54 TTL logic. The two shift-register chains are independently clocked by two sets of clock drivers included in the array. Also contained in the array is an output buffer stage at the end of each chain (see Figure 7) which assures output levels compatible with series 54 TTL and provides a fan-out of 5 from both true and complement outputs. The registers are capable of storing and shifting information at rates from 0 to 8 MHz.

Procedure—Prior to the actual operating life test, the six E-30 devices were given a functional dc check with V_{CC} at 4.5 V, 5.0 V and 5.5 V. In addition, they were subjected to an operational check at 25°C as per conditions described in Table I and Figure 8.

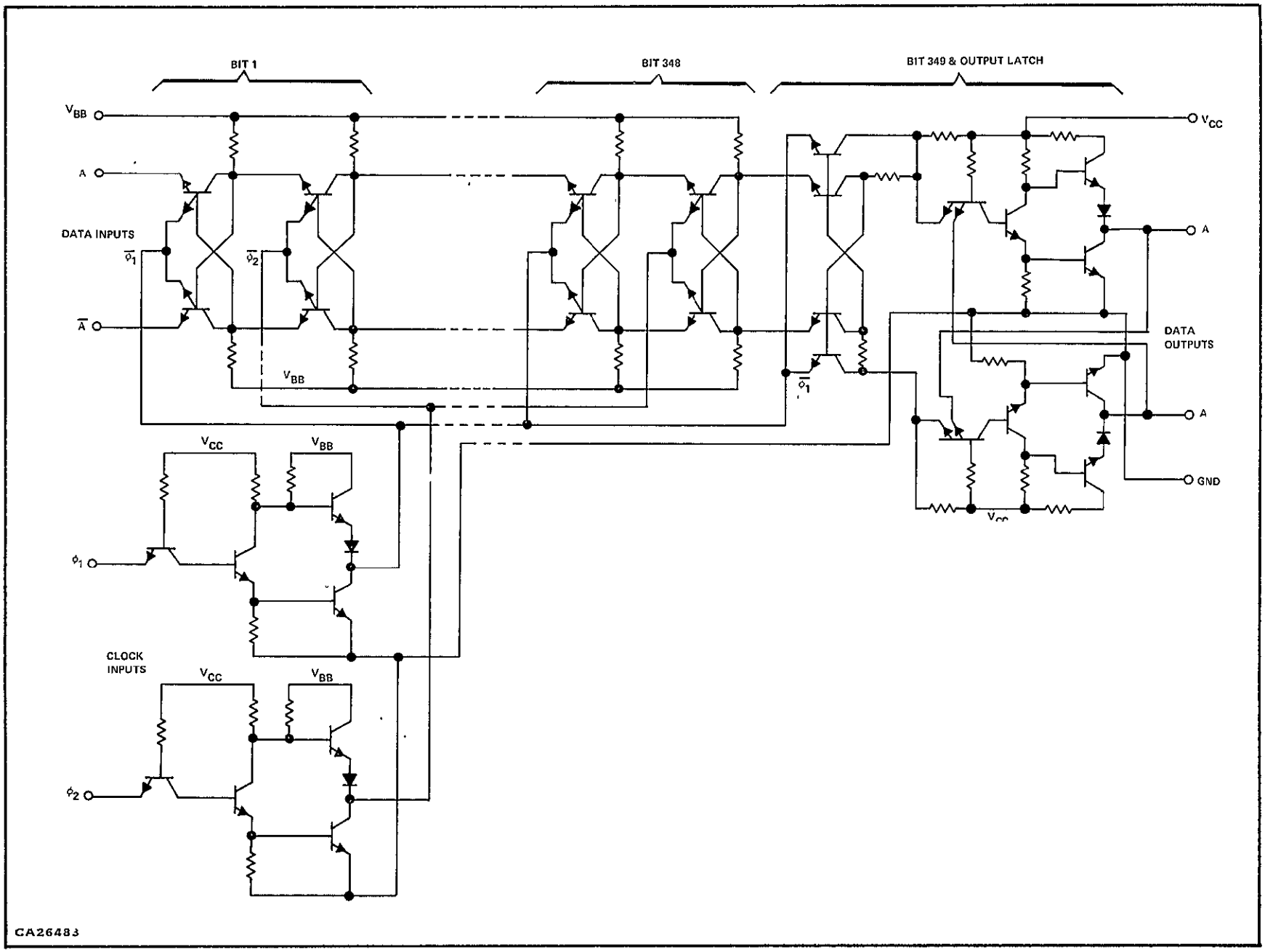


Figure 7. Array Circuits for TA00050

Table I. Operating Conditions

Package Pin No.	Input Voltage	Package Pin No.	Output Voltage
54/5	Figure 8(a)	82/27	Figure 8(b)
53/4	2.4 dc	75/25	Complement of Figure 8(b)
56/7	2.4 dc	90/35	Figure 8(c)
68/17	2.4 dc	89/34	Complement of Figure 8(c)
69/18	2.4 dc	55/6	Complement of Figure 8(a)
71/22	2.4 dc	57/9	Figure 8(a)
67/16	2.4 dc	61/10	Figure 8(d)
65/15	2.4 dc	62/11	Complement of Figure 8(d)
64/13	2.4 dc	63/12	Figure 8(d)
73/74	2.4 dc		
85/30	Figure 8(a)		

V_{CC} = 5.0 volts

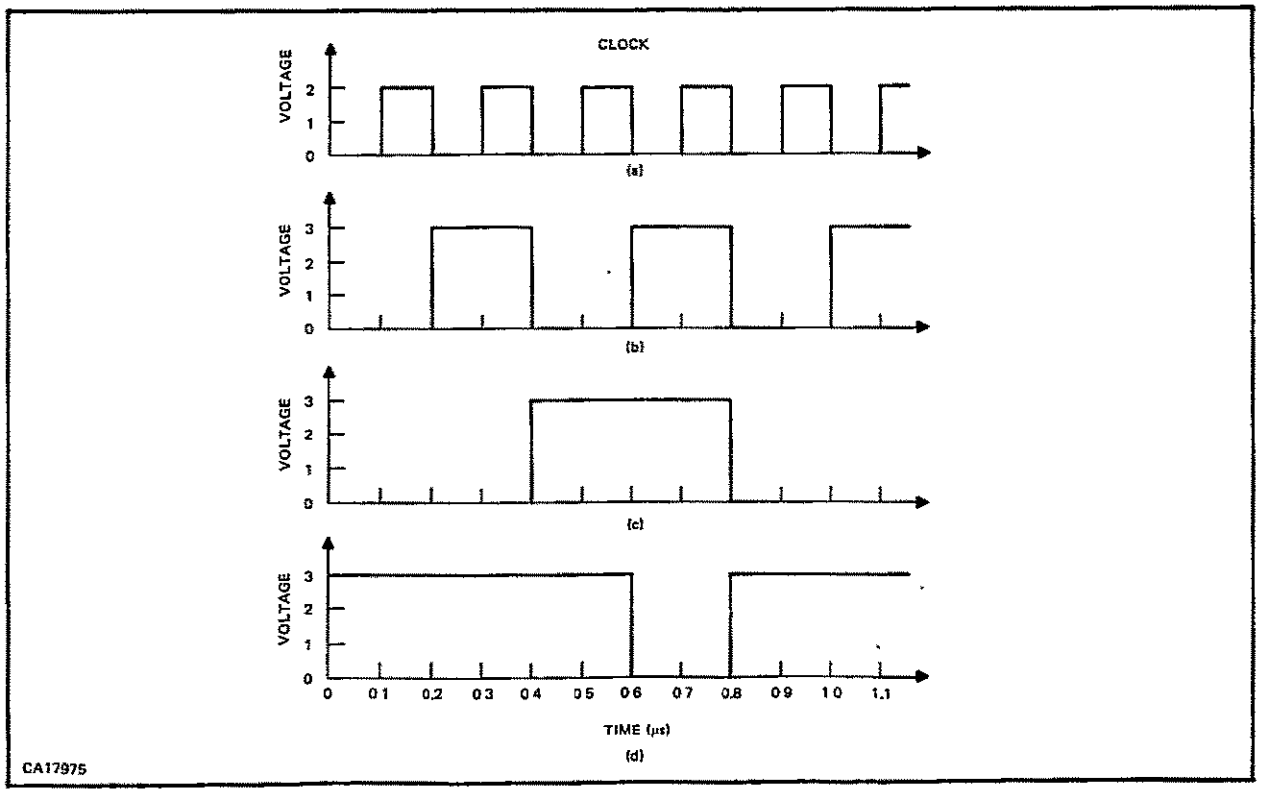


Figure 8. Voltage versus Time Curves for E-30 Operating Life Test

Having obtained satisfactory results from the pretests, the E-30's were subjected to an ambient temperature of 70°C, with all flip-flops and gate inputs at 2.4 volts dc and the E-30's being driven by a 2.0 volt, 5-MHz clock pulse.

4. Life-Test Summary

The results obtained from the above tests are summarized and tabulated in Tables II and III.

As can be observed, there were no failures during the entire period of the test. This was not much of a surprise due to the fact that all the cells that are interconnected by the multilevel metal are those that have passed all the parametric and functional tests prior to metallization.

As a matter of fact, these devices were manufactured about a year previously, and from that time to date, many refinements have been made in the metallization process. Consequently, one can expect the current devices to exhibit improved reliability characteristics.

The fact that there were no failures even after the devices had been subjected to thousands of hours of test and that the devices were not subjected to any burn-in prior to life test, suggests the

Table II. Bipolar LSI Reliability Data

Test Conditions	Device Type	No. Devices	Test Hours	Failures	Device Hours
Operating Life Test @ 125°C	TA00050 (Shift Register)	5	336	0	1680
Operating Life Test @ 70°C	E-30 (Logic)	1	6855	0	6855
Operating Life Test @ 70°C	E-30 (Logic)	5	4984	0	24,920
Static Bias 500 Hours @ 85°C 500 Hours @ 125°C	E-17 (Logic)	2	1000	0	2000
			Total Operating Life		35,455
Storage Life @ 125°C	E-17 (Logic)	2	6094	0	12,188

Table III. Bipolar LSI Test Summary*

Test Condition	Device Hours	Failures	MTBF (60% Confidence)
In-house life tests: operating life and static bias	68,386	0	104.4 Months
Storage life	82,878	0	126.3 Months
TOTALS	151,264	0	231.4 Months
Field Use Data: LSI Computer	14,294	2	7.31 Months

* Actual tests results of in-house elevated temperature testing has been converted to equivalent test hours @ 55°C using the following industry accepted acceleration factors:

Test Temperature	Acceleration Factor to Relate Data to 55°C
70°C	1.5
85°C	2.5
125°C	6.8
150°C	8.0
200°C	18.7

possible elimination of burn-in as a screening test. For this reason, current processing of commercial devices does not include burn-in as standard processing. However, until further data reinforces this position, TI still recommends burn-in as an in-line screen for high-reliability or aerospace applications where reliability is the primary requirement.

B. SHOCK/STORAGE CYCLING TEST

Purpose—The shock/storage test was performed in order to evaluate the ability of LSI packages to withstand shock and high temperature.

Test Vehicle—To cover a range of epoxy-sealed ceramic packages, five different types of ceramic packages (28, 36, 64 and 156 pin) were used. In order to eliminate the epoxy sealant as a variable in this evaluation, all packages were sealed with Shell Epon 9601. Five packages of each configuration were used.

Procedure—The devices were subjected to a test sequence as shown in Figure 9. When the packages were checked for initial hermeticity, using the radioisotope technique (Radiflo), the

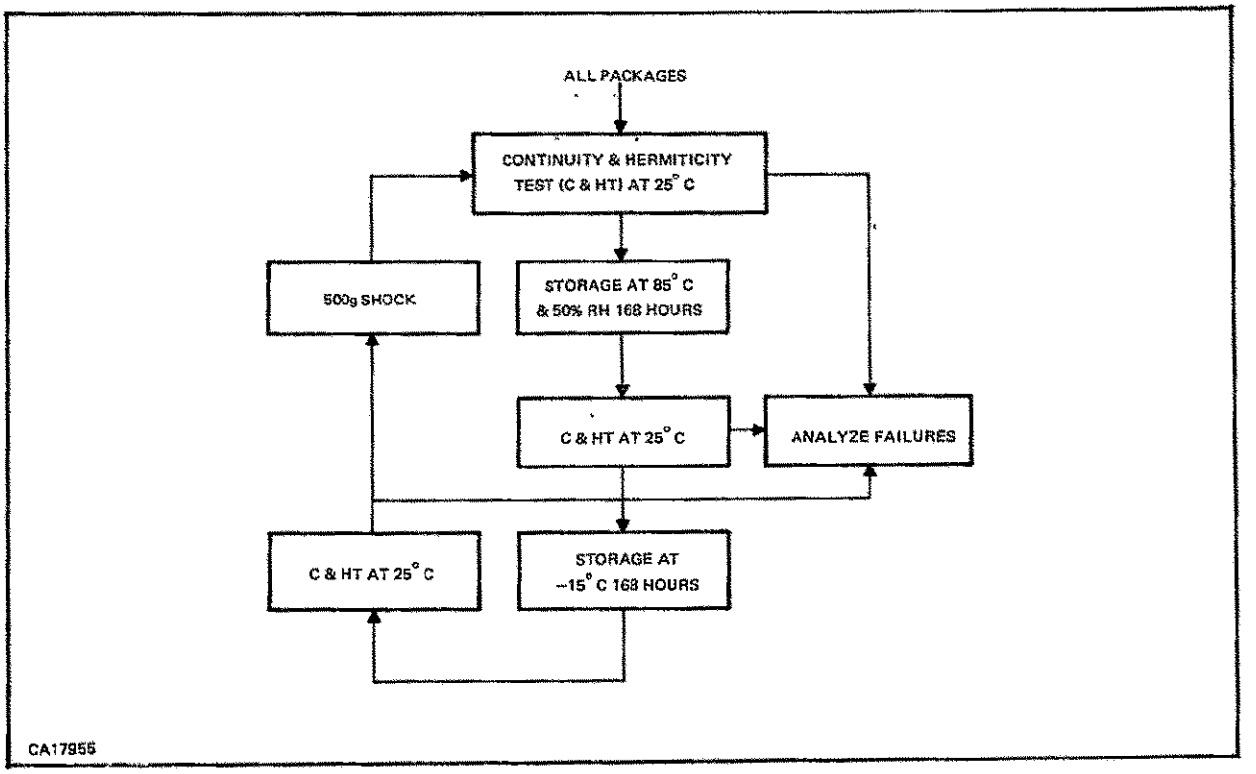


Figure 9. Test Sequence

readings obtained were surprisingly high (see Table IV) of a magnitude greater than the intrinsic or characteristic leak rate expected from the basic package type (flat ceramic). Although the results appeared spurious, the testing sequence was continued. At the same time, the possible causes for the erroneous results were considered.

When the second leak test was conducted, readings less than 10^{-8} atm cc/sec were obtained compared to 10^{-7} atm cc/sec obtained during the first test. The cause of the conflicting results was traced to gas (Krypton) desorption from the outer surface of the ceramic packages. This desorption is very rapid when the devices are removed from the activation chamber and continues to be significant for about ten minutes thereafter.

The above error was discounted and the devices were subjected to the test sequence.

Results—There were no failures of the 28-, 36-, and 64-pin packages which demonstrates the ability of these packages to stand shock/storage. However, in the case of the 156-pin LSI packages, there were no survivors. Since equipment was not available for detection of fine leak on these units, they were checked for gross leak and put on storage-life test. When the units were tested for leaks after storage, two of the devices failed gross-leak tests (the lid of one of the devices had come off) the third device failed gross leak after the shock sequence.

Table IV. Initial Fine-Leak Hermeticity Readings of Storage/Shock Cycle

28-Pin Dual In-Line (Large Lid)	
Serial No.	Reading (atm cc/sec)
1 J	0.83×10^{-7}
2 K	0.83×10^{-7}
3 L	1.16×10^{-7}
4 M	1.33×10^{-7}
5 N	0.83×10^{-7}
AVG	1.0×10^{-7}

36-Pin Flat with Two-Sided Lead Arrangement

Serial No.	Reading (atm cc/sec)
1 A	1.66×10^{-7}
2 B	1.66×10^{-7}
3 C	1.16×10^{-7}
4 D	1.83×10^{-7}
5 E	1.33×10^{-7}
AVG	1.5×10^{-7}

64-Pin Flat with Four-Sided Lead Arrangement	
Serial No.	Reading (atm cc/sec)
1 F	2.16×10^{-7}
2 G	1.83×10^{-7}
3 H	2.00×10^{-7}
4 R	2.50×10^{-7}
5 I	1.50×10^{-7}
AVG	2.0×10^{-7}

156-Pin Flat with Four-Sided Lead Arrangement	
Serial No.	Reading (atm cc/sec)
1 Q	Equipment for reading
2 O	as yet unavailable.
4 P	Gross leak test only

The results of the above tests triggered a series of design reviews and evaluations towards improvement of the package design (see Appendix). These efforts, resulted in the design which is in use today. Thirteen packages manufactured to the present design specifications were subjected to a test cycle as detailed in Figure 10, with no resultant seal failures. Testing is being continued on the new packages and the test results indicate the new package will provide more than adequate protection for the LSI units.

C. MULTILEVEL TEMPERATURE/HUMIDITY TEST

Purpose—The objective of this test was to determine the effect of high temperature and humidity on multilevel metallization and thus evaluate the need for hermetic sealing.

Test Vehicle—Two different combinations of metallization patterns were evaluated. These were basically tungsten-gold and molybdenum-gold metallization systems. Four metallization-evaluation test (MET) structures (tungsten-gold) and two E slices (molybdenum-gold) were used.

The MET structure consists of 28 identical test cells with each cell having three levels of metallization. These cells are placed on a 1 1/4-inch diameter silicon slice and are arranged in a 7 by 4 array. Each cell contains 100 series-connected feed-through holes with a hole size of one square mil and also 1000 one-square-mil metal crossovers. A slice with test cell structure (less third-level metal) is illustrated in Figure 11.

Procedure—The MET slices were subjected to a probe test prior to exposing them to specified levels of temperature and humidity. The probe test consisted of measuring the resistance of 100 series-connected feed-through holes with a hole size of one square mil and also of checking the 1000 one-square-mil cross-over patterns. The test vehicles (E-30 and MET slices) were then subjected to visual inspection and photographs were taken to compare the effects of temperature and humidity on the structure, with the original structure.

The slices were next subjected to a test sequence as detailed in Table V. This test sequence was extended fixing the environmental conditions at 70°C and 95% RH to further stress the units.

After 672 hours of testing the MET slices showed some slight corrosion on the tungsten-gold metallization and after 840 test hours the corrosion was so severe that testing was terminated.

However, the molybdenum-gold metallized samples were not affected until approximately 2184 hours of operation, at which time corrosion was observed on a number of isolated locations across the slice (confined to the third-level metal). The edge of one cell lead pattern appeared to be lifted (see Figure 12).

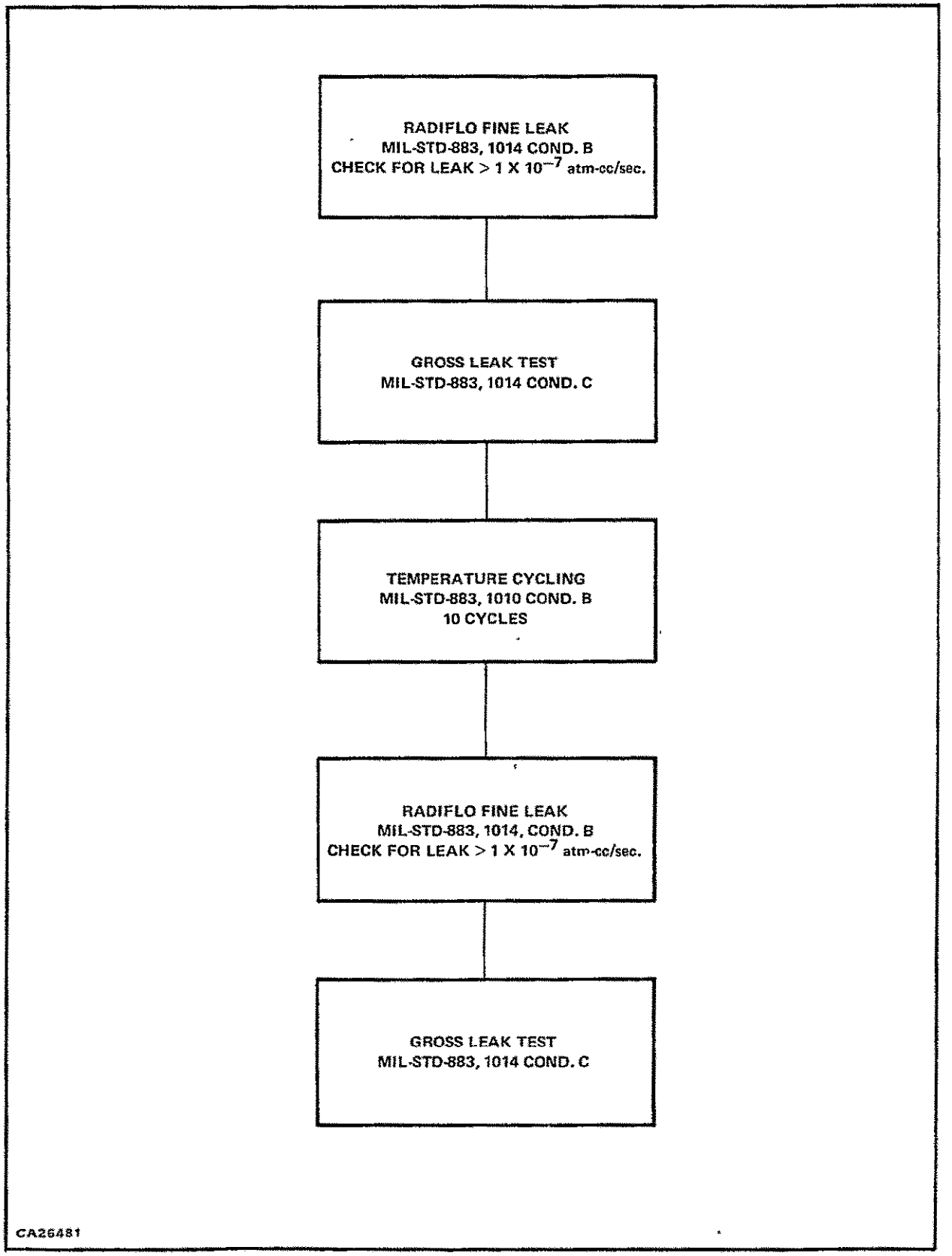
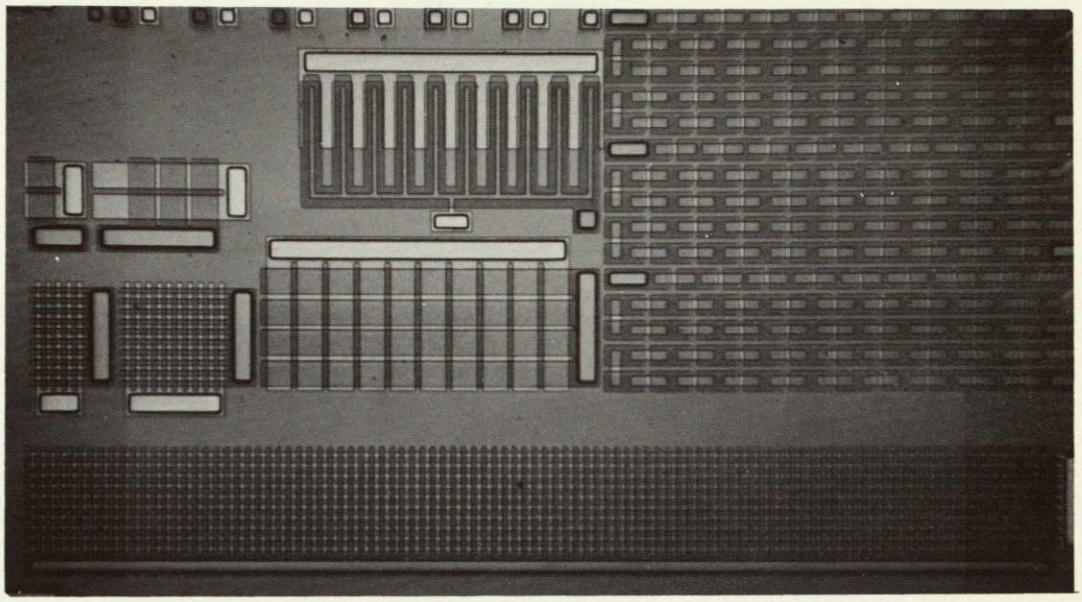


Figure 10. Test Sequence



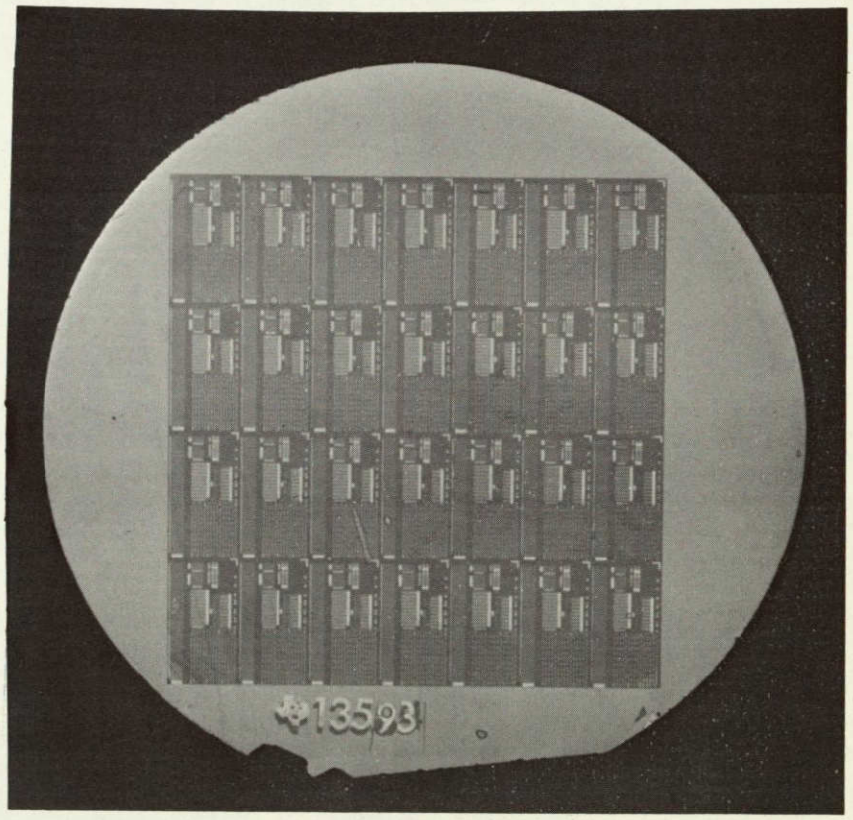


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Figure 11. Metallization Test Vehicle

Table V. Test Sequence for Multi-Level Evaluation

Test Sequence No.	Test Conditions	Duration
1	70°C and 50% RH	168 hours
2	70°C and 75% RH	168 hours
3	70°C and 85% RH	168 hours
4	70°C and 95% RH	168 hours

* After each test step, the slices are checked electrically for open feedthrough connections and interlevel shorts as well as being visually inspected for metallization deterioration.

Results–The above tests, in conjunction with other evaluations, demonstrate that molybdenum-gold is a better combination than tungsten-gold metallization. It also pointed out the advisibility of hermetic packaging of LSI devices used in high-reliability applications.

As a consequence of this test the design engineering effort was directed towards development and finalization of a multi-level metallization and packaging system. After many engineering tests and evaluations, the molybdenum-gold-molybdenum system was chosen for multilevel metal.

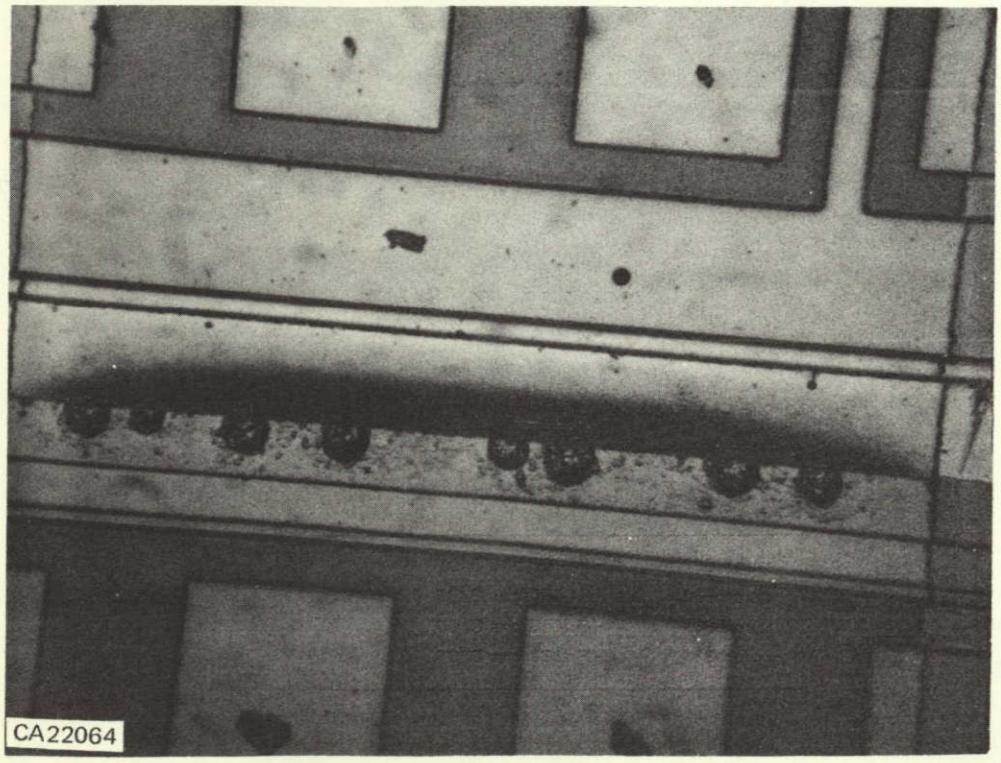


Figure 12. Partially Lifted Gold Lead

D. INTRAFACIAL LEAKAGE CURRENT

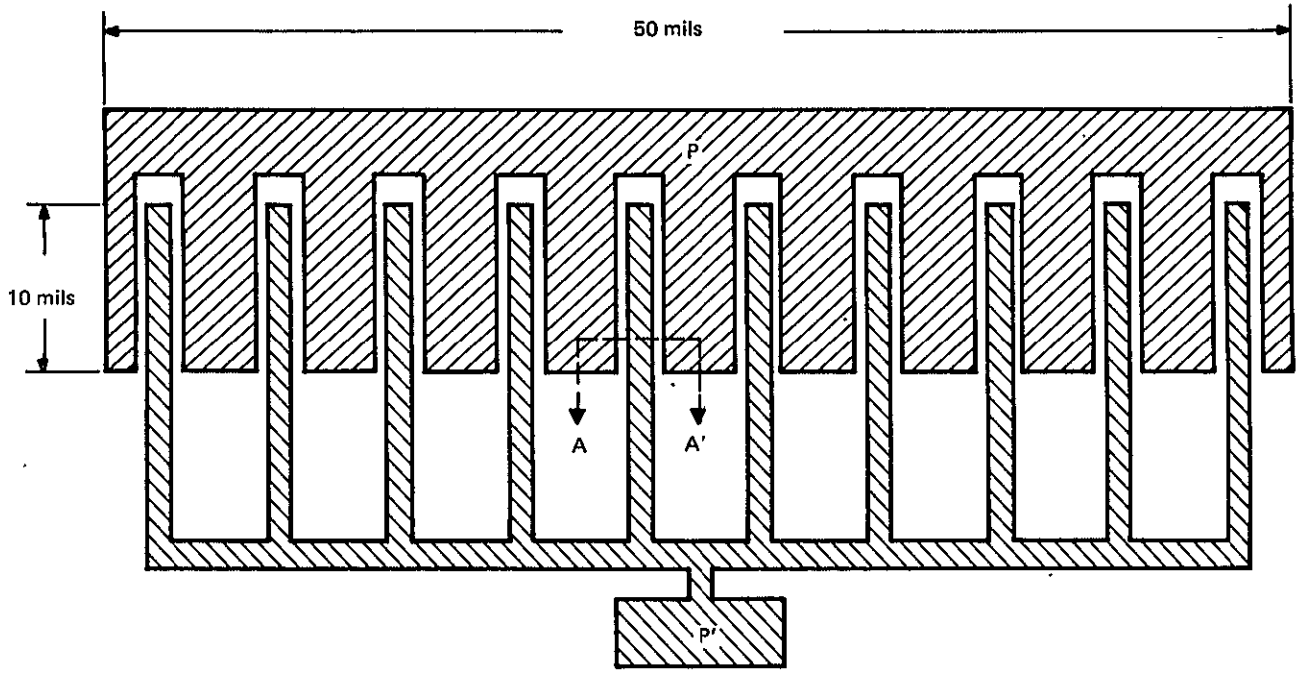
Purpose—In the formation of a bipolar LSI array, the first layer of oxide is thermally grown over the silicon, whereas subsequent layers of oxide are deposited. When the state of the art of LSIs was in its infancy, intrafacial leakage current was thought of as posing a potential reliability problem to devices incorporating multilevel systems. Consequently, conduction at the interface of dissimilar oxides was investigated. The objective of this test was to measure the intralevel leakage current as a function of applied voltage and temperature as well as to determine its significance on the reliability of an IEC.

Test Vehicle—A special test vehicle was fabricated for the above test and is illustrated in Figure 13. It was necessary to deposit metallization pattern on a glass substrate in order to prevent interlevel leakage.

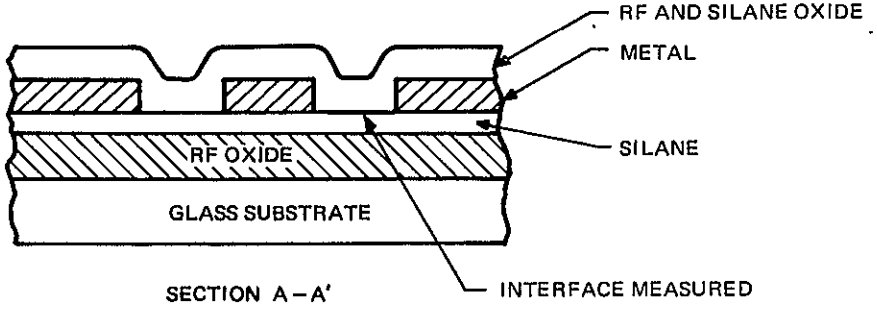
Procedure—The intralevel breakdown problem can be explained by referring to Figure 14. The potential, V, which is applied between the metal conductors, causes a charge distribution to exist on the adjacent conductors. This distributed charge induces a charge at the oxide-silicon interface which causes an electric field to exist in the oxide between the metal and the silicon.

Because the relative separation between the adjacent metal conductors and the metal conductor and the silicon is about 25 to 1, the electric field between the metal and silicon is considerably larger (approximately 10 times) then the electric field between the two adjacent pieces of metal. The net affect was that meaningful intrafacial leakage measurements could not be made because the measurements included the sum of the interlevel and intrafacial leakage current. Also, interlevel breakdown to the substrate precluded measurements at high voltages. By replacing the silicon with glass (a nonconductor) the interlevel-breakdown problem is eliminated. In order to obtain a comprehensive picture of the intrafacial leakage current as a function of temperature and voltage, six test vehicles from two substrates were examined at the following temperatures: 25, 50, 75 and 100°C.

Results—Figure 15 is a plot of current as a function of voltage at each of these temperatures. These curves were obtained from the test vehicle which gave the greatest and least values of leakage current. The average intrafacial current for the six test vehicles at a given voltage as a function of temperature is illustrated in Figure 16. From this data, the intrafacial sheet resistance was determined to be greater than 10^{13} ohms/□ for temperature of 50°C or less than 10^{11} ohms/□ at 100°C. For comparison, the intrafacial sheet resistance of a perfect SiO_2 - SiO_2 interface would be about 10^{19} to 10^{22} ohms/□. Thus, for normal operating voltage (5 volts) and for a temperature of 100°C, one could expect a leakage current level of less than 5 pA/mil for a metal separation of 1 mil. The above results indicate that intrafacial leakage current is not a significant reliability problem.



NOTE: 1. VOLTAGE APPLIED BETWEEN P AND P'
2. THE EFFECTIVE METAL EDGE LENGTH IS APPROXIMATELY 210 mils



SECTION A – A'

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Figure 13. Test Vehicle for Measuring Interfacial Leakage (Not to Scale.)

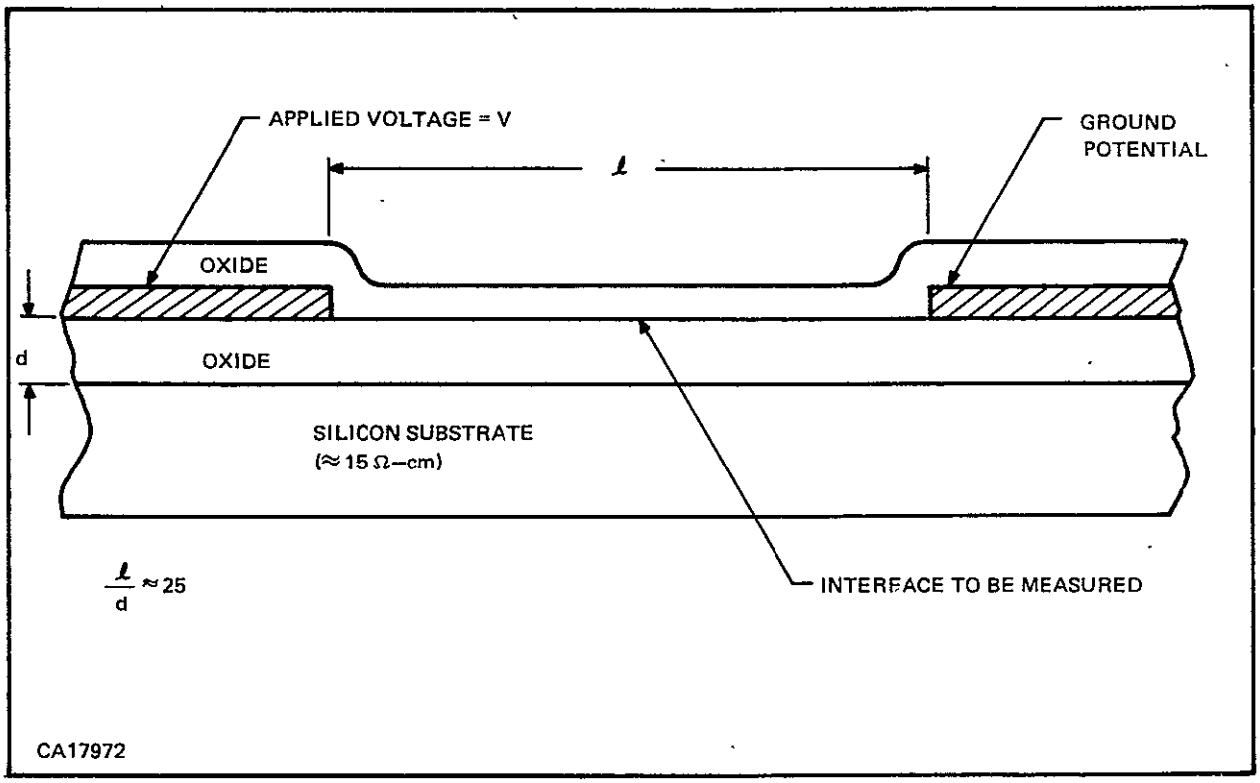

Figure 14. Relative Separation Between Adjacent Metal and the Substrate

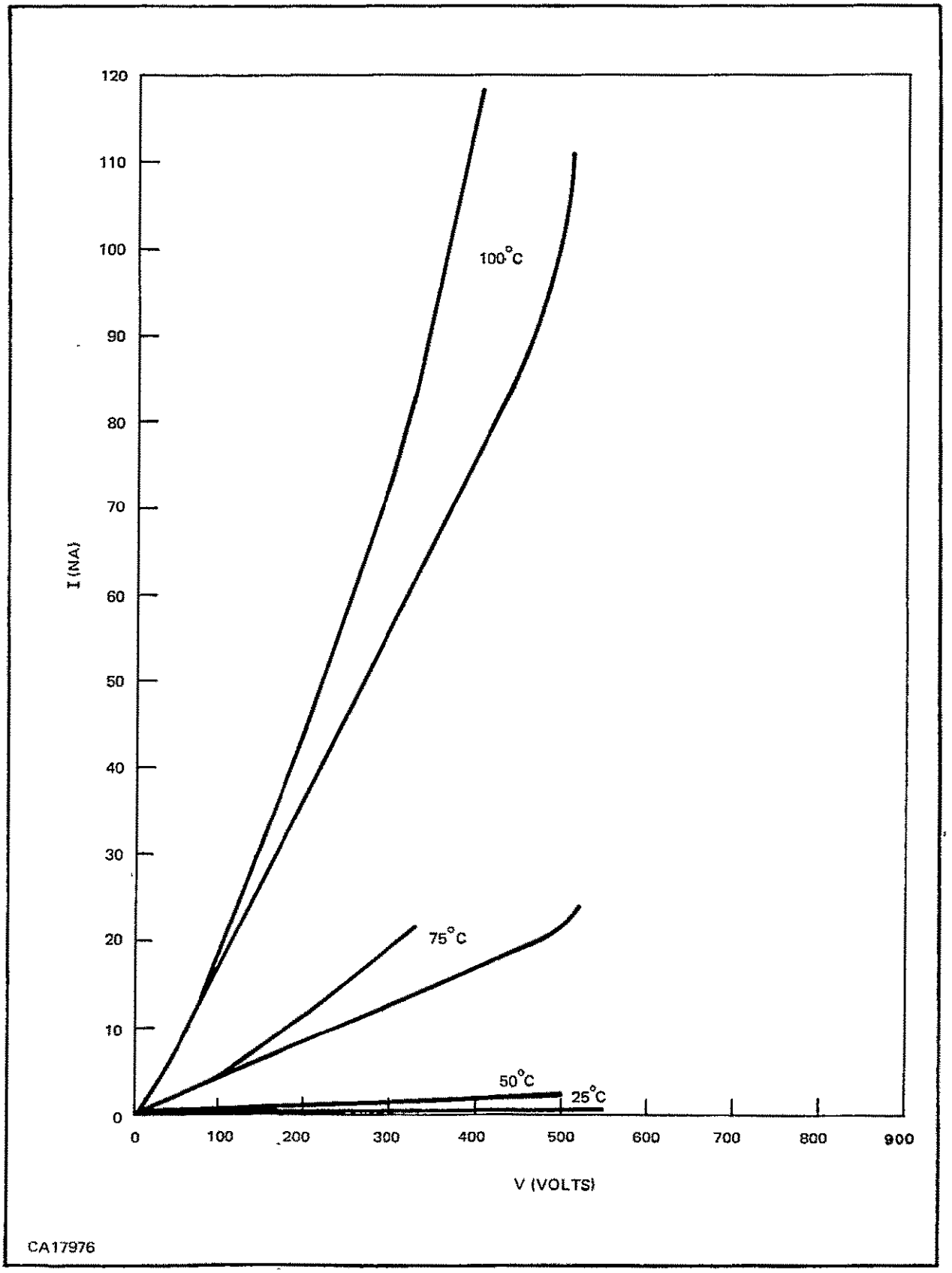

Figure 15. Interfacial Current versus Voltage

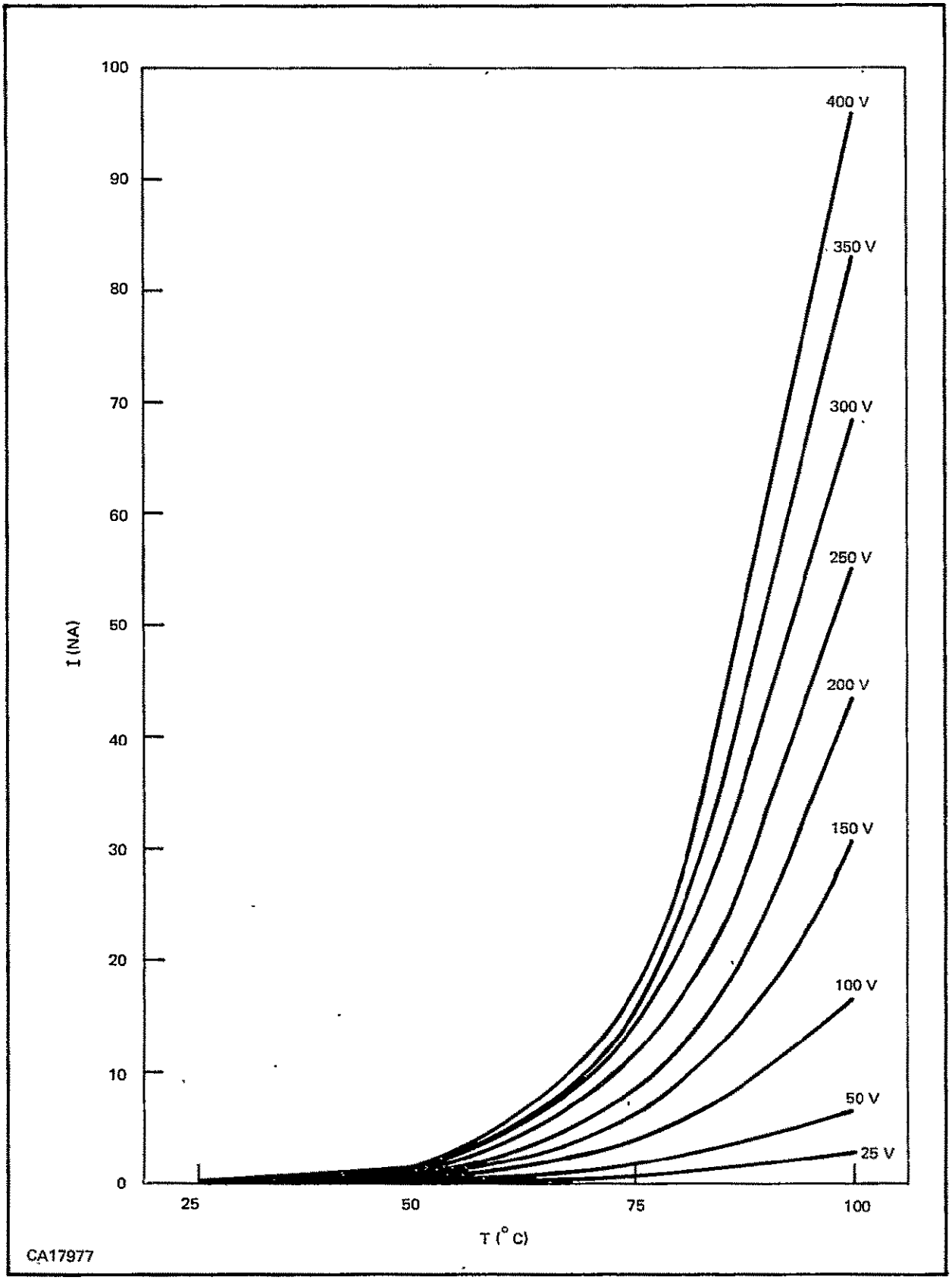

Figure 16. Average Interfacial Current versus Temperature

SECTION IV

FAILURE MECHANISMS

Failures of bipolar LSI arrays can be classified into three broad categories:

1) Slice failure

2) Multilevel-metallization failure

3) Packaging failure.

A. SLICE FAILURE MECHANISMS

Failure mechanisms associated with the slice process through first metal fall in this category. Defects found in processed slices can be identified as belonging to one of the following two groups:

1) Those defects which lead to malfunction of all cells on the slice or of all cells in a large sector of the slice (e.g., contamination, misalignment of mask, improper diffusion control, improper metal etch, etc.).

2) Those which cause some distribution of defects over the slice (e.g., preferential diffusion at crystal defect sites, pin holes in oxide or photoresist, localized mask defects, etc.).

Defects of the second type could cause cell failures during the processing sequence or after the device has been delivered to the customer. Thus, these failures become more important from a reliability point of view. These various failure mechanisms associated with distributed defects are detailed below.

1. Bulk Failure Mechanisms

These are mainly due to crystallographic defects such as dislocation, stacking faults, twins (strain-induced crystal dislocations) and growth strains. These are quite uncommon, yet, as these result in long-term degradations, they are to be taken into consideration when determining the reliability of any semiconductor device.

The diffusion of dopant impurities into silicon will cause the silicon lattice to contract, introducing strains into the bulk material. Excessive strains cause dislocations; since diffusion is enhanced along dislocations, this can cause nonuniformly-diffused junctions to occur. Dislocations also act as nucleation centers for precipitation of interstitial metals. These conditions result in a softening of junction breakdown voltage as well as excessive reverse leakage currents. This is a particularly troublesome failure mechanism because precipitations can occur after the device is in use. Twins and stacking faults also enhance the precipitation of impurities in silicon, but are not as severe as dislocations.

2. Surface-Related Failures

Ionic contaminants (like sodium ions usually present in diffusion furnaces) in the oxide at the silicon-oxide interface and on the oxide surface are sources of mobile charge. Charge migration along the silicon surface, especially in the vicinity of P-N junctions, is a principal mechanism of surface instability and can be directly related to the stability of the transistor parameters.

Another group of failure mechanisms associated with the oxide is pin holes, pores, and impurity inclusions. All of these imperfections reduce the dielectric strength and can also lead to spurious diffusions. Other process-oriented failure mechanisms such as oxide scratches and oxide undercutting can also cause reliability problems.

3. Metallization (Molybdenum-Gold)

Defects associated with thin-film Mo-Au metallization are usually a result of poor process control. A few of the possible metal defects are:

1) Delamination of gold from the molybdenum which is aggravated by molybdenum undercutting

2) Thin metallization at an oxide step which causes abnormally high current densities to exist at the oxide step

3) Improper thickness of metallization

4) Scratches across the metal surface

B. MULTI-LEVEL METALLIZATION FAILURE MECHANISMS

Multi-level metallization failure could be due to:

1) Inter-level or intra-level shorting

2) Opens in metallization at crossover steps or at inter-level feed-through connections.

1. Inter-Level or Intra-Level Shorts

Inter-level shorts are mostly due to oxide pin holes at metallization crossovers (see Figure 17). The usual cause of oxide pinholes is particulate contamination introduced during the oxide deposition process. To help alleviate this problem, a typical insulation deposition process requires the formation of at least two separate layers of insulating material. The first layer consists of RF-sputtered SiO_2 and the second layer consists of SiO_2 formed by the oxidation of silane ($SiH_4 + 2O_2 \rightarrow SiO_2 + 2H_2O$). This two-layer process tends to minimize the occurrence of short-producing pinholes by reducing the probability that pinholes in the two independently deposited oxide layers will be coincident.

The principal cause of intra-level shorts is incomplete metal removal and mask defects.

2. Opens at Crossovers and Feedthroughs

When oxide is placed over Mo-Au-Mo metallization, there is a tendency for a lip of oxide to build up at the edge of the metallization (see Figure 17). This lip can cause the metallization which is deposited on top of the oxide, to build up nonuniformly at the lip and, in some cases, leads to an open circuit or thin metallization (a condition conducive to electromigration) at the oxide step.

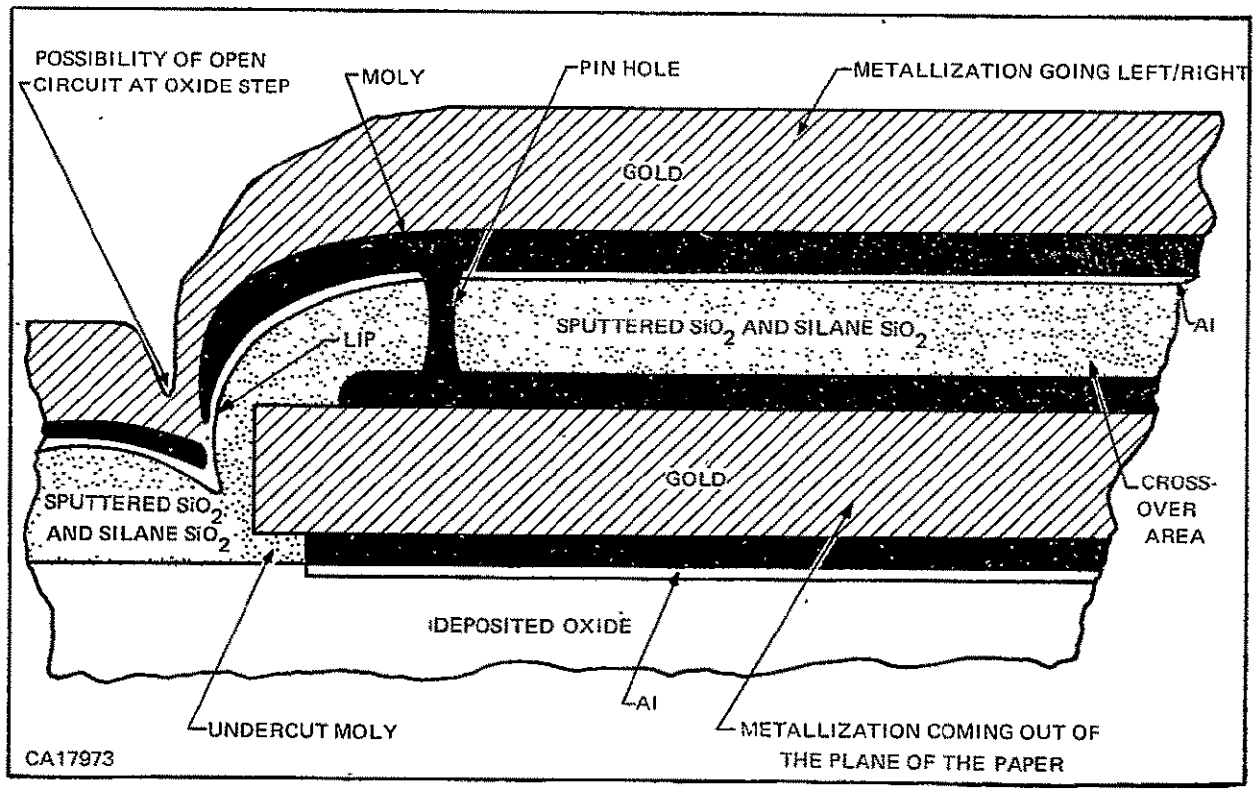

Figure 17. Cross-Section Showing Metallization Crossover (Not to Scale. First-level metal is not shown.)

Open or high-contact resistance at feedthrough holes (i.e., holes to permit interconnection between metallization located on different levels) can be caused by incomplete oxide removal. Note that the feedthrough hole shown in Figure 18 is wider at the top than it is at the bottom. This is due to the fact that silane oxide etches faster than RF-sputtered oxide. High contact resistance could also be caused by contamination at the interface but this problem has not been observed to date.

C. PACKAGE FAILURE MECHANISMS

At present, there are two designs in use for packaging of LSI devices.

First, the ceramic package consists of a flat ceramic base with gold-plated lands and a circular ceramic lid. The slice is mounted on the ceramic base with high-temperature epoxy and connections are made between the slice bonding pads and the metal lands by ball-bonding techniques. The lid is attached to the ceramic base using an epoxy sealant and a metal lead frame is brazed to that portion of the lands which is not covered by the lid.

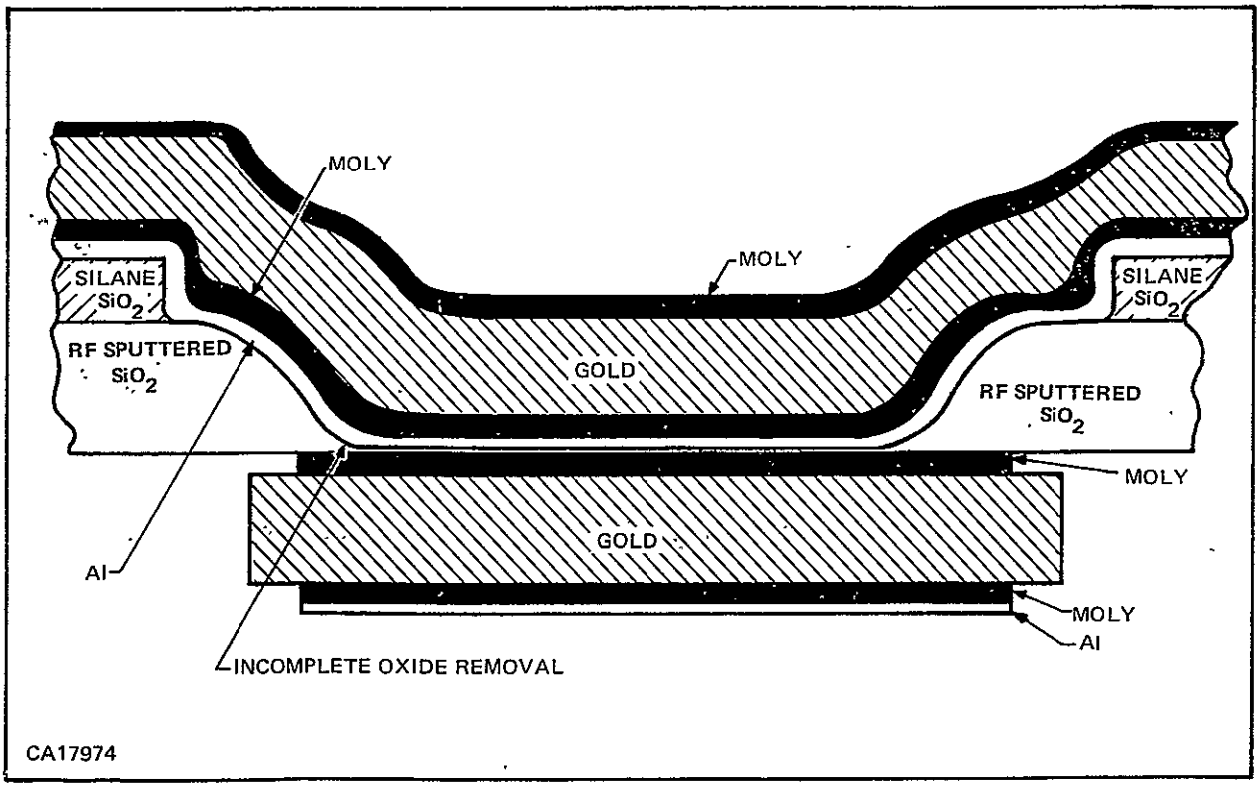

Figure 18. Cross-Section of Feedthrough Connection

Second, the hermetic package differs from the ceramic package in that a (gold-plated) ceramic ring is fired on top of the ceramic base. A gold-plated kovar lid is brazed onto the ring.

The various failure mechanisms associated with the packages are:

1) Failure of the epoxy to bond the slice to the ceramic base
2) Failure of epoxy seal to adhere to metal lands on ceramic header (seal failure in ceramic-lid packages)
3) Failure to effect a continuous seal between ring and kovar lid due to anomalies in either seal-ring or lid geometries (seal failure)
4) Rupture of the ceramic base or lid
5) Failure of ball or stitch bonds to make proper contact (open circuit or high resistance)

D. SUMMARY

Table VI presents comparison of the relative contribution of each class of failure mechanisms to the total number of failures, as predicted earlier (August '68, First Quarterly Report, NASA Contract No. NAS8-21319) and as observed at the present time.

In the developmental stages, due to the complexity of the multilevel interconnection system, it was expected that these interconnections would contribute a major share to the overall failure rate. As the technology matured most of the obstacles were overcome and the percentage failures attributable to multi-levels are at present only 12 percent as compared to the 50 percent that was expected about 1 1/2 years previously.

Table VI. Relative Comparison of Failure Mechanisms

Class of Failure Mechanism	% Total Failure	
	Predicted in 1968	Observed Now
Slice	30	21
Multi-level	50	12
Package and Bonds	20	28
Others	—	39

In spite of the fact that the package design has evolved to a hermetic enclosure, the percentage of failures contributed by package and package/lead interconnections has increased from 20 to 28 percent. The great majority of these failures may be classified as poor bonding and damaged wire bonds, which are attributed to the fact that the bonders are inexperienced and have yet to acquire the necessary skills. It is expected in the near future that the minor problems explained above will be overcome. The number of rejects have been steadily decreasing and every effort is being expended to continue the downward curve.

SECTION V

PRODUCT AND PROCESS CONTROL SYSTEMS

A. PROCESS CONTROL SYSTEM

A conventional product qualification program as a part of a QRA program is one in which samples of the end-product of the process are subjected to a sequence of pre-determined electrical, mechanical, environmental and life tests, (i.e., product examination after the fact) to qualify to certain LTPD's as stipulated by customer procurement documents.

A few factors that make the LSI manufacturing process unique are:

1) Several steps in manufacturing (like masking, etc.) are so critical that any defects at these stages are irreparable

2) The end-product attains such a complexity that parametric testing of all the components incorporated in the slice is impossible

3) By the time the end-product is fabricated it accrues such a value that destructive testing becomes economically unrealistic

Taking into consideration the above factors, and in a large measure as a direct result of this program, TI has developed a new approach which places major emphasis on process-control techniques and a Quality Reliability Assurance Test Program. Rather than relying on just final testing with lot qualification, (lot qualification is less than meaningful for LSI) the above mentioned plan was conceived to insure built-in quality, process stability, and design verification, as well as removal of possible early-life failures.

The process-control considerations can be well understood through an explanation of the process itself. Figure 19 shows a manufacturing flow diagram encompassing Quality Control (QC) inspection points and criteria for inspection. An explanation of the TI philosophy pertaining to QC points and their impact on the finished product is pertinent at this point.

Too often the role of QC in process control is misconstrued to be that of a "policeman". This attitude evolves when QC points are placed in a process so that QC simply checks on the work of the manufacturing inspectors.

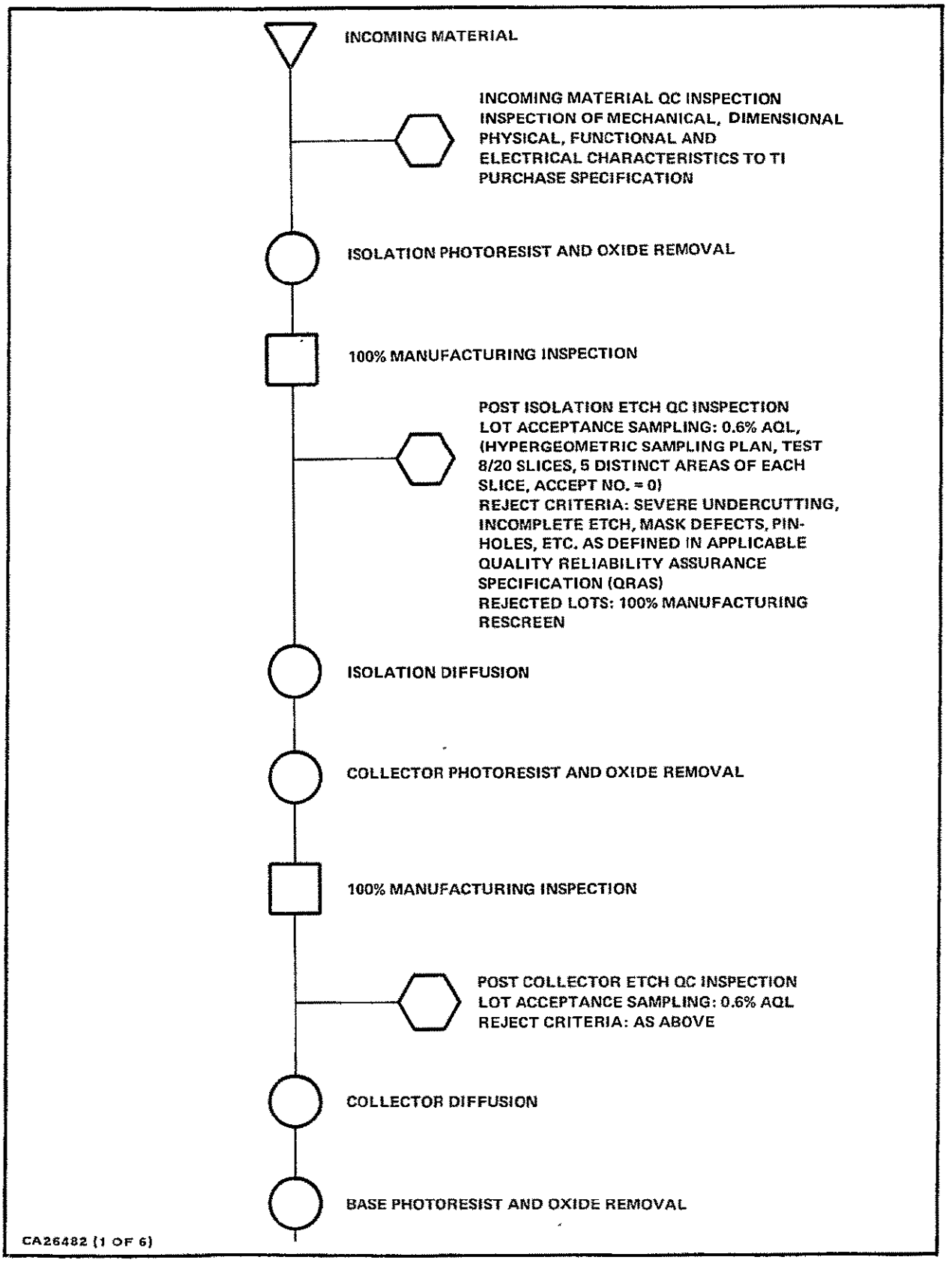

Figure 19. Logic Device Flow Diagram (Sheet 1 of 6)

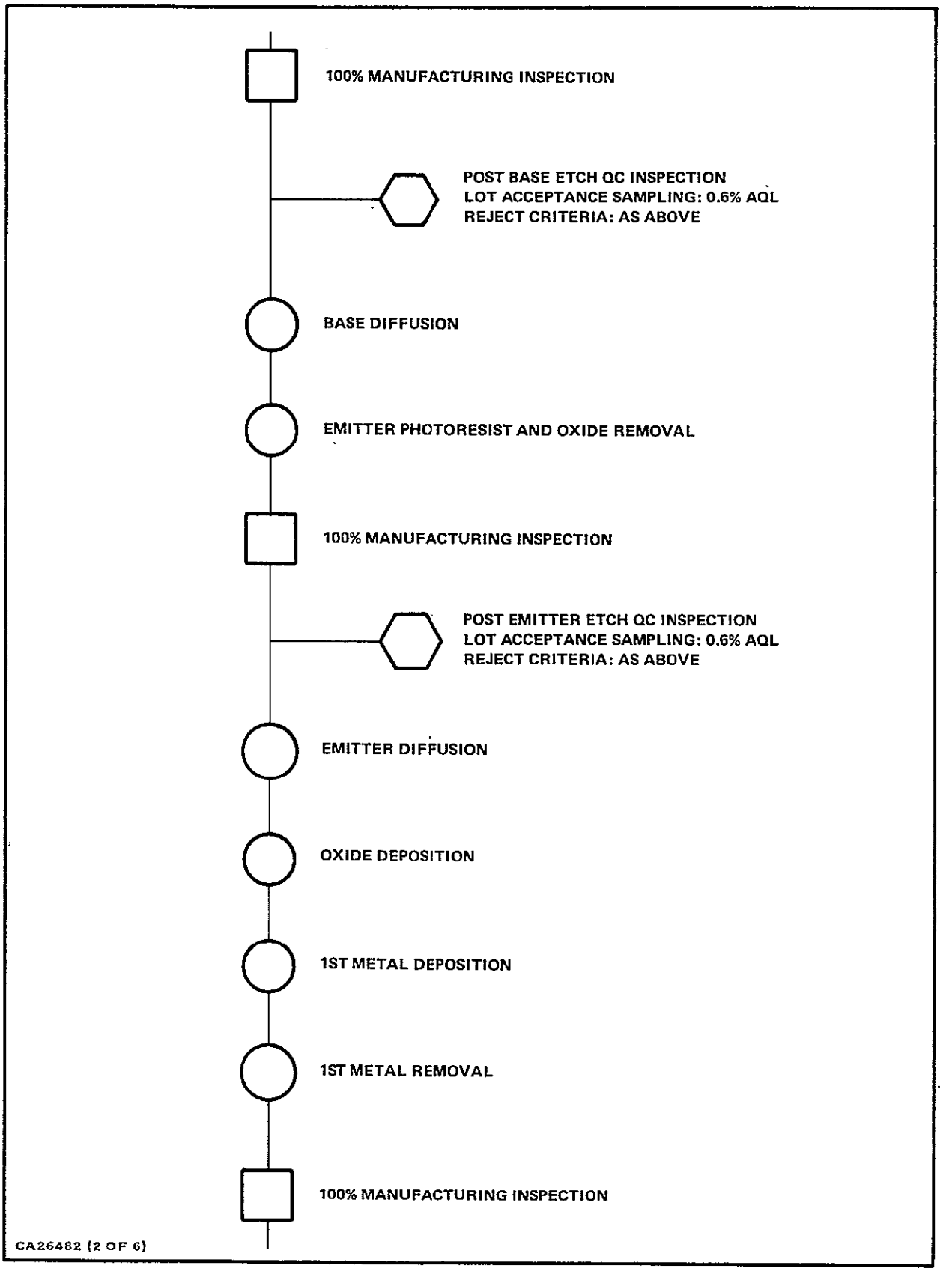

Figure 19. Logic Device Flow Diagram (Sheet 2 of 6)

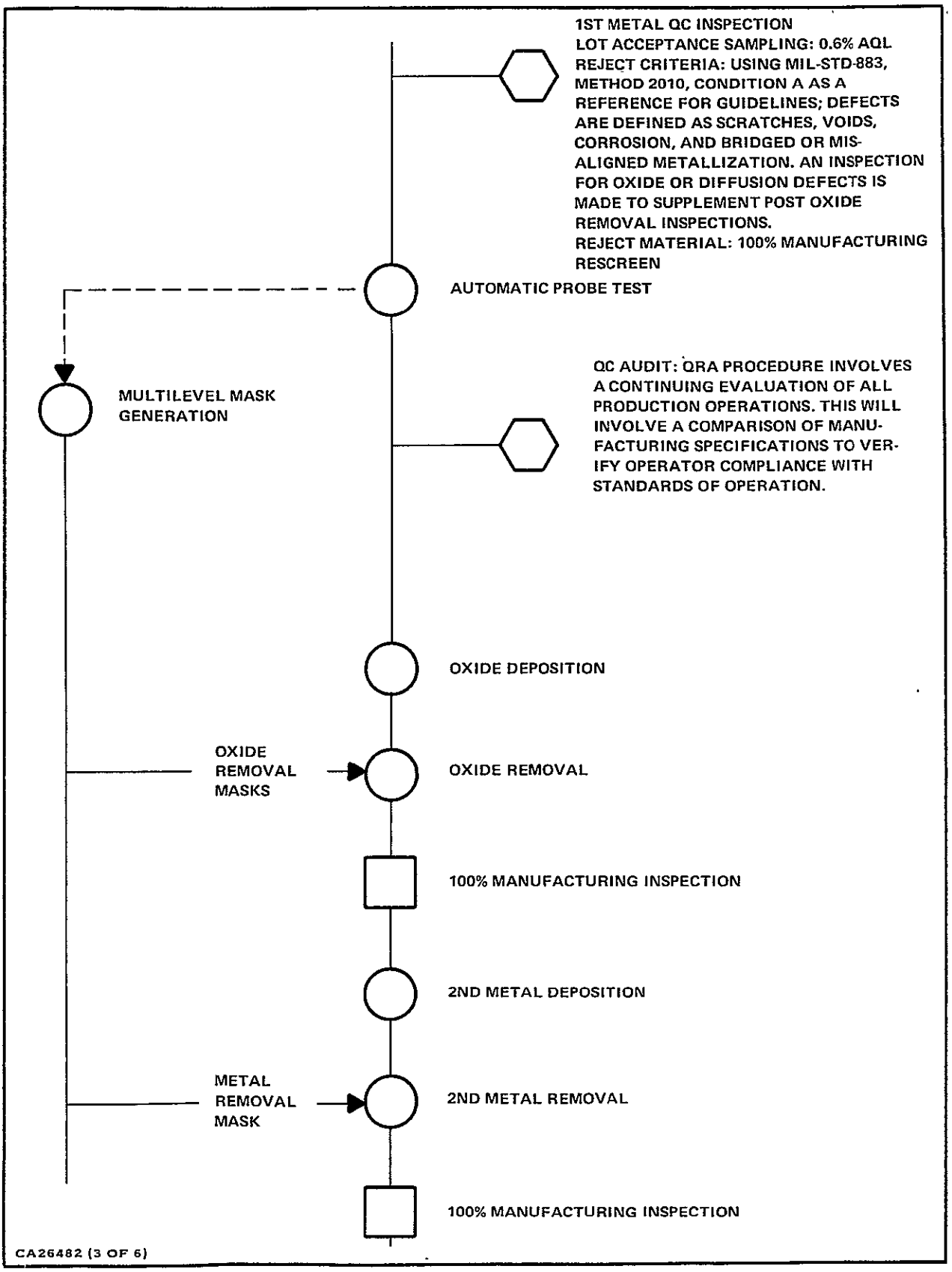

Figure 19. Logic Device Flow Diagram (Sheet 3 of 6)

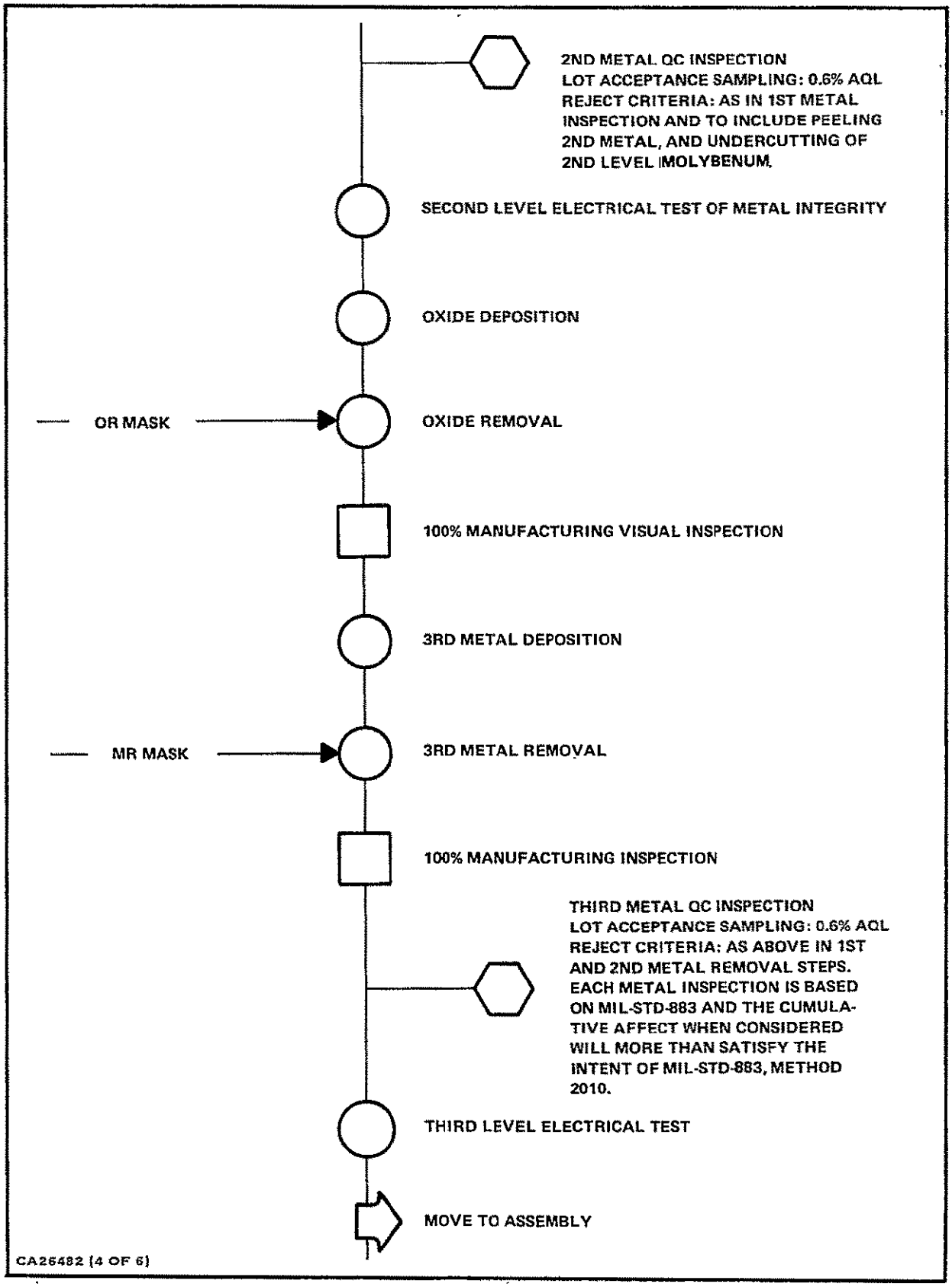

Figure 19. Logic Device Flow Diagram (Sheet 4 of 6)

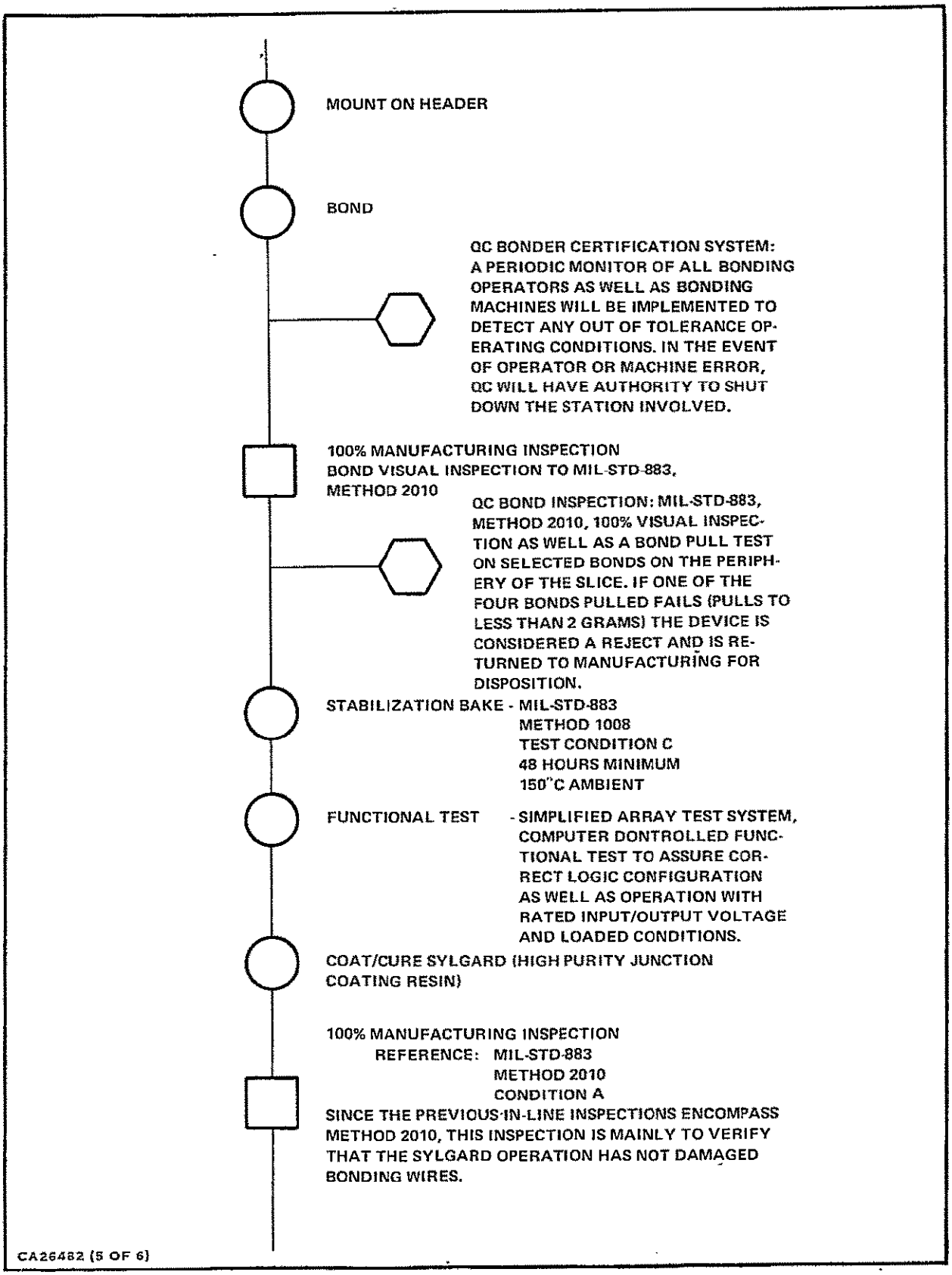

Figure 19. Logic Device Flow Diagram (Sheet 5 of 6)

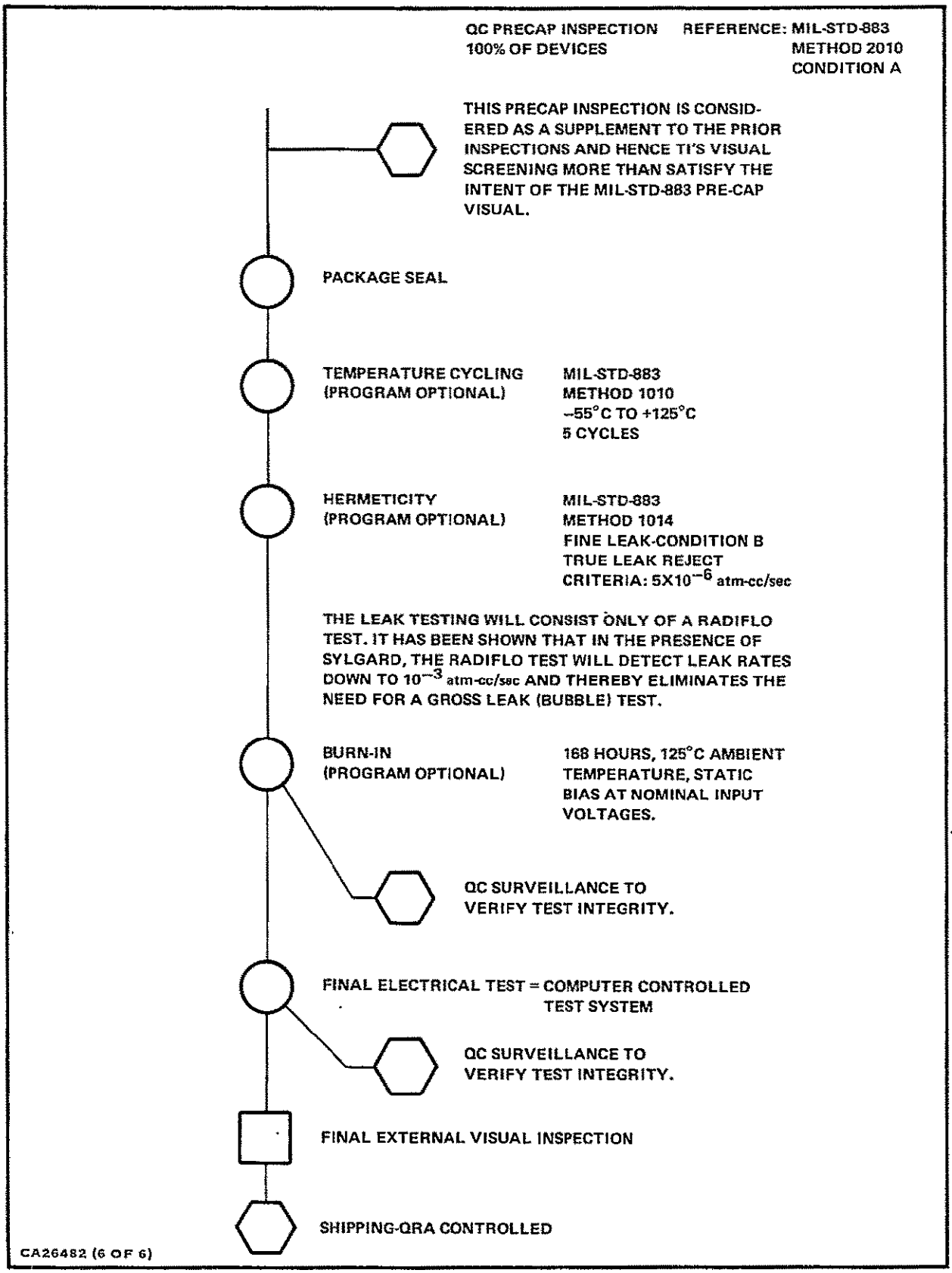

Figure 19. Logic Device Flow Diagram (Sheet 6 of 6)

The term "policeman" comes from the traffic directing of good or bad slices; the QC inspector becomes the primary individual responsible for product integrity. An example of this would be that of placing QC inspection station just prior to an etch operation but after a 100% manufacturing inspection for that operation. Because of this arrangement, manufacturing inspectors often become lax in their job, knowing that QC will catch any defects they neglect before the slices are etched.

In an effort to upgrade the role of process control, a new philosophy for avoiding this situation has been incorporated into the TI LSI process. The goal is essentially to motivate manufacturing personnel to be responsible for their mistakes. Referring to the previous example, this can be done by moving the QC inspection point to a post-etch position. In this light, manufacturing inspectors and operators must be more responsible for product quality because any defects they pass will, when etched, result in defective slices. Consequently, QC now assumes its proper role of inspecting slice/lot integrity on a lot-acceptance basis at critical control points, while providing real-time feedback for on-line corrective action to the process. This is shown in the flow diagram (see Figure 19); hence, we see that TI's LSI process control program focuses on establishing operator integrity and thereby building quality into the array.

In order to monitor the stability of the manufacturing process, and ultimately the level of reproducibility for a given product, the TI Quality Control program also includes a QRA test program.

Under the QRA test program, samples are periodically chosen from the outgoing products and subjected to various electrical, mechanical, environmental and life tests. The data generated in these tests will, in addition to establishing a realistic assessment of the stability of the manufacturing process, also provide meaningful and current reliability data.

B. LSI SCREENING PROCEDURES AND TECHNIQUES

As can be seen from the flow diagram (Figure 19), certain screening and inspection operations have been incorporated in the LSI manufacturing flow. These process controls involve both quality control inspections in the process as well as the screens after package sealing as shown in Figure 19. The testing procedures and philosophy concerning each screen after package seal are detailed below. These tests after seal are meant to remove any units that could possibly adversely affect system reliability.

1) Temperature Cycling (Metal-Lid Package)—This temperature cycling test will eliminate any devices that would become non-hermetic over their operating life, as well as uncover any devices that could have multi-level metal delamination faults when exposed to temperature stresses (at this point in time this has not proven to be

a problem). Loss of hermeticity during life could conceivably result in contaminates or corrosion at the slice surface. The stress as applied, −55°C to +125°C is meant to reflect actual operating conditions rather than applying an artificial overstress.

2) Hermeticity (Metal-Lid Package)—As outlined in the flow diagram, Figure 19, the LSI hermeticity tests consist only of a radioisotope fine leak test. Tests have shown that when Sylgard is present within the package, the Radiflo test will detect and register either gross or fine leaks, because of the absorption of the tracer gas by the Sylgard. The reject criteria is 5×10^{-6} atm-cc/sec (calculated) which is consistent with criteria of MIL-STD-883 for packages with internal cavities greater than 0.1 cc.

3) Burn-in—Burn-in will be employed as an in-process screen for all high-reliability device requirements. At the present time, data indicates that burn-in has limited value and for this reason, as well as economic considerations, burn-in will not be a standard process for commercial devices. In the event of minor device failures at burn-in, limited rework will be attempted (as per Section V-C). After any rework another burn-in cycle will be performed.

4) Final Electrical Test—The final electrical test subjects the array to another computer-controlled functional test to verify that array performance has not been degraded by the previous environmental screens.

5) Final Visual Inspection—This final visual inspection, in conjunction with Quality Control inspections at time of shipment, will verify product mechanical and visual integrity. This inspection will be based on MIL-STD-883, Method 2009.

The above tests, and those of the flow diagram of Figure 19, are integral to standard LSI processing; as such, they will eliminate the great majority of devices that are potentially unreliable. In the event a potential user requires an extraordinary degree of confidence in the integrity of the arrays supplied, additional tests could be implemented but the ability of additional testing to enhance the system reliability is doubtful.

Additionally, most other tests as defined in MIL-STD-883 are not suitable for 100% screens since they are considered destructive. Added confidence in the LSI arrays could be made available through a testing program of representative devices in a supplementary QRA test program that would be meant to establish and maintain process or line qualification.

C. REWORK FEASIBILITY AND TECHNIQUES

As has been reported in previous quarterly reports, the major defect associated with the discretionary routing (multi-level metal) of an LSI unit is the contouring problem of metal leads

over oxide steps (cross-overs). Defect densities associated with this process have been established as typically 1 defect per 100,000 crossovers for a well controlled multi-level process. A typical complex array of 250 gates will have approximately 5000 crossovers. Since defect densities are so low a maximum of one repair is expected per array for multi-level lead defects.

In the event that a multi-level metallization defect is isolated it is repaired on the surface of the slice by using wire-bonding techniques. One-mil diameter gold wire is thermo-compression bonded to bridge the multi-level defect. To prevent wire movement after repair bonding on the slice surface the wire and surrounding slice area are coated with Sylgard (a high-purity junction-coating resin). The result is a repair that has high electrcial and mechanical integrity.

In addition to the rework procedures described above for discrete multi-level defects, the possibility of total cell failures or out of specification condition exists for the cells formed by the first level of metal. These cell defects after multi-level are rarely observed, but to enable repair of the array a unit cell of each type used on the slice has bonding pads brought up to the third-level metal. In the event of a cell failure, the failed cell is removed from the logic implementation (by opening interconnections with current overstresses) and bonds are made to insert the replacement cell. As described above the bonding wires are coated with Sylgard.

A study is presently under way to set up criteria to limit the number of repair bonds. This study is based primarily on economic considerations. There is a point where too much manufacturing cost is added to the unit as a result of manual rework procedures by highly trained technicians. These preliminary studies have shown that a maximum of one cell and four discrete metal flaws can be replaced and still maintain a favorable manufacturing cost.

At this time, no array failures have been a result of rework procedures on the slice surface. In addition, as more strict process controls evolve and the multi-level metal process becomes more refined, an even smaller defect density is expected. Thus, slice surface rework should be entirely eliminated.

The rework procedures discussed above have centered on in-process rework methods. However, field-use failures can also be reworked in the same manner. The major obstacle to this rework is the resealing of the hermetic package after delidding. A delidding apparatus is currently being designed and should eliminate this obstacle to rework of field failures.

SECTION VI

CONCLUSIONS AND RECOMMENDATIONS

A. SUMMARY OF LSI ADVANCEMENTS DURING CONTRACT PERIOD

Major accomplishments during the contract to "Establish Quality Standards for Bipolar LSI" centered on the investigation of predominant failure mechanisms for multi-level metallized LSI units as well as their elimination by process controls or design modifications.

The major failure mechanisms as detailed in Section IV and seen during the work on this contract involve the following areas:

1) Multi-level metallization systems failures
   a) undercut molybdenum
   b) delamination of molybdenum
   c) thin metallization at oxide step
   d) scratches on metal surfaces
   e) inter-level or intra-level shorting due to oxide faults or incomplete metal etch
2) Package Failures
   a) seal failure
   b) wire bonding failures

The failure mechanisms as listed above have been greatly reduced in frequency through efforts connected with this contract. The processing steps and screening methods already employed (or in the process of being effected) to limit these failure modes are as follows:

1) Multi-level metal failures
   a) An optimization of metal-etch time coupled with comprehensive visual inspections has controlled the problems associated with undercut molybdenum.

b) The delamination of RF-sputtered molybdenum to silica has been eliminated by applying a thin flash of Al under the Mo-Au-Mo metallization. The Al-Mo-Au-Mo metal system is applied in three cathode RF-sputtering equipment so that the metals are applied without breaking vacuum and, hence, the possibility of contaminants is alleviated. The reaction between Al and SiO_2 is thermodynamically favorable and a strong flash bond is effected. In addition an annealing step after metallization relieves stresses through Al recrystallization and improves the Mo-Au eutectics to provide a more reliable metallization system.

c) In order to solve the problem of thin metallization at an oxide step, as well as that of high-resistance feed-through contacts, a change was made in multi-level insulation thickness. The RF-sputtered oxide thickness has been increased. It is applied with a temperature gradient (change with time) to enhance etching characteristics. The thickening of this oxide coupled with the application of a second oxide layer (silane SiO_2) has all but eliminated oxide pinholes, metallization opens at oxide steps, as well as feed-through contact problems.

To reinforce these process advances a 100% visual inspection (that is, five selected areas of each device) is performed by manufacturing inspectors. In addition after this 100% inspection, Quality Control performs a lot acceptance screen as per the flow diagram in Figure 19. These double inspections will also eliminate scratches or other handling-induced metal faults.

2) Package failures

a) The lack of an advanced package in which to mount the LSI slice was a major constraint on aerospace use of LSI units when this reliability contract was begun. The epoxy-sealed 156-lead ceramic flat pack was determined not to provide adequate protection in a temperature-cycling environment or to provide a seal that was impervious to moisure. Hence, the present hermetic kovar-lid package (see Appendix) was developed. This package has proven to be more than adequate in tests that simulate end use environments.

b) Wire-bonding has proven to be a weak link in the LSI production process. However, in recent tests it has been determined that the gold-to-gold bonding method (gold-wire to gold-land on package and slice surface) is a very reliable bonding technique. The early failures were due mainly to operator incompetence. These recent tests have shown no failures in bond-pull tests where the reject criteria was a broken bond at a pull of 2 grams or less. In order to insure that this level of bond integrity is maintained, each LSI device will have four extra bonds (not necessary for device functionality) placed in

selected areas over the slice. These bonds will then be pull-tested to insure the continued integrity of the bonding operation.

It is concluded that these steps, as defined above, have substantially enhanced the end-use reliability of LSI. In conjunction with these processing changes, the in-line screens necessary to insure quality LSI units are defined in the flow diagram of Section V. These screens, based on the state-of-the-art bipolar LSI today, will provide LSI units consistent with their intended use as electronic sub-systems.

B. RECOMMENDATIONS FOR LSI PROCUREMENT

The following suggestions are made as guidelines for the determination of screening procedures in the procurement of any LSI units. These recommendations should be used in conjunction with the General Quality Reliability and Maintainability guidelines contained in Volume II of this report.

1) Screening procedures of MIL-STD-883 should be used as valuable aid in the formulation of in-line screens.

2) Screening levels of MIL-STD-883 (intended primarily for ICs) must be re-evaluated so that screening procedures more closely reflect actual end-use conditions rather than subject the LSI units to artificial overstress conditions.

3) The most valuable Reliability Assurance program for LSI will take advantage of the small quantity orders (due to the replacement ratio of LSI to IC) to utilize 100 percent in-line screens rather than lot qualification at overstress conditions.

4) Any environmental testing that is felt necessary and must be done at overstress levels (and is therefore a destructive test) should be performed on test devices for the obvious economical considerations.

5) In-process quality control must play an ever increasing role in LSI reliability considerations due to the difficulty of detecting weaknesses with after-the-fact screens.

6) Since it is impossible to perform electrical tests with every input/output combination considered (the time to test even at millisecond speed by computer control is prohibitive) an acceptable solution must be negotiated between producer and customer. Generally, the customer must rely on the producer's expertise in this LSI testing area, and merely attempt to verify the quality of the test procedure.

C. RECOMMENDATIONS FOR FUTURE DEVELOPMENT OF QUALITY LSI UNITS

In addition to the above recommendations for LSI procurement today, the following areas for further work in the development of quality standards and processing methods should be investigated to develop more reliable LSI devices.

1) A study of current methods for LSI testing (both probe and final test) should be undertaken to establish a philosophy as well as techniques for improvement of these tests.

2) A study of the strength of LSI devices as applied to multi-level metallization, thermal integrity, slice mounting, package and hermetic-seal characteristics for a range of stresses could be undertaken to establish a stress-strength model to be used in predicting reliability of LSI devices.

3) Studies on the use of infrared analysis techniques for possible identification of failure mechanisms could be undertaken.

4) Studies of the applicability of line or process qualification techniques and methods to the inherently limited production runs of LSI devices.

APPENDIX

LSI PACKAGE EVOLUTION

LSI PACKAGE EVOLUTION

With the advent of monolithic large scale integration and the enormous increase in complexity of semiconductor units made possible by this technique, a rather unusual set of packaging requirements became apparent. The various package design constraints imposed by large scale integrations are:

1) The large slice size amplified the effect of any thermal expansion mismatch between the silicon slice and the package material.

2) Due to the increased complexity, a large number of exterior connections are required. These numerous leads must be spaced far enough apart to be easily handled, placed in connectors or attached to printed-circuit boards. However, since one of the potential benefits of LSI is an advance in system miniaturization, the overall package must be reasonably compact lest this advantage be lost.

3) Due to the heat generated by their operation, an effective heat-dissipation system must be incorporated into the design.

4) The final major constraint involves dealing with the reliability of the finished part, especially its ability to continue functioning through exposure to various forms of abuse. The added cost of generating and processing a unique interconnection system for each array makes the value of a completed array such that no losses attributable to the packaging process can be tolerated.

In an effort to overcome the above constraints various designs were tried. The earliest LSI packages utilized an etched, gold plated Kovar lead frame to which the slice was bonded. The assembly was then potted with resin to form a protective package (see Figure 20). As a result of the high-viscosity characteristics of the available resins, damage resulted to the lead-frame assembly.

At the same time the plastic package was being developed, a parallel effort was concentrated on the development of inorganic ceramic packages. The original inorganic package design consisted of a ceramic substrate and a potted epoxy cover. Again the potting of resins were found damaging to the slice and lead-frame assembly.

This led to the development of an all inorganic package. The early packages of this type consisted of a flat ceramic header with the lead frame bonded to the top surface (see Figure 21).

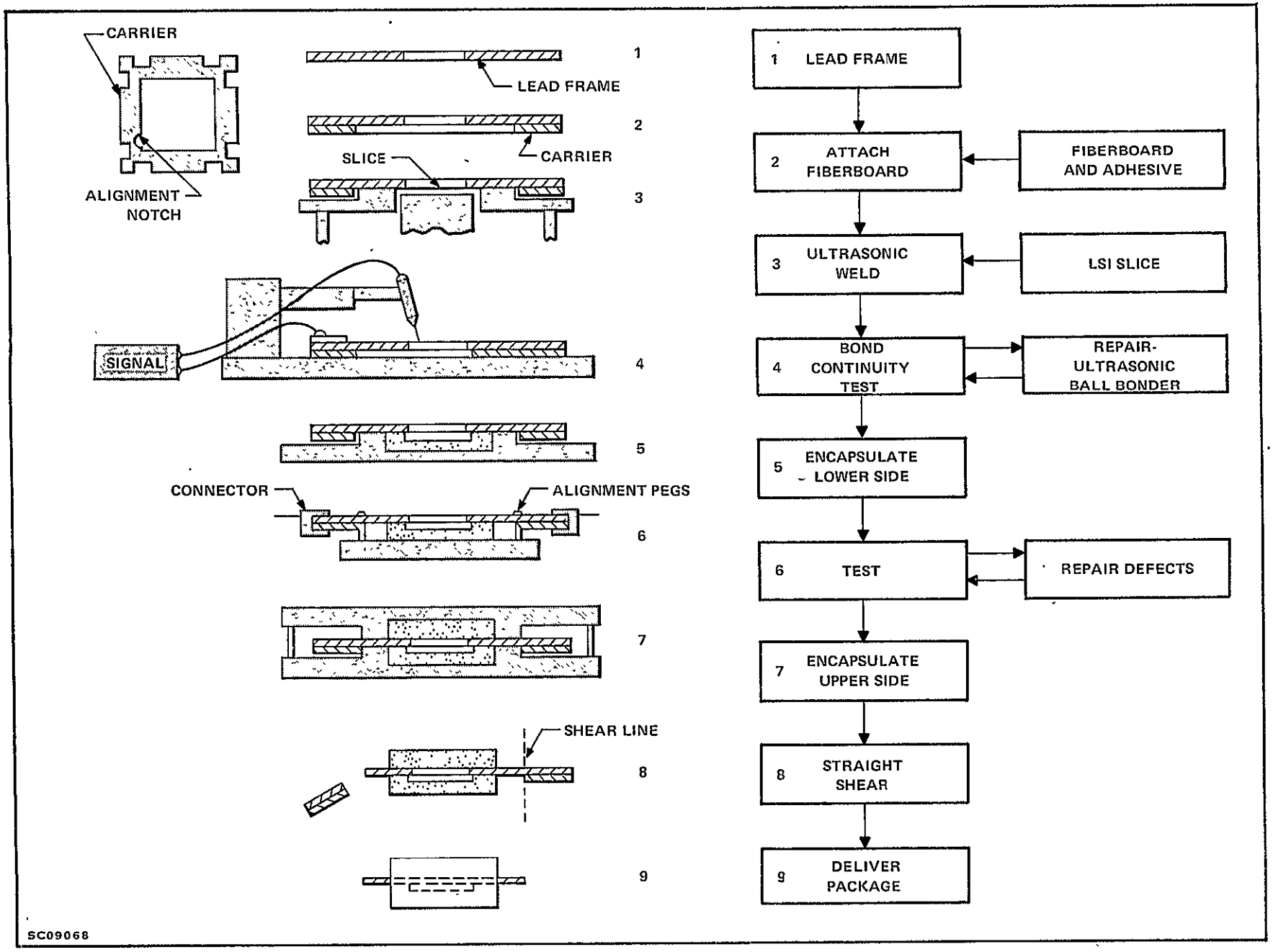

Figure 20. LSI Array Packaging

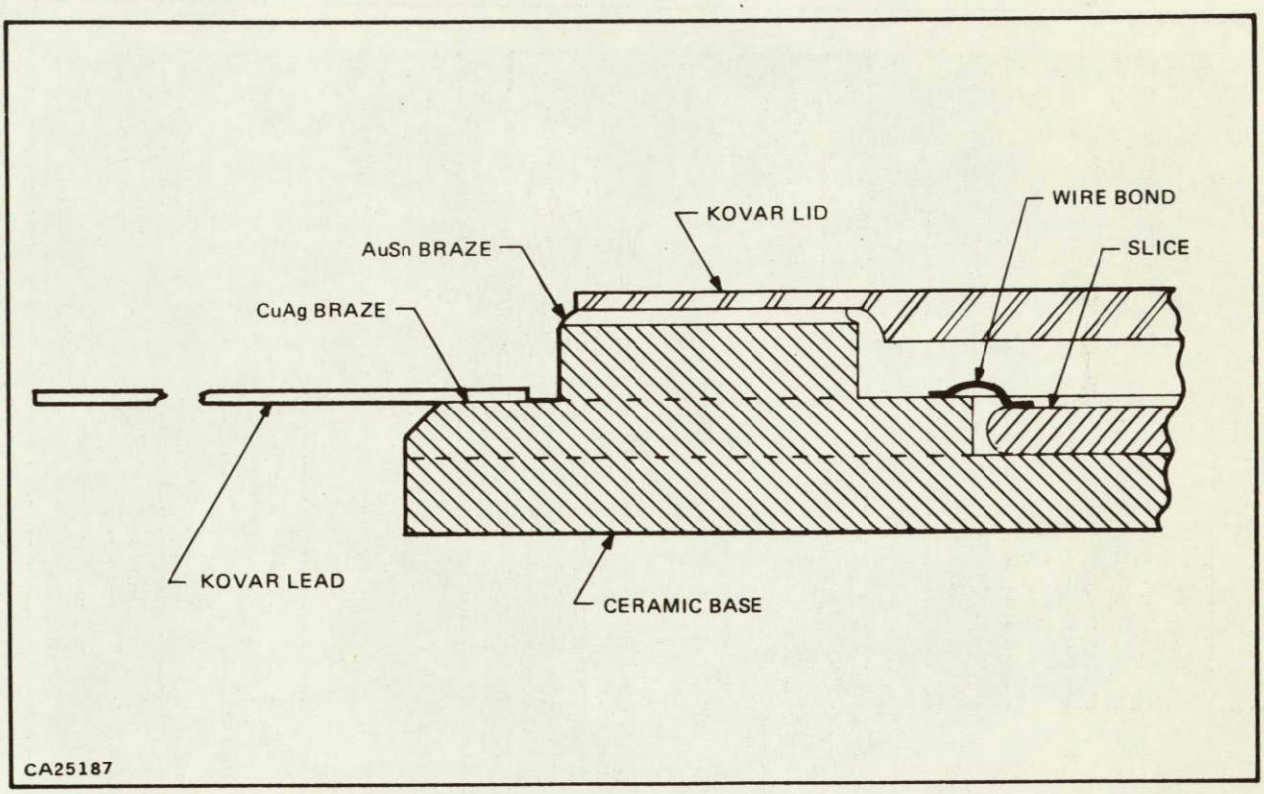

Figure 21. LSI Hermetically-Sealed Package Construction

The slice was mounted onto the header using epoxy. The ceramic lid, epoxy sealed to the header served as a cover to the package.

Since the top edge of the slice lies above the surrounding header, downhill bonding was necessary to connect the slice to the metallized conductors on the header. Downhill bonding created problems of bond shorts to the slice edge and little protection was offered to the slice because of its top surface mount.

In these types of packages the sealing was done using an epoxy ring (see Figure 21). The epoxy ring was placed on top of the interior leads circling the slice and its lid was set on the epoxy. The assembly was then baked to cure the epoxy. This sealing method often produced a reasonably hermetic package but not a package that retained its hermeticity during environmental testing.

In an effort to overcome the above defects, a package redesign was undertaken. The resultant header consists of three layers of ceramic, (a base with two additional layers fired to it) with the leads sandwiched between the upper two layers (see Figure 22). The two upper layers of ceramic form a central cavity to accommodate the slice. The cavity is capped with a lid. A Kovar lid with a brazed seal (using high-frequency current pulses) is used for the hermetic packages (Figure 22) and a ceramic lid with an epoxy seal is used for the non-hermetic package (Figure 23).

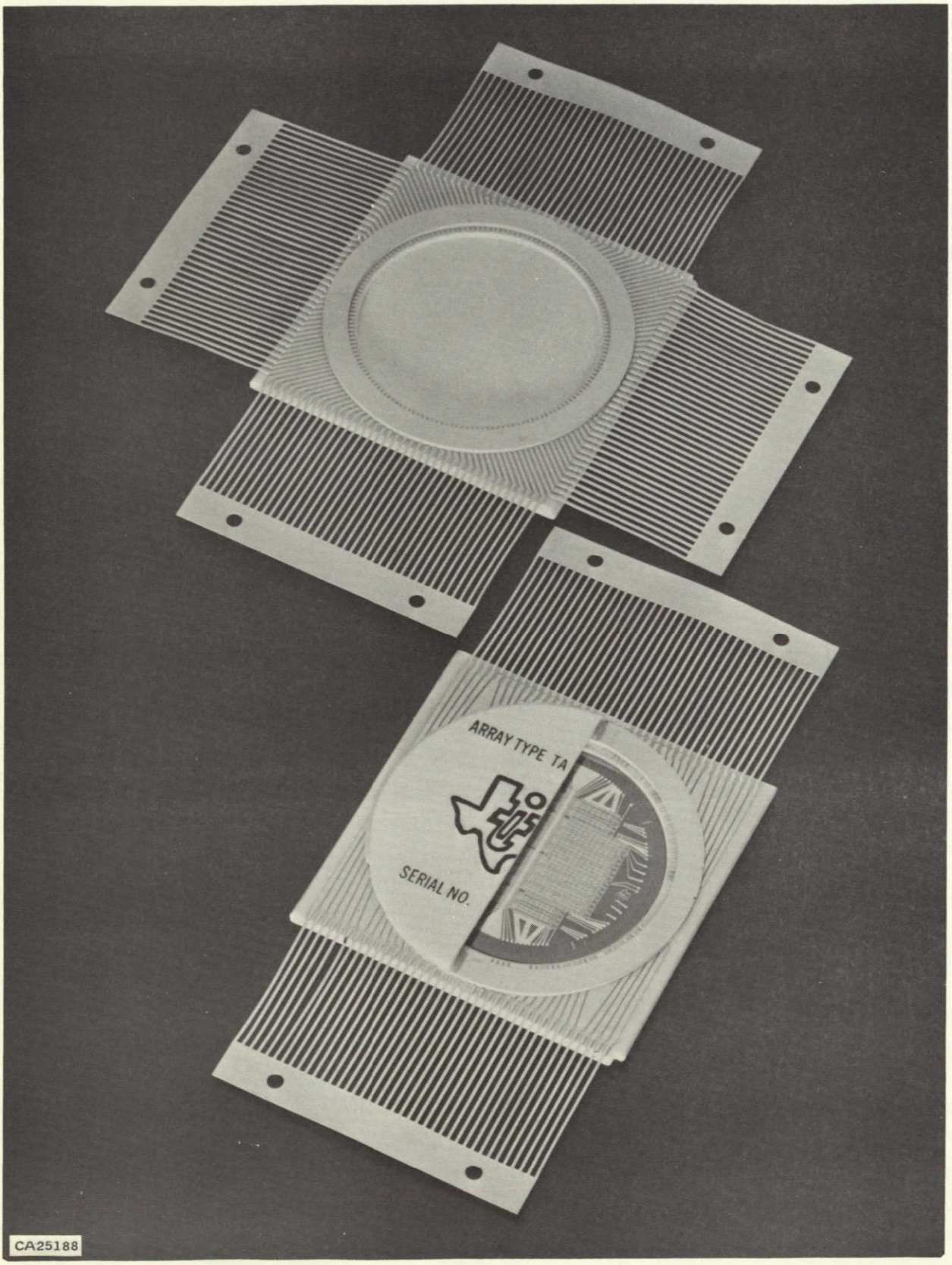

Figure 22. 156-Lead and 78-Lead Packages

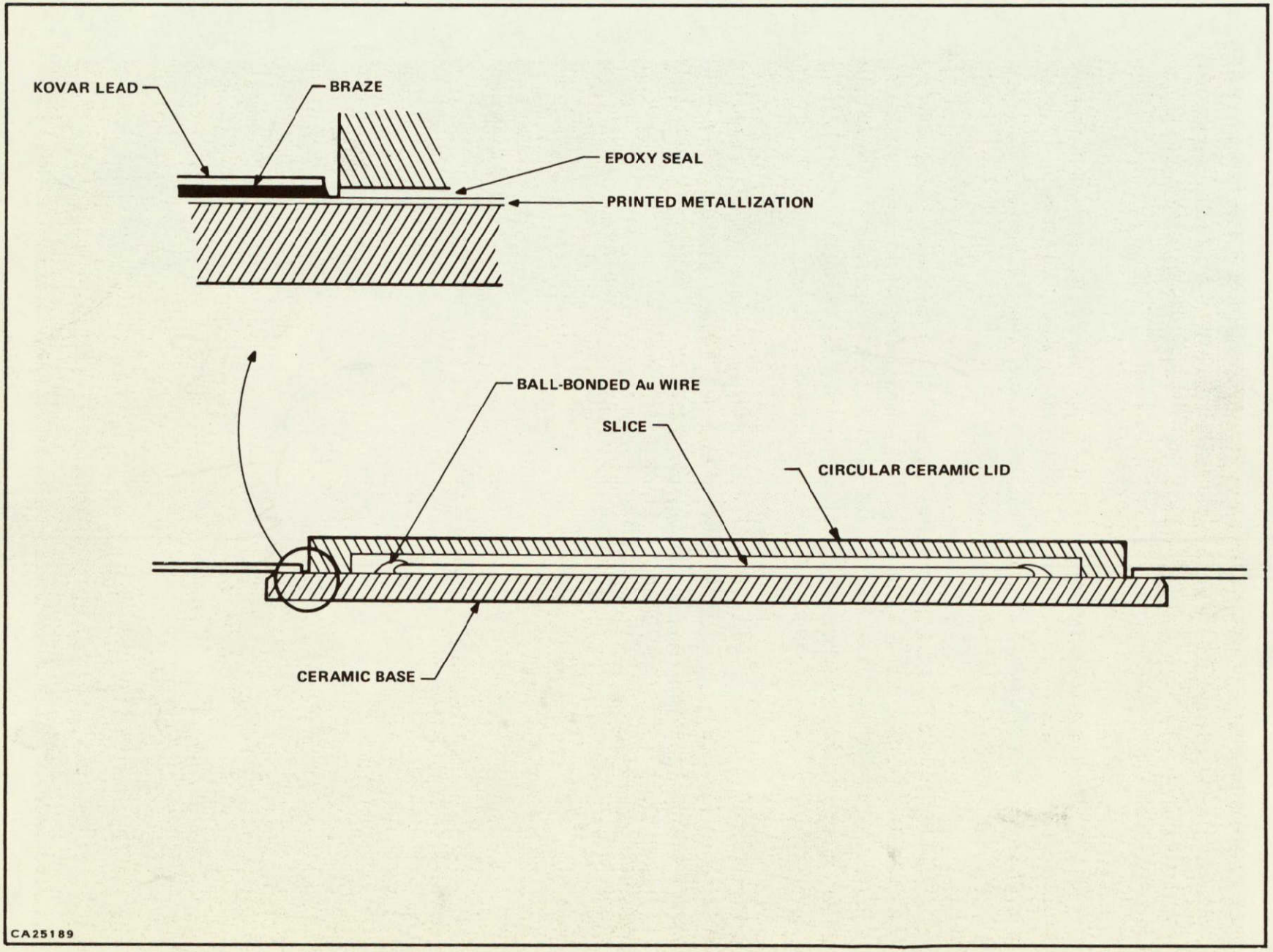

Figure 23. LSI Package Construction (Ceramic-Lid Type)

To give the ceramic base greater mechanical strength and more protection from leakage caused by cracks or interconnecting pores, its thickness was increased from 30 to 40 mils. The package base was also increased from 2.00 to 2.12 inches square in order to provide adequate length on which to braze the lead frames.

Leads for the current packages are silk-screened, high-temperature metallization on the ceramic and gold-plated Kovar for the lead frame. The metallization is nickel-plated molybdenum-manganese, which is then gold plated. The leads are arranged symmetrically around the central cavity for the 156-lead header (see Figure 24).

Different lid configurations have been developed to meet the varying demands imposed by the change in the header design. Two Kovar lid designs are being evaluated for the hermetically-sealed package. One lid is 4-mils thick. The other lid is a wafer 4-mils thick on the edges and 15-mils thick at the center (see Figure 22). Tests are being conducted to determine if the more flexible thin lid or the structurally stronger coined lid will best meet the requirements of the LSI package.

The capability now exists to package LSI devices in either non-hermetic or hermetically sealed packages. The package designs are for 78 or 156 external leads, (shown in Figure 25) depending upon the input-output requirements of the LSI slice.

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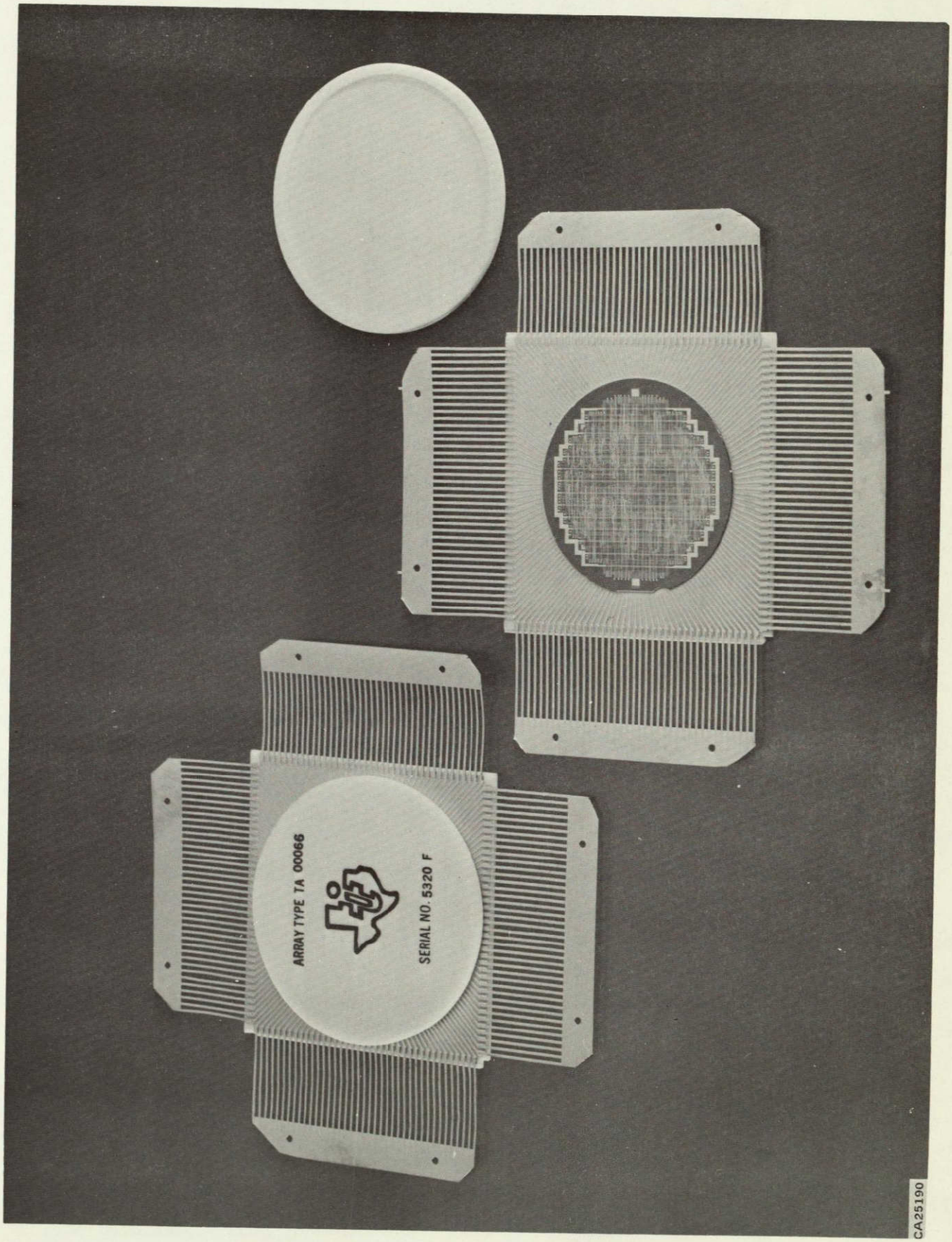

Figure 24. Flat Ceramic Packages (Shown sealed and with mounted slice)

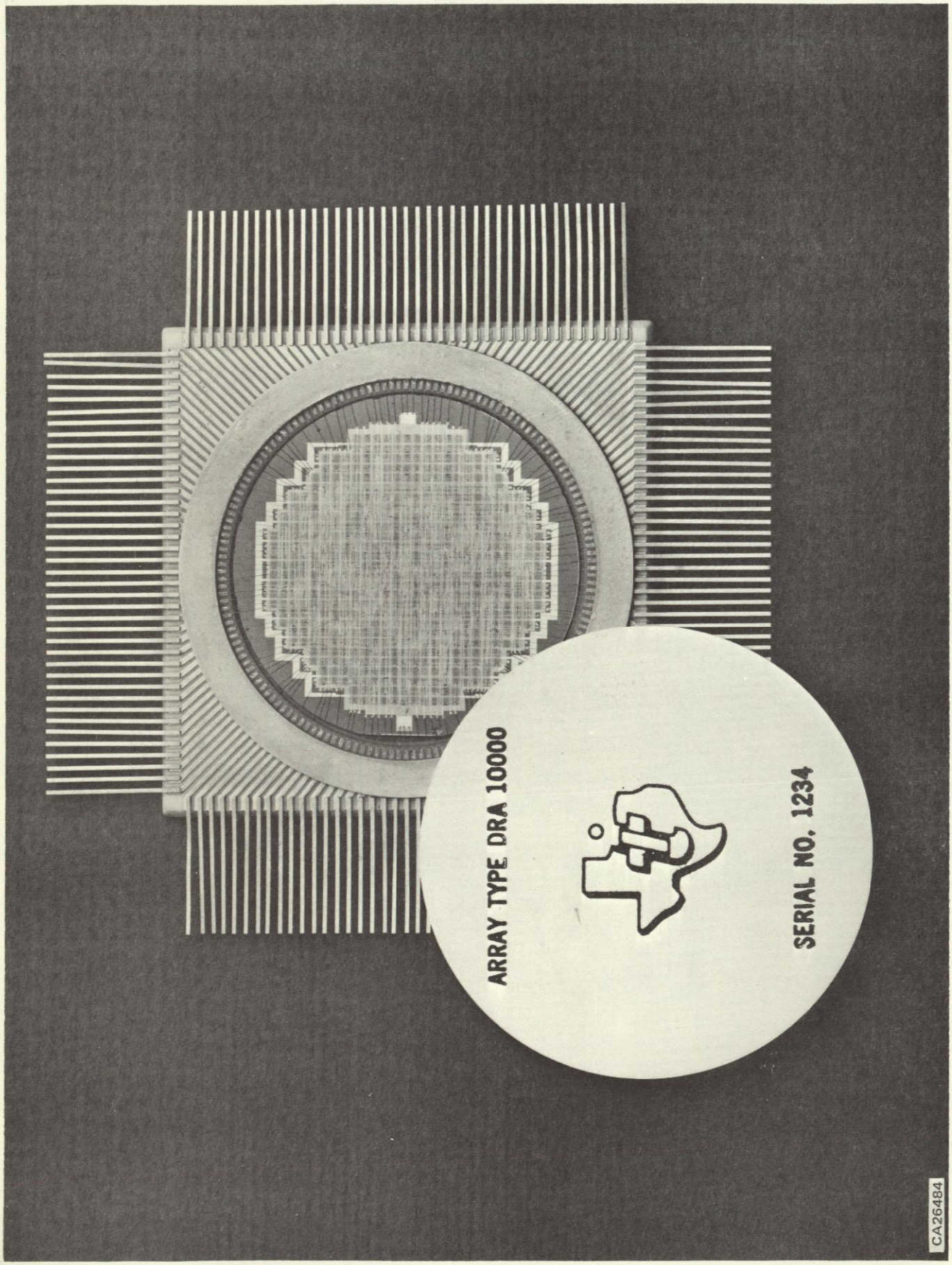

Figure 25. Hermetic Package with Kovar Lid