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DESIGN EVALUATION OF DISTRIBUTED SATURATION CHARACTERISTICS IN INTEGRATED DEVICES

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16. Abstract

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SUMMARY

To evaluate the characteristics of an integrated circuit transistor operating in the saturated mode, it is necessary to determine the parameters for the distributed model. In addition, the lateral currents in the base and collector regions cause corresponding variations in the junction potentials. Formulas are given for the series collector resistance, and it is shown that normalized "A" parameters can be measured and will be constant for a given impurity profile. The difference equations are solved with the aid of a computer. The solutions give not only the terminal saturation characteristics but also the internal current densities. Comparison of experimental values of the saturation characteristics with theory shows excellent agreement.

INTRODUCTION

A previous investigation (refs. 1,2) presented new approaches to model distributed saturation resistance in integrated devices and to develop a method for calculating the saturation voltage, specifically:

(1) The transistor is separated into five distinct regions.

(2) A distributed model is developed for each region which includes the effect of the base resistance and collector resistance.

(3) A method for accurately calculating the value of these resistances using conformal mapping is given.

This investigation will examine the validity and limitation of these modelling procedures, specifically:

(1) The model parameters are determined from the geometry of the integrated device.

(2) A specific integrated circuit transistor is analyzed numerically.

(3) Experimental results are compared, with computer-aided design calculations.

Finally, the use of these techniques and models in the design of integrated circuits is discussed in the light of current manufacturing experience and current laboratory prototypes now under development.

DETERMINATION OF THE MODEL PARAMETERS

One of the requirements of a useful transistor design model is that the relationship between the parameters and the geometry of the transistor being modeled can be determined by calculation or measurement. The model developed above has this desirable property. (Symbols used are defined in the Appendix.)

Expressions for the A(e,c) parameters for drift transistors have been developed by Narud and Myer (ref. 3) and Callahan (ref. 4). The dc expression for A_{cc} is:

$$\frac{A_{cc}}{A_e} = \frac{D_q P_{no}}{W} \left[1 + \frac{W^2}{2 L_\rho^2} + \frac{\ln K}{2} \right] \qquad (1)$$

where K accounts for the field and is the ratio of the base majority carriers at the emitter junction to the base majority carriers at the collector junction. A_e is the emitter area, and the other parameters have the standard notation (ref. 1).

The expressions for the other A(e,c) parameters and current gains are similar and involve the same terms (ref. 3).

It is difficult to calculate the A(e,c) parameters with accuracy, mostly because of the unknown lifetime involved in L_p. However, the A(e,c) parameters per unit area may be accurately measured. Such measurements must be made at low current densities where the effects of the lateral current flow are negligible.

Fortunately, it is a common practice for semiconductor manufacturers to use relatively few different impurity profiles. An impurity profile defines the collector material and base and emitter diffusions. Generally, each manufacturer uses one standard inpurity profile to fabricate most saturating logic circuits. If the A(e,c) parameters (normalized with respect to area) are measured for this standard impurity profile, the necessary A(e,c) parameter information is availalbe and the model may be used to predict $V_{ce(sat)}$ for various transistor geometries.

General curves for the calculation of R_{sc} are given in Figures 1 and 2, and a table of useful approximations is given in Table I. This table is adapted for resistance calculation from a similar table by Compton and Happ (ref. 5). The original table contained some errors which are corrected here.

TABLE I.- USEFUL APPROXIMATIONS FOR R_{sc}

$A = \frac{\pi L}{4d}$	$D = \frac{\pi m}{2d}$	$\frac{Ul}{U2} = \frac{\tan h\ A}{\tan h\ (A + D)}$	$\frac{K_o(Ul/U2)}{K_o'(Ul/U2}$
$A << D$	$D >> 1$	$\frac{A}{A + D}$	$\frac{\pi}{2\ \ell n\ (4D/A)}$
$A << 1$	$D >> A$	1	$\frac{4}{\pi \ell n\ (2D/A)}$
$A << 1$	$D >> 1$	A	$\frac{\pi}{2 \ell n\ (2/A)}$
$A >> 1$	$D << 1$	1	$\frac{2}{\pi} A + \ell n\ 2 - \frac{1}{2} \ell n (1 - e^{-2D})$
$A >> 1$	$D >> 1$	1	$\frac{2}{\pi} A + 1n\ 2$

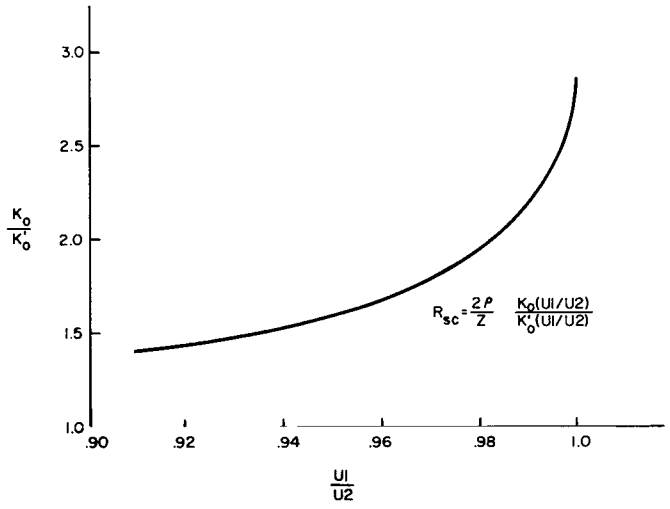


Figure 1.- Series collector resistance R_{sc} as a function of the normalized spreading U_1/U_2

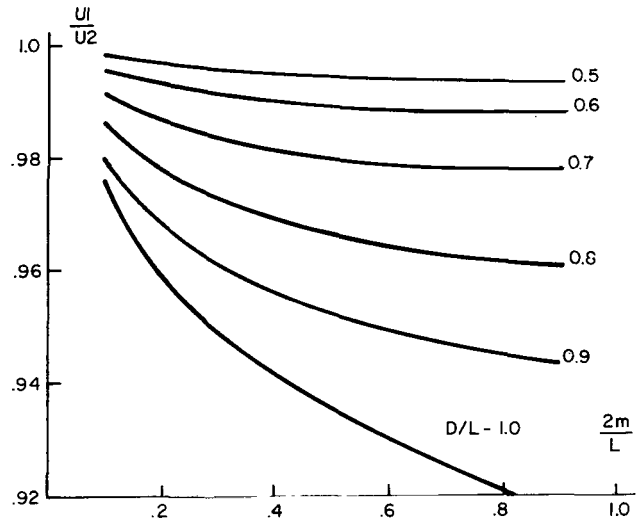


Figure 2.- Series collector resistance R_{SC} as a function of geometry m/L and D/L from

$$\frac{U1}{U2} = \frac{\tan h\ \pi L/4d}{\tan h\ (L/4d + \pi m/2d)}$$

Approximation A>>1 in Table I is accurate to within 1% and leads to the simple equation for the calculation of the series collector resistance:

$$R_{\simeq} = \frac{\rho L}{dz}\left(1 + .88\right) \text{ for } \frac{\pi L}{4d}, \frac{m}{2d} >> 1 \qquad (2)$$

This is the case when the distance between the emitter and collector contact is much greater than the thickness of the N region of the semiconductor material. Approximation 4 in Table I is important when the widths of the emitter and collector contacts become small, and the contact resistance becomes quite large. Rearranging the results of this approximation,

$$R \simeq \frac{\rho}{z}\left[\frac{L}{d} + .88 + \ln f\right] \qquad (3)$$

where $1/f = 1 - \exp(-\pi m/2d)$

The last term in Eq. (3) becomes very large for small contacts, thus the equation predicts the effect of the construction or contact resistance. Equations (2) and (3), then, give a straightforward method for calculating the series collector resistance in terms of the device geometry for the two specific cases.

THE BASE RESISTANCE, R_B

The sheet resistance (average resistivity divided by the width of layer) for thin diffused layers of silicon has been calculated by Irwin (ref. 6), and his results are widely used

by most semiconductor manufacturers. Using these results, the sheet resistance (ρ_{sb}) of the base in Region I may be calculated. Then, the value of R_B for each section in Region I is simply:

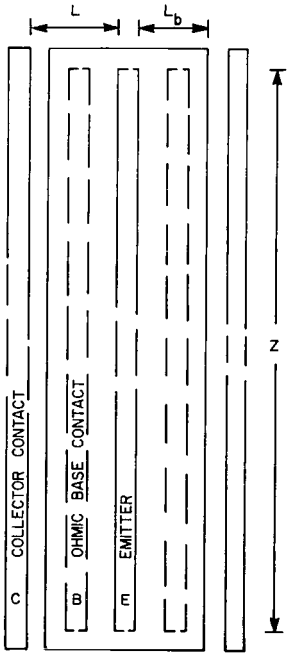
$$R_B = \rho_{sb} \frac{m/2}{Z}$$

where m is emitter width, n is the number of section, and Z is the emitter length. The base resistance in Region II, R_{B_1}, can be calculated using the formulas developed for R and image techniques. An average resistivity, $\bar{\rho}$, must be used. Its value is found by multiplying the total base sheet resistance by the base-collector junction depth.

In this section, the methods for finding A(e,c) parameters, R_B, R_{B_1}, and R_{sc} have been discussed. With this information available, the model may be used to calculate the $V_{ce(sat)}$ for an integrated circuit transistor.

A NUMERICAL EXAMPLE

The saturation characteristics of the transistor, with dimensions given in Figure 3, will be evaluated from theory and compared with corresponding experimental results. Table II gives a summary of the measured A(e,c) parameters, alphas, and the calculated resistance.



L = .40 mils

L_b = .30 mils

Z = 3 mils

Figure 3.- Scale drawing of the integrated circuit transistor

C=Collector contact

B=Ohmic base contact

E=Emitter contact

TABLE II.- NUMERICAL VALUES OF PARAMETERS

A_{ee}	=	9.3 S 10^{-17}/mil^2
A_{cc}	=	3.1 X 10^{-17}/mil^2
n	=	.96
I_o	=	.85 intrinsic - Region I
R_{sc}	=	14 ohms total
R_{sc}	=	.07 ohms/section in Region I
R_{sc}	=	.49 ohms/section in external regions
R_B	=	4.17 ohms/section in Region I
R_B	=	1.75 ohms/section in external regions

From these values in Table II, the following can be observed:

1) Although A_{ee} is larger than A_{cc}, the effective A_{ee} is less than the effective A_{cc}, because of area considerations.

   The effective values are:

$$A_{ee} = 3 \text{ X } 10^{-17}/\text{mil}^2$$

$$A_{cc} = 7 \text{ X } 10^{-17}/\text{mil}^2$$

2) The emitter base forward bias potential, V_e, is larger than the collector forward bias potential, V_c, at the same current level.

The resistors are given in ohms per section and the intrinsic Region I of the model in Figure 4 will be divided into 20 sections. The value of R_{sc} for each section is found by taking the ratio of the length of one section under the emitter to the total length between the emitter and collector contacts and multiplying this ratio times R_c total. This procedure essentially linearizes R_{sc} and appears to be in conflict with its method of calculation. However, as will be shown later, the results from this approximation are fairly

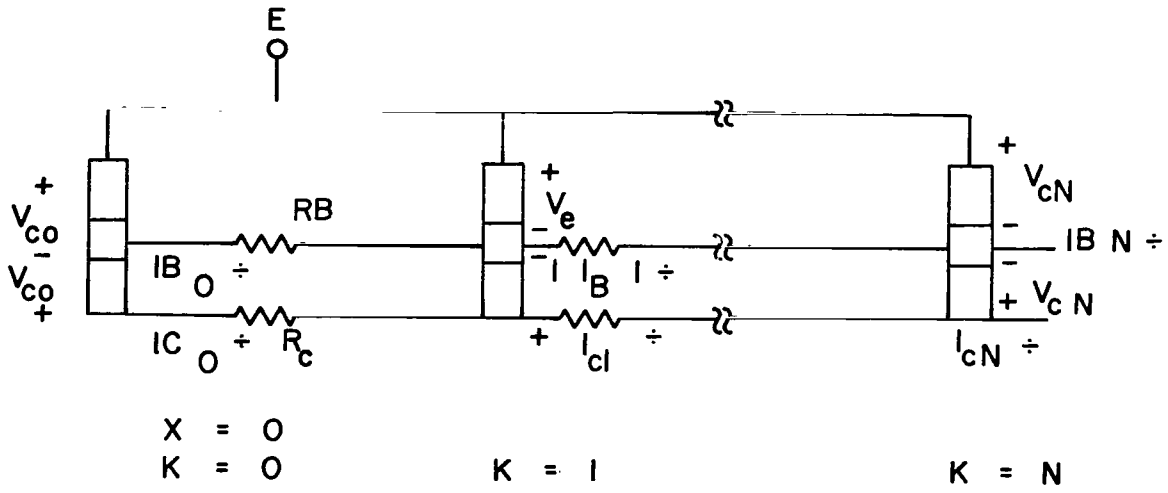


Figure 4.- Distributed model of region I - the intrinsic region

accurate. Dividing the extrinsic regions into 20 sections gives considerably larger values per section than in Region I, due to the larger sections. The same procedures have been followed in the base regions.

COMPUTER EVALUATION - STRATEGY

To gain insight into the operation of the integrated circuit transistor in saturation, the base and collector currents, as well as corresponding voltages, are calculated for each of the forty sections of the model. A high-current (IC = 40 ma) example and a low-current (I_C = 3 ma) example were examined.

Collector Voltage and Injected Current, JC

Figure 5 shows the forward biased collector voltage V_C as a function of the lateral distance from the center of the transistor. For convenience, the cross-section of the transistor is reproduced at the top of the figure. To fully understand the results of Figure 5, one should re-examine the dimensions of the transistor given in the top view (Figure 3). In the high-current mode, the differences in slope are evident, and the collector base junction is more heavily forward biased underneath the emitter and less forward biased at the edge of the base than is the same junction for the low current case. The importance of this gradient in the collector bias is best appreciated if one realizes that for a change of 18 millivolts, the current density, J_C, injected across the junction is reduced by one half. Then, the current being injected by the collector diode at X = .05 is more than two orders of magnitude greater than the current through the diode of X = .40 for the high-current case.

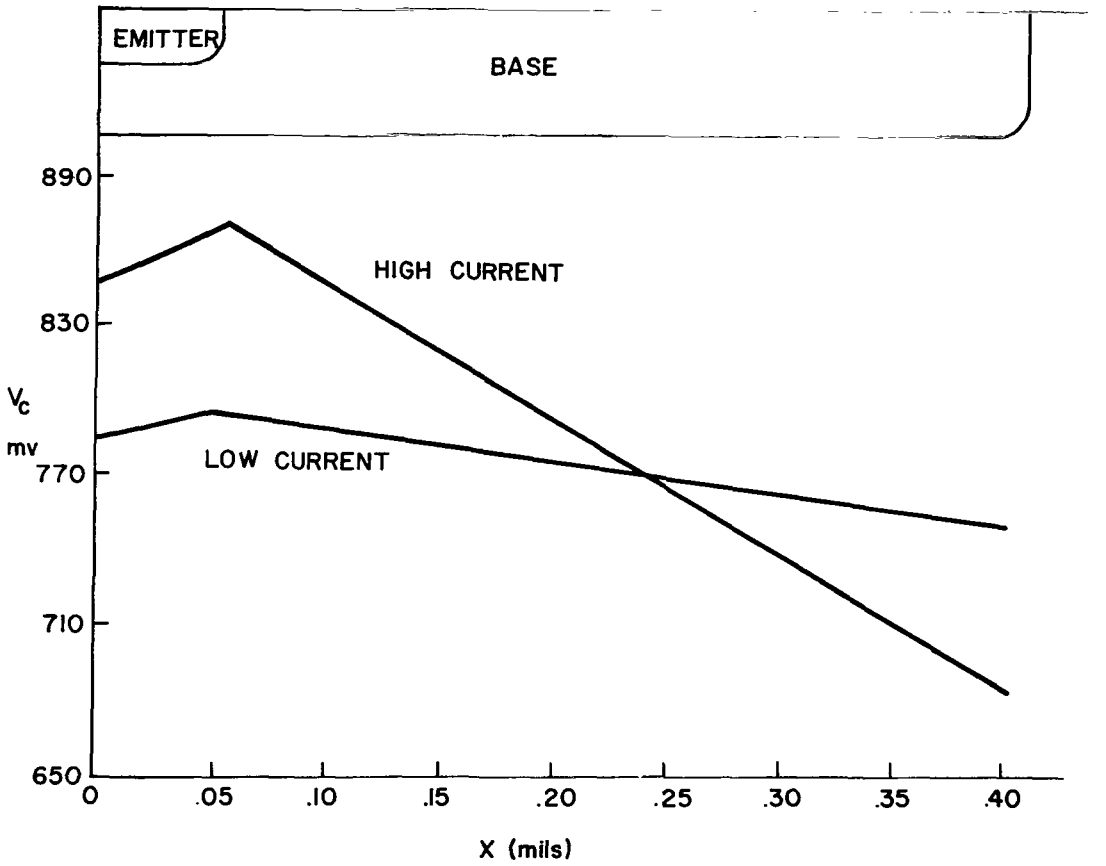


Figure 5.- Computer evaluation of the collector base forward bias potential as a function of distance

The plot of J_C, shown in Figure 6, illustrates this fact. Clearly, the assumption that very little current is flowing in the base to the right of the base contact is a valid assumption for the high-current case. In the low-current case, the lateral current effects are less promounced, but the same trends hold. It is interesting to note that the diode at X = .40 is injecting more heavily for the low-current case than the high-current case. This is a result which would not be predicted by the classical models.

Lateral Collector and Base Currents

The total collector current (I_C) flowing laterally in each section of the transistor (Figure 7) increases rapidly in the intrinsic region underneath the emitter and diminishes in the extrinsic base regions. The total base current flowing in each section of the model (Figure 8) also increases rapidly in Region I underneath the emitter, but continues to increase in the extrinsic regions. In fact, most of the base current originates in the extrinsic regions, and hence, comes from the collector.

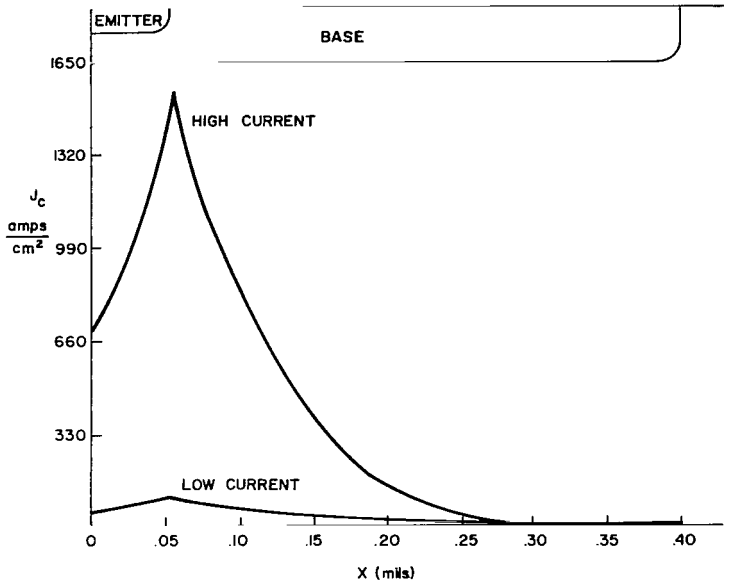


Figure 6.- Computer evaluation of the current injected from the collector into the base as a function of distance

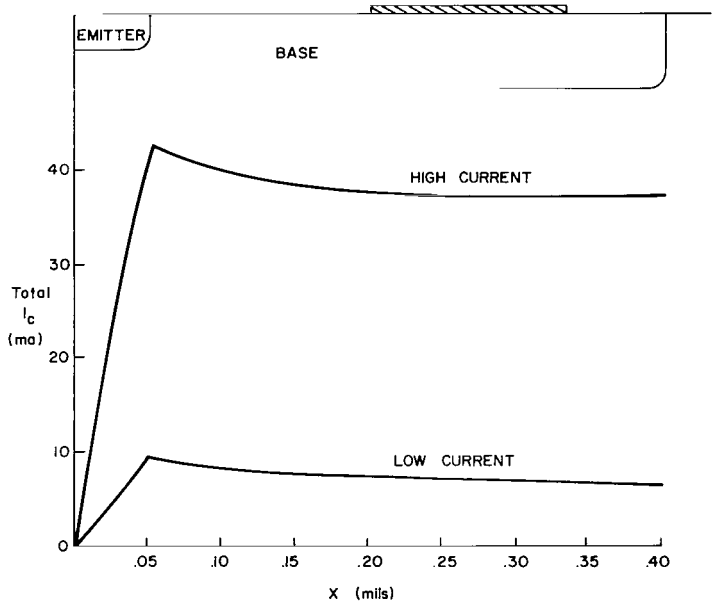


Figure 7.- Computer evaluation of the total collector current flowing laterally as a function of distance

Emmiter Current Density, J_e and V_{be}

Hausser (ref. 7) has shown that J_e is a function of the lateral distance (X) for the intrinsic region in the active mode. Figure 9 shows the variation of J_e for an integrated circuit transistor in the saturated mode. These results were obtained from the model consisting of 20 sections for the intrinsic region. The crowding effect or the change of current density with lateral distance is due to the potential

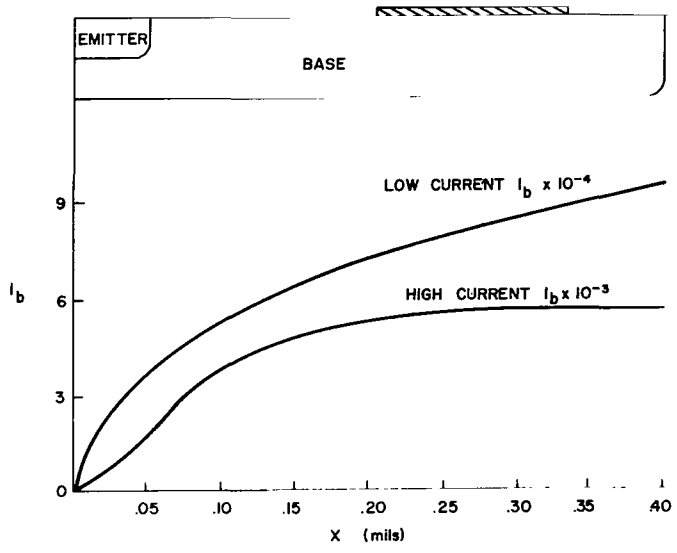


Figure 8.- Computer evaluation of the total base current as a function of distance

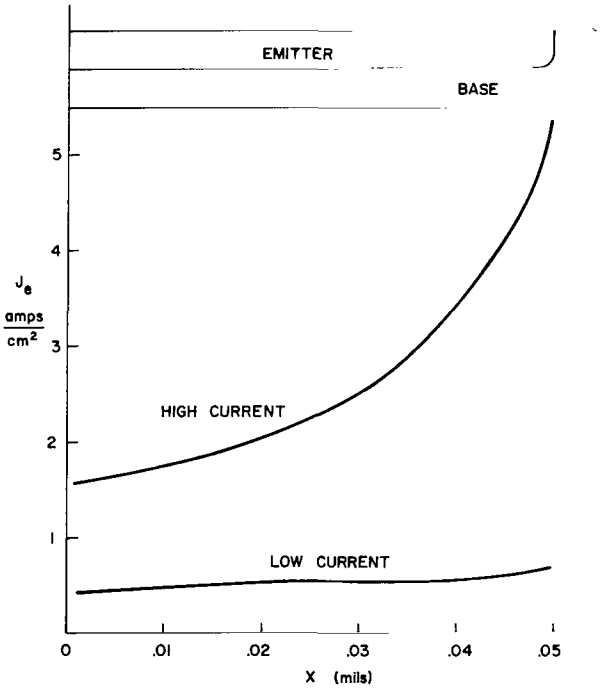


Figure 9.- Computer evaluation of the injected emitter current as a function of distance for region I

drop of the lateral base current flow, and is much more pronounced at high currents. Figure 10 gives the variation of the base to emitter voltage in the intrinsic region. When the I_b total X R_{b1} extrinsic potential change is added to the junction voltage of the last section shown in the figure, the total potential between emitter and base contacts is found. No general curves of V_{be} versus I_e were made, but the results of Figure 10 give a 10-mv agreement with the experimental results.

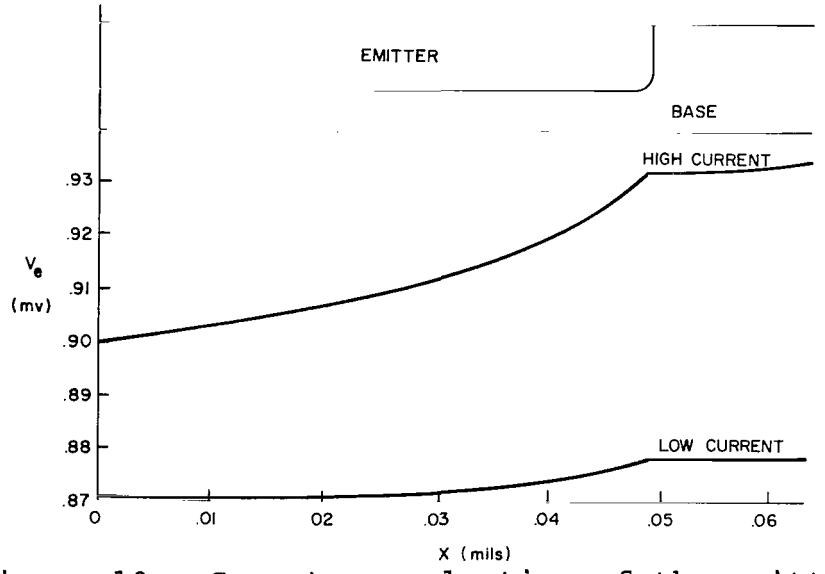


Figure 10.- Computer evaluation of the emitter base potential as a function of distance

α_I Effective

All of the above results deal with currents and voltages inside the transistor rather than the terminal properties; however, as previously stated, these results may be used to calculate α_I effective. The results of the calculations for the transistors at both current levels are given in Table III.

TABLE III.- COMPARISON OF CALCULATED AND EXPERIMENTAL VALUES.

PARAMETER		I_C TOTAL (3.0 ma)	I_C TOTAL (40 ma)
I_{bi}	mamp	.60	3.67
I_{ci}	mamp	.73	5.75
α_I	calculated	0.140	0.360
α_I	experimental	0.148	0.405
%	error	6%	12%

SIGNIFICANCE OF RESULTS

From the examination of these results and Figures 5 and 6, the following significant conclusions can be drawn:

(1) At the high current levels, most of the carrier injection from the collector occurs near the emitter, thus causing a higher alpha inverse.

(2) Differences in the injection level are due to the lateral pinch off of the collector base voltage as shown in Figure 5.

(3) The lateral pinch off at high-current levels causes an increase in the current injected from the collector near the edge of the emitter, and thus, the assumption that only carriers injected in the intrinsic region will be collected becomes less valid.

(4) Because of the results of C, α_{Ieff} will be somewhat larger at high current densities than the model predicts.

$V_{ce(sat)}$

The experimental values of several transistors of $V_{ce(sat)}$ are given by the curve of Figure 11. For collector currents of 3 milliamps, the model predicts the saturation voltage within 5 millivolts, and for collector currents of 40 ma, the agreement is within 25 millivolts with the exception of the measurements for low base currents. Both results are surprisingly accurate, but more important the general shape of the curves is in agreement with theory. As the base current is increased with a constant terminal collector current, the collector base junction becomes more heavily forward biased V_C increases and $V_{ce(sat)}$ decreases.

R_{sc}

The series collector resistance as measured on the transistors was 8 ohms. This is the resistance from the two halves of the transistor in parallel and corresponds to a total collector resistance of 16 ohms for the proposed model, computed to a calculated value of 14 ohms. The error is probably due to the fact that R_{sc} was linearized, plus the fact that there is a finite (approximately .5 ohms) resistance in the connections to the integrated circuit transistor.

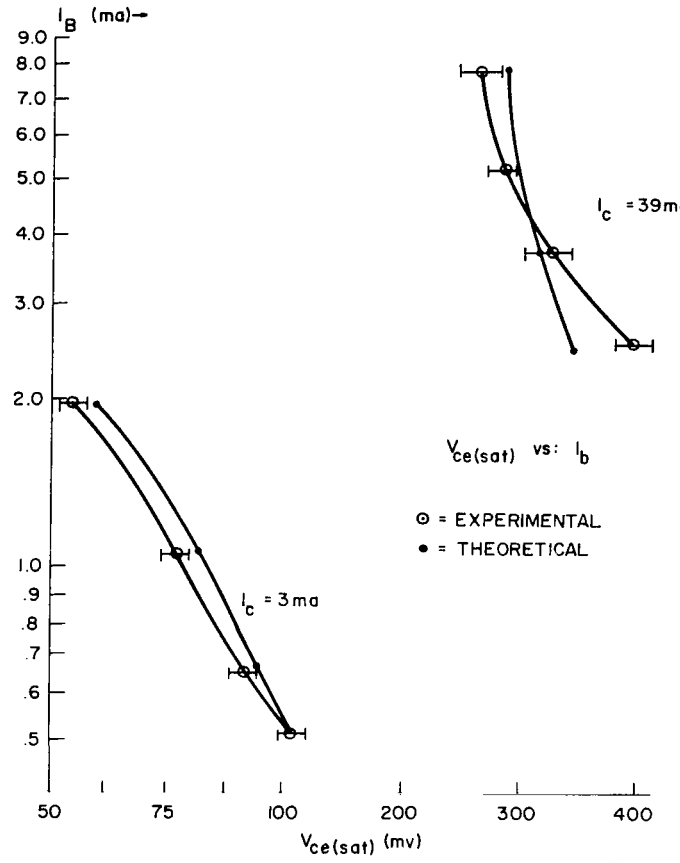


Figure 11.- Comparison of computer evaluation with experimentally determined saturation characteristics

CONCLUSIONS

(1) The proposed model predicts the series collector resistance, the effective alpha inverse, and the saturation voltage for widely separated collector current levels, and just as important, it predicts the various current densities and voltages inside the integrated circuit transistor.

(2) Parameters governing the operation of this transistor model were specified; and it was shown that, although these parameters are difficult to calculate, a set of normalized numerical values may be determined for a given impurity profile used to fabricate a type of integrated circuit. This is an important and favorable result, because semiconductor manufacturers tend to use only a few types of standard impurity profiles to fabricate their circuits and each of these can be characterized.

(3) An illustrative example has been presented for which the proper parameters have been calculated and used in the model.

REFERENCES

1. Happ, W. W. and Dickson, L. B.: Development of a Model for Distributed Saturation Characteristics in Integrated Devices. NASA TN D-5888, Mar., 1970.

2. Dickson, L. B. and Happ, W. W.: A Distributed Model of the Saturation Characteristics of Integrated Circuit Transistors. Convention Record, International Conference of Solid State Circuits, Philadelphia, Pa. Feb., 1967.

3. Narud, J. A. and Meyer, C. S.: Characterization of Integrated Logic Circuits. Proc. IEEE, vol. 52, no. 12, Dec., 1964.

4. Narud, J. A. and Callahan, M. J.: Network Theory for Integrated Circuits. Trans. IEEE on Circuit Theory, vol. CT-11, June, 1964, pp. 312-313.

5. Compton, J. B. and Happ, W. W.: Capacitive Design Considerations for Film-Type and Integrated Circuits. Trans. IEEE on Electron Devices, vol. ED-11, Oct., 1964, pp. 447-455.

6. Irwin, J. C.: Resistivity of Bulk Silicon and of Diffused Layers in Silicon. The Bell System Technical Journal, vol. 41, no. 2, Mar., 1962, pp. 387-410.

7. Hauser, J. R.: The Effects of Distributed Base Potential on Emitter-Current Injection Density and Effective Base Resistance for Stripe Transistor Geometries. Trans. IEEE on Electron Devices, vol. ED-11, May 1964, pp. 237-242.

APPENDIX

Glossary of Terms

A	A basic parameter used to model transistors - defined in Eqs. (1) and (2)
α_n	The common base current gain of a transistor operating in the normal mode, i.e., $\alpha n = Ic/Ie$, V_c = constant
α_I	The common base current gain of a transistor with the collector acting as the emitter, i.e., in the inverse mode
$\varepsilon, \varepsilon_o$	Permitivity
D	Diffusion coefficient of minority carrier in a semiconductor
I_b	Base current
I_c	Collector current
I_e	Emitter current
J	Current density in amps/cm^2
k	Boltzman's constant = 8.63 X 10^{-5} eu/°K
$\frac{kT}{q}$	Reference voltage at 25°C of value - 26 millivolts
K, K_1	The complete elliptic integral of the first kind and its conjugate
K	The field factor in Eq. (12). K is the ratio of the doping in the base at the emitter to that at the collector
K	The general section of the distributed mode 1
L_p	Diffusion length of holes in N-type semiconductors
M	The section immediately under the base contact
N	The section at the edge of the emitter
N_1	The section at the edge of the base-collector junction
P_{no}	The equilibrium concentration of minority carriers in the base of a PNP transistor

q	Electronic charge - 1.6×10^{-19}
R_B	Distributed base resistance under the emitter (in the active region).
R_{B_1}	Distributed base resistance in the external region.
R_{C_1}	The lumped resistance external to the collector-base junction.
R_{sc}	The total series collector resistance
ρ	Resistivity
$V_{ce(sat)}$*	The saturation voltage of an ideal one dimensional transistor with no series resistance
$V_{ce(sat)}$	The saturation voltage
V_e	Emitter-base potential at any point
V_c	Forward biased collector-base potential at any point. The base width of the transistor in the active region.

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