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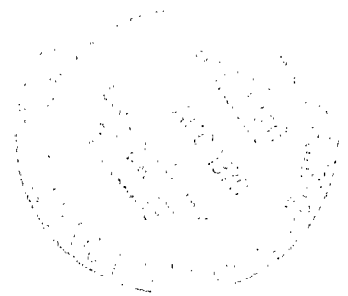


DEVELOPMENT OF A MODEL FOR DISTRIBUTED SATURATION CHARACTERISTICS IN INTEGRATED DEVICES

by W. W. Happ and L. B. Dickson

Electronics Research Center

Cambridge, Mass. 02139





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DEVELOPMENT OF A MODEL FOR DISTRIBUTED SATURATION CHARACTERISTICS IN INTEGRATED DEVICES*

By W. W. Happ
National Aeronautics and Space Administration
Cambridge, Massachusetts
and

L. B. Dickson
Motorola Semiconductor Co.
Scottsdale, Arizona

SUMMARY

The characteristics of an integrated circuit transistor, operating in the saturated mode, cannot be determined from simple lumped parameter relationships. Due to the geometry of these transistors, the series collector resistance must be calculated using conformal mapping techniques.

To accurately determine the saturation characteristics, distributed models are developed for the five regions of the transistor. Using these models as a guide, difference equations describing each region are formulated. Insight into the operation of the transistor can be gained by examining the internal current densities predicted by the model.

INTRODUCTION

The saturation voltage specification is often the most severe specification placed upon an integrated circuit transistor, and many times the ac as well as the dc-voltage performance is limited by this specification. To truly optimize the design of an integrated circuit transistor, a method for calculating the saturation voltage, $V_{ce(sat)}$, is necessary. (All symbols to be used are defined in the Appendix.)

The saturation characteristics of the integrated circuit transistor in Figure 1 depend upon two-dimensional current flow. The following must be considered:

- (1) The effect on the emitter-base potential, V_e , of the lateral current flow in the distributed base resistance.
- (2) The combined effects of lateral current flow in the base and collector regions on the collector base potential, V_c .
- (3) The effect of the planar base and collector contacts on the series base resistance, R_{B1} , and series collector resistance, R_{SC} .

*The work reported here was published in part as an M.S. thesis of L. B. Dickson at Arizona State University.

This investigation considers all of these effects. Previous related investigations by Ebers and Moll (ref. 1), Gosh (ref. 2), and Hauser (ref. 3) have only partially treated this problem. Dr. F. A. Lindholm of the University of Florida and Dr. J. Staudhammer of Arizona State University have significantly contributed ideas and valuable suggestions to this work.

ASSUMPTIONS FOR THE DISTRIBUTED MODEL

A one-dimensional model for the intrinsic transistor has been postulated by Ebers and Moll (ref. 1). This model gives the black-box performance of a three-layer transistor in terms of the junction potentials, terminal currents, and $A(e,c)$ parameters, as defined in Eqs. (1) and (2) in Figure 2, using the terminology defined in the Appendix.

$$I_e = A_{ee} \left[\exp \left(\frac{V_e}{V_t} \right) - 1 \right] - A_{ec} \left[\exp \left(\frac{V_c}{V_t} \right) - 1 \right] \quad (1)$$

$$I_c = A_{ce} \left[\exp \left(\frac{V_e}{V_t} \right) - 1 \right] + A_{cc} \left[\exp \left(\frac{V_c}{V_t} \right) - 1 \right] \quad (2)$$

$$\text{where: } V_t = \frac{kT}{q}$$

The intrinsic saturation voltage, $V_{ce(sat)}^*$, may be obtained from this model by solving Eqs. (1) and (2) for V_e and V_c .

then

$$V_{ce(sat)}^* = V_e - V_c = V_t \ln \left[\frac{1 + I_c/I_b (1 - \alpha_n/\alpha_n) (1 - \alpha_I)}{\alpha_I (1 - I_c/I_b) (1 - \alpha_n/\alpha_n)} \right] \quad (3)$$

$V_{ce(sat)}^*$ is proportional to $\log \alpha_I$. For small values of α_I , such as those experienced in integrated circuit transistors, $V_{ce(sat)}^*$ is sensitive to changes in α_I .

The expression for $V_{ce(sat)}^*$ neglects the effect of R_{sc} . The standard approximation defining the total saturation voltage

$$V_{ce(sat)} = V_e - V_c + I_c R_{sc} = V_{ce(sat)}^* + I_c R_{sc} \quad (4)$$

is valid only for conventional transistors with one-dimensional flow.

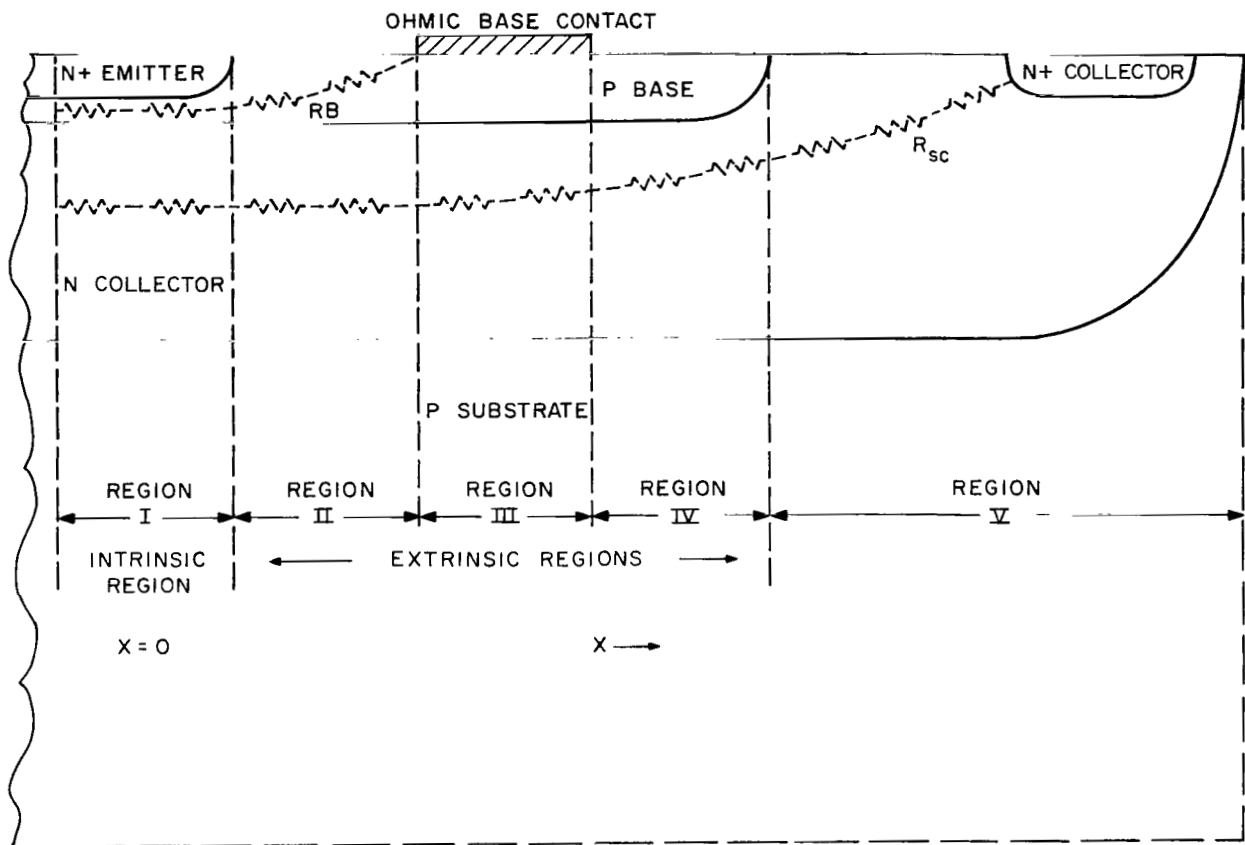


Figure 1.- Cross section of one half of an integrated circuit transistor showing the structure, distributed resistances, basic regions, and X axis

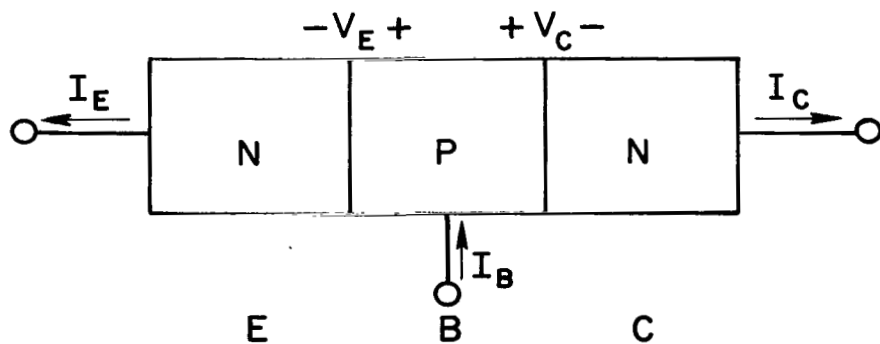


Figure 2.- Currents and voltages for the Ebers and Moll model

The lateral flow of collector and base currents in integrated circuit transistors prevents the separation of the terms in such a simple manner, and for such a transistor, V_c , V_e , $V_{ce(sat)}$, and α_I are functions of R_{sc} and the base resistance, R_b . In fact, V_c and V_e become functions of the lateral distance in Figure 1 and cannot be treated as constant across the transistor (refs. 2, 3).

To examine the operation of the transistor under such conditions, a distributed model with one-dimensional transistors interconnected with appropriate resistors is developed.

Gosh (ref. 2) developed a similar model for operation in the active mode, but did not apply it to saturated mode of operation, and, thus, did not include the effect of R_{sc} .

It is assumed that the transistors to be modeled in this manner will be gold diffused to improve their switching performance. This technique essentially eliminates the active parasitics created by the substrate-collector junction of an integrated circuit transistor (ref. 4). Therefore, the effect of this junction is simply to constrain the collector current. This constraint will be considered in the calculation of R_{sc} and accurate results may be obtained.

DEVELOPMENT OF THE DISTRIBUTED MODEL

The transistor shown in Figure 1 may be divided into five regions:

- Region I: The intrinsic region consisting of the cross section which includes the emitter
- Region II: The area between the emitter and base contact
- Region III: The equipotential base contact region
- Region IV: The region between the edge of the base and the base contact
- Region V: The region between the base and collector contact

Regions II, III, and IV will be referred to as the extrinsic regions. Each section of the intrinsic region (Region I), represents a classical one-dimensional transistor with the emitter area equal to the collector area. The sections in the extrinsic regions are collector base diodes. In Region III, the effective base resistance is zero because of the ohmic contact, and in Region IV the base resistance

is assumed to be zero for simplicity. The validity of this approximation is discussed later.

Figure 3 shows the distributed model for all regions of the transistor. Using this figure as a guide, $V_{ce(sat)}$ may be found by summing the terminal voltages.

$$V_{ce(sat)} = V_{en} + V_b - V_{cn1} + V_{1c} \quad (5)$$

where the above voltages are functions of the terminal currents and the "A" parameters of each region. Closer examination shows that the voltages in Eq. (5) are also strong functions of the lateral collector and base currents; therefore, $V_{ce(sat)}$ determined from Eq. (5) will be accurate for "top collector" transistors.

The values of the voltages in Eq. (5) can be found by writing difference equations rather than differential equations using the distributed model as a guide. For Region I (Figure 4), the current relationships are given by:

$$I_{bo} = (1 - \alpha_n) A_{ee} \left(\exp \frac{V_{eo}}{V_t} \right) + (1 - \alpha_I) A_{cc} \left[\exp \left(\frac{V_{co}}{V_t} \right) - 1 \right] \quad (6)$$

$$I_{co} = \alpha_n A_{ee} \left[\exp \left(\frac{V_{eo}}{V_t} \right) \right] - A_{cc} \left[\exp \left(\frac{V_{co}}{V_t} \right) - 1 \right] \quad (7)$$

$$\text{that is: } I_{bo} = f_1 (V_e, V_c)$$

$$\text{and } I_{co} = f_2 (V_e, V_c)$$

$$V_{e1} = V_{eo} + I_{bo} R_b \quad (8)$$

$$V_{c1} = V_{co} + I_{bo} R_b - I_{co} R_c \quad (9)$$

Subscripts 0 and 1 refer to the initial and first region of the model shown in Figure 4. Typically, the change in voltage from one section to another is in the order of few millivolts, but because the currents are exponential functions of these voltages, this change in voltage is important.

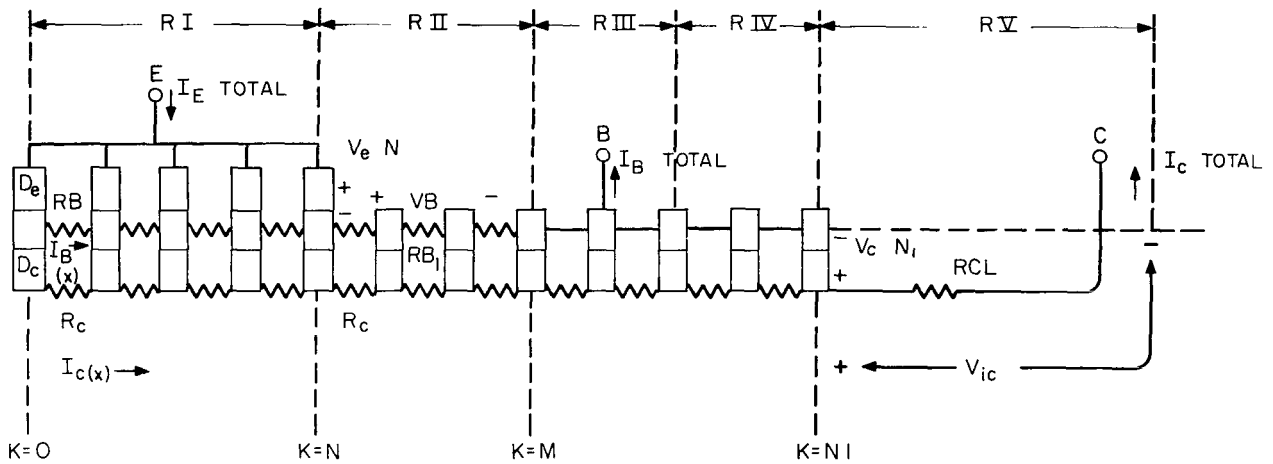


Figure 3.- Distributed model of integrated circuit transistor defining voltages that make up $V_{ce(sat)}$, limits to summations (N , M , and N_1) and currents

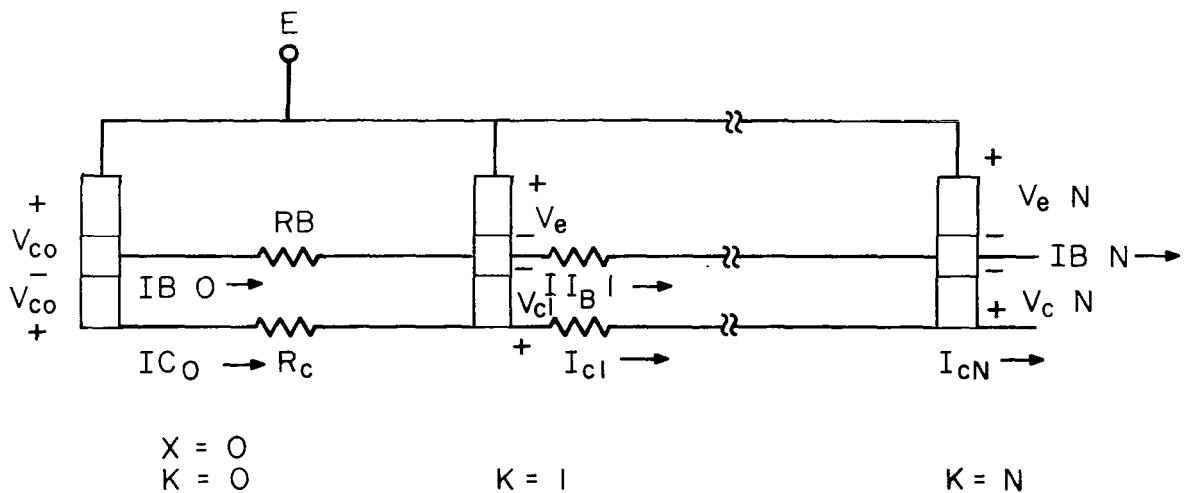


Figure 4.- Distributed model of region I - the intrinsic region

The equations for the nth section in Region I are:

$$\begin{aligned}
 I_{bn} &= \sum_{k=0}^n I_{bk} = \sum_{k=0}^n (1 - \alpha_n) A_{ee} \exp\left(\frac{V_{ek}}{V_t}\right) \\
 &= (1 - \alpha_I) A_{ec} \left[\exp\left(\frac{V_{ek}}{V_t}\right) - 1 \right]
 \end{aligned} \tag{10}$$

$$\begin{aligned}
 I_{cn} &= \sum_{k=0}^n I_{ck} = \sum_{k=0}^n \alpha_n A_{ee} \exp\left(\frac{V_{ek}}{V_t}\right) \\
 &= A_{cc} \left[\exp\left(\frac{V_{ck}}{V_t}\right) - 1 \right]
 \end{aligned} \tag{11}$$

with

$$V_e(k+1) = V_{ek} + I_{bk} R_B \tag{12}$$

$$V_c(k+1) = V_{ck} + I_{bk} R_B - I_{ck} R_C \tag{13}$$

then, V_{eN} , V_{cN} , I_{bN} , and I_{cN} can be found by setting $n = N$

The equations governing the performance in Region II are:

$$I_{bn} = I_{bN} + \sum_{k=N+1}^n A_{cc} \left[\exp\left(\frac{V_{ck}}{V_t}\right) - 1 \right] \tag{14}$$

$$I_{cn} = I_{cN} - \sum_{k=N+1}^n A_{cc} \left[\exp\left(\frac{V_{ck}}{V_t}\right) - 1 \right] \tag{15}$$

$$V_c(K+1) = V_{ck} + I_{bk} R_{b1} - I_{ck} R_C \tag{16}$$

The equations governing Regions III and IV are identical to those for Region II with $R_{b1} = 0$.

With the equations written above, the necessary voltages to find $V_{ce(sat)}$ are available.

Then

$$V_{eN} = V_{eo} + \sum_{k=1}^N I_{bk} R_B, \quad (17)$$

$$V_b = \sum_{k=N+1}^M I_{bk} R_{B1}, \quad (18)$$

and

$$\begin{aligned} V_{cN1} = V_{co} + \sum_{k=0}^N I_{bk} R_B + \sum_{k=N+L}^M I_{bk} R_{B1} \\ - \sum_{k=0}^{N1} I_{ck} R_c \end{aligned} \quad (19)$$

Substituting Eqs. (17), (18), and (19) into Eq. (5):

$$V_{ce(sat)} = V_{eo} - V_{co} + \sum_{k=0}^{N1} I_{ck} R_c + I_{cN1} R_{c1} \quad (20)$$

The terminal base and collector currents are evaluated at $n = N_1$ and similar equations can be written for them.

With the results from the above equations, the necessary currents and voltages are given in terms of V_{co} and V_{eo} and the $A(e,c)$ parameters. With a judicious choice of V_{co} and V_{eo} and the use of a computer, $V_{ce(sat)}$ can be calculated for any desired terminal current.

THE EFFECTIVE INVERSE CURRENT GAIN

The effective α_I of an integrated circuit transistor is a function of the lateral position of the current being injected from the collector into the base. Figure 1 shows the collector junction is much larger than the emitter junction, and current injected long distances away from the emitter will not contribute to the inverse emitter current and thus reduce α_I .

Assuming an inverse current gain, α_{I0} , for Region I and an inverse current gain of zero for the extrinsic regions,

then the results of the previous section can be used to calculate the effective α_I . If I_{bi} is defined as the total base current which originates in the collector and I_{ci} as the total current injected out of the collector, the alpha effective inverse is given by:

$$\alpha_{Ieff} = (1 - \frac{I_{bi}}{I_{ci}}) \quad (21)$$

where I_{ci} is given by:

$$I_{ci} = \sum_0^{N_1} A_{cc} \exp \frac{V_c}{V_t} \quad (22)$$

where the summation extends over all regions of the transistors, and

$$\begin{aligned} I_{bi} = & \sum_k^N (1 - \alpha_{I \text{ intrinsic}}) A_{cc} \exp \left(\frac{V_c}{V_t} \right) \\ & + \sum_{k=N_1+1}^{N_2} A_{cc} \exp \left(\frac{V_c}{V_t} \right) \end{aligned} \quad (23)$$

THE SERIES COLLECTOR RESISTANCE

The series collector resistance, R_{sc} , may be approximated to be the resistance between two conducting planes as shown in Figure 5b, with one contact representing the collector N+ diffusion and the other the emitter diffusion (Figure 5a). Assuming charge neutrality (i.e., $\nabla^2 \rho = 0$) in the collector area, mapping techniques (Eqs. (5), (6), and (7)) may be used to find the capacitance for this geometry:

$$C = \frac{1}{2} \epsilon \epsilon_0 Z \frac{K_1(U_1/U_2)}{K(U_1/U_2)} \quad (24)$$

$$\text{where } U_1 = \frac{\pi}{2d} \tanh \frac{\pi L}{4d} \quad (25)$$

$$\text{and } U_2 = \frac{\pi}{2d} \tanh \left(\frac{\pi L}{4d} + \frac{\pi m}{2d} \right) \quad (26)$$

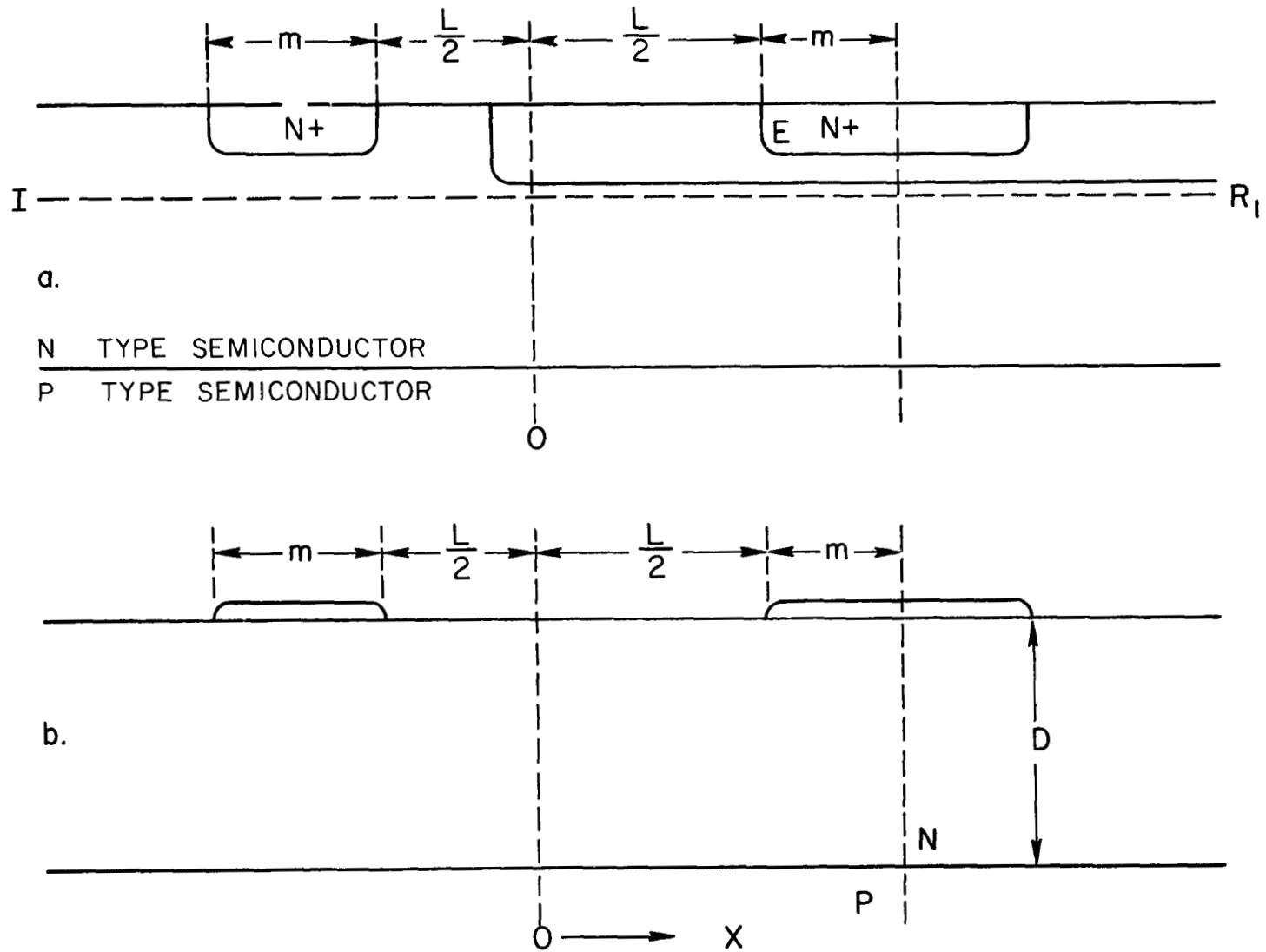


Figure 5.- Shows the similarity of the cross-section of the integrated circuit transistor (Part a) to the geometry, which was conformally mapped by Kaiser and Castro

and Z in the length of the stripe perpendicular to the directions shown. K and K' are the complete elliptic integral of the first kind of its conjugate respectively; i.e.:

$$K' \left(\frac{U_1}{U_2} \right) = K \left[1 - \left(\frac{U_1}{U_2} \right)^2 \right]^{1/2} \quad (27)$$

Utilizing the analogy between capacitance and resistance, $RC = \rho \epsilon \epsilon_0$, Smythe (ref. 8), where R and C are the lumped equivalent resistance and capacitance, respectively, and ρ and $\epsilon \epsilon_0$ are the distributed resistivity and permittivity of the material, these results can be used to calculate the series resistance for an integrated circuit transistor. The series collector resistance for a transistor with emitter length Z is:

$$R_{sc} = \frac{\rho \epsilon \epsilon_0}{C} = \frac{2\rho}{Z} \times \frac{K \left(U_1/U_2 \right)}{K_1 \left(U_1/U_2 \right)} \quad (28)$$

The analysis has been two dimensional, but for most transistors of interest, Z is $\gg L, d$ and the end effects can be neglected. If Eq. (28) is used when $Z = L$, worst-case value results.

LIMITATIONS OF THE MODEL

The model is accurate for low current ranges, but has anticipated limitations at high current levels. Important factors not included in the model which affect the results at high current levels are:

- (1) At high current levels, α will decrease because of the electronic junction motion which increases the base width, (refs. 9, 10), and, thus, reduces the base transport factor and the emitter efficiency. For large currents, conductivity modulation also reduces the emitter efficiency, and the net result is that, at high current levels, α will decrease rapidly.
- (2) The resistivity and associated resistances for the base and collector regions are inversely related to the majority carrier concentrations in these regions. At high current densities, the number of majority carriers is radically increased to maintain charge

neutrality, and the resistivity and the values of the resistances are reduced.

- (3) A third limitation to this model results from the linearization of the series collector resistance.

It was shown that this resistance is effected by the crowding of the current near the collector contact and emitter, and the method for accurately calculating the resistance is given especially for high currents. The value of collector resistance used in each section of the model was found by dividing the total R_s by the number of sections. This linearization assumes a constant distributed collector resistance. This assumption introduces a second-order inaccuracy which becomes important at high current levels.

APPLICATIONS OF THE MODEL

The model is a distributed version of the non-linear model proposed by Narud and Meyer (ref. 9) and will accurately predict operation in the active mode. In the active mode, one can predict the emitter current density for a given total emitter current. As was shown by Kirk (ref. 10), the maximum number of carriers passing through the collector-base depletion region must be kept less than the ionized impurity distribution in that region for the transistor to operate.

The number of carriers passing through a region as related to the current density may be determined. This model gives the current density in any region, and thereby, provides a means to ensure that the maximum allowable current density will not be exceeded.

The model may be expanded to give the transient response of an integrated circuit transistor. It would be necessary to include both junction and diffusion capacitances for each section of the model. An analysis based on the model of the collector region would give the storage time of the transistor; however, the relationships are nonlinear and a computer solution would be necessary.

PRINCIPAL CONTRIBUTIONS OF MODEL

The model here proposed, and the techniques developed to utilize it, offer significant aids to the device designer.

- (1) Appropriate formulas were devised for the calculation of the series collector resistance of integrated circuit transistors.

- (2) The expressions for the saturation voltage and effective α_I were developed from a distributed model.
- (3) Perhaps the most important result of this analysis is the insight into the operation of the transistor that has been gained by examining the potentials and currents inside the transistor as a function of lateral distance. This insight aids in the optimization of transistors for a given function.

An experimental verification of the model here developed shows excellent agreement with theory, and has been discussed elsewhere (refs. 11, 12).

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APPENDIX

Glossary of Terms

A	A basic parameter used to model transistors - defined in Eqs. (1) and (2)
α_n	The common base current gain of a transistor operating in the normal mode, i.e., $\alpha_n = I_c/I_e$, $V_c = \text{constant}$
α_I	The common base current gain of a transistor with the collector acting as the emitter, i.e., in the inverse mode.
ϵ, ϵ_0	Permittivity
D	Diffusion coefficient of minority carriers in a semiconductor
I_b	Base current
I_c	Collector current
I_e	Emitter current
J	Current density in amps/cm ²
k	Boltzman's constant = 8.63×10^{-5} eu/°K
$\frac{kT}{q}$	Reference voltage at 25°C of value - 26 millivolts
K, K'	The complete elliptic integral of the first kind and its conjugate
k	General section of distributed model, e.g., Eq. (12)
L_p	Diffusion length of holes in N-type semiconductors
M	The section immediately under the base contact
N	The section at the edge of the emitter
N_1	The section at the edge of the base-collector junction
P_{no}	The equilibrium concentration of minority carriers in the base of a PNP transistor

q	Electronic charge - $1.6 \times 10^{-19} \text{ es}_u$
R_B	Distributed base resistance under the emitter (in the active region)
R_{B1}	Distributed base resistance in the external region
R_{C1}	The lumped resistance external to the collector-base junction
R_{sc}	The total series collector resistance
ρ	Resistivity
$V_{ce(sat)}$	*The saturation voltage of an ideal one dimensional transistor with no series resistance
$V_{ce(sat)}$	The saturation voltage
V_e	Emitter-base potential at any point
V_c	Forward biased collector-base potential at any point,
W	The base width of the transistor in the active region

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