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INTRODUCTION

Personnel of Checkout Systems Branch, who have been involved in Apollo Checkout are presently attempting to identify what a next generation checkout system must consist of to support new manned spaceflight programs. In considering the two most likely missions, the space station/space base and the logistics vehicle or shuttle craft, two things become readily apparent. The space base will require on Onboard Data Management System, as well as a Ground Data Management System of some complexity, and the space shuttle will require some level of ground preparation with possibly an instrumentation philosophy similar to the X-15 experimental craft. Therefore, the primary effort to date has been the definition of the Onboard Data Management System and the Ground Data Management System. During the definition of these two systems, it became apparent that a common interface was lacking for the factory through complete mission type of checkout required. This paper is an attempt to define that interface and concurrently propose a new concept in checkout that substantially reduces the complexity of both systems.

In developing any new concept, it is only natural to reflect on past programs. Some implications gained from reviewing Apollo checkout are that the most critical area of checkout equipment was the spacecraft interface equipment, or the actual

[redacted]

ACE interface to the GSE or spacecraft system. Therefore, it follows that the proper point to approach the checkout problem is at the spacecraft system level. Further investigation raised a very interesting question. Why not build the checkout capability into the spacecraft system itself? With this concept in mind, an effort was launched to determine the feasibility of BIC, or built In Checkout. The remainder of this paper describes the technique of BIC and the advantages gained by utilizing this approach.

BIC, as has been pointed out, is test capability which is designed and built into a spacecraft or GSE system or subsystem and its components to provide a common interface for Ground/Flight/Bench maintenance checkout as required. As shown in Figure 1, BIC consists of a controller and as many cells as necessary to checkout a particular system. The system above the dotted line, called simply the Control Center, may be a Ground, Onboard Data Management System, or some other Control Center. Its communication to the spacecraft system cells is through the controller via a single cable utilizing digital data. Where physical distance makes it feasible, a party line technique using a single cable for several controllers can be utilized. In addition, the controller-to-cell communication may take on this same form, with a substantial savings in cables and weight. For a spacecraft BIC will consist of a family of BIC controllers and a family of BIC cells. Creating families of controllers and cells limits the amount of hardware required, yet provides the flexibility necessary to accommodate a variety of systems components without excessive BIC circuitry.

A typical BIC controller and its grouping of cells is shown in Figure 2. As pointed out, the BIC controller interfaces with some Control Center, and provides sequences to cause stimuli to be generated, measurement points to be accessed and limit checks to be performed by the cells. The controller also accepts code words from the Control Center to set up any of the modes of operation shown in Figure 3. The BIC cell, upon command from the BIC controller, will accept digitized data and compare it to predetermined limits, generate stimuli as commanded by the controller, and provide an interrupt capability to the controller in the event that parameters exceed predetermined limits.

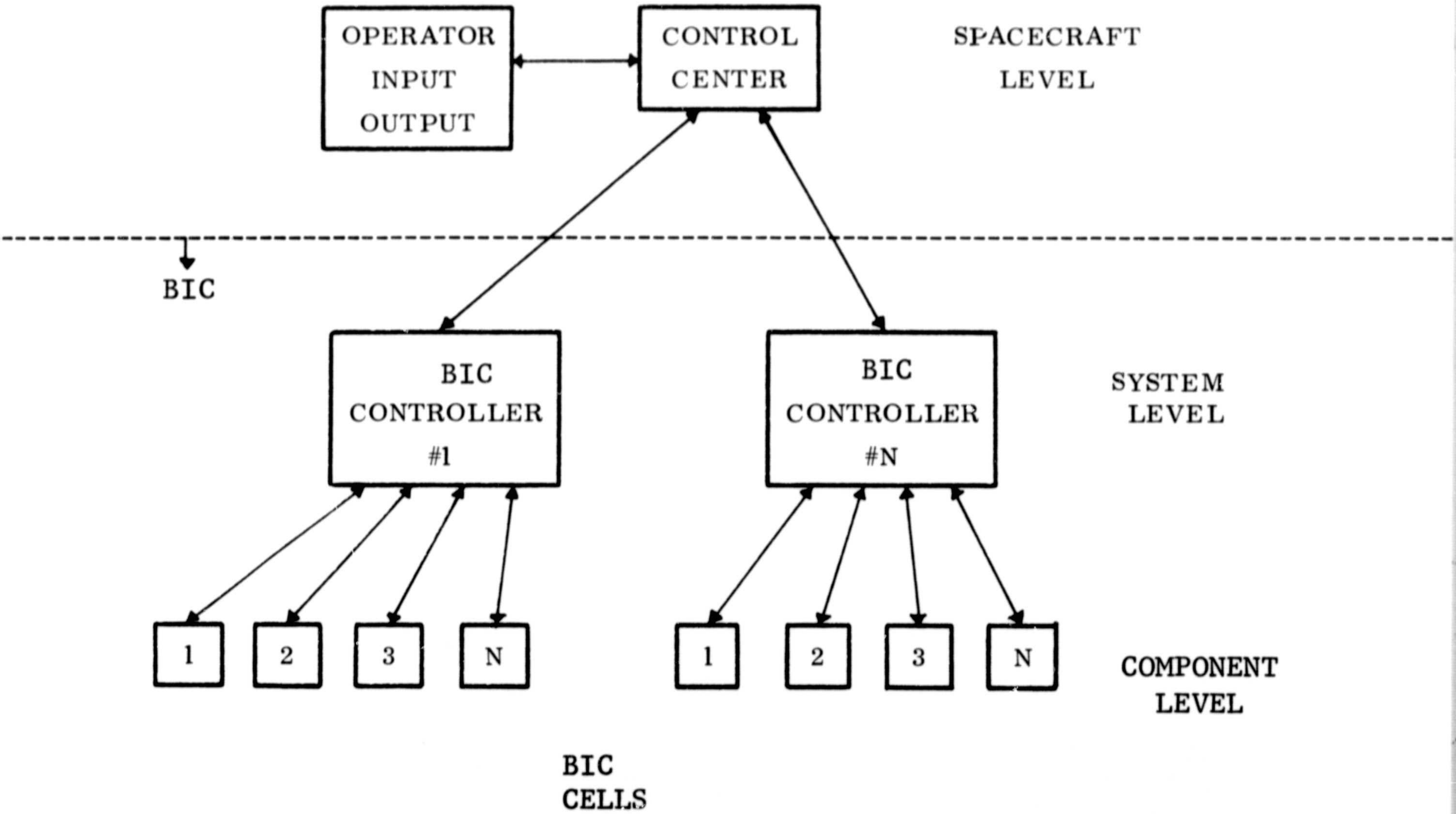

OPERATOR
INPUT
OUTPUT
CONTROL
CENTER
SPACECRAFT
LEVEL
BIC
BIC
CONTROLLER
#1
BIC
CONTROLLER
#N
SYSTEM
LEVEL
1
2
3
N
1
2
3
N
COMPONENT
LEVEL
BIC
CELLS

FIGURE 1

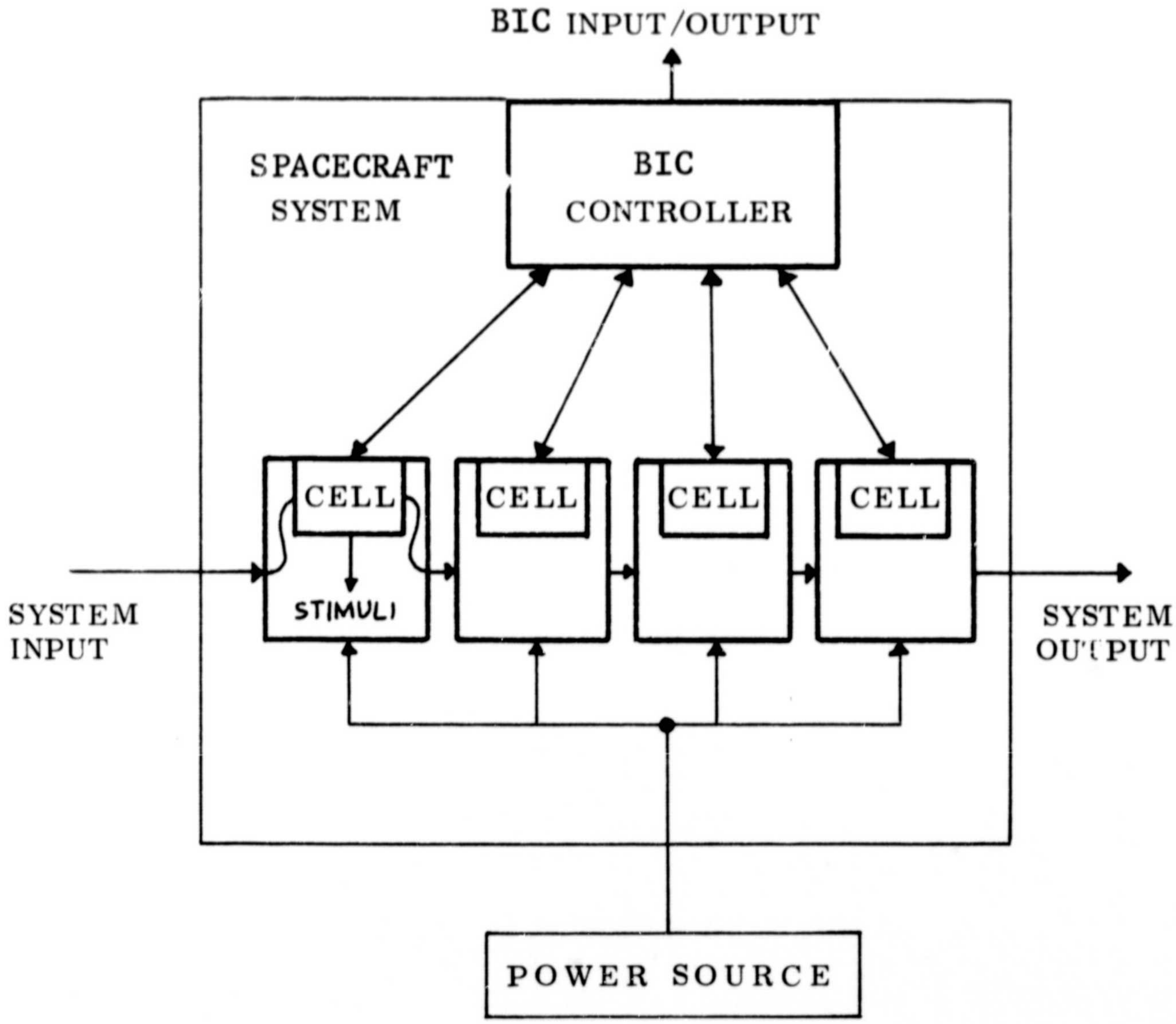

BIC INPUT/OUTPUT
SPACECRAFT SYSTEM
BIC CONTROLLER
CELL
CELL
CELL
CELL
STIMULI
SYSTEM INPUT
SYSTEM OUTPUT
POWER SOURCE

FIGURE 2

As shown in Figure 3, there are six modes of operation available to BIC. The Activate Mode (1) is primarily a wake-up type command from the Control Center to BIC activating the logic, while the Deactivate Mode (6) turns the logic off. This conserves power when BIC is not in use, an especially important consideration for long duration missions. The Bypass Mode (5) allows the Control Center to bypass the Controller and communicate directly with the Cells, providing a redundant capability in case of a Controller malfunction during a critical phase of the mission. The Checkout Mode (2) is used primarily for detailed ground checkout when all data from the spacecraft must be evaluated to determine that the system performs within design limits. The Operational Mode (3) would be used primarily in flight and provides only cursory or summary data to assure system availability, while the Monitor Mode (4) provides for a fast reaction caution and warning type response. The Checkout, Operational and Monitor Modes will now be discussed in greater detail to emphasize BIC's capabilities.

Checkout Mode - The communications path for data in the Checkout Mode is shown in Figure 4. In this Mode, complete checkout sequences for a particular test of the concerned subsystem are transmitted to the BIC Controller from the Control Center . The Controller then conditions the Cell logic, establishing limits for particular points to be measured, and preparing the cell to generate stimuli if required. Next the BIC Controller will receive a coded command from the Control Center to start a checkout sequence. The BIC Cells, when commanded by the Controller will generate stimuli and make measurements of the signal points. The end result is a digital word of ten bits (eight bits will carry data and two bits will be used to indicate whether data is within predetermined limits) which is communicated to the BIC Controller for data averaging and transmission to the Control Center for overall assessment of the

MODES OF OPERATION

1. ACTIVATE	(WAKE UP)
2. CHECKOUT	(DETAILED-GROUND)
3. OPERATIONAL	(FLIGHT-CURSORY)
4. MONITOR	(CAUTION-WARINING)
5. BYPASS	(BIC CONTROLLER)
6. DEACTIVATE	(SLEEP)

FIGURE 3

CHECKOUT MODE

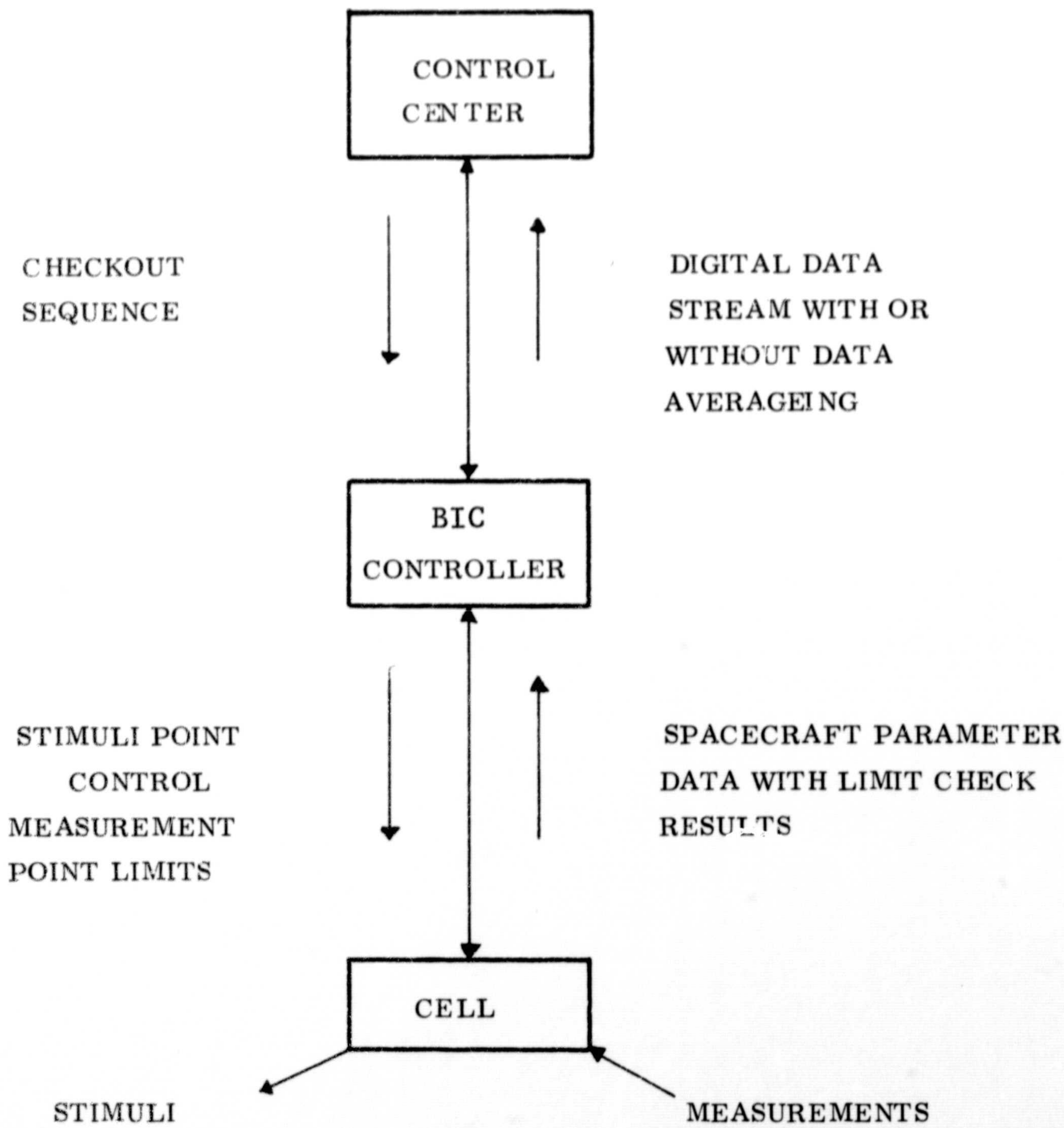


FIGURE 4

quality of the system. As pointed out previously this mode of operation is most applicable to detailed ground checkout.

Operational Mode - The communication flow for the Operational Mode is shown in Figure 5. This mode is similar to the Checkout Mode except for the amount of data transfer between the Controller and Control Center. The Control Center still sends an operational sequence to the Controller which in turn conditions its cells, and then makes one scan of all Cells. Each Cell reports the status of its spacecraft components as being GOOD, MARGINAL, or BAD. A GOOD condition means all is well, a MARGINAL condition may refer to operation of an alternate or backup mode, while a BAD condition refers to a malfunction. The Controller then assesses all of its Cells outputs and reports a GOOD, MARGINAL or BAD system status to the Control Center. In the case of a BAD or MARGINAL condition the Component ID is transmitted as part of the status. Thus the Operational Mode serves as a cursory check to assure that each spacecraft system is available to support the mission, or point up a MARGINAL or BAD condition for further corrective action if desired.

Monitor Mode - The Monitor Mode serves as the Caution and Warning Mode whereby the BIC functions passively, continuously monitoring selected signal points. In this Mode of operation the BIC cell makes comparisons of selected signals with predetermined limits; however, no output is generated unless the Cell comparison indicates a MARGINAL, BAD or a BIC SICK condition in which case an interrupt signal is transmitted to the BIC Controller. The Controller will assess the condition and initiate corrective action as required. If the condition which generated the interrupt cannot be corrected and it affects system performance, the Controller will transmit a system MARGINAL, BAD or BIC SICK indication to the Control Center for further action.

OPERATIONAL MODE

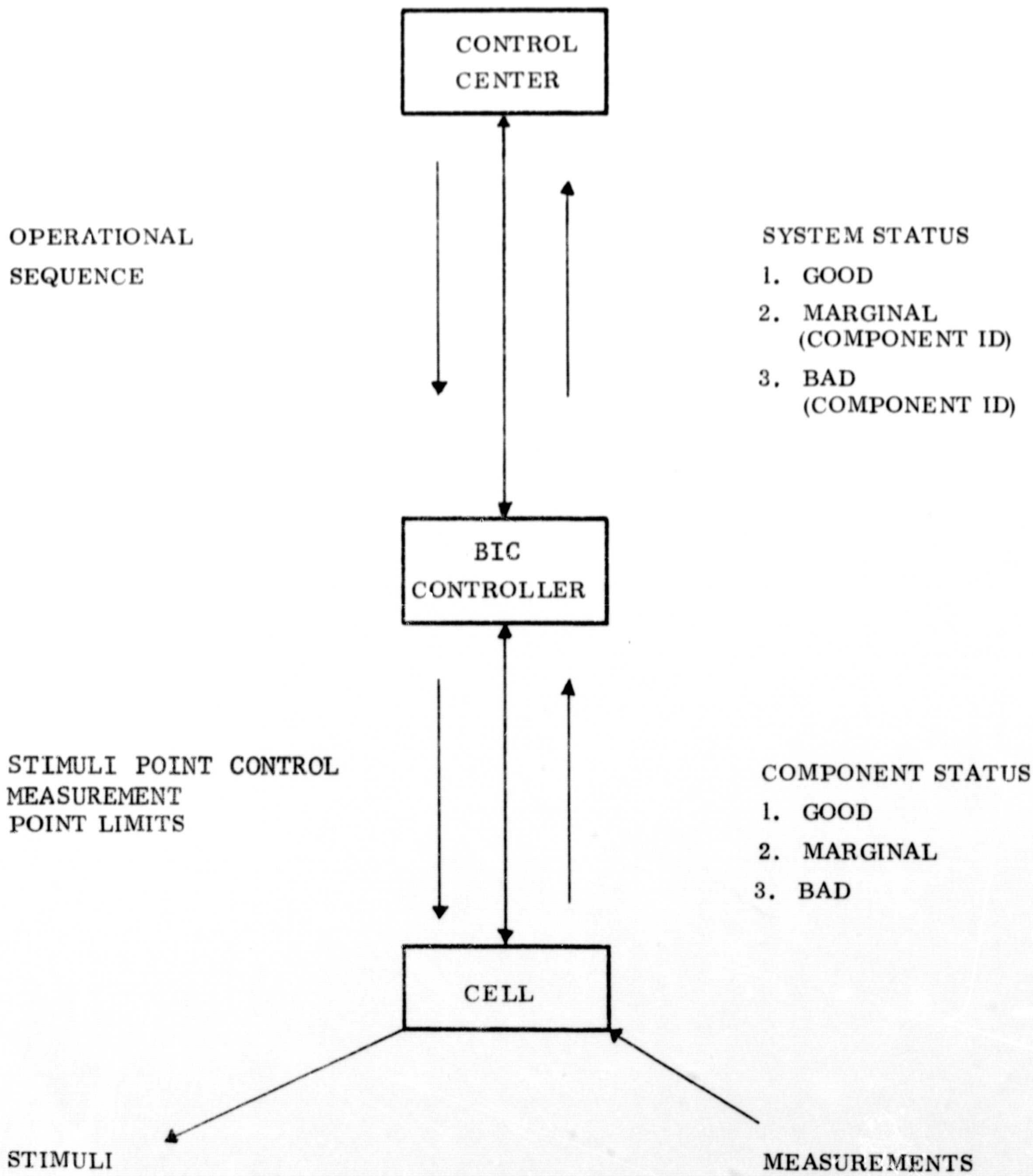


FIGURE 5

MONITOR MODE

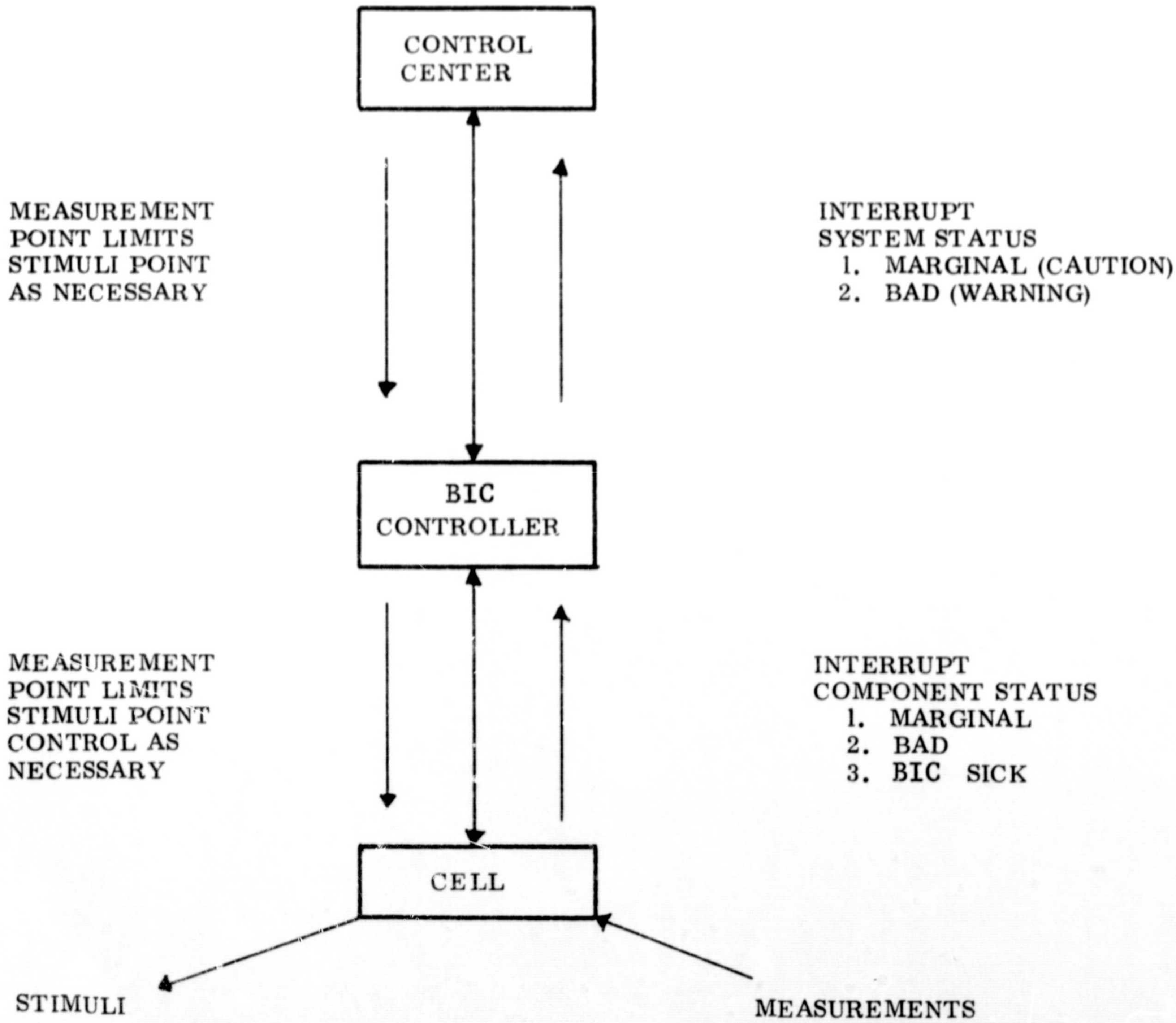


FIGURE 6

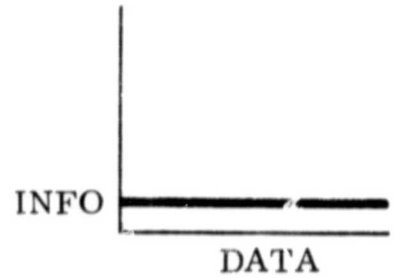
Information to Data Ratio - A further assessment of the three primary modes of BIC operation reveals some very interesting possibilities in the area of Data Compression at various levels of test. As can be seen from Figure 6, the amount of actual useful information in relation to Data Rate is very low on present Apollo. Should you only need one word a second, the basic Data Rate is still 204.8 kbs. In the BIC Checkout Mode, the amount of data is similar to that obtained under present Apollo checkout, however, additional useful information as to whether the system meets predetermined limits is also provided. To further enhance the ratio of Information to Data in the Checkout Mode, data averaging can be performed by the BIC Controller prior to transmitting data to the Control Center. This enhancement is further developed by operation in the Operational Mode, since only status data, all of which is useful, is transmitted to the Control Center. It follows then that in the Monitor Mode, the ratio of Information to Data is greatest since only indication of anomalies or impending anomalies are transmitted beyond the Cell level.

BIC Design

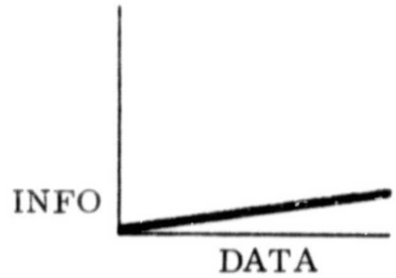
From the forgoing description of BIC capabilities, it would appear that a great deal of logic and hardware is involved. However, the design accomplished to date indicates a conclusion quite the contrary. By tailoring each Cell to fit the spacecraft system Component requirement, and each Controller to the Black Box level, the extra logic always included in normal test equipment to provide universality and flexibility is no longer required and can be eliminated.

INFORMATION TO DATA RATIO

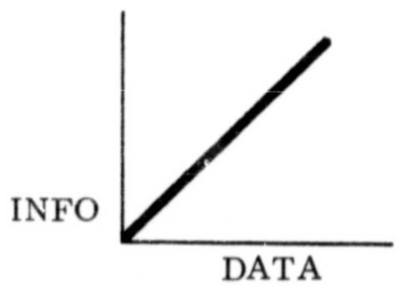
PRESENT APOLLO



BIC CHECKOUT
MODE



BIC OPERATIONAL
MODE



BIC MONITOR MODE

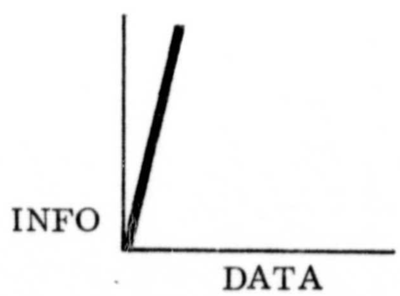


FIGURE 7

BIC Cell

By referring to Figure 8, it can be seen that a typical BIC Cell is really quite simple in operation and in design. The particular Cell illustrated is designed to measure an analog voltage and close or open a relay for a stimulus point. If a discrete or analog voltage output were required at this or some other test point, the particular Cell involved would be designed to output the required function, or if a voltage level detection only were required, then the Cell would be configured to that type of measurement. Hence, it should again be emphasized that the Cell is tailored to perform only the function required by its spacecraft system component.

Referring back to figure 8, a typical BIC Cell consists of an Input/Output Register, Analog-to-Digital Converter, Limit Register, Comparator, Stimuli Register and some Control Logic. The Input/Output Register is a 12 bit serial to parallel converter that is required to receive and transmit messages to the BIC Controller in a serial fashion. This technique reduces the internal cabling from 12 cables to a single wire. The Limit Register is used to store the limits to be compared with the measurements. For a dynamic spacecraft component this register could be updated as required to meet changing test requirements through the Input/Output Register. The Comparator is used to detect when the measurement data is not within its assigned limits by performing a less than or greater than function. The Comparator will also generate a 3 bit code which represents GOOD, MARGINAL or BAD, and when a MARGINAL or BAD condition occurs, flag the BIC Controller. The Stimuli Register will store a word which represents the desired state of the stimuli point(s) and status of the backup spacecraft component. The Register may be loaded from the Controller and can transmit status to the Controller via the Input/Output Register.

BIC CELL

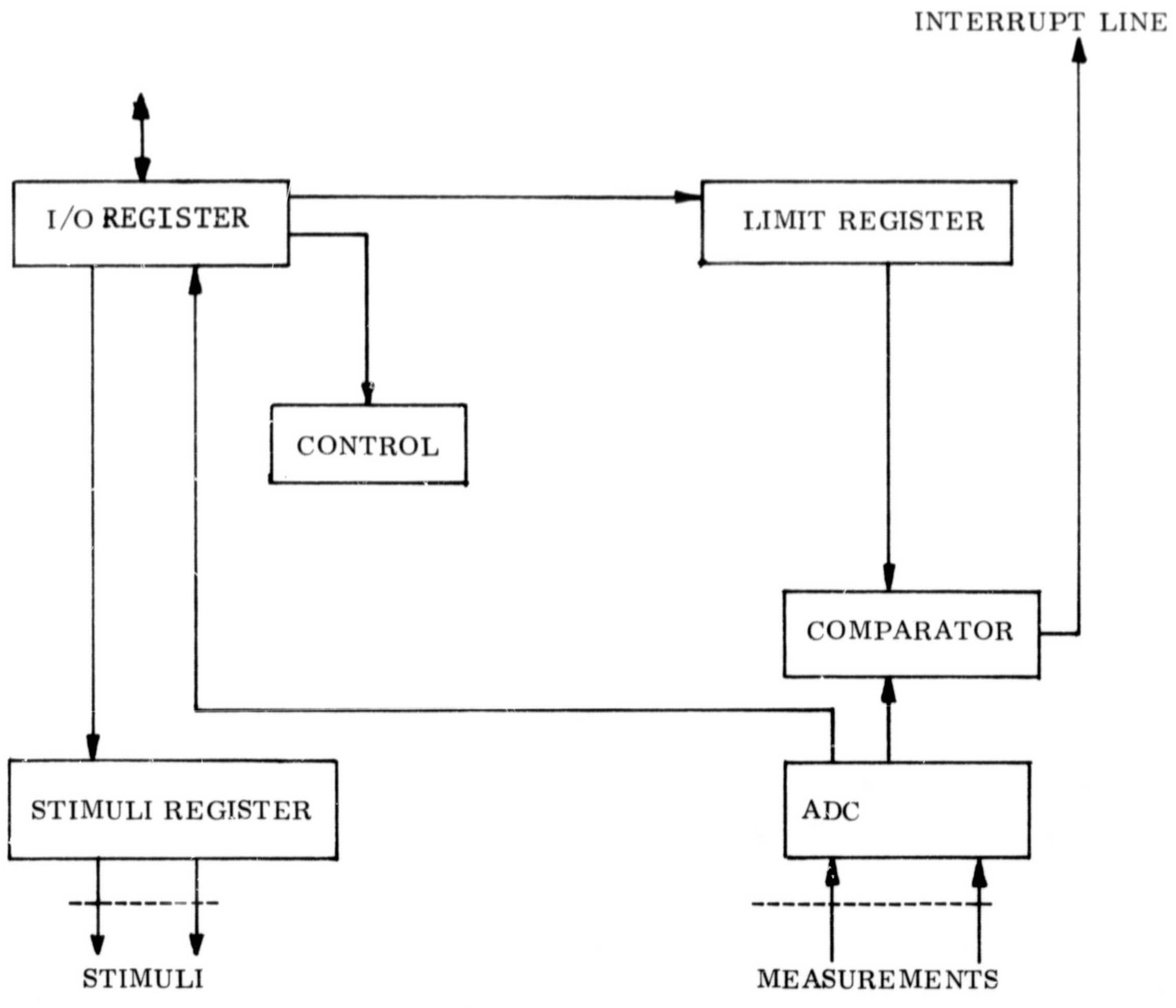


FIGURE 8

The Analog-to-Digital Converter (ADC) maps the analog value to its equivalent digital state. The Control Logic integrates the cell operation and provides for proper mode recognition.

BIC Controller

As pointed out before,the BIC Controller provides the common external interface to the Control Center. It is somewhat more sophistocated than the Cell, and may or may not contain a small memory, since it is also tailored to the "Black Box" or system. As many Cells as required can be serviced by a single Controller. To date, no communication directly between Controllers is envisioned; however, this concept may be modified at a later date. A typical BIC Controller is shown in Figure 9. The Input/Output Register receives serial digital data from some Control Center. Depending upon the nature of the data and the selected mode of operation, the Control Logic may exercise the Controller Cells or load/modify/dump the memory. The Cell Interrupt Scanner is used to sequentially monitor the interrupt lines. When an interrupt line is set, the monitoring of all other lines is stopped and the Cell Address Decoder is signalled. The Cell Address Decoder determines which Cell set the interrupt line and enables gating to establish a communication link between that Cell and the Control Logic. The Decoder also has the ability to initiate the communication link from the Controller to a Cell in order to update the Cells reference data or to status the Cell. The Control Function will provide the proper sequence of reference data for each Cell. This will be accomplished by utilizing or accessing the memory. The Control Function also summarizes the system status and decides if the system is GOOD, MARGINAL or BAD, and may, if the conditions dictate, generate an interrupt to the Control Center.

BIC CONTROLLER

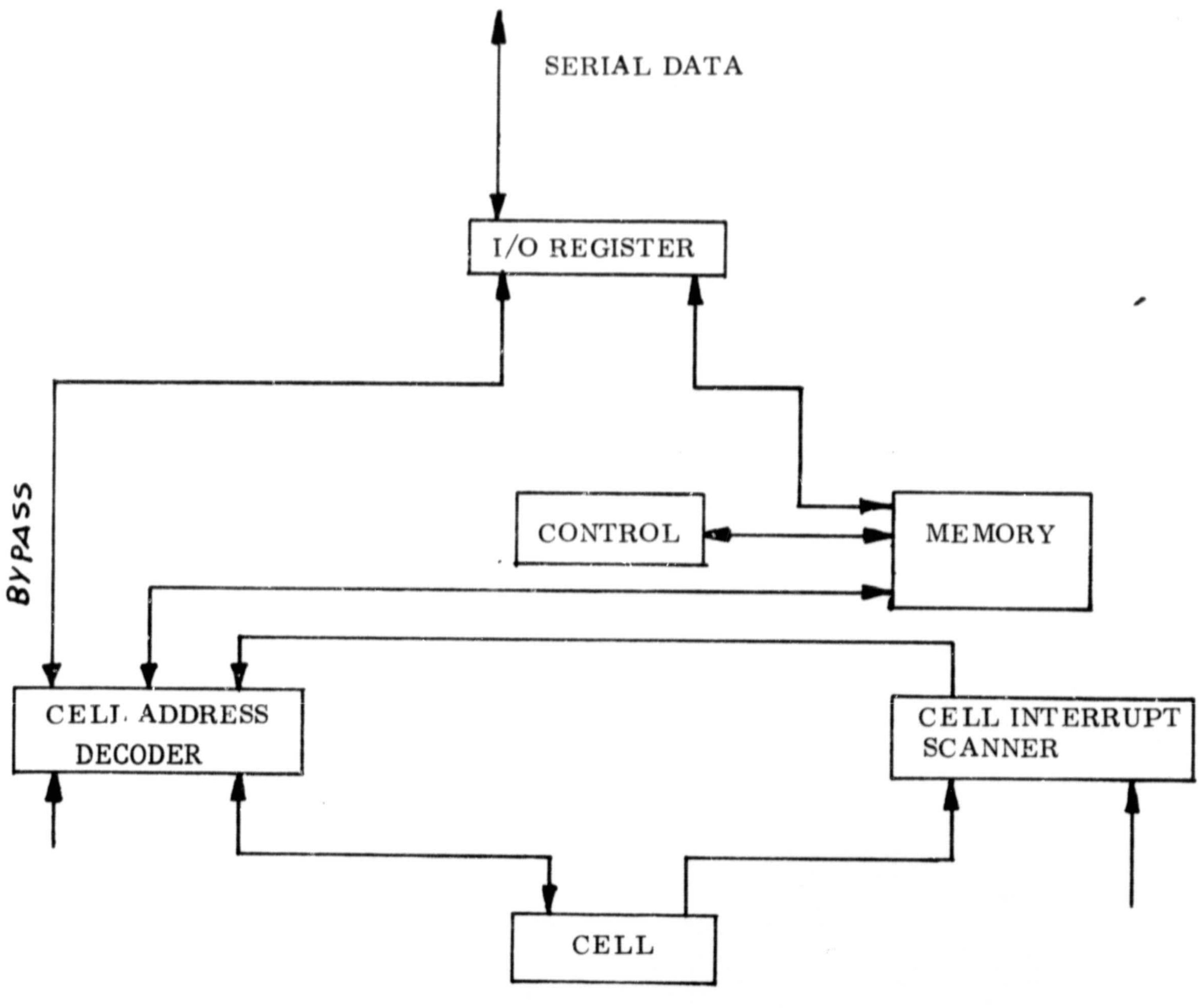


FIGURE 9

Application

When attempting to develop a new approach in any discipline, unforeseen problems usually occur. In order to understand and solve these problems, it is planned to demonstrate a breadboard version of BIC in the Checkout Systems Branch Laboratory. To achieve this,the test setup shown in Figure 10 is being built. The Test Article chosen is an electrical simulation of a portion of the Environmental Control System. A very simplified block diagram is shown in Figure 10. The BIC Controller and a total of 7 Cells are currently being built. A planned feasibility test is presently scheduled for July 11, 1969. Two other efforts will be initiated as soon thereafter as possible. The first is to utilize a Large Scale Integration (LSI) packaging technique in the hope of reducing the Cell to less than 1/2 inch square, and a Controller to about a 2" x 3" printed circuit card. Concurrently with this, further design will be initiated to breadboard a Controller and Cells to either checkout an operational Apollo System or some other chosen Test Article.

Summary

At this time, many problems still exist before BIC can be proven operational. However, design has progressed far enough to prove the concept is feasible, and these problems are primarily interface problems that can be solved with time and effort. The simplicity of the Cell concept is unique, but what better place is there to simplify and integrate checkout than to build it in the unit to be checked?

PRESENT SUBSYSTEM SAMPLE

(ECS - CRYOGENICS)

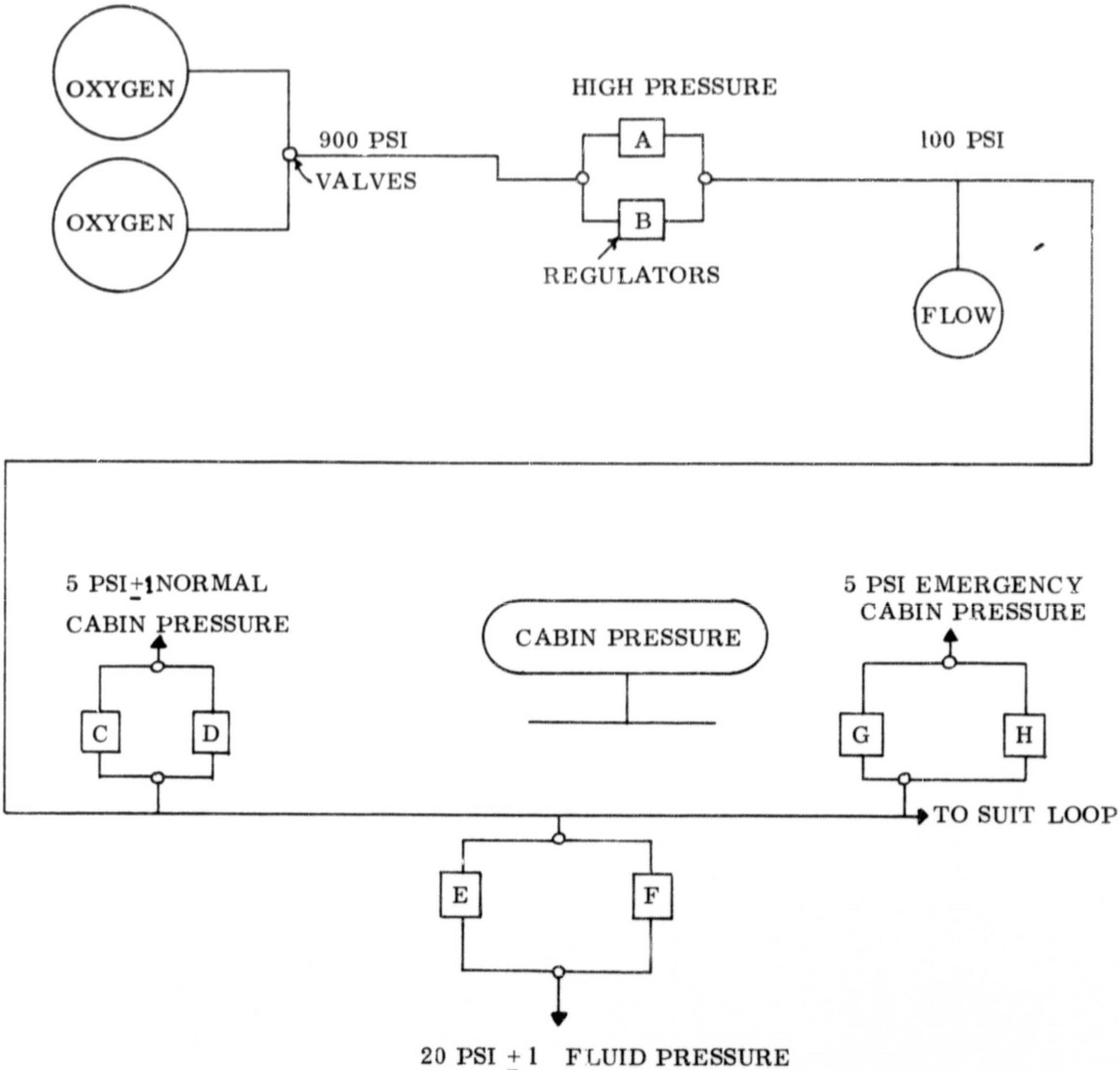


FIGURE 10