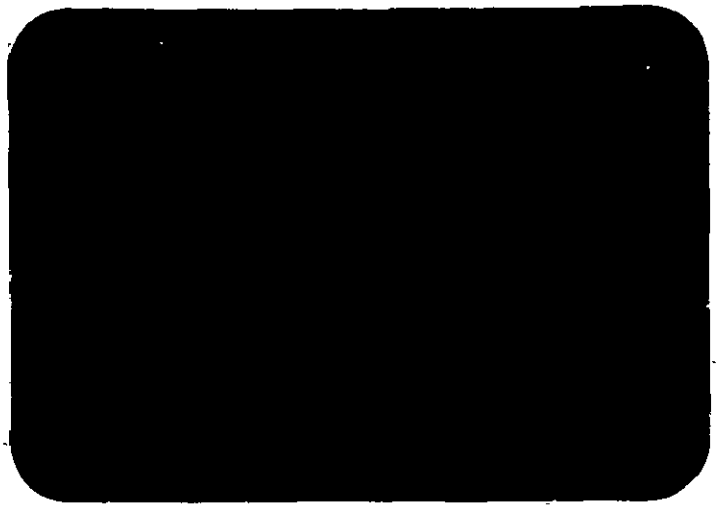

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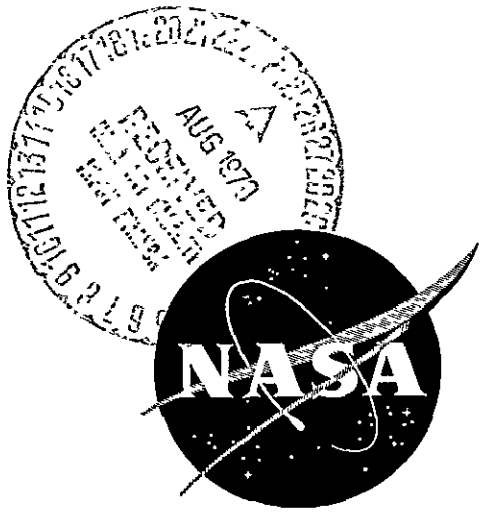

Manned Spacecraft Center

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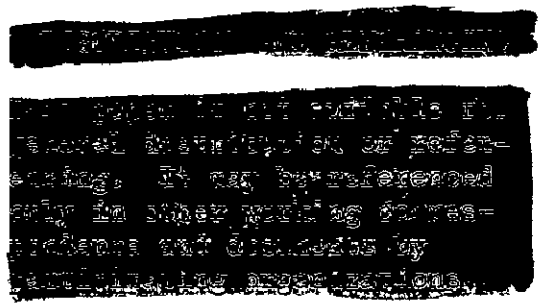
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

INTERNAL NOTE MSC-67-EE-12, REV. A

DEVELOPMENT OF A SPACECRAFT ATOMIC TIMING SYSTEM



MANNED SPACECRAFT CENTER
HOUSTON, TEXAS

May 6, 1968

MSC INTERNAL NOTE MSC-67-EE-12, Rev. A

Apollo Applications Program

DEVELOPMENT OF A SPACECRAFT ATOMIC TIMING SYSTEM

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NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

MANNED SPACECRAFT CENTER

INSTRUMENTATION AND ELECTRONIC SYSTEMS DIVISION

HOUSTON, TEXAS

May 6, 1968

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PART 1 - PROJECT DEVELOPMENT PLAN

1 GENERAL

The purpose of this document is to describe the development of a central timing system with the required stability, accuracy, reliability, and versatility necessary to support critical future spacecraft needs. Present timing equipment is capable of meeting only the minimum accuracy and stability requirements. This system will be capable of supplying all spacecraft timing needs, both operational and experimental.

In order to provide increased timing accuracy and stability, it is necessary to utilize some form of atomic frequency control. In order to accomplish this, a contract has been awarded to Varian Associates for the design, development, and construction of both a breadboard and an engineering model Atomic Timing System. The design and construction of the engineering model has been subcontracted to General Radio. This system will make use of a Rubidium gas resonance cell. Full evaluation of the breadboard and complete qualification of the engineering model will be performed at MSC.

The Apollo Spacecraft Timing Equipment is dependent upon a ground station reference. Periodic updating via the updata link from the ground station is required to maintain the accuracy stability of the Central Timing Equipment. The frequency stability cannot be adjusted at all. The proposed system will make the spacecraft independent from the earth for all timing and frequency source needs, thereby enabling the crew to analyze time and frequency dependent problems, determine

the necessary action to alleviate the problems, and perform required critical mission functions with fewer constraints. A block diagram of the proposed system is shown in Figure 2-1.

2. PROJECT OUTLINE

This project is divided into three major parts: Breadboard Model development, Engineering Model development, and Flight Model development. An outline of these stages is shown below

PART 1 - Breadboard Model Development

a. Design study
b. Breadboard design and construction
c. Test facility design and construction
d. Breadboard evaluation
e. Breadboard long term stability test

PART 2 - Engineering Model Development

a. Design finalization
b. Engineering model construction
c. Electrical and performance tests*
d. Environmental tests*
e. Long term stability test

PART 3 - Flight Model Development

a. Determination of redundancy and particular flight requirements
b. Flight model design
c. Flight model construction
d. Type qualification

*Part 2, c., and d., comprise the Design Verification Test (DVT)

3. MODEL DEFINITIONS

A Breadboard Model is herein considered an assembly of preliminary parts designed to prove the feasibility of a device, system, or principle in rough form without particular regard to the eventual overall mechanical design.

An engineering Model is herein considered a model that is designed and fabricated to electrically and mechanically meet the requirements of the specification. It's purpose is to demonstrate the technical soundness of the design. It is not required to comply with all of the usual quality requirements for manned spacecraft flight hardware; however, it shall employ approved parts or their interchangeable equivalents.

A Flight Model is herein considered a flight configured, flightweight model suitable for complete evaluation of all physical and functional characteristics. It is in final form, employs approved parts, and is fabricated under full Government Source Inspection using approved tooling and processes.

SPACECRAFT ATOMIC TIMING SYSTEM (SATS) DEVELOPMENT PART 2 - SYSTEM DESCRIPTION

1. GENERAL

The Spacec[illegible]iming System presently under development takes advantage of the microwave resonance of rubidium gas and employs a rubidium gas reference cell as the frequency determining element. This system will have long term stability of five parts in 10^{11} for a period of one year. This represents an error in total time accumulation of only one second in 50 years. The short term stability will be three parts in 10^{11} for a one second averaging time.

1.1 Basic Principle of Operation

A rubidium frequency standard uses a microwave resonance in the ground state of rubidium 87 as the discriminator in an AFC loop to maintain a quartz crystal oscillator at a subharmonic of that resonant frequency. The rubidium in which the resonance occurs is in the form of a vapor contained within a small glass cell that is enclosed in a microwave cavity (see Figure 2-1). This cell is illuminated by light from a lamp filled with rubidium 87 and the light passes through a filter cell that contains rubidium 85. The filter cell acts as an absorption filter and passes only a selected spectral bandwidth of the light from the lamp. This light has the effect of raising the rubidium atoms in the gas cell to the higher of two hyperfine energy levels, and hence light energy is extracted from the beam. This phenomenon is called optical pumping. When microwave energy from the crystal oscillator-multiplier chain is introduced into the cavity at exactly the hyperfine transition frequency (6,834.688000 megacycles) of the outer electron in the rubidium atom, the atom is induced back to the lower energy level. As a result of this combined action, as

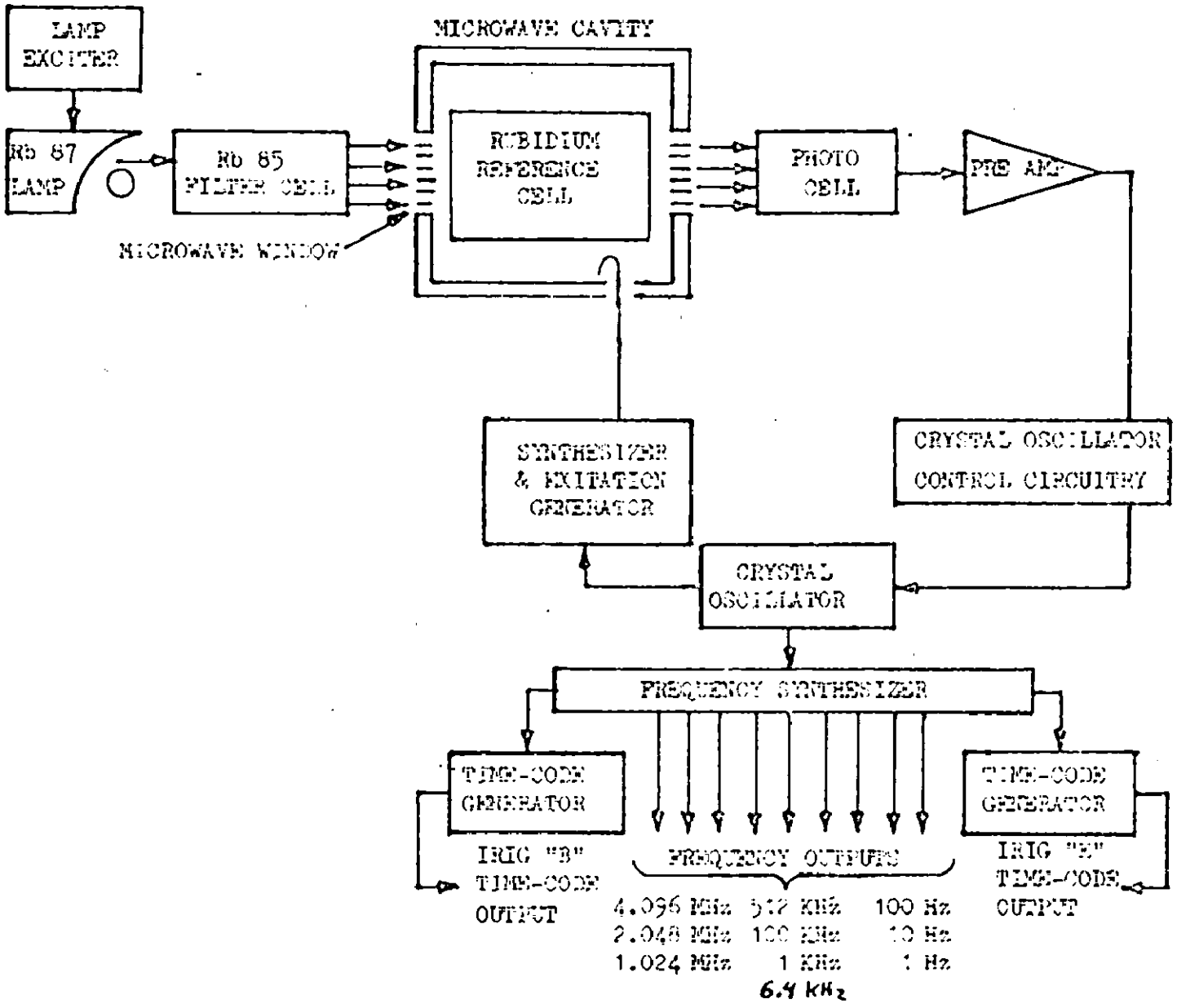


Figure 2-1. Spacecraft Atomic Timing System Block Diagram

long as the microwave signal is exactly on frequency the rubidium gas will continue to absorb light energy and the light energy falling on the photo detector will be at a minimum. If the microwave signal is not present, or is off frequency, the rubidium atoms are rapidly "pumped" to the higher energy level, after which only a small amount of light is absorbed, and the incident light on the photocell increases. The microwave signal is phase modulated and the resulting modulation that appears on the output of the photocell is used in a synchronous detector to maintain the crystal oscillator at the atomic resonance frequency. The crystal oscillator then drives a frequency synthesizer and time code generators which produce the required discrete frequencies and time codes for use in the various spacecraft systems.

SPACECRAFT ATOMIC TIMING SYSTEM (SATS) DEVELOPMENT

PART 3 - TEST PLAN

1. GENERAL

There are four basic groups of tests which will be required in order to bring the SATS to flight hardware status. These are as follows: engineering evaluation of the breadboard system; Design Verification Test (DVT) of the engineering model to all electrical and environmental specifications; type qualification of a production unit which will involve the same tests as the DVT with a shorter duration stability test; and flight qualification of each unit which is committed to fly in space. A general discussion of the goals of each group of tests is given below.

1.1 Engineering Breadboard Model Evaluation.

The breadboard is intended to meet all of the electrical requirements for spacecraft use; however, it will not be capable of sustaining any environmental tests except temperature.

When the system first arrives, it will be given a thorough electrical test. Since this will be the first opportunity to thoroughly exercise the test station, many tests will be conducted for the purpose of developing effective procedures to be used in testing the engineering model.

After the operation and performance of the breadboard and test station are established and understood, a temperature test will be conducted.

Finally the breadboard system will be checked for long term stability by running a continuous comparison between the SATS and the test station standards for a period of one year. The ATLAS computer complex will be used to receive, tabulate, and analyze the frequency stability data. It will also be used to monitor the performance of the hydrogen maser frequency standards.

All data, significant observations, and special procedures will be collected and retained in a permanently bound engineering notebook. Periodic reports and bulletins will be issued presenting a synthesis of pertinent data. (See Figure 3-1.)

See Appendix B for Evaluation Test Report.

1.2 Design Verification Test (DVT)

The engineering model will be constructed in flight configuration to meet all electrical and environmental requirements for spacecraft applications.

From the tests performed on the system breadboard, a complete DVT procedure will be written in approved form. Full electrical evaluation will be performed first. Environmental test will then be conducted in accordance with the requirements of the contract. Following these tests, the unit will be subjected to long term stability evaluation for a period of one year. This test will be continuous and will be similar to that performed on the breadboard with any necessary refinements in procedures incorporated.

This series is intended to prove that the concept of flying an independent time and frequency standard on long duration space missions is practical, and that this design is capable of doing the job.

LAB FREQUENCY STANDARDS

H-10 HYDROGEN MASERS - SERIAL Nos. 7 and 8

Deviation at start of test _____

Present deviation _____

Max. Deviation to date _____

Min. deviation to date _____

*RMS of daily averages to date _____

Test started: _____ Days _____ Hrs. _____ Min.

RMS taken at: _____ Days _____ Hrs. _____ Min.

*The beat frequency between the two masers is continuously monitored. The $\Delta f/f$ for each period between nulls is calculated and all periods are averaged for each day. An accumulated RMS of these daily averages is calculated and shown here.

LAB TIME STANDARDS

DIGITAL TIME CODE GENERATORS**

Deviation at start of test _____

Present Deviation _____

Test started: _____ Days _____ Hrs. _____ Min.

Present Readings: _____ Days _____ Hrs. _____ Min.

**Each generator is being driven by one of the masers, and each is running on Central Standard Time. TCG #1 is designated as the reference unit for comparison purposes. Measurement is made on TCG #2 and entered as + or - referenced to #1.

Figure 3-1. Timing Lab Equipment Performance Bulletin (continued)

SPACECRAFT FREQUENCY STANDARD

RUBIDIUM STANDARD ENGINEERING BREADBOARD

Lab Standard in use: Maser #7 [ ] #8 [ ]

Deviation at start of test _____

Max. daily average to date _____

***RMS of daily averages to date _____

Short term stability (for 1 sec. avg. time) _____

Test started: _____ Days _____ Hrs. _____ Min.

RMS taken: _____ Days _____ Hrs. _____ Min.

***Period measurements of the 1000 CPS signal derived from the comparison of the spacecraft standard and the lab standard are taken over a 100 second averaging time. These measurements are taken every 100 seconds and are averaged for each day. An accumulated RMS of these daily averages is calculated and shown here.

SPACECRAFT TIME STANDARD

ENGINEERING BREADBOARD

At start of test the Spacecraft Standard led [ ] lagged [ ]

the lab Standard by _____.

Spacecraft Standard presently leads [ ] lags [ ]

the lab Standard by _____.

Test started: _____ Days _____ Hrs. _____ Min.

Present reading: _____ Days _____ Hrs. _____ Min.

Figure 3-1. Timing Lab Equipment Performance Bulletin (Concluded)

1.3 Type Qualification

This test will be identical to the DVT described above with the exception of the long term stability test which will be shortened to a period not yet determined (probably 6 months or less).

1.4 Flight Qualification

Each flight unit will be required to undergo the standard flight qualification test which includes the following: electrical, temperature, vibration, altitude, and acceleration.

In addition to the standard tests, each unit, due to the extreme stability requirements, will be required to pass a minimum two-weeks stability test continuously monitored.

2. DESCRIPTION OF TESTS

2.1 Preliminary Electrical Tests

a. Functional check: check for the generation of all required output signals.
b. Input power.
c. Power line feedback.
d. Power source transient effects.
e. Insulation resistance.

f. Output impedance on each signal output.

g. Short term stability.

h. Long term stability over one to five days per test.

i. Debug ATLAS computer programs.

2.2 Test Station Compatibility Tests

a. Test each piece of test equipment separately for proper operation.

b. Check each equipment interface for proper combined operation.

c. Activate complete test station and check for proper operation by means of simulated flight system failures as well as normal measurements.

d. Check ATLAS computer programs for proper operation.

2.3 Final Electrical Tests

Repeat all tests listed in paragraph 2.1 using the test station in its final configuration.

2.4 Temperature Test

This test will consist of a one day cycle through both the high and low temperature environments as specified in the contract. Measurements of frequency stability, power consumption, and time keeping will be made throughout the test.

2.5 EMI

The Breadboard Model is not required to meet all EMI specifications; however, data will be collected and analyzed to determine if there are any particular areas where special care or added design effort will be required in building the Engineering Model.

2.6 Long Term Stability

The Test Station will be fully activated in the automatic mode with the ATLAS computer complex on the line. A continuous monitor of frequency stability and time keeping will be kept. In addition, daily checks will be made of all pertinent internal system test points. Periodic performance bulletins will be issued. (See Figure 3-1.) This test will run continuously for one year.

2.7 Design Verification Test (DVT) Criteria

a. Electrical and Functional - All tests described in paragraph 2.1 will be performed in accordance with the requirements of MSC/IESD Document 19-2, Part 1.
b. EMI - All tests will be performed in accordance with the requirements of MSC/IESD Document 19-3.
c. Environmental - All tests will be performed in accordance with the requirements of MSC/IESD Document 19-2, Part 1.
d. Long Term Stability - This test will be identical to that described in paragraph 2. If refinements are desired as a result of what is learned from the breadboard test, they will be incorporated.

2.8 Type Qualification Test Criteria

This test will be identical to the DVT described in paragraph 2.7 with the exception of the Long Term Stability test which will be shortened to a period not yet determined (probably 6 months or less).

2.9 Flight Qualification Criteria

a. Electrical and Functional - All tests described in paragraph 2.1 will be performed in accordance with the requirements of MSC/IMSD Document 19-2, Part 3.

b. Environmental - All tests will be performed in accordance with the requirements of MSC/IMSD Document 19-2, Part 3.

SPACECRAFT ATOMIC TIMING SYSTEM (SATS) DEVELOPMENT

PART 4 - TEST STATION DESCRIPTION

During evaluation of the performance of any device, it is a basic axiom that the instruments used in the evaluation must have accuracies of at least one order of magnitude greater than that required of the parameter being measured.

The accuracy and stability of the Spacecraft Atomic Timing System (SATS) is expected to be on the order of 5 parts in 10^{11} therefore, any device used as a comparison reference must have an accuracy and stability on the order of 5 parts in 10^{12} or better. The only frequency standard presently available with both long and short term stability equal to or greater than 1 part in 10^{12} is the H-10 Hydrogen Maser built by Varian Associates. This instrument will become the heart of the qualification test equipment facility at MSC for this project. Figure 4-1 is a rack configuration and Figure 4-2 is a block diagram of the overall test configuration.

It is possible to make long term stability measurements over a period of about one month and mathematically project what may happen over longer periods. However it is our intention to actually operate the Spacecraft Atomic Timing System for a period of one year and continuously monitor its performance by comparing the oscillator frequency with the Hydrogen Maser, and the digital time output with a time code generator driven by the Maser. In order to accomplish this without interruption to the data, it will be necessary to provide redundancy in the test equipment. There will be two identical channels for evaluation of the digital data thus insuring that there will always be at least one reference signal for comparison. The Phase Lock Loop Receiver (Figure 4-3) consists of a crystal oscillator, phase locked to the Maser. The output of the receiver will drive a reference time code generator.

PHASE LOCK LOOP RECEIVER NO. 1	FREQUENCY STABILITY CHECK SUBSYSTEM	"SEED" NO. 1	WWV RECEIVER TIME CODE GENERATOR NO.1	COMPUTER INTERFACE EQUIPMENT	ERROR DATA RECORDERS
		"SEED" NO. 2	TIME CODE GENERATOR NO.2	TEST STATION METER PANEL	NO. 1
	COUNTER	JUNCTION PANEL	"SATS" TIME DISPLAY	MASER RECORDERS	
PHASE LOCK LOOP RECEIVER NO. 2	RECORDER			OSCILLOSCOPE	NO. 2
		"SATS" AND TEST PANEL	COUNTER	SIGNAL MONITOR PANEL	
	PRINTER		PRINTER	SINE WAVE GENERATOR	NO. 3
	DISTRIBUTION AMPLIFIERS			28-Vdc POWER SUPPLY	NO. 4

Figure 4-1. Test Station Console Configuration For the Spacecraft Atomic Timing System

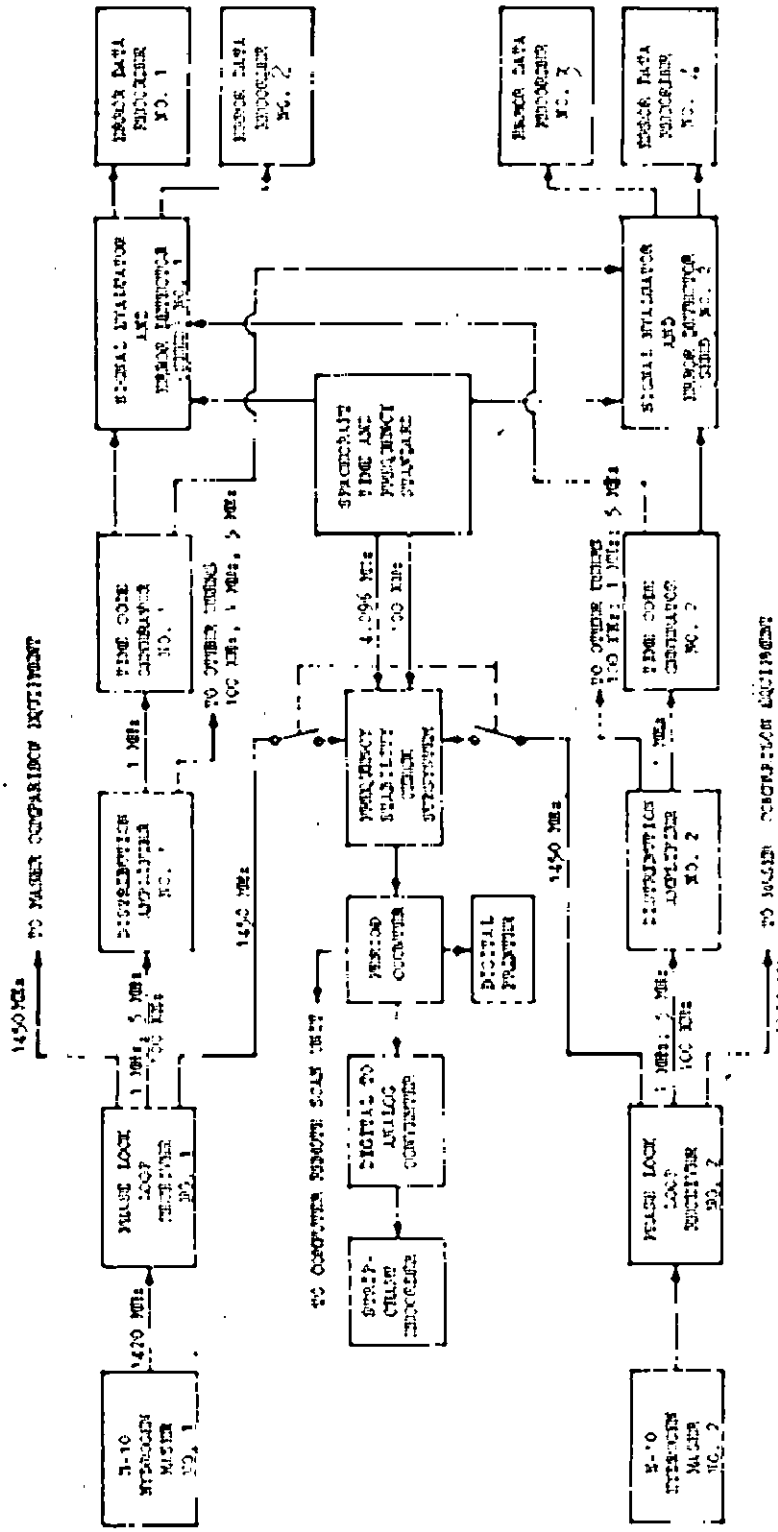


Figure 4-2. Spacecraft Atomic Timing System
Test Facility

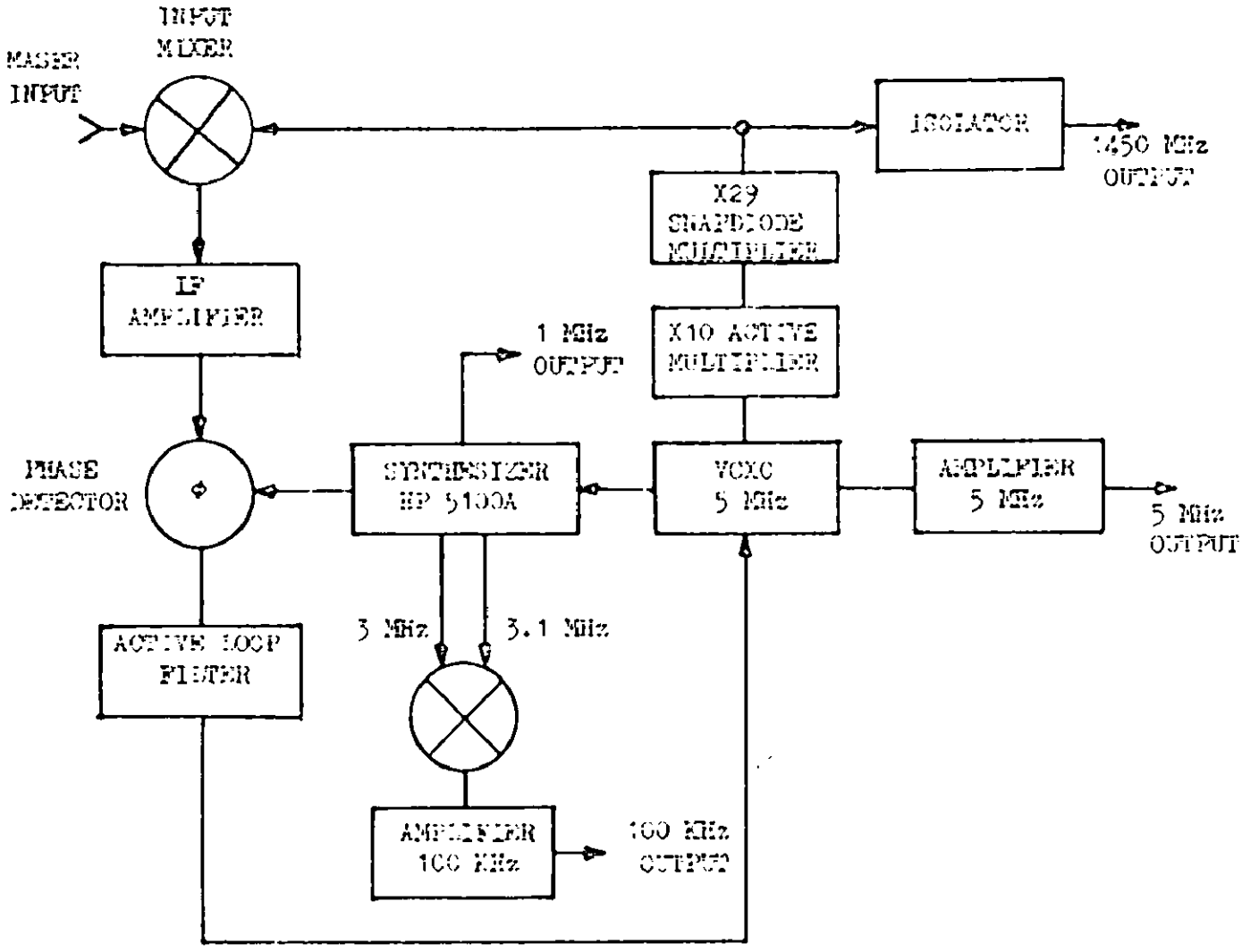


Figure 4-3. Phase Lock Loop Receiver Block Diagram

The performance of the masers will be continuously monitored by the equipment shown in Figure 4-4. A distribution amplifier is used to distribute the output signals from the phase lock loop receiver (see Figure 4-3).

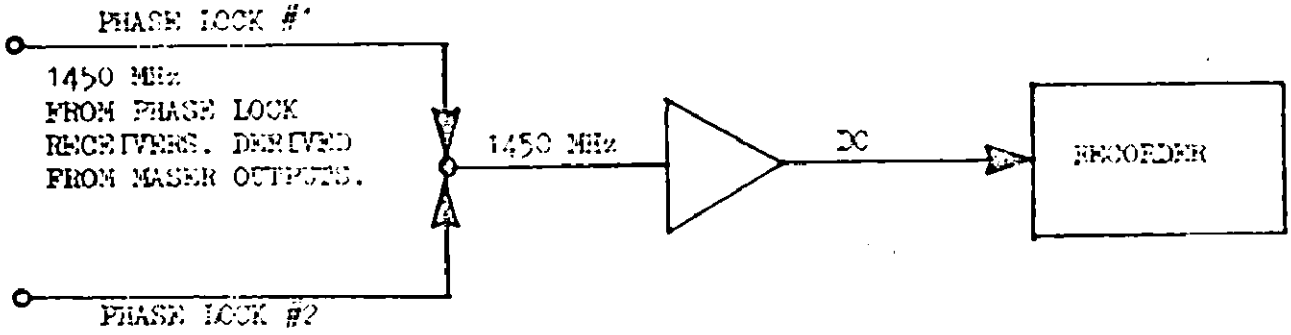


Figure 4-4. Maser Comparison Equipment

The 1450 MHz output of the phase lock loop receiver is fed to the frequency stability check subsystem where long and short term frequency stability of the spacecraft system is measured. See Figure 4-5.

The output of the reference time code generator is fed to the Signal Evaluator and Error Detector (SEED). See Figure 4-6. The SEED receives signals from the spacecraft time code generator, and each Maser driven reference time code generator. If at anytime the three inputs to the SEED do not correspond, the recorder is automatically turned on. All three time code signals are recorded as well as error signals which indicate which channel is in error.

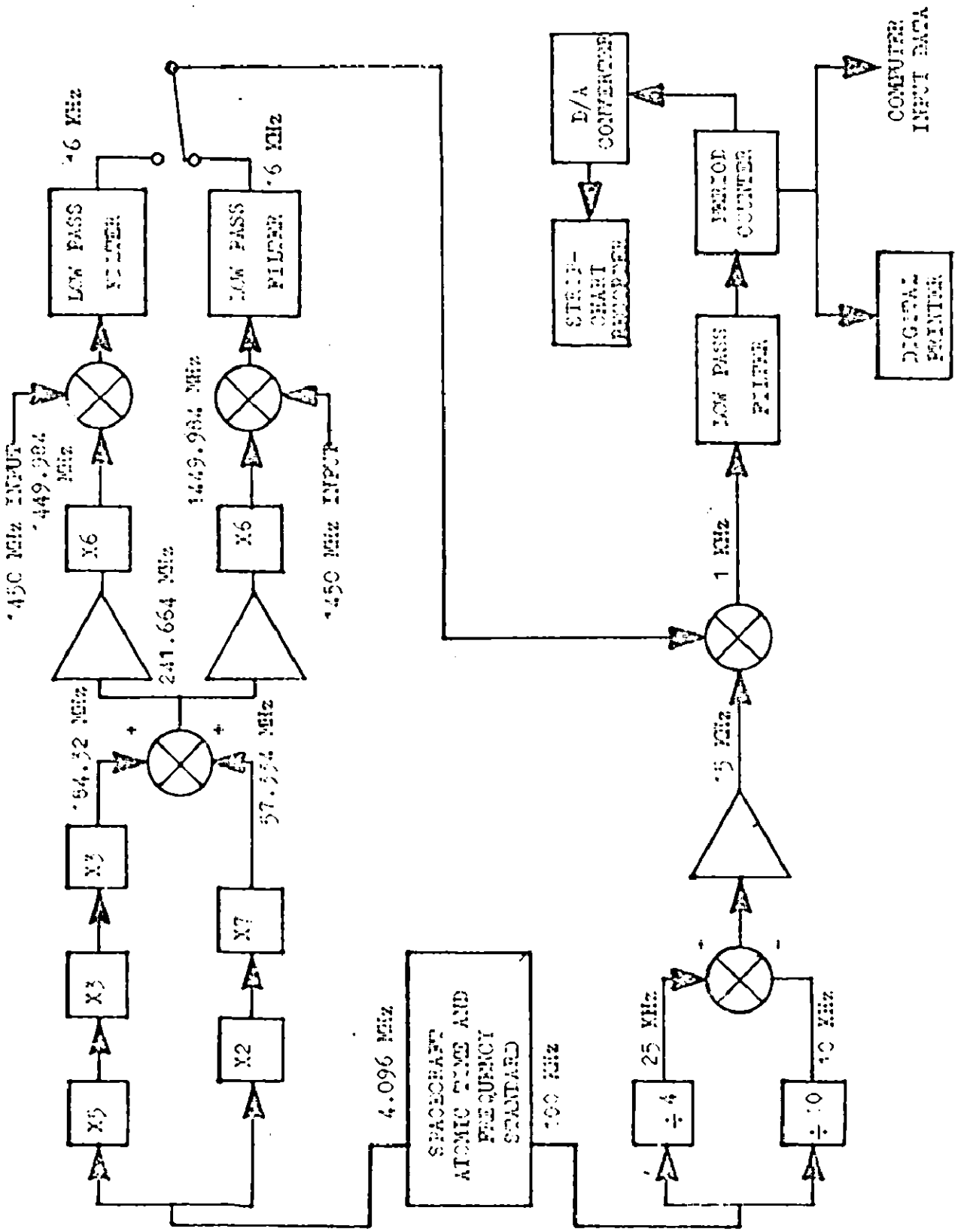
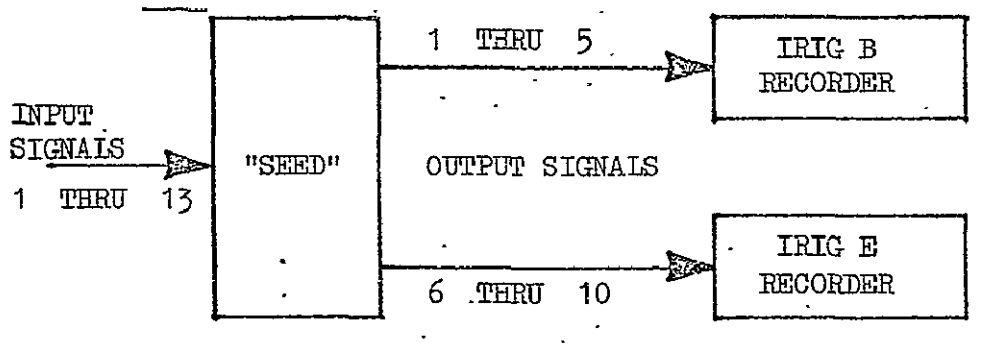


Figure 4-5. Frequency Stability Check Subsystem

"SEED" INPUTS		"SEED" OUTPUTS	
* 1	IRIG B	* 1	IRIG B
* 2	IRIG E	* 2	IRIG B error signals
3	4096 KHz square wave	3	Frequency error signal
4	2048 KHz square wave	4	Pulse Amplitude Error signal
5	1024 KHz square wave	5	Recorder Turn-on signal
6	512 KHx square wave	* 6	IRIG E
7	100 KHz square wave	* 7	IRIG E error signals
8	1 KHz square wave	8	Time Deviation Error signal
10	10 Hz square wave	10	Recorder Turn-on signal
11	1 Hz square wave		
12	1 Hz square wave 0 to 5 V		
13	1 Hz square wave 0 to 5 V		

*3 signals, one each from: Time Code Generator #1
Time Code Generator #2
Spacecraft Atomic Timing System



TWO IDENTICAL "SEED" SYSTEMS IN THE SATS TEST STATION.

Figure 4-6. Signal Evaluator and Error Detector "SEED"

The test station will be operated from an independent 28 volts DC supply. A system of batteries and associated charging and switching will be used as a back up supply in the event of main power failure. (See Figure 4-7.)

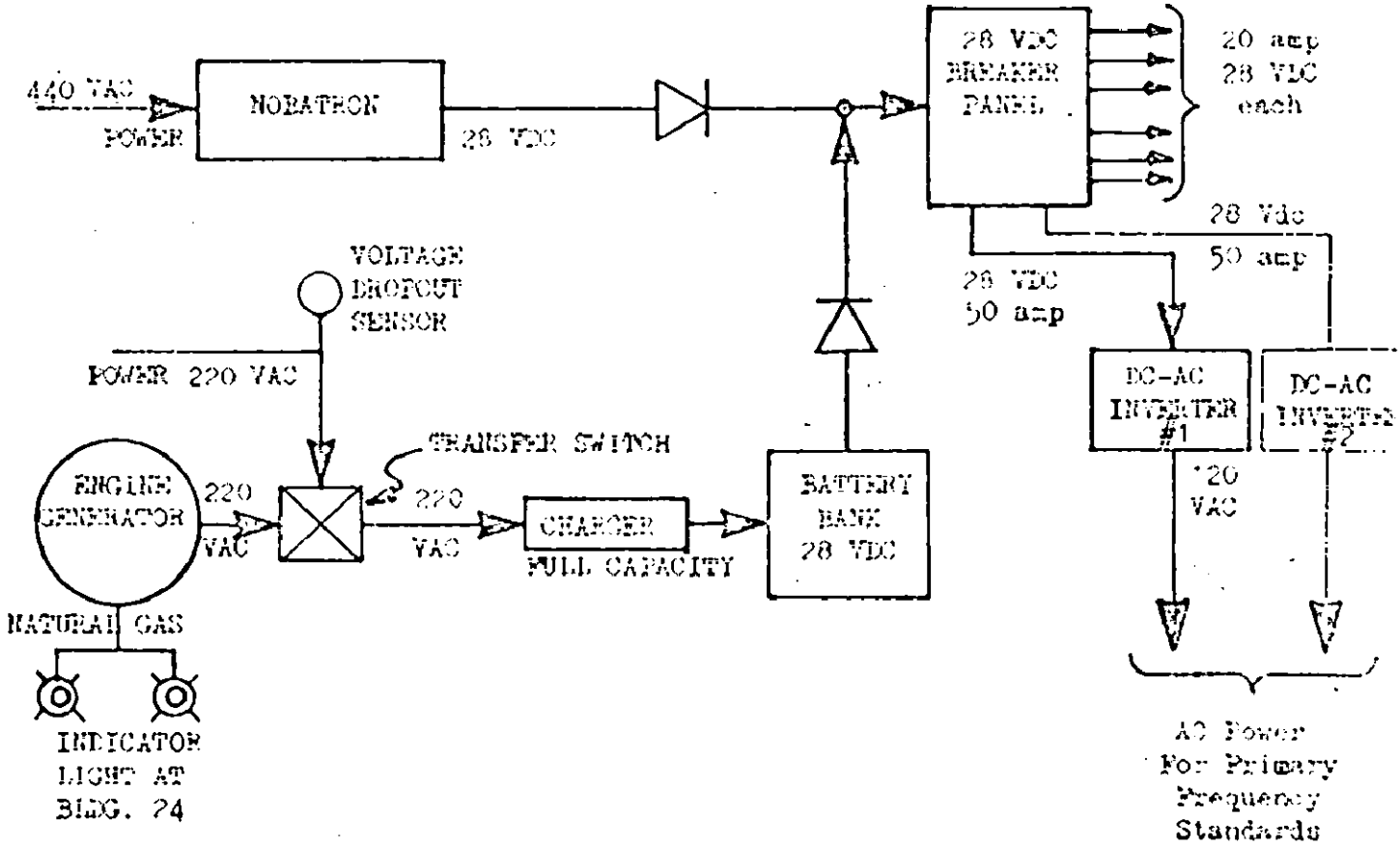


Figure 4-7. Auxiliary Power System for Spacecraft Atomic Timing System Test Station

SPACECRAFT ATOMIC TIMING SYSTEM (SATS) DEVELOPMENT

APPENDIX A - WORK STATEMENT

1.0 DESIGN GOALS AND INTENDED USE

1.1 The purpose of this work statement is to define the requirements for an engineering model of the Spacecraft Atomic Timing System, hereinafter referred to as the SATS.

1.2 An engineering model is considered here as a model that is designed and fabricated to electrically and mechanically meet the requirements of the specification. Its purpose is to demonstrate the technical soundness of the design. It is not required to comply with all the usual quality requirements for manned spacecraft flight hardware; however, it shall employ approved parts or their interchangeable equivalents.

1.3 The SATS shall employ a rubidium gas reference cell in the frequency stabilizing loop. The SATS shall also make use of micrologic circuit elements wherever possible.

1.4 When finally qualified for spacecraft use, the SATS is intended to be used as the central spacecraft timing and frequency standard. It will provide the spacecraft with a highly accurate reference for use by the onboard programming, sequencing, communications, guidance and navigation, and tracking systems, as well as all control panel time displays. It will also provide onboard experiments with precise time and frequency as required.

1.5 It is intended that the SATS will be used aboard future long duration (up to several years in duration) manned space missions.

2.0 ELECTRICAL AND PERFORMANCE SPECIFICATIONS

The SATS shall be designed and constructed with the objective to operate within the specifications listed below for a minimum of twelve months continuously without repair or adjustment, and when subjected to the environments and power source conditions specified in section 3.0.

2.1 Long Term Stability

2.1.1 Frequency - Long term frequency stability shall be arrived at by daily measurements of frequency determined as the average of at least ten frequency measurements each taken over a 100-second averaging time. The standard deviation of the daily measurements shall be less than five parts in 10^{11} in a one-year period. Measurements will be made at constant temperature $\pm 3°C$.

2.1.2 Time - The accumulated time change shall not exceed that which is commensurate with the requirements of Paragraph 2.1.1 after initial frequency and time calibration at NASA based on at least one day of measurements relative to a hydrogen maser reference.

2.2 Short Term Stability

2.2.1 The short term frequency stability shall be equal to or less than three parts in 10^{11} rms for one second averaging times, except that during vibration, and acoustic environments described in 3.0 the short term stability shall be equal to or less than five parts in 10^{10} rms for one second averaging times with a target specification of 5 parts in 10^{11}.

2.2.2 Time - The time error due to any single shock shall not exceed 10 nanoseconds.

2.3 Output Signals - The SATS shall produce the following outputs in the A-1 time scale.

2.3.1 One 4096 kc square wave

2.3.2 One 2049 kc square wave

2.3.3 One 1024 kc square wave

2.3.4 One 512 kc square wave

2.3.5 One 100 kc square wave

2.3.6 One 6.4 kc square wave

2.3.7 One 1.0 kc square wave

2.3.8 One 100 cycles per second square wave

2.3.9 One 10 cycles per second square wave

2.3.10 One 1 cycle per second square wave

2.3.11 One time code output per IRIG standard format B

2.3.12 One time code output per IRIG standard format E

2.3.13 Time accumulator "flip flop" outputs: The "one", or positive output of each flip flop in the accumulator shall be brought out through a buffer to an external connector to give an output from 0.1 second to 365 days, 23 hours, 59 minutes, 59.9 seconds.

2.4 Output signals 2.3.1 through 2.3.10 shall produce 3 ±0.3 V peak-to-peak between a baseline of 0 ±.2 V DC and 3 ±.3 V DC into a 100 ohm load, with a 100 nanosecond rise and fall time.

2.5 Output signals 2.3.11 through 2.3.13 shall produce 5 ±.5V peak-to-peak between a baseline of 0 ±.2 V DC and +5 ±0.5 V DC into a 1000 ohm load.

2.6 Output signals 2.3.1 through 2.3.10 shall have a 50 ±3% (or ±60 nanoseconds, whichever is greater) duty cycle.

2.7 Outputs 2.3.11 and 2.3.12 are not required to contain the straight binary seconds time of day code between position identifiers P_8P_0.

2.8 The total time accumulation capability of the SATS shall be 365 days, 23 hours, 59 minutes, 59.9 seconds.

2.9 A method shall be provided, through the external cabling to the SATS, whereby a selection may be made to accumulate either 364 days, etc. or 365 days, etc., to accommodate the possibility of leap year.

2.10 A method shall be provided through external cabling to the SATS whereby the SATS can be synchronized with an external time reference to within ±1 microsecond.

2.11 Power Consumption: The power consumption of the SATS shall not exceed 30 W from +75°F to +142°F, and shall not exceed 42 W from +75°F to -30°F.

2.12 No damage shall occur if a momentary or permanent short circuit is applied to any of the outputs.

2.13 Grounding Procedure - The negative and positive of the 28 V circuit and the case ground shall be isolated from each other. The unit shall perform within specifications if the ground side of these circuits are made common externally. Provision shall be made for attaching an external grounding strap to the case of the SATS.

3.0 ENVIRONMENTS AND POWER SOURCE CONDITIONS

The SATS shall operate within the specifications listed in 2.0 when subjected to the environmental and power source conditions, either singly or any combination thereof, as described in NASA-MSC-IESD Document 19-2, Part I except as listed below.

3.1 The SATS shall be energized and operating within specifications during the tests described in paragraphs 2.4.2 through 2.4.5 of 19-2, Part I instead of being de-energized periodically as indicated. Maximum frequency change over the temperature range of -30° to +142°F shall be less than 1×10^{-10}.

3.2 In paragraph 2.4 and 2.4.3 of 19-2, Part I, change "160 ±5°F" to read "142 ±5°F" and add "at a rate not exceeding 4°F per minute".

3.3 In paragraph 2.4.4 of 19-2, Part I, change "to 0 ±5°F" to read "linearly to -30 ±5°F" and "15 ±5 minutes" to "50 ±5 minutes".

3.4 In paragraph 2.14 of 19-2, Part I, change "MIL-I-26600/MSC-EMI-10A" to read, "NASA-MSC-IESD Document 19-3".

4.0 MECHANICAL SPECIFICATIONS

4.1 Volume - The SATS volume, exclusive of connectors, shall not exceed 600 cubic inches maximum.

4.2 Weight - The SATS weight shall not exceed 25 pounds maximum.

4.3 Case Color - The color shall be selected by the contractor.

4.4 Produce Marking - Marking for identification shall be as specified in MIL-STD-130.

5.0 DELIVERABLE ITEMS

5.1 The contractor shall deliver two engineering models, as defined in Paragraph 1.2, three mating connectors for each external connector on both engineering models, and one dust cover for each external connector on both engineering models.

5.2 The contractor shall provide a minimum of two (2) weeks, at MSC, of engineering services but not to exceed one (1) qualified engineer to advise, assist, and instruct NASA personnel on matters of use, support, and solution of technical problems.

5.3 The contractor shall submit three (3) copies of the following documentation upon delivery of each equipment. All drawings shall be on D size paper. An 8 x 10 in. film positive of each drawing shall be provided.

5.3.1 Detailed electrical schematic drawings.

5.3.2 Detailed mechanical drawings.

5.3.3 Detailed parts list. Non-commerical parts such as transformers, inductors, special crystals, etc., will be identified in sufficient dimensional detail to reproduce. Commerical parts will be identified by manufacturer's part number.

5.3.4 Test and calibration data.

5.3.5 Instruction manuals.

5.4 Reports

5.4.1 The contractor shall submit ten (10) copies each of a monthly progress report during the performance of the contract. Reports shall be informal and shall include, but not be limited to, (a) a description of overall progress, (b) an indication of any current problems, along with proposed solutions, and (c) a discussion of the work to be performed during the next monthly reporting period.

5.4.2 The contractor shall submit ten (10) each of a formal final report which documents and summarized the results of the entire contract work, including recommendations and conclusions based on the experience and results obtained. The final report shall include tables, diagrams, curves, sketches, photographs, and drawings in sufficient detail to comprehensively explain in detail the results achieved under the contract.

6.0 DESIGN REVIEWS

6.1 A design review shall be held at MSC at the time the design of the engineering model is complete, and prior to the start of its construction.

6.2 Other design and progress reviews may be held at the contractor's facility from time to time throughout the performance of this effort.

6.3 A final design review shall be held at MSC upon completion of the final report described in Paragraph 5.4.2.

SPACECRAFT ATOMIC TIMING

SYSTEM EVALUATION
(Varian Associates)

ELECTRICAL AND TEMPERATURE

TEST REPORT

MSC/IESD Document 21-63

6 May 1968

Prepared By
Lockheed Electronics Company
for
Instrumentation and Electronic Systems Division

LEC Document 641D.21-478

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Instrumentation and Electronic Systems Division
Houston, Texas

INTRODUCTION

This report presents results of a part of the evaluation of a Varian Associates Spacecraft Atomic Timing System (SATS). Tests conducted in this evaluation included high- and low- temperature tests and the following electrical tests:

- Input voltage and current variation
- Power line transient feedback
- Power source effect
- Input voltage effect on frequency and short term stability

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LIST OF TABLES

SPACECRAFT ATOMIC TIMING SYSTEM EVALUATION
(Varian Associates)
ELECTRICAL AND TEMPERATURE
TEST REPORT

1. GENERAL

This document reports the results of the electrical and temperature tests performed on the Varian Associates engineering breadboard of the spacecraft atomic timing system (SATS) on January 4, 8, 9, 10, 11, and 25, 1968.

2. TEST METHODS

2.1 Monitoring

The error detection and recording section of the SATS test station was operated to automatically monitor the SATS IRIG time formats to verify conformance to the reference formats of the time code generators. The SATS Test and Calibration unit was utilized as a visual indicator for phase lock and acceptable signal levels.

2.2 Measuring

The input current was measured with an ammeter inserted in the negative power lead. The power line transient feedback was measured with an oscilloscope applied across a one-ohm resistor inserted in the negative power lead. Frequency stabilities were measured with the SATS test station frequency comparison section shown in the Figure 1 block diagram. Stability information was obtained for electronic

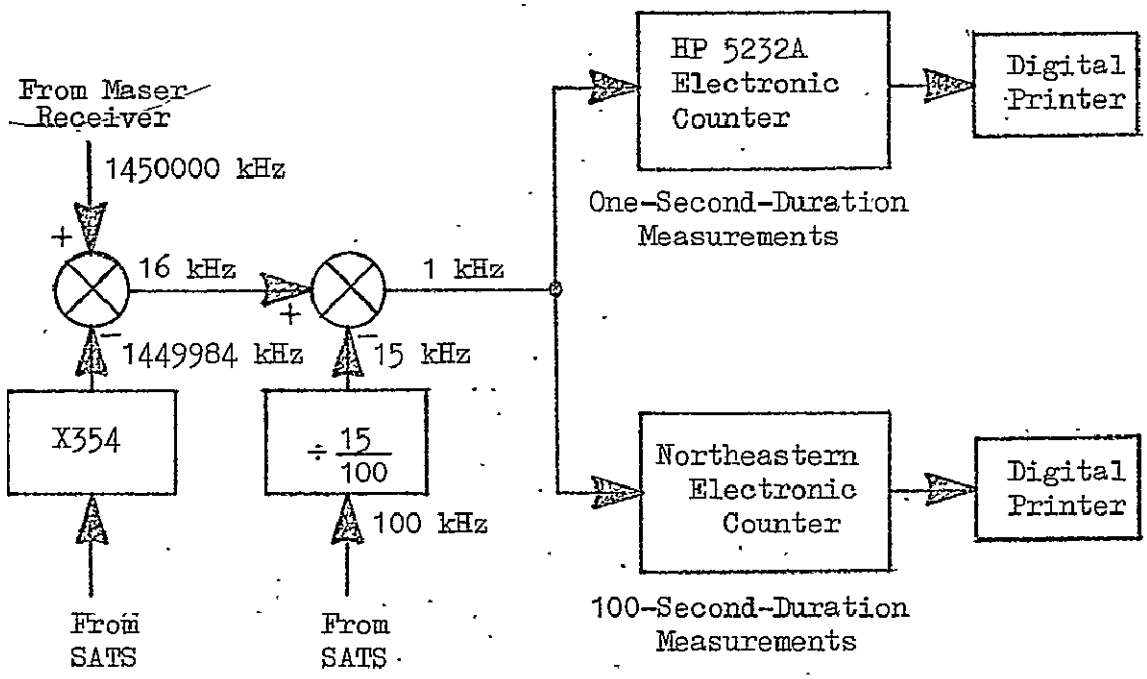


Figure 1. SATS Test Station Frequency Comparat

counter control functions measuring:

- the period required to count 100,000 cycles of the 1-kHz comparison signal; hereinafter referred to as 100-second-duration measurements.
- the period required to count 1000 cycles of the comparison signal; hereinafter referred to as one-second-duration measurements.

2.3 Calculating

a. 100-Second-Duration Data

Ten successive measurements were averaged to provide each 100-second-duration data point reported in this document. The measured frequency was divided by the comparison frequency (1.45×10^9 Hz) to provide the $\Delta f/f$ reading.

b. One-Second-Duration Data

One hundred successive measurements were recorded for each data point. The rms of the individual deviations from the applicable 100-second-duration data was computed to provide the one-second-duration value.

3. RESULTS

3.1 Electrical Tests

a. Input Voltage and Current Variation

When the input voltage was changed, the SATS input current varied as follows:

Input Voltage	Input Current
24 Vdc	860 mA
28 Vdc	800 mA
32 Vdc	750 mA

The SATS input current increased to approximately 100 mA as the reverse polarity voltage increased toward 10 Vdc.

b. Power Line Transient Feedback

When the input voltage was changed, the ripple voltage measured across a one-ohm resistor in the negative power lead varied as

follows:

Input Voltage	Ripple
24 Vdc	80 mV
28 Vdc	95 mV
32 Vdc	105 mV

c. Power Source Effect

While the input power was pulsating between 26 V and 30 V at a frequency swept from 1 Hz to 2000 Hz, the SATS operated for two minutes without indicating a loss of phase and without creating an erroneous IRIG format. The SATS short term stability computed from the rms of the deviations of 100 measurements of one second duration was $\Delta f/f = 2.66 \times 10^{-10}$.

When the input power was pulsed with a positive-going, 9-V amplitude, 200-millisecond basewidth transient, the SATS lost phase lock and created erroneous IRIG formats.

When the input power was pulsed with ten negative-going, 9-V amplitude, 200-millisecond basewidth transients, the SATS operated without indication of lock loss or IRIG error.

d. Input Voltage Effect on Frequency

The graph in Figure 2 depicts the effects of input voltage changes. The SATS had stabilized at each voltage for at least thirty minutes before the measurements were recorded, and ten 100-second measurements were averaged for each plot. The 100-second-duration data varied as listed in Table 1.

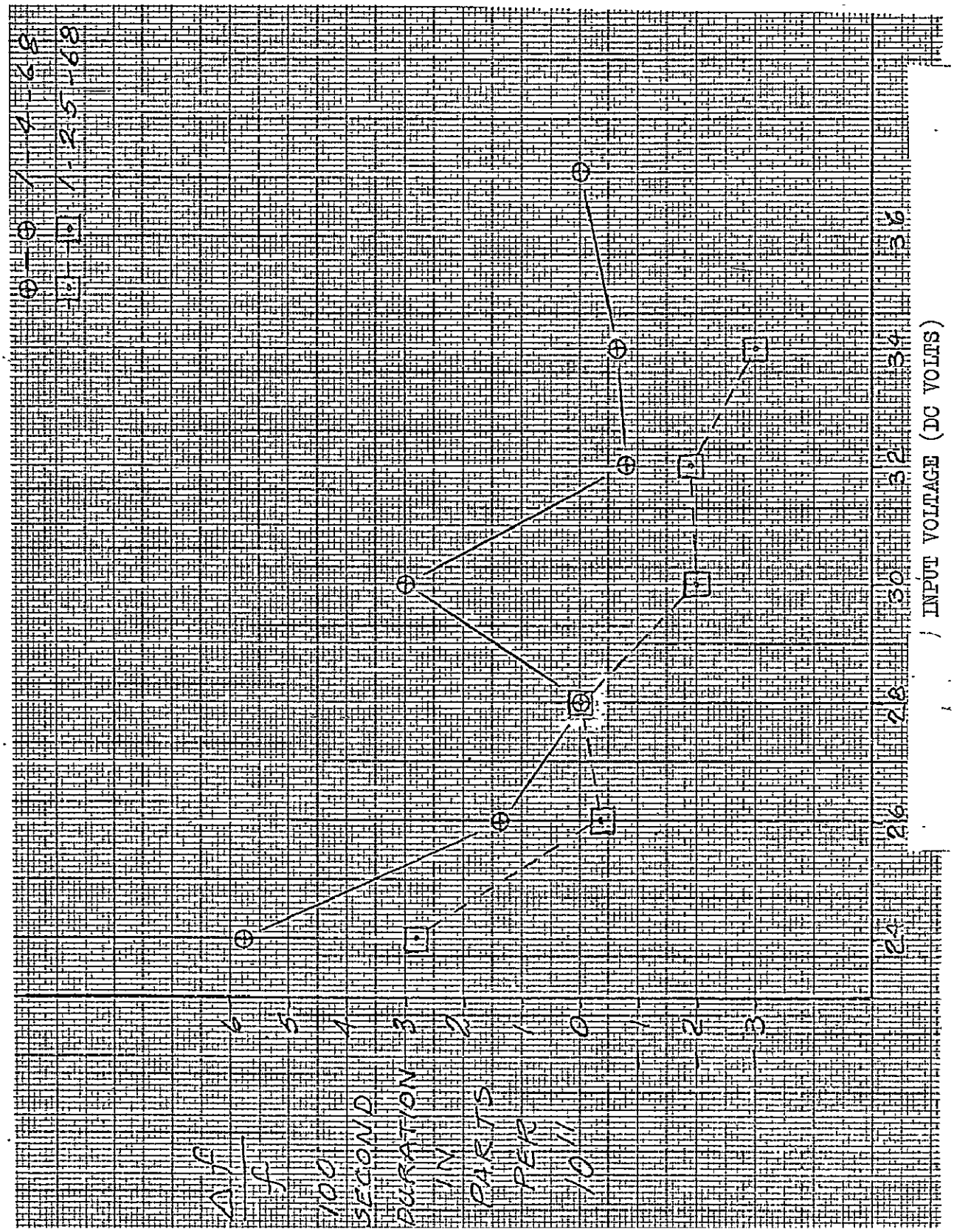


Figure 2. Input Voltage Test, 100-Second Duration Measurements

TABLE 1. INPUT VOLTAGE VS 100-SECOND DURATION MEASUREMENTS

Date	Input Voltage	Period (μSec)	$\Delta f/f$
1-4-68	24	1000.0888	$+5.75 \times 10^{-11}$
	26	1000.0251	$+1.36 \times 10^{-11}$
	28	1000.0054	- -
	30	1000.0485	$+2.98 \times 10^{-11}$
	32	999.9942	-0.77×10^{-11}
	34	999.9960	-0.65×10^{-11}
	37	1000.0054	0
1-25-68	24	999.9341	$+2.82 \times 10^{-11}$
	26	999.8879	-0.37×10^{-11}
	28	999.8932	- -
	30	999.8644	-1.99×10^{-11}
	32	999.8654	-1.91×10^{-11}
	34	999.8495	-3.02×10^{-11}

e. Input Voltage Effect on Short Term Stability

The one-second-duration measurements varied as plotted in Figure 3 and listed in Table 2.

3.2 Temperature Tests

a. First Low-Temperature Test

After 25 minutes at 0 degree F, the SATS 100-kHz synthesizer malfunctioned and disabled the frequency comparison. The

Figure 3. Input Voltage Test 1 -Second Duration Measurements

TABLE 2. INPUT VOLTAGE VS ONE-SECOND DURATION MEASUREMENTS

Date	Input Voltage	$\Delta f/f$
1-4-68	24	0.97×10^{-10}
	26	1.10×10^{-10}
	28	1.11×10^{-10}
	30	0.97×10^{-10}
	32	0.99×10^{-10}
	34	0.98×10^{-10}
	37	0.91×10^{-10}
1-25-68	24	1.05×10^{-10}
	26	0.91×10^{-10}
	28	0.89×10^{-10}
	30	0.91×10^{-10}
	32	1.01×10^{-10}
	34	1.06×10^{-10}

SATS had not reached thermal equilibrium at 0 degree F before malfunctioning. The 100-second-duration measurements obtained at this transition temperature were:

Temperature	Period (μSec)	$\Delta f/f$
76°F	1000.0313	
0°F	999.948	-5.7×10^{-11}

The one-second duration measurements were 3.28×10^{-10} at 76 degrees F and 3.95×10^{-10} at 0 degree F.

b. Second Low-Temperature Test

The SATS operated without fault indication through 80 minutes at 32 degrees F and 80 minutes at 0 degree F. After 20 minutes at -30 degrees F, the 100-kHz synthesizer failed, and the frequency comparator requirement for 100 kHz was supplied from the maser-referenced distribution amplifier. With this exception, the SATS operated without fault indication through 60 minutes at -30 degrees F. The 100-second-duration measurements, plotted on Figure 4, were:

Temperature (°F)	Period (μSec)	$\Delta f/f$
76	1000.0261	
32	999.8354	-1.32×10^{-10}
0	999.7580	-1.94×10^{-10}
-30	999.4258	-4.15×10^{-10}

The rms of the deviations of the one-second-duration measurements varied with temperature as plotted on Figure 5 and listed below:

Temperature (°F)	$\Delta f/f$
76	1.13×10^{-10}
32	1.52×10^{-10}
0	1.46×10^{-10}
-10	1.51×10^{-10}

c. First High-Temperature Test

The SATS lost phase lock before reaching thermal equilibrium after 35 minutes at a chamber temperature of 130 degrees F. The unlock condition did not correct itself until the chamber temperature decreased to ambient. The 100-second-duration measurements, made immediately prior to lock loss, averaged 1000.0076 μsec for $\Delta f/f = 2.04 \times 10^{-10}$. The one-second-duration

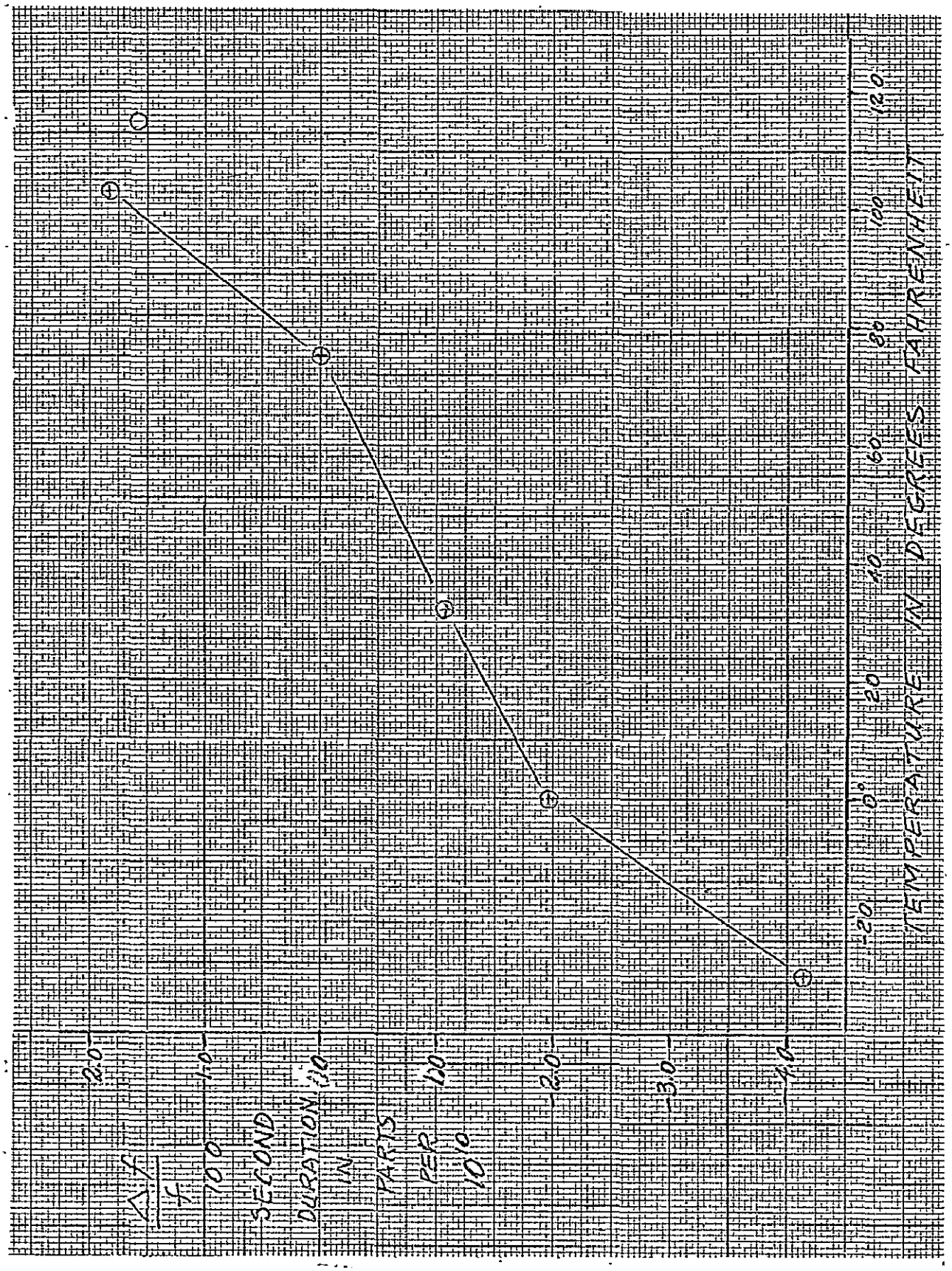


Figure 4. Temperature Test, 100-Second Duration Measurements

Figure 5. Temperature Test, One-Second-Duration Measurements

measurements were 0.89×10^{-10} at ambient temperature and 1.75×10^{-10} just before lock loss.

d. Second High-Temperature Test

A reduced maximum temperature of 115 degrees F was selected for the second test after consideration of the vendor's test results. The SATS lost phase lock after approximately 70 minutes at a chamber temperature of 115 degrees F. The lock loss occurred when the high temperature caused a critical reduction in signal strength from the high frequency multiplier. This evidence and the relatively small mass of the multiplier indicate that thermal equilibrium was not reached at 115 degrees F. The SATS operated without a fault indication for 120 minutes at 103 degrees F after the SATS acquired phase lock while operating at that temperature. The 100-second-duration measurements varied as plotted in Figure 4 and listed below:

Temperature (°F)	Period (μSec)	$\Delta f/f$
76	1000.0231	
103	1000.2716	$+1.79 \times 10^{-10}$
115	1000.2544	$+1.60 \times 10^{-10}$

The one-second-duration measurements varied as plotted in Figure 5 and listed below:

Temperature (°F)	$\Delta f/f$
76	0.90×10^{-10}
103	1.51×10^{-10}
115	2.16×10^{-10}

4. CONCLUSIONS

4.1 Electrical Tests

Changes are required in the dc-to-dc converter to provide reverse-polarity protection and compatibility with positive-going pulses on the input power. Regulation of the power to the temperature-controlling ovens is required to eliminate the input voltage level effect on frequency stability.

4.2 Temperature Tests

The temperature effect on frequency stability is of such magnitude that a complete design study has been started. The 100-kHz synthesizer and high frequency multiplier must be redesigned to permit low and high temperature operation.

SPACECRAFT ATOMIC TIMING SYSTEM
(SATS) DEVELOPMENT

APPENDIX C - TEST EQUIPMENT SPECIFICATIONS

PHASE LOCK LOOP RECEIVER

1. GENERAL

This document presents specifications for a Phase Lock Loop Receiver. The Phase Lock Loop Receiver shall operate as a narrow-band amplifier-filter for the low power, L Band output signal of the Varian Associates Model H-10 hydrogen maser.

2. OPERATING CONDITIONS

2.1 Environment

2.1.1 Temperature: 0 to 50 degrees C.

2.1.2 Relative Humidity: 0 to 100 percent.

2.2 Input Power

2.2.1 Voltage: 28 ($\pm$4) VDC.

2.2.2 Current: No maximum within the limits of standard design practice.

2.3 Packaging

The receiver shall be packaged on chassis which are suitable for slide mounting in a standard 19 inch equipment rack.

2.4 Display

A "lock status" front panel meter shall be provided to permit visual indication of loop performance.

3. INPUT SIGNAL

3.1 Frequency: 1,420, 405, 751.73 (±0.03) Hz

3.2 Power: 2 microvolts RMS developed across 50 ohms.

3.3 Input Connector: Type N coax.

4. OUTPUT SIGNALS

4.1 Frequency: 1450 MHz

4.1.1 Power: 1 milliwatt into 50 ohms.

4.1.2 Stability and Noise Figure: The long term frequency stability and the signal to noise ratio of the 1450 MHz signal shall be equal to or better than the values of the phase lock loop signal which is mixed with the maser input frequency.

4.1.3 Isolation: A minimum of 60 DB isolation shall be provided between the 1450 MHz output and the phase lock loop signal which is mixed with the maser input.

4.2 Frequency: 5 MHz

4.2.1 Power: 1 volt RMS across 50 ohms.

4.2.2 SNR: 85 DB.

4.2.3 Harmonic Distortion: down 40 DB from rated output.

4.3 Frequency: 1 MHz

4.3.1 Power: 1 volt RMS across 50 ohms.

4.3.2 SNR: 85 DB.

4.3.3 Harmonic Distortion: down 40 DB from rated output.

4.4 Frequency: 100 KHz

4.4.1 Power: 1 volt RMS across 50 ohms

4.4.2 Harmonic Distortion: down 40 DB from rated output.

4.5 Output connectors

4.5.1 1450 MHz: Type N coax.

4.5.2 BNC coax bulkhead receptacles.

5. OPEN LOOP OSCILLATOR CHARACTERISTIC

5.1 Short Term Stability

2×10^{-11} for one second averaging time while operating at specified environments and input power.

5.2 Long Term Stability

This parameter is determined by phase lock loop response. The phase detector correction voltage must be capable of maintaining lock for an accumulated oscillator frequency drift over a period of 400 days.

6. LOOP RESPONSE CHARACTERISTICS

6.1 Receiver Noise Figure

11 DB maximum (as presented to input signal).

6.2 Lock Acquisition Time

One millisecond maximum

6.3 Design Considerations

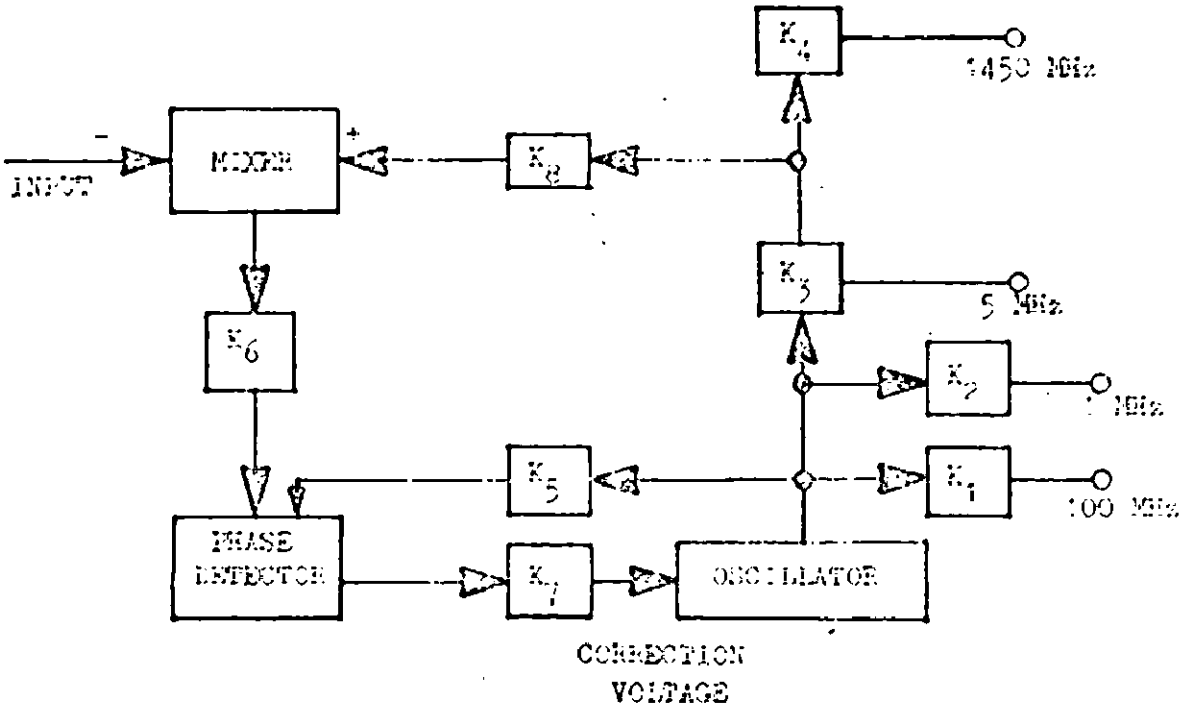
Qualitative requirements for loop response are outlined in Cutler and Searle's "Some Aspects of the Theory and Measurement of Frequency Fluctuations in Frequency Standards," IEEE Proceedings, February, 1966, pages 150 and 151. A high drive level, high frequency crystal oscillator is required. The frequency multiplier, the frequency synthesizer and the mixer-preamp must be carefully selected to minimize their frequency power spectral densities within the loop bandwidth.

7. RELIABILITY

The design and the materials for the phase lock loop are to be chosen so as to ensure maximum operating reliability. The minimum reliability goal is continuous, failure free operation for a period of 100 days.

8. FUNCTIONAL DIAGRAM

The diagram is general and no restrictions on design are to be imposed by any portion of it. In particular, all transfer functions are given a K designation although it is recognized that any individual K-block might represent a frequency multiplier, a filter, an amplifier or some other function.



DISTRIBUTION AMPLIFIER

1. GENERAL

The distribution amplifier shall provide multiple signal outputs for each of three stable frequency, sine wave inputs.

2. OPERATING CONDITIONS

2.1 Temperature: 0 to 50 degrees C.

2.2 Relative Humidity: 0 to 100 percent

2.3 Input Power

Voltage: 28 (±4) VDC
Current: 1.6 amperes maximum

3. INPUT SIGNALS

3.1 Frequency: 5 MHz

Voltage: 1 (±0.25) volts RMS
Input Impedance: 50 ohms or greater

3.2 Frequency: 1 MHz

Voltage: 1 (±0.25) volts RMS
Input Impedance: 50 ohms or greater

3.3 Frequency: 100 KHz

Voltage: 1 (±0.25) volts RMS
Input Impedance: 50 ohms or greater

3.4 Isolation

Each input shall be floating and independent of the other two.

4. OUTPUT SIGNALS

4.1 Number

A minimum of four output signals shall be provided for each input signal.

4.2 Output Signal Level

Adjustable to within 0.5 volts of 4 volts RMS. All output signals from one input shall be adjusted by a single control.

4.3 Noise

Harmonic Distortion: 60 DB below signal level
Spurious: 80 DB below signal level.

4.4 Isolation

Less than 3 percent change in any channel for a short circuit on another channel of the same input signal.

4.5 Stability

The phase fluctuation, for a one second averaging time, between the input and output signals shall be less than 5 parts in 10^{11}. The long-term, one week averaging time, stability shall be essentially zero (not measurable with present techniques).

5. PACKAGING

5.1 Chassis

The unit shall be packaged on a chassis suitable for slide mounting in a standard 19 inch equipment rack.

5.2 Controls and Display

Front panel control and display shall include meters, switches, or other components which provide indication of amplifier performance.

5.3 Connectors

Rear panel BNC coax bulkhead receptacles shall be provided for all input and output signals.

5.4 RELIABILITY

All circuitry shall be solid state components. The design, materials and fabrication techniques for the amplifier shall be selected so as to ensure maximum operating reliability. The minimum reliability goal is continuous, failure free operation for a period of 100 days.

TIME CODE GENERATOR

1. GENERAL

This document presents the specifications for a Time Code Generator. The Time Code Generator shall operate with an ultra stable 1 MHz input signal to provide lower frequency outputs and IRIG time formats. No internal oscillator is required.

2. OPERATING CONDITIONS

2.1 Environment

- Temperature: 0 to 50 degrees C
- Humidity: 0 to 100 percent relative humidity

2.2 Input Power

- Voltage: 28 (±4) VDC
- Current: Maximum: 3.5 amperes

2.3 Packaging

The Time Code Generator shall be packaged on a chassis which is suitable for slide mounting in a standard 19 inch relay rack.

3. INPUT SIGNAL

- Frequency: 1 MHz
- Amplitude: 2 to 10 volt peak-to-peak sine wave
- Time Code Generator Input Impedance: greater than 10 K ohms

. OUTPUT SIGNALS

.1 IRIG B standard time format (DC level shift) with pulse amplitude adjustable from 4 to 8 VDC and space ampltude at ±0.3 VDC. Output impedance: 600 ohms.

.2 IRIG E standard time format (DC level shift) with pulse amplitude adjustable from 4 to 8 VDC and space amplitude at ±0.3 VDC. Output impedance: 600 ohms.

.3 1000 PPS, symmetrical, 0 to 3 volts, output impedance: 100 ohms.

.4 10 PPS, symmetrical, 0 to 3 volts, output impedance: 100 ohms.

.5 1 PPS, symmetrical, 0 to 3 volts, output impedance: 100 ohms.

. VISUAL DISPLAY

The accumulated time shall be visually displayed as seconds, minutes, and days.

. TOTAL ACCUMULATED TIME

Accumulated time storage elements and visual display shall be provided to accommodate a minimum of 399 days.

. PRESET ACCUMULATED TIME

Front panel controls shall be provided to preset the accumulated time storage elements and the visual display to any desired value. Capability for remote control of the preset accumulated time function shall be provided by paralleling the front panel switch connections to a rear panel mounted connector.

8. REMOTE ACCUMULATED TIME INFORMATION OUTPUT

The condition of each data storage element, from tenths of seconds to hundreds of days, in the time accumulator shall be available for remote monitoring. This information shall be provided on a rear panel mounted connector.

9. TIME ADVANCE AND RETARD

Front panel controls shall be provided for advancing or retarding the pulse repetition rate to permit synchronization with a second time code generator. The most sensitive control shall provide for adding and for inhibiting changes of state in the 1 MHz flip flop of the frequency divider network. Less-sensitive controls shall be provided which add or inhibit at rates of 0.1 and 0.01 or 0.125 and 0.0078125 of the most sensitive rate. Capability for remote control of the advance and retard function shall be provided by paralleling the front panel switch connections to a rear panel mounted connector.

10. RESET CAPABILITY

10.1 A single front panel switch shall be provided to reset and maintain all accumulated time storage elements and the display to zero elapsed time. Capability for remote control of the reset function shall be provided by paralleling the switch connections to a rear panel mounted connector.

10.2 A single front panel switch shall be provided to initiate time keeping after reset. Capability for remote control of the initiate function shall be provided by paralleling the switch connections to a rear panel mounted connector.

11. REAR PANEL CONNECTOR

A mating connector shall be provided for the rear panel mounted connector which contains the pins for all remote control functions.

12. RELIABILITY

The design and the material for the time code generator are to be chosen so as to ensure maximum operating reliability. The minimum reliability goal is a continuous failure-free operation for 100 days.

SIGNAL EVALUATOR AND ERROR DETECTOR (SEED)

1. GENERAL

The signal evaluator and error detector shall perform measurements on input signals and shall, when error conditions are detected, generate output signals. Pulse amplitude limit detection, pulse coincidence detection, maximum accumulated time deviation detection, and signal presence monitoring shall be performed. An output signal shall be generated which identified the measurement which has been detected to be in error. Time sequence controlled switching functions shall be generated.

2. OPERATING CONDITIONS

2.1 Environment

2.1.1 Temperature: 0 to 50 degrees C.

2.1.2 Relative Humidity: 0 to 100 percent.

2.2 Input Power

2.2.1 Voltage: 28 (±4) VDC

2.2.2 Current: Not to exceed 650 milliamperes

2.3 Packaging

The unit shall be packaged on a chassis which is suitable for slide mounting in a standard 19 inch relay rack.

3. INPUT SIGNALS

3.1 IRIG E time format (DC level shift), 0 (±0.3) to 5 (±0.5) volt amplitude, required input impedance greater than 10 kilohms.

3.2 Same as 3.1.

3.3 Same as 3.1.

3.4 IRIG B time format (DC level shift), 0 (±0.3) to 5 (±0.5) volt amplitude, required input impedance greater than 10 kilohms.

3.5 Same as 3.4.

3.6 Same as 3.4.

3.7 4096 KHz, square wave, 3 (±0.1) volt amplitude, required input impedance greater than 200 ohms.

3.8 2048 KHz, same conditions as 3.7.

3.9 1024 KHz, same conditions as 3.7.

3.10 512 KHz, same conditions as 3.7.

3.11 100 KHz, same conditions as 3.7.

3.12 1 KHz, same conditions as 3.7.

3.13 100 Hz, same conditions as 3.7,

3.14 10 Hz, same conditions as 3.7.

3.15 1 Hz, same conditions as 3.7.

3.16 1 Hz, square wave, 0 (±0.3) to 5 (±0.5) volt amplitude, required input impedance greater than 10 kilohms.

3.17 Same as 3.16.

4. MEASUREMENTS

Capability shall be provided to perform the following measurements.

4.1 Determination of pulse amplitude:

4.1.1 Limit detection to ensure that each pulse of Signal 3.1 has an amplitude of 5 (±0.5) volts. Zero signal level shall be 0 (±0.3) volt.

4.1.2 Limit detection to ensure that each pulse of Signal 3.4 has an amplitude of 5 (±0.5) volts.

4.2 Time deviation detection shall be performed on the positive-going excursions of the following signal pairs (the maximum permissible time deviation is 1600 +0, -20 microseconds).

4.2.1 Signal 3.15 against 3.16.

4.2.2 Signal 3.15 against 3.17.

4.3 Pulse Comparison of Signal Combinations

The signals shall be compared on a pulse-by-pulse basis so that error detection is performed whenever a pulse appears on only one signal or when the pulse durations are not identical.

The duration detection is necessary because the work marker, the information marker, and the time marker pulses are respectively 8, 5, and 2 time units in duration.

4.3.1 Signals 3.1 and 3.2

4.3.2 Signals 3.1 and 3.3

4.3.3 Signals 3.2 and 3.3

4.3.4 Signals 3.4 and 3.5

4.3.5 Signals 3.4 and 3.6

4.3.6 Signals 3.5 and 3.6

4.4 Signal Presence Monitoring

Capability shall be provided to monitor signals 3.7 through 3.14 to ensure that a signal is present. No particular parameter must be monitored; the requirement is detection of signal failure. Continuous monitoring of each signal is not required; time sharing is permissible with the restriction that equal time shall be allotted to each signal.

5. OUTPUT SIGNALS

5.1 Input Signal Transfer

Input signals 3.1 through 3.17 shall be transmitted as output signals. Signal conditioning shall be provided to transform each output signal to an amplitude of 0 ($\pm$0.3) to 5 ($\pm$0.5) volts across 100 ohms.

5.2 Error Signal Generator

An output shall be generated for each of the following error conditions detected. Each error signal shall be a 5 pps, 0 to 4 volt, square wave.

5.2.1 IRIG E amplitude error (4.1.1)

5.2.2 IRIG B amplitude error (4.1.2)

5.2.3 Time coincidence error (4.2.1)

5.2.4 Time coincidence error (4.2.2)

5.2.5 Pulse comparison error (4.3.1)

5.2.6 Pulse comparison error (4.3.2)

5.2.7 Pulse comparison error (4.3.3)

5.2.8 Pulse comparison error (4.3.4)

5.2.9 Pulse comparison error (4.3.5)

5.2.10 Pulse comparison error (4.3.6)

5.2.11 Loss of signal (4.4)

6. CONTROL AND TIMING FUNCTIONS

6.1 Output Control Function

Error signals generated by ORing groups of output signals shall be utilized to control two switching functions, each operating between a pair of rear panel mounted connector pins. The connector pins and the selected switching technique shall be capable of controlling 300 watts of 115 VAC power. Either relay or solid state switching is permissible. If a relay switch is selected, the design shall provide for transient generation protection by coil suppression diodes and physical isolation. The chassis-enclosed length of each switch line shall be kept to a minimum.

6.2 IRIG "B" Timing Function

Signals 5.2.1, 5.2.8, 5.2.9, 5.2.10 and 5.2.11 shall be ORed to generate a composite error signal which shall be utilized to initiate a timing sequence. The earliest error signal shall close the switch across the first pair of connector pins referred to in 6.1.

6.2.1 3.2 Seconds Time Delay

A 3.2 ($\pm$0.2) second time delay shall be triggered by the arrival of each error signal; this time delay shall be utilized to maintain switch closure.

6.2.2 25 Second Time Delay

The earliest error signal shall trigger a 25 (±2) second time delay. At the completion of the 25 second delay, the switch shall be opened overriding the 3.2 second delay, if necessary. A front panel control shall be provided to permit manual reset of the 25 second delay.

6.2.3 600 Second Time Delay

A 600 (±30) second time delay shall be triggered by the arrival of each error signal. The completion of this delay shall, by generating a reset of the 25 second delay, enable another switch closure cycle.

6.3 IRIG "E" Timing Function

Signals 5.2.2, 5.2.3, 5.2.4, 5.2.5 and 5.2.6 shall be ORed to generate a composite error signal which shall be utilized to initiate a timing sequence. The earliest error signal shall close the switch across the second pair of connector pins referred to in 6.1.

6.3.1 25 Second Time Delay

A 25 (±2) second time delay shall be triggered by the arrival of each error signal; this time delay shall be utilized to maintain switch closure.

6.3.2 200 Seconds Time Delay

The earliest error signal shall trigger a 200 (±20) second time delay. At the completion of the 200 second delay, the switch shall be opened, overriding the 25 second delay if necessary. A front panel control shall be provided to permit manual reset of the 200 second delay.

6.3.3 600 Second Time Delay

A 600 (±30) second time delay shall be triggered by the arrival of each error signal. The completion of this delay shall, by generating a reset of the 200 second delay, enable another switch closure cycle.

7. MATERIALS

7.1 Circuitry

Except for the switching function specified in 6.1, all circuitry shall be solid state components.

7.2 Connectors

Connectors for the input signals specified in paragraph 3 and the output signal specified in paragraph 5 shall be rear-panel mounted BNC bulkhead receptacles. The connector to implement the function of paragraph 6 shall not be specified except that a mating connector shall be provided.

8. RELIABILITY

The design and the materials are to be chosen so as to ensure maximum operating reliability. The minimum reliability goal is continuous, failure free operation for 100 days.