IMPROVEMENT OF SCREENING METHODS FOR SILICON PLANAR DEVICES

QUARTERLY PROGRESS REPORT

1 APRIL 1970 - 30 JUNE 1970

Prepared for

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

MARSHALL SPACE FLIGHT CENTER

by

PHILCO-FORD CORPORATION
MICROELECTRONICS DIVISION

Blue Bell, Pennsylvania

under

CONTRACT NAS12-2197

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HUNTSVILLE, ALABAMA

QUARTERLY PROGRESS REPORT NO. 4

This report describes the studies performed in accordance with Contract NAS12-2197, for the Improvement of Screening Methods for Silicon Planar Devices. The report covers the work performed between 1 April 1970 and 30 June 1970.

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SECTION I - INTRODUCTION

1.1 SCOPE OF REPORT

This report describes the work performed during the period 1 April 1970 through 30 June 1970 on the program Improvement of Screening Methods for Silicon Planar Semiconductor Devices. This program is being conducted for the National Aeronautics and Space Administration's Marshall Space Flight Center at Huntsville, Alabama, under Contract NAS12-2197.

1.2 PROGRAM OBJECTIVES

The purpose of the program is the development of a more sensitive method of selecting silicon planar semiconductor devices for long life applications. The methods developed are to be generally applicable to all types of semiconductor components. The program effort, however, is primarily concerned with the screening of highly time dependent failure mechanisms which are difficult to accelerate to a degree that renders them detectable in a reasonable period of time. The objective of the work is to improve the effectiveness of acceleration methods and/or the sensitivity of detection techniques for failure mechanisms that have been shown capable of escaping the best current practical screens, and ultimately capable of contributing, in a significant way, to system failure.

1.3 PROGRAM APPROACH

Our approach to attaining the objectives of the program is:

a. The development and evaluation of feasible preseal visual and preseal electrical test procedures, supplementing normal in-process screens, which will effectively screen failure mechanisms associated primarily with the semiconductor die and with bonding procedures.

How are these different?

b. The development and evaluation of feasible post seal electrical, mechanical, and thermal test methods which will effectively screen failure mechanisms associated with packaging, thermal stress and packaged device ambient.

c. The correlation of short term test data from sensitive test patterns with long-term-difficult-to-accelerate failure mechanisms of functional devices. The purpose of this is to establish a set of practical short term acceptance criteria, based on measurements of test structures fabricated on the same wafer as the functional devices, and thus to insure the long term reliability of functional devices.

what are these?

what are these?

The utilization of sensitive test patterns permits the acceleration of potential failure mechanisms which would be difficult or impossible to accomplish on complex functional devices within a reasonable period of time. This is because the metallization interconnections prevent the application of sufficiently large stresses to the regions where it is desired to accelerate the degradation that can occur during long term applications of in-use stresses. Secondly, utilization of a standard test pattern will monitor the basic failure mechanisms of any process and identify potential failure mechanisms regardless of device complexity. However, since test patterns can occupy only a finite area on any wafer, they

will determine potential failure mechanisms that are common to an entire wafer or lot, but will not detect localized defects that occur in an area that does not contain the test pattern. Therefore, to insure long term reliability, the test pattern screens developed as a result of this program will be used to supplement the 100% pre- and post-seal visual, electrical, and thermal screens also developed as a result of this contract.

1.4 SUMMARY OF WORK PERFORMED

During the course of this contract both MOS and Bilayer-Bipolar wafers have been fabricated which contain sensitive test patterns liberally interdispersed throughout the wafers. The ratio of test patterns to functional devices on these wafers are one test pattern per 5 functional devices. The MOS test patterns are vehicles whose utility in the determination of basic failure mechanisms had been previously demonstrated and reported by Philco-Ford during the performance of work on the program, "Study of Failure Modes of Multilevel Large Scale Integrated Circuits" for the National Aeronautics and Space Administration's Electronic Research Center, under Contract NAS12-544. The bilayer-bipolar test patterns have been designed and fabricated since the initiation of work on this program. The design of these patterns was based on published data, and conferences between personnel from our Research and Engineering, Production Engineering, and Reliability Groups. These patterns, which are described in detail in Section II of this report, provide test structures for the evaluation of a wide variety of bilayer-metalized-bipolar failure mechanisms.

During this quarterly reporting period, the work performed consisted of:

a. The completion of the Phase I MOS wafer screening measurements and the initiation of the statistical analysis of the resulting data.

b. The completion of the electrical die sort on the Phase I MOS functional devices and the scribing and the assembly of a sufficient quantity of dice, both functional and test pattern structures, from each wafer to obtain the quantities of encapsulated test elements required for Phase I testing.

c. The completion of the preseal visual inspection on the Phase I MOS test vehicles. At the request of NASA/ERC, the location and type of every abnormality observed was manually recorded on a separate sheet for each device. Examples of this data are given in the main body of the report.

d. The completion of the Bilayer-Bipolar masks sets and the initiation of the fabrication of wafers.

e. The initiation of the generation of masks sets for the Phase III test vehicles. These mask sets will contain both functional devices and test patterns.

A detailed description of the items outlined above is contained in Section II of this report.

As in the previous quarterly reports, we include, as an Appendix, a list of the pertinent bibliography that has come to our attention since the preceding report.

SECTION II - FACTUAL DATA

2.0 GENERAL

This section of this report deals with the detailed factual data obtained during the performance of work on this contract during the period 1 April 1970 through 30 June 1970.

2.1 PHASE I, MOS WAFER SCREENS

All of the MOS screening measurements have been completed. These measurements, summarized in Table I, were performed on a total of 22 of the 30 wafers fabricated for this program. The quantity of wafers, from each of the three 10-wafer lots, in which the wafer screening measurements were performed, are summarized below:

Lot No.	Original Lot Size	Wafers Screened	Comments
12-9-47	10	9	1 Wafer given to NASA/ERC and JPL for SEM Evaluation.
13-9-47	10	10	----------
14-9-47	10	3	The metallization pattern on 7 wafers was not row and column aligned, resulting in unusable test patterns, although most of the functional devices were satisfactorily aligned.

Frequency distributions for the Phase I MOS wafer screening measurements have been generated. It is evident from the computer generated distributions that the data taken for some parameters are quite similar and stable regardless of the lot or wafer on which the measurements were taken, or in the case of 300°C drift measurements, the treatment to which the wafer was exposed. Other parameters show a considerable spread or change during 300°C drift measurements. It is the parameters that show spread or change that are most likely to be usable as wafer screening parameters. The parameters which exhibited these effects are summarized in the comments column of Table I. The effectiveness of using these parameters as screens will be evaluated through correlation of the wafer screening data with the data obtained during the subsequent testing of the encapsulated functional devices. The subsequent testing includes normal 100% in-process screening, accelerated screening, and normal operational and environmental testing. The ability to make this type of correlation depends upon retention of the identity of the wafer from which each of the individual devices were obtained, and this will be done.

2.2 SCRIBING AND ASSEMBLY OF MOS VEHICLES

The MOS test vehicles, both the test patterns and the functional devices, have been assembled in sufficient quantities to obtain the number of devices required for Phase I of the MOS program.

Prior to scribing the wafers, the 5R100 devices were subjected to a 100% electrical die sort, which consisted of:

a. A high voltage pulse applied to all inputs and clocks followed by,

b. A D.C. leakage current measurement at all input terminals, all clock input terminals and at the V_{DD} terminal, and

c. A D.C. supply current measurement at both output terminals, and

d. A D.C. R_{ON} measurement at both output terminals, and

e. A 10KHz functional test.

The functional devices which did not meet the requirements of this test were marked and were not assembled.

To insure that both test patterns and functional devices from each of the 22 wafers were included in the encapsulated sample for the Phase I MOS testing, assembly of the chips was performed as indicated below:

Vehicle	Package	Quantity Assembled/Wafer	Bonding Configuration
Test Pattern A	8 lead TO-5 (1-1/2" long leads)	5	Configuration A Figure 1
Test Pattern A	8 lead TO-5 (1-1/2" long leads)	5	Configuration B Figure 2
Test Pattern B	10 lead TO-5 (1/2" long leads)	10	Figure 5
Functional Devices 5R100 Dual 50 Bit Shift Register	10 lead TO-5 (1/2" long leads)	30	Standard Product Assembly Figure 6

The utilization of 1-1/2" long leads on the test pattern "A" packages was required because these devices will be subjected to 300°C drift measurements as part of the accelerated screening to be performed on the encapsulated test vehicles and the only 300°C sockets available require long stemmed packages. The Test Pattern B devices and the 5R100 devices will not be subjected to 300°C electrical testing, and therefore the normal 1/2" long lead packages could be used.

2.3 SEM EVALUATION

The MOS wafer from lot 12-9-47 that was supplied for SEM evaluation was split into two pieces. Scanning electron microscope evaluations were performed by both NASA/ERC under the direction of Mr. T. M. Liimatainen and by JPL, under the direction of Dr. J. Sung. Figures 3 and 4 are reproductions of SEM photomicrographs made by JPL at a magnification of 5700X, and an angle of 65° to the chip surface, prior to and after removal of the top layer passivating glass, of the area indicated by the arrow in Figure 1.

Figure 3 illustrates the typical billowing of the deposited dielectric at the edges of oxide steps and small mounds and depressions in the deposited dielectric. The mounds and depressions are of little significance because the deposited dielectric provides mechanical protection of the metallization and thermal oxide surfaces of the device. Figure 4 shows the same area as Figure 3 after removal of the deposited dielectric, presumably by buffered HF. It should be noted that the deposited dielectric etch also removed a thin layer of the thermal oxide, estimated to be approximately 2000 Å thick from the thickness of the metal stripe, and may have also resulted in the removal of a lesser thickness of the aluminum metallization. The removal of the thermal oxide is exhibited by the thin layer of glass visible between the bottom of the metal stripes and the planar surface of the thermal oxide. The photomicrograph shows, however, more than adequate metal coverage at the oxide step, considering the low current carrying requirements of this MOS device, and a good taper of the oxide step, which minimizes shadowing during aluminum evaporation and results in reliable metallization coverage at steps.

Figures 7 and 8 are SEM photomicrographs taken by JPL of the area indicated by arrow 2 in Figure 5. Figure 7 is the pre-deposited oxide removal view and Figure 8 is the post-deposited oxide removal view. The magnification of both views is 1100X, and both views were made at an angle of 65° to the chip surface. These views illustrate the only difficulty we have experienced with the test patterns. The designed metal to metal separation between the contact metallization for the silicon bottom capacitor plate and the aluminum top capacitor plate was established to meet the minimum design rules for normal metallization widths. However, the metal width at this region is approximately 8 times the normal metal widths, and because of light scattering during the photo resist process, the delineation of the metal is inadequate near the center of the region; there is, however, adequate separation at the edges of the metal, thereby illustrating that if the metal were of the normal width used in functional devices, no difficulties would be experienced, because etching in from both sides would insure adequate separation. During our electrical evaluation of the MOS capacitors on this test element, we observed approximately 20% of the capacitors measured were shorted because of this effect.

Figures 9, 10, 11, and 12 are SEM views of the area indicated by arrow 3 on Figure 1. Figures 9 and 10 were taken by NASA/ERC at an angle of 90° to the chip surface, and at magnifications of 5000X and 7000X, respectively. Figure 9 is prior to deposited oxide removal and Figure 10 is after oxide removal. Figures 11 and 12 are pre- and post-deposited oxide removal photos, taken by JPL at a magnification of 5500X, at an angle of 65° to the chip surface. The dark and light circular areas visible over the metal pattern in Figure 9 are the result of mounds and depressions in the deposited oxide surface, not metallization defects, as can be observed in Figure 10. Figure 11 also shows a relief view of the mounds and depressions in the top glass that are visible in the normal view of Figure 9. Figure 12 shows the tapered edge of the oxide step and the good coverage of the metal across the step. There is also, as was previously discussed, evidence of some thermal oxide removal in this photomicrograph.

Figures 13 and 14 are 2300X SEM views, taken by JPL, at an angle of 65° to the chip, of the area indicated by the arrow in Figure 6. Figure 13 is pre-deposited oxide removal and Figure 14 is post-oxide removal. The area shown is the gate metal of an MOS transistor and the photographs illustrate the good metal coverage and the tapered edge of the oxide step.

2.4 PRE-SEAL VISUAL INSPECTION OF PHASE I MOS VEHICLES

All of the assembled Phase I MOS test vehicles have been subjected to pre-seal visual inspection and have been returned to our production area for encapsulation. Every abnormality observed has been recorded on an individual printed copy of a photomicrograph of the test element, together with the identification the device will retain through all subsequent testing and evaluation. The record of the visual abnormalities will be utilized to correlate any failure incurred with the microscopic observations. Figure 15 is a typical example of the method utilized to record the microscopic pre-seal visual observations.

2.5 BILAYER-BIPOLAR TEST PATTERNS

At the initiation of the work on this contract, meetings and discussions were held between personnel from the Reliability Engineering, Research and Engineering, Circuit Development, and Production Departments to obtain recommendations concerning the individual test structures that should be incorporated into a bipolar-bilayer test pattern. Based on the recommendations obtained during these meetings and information obtained from published literature, [1, 2] test patterns were designed which incorporate the structures that promise to yield the most significant long term reliability information. Because of the number of individual structures required, it was necessary to utilize two separate test patterns to limit the chip to a size that would be satisfactory for a universal test pattern. One of the chip designs contains structures intended for the evaluation of metallization and oxide integrity, and the second chip contains structures intended for the evaluation of bulk and surface effects.

2.6 BILAYER TEST PATTERN, CHIP NUMBER 1

The initially proposed design of the bilayer metallization test pattern, Chip Number 1, is shown in Figure 16. The final metalized product, which contains several minor modifications to the initial design, is shown in Figure 22. These modifications are:

a. The addition of a bottom layer metallization stripe with a minimum number of angle points. This stripe can be utilized to evaluate the effect of angle points on the effective sheet resistance of aluminum by comparing the data obtained from this stripe to the data from the bottom layer metal stripe which contains 18 angle points.

b. The relocation of the metallization and oxide thickness monitoring structure and the addition of metallization to permit the measurement of the thickness of the thermally grown oxide.

c. The modification of the contact resistance stripe to conform to design rules.

d. A slight modification in the areas of both the planar and the interdigitated capacitors to make the metal over metal areas equal.

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1. Barone, F. J. and C. F. Myers - Toward Making LSI Work - Motorola Monitor, 1969.

2. Barone, F. J. and C. F. Myers - Getting Beneath the Surface of Multilayer Integrated Circuits - Electronics, July 22, 1968.

It should be noted that the bonding pads have been made sufficiently large to permit Kelvin connections at all locations where accurate low resistance measurements are required and that all metallization stripes run both horizontally and vertically to permit the evaluation of the shadowing effect that can occur during metallization.

The structures included in the final pattern (see Figure 22), and their purpose are:

Pins 1-13 - A bottom layer metal resistor to monitor the sheet ρ of bottom layer aluminum.

Pins 2-13 - A top layer metal resistor crossing over the oxide steps caused by the bottom layer metal to monitor the effect of the oxide steps on top layer metal resistance.

Pins 3-4 - Two planar plates consisting of bottom and top layer aluminum separated by deposited oxide to evaluate deposited oxide pinhole densities.

Pins 4-7 - Two planar plates consisting of bottom layer aluminum and a "P" diffusion separated by thermally grown borosilicate glass to evaluate pinhole density. The borosilicate dielectric is utilized because it is the thinnest layer in a circuit over which metallization patterns cross.

Pins 5-6 - A top layer aluminum planar plate separated from a bottom layer aluminum comb by deposited oxide to evaluate oxide integrity at the steps in the oxide caused by the bottom layer metal.

Pins 6-7 - The same as 4-7, except the bottom layer aluminum is a comb rather than a planar plate.

Pins 8-13 - A series string of vias to evaluate the integrity of the contacts between top and bottom layer metallization.

Pins 9-13 - A series string of ohmic contacts between bottom layer aluminum and isolated "p" type diffusions to evaluate the integrity of the ohmic contacts. Contacts to "P" region were selected because this is the most difficult contact cut to make since the borosilicate glass (over the "p" diffusions) etch rate is an order of magnitude slower than phosphosilicate glass that is over the emitter and the collector regions during contact cutting. The phosphosilicate glass over the collector contact area results from the N+ doping of that area during emitter diffusion.

Pins 9A-13 - A bottom layer aluminum stripe with a minimum number of angle points to evaluate the effect of current crowding at angles by comparing the resistance value obtained from this stripe with the value obtained from structure 1-13.

Pins 10-11 - A bottom layer aluminum stripe to evaluate the tendency of the stripe to fail because of electromigration. A contact cut to silicon is provided to represent a realistic situation, because all stripes in a functional circuit contact silicon.

Pins 11-12 - A top layer aluminum stripe to evaluate the tendency of the stripe to fail because of electromigration. A via is provided to permit contact with silicon to simulate a realistic circuit configuration.

Pins 13-14 - A bottom layer aluminum stripe over which the deposited glass is removed to evaluate the effect the glass etch has on the sheet ρ of the bottom layer metal. This measurement will be made subsequent to second layer metallization. After second layer metallization, the top layer metal is delineated to be coincident with the bottom layer stripe. The resistance value for the bottom layer stripe will be obtained by an appropriate correction for the additional second layer aluminum thickness.

Pin 14 - Double bonding pads to evaluate the integrity of wire bonds through resistance measurements.

Pins 15-13 - A top layer metal resistor to monitor the sheet ρ of top layer aluminum. A test pattern to monitor metallization and oxide thicknesses with the utilization of microscopic inspection of optical interference patterns obtained with a monochromatic life source.

Oxide and Metallization Thickness Monitor - Located along edge of chip between pads 1 and 2 - This structure is for the use in the determination of metal and oxide thickness.

Photomicrographs of various steps in the fabrication of this test pattern are shown in Figures 17 - 22.

2.7 BIPOLAR TEST PATTERN - CHIP NUMBER 2

The initially proposed design of the bipolar test pattern is shown in Figure 23, and a photomicrograph of the final product is shown in Figure 29. The chip is intended to evaluate bulk and surface effects. Two minor modifications were incorporated into the final design. These modifications to the proposed design include:

a. Re-orientation of the emitter sheet ρ vehicle to minimize shunt resistance.

b. The addition of a substrate ground connection for the "p" channel, enhancement mode MOS transistor.

The structures included in the final design of this chip and their purposes are:

Pins 1-2 - A diffused resistor of the same design width utilized in the functional device to evaluate the effect of variations is the diffusion mask on resistance value.

Pins 3-4-5 - A NPN transistor of the same geometry as the output transistors utilized in the functional device for the comparison of the actual electrical characteristics of the device with the design characteristics.

Pins 6-1 - A diffused resistor for the determination of the sheet ρ of the base diffusion.

Pins 7-1 - A diffused pinch resistor consisting of an emitter diffusion set on top of a base diffusion for the evaluation of base width and r_b'.

Pins 8-1 - A resistor consisting of the buried layer N+ for the evaluation of the extent of out diffusions of the buried layer during subsequent processing steps and the evaluation of the final resistivity of the buried layer.

Pins 9-10-11 - A "p" channel MOS transistor for the evaluation of the tendency of the device to exhibit inversion during operation.

Pins 12-14 - A collector base diode with no buried layer to evaluate the breakdown of the epitaxial material.

Pins 13-14 - A collector base diode with a buried layer to monitor the effect of the buried layer on collector base breakdown.

Pins 14-15 - A large area collector base diode to monitor effect of area on leakage currents.

Pins 16-17-18 - A substrate collector PNP transistor.

Pins 19-21 - A pinch resistor consisting of a base diffusion on top of the epitaxial layer (no buried N+).

Pins 20-21 - An epitaxial resistor to monitor epitaxial layer sheet ρ.

Pins 22-1 - An n type diffused resistor in a p type base diffusion to monitor emitter diffusions sheet ρ .

Pins 23-24-25-26 - A multi-emitter npn transistor of the same geometry as the input transistors of the functional device to monitor parasitic actions and to compare the actual electrical characteristics of the device with the design characteristics.

Pins 14-16 - These pins can be utilized to determine the isolation breakdown voltage of the device.

A. Mask alignment marks to insure adequate alignment of the various diffusion steps. These structures are the rectangular regions located along the two edges of the chip.

B. A checkerboard pattern developed one row at a time during each processing step. This pattern will be utilized as an optical monitor of the accuracy of alignment, diffusion cuts, and metal delineations. Variations in the line formed by the checkerboard will indicate misalignments and variations in the size of the individual blocks will indicate inaccurate diffusion of metallization delineation. This structure is located adjacent to pin 5.

Photomicrographs of various steps in the fabrication of this test pattern are shown in Figures 24 - 29.

2.8 DESCRIPTION OF THE SP0199A, DIGITAL CROSSPOINT QUAD

The Digital Crosspoint Quad (DCQ) is a 2 x 2 array of crosspoints arranged to form a switching matrix. Each crosspoint is bi-directional and includes selection and holding logic. A large square or rectangular matrix, such as required in communcations switching networks, can be formed by the proper arrangement of many DCQ's along the X and Y axis. This particular design is an effective crosspoint element for any switching technique in which the information to be switched is in digital form. Figure 30 shows a logic diagram of the DCQ.

A brief and simplified explanation of the actual operation of one digital crosspoint is as follows: For the purpose of this explanation, refer to Figure 31. The hold and select lines (i.e., X1 hold, X1 select, Y1 hold, Y1 select) are simultaneously actuated by the process of dialing a number and thereby selecting a crosspoint. The select lines may now drop, but the crosspoint is still enabled due to the presence of a hold signal. The caller then "speaks into" an X data in line (X1 data in) and this information is transferred out to the listener on the Y data out line (Y1 data out). The listener then replies to the caller and this reply is transferred in on the Y data in line (Y1 data in). The caller hears the reply on the X data out line (X1 data out). When the conversation is complete, the "phone is hung up" and the hold signal drops; the crosspoint is no longer enabled and it is free to be reselected by another caller. It must be noted that at no time does the crosspoint handle anything but digital information. The transformation of analog information to digital information (and vice-versa) occurs before and after the crosspoint matrix.

The DCQ utilizes transistor-transistor logic (TTL) circuits in a low power circuit configuration, which will interface directly with both series 54/74 and series 54L/74L. Power dissipation is typically 36 milliwatts per chip. A circuit schematic is shown in Figure 32.

The selection and hold mode is accomplished within a typical value of 60 nanosecs. Information can be transferred through the data lines at rates up to 2 megahertz.

This circuit is produced utilizing double layer metallization. The physical configuration of the DCQ is derived from an array consisting of four "basic cells," each cell containing two AOI gates and one NAND gate. This array is designed to be customized by the application of two layers of interconnecting metallization. Photomicrographs of this device during various stages in the fabrication process are shown in Figures 34 - 38.

2.9 ELECTRICAL TEST OF BILAYER-BIPOLAR TEST PATTERNS

All of the electrical tests and the purpose of each test that can be performed on the two bilayer-bipolar test patterns are summarized in Table II. The number and extent to which each one of these tests will be performed will be limited by how effectively the measurements can be automated, and by the significance any given measurement will have in the determination of potential reliability problems. This will be determined by preliminary evaluations.

Historically metallization difficulties have been one of the major problems with bilayer metalized devices, and therefore, we currently intend to make all of the measurements indicated in Table II for Test Pattern 1. It should be noted, however, that the SP0199A and both test patterns utilize a proprietary process for accurately tapering the bottom layer metal and via holes to eliminate abrupt deposited dielectric steps and thereby minimize the possibility of metallization opens at oxide steps resulting from abrupt changes in the topography of the surface under the deposited dielectric or abrupt steps at via holes. The reproducibility of the tapering process is illustrated in Figures 39 and 40. If, during the early measurement of the test structures of Test Pattern Number 1, we do not observe indications of potential metallization reliability problems, the number of measurements made on subsequent test patterns will be reduced.

Concerning Test Pattern 2, we intend to make a sufficient number of measurements to characterize each test structure. After the characterization of each structure, the measurements of those structures which do not indicate significant variation between wafers and/or lots, will be discontinued.

2.10 STATUS OF BILAYER-BIPOLAR WAFERS

Bilayer-Bipolar wafers have been partially fabricated. We are now initiating electrical die sort on the functional devices. The performance of the electrical die sort measurement prior to the electrical wafer screening measurments is a deviation from the approach taken during the MOS portion of the program where the wafer screening measurements were made prior to electrical die sort of the 5R100 functional devices. The reason for the deviation in procedure is that the yields on the SP0199A, a fairly complex device, are relatively low and we want to be sure that we obtain a sufficient number of good functional devices from each wafer to justify the amount of time and effort required to make the electrical wafer screening measurement. The yields that we have experienced on the bilayer-bipolar wafers thus far die sorted, indicate that there will probably be a further delay in this portion of the program.

2.11 PHASE III MOS VEHICLES:

The masking required for the generation of the Phase III MOS Test Vehicles has been initiated. The Phase III function test vehicle will be the P2000, an MOS Dual 50 Bit Shift Register, fabricated according to the regrown IIT process. This process results in thicker oxide over the "p" diffused regions, and thereby improves the product because:

a. The 'p'-'n' junctions surrounding the gate metal are covered with the thicker oxide minimizing the possibility of gate metal to silicon shorts at the high electric field points located at the edge of the gate metal.

b. All metalization busses (i.e., clock lines, V_{DD} lines) cross over the thicker oxide minimizing the possibility of parasitic transistor action and the possibility of shorts through the oxide.

The P2000 also utilizes improved input protection devices. These were described in Progress Letter No. 6.

Regrown IIT versions of the test patterns utilized on the Phase I MOS wafers will also be included on each Phase III wafer in the same manner they were on the Phase I wafers.

SECTION III - FUTURE ACTION

3.0 GENERAL

The work planned for the next quarter for both the MOS and the bilayer-bipolar phases of this contract is described in the subsequent paragraphs of this section of this report. It should be noted that the next quarter contains the annual company vacation and that no effort will be expended during this period, the last two weeks of July.

3.1 PHASE I, MOS EFFORTS

During the next quarter we intend to complete the 100% in-process screens on the encapsulated Phase I MOS vehicles.

The 100% in-process screens consist of:

a. Stabilization Bake - 16 hours at 150°C.

b. Temperature Cycling - 10 cycles from -55°C to +150°C.

c. Pneupactor Shock Test - 1 blow, Y1 plane, 25K "G".

d. Hermeticity Testing -

1. Helium Fine Leak.

2. Freon Bubble Gross Leak.

e. Final Electrical Test.

Upon completion of the 100% in-process screening tests, the functional devices and the test patterns will be subjected to additional testing to aid in the determination of accelerated screens.

Also, per the request of Mr. T. M. Liimatainen, at the contract status review meeting held at Blue Bell on the 10 and 11 of June, we will perform a radiographic inspection of the Phase I MOS devices to ascertain if the pre-seal visual inspection criteria for eutetic flow is sufficient to insure the integrity of the chip to header bond. The initial radiographic inspection will be on a sampling basis, however, if the sample fails the criteria yet to be established, we will perform a 100% inspection. We will also make some modifications to the MOS pre-seal visual inspection criteria, and obtain reproductions of photomicrographs of the typical visual defects observed during our pre-seal visual inspection of the Phase I MOS vehicles. These modifications and photomicrographs were requested by Mr. T. M. Liimatainen, NASA/ERC and Dr. J. Sung, JPL, during our review of the criteria at the June contract review meeting.

We will also initiate the infrared scanning of internal lead wires and chip to header bonds as described in our proposal. The purpose of this effort is to demonstrate the effectiveness of the infrared techniques in determining the integrity of chip to header bonds and to extend the knowledge obtained by Philco-Ford (during work for the Marshall Space Flight Center under Contract NAS8-21219, The Study of Infrared Evaluation in Qualification and Failure Analysis of Semiconductor Devices) concerning the non-destructive determination of inferior wire bonds through the utilization of infrared determined temperature gradients between the bonded wire and a point on the bonding surface immediately adjacent to the bond.

3.2 BILAYER-BIPOLAR EFFORTS

During the next quarter we intend to obtain all of the bilayer-bipolar wafers necessary to assemble the bipolar-bilayer vehicles required by this contract. We also intend to complete the wafer screening, and the pre-seal visual inspection on these devices, and encapsulate the necessary quantity of test vehicles.

3.3 PHASE III MOS DEVICES

During the next quarter, we intend to complete the masking of the Phase III MOS test vehicles and initiate the fabrication of the wafers required for this portion of the contract.

TABLE I

ELECTRICAL AND VISUAL MEASUREMENTS ON MOS WAFERS

TABLE I - ELECTRICAL & VISUAL MEASUREMENTS ON MOS WAFERS

MOS TEST PATTERN A

Test Structure	Description	Measurements	Measurements/Wafer	Comments
1	MOS Capacitor over Field Oxide	Flat Band Voltage		
		a. Initially.	4 locations on wafers 1,2,& 3 of all lots.	Data quite tight and consistent within lots & relatively tight & consistent between lots.
		b. After 300°C, +36V, 12 min. drifting.	4 locations on wafers 1,2,& 3 of all lots. 12 locations on wafer 4, lots 1 & 2. 2 locations on all other wafers.	Distribution normal, range is tight, values show general increase over pre-drift measurement.
		c. After 300°C, 0V, 12 min. drifting.	4 locations on wafers 1,2,& 3 of all lots. 12 locations on wafer 4 of lots 1 & 2.	Data shows that structures return to their original-pre-drifting-condition.
		d. After 300°C, -36V, 12 min. drifting	4 locations on wafers 1,2,& 3 of all lots. 12 locations on wafer 4 of lots 1 & 2. 2 locations on all other wafers.	Distribution of values show considerable spread & general decrease from pre-drift measurement.
2	MOS Capacitor over Gate Oxide	Flat Band Voltage		
		a. Initially	4 locations on wafers 1,2,& 3 of all lots.	Distributions of values quite tight.
		b. After 300°C, +12V, 12 min. drifting.	4 locations on wafers 1,2,& 3 of all lots.	Distributions of values tight.
		c. After 300°C, 0V, 12 min. drifting.	4 locations on wafers 1,2,& 3 of all lots.	Distributions of values very similar to initial values.
		d. After 300°C, -12V, 12 min. drifting.	4 locations on wafers 1,2,& 3 of all lots.	Distribution of values show most spread of all measurements made on this structure.

TABLE I - ELECTRICAL & VISUAL MEASUREMENTS ON MOS WAFERS (Cont'd.)

MOS TEST PATTERN A (Cont'd.)

Test Structure	Description	Measurements	Measurements/Wafer	Comments
3	Large area p-n junction diode	Reverse leakage at 20 V & reverse breakdown at 10 μA	4 locations on all wafers of all lots except 12 locations were measured on wafer 4 of lots 1 & 2.	Distributions show some lot to lot variation.
4	Lateral Diffusion Vehicle	Punch through voltage for each designed separation.	4 locations on wafers 1,2,& 3 of all lots.	Data shows considerable shorting of 0.1 mil separation structures.
5	Gate Controlled Diode	Surface recombination velocity.	4 locations on wafers 1,2,& 3 of all lots. 12 locations on wafer 4 of lots 1 & 2.	Distribution of values normal.
6	Field Oxide MOS transistor	V_{GST} at 10 μA I_{DS} V_{GDT} at 10 μA I_{DS}	4 locations on wafers 1,2,& 3 of all lots. 4 locations on wafers 1,2,& 3 of all lots.	Distribution of values are tightly grouped & indicate symmetry of device.
7	Gate Oxide MOS Transistor	V_{GST} at 10 μA I_{DS} V_{GDT} at 10 μA I_{DS} V_{GST} at 10 μA after 300°C, -12V drifting. V_{GST} at 10 μA after 300°C, +12V drifting.	4 locations on wafers 1,2,& 3 of all lots. 12 locations on wafer 4 of lots 1&2. 4 locations on wafers 1,2,& 3 of all lots. 2 locations on wafers 5-10 lot 1 & 5-9, lot 2. 2 locations on wafers 5-10, lot 1 & 5-9, lot 2.	Distribution of values are tightly grouped & distribution is very similar to V_{GDT} distribution. See Comment above. Distribution of values are tightly grouped & similar to V_{GST} distribution w/o drifting Values show some increase due to positive drifing.
8	Lateral Bipolar Transistor	h_{fe} at 5V_{CE} & 5μAI_C	4 locations on wafers 1,2,& 3 of all lots.	Distribution of values tightly grouped and normal.

TABLE I - ELECTRICAL & VISUAL MEASUREMENTS ON MOS WAFERS (Cont'd.)

MOS TEST PATTERN B

Test Structure	Description	Measurements	Measurements/Wafer	Comments
1	Aluminum Stripe	Resistance @ 1mA Line width (visual)	4 locations on all wafers of all lots. 4 locations on wafers 1,2,& 3 of all lots. 2 locations on all other wafers.	Resistance values exhibit a normal distribution. Line width distributions are tight.
2	Diffused P Type Resistor	Resistance @ 100μA Line width (visual)	4 locations on all wafers of all lots. 4 locations on wafers 1,2,& 3 of all lots. 2 locations on all other wafers.	Resistance values exhibit a normal distribution. Line width distributions are tight.
3	Contact Resistance String	Resistance @ 100μA Line width & Contact Cut alignment (visual)	4 locations on all wafers of all lots. 4 locations on wafers 1,2,& 3 of all lots 2 locations on all other wafers.	Resistance values exhibit a normal distribution. No alignment difficulties.
4	Metal Step Down String	Resistance @ 1 mA Metal neck down at oxide steps (visual)	4 locations on all wafers of all lots. 4 locations on wafers 1,2,& 3 of all lots. 2 locations on all other wafers.	Resistance values exhibit a normal distribution No neck down difficulties.
5	Metal & Oxide Thickness Monitor	Metal thickness (visual) Gate oxide thickness(visual) Field oxide thickness (")	1 location on all wafers of all lots. 1 location on all wafers of all lots. 1 location on all wafers of all lots.	Distributions of thickness are tight for all measured values-some measurements could not be made because roughness of metal surface made measurement impossible.
6,7,8,9	MOS Capacitors over Various Oxide Surfaces	Oxide breakdown voltage	4 locations on all wafers	Distribution of voltages show considerable spread, except for Structure 7. Some capacitor structures are initially shorted because of bridged metal.

TABLE I - ELECTRICAL & VISUAL MEASUREMENTS ON MOS WAFERS (Cont'd.)

MOS TEST PATTERN B

Test Structure	Description	Measurements	Measurements/Wafer	Comments
--	Metal at Bonding Pads	Grain size	1 location on wafers 1,2,& 3 of all lots.	Measurement highly subjective & time consuming, and therefore discontinued.
--	Interference Contrast Scan of Entire Wafer	Residual photoresist & oxide thickness variations & crystaline defect density.	Wafers 1,2,& 3 of all lots	No evidence of residual photoresist, variations in oxide thickness, or crystaline defects.
--	High Power Magnification Observation of Corner of Individual Chip.	Oxide pinhole density.	1 location on all wafers of all lots.	Differentiation between thermal & passivation oxide pinholes impossible.
--	High Power Magnification Observation In Glass Free Scribe Lines	Boron Pitting Density	1 location on all wafers of all lots.	Pitting density on several wafers higher than majority of wafers.

FUNCTIONAL DEVICE - 5R100

--	MOS Test Transistor	Contact cut size and alignment. Alignment of Gate Metal.	4 locations on wafers 1,2,& 3 of all lots. 2 locations on all other wafers	No difficulties observed.

TABLE II

- SUMMARY -

INDIVIDUAL BILAYER-BIPOLAR TEST STRUCTURES, APPLIED TEST CONDITIONS, AND FAILURE MECHANISMS THAT EACH STRUCTURE WILL DETECT.

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INDIVIDUAL BILAYER-BIPOLAR TEST STRUCTURES, APPLIED TEST CONDITIONS, AND FAILURE MECHANISMS THAT EACH STRUCTURE WILL DETECT

TEST PATTERN 1 (See Figure 22)

Structure No.	Test Condition	Detectable Failure Mechanisms
1. Pins 1-13 Bottom layer Al stripe.	Measure voltage drop along stripe at current of 1 mA. Calculate sheet ρ of Aluminum.	High sheet ρ resulting from contamination, high temperature alloying, layer thickness, or excessive undercutting of photoresist.
2. Pins 2-13 Top layer Al stripe over oxide steps caused by bottom layer metal.	" " "	High effective sheet ρ resulting from notches, microcracks, tunnels, or shadowing of the metal at oxide steps.
3. Pins 8-13 Series string of vias between top and bottom layer metalization.	" " "	High effective sheet ρ resulting from insufficient via cross section or inadequate contact between metal layers.
4. Pins 9-13 Series string of ohmic contacts between "p" diffusions and bottom layer Al.	Measure voltage drop along structure at current of 100 μA.	High resistance resulting from poor ohmic contact or metal thinning at oxide steps.
5. Pins 9A - 13 Bottom layer Al with a minimum number of bends.	Measure voltage drop along stripe at current of 1 mA. Calculate sheet ρ.	Compare data with data from Structure 1 to determine affect of metalization bends on effective sheet ρ.
6. Pins 10-11 Bottom layer Al electromigration stripe. Pins 10-12 Top layer Al electromigration stripe.	Conditions to be determined.	Rate and location of electromigration of aluminum.
7. Pins 13-14 Bottom layer Al stripe.	Measure voltage drop along stripe at current of 1 mA after 2nd layer metal evaporation, make appropriate correction for conductivity contributed by 2nd layer metal. Calculate sheet ρ.	Compare data with test Structure 1 to determine extent of metal removal during glass etch.

Table II (Cont'd.)

Structure No.	Test Condition	Detectable Failure Mechanisms
8. Pins 13-16 Bottom layer Al stripe over deep thermal oxide cuts.	Measure voltage drop along stripe at current of 1 mA. Calculate sheet ρ .	High sheet ρ resulting from notches, microcracks, tunnels, or shadowing at oxide steps.
9. Pins 15-16 Top layer Al stripe.	Measure voltage drop along stripe at current of 1 mA. Calculate sheet ρ .	High sheet ρ resulting from contamination, high temperature alloying, or layer thickness.
10. Pins 3-4 Planar Al plates separated by deposited dielectric.	Measure oxide breakdown voltage,	Shorts through deposited dielectric.
11. Pins 5-6 Top layer planar plate separated from bottom layer Al comb by deposited dielectric.	" " "	Shorts through deposited dielectric. Comparison of data with that obtained from Structure of Item 10 will yield estimate of shorts at metalization periphery.
12. Pins 4-7 Bottom layer Al planar plate separated from "p" diffusion by thermally grown borosilicate.	" " "	Shorts through borosilicate glass. (Thinnest glass in device.)
13. Pins 6-7 Bottom layer Al comb separated from "p" diffusion by thermally grown borosilicate.	" " "	Shorts through borosilicate glass. Comparison of data with that obtained from Structure of Item 12 will yield estimate of shorts at metalization periphery.
14. Pin 14 Double bonding pad for bond attachment.	Measure resistance (from external package terminals) at current of 1 mA.	High resistance indicative of poor wire bonds at the chip or package.
15. Oxide & Metalization Thickness Monitor.	Measure oxide and metalization thickness with Nomarski Polarization Interferometer.	Inadequate control over oxide & metalization thicknesses.

TABLE II (Cont'd.)

CHIP NUMBER 2 (See Figure 29)

Structure No.	Test Condition	Detectable Failure Mechanisms
1. Pins 1-2 Narrow, diffused "p" type resistor.	Determine resistance at current level of 10 μA. Pin 2 = V^+ Pin 1 = Gnd.	Marginal resistance values caused by variations in sheet ρ, resistor width, localized breakdown and resulting in marginal circuit performance over its specified temperature range.
2. Pins 3, 4, 5 NPN Bipolar Transistor	Measure: h_{FE}, V_{SAT}, I_{CEO} } Conditions to be determined. Pin 1 must be at gnd.	Marginal circuit performance because of improper diffusion delineation, bulk properties, or alignment.
3. Pins 6-1 Wide, diffused "p" type resistor.	Measure resistance at current level of 10 μA. Determine sheet ρ.	Utilize data in conjunction with data from test Structure 1 to determine reasons for resistance variations.
4. Pins 7-1 Pinch resistor formed by base and emitter diffusion.	Measure resistance at current level of 10 μA.	Utilize data in conjunction with data from structures 3 and 13 to determine base widths.
5. Pins 8-1 Buried n+ resistor.	Measure resistance at current level of 1 mA. Determine sheet ρ.	Determine extent of out diffusion on n+ during subsequent processing.
6. Pins 9, 10, 11 P channel, enhancement mode MOS transistor.	Measure V_{GST} & V_{GDT} I_{DS} = 10 μA.	Charge density in the oxide, or instability of the oxide layer if electrical measurements are made prior and subsequent to high temp. reverse bias operation.
7. Pins 12-14 Collector base diode (No buried n+).	Measure reverse current (I_R) at V_R = 20V - Measure reverse breakdown at 10 μA.	Leakage current, a significant cause for failure in bipolar circuits. Structure will also evaluate breakdown of epitaxial material.
8. Pins 13-14 Collector Base Diode (with buried n+).	Same as Structure 7	Leakage current, a significant cause for failure in bipolar circuits, Structure will also evaluate effect of n+ layer on collector base breakdown.
9. Pins 14-15 Large periphery Collector base diode.	Same as Structure 7	Leakage current, a significant cause for failure in bipolar circuits. The large areas involved in this structure make it a more sensitive vehicle for the determination of the extent of leakage current increases.
10. Pins 16, 17, 18 Substrate collector PNP Bipolar Transistor.	To be determined	This type of structure is used on some linear microcircuits and can be used to evaluate the electrical characteristics of such devices.

TABLE II (Cont'd.)

Structure No.	Test Condition	Detectable Failure Mechanisms
11. Pins 19-21 Wide pinch resistor formed by epitaxial n type & p type base material.	Measure resistance at 10 μA. Determine sheet ρ .	Provides information about the base substrate spacing, (a factor in collector breakdown.)
12. Pins 20-21 Wide, n type epitaxial material resistor.	Measure resistance at 10 μA.	Determine effect of epitaxial material resistivity on transistor V_{SAT} and collector breakdown.
13. Pins 22-1 n+ type resistor	Measure resistance at 1 mA. Determine sheet ρ .	Improper n+ resistor values or high n+ underpass values caused by variations in sheet ρ , diffusion widths, or localized breakdown resulting in marginal circuit performances.
14. Pins 23,24,25,26 Multi-emitter NPN Bipolar Transistor.	Measure: h_{FE} - single transistor V_{SAT} " " I_{CRO} " " Emitter to Emitter leakage. All of above - Conditions to be determined.	Determine bulk interactions which can result in degradation of electrical characteristics of functional devices.
15. Pins 14-16 Isolation Diode.	Measure isolation breakdown.	Determine if localized imperfections or improper resistivities can result in premature isolation breakdown.
16. A Mask Alignment Marks	Observe microscopically	Aid to the observation of misalignments which can result in failure.
17. B Optical Monitor for process step alignments.	Observe microscopically	Aid to the observation of misalignments and photolithographic errors that can lead to device failure.

Pin 4 is Substrate Ground

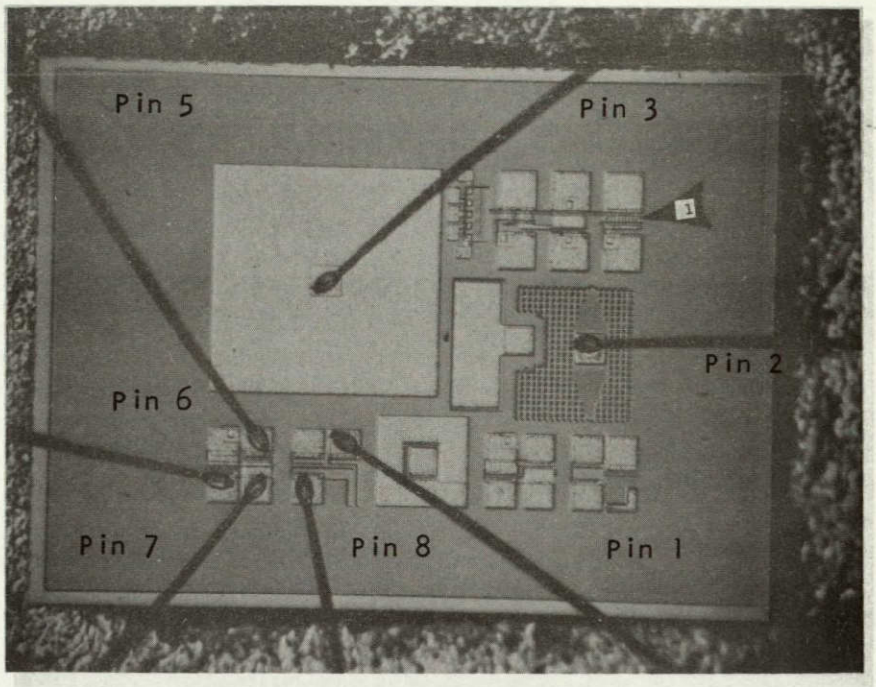


FIGURE 1 - PHOTOMICROGRAPH OF MOS TEST PATTERN "A", SHOWING BONDING CONFIGURATION A AND LOCATION OF SEM PHOTOMICROGRAPHS OF FIGURES 3 AND 4.

Pin 4 is Substrate Ground

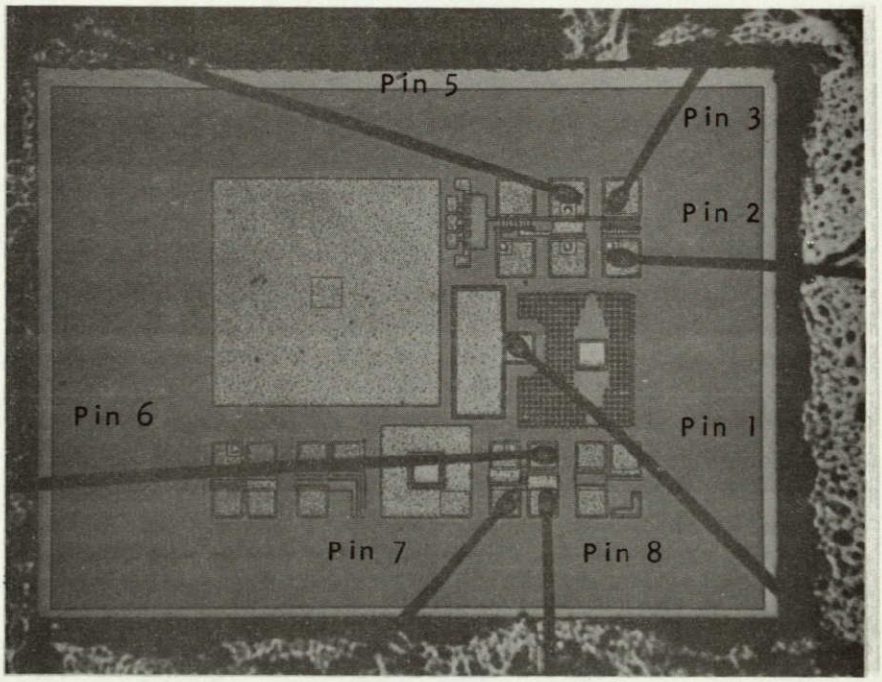


FIGURE 2 - PHOTOMICROGRAPH OF MOS TEST PATTERN "A", SHOWING BONDING CONFIGURATION "B".

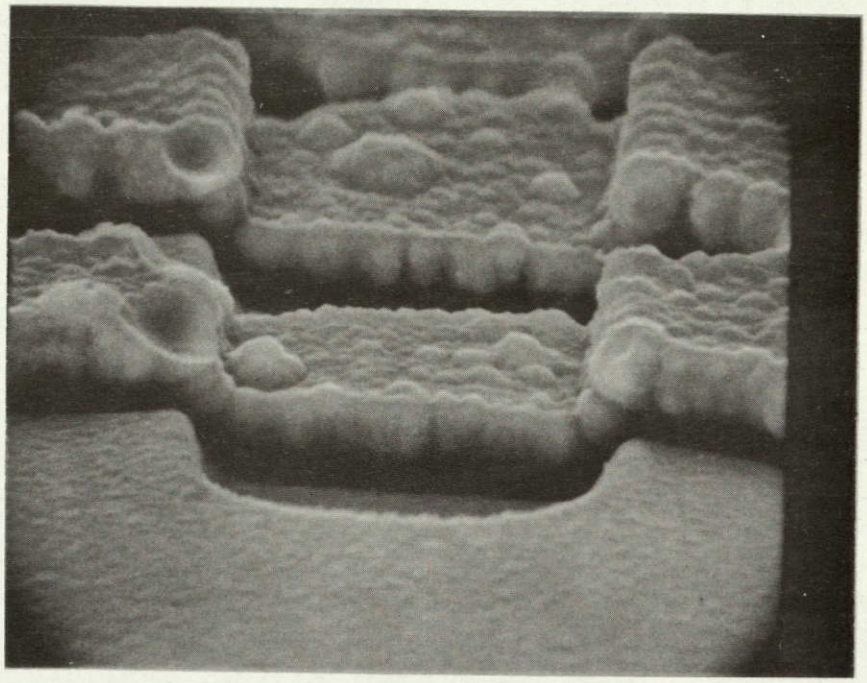


FIGURE 3 - SEM PHOTOMICROGRAPH, PRIOR TO DEPOSITED DIELECTRIC REMOVAL, OF AREA INDICATED BY ARROW IN FIGURE 1. BILLOWING OF DEPOSITED DIELECTRIC IS VISIBLE ON TOP OF METAL WHERE METAL STEPS INTO OXIDE CUTS. MOUNDS & DEPRESSIONS IN THE DEPOSITED DIELECTRIC ARE ALSO VISIBLE. (MAG. = 5700X, ANGLE = 65°)

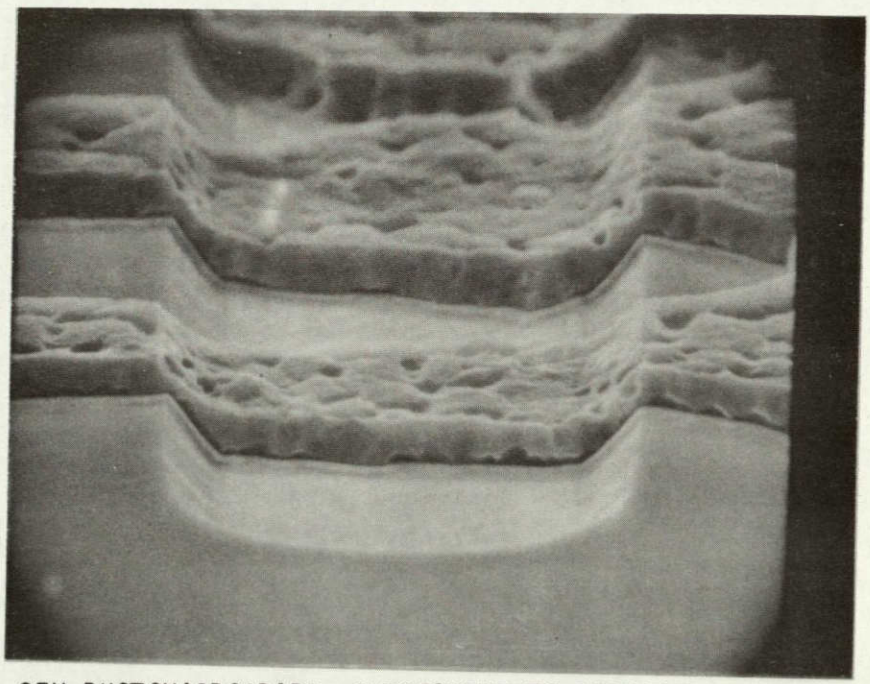


FIGURE 4 - SEM PHOTOMICROGRAPH, SUBSEQUENT TO DEPOSITED OXIDE REMOVAL, OF SAME AREA SHOWN IN FIGURE 3. GOOD METALLIZATION COVERAGE AT TAPERED OXIDE STEP IS VISIBLE. THIN LAYER VISIBLE UNDER METAL STRIPES INDICATES SOME THERMAL OXIDE REMOVAL DURING DEPOSITED OXIDE ETCH. (MAG. = 5700X, ANGLE = 65°)

Pin 5 is Substrate Ground

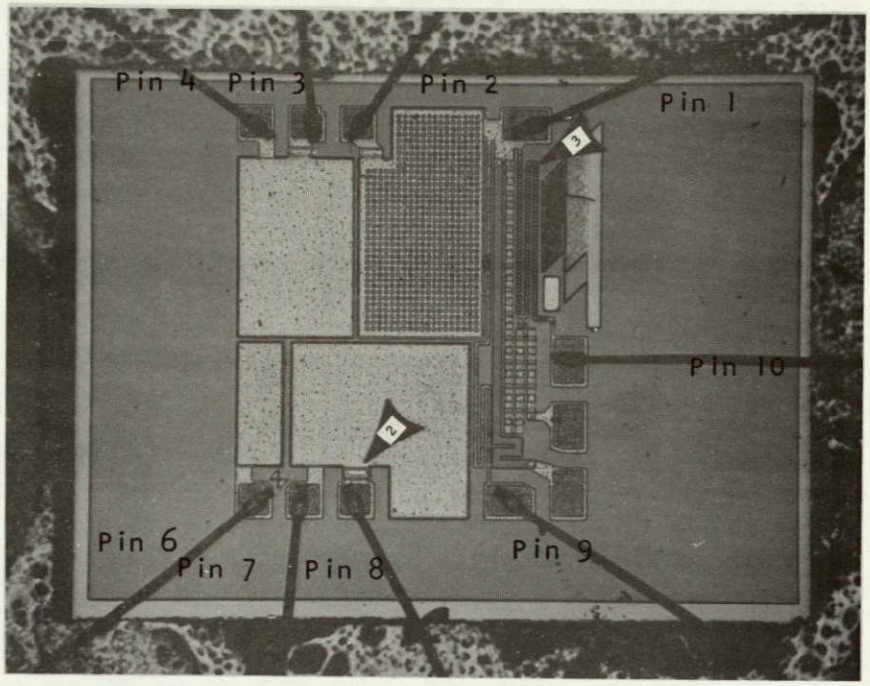


FIGURE 5 - PHOTOMICROGRAPH OF MOS TEST PATTERN "B", SHOWING BONDING CONFIGURATION AND LOCATION OF SEM PHOTOMICROGRAPHS OF FIGURES 7, 8, 9 AND 10.

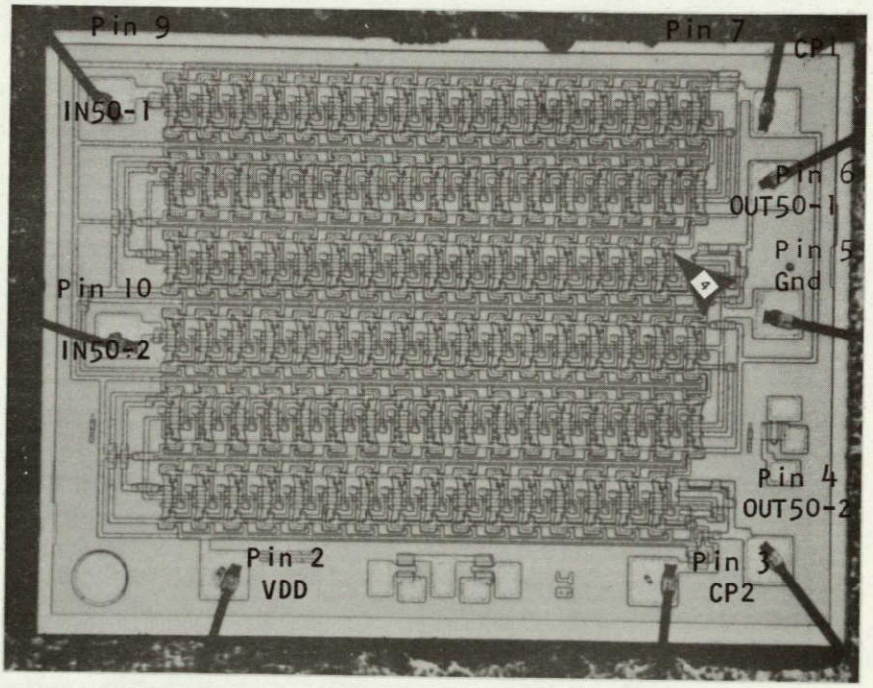


FIGURE 6 - PHOTOMICROGRAPH OF MOS 5R100 DUAL 50 BIT SHIFT REGISTER, SHOWING BONDING CONFIGURATION AND LOCATION OF SEM PHOTOMICROGRAPHS OF FIGURES 11 AND 12.

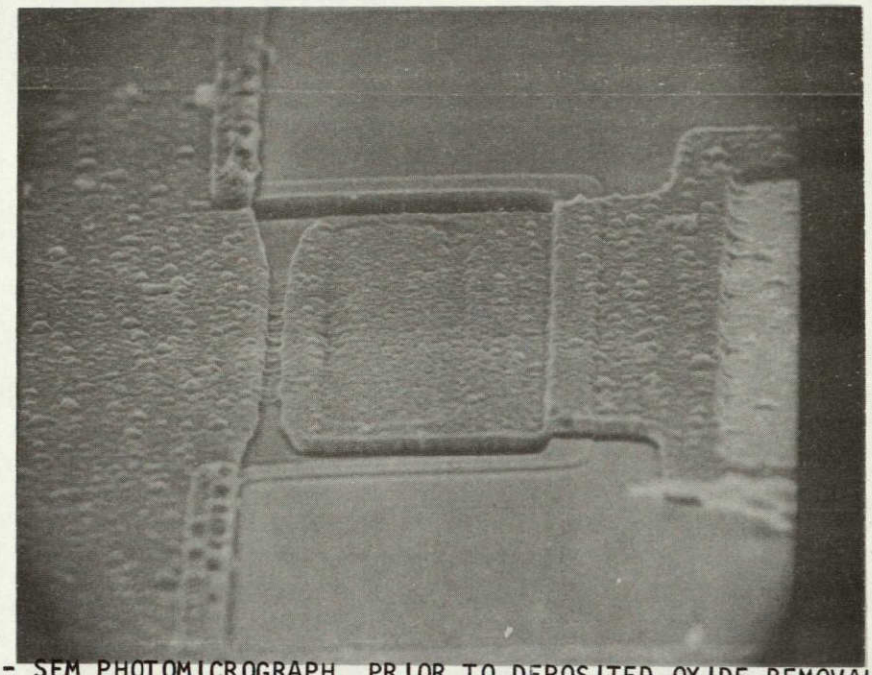


FIGURE 7 - SEM PHOTOMICROGRAPH, PRIOR TO DEPOSITED OXIDE REMOVAL, OF AREA INDICATED BY ARROW 2 OF FIGURE 5. PHOTOMICROGRAPH SHOWS BRIDGING OF METALLIZATION PATTERN. (MAG. = 1100X, ANGLE = 65°)

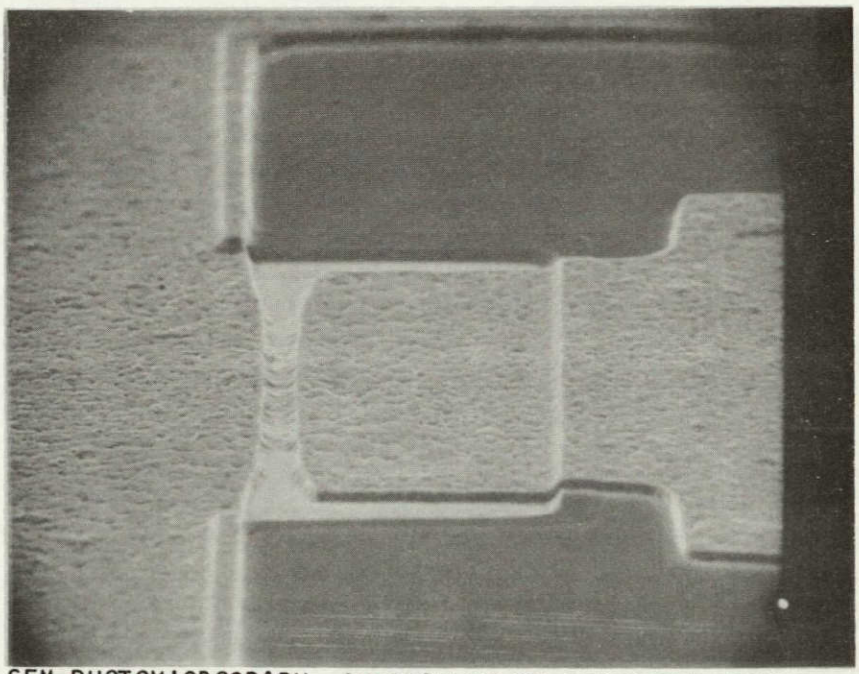


FIGURE 8 - SEM PHOTOMICROGRAPH, SUBSEQUENT TO DEPOSITED OXIDE REMOVAL, OF SAME AREA SHOWN IN FIGURE 7. (MAG. = 5700X, ANGLE = 65°)

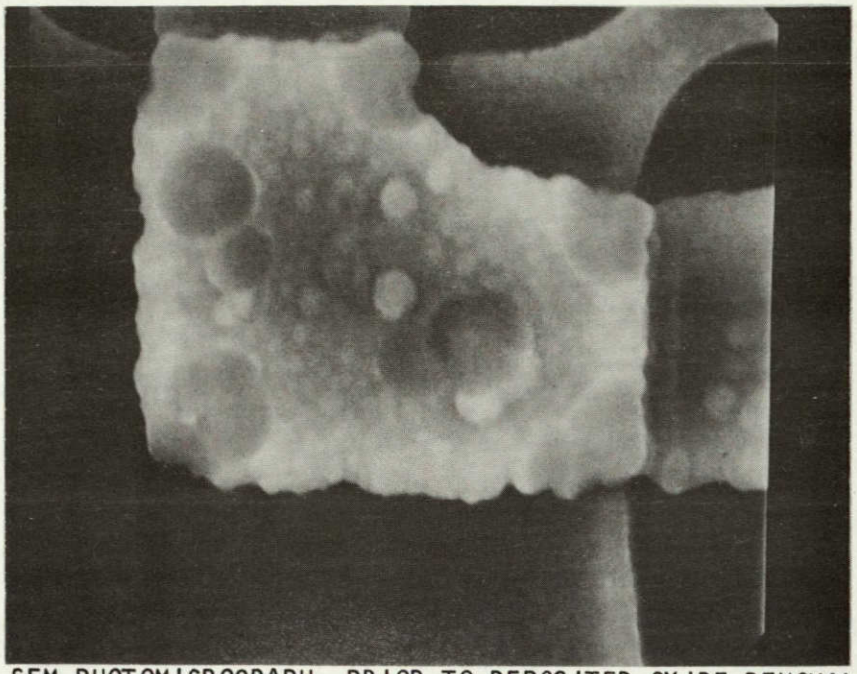


FIGURE 9 - SEM PHOTOMICROGRAPH, PRIOR TO DEPOSITED OXIDE REMOVAL, OF AREA INDICATED BY ARROW 3 OF FIGURE 5. DARK AND LIGHT CIRCLES IN AREA OVER METAL STRIPE ARE THE RESULT OF MOUNDS AND DEPRESSIONS IN THE DEPOSITED OXIDE AND DO NOT AFFECT RELIABILITY OF DEVICE.
(MAG. = 5000X, ANGLE = 90°)

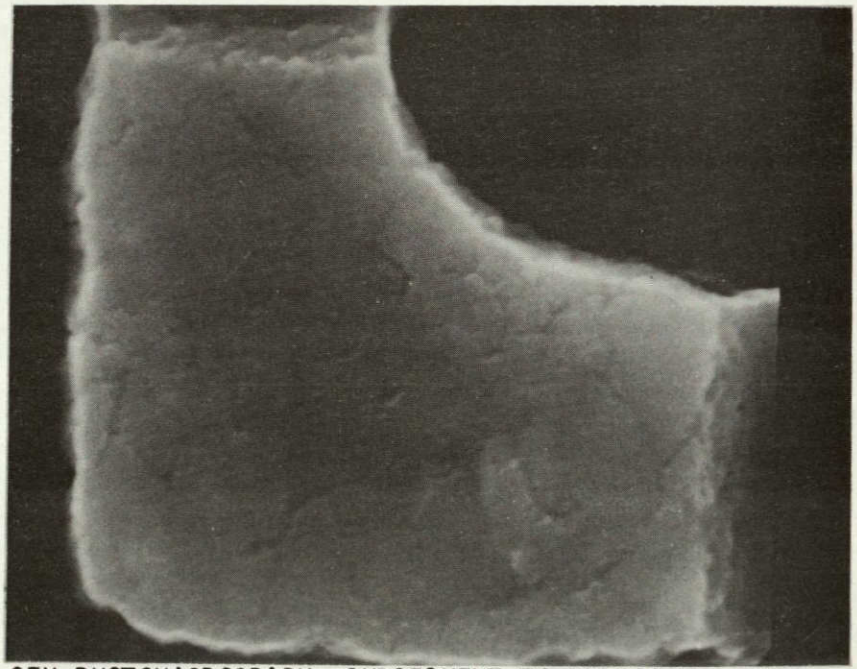


FIGURE 10 - SEM PHOTOMICROGRAPH, SUBSEQUENT TO DEPOSITED OXIDE REMOVAL, OF SAME AREA SHOWN IN FIGURE 9. NOTE RELATIVELY SMOOTH METALLIZATION SURFACE COMPARED TO CIRCULAR AREAS VISIBLE IN FIGURE 9.
(MAG. = 7000X, ANGLE = 90°)

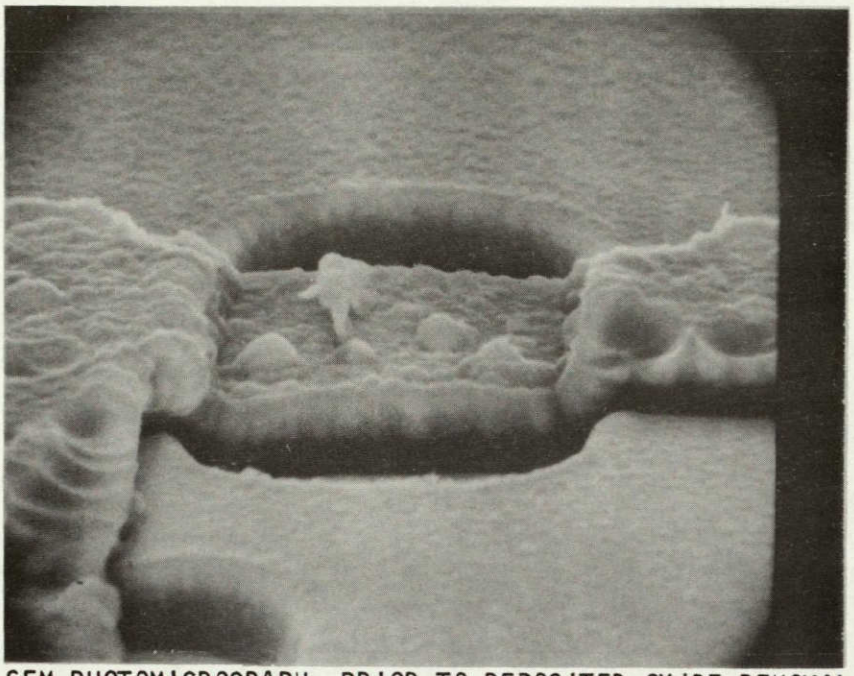


FIGURE 11 - SEM PHOTOMICROGRAPH, PRIOR TO DEPOSITED OXIDE REMOVAL, OF AREA INDICATED BY ARROW 3 OF FIGURE 5. MOUNDS AND DEPRESSIONS IN THE DEPOSITED OXIDE ARE VISIBLE. (MAG. = 5500X, ANGLE = 65°)

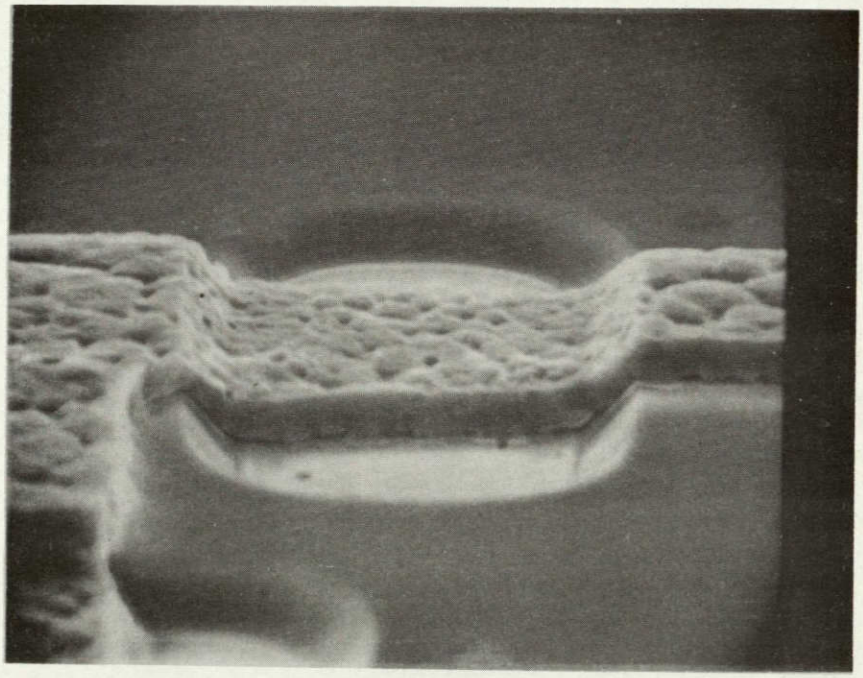


FIGURE 12 - SEM PHOTOMICROGRAPH, SUBSEQUENT TO DEPOSITED OXIDE REMOVAL, OF SAME AREA SHOWN IN FIGURE 11. PHOTOMICROGRAPH SHOWS GOOD METALLIZATION COVERAGE AT EDGE OF TAPERED OXIDE STEP.
(MAG. = 5500X, ANGLE = 65°)

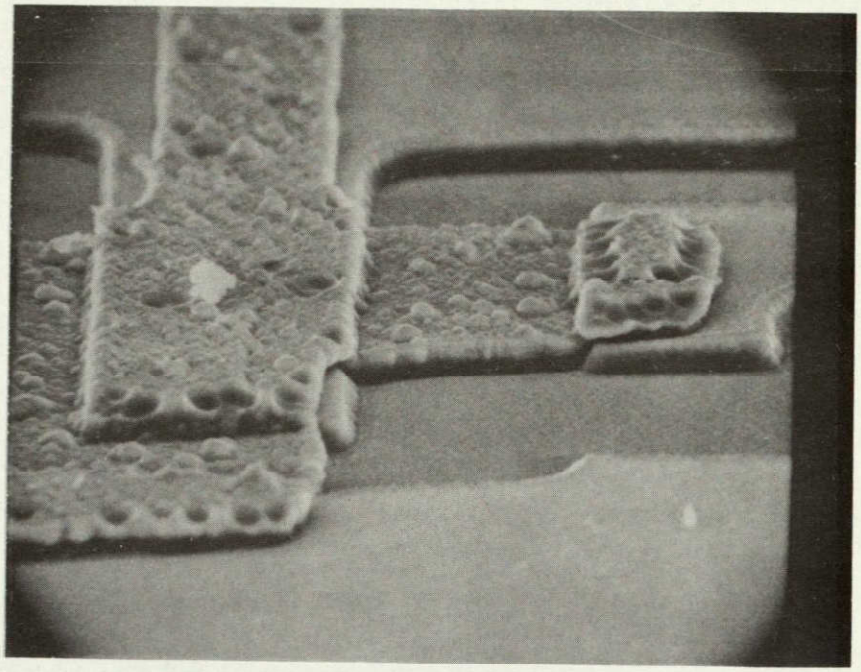


FIGURE 13 - SEM PHOTOMICROGRAPH, PRIOR TO DEPOSITED OXIDE REMOVAL, OF AREA INDICATED BY ARROW 4 IN FIGURE 6. THE AREA SHOWN IS AN MOS GATE.
(MAG. = 2300X, ANGLE = 65°)

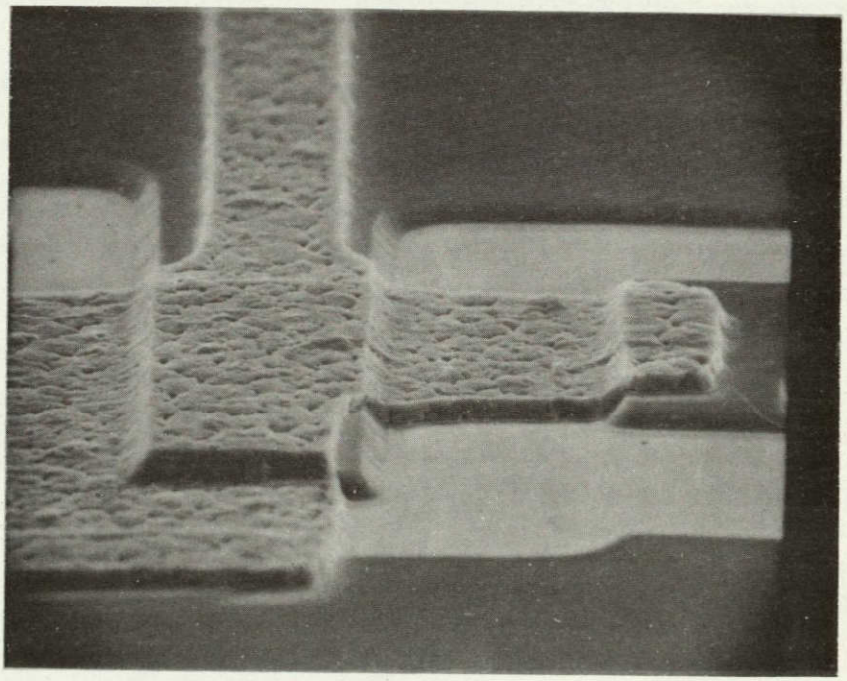


FIGURE 14 - SEM PHOTOMICROGRAPH, SUBSEQUENT TO DEPOSITED OXIDE REMOVAL, OF THE SAME AREA SHOWN IN FIGURE 13. THE PHOTOMICROGRAPH ILLUSTRATES GOOD METAL COVERAGE AT THE TAPERED OXIDE STEPS.
(MAG. = 2300X, ANGLE = 65°)

7025	(TYPE OF STRUCTURE CODE)
14-9-47	(LOT NUMBER FROM WHICH CHIP WAS OBTAINED)
WAFER 2	(WAFER FROM WHICH CHIP WAS OBTAINED)
DEVICE 222 4	(DEVICE SERIALIZATION)

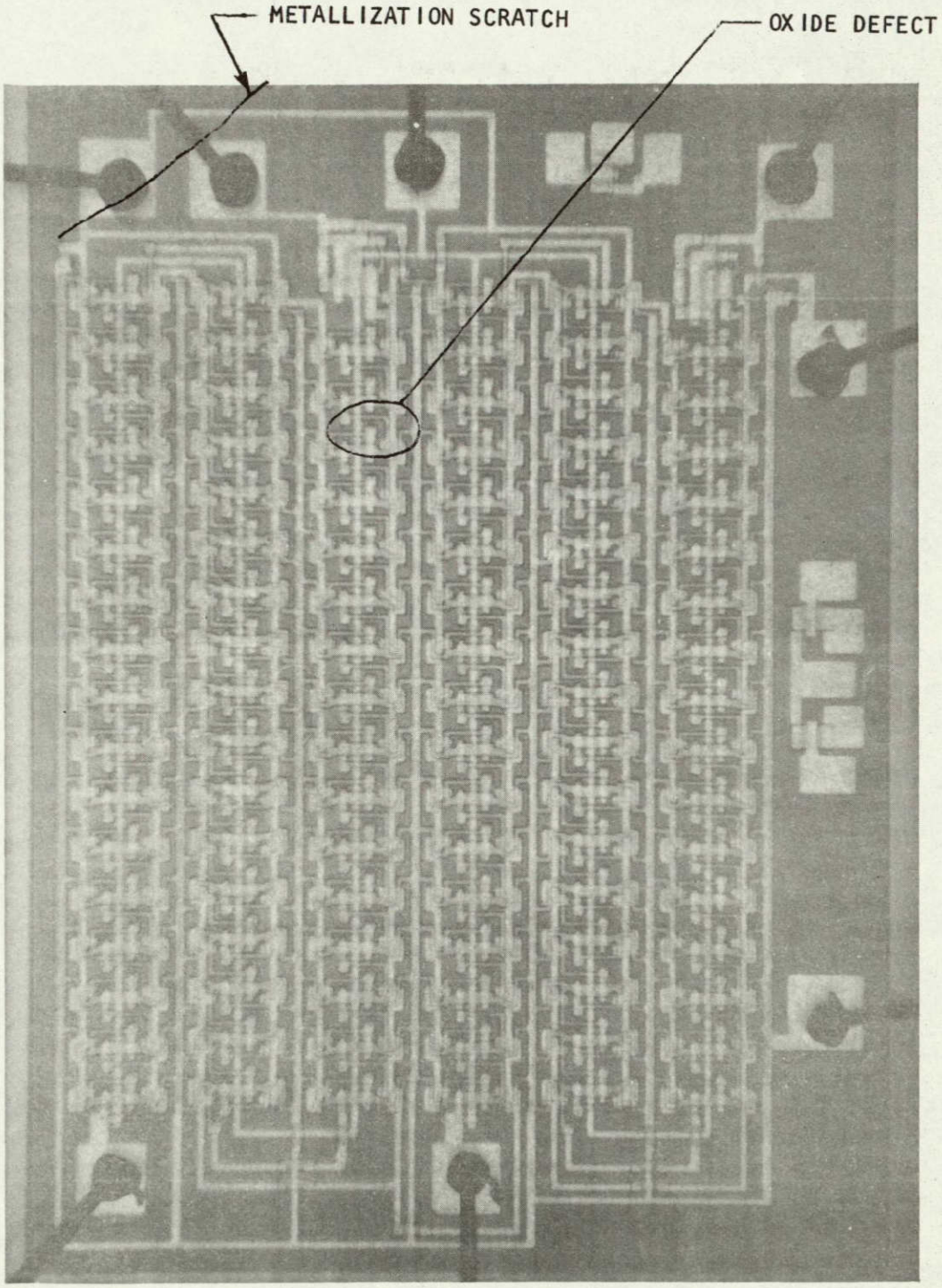
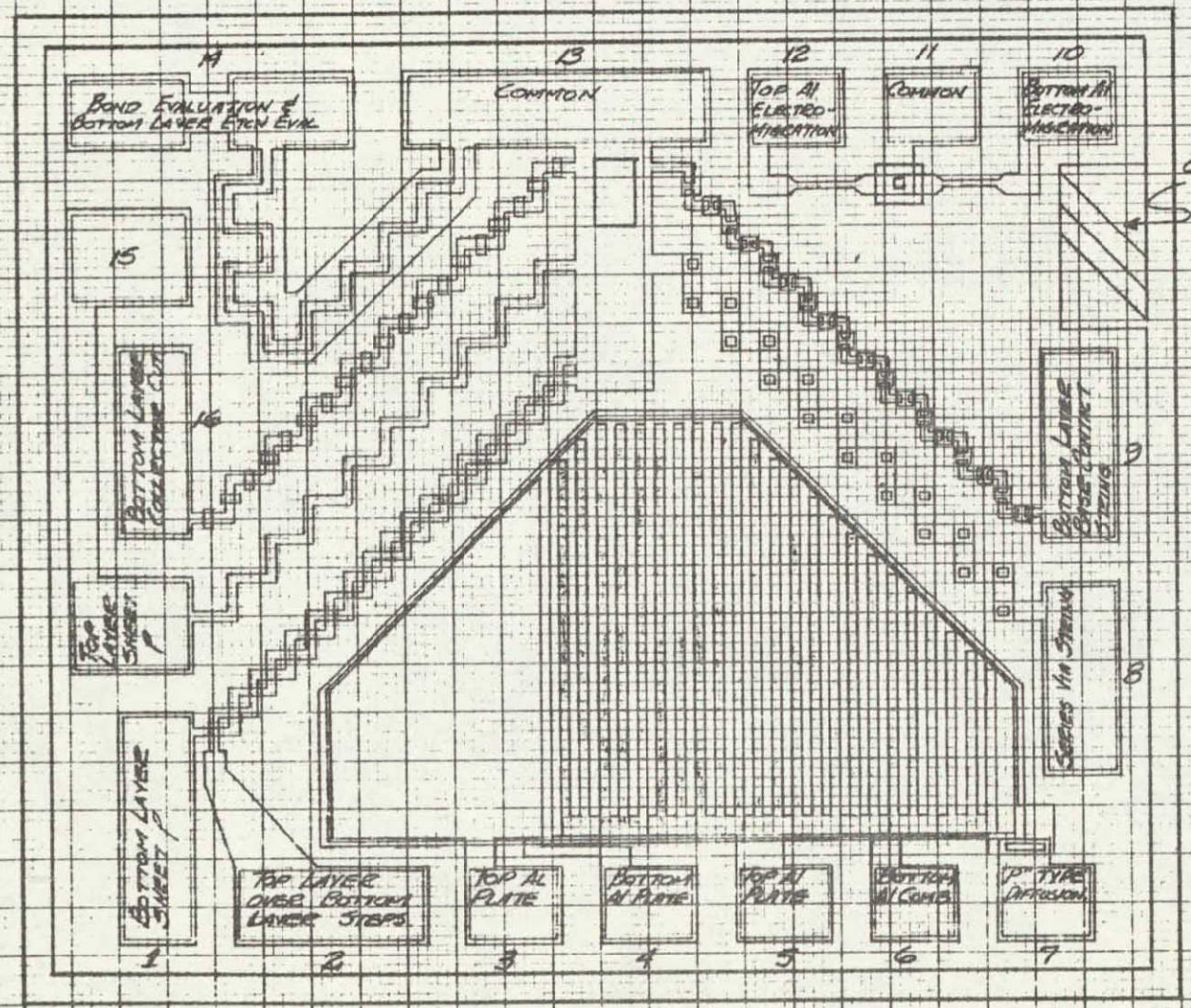


FIGURE 15 - ILLUSTRATION OF METHOD BEING UTILIZED TO RECORD OBSERVED PRE-SEAL VISUAL DEFECTS.



PINS	DESCRIPTION
3-4	TOP ALUMINUM PLATE OVER BOTTOM ALUMINUM PLATE FOR EVALUATION OF DEPOSITED OXIDE
3-7	BOTTOM ALUMINUM PLATE OVER P+ DIFFUSION FOR EVALUATION OF THERMAL OXIDE
5-6	TOP ALUMINUM PLATE OVER BOTTOM ALUMINUM COMB FOR EVALUATION OF OXIDE INTEGRITY AT STEPS
5-7	BOTTOM ALUMINUM COMB OVER P+ DIFFUSION.

NOTE:

1. THE AREA OF OXIDE DELINEATED BY THE PLANE PLATES (PINS 3 & 4) AND THE PLANE PLATE OVER THE ALUMINUM COMB (PINS 5, 6) ARE APPROXIMATELY THE SAME AND EQUAL TO 200 SQ MILS.
2. PROVISIONS ARE MADE FOR KELVIN CONTACTS AT ALL BONDING PADS WHERE ACCURATE RESISTANCE MEASUREMENTS ARE REQUIRED.
3. SCALE 10 mm ≈ 2.5 MILS

FIGURE 16 PROPOSED BILAYER METAL TEST PATTERN - CHIP NUMBER 1

CHIP SIZE 51 X 60 MILS

9130/1.7
W Beyer - EEGC

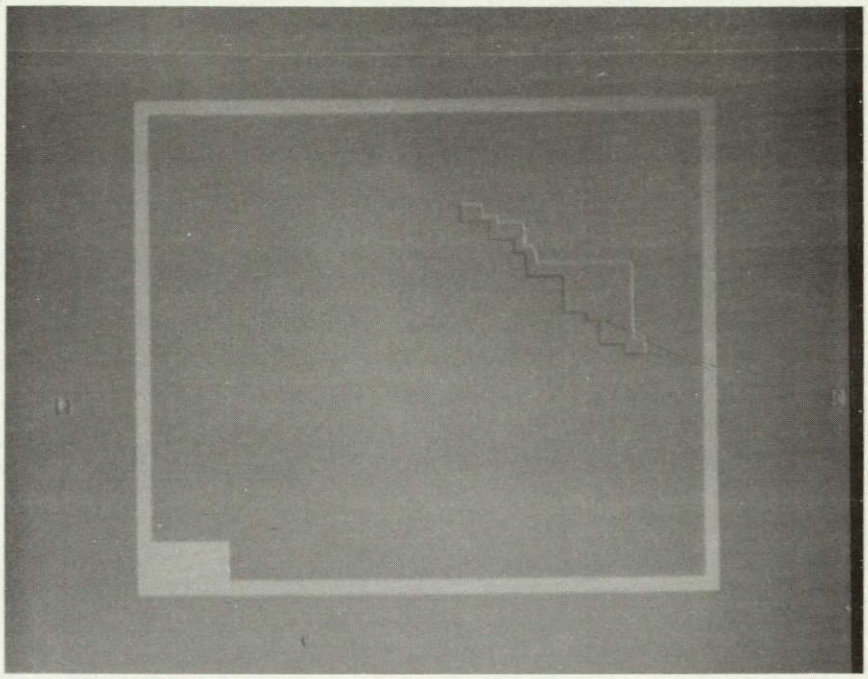


FIGURE 17 - PHOTOMICROGRAPH OF BILAYER- BIPOLAR TEST PATTERN 1, SUBSEQUENT TO ISOLATION DIFFUSION. BURIED N+ DIFFUSIONS, PRIOR TO EPITAXIAL GROWTH, IS VISIBLE IN UPPER RIGHT HAND CORNER OF CHIP.

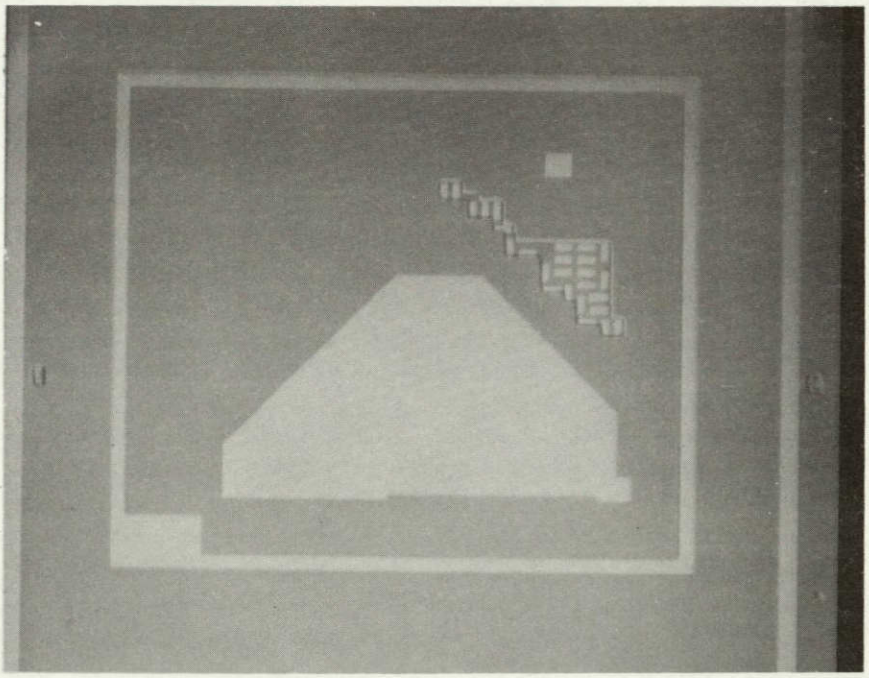


FIGURE 18 - PHOTOMICROGRAPH OF BILAYER-BIPOLAR TEST PATTERN 1, SUBSEQUENT TO "P" DIFFUSION.

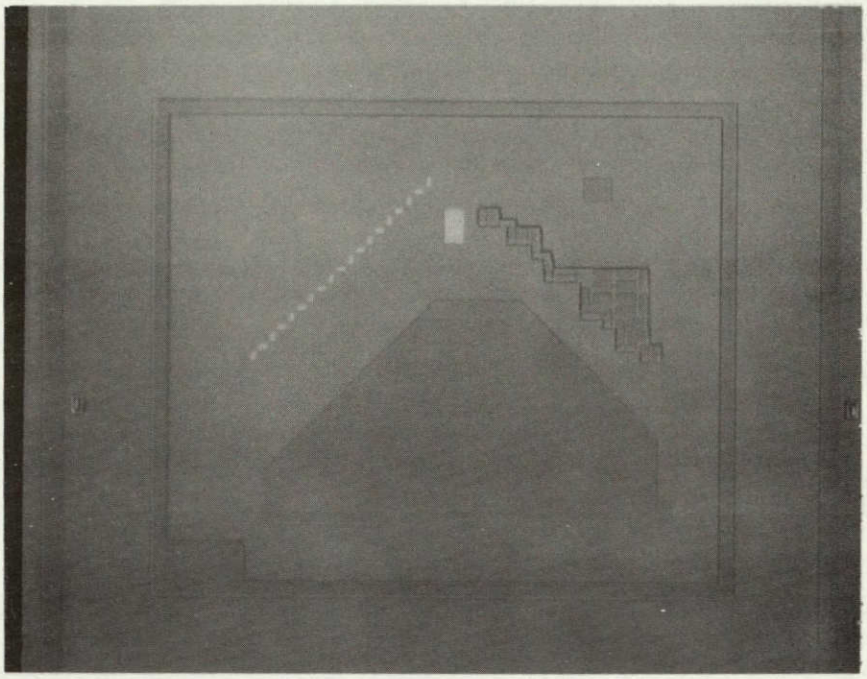


FIGURE 19 - PHOTOMICROGRAPH OF BILAYER-BIPOLAR TEST PATTERN 1, SUBSEQUENT TO "N" DIFFUSION.

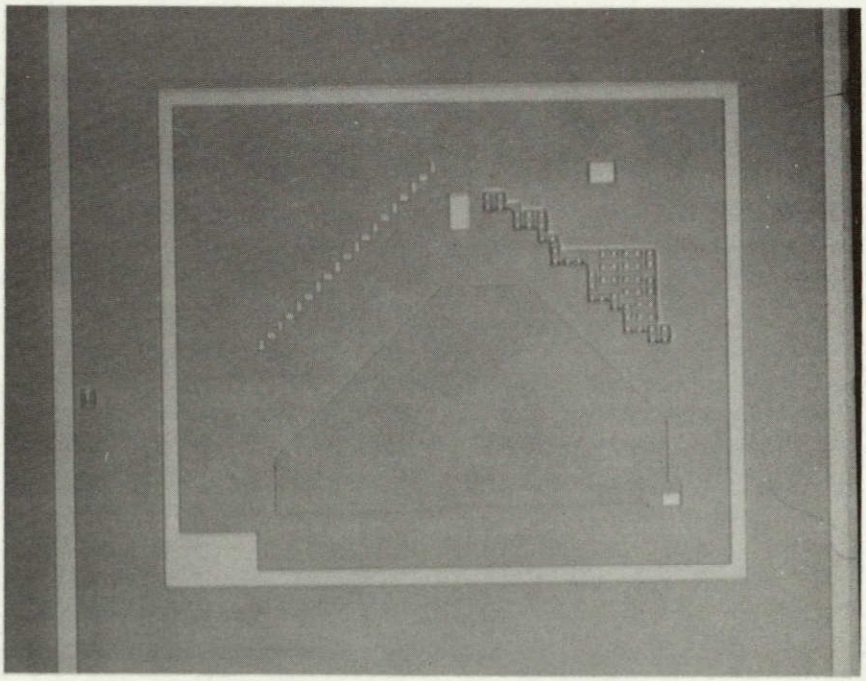


FIGURE 20 - PHOTOMICROGRAPH OF BILAYER-BIPOLAR TEST PATTERN 1, SUBSEQUENT TO THERMAL OXIDE CONTACT CUT.

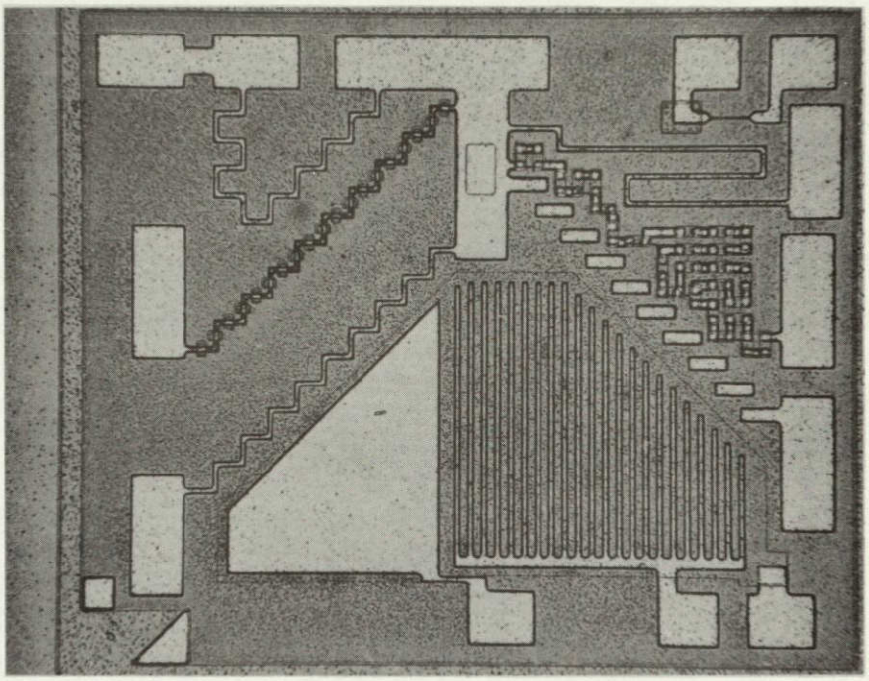


FIGURE 21 - PHOTOMICROGRAPH OF BILAYER-BIPOLAR TEST PATTERN 1, SUBSEQUENT TO BOTTOM LAYER METALLIZATION.

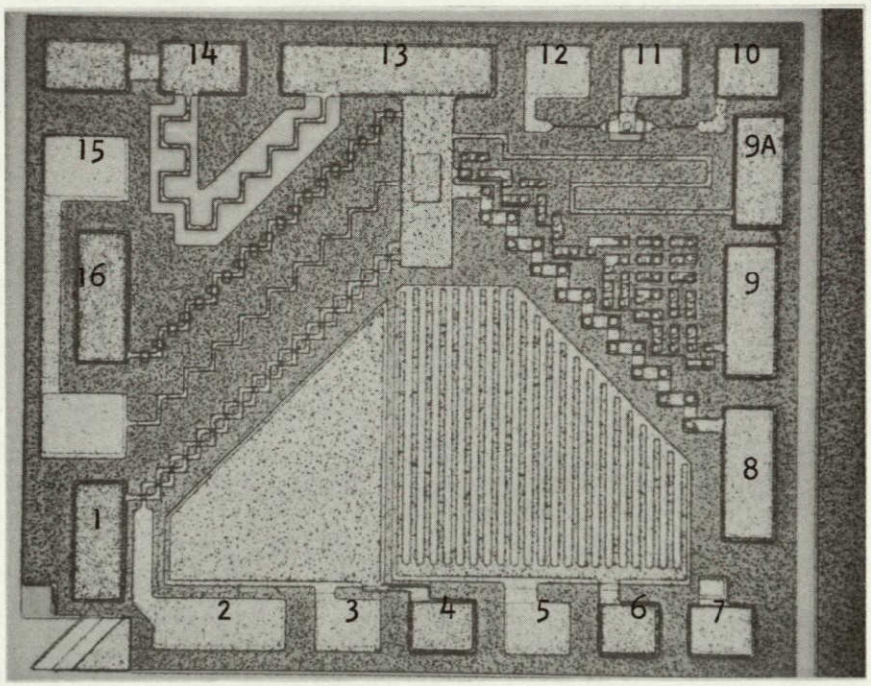
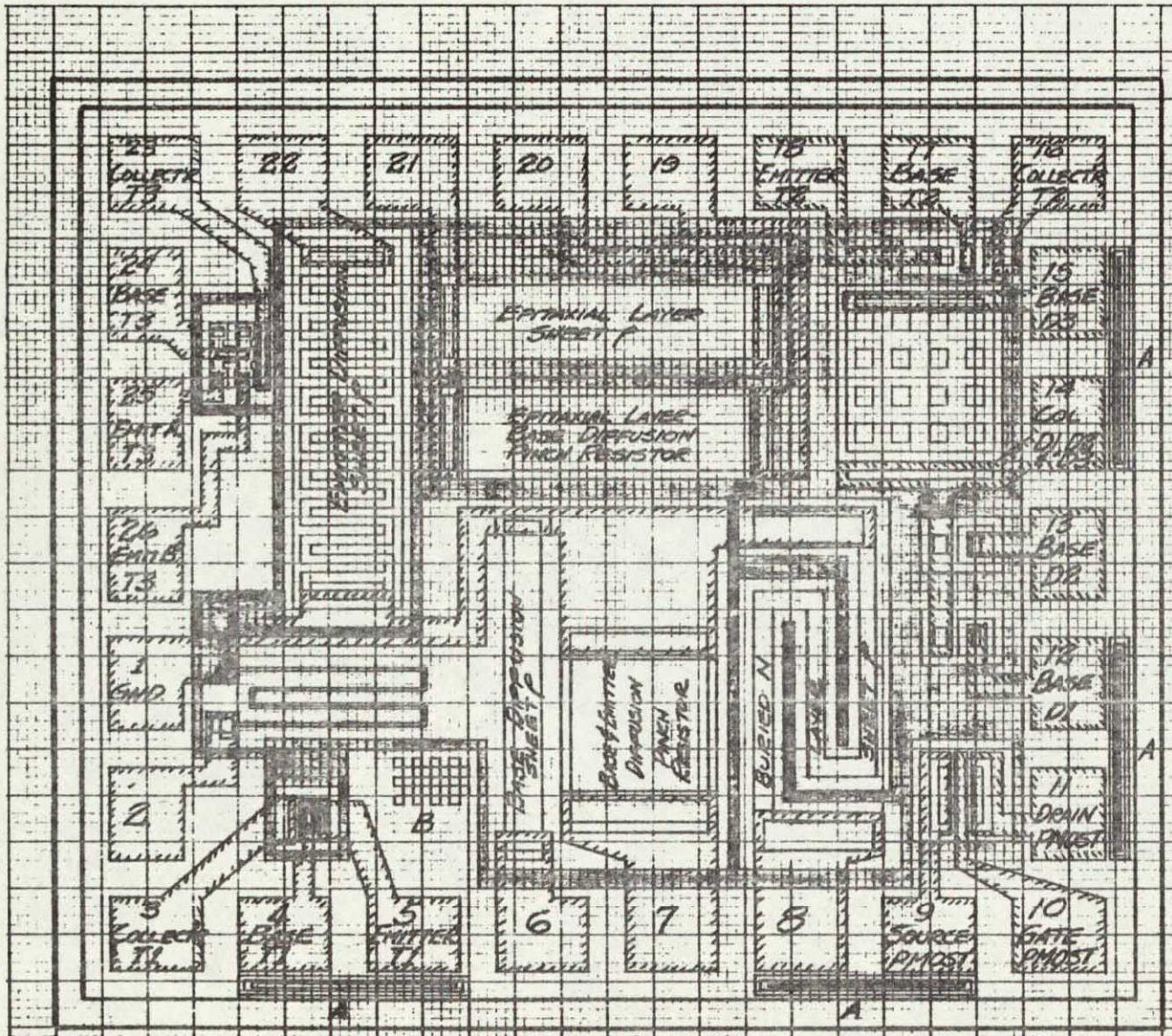


FIGURE 22 - PHOTOMICROGRAPH OF BILAYER-BIPOLAR TEST PATTERN 1, SUBSEQUENT TO TOP LAYER METALLIZATION AND TOP GLASS CUT.



CHIP SIZE 51 x 60 MILS

PINS	DESCRIPTION
1-2	RESISTOR, 25K, 8x15 x 4 MILS
3-4-5	NPN BIPOLAR TRANSISTOR
6-1	BASE DIFFUSION SHEET P VEHICLE 2.1K Ω
7-1	PINCH RESISTOR EMITTER DIFFUSION OVER BASE DIFFUSION, ≈ 2.5K
8-1	BURIED LAYER SHEET P VEHICLE, ≈ 730 Ω
9-10-11	MOS "P" CHANNEL TRANSISTOR
12-14	COLLECTOR BASE DIODE (NO BURIED LAYER)
13-14	COLLECTOR BASE DIODE (WITH BURIED LAYER)
15-15	LARGE PERIMETER COLLECTOR BASE DIODE
16-17-18	SUBSTRATE COLLECTOR AND BIPOLAR TRANSISTOR (NO BURIED LAYER)
19-21	EPITAXIAL LAYER SHEET P, ≈ 2.5 KΩ (NO BURIED LAYER)
20-21	PINCH RESISTOR BASE DIFFUSION OVER EPITAXIAL LAYER, ≈ 3.3 KΩ (NO BURIED LAYER)
22-1	EMITTER DIFFUSION SHEET P VEHICLE, ≈ 32.5 Ω
23-24-25-26	MULTI EMITTER NPN BIPOLAR TRANSISTOR

FIGURE 23 PROPOSED BIPOLAR TEST PATTERN
CHIP NUMBER 8.

SCALE 10 mm = 2.5 MILS

9/30/69
W. Bitzer
P.E.

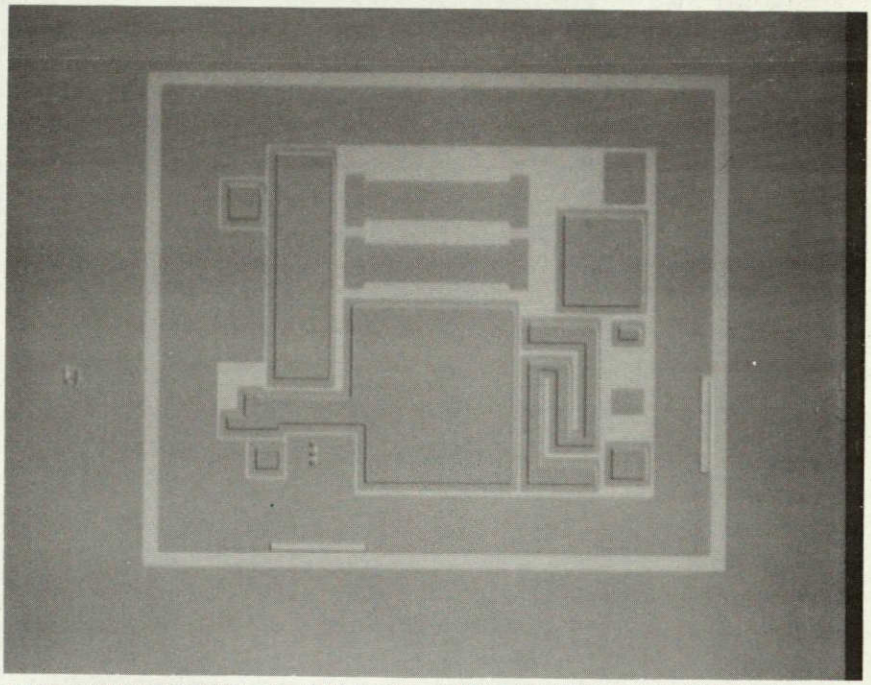


FIGURE 24 - PHOTOMICROGRAPH OF BILAYER-BIPOLAR TEST PATTERN 2, SUBSEQUENT TO ISOLATION DIFFUSION. BURIED N+ DIFFUSIONS, PRIOR TO EPITAXIAL GROWTH, ARE VISIBLE

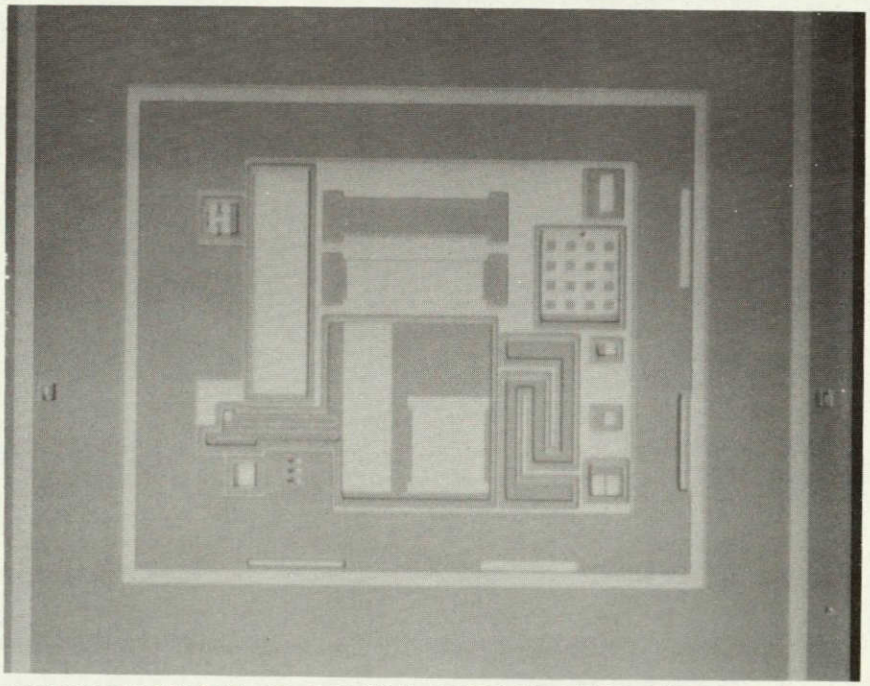


FIGURE 25 - PHOTOMICROGRAPH OF BILAYER-BIPOLAR TEST PATTERN 2, SUBSEQUENT TO "P" DIFFUSION.

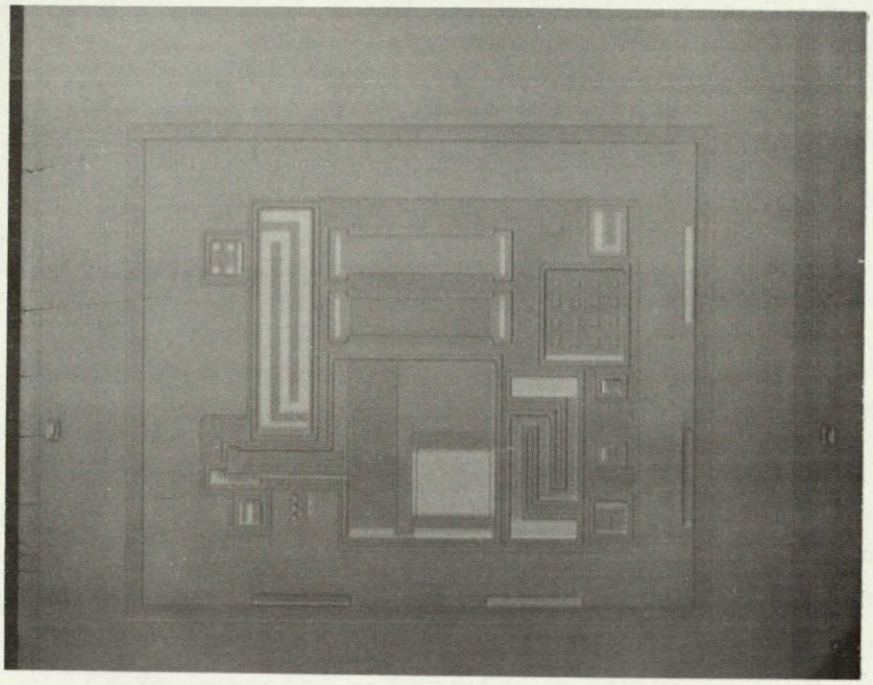


FIGURE 26 - PHOTOMICROGRAPH OF BILAYER-BIPOLAR TEST PATTERN 2, SUBSEQUENT TO "N" DIFFUSION.

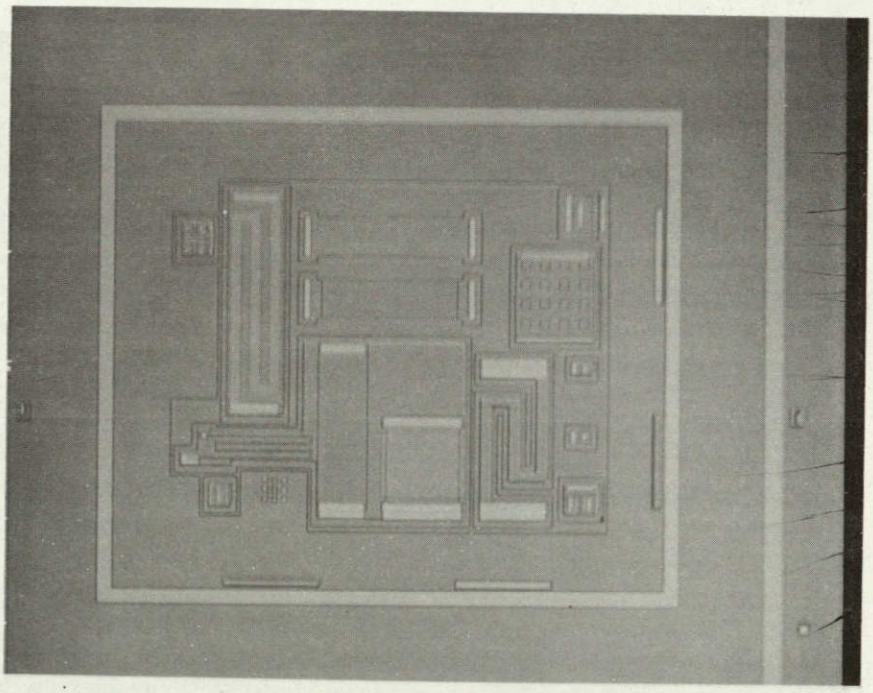


FIGURE 27 - PHOTOMICROGRAPH OF BILAYER-BIPOLAR TEST PATTERN 2, SUBSEQUENT TO THERMAL OXIDE CONTACT CUT.

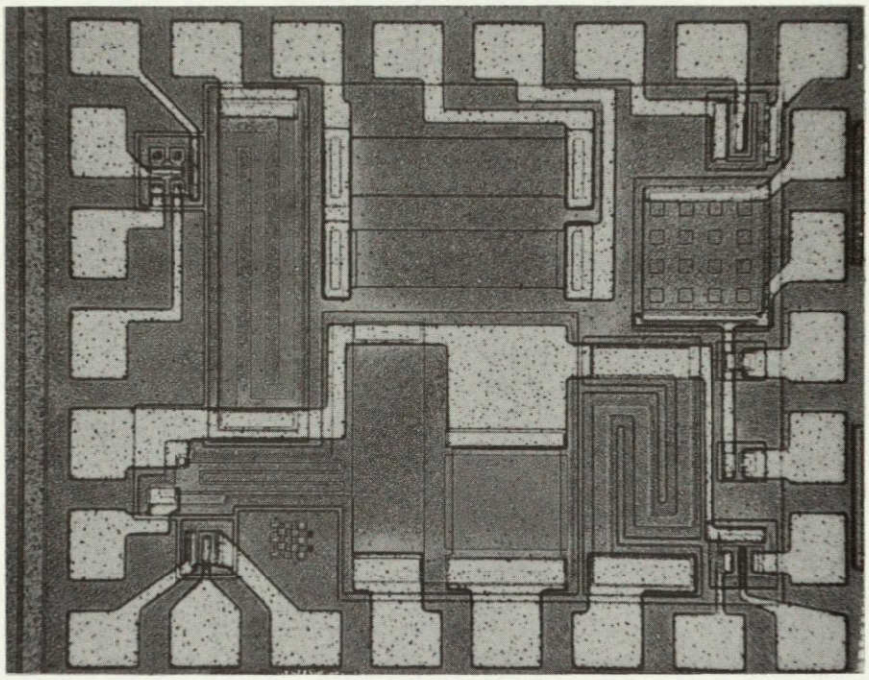


FIGURE 28 - PHOTOMICROGRAPH OF BILAYER-BIPOLAR TEST PATTERN 2, SUBSEQUENT TO BOTTOM LAYER METALLIZATION.

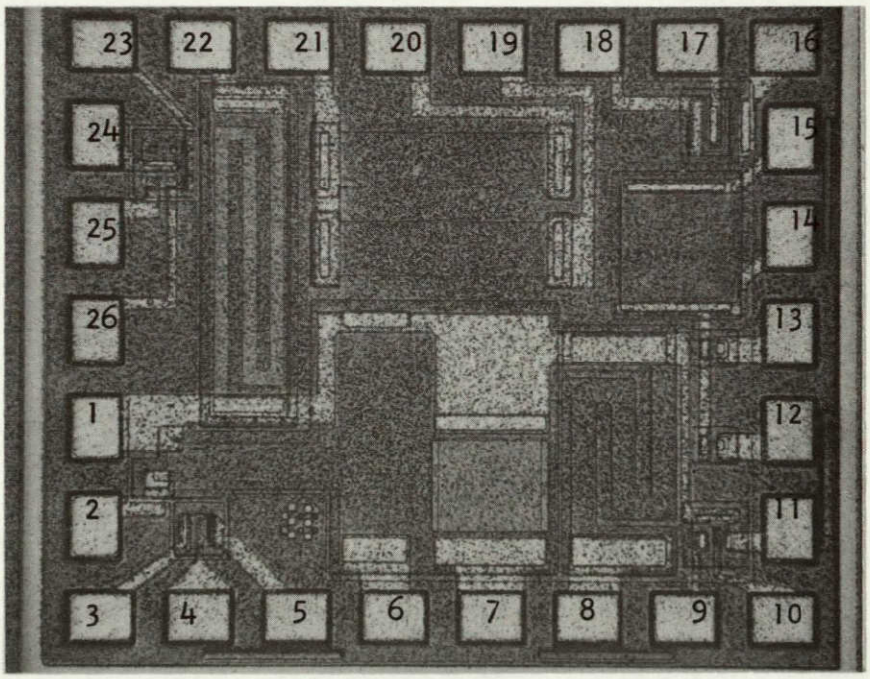
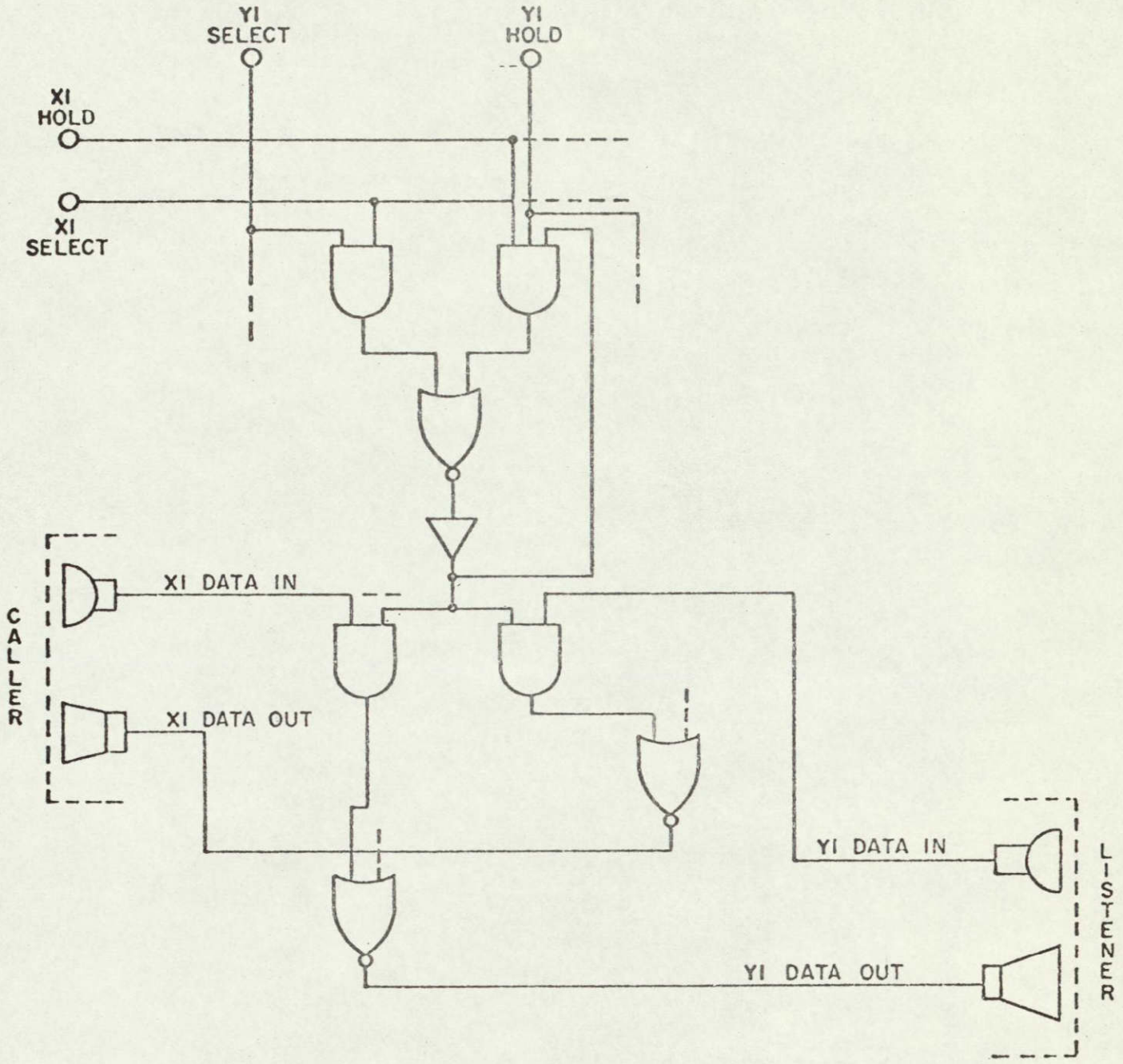
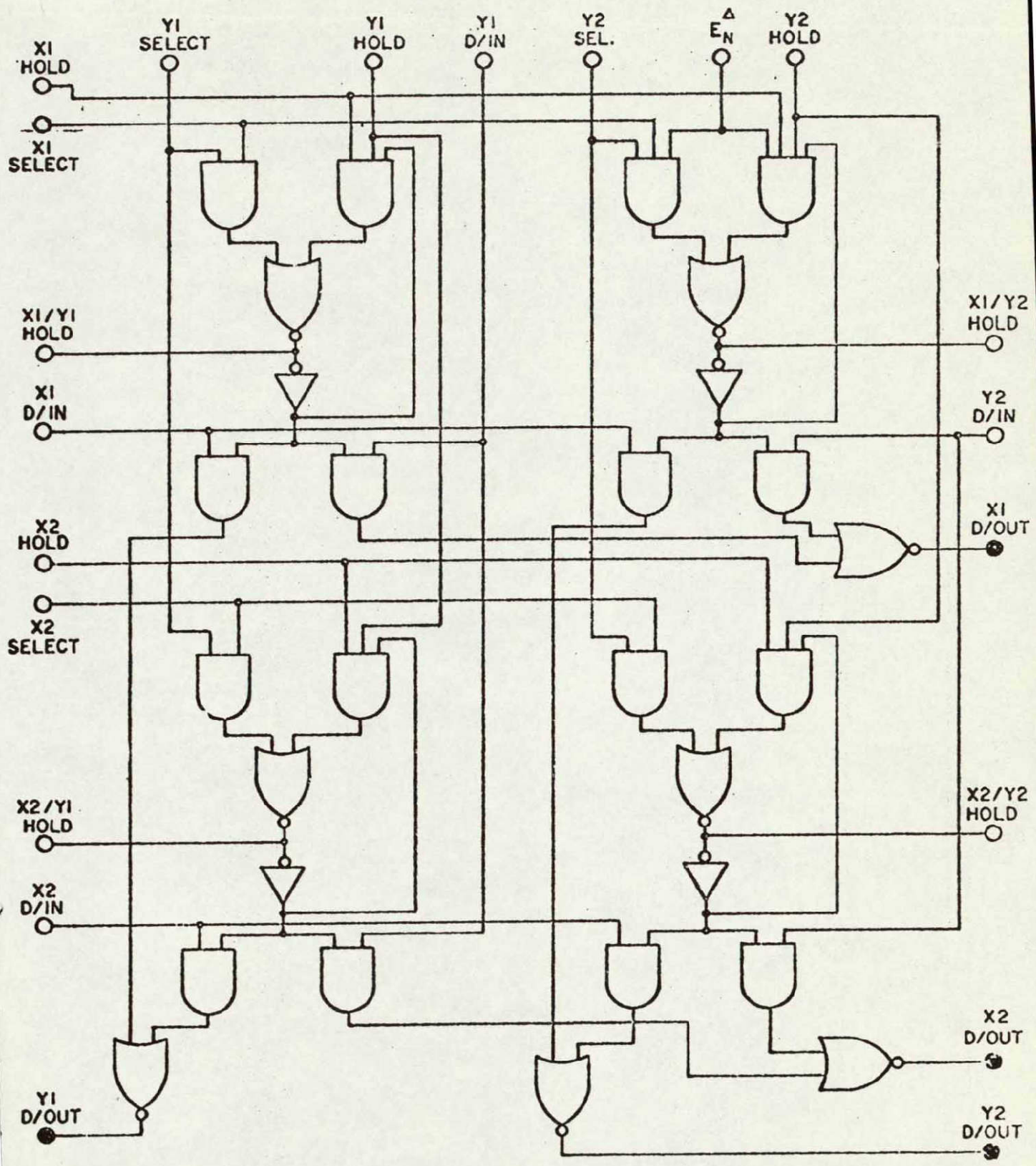


FIGURE 29 - PHOTOMICROGRAPH OF BILAYER-BIPOLAR TEST PATTERN 2, SUBSEQUENT TO TOP LAYER METALLIZATION AND TOP GLASS CUT.



SIMPLIFIED LOGIC FLOW DIAGRAM FOR XI/YI CROSSPOINT

FIGURE 30.



NOTE:
● DESIGNATES COLLECTOR TIES

FIGURE 31 - Logic Diagram

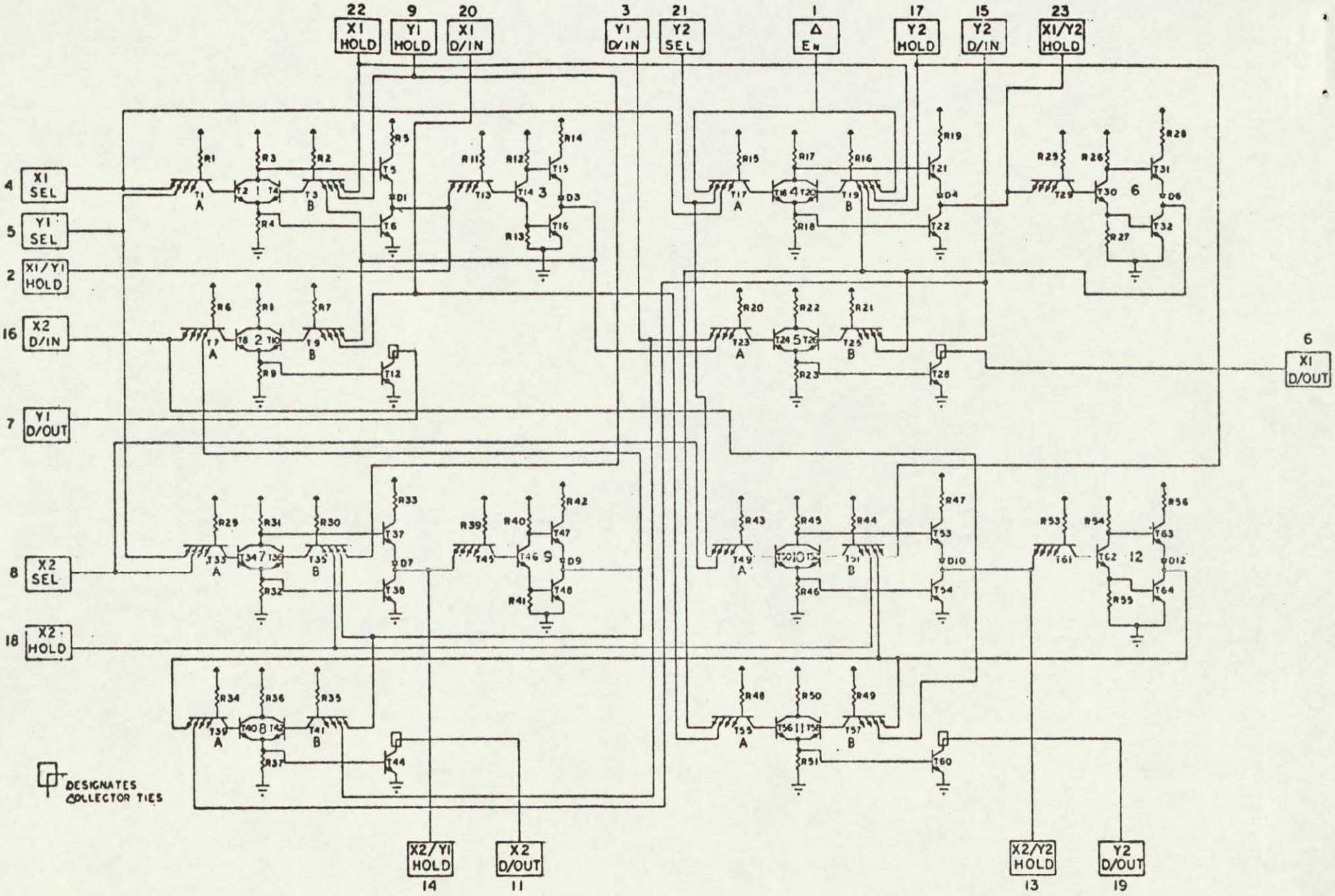


FIGURE 32 - Circuit Schematic Diagram of SP0199A.

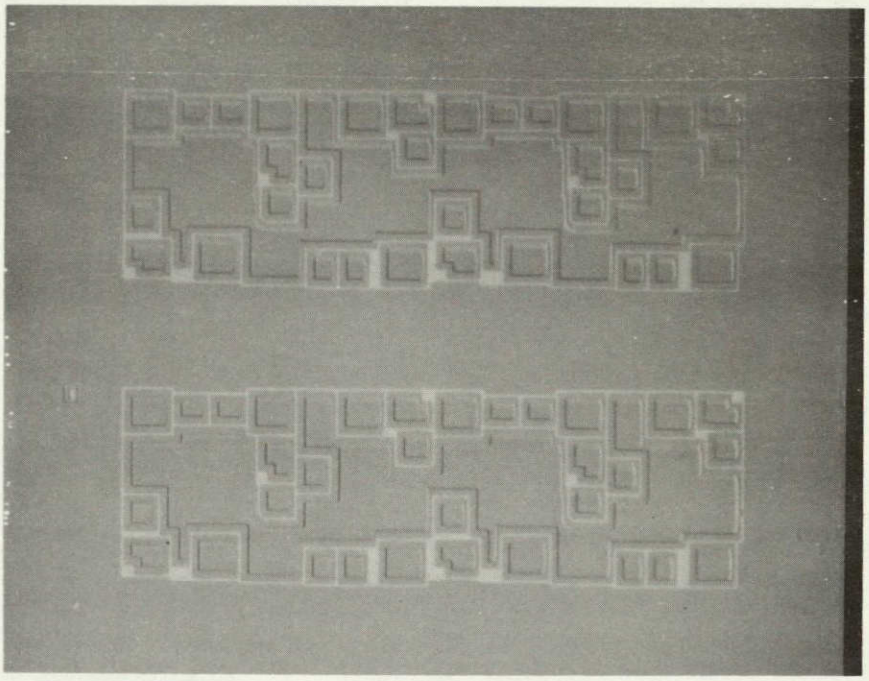


FIGURE 33 - PHOTOMICROGRAPH OF DCQ, SUBSEQUENT TO ISOLATION DIFFUSION. BURIED N+ DIFFUSIONS, PRIOR TO EPITAXIAL GROWTH, ARE VISIBLE.

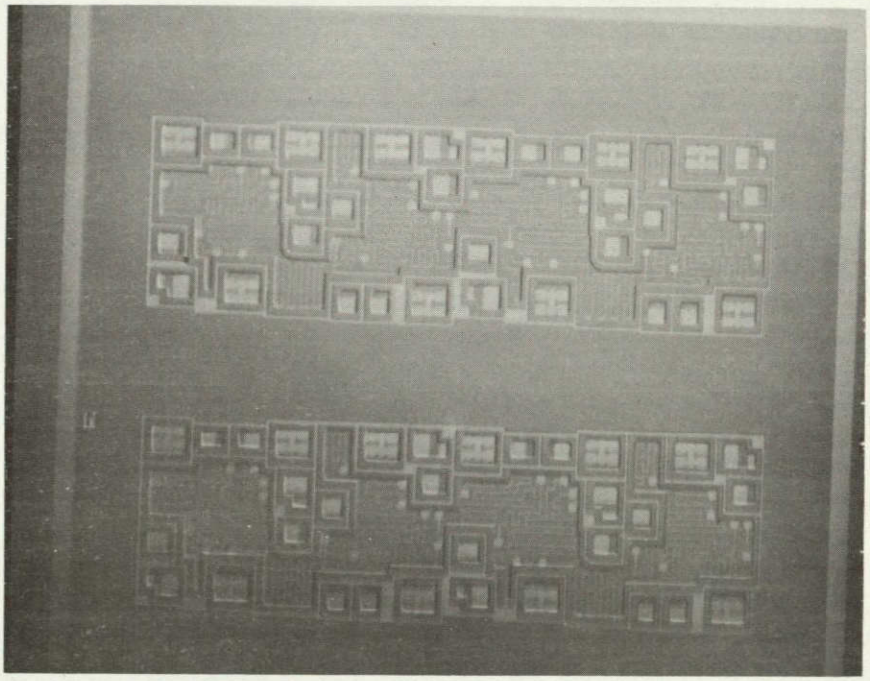


FIGURE 34 - PHOTOMICROGRAPH OF DCQ, SUBSEQUENT TO "P" DIFFUSION.

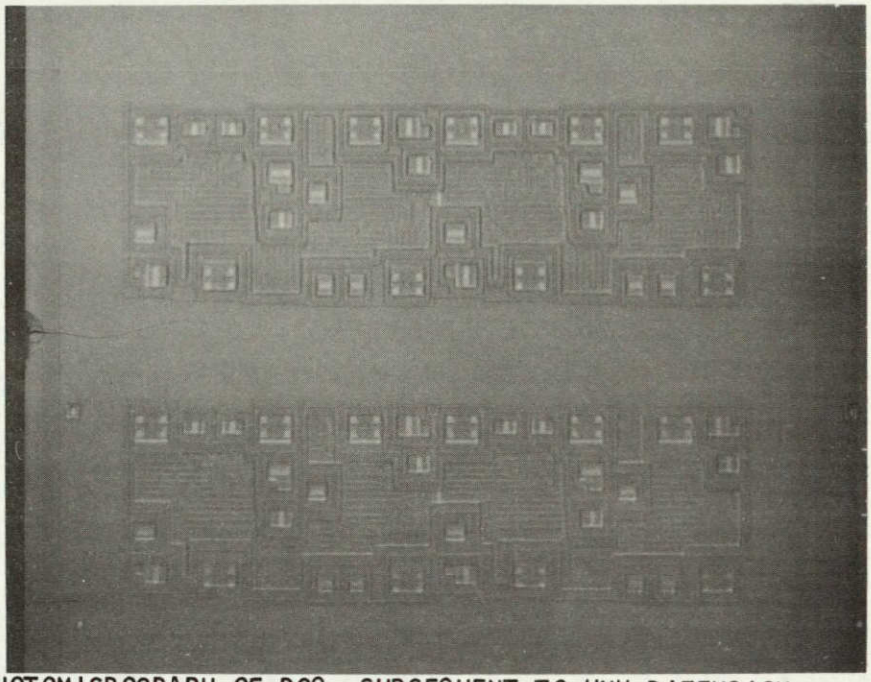


FIGURE 35 - PHOTOMICROGRAPH OF DCQ, SUBSEQUENT TO "N" DIFFUSION.

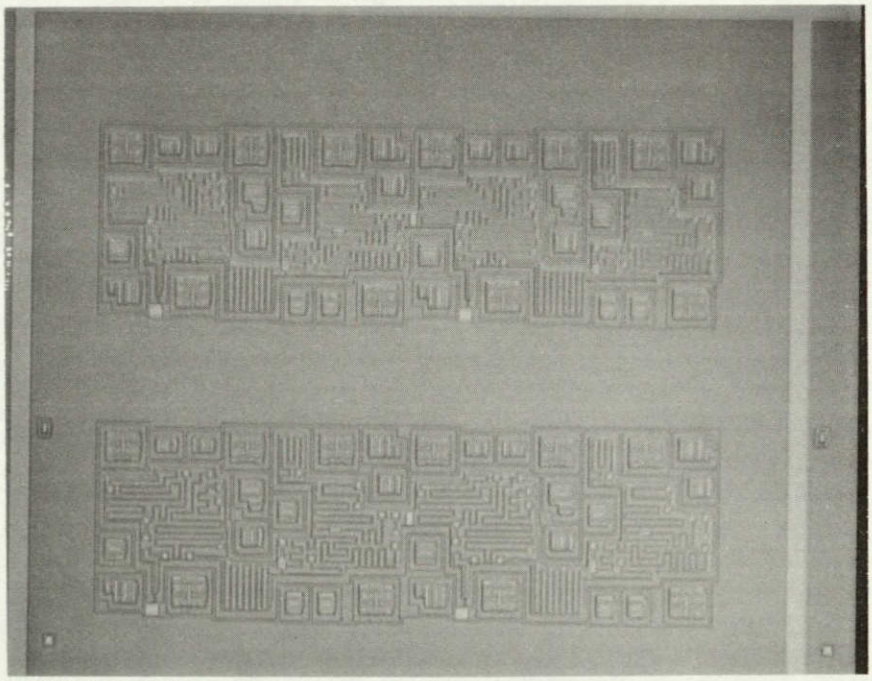


FIGURE 36 - PHOTOMICROGRAPH OF DCQ, SUBSEQUENT TO THERMAL OXIDE CONTACT CUT.

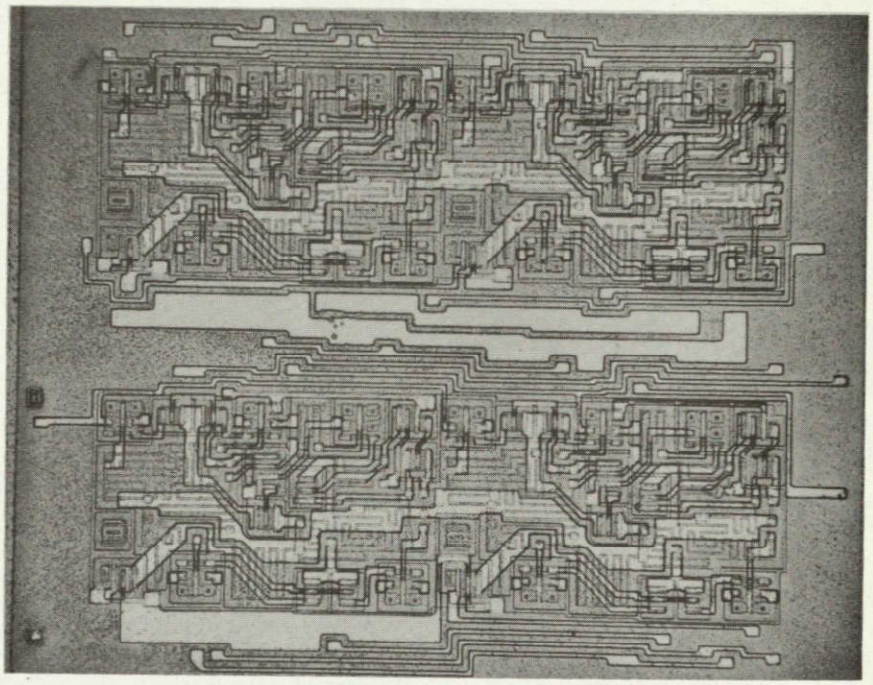


FIGURE 37 - PHOTOMICROGRAPH OF DCQ, SUBSEQUENT TO BOTTOM LAYER METALLIZATION.

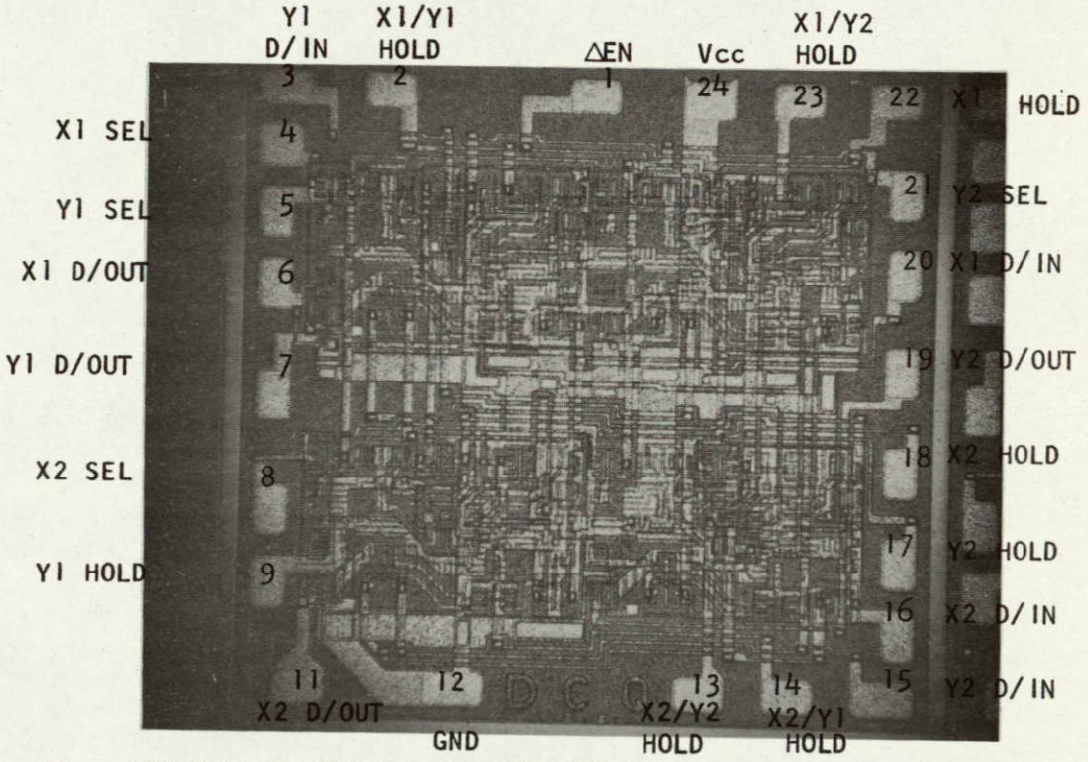


FIGURE 38 - PHOTOMICROGRAPH OF DCQ, SUBSEQUENT TO TOP LAYER METALLIZATION AND TOP GLASS CUT.

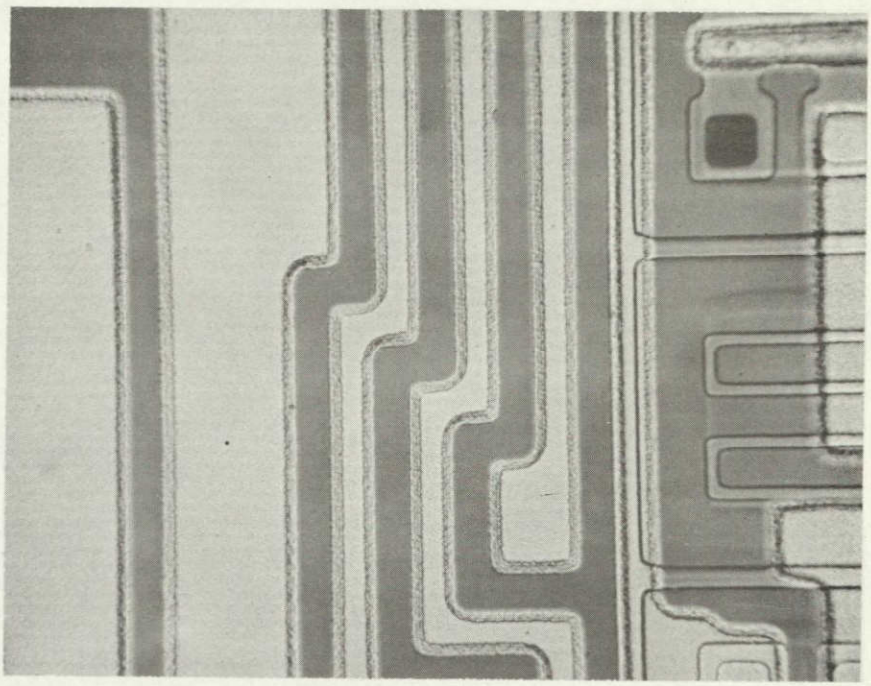


FIGURE 39 - PHOTOMICROGRAPH OF PORTION OF BOTTOM LAYER METALLIZATION ON DCQ CIRCUIT SHOWING CONSISTENCY OF TAPERED METALLIZATION PROCESS.

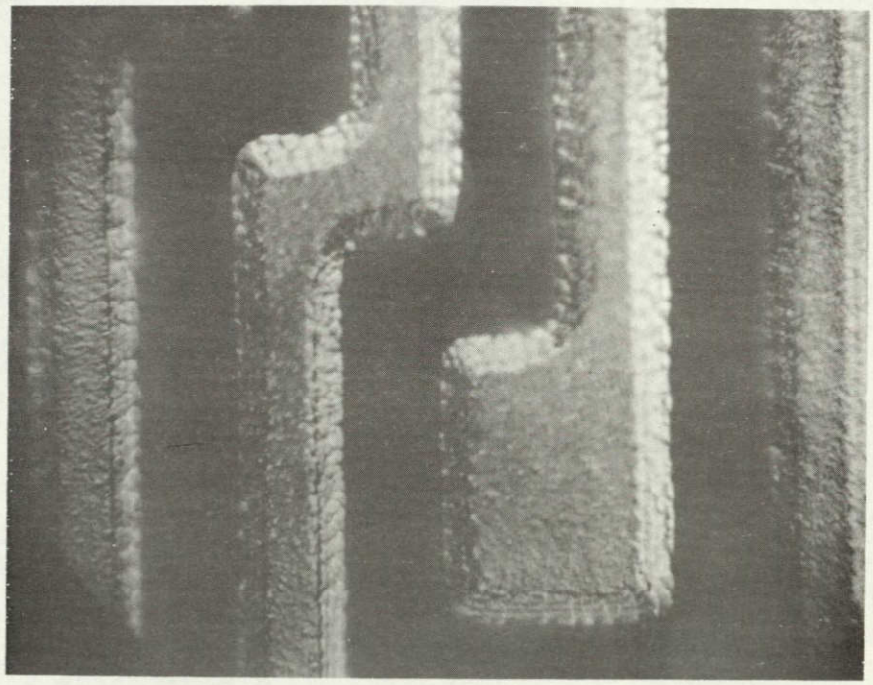


FIGURE 40 - PHOTOMICROGRAPH OF PORTION OF FIGURE 39 SHOWING ENLARGED VIEW OF TAPERED METALLIZATION PROCESS.

APPENDIX A

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