Final Report
No. 122-93

AN INVESTIGATION OF METAL-INSULATOR INTERFACES

BUREAU OF ENGINEERING RESEARCH

Final Report

on

NASA Contract

NAS8-24654

DNC 1-X-40-92281 (1F)

by

Wilford D. Raburn
Project Director

Submitted to

The National Aeronautics and Space Administration
George C. Marshall Space Flight Center
Huntsville, Alabama

BER

COLLEGE OF ENGINEERING

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June, 1970

This is the final report on investigation of metal-insulator interfaces. The work effort for this reporting period consists of one week for the Project Director, W. D. Raburn, one-half time for Research Associate, D. Mathews, approximately one-third time for Research Assistant, W. H. Causey, and part-time for an Undergraduate Assistant. The results of the theoretical investigation and experimental results are presented. The current-voltage and capacitance-voltage characteristic for Metal-Nitride-Oxide-Silicon (MNOS) devices are given for wide ranges of voltage and temperature.

Financial

The total project expenditures and expenditures for this quarter are shown in Table 1. There has been some shifting of funds to meet budget requirements in completing the contract. Expenditures such as supplies and fringes are shown as having occurred this quarter although they actually occurred through the contracting period. This was because of the University's bookkeeping procedures.

Table 1

Project Expenditures

	Original Budget Estimate	Expenditures This Quarter	Total Expenditures
Salaries & Overhead	$7131.33	$3251.82	$9125.06
Supplies & Materials	926.86	135.33	135.33
Telephone & Telegraph	100.00	--	--
Travel	800.00	155.00	281.00
Publications	300.00	--	--
Fringes	389.81	406.61	406.61
Computer	300.00	--	--
	$9948.00	$3948.76	$9948.00

INTRODUCTION

The voltage-current and voltage-capacitance characteristics of MNOS capacitors were investigated over a wide range of temperatures to determine the effects of fast and slow interface states on the performance of MNOS devices. In particular, the model proposed by Frohman-Bentchkowsky and Lenzlinger[1] was investigated, since it appeared to be the most comprehensive and embodied much of the theory proposed by others for MNS[2] and MOS[3] capacitors. Briefly stated, the model of Reference 1 assumes conduction due to tunneling from the silicon into the oxide conduction band then drifting to the nitride, conduction in the silicon nitride due to repeated excitations from traps into the nitride conduction band, and accumulation of either positive or negative charge at the oxide-nitride interface. Their proposed energy band diagram and bias convention are reproduced as Figure 1. A detailed analysis of the results of our data, based primarily on their model and other work in the literature, appears in subsequent sections of this report.

The samples investigated were made at the Astrionics Laboratory of Marshall Space Flight Center, Huntsville, Alabama. Nitride thicknesses of 500Å and 2000Å were used. The thickness of the oxide, which was thermally grown, was about 50Å. Both n-type (3.2 - 4.8 Ω-cm) and p-type (.4 - .6 Ω-cm) silicon substrates were used. The substrate orientation was (111) in each case. A circular dot of aluminum of radius .102 cm was deposited on the nitride surface. The silicon chip (.254 cm x .254 cm) was bonded to a TO-5 header.

1. V-I CHARACTERISTICS

The model of Frohman-Bentchkowsky and Lenzlinger[1] assumes that the conduction mechanisms in the nitride and oxide layers are different and that, as a result, current continuity requires a buildup of charge at the interface such that the proper electric field distribution is set up in each material. The expression for current density J_n in the nitride as a function of temperature T and electric field ε_n consists of three terms[4]:

$$J_n = J_{n_1} + J_{n_2} + J_{n_3} \tag{1-1}$$

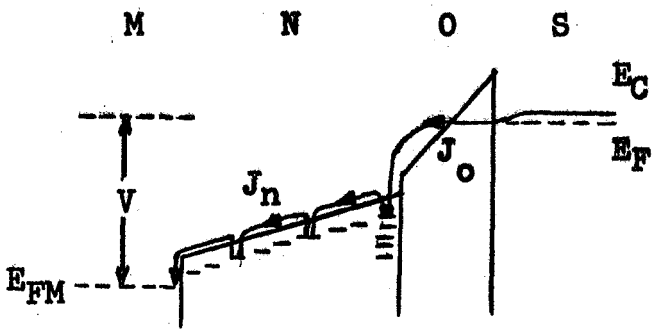
where,

$$J_{n1} = C_1 \varepsilon_n \exp(-q\phi_1/kT) \exp[(q/kT)(\beta\varepsilon_n)^{1/2}] \tag{1-2}$$

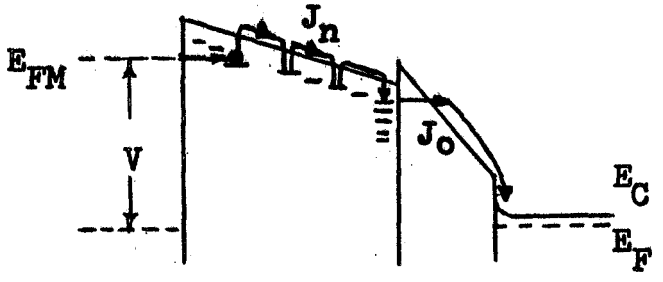
$$J_{n2} = C_2 \varepsilon_n^2 \exp(-\varepsilon_2/\varepsilon_n) \tag{1-3}$$

$$J_{n3} = C_3 \varepsilon_n \exp(-q\phi_3/kT) \tag{1-4}$$

J_{n1} corresponds to the Poole-Frenkel effect (field-enhanced thermal emission from traps). C_1, ϕ_1, and β are constants. J_{n1} should account for nearly all of the temperature dependence of J_n. Field emission from the same traps into the dielectric conduction band leads to a second term, J_{n2}, which is independent of temperature. C_2 and ε_2 are constants. J_{n2} should become significant only at very high fields and might well be considered an indication of incipient breakdown. J_{n3} corresponds to hopping of thermally excited electrons between isolated trapping states[5] and should be more important at low fields than high; it is also temperature dependent. C_3 and ϕ_3 are constants. A plot of J_{n3}/ε_n vs. ε_n at constant temperature should yield a straight line of



(a) Positive bias



(b) Negative bias

Fig. 1. Energy band diagram of MNOS structure[1]

zero slope. A corresponding plot of log J_{n1}/ε_n vs. $\sqrt{\varepsilon_n}$ should yield a line of constant slope at low fields, becoming supralinear at higher fields. A Fowler-Nordheim plot (log J_{n2}/ε_n^2 vs. $1/\varepsilon_n$) would be required to display the effects of J_{n2} as a straight line. Thus, by making such plots at various constant temperatures and investigating any linear portions, the theory could be verified for any MNS device (no oxide layer). Unfortunately, the presence of an oxide layer complicates this procedure. In general this will require a computer solution of simultaneous equations for currents, charge, and fields. The following argument demonstrates that graphical analysis as explained above is valid for our samples because the applied voltage appears almost entirely across the nitride and hence directly determines ε_n.

Continuity of electric flux determines the interface charge Q_I as,

$$Q_I = K_o e_o \varepsilon_o - K_n e_o \varepsilon_n. \tag{1-5}$$

The total applied voltage V divides between the two insulating layers as,

$$V = \varepsilon_o x_o + \varepsilon_n x_n, \tag{1-6}$$

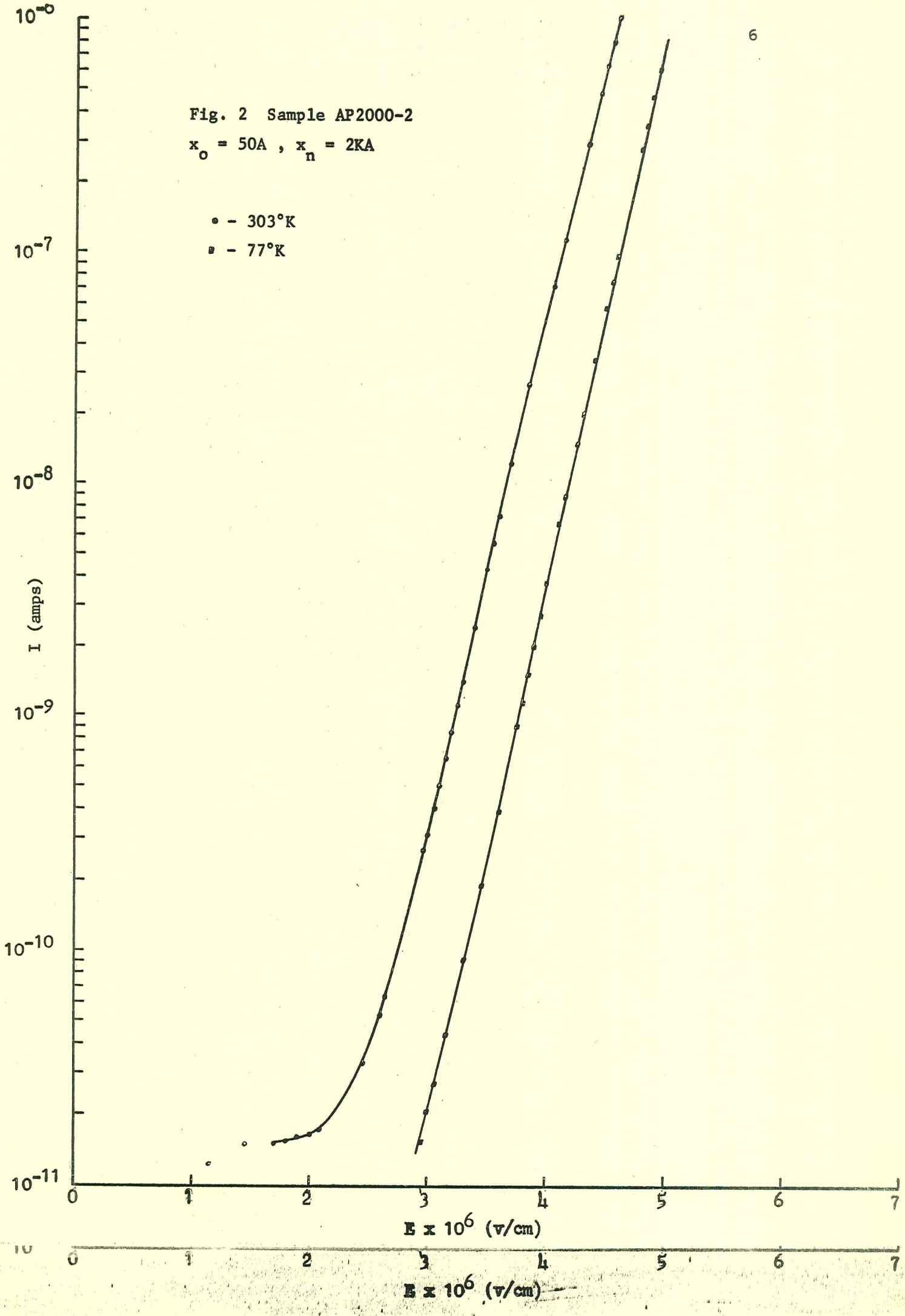
where x_o and x_n are the thicknesses of the oxide and nitride layers, respectively. Solving for ε_o and ε_n,

$$\varepsilon_o = \frac{V + \dfrac{Q_I x_n}{K_n e_o}}{x_o + \dfrac{x_n K_o}{K_n}} \simeq \frac{K_n V}{K_o x_n} \tag{1-7}$$

$$\varepsilon_n = \frac{V - \frac{Q_I x_n}{K_n e_o}}{x_n + \frac{x_o K_n}{K_o}} \simeq \frac{V}{x_n} \qquad (1\text{-}8)$$

where, based on pulse tests, the value of Q_I is at most on the order of 10^{-7} C for our samples. Hence, the applied voltage effectively appears across the nitride layer. While the mechanisms in the nitride will thus dominate the externally measured characteristics, it should be mentioned that the oxide conduction mechanism proposed is the Fowler-Nordheim model[3,6]. The current equation is basically the same as Equation (1-3) for J_{n2}, with temperature-dependent terms which change the characteristics very little. It has been suggested[1,7] that direct tunneling may play an important role in oxide layers thinner than ours (50Å); this effect was not investigated.

Figures 2, 3, and 4 show typical V-I characteristics (plotted as log I vs. ε) for various temperatures. The results are in agreement with those given by Sze[2] for an MNS device, indicating further that the nitride behavior dominates the external V-I characteristics. Figures 5, 6, and 7 show log J/ε vs. $\sqrt{\varepsilon}$. A line of constant positive slope here suggests the Frenkel-Poole effect (J_{n1}). A flat portion at low fields could indicate dominance by J_{n3}, the ohmic component, especially at higher temperatures. As temperature increases, the slope of the straight line due to J_{n1} should increase, and the line itself should shift to the left on the graph (see Equation (1-2)). Any flat portion due to J_{n3} should merely shift upward. The curves of Figures 5, 6, and 7 exhibit this behavior but the "flat" portion has a slightly negative slope. Although the rate of change of voltage with



0 1 2 3 4 5 6 7
E x 10^6 (v/cm)

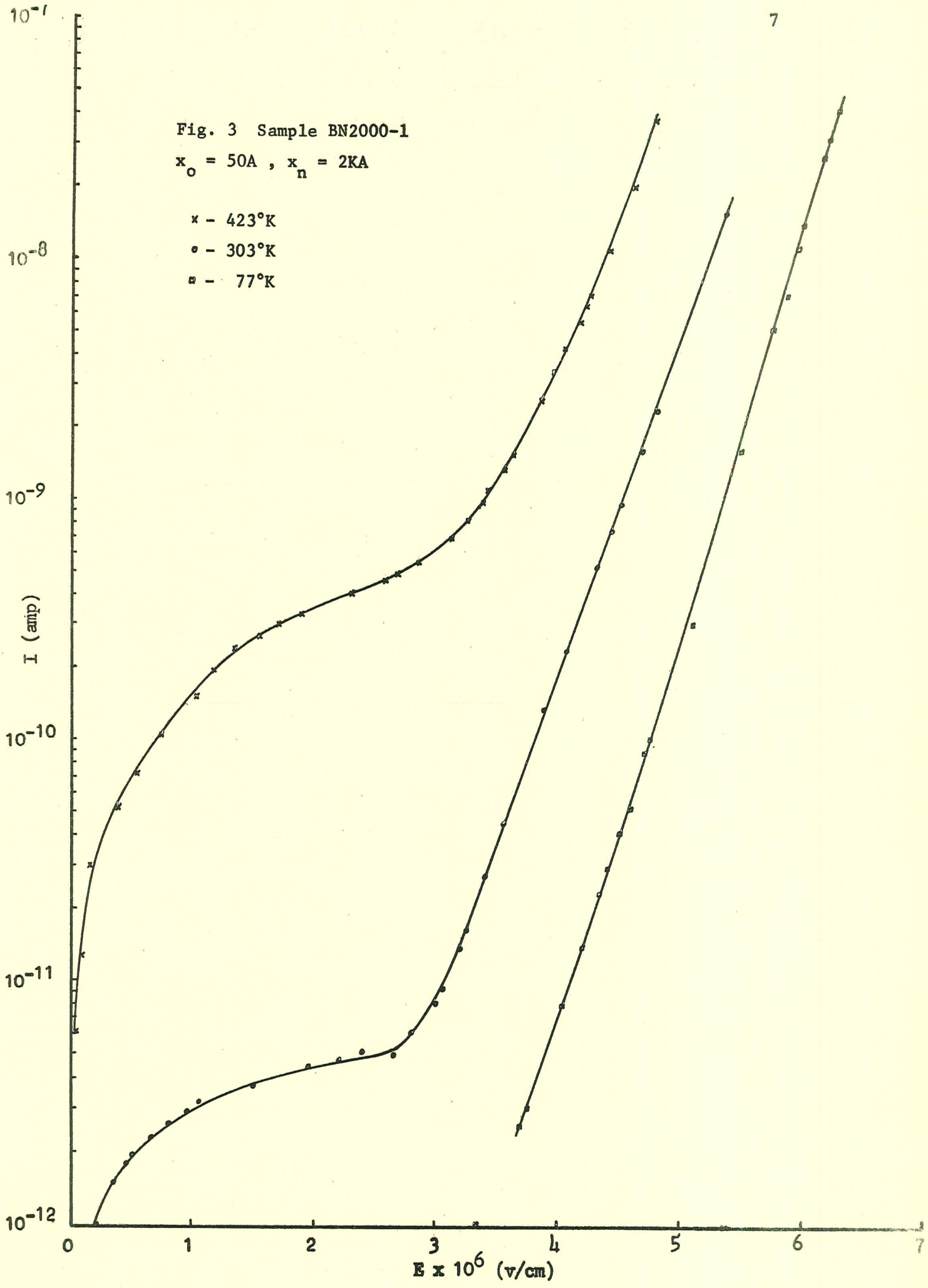


Fig. 3 Sample BN2000-1
x_o = 50A , x_n = 2KA
× - 423°K
∘ - 303°K
▫ - 77°K
10^{-7}
10^{-8}
10^{-9}
10^{-10}
10^{-11}
10^{-12}
I (amp)
0
1
2
3
4
5
6
7
E x 10^6 (v/cm)

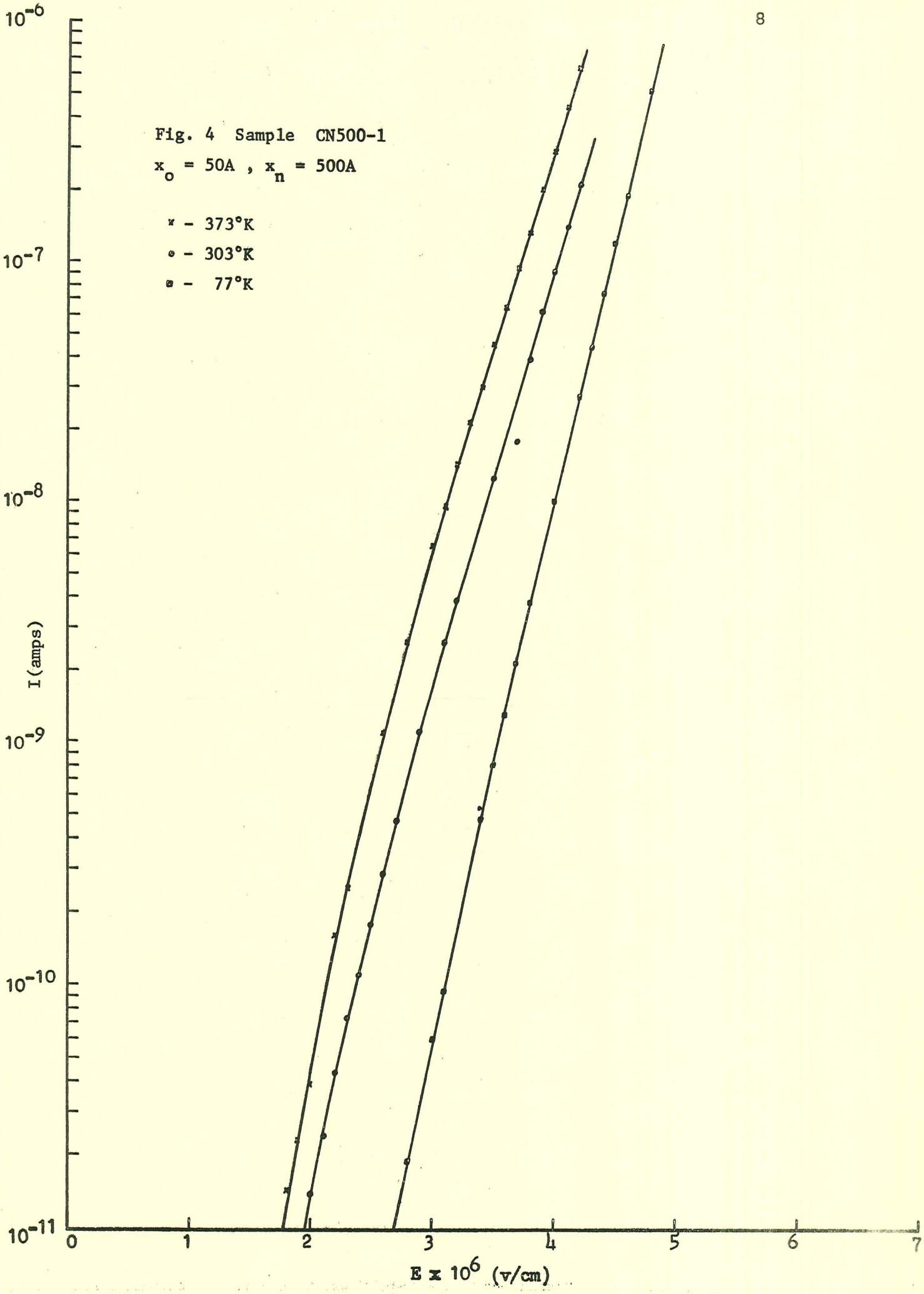


Fig. 4 Sample CN500-1
x_o = 50A , x_n = 500A
× - 373°K
○ - 303°K
□ - 77°K
10^{-6}
10^{-7}
10^{-8}
10^{-9}
10^{-10}
10^{-11}
I(amps)
0
1
2
3
4
5
6
7
E x 10^6 (v/cm)

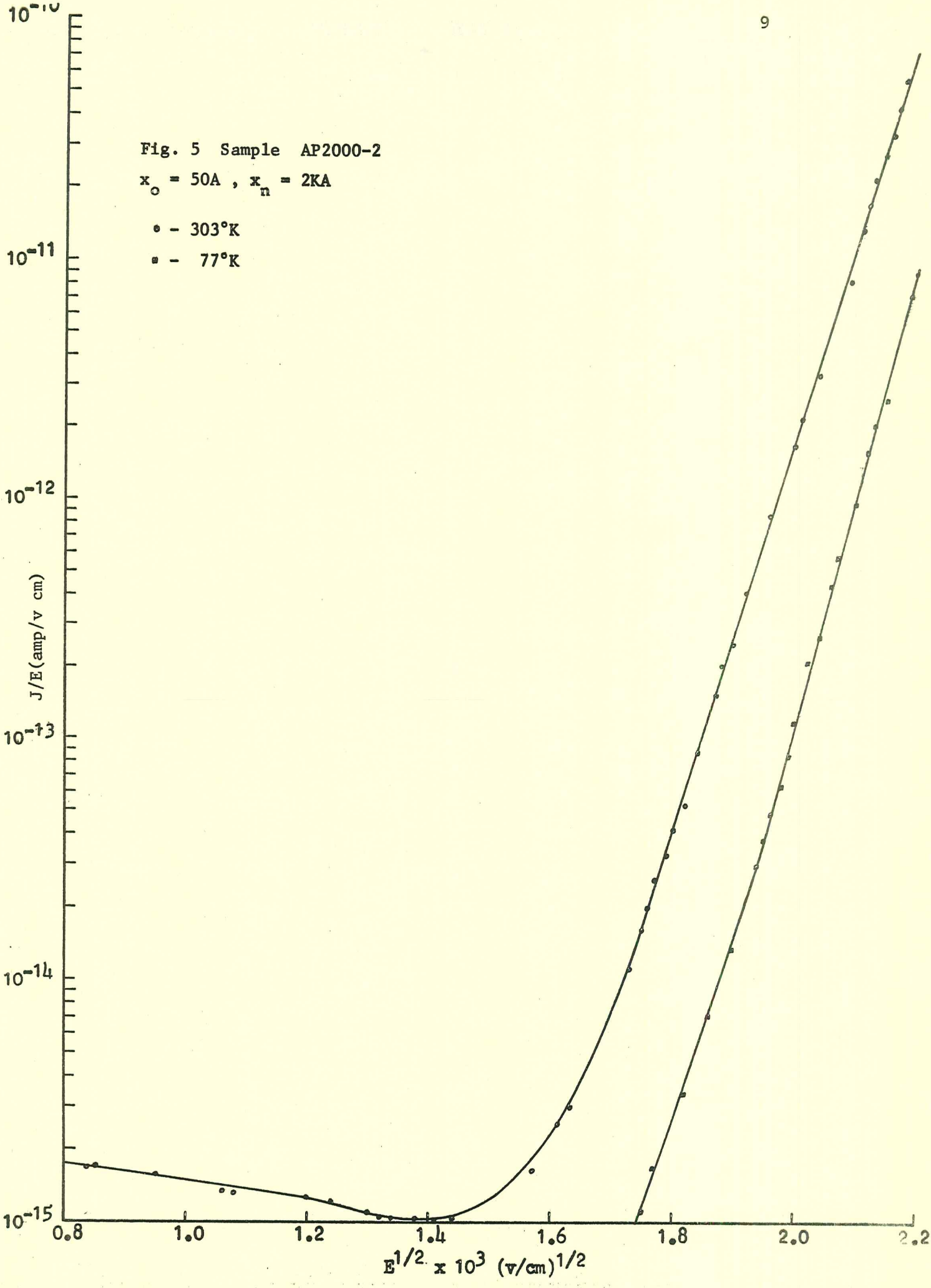


Fig. 5 Sample AP2000-2
x_o = 50A , x_n = 2KA
• - 303°K
▪ - 77°K
10^{-10}
10^{-11}
10^{-12}
10^{-13}
10^{-14}
10^{-15}
J/E(amp/v cm)
0.8
1.0
1.2
1.4
1.6
1.8
2.0
2.2
$E^{1/2} \times 10^3$ (v/cm)$^{1/2}$

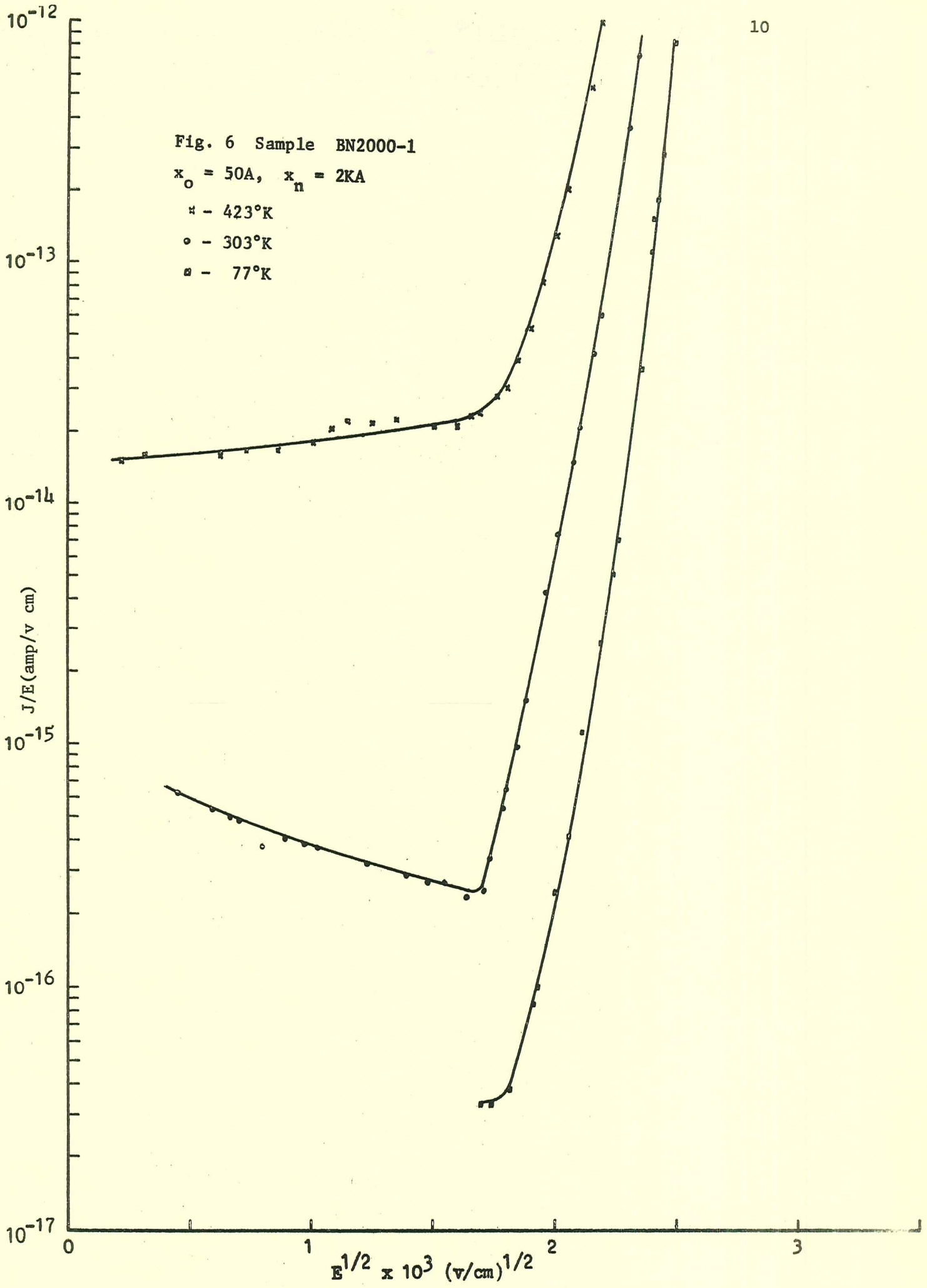


Fig. 6 Sample BN2000-1
x_o = 50A, x_n = 2KA
× - 423°K
○ - 303°K
▣ - 77°K
10^{-12}
10^{-13}
10^{-14}
10^{-15}
10^{-16}
10^{-17}
J/E(amp/v cm)
0
1
2
3
$E^{1/2} \times 10^3$ (v/cm)$^{1/2}$

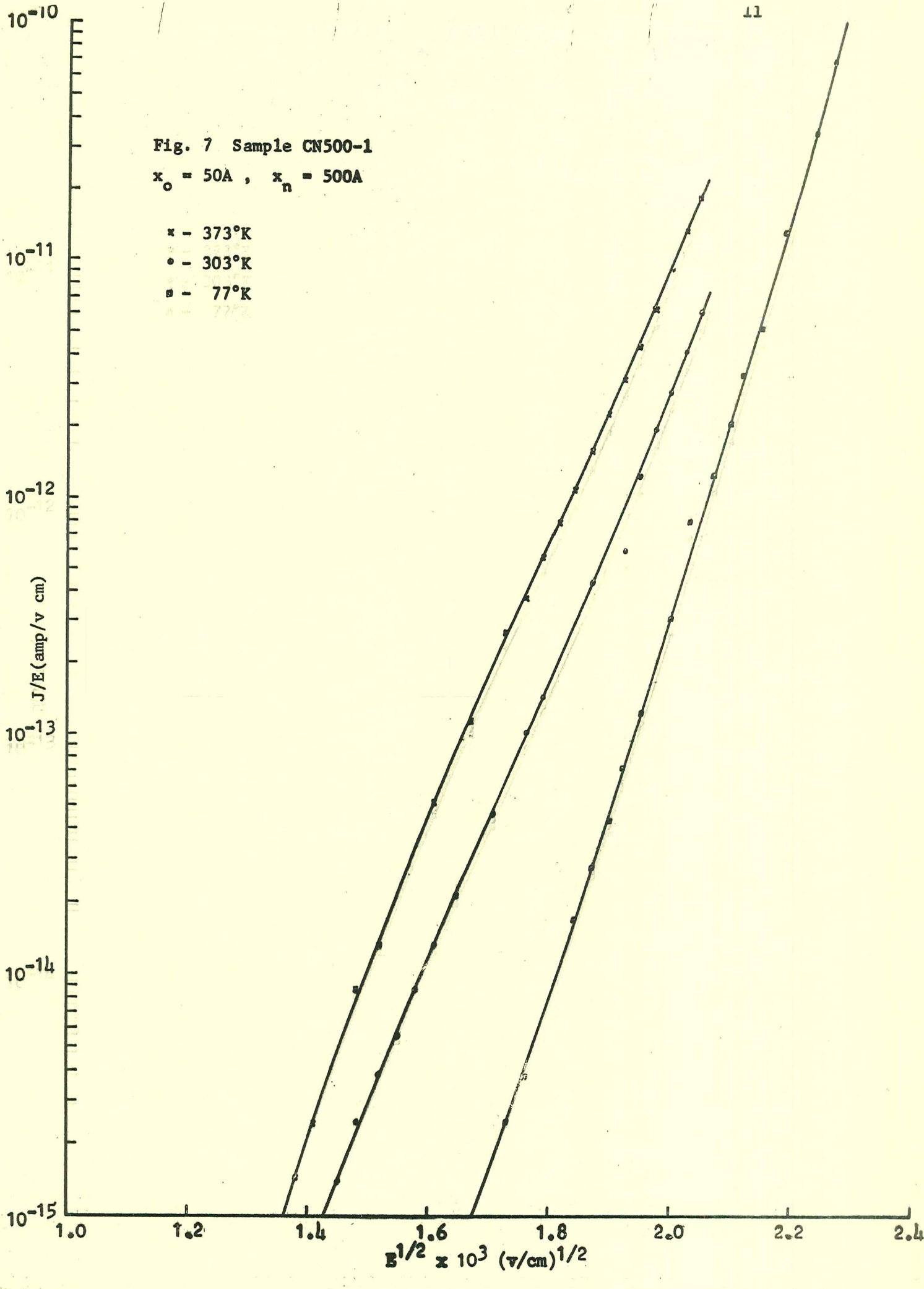


Fig. 7 Sample CN500-1
x_o = 50A , x_n = 500A
× - 373°K
• - 303°K
▪ - 77°K
10^{-10}
10^{-11}
10^{-12}
10^{-13}
10^{-14}
10^{-15}
J/E(amp/v cm)
1.0
1.2
1.4
1.6
1.8
2.0
2.2
2.4
$E^{1/2} \times 10^3$ (v/cm)$^{1/2}$

time was extremely slow (several hours were required to traverse the entire voltage range), indications during testing point to a non-equilibrium charge condition at lower currents. Figures 8, 9, and 10 show log J/ε^2 vs. $1/\varepsilon$. A line of constant, negative slope here suggests field emission. No such line appears here, although a general trend in the proper direction and with roughly the slope given in Reference 1 can be seen. Thus, while the data does not completely preclude the possibility of field emission at high fields, masked by other effects, the linearity of the curves in Figures 5, 6, and 7 and on several other samples not displayed here makes it extremely doubtful that field emission plays a significant role as a conduction mechanism within the range of temperatures and electric fields investigated. Devices which broke down exhibited characteristics over the last few volts which could be attributed to field emission; if so, the breakdown and field emission processes are related. It should be mentioned that the only difference in behavior between the 500Å and 2000Å devices was the lack of a significant ohmic contribution in the thinner samples.

2. C-V CHARACTERISTICS

A very good approximation for the capacitance of an MOS capacitor (p-type silicon) in the depletion mode is[8]:

$$C = \frac{C_o}{\sqrt{1 + \frac{2K_o^2 e_o}{qN_A K_s x_o^2} V}} \qquad (2\text{-}1)$$

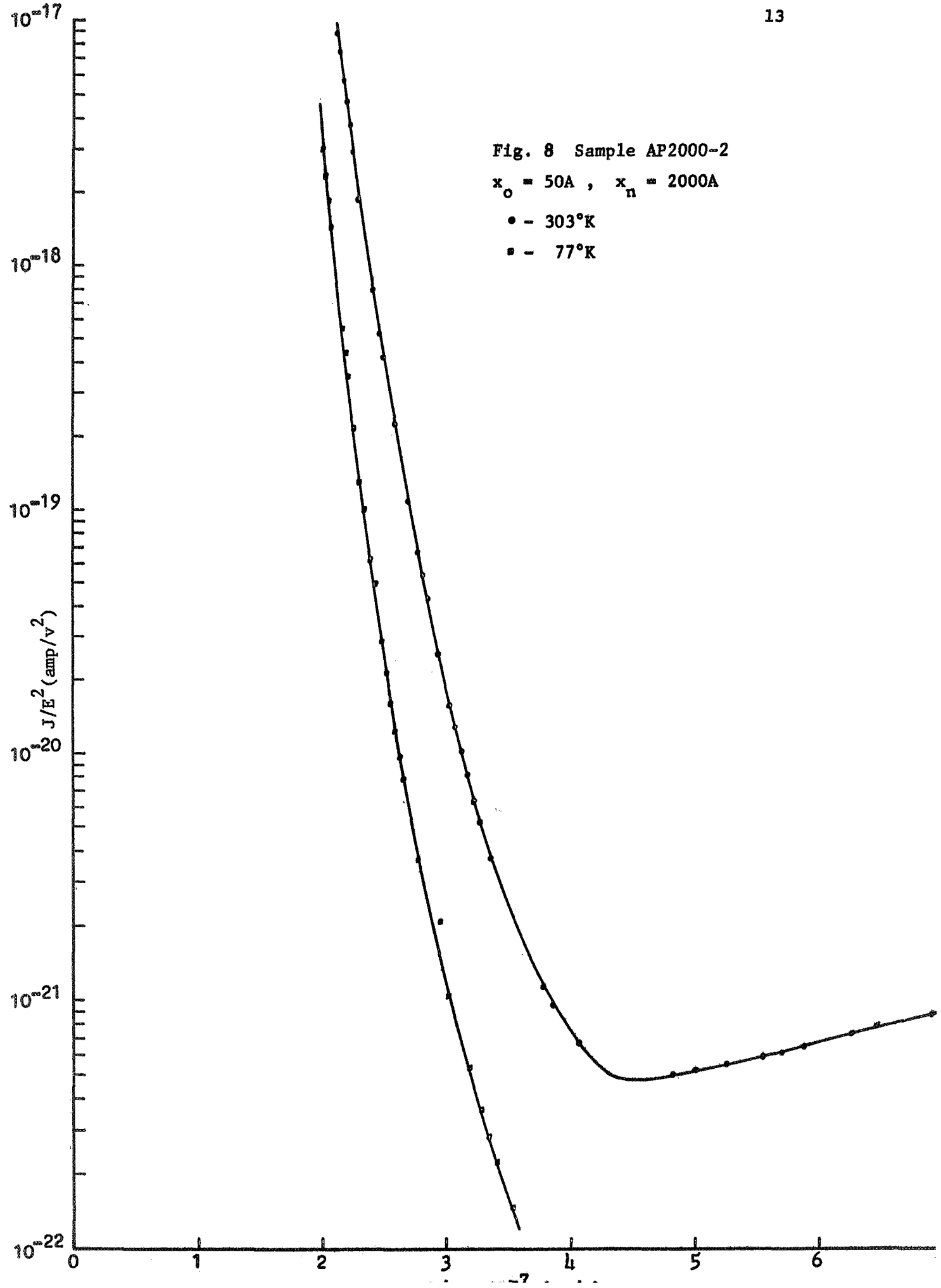


Fig. 8 Sample AP2000-2

x_o = 50A , x_n = 2000A

• - 303°K

▪ - 77°K

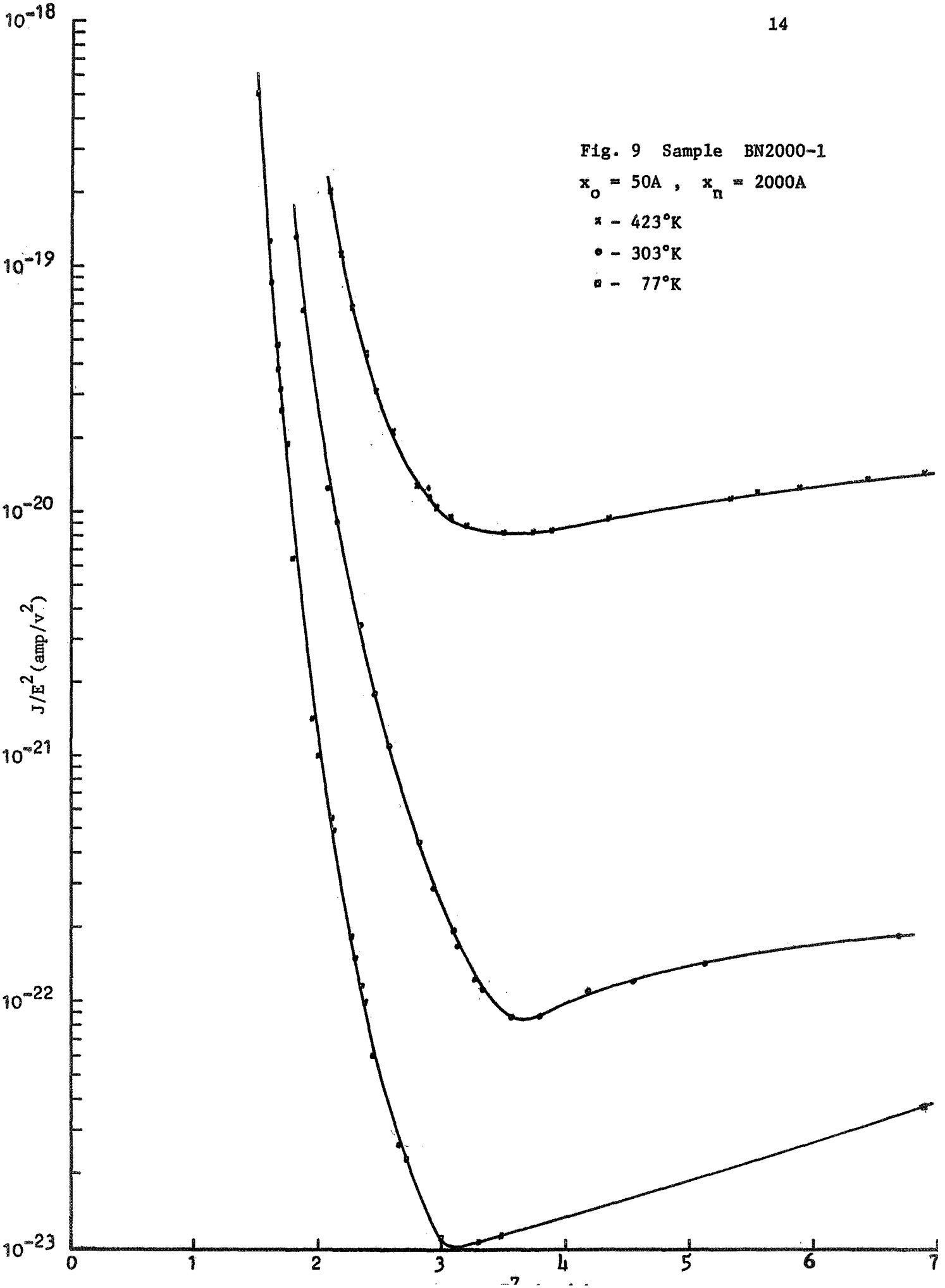


Fig. 9 Sample BN2000-1
x_o = 50A , x_n = 2000A
x - 423°K
• - 303°K
▫ - 77°K
10^{-18}
10^{-19}
10^{-20}
10^{-21}
10^{-22}
10^{-23}
J/E^2 (amp/v^2)
0
1
2
3
4
5
6
7

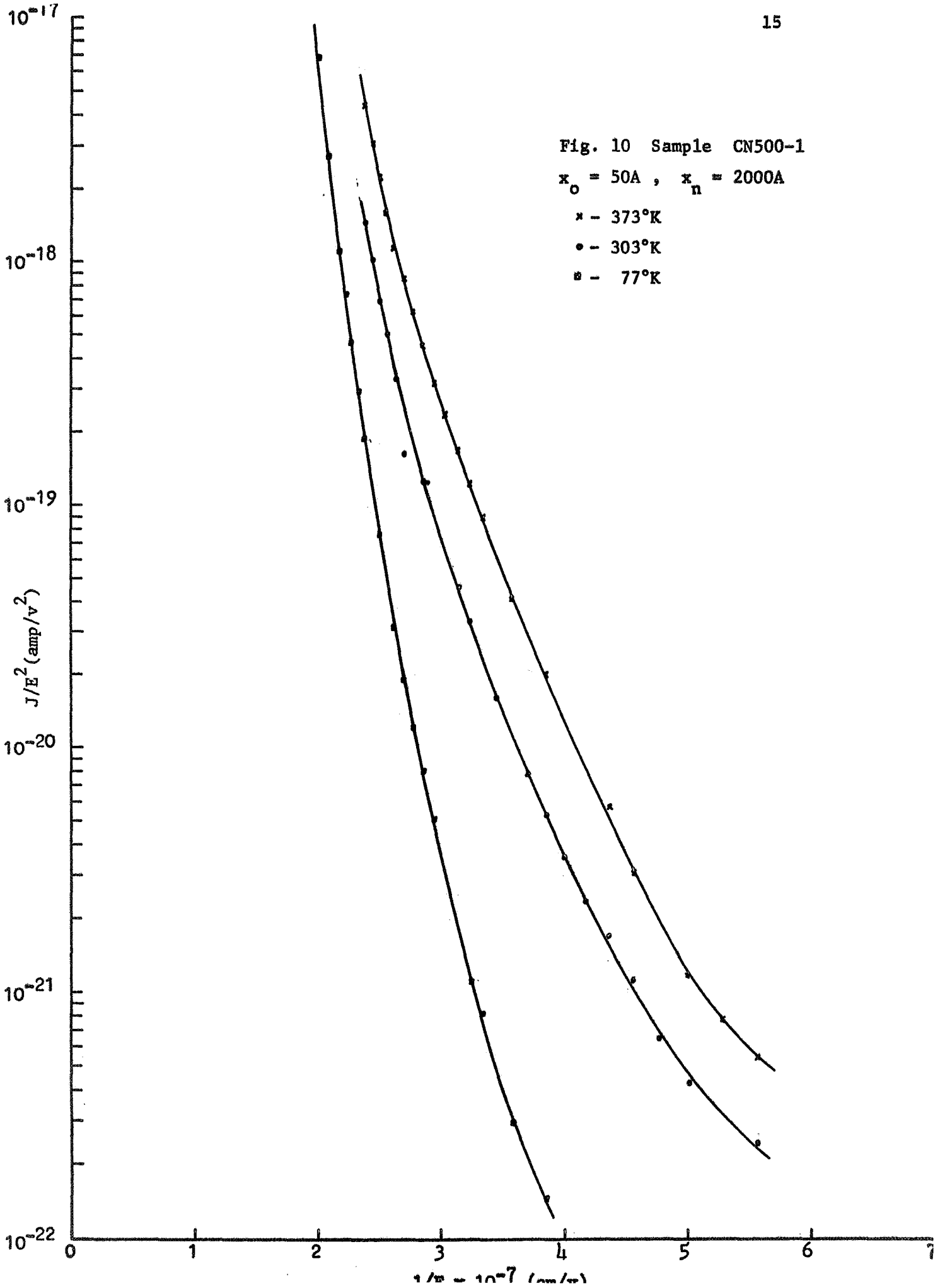


Fig. 10 Sample CN500-1
x_o = 50A , x_n = 2000A
× - 373°K
• - 303°K
▫ - 77°K
10^{-17}
10^{-18}
10^{-19}
10^{-20}
10^{-21}
10^{-22}
J/E^2 (amp/v^2)
0
1
2
3
4
5
6
7
$1/E \times 10^{-7}$ (cm/v)

where:

C_o = oxide capacitance

K_o = oxide dielectric constant

e_o = permittivity of free space

K_s = silicon dielectric constant

N_A = doping density of silicon

q = electron charge

V = applied voltage

x_o = oxide thickness

If $V \leq 0$ (accumulation mode), $C = C_o$ since no depletion region exists. For large positive bias, the interface layer of silicon inverts, and the capacitance approaches a constant minimum $C = C_\infty$. The corresponding voltage is[8]:

$$V = V_{inV} = \frac{2}{C_o}\sqrt{N_A K_s e_o (E_i - E_f)} + \frac{2}{q}(E_i - E_f) \qquad (2\text{-}2)$$

where:

E_i = intrinsic fermi level

E_f = actual fermi level

In the case of an MNOS capacitor, the dielectric constant of the nitride modifies the capacitance expression slightly, but the voltage dependence is still $1/\sqrt{V}$. The effect of stored charge Q_{ss} at the oxide-nitride interface is to shift the curve parallel to the original curve with no stored charge; i.e., Q_{ss} is independent of band bending. Effectively, V is replaced by $V - V_{sh}$ in the capacitance formula, where V_{sh} is the voltage shift (ideally, V_{sh} is the same as the shift ΔV_{FB} in the flatband voltage). The equation obtained by making this substitution fits the

portion of the curve where C varies rapidly with V; however, since it is only an approximation, it does not fit the two "knees" of the curve where C approaches a constant value. As observed by Chu, et al.[9], no hysteresis loop occurs if the bias voltage (v) excursion is limited to a narrow range around the flatband voltage. Increasing the bias voltage beyond this range causes a hysteresis loop which may be enlarged or displaced by changing the endpoints of the voltage excursion. Two other phenomena were observed which agreed with Reference 9 and other work in the literature. First, the hysteresis loop may be shifted back and forth parallel to the voltage axis by the application of voltage pulses. Second, the loop may be shifted to lower capacitances by decreasing the temperature. These points will be discussed below. Figure 11 shows the C-V characteristics of a typical device, illustrating the definitions given above. The approximation equation for C has been rearranged for simplicity.

The flatband capacitance C_{FB} of an MIS capacitor is[10]:

$$C_{FB} = \frac{BC_o}{(B-1) + C_o/C_\infty} \qquad (2\text{-}3)$$

$$B = 3.04 \sqrt{\log_{10} N/n_i}$$

For our samples, the value of B would be 6.7 for the n-type and 7.7 for the p-type. The form of the equation is the same for MNOS capacitors. It is independent of V_{sh}, since the shift is parallel to the original curve.

The symmetry of our data curves indicates[11] that the density of fast surface states or interface states (denoted in the literature by N_{st})

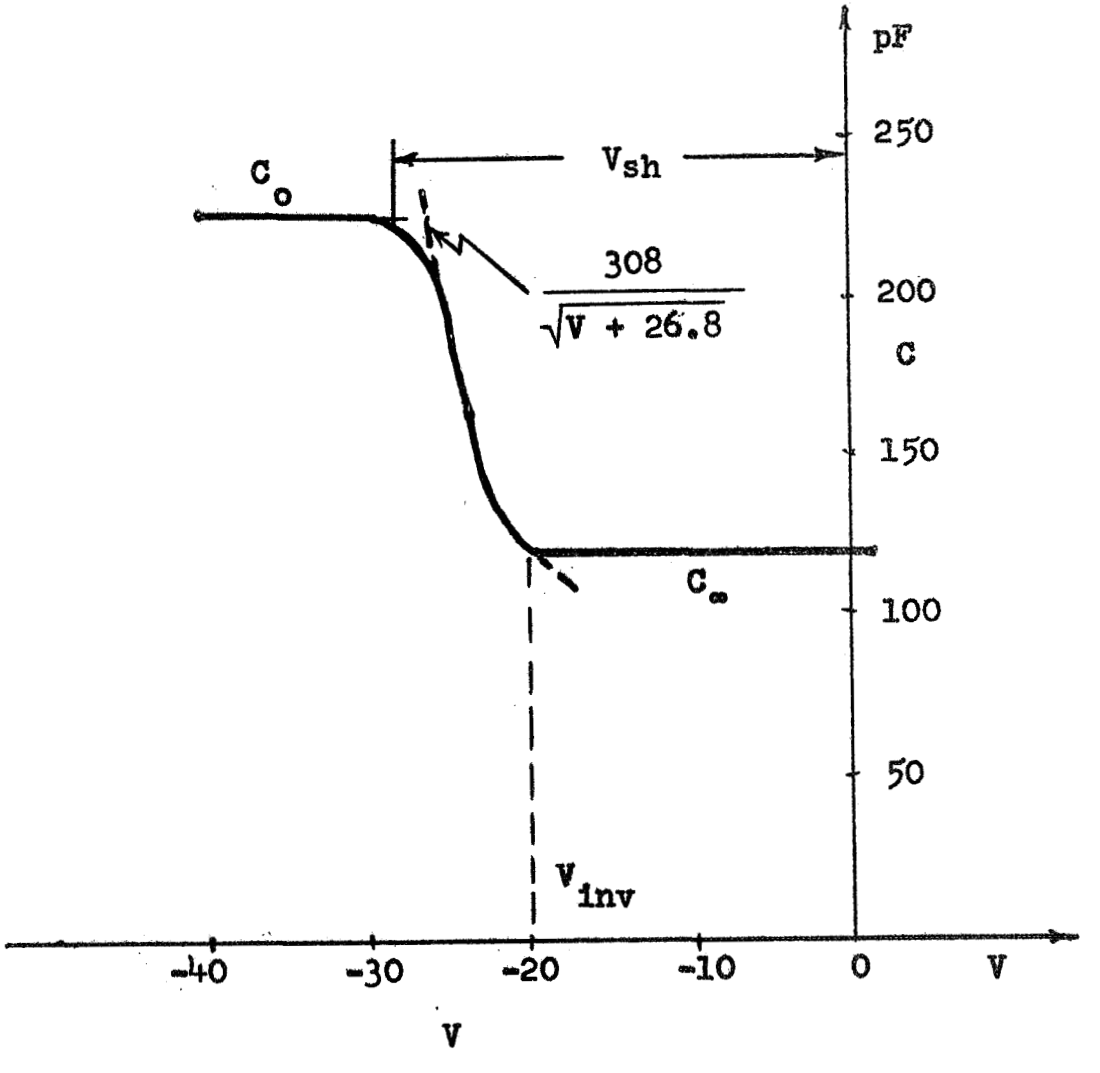


Figure 11. C-V Characteristics of Sample AP2000-1 at 300°K

is negligible. Figure 12 shows the predicted effects and the location of the corresponding energy levels in the energy band gap. Tests run with samples immersed in liquid air, such that the fermi level would shift and accentuate the effects of the fast states, further indicate that N_{st} is negligible. Figure 13 shows the C-V characteristics of a device run at 77°K, illustrating the absence of distortion. The lack of fast surface states gives some indication as to the quality of the devices, since distortion of the hysteresis loop is undesirable.

Tests indicate that a definite pulse height threshold exists before pulsing will shift the flatband voltage and that this threshold is dependent upon pulse width, in agreement with Pao and O'Connell[12]. Repeated pulses of the same polarity yielded a diminishing amount of shift in V_{FB} until a "saturation" occurred. After a shift in V_{FB} was caused by a pulse of one polarity, it was not possible to return to the original V_{FB} by applying an identical pulse of the opposite polarity, again in agreement with Pao and O'Connell, who investigated the net shift after a pair of pulses of opposite polarity. The requirement of large pulses of long duration(e.g., 80 volts, 1 msec.) to obtain a change of a few folts in V_{FB} suggests the need for radical changes in structure from the present experimental devices.

3. EXPERIMENTAL PROCEDURE

3.1 V-I Characteristics

The third progress report gave a detailed description of the automated test equipment, under construction at that time, to be used in obtaining measurements of DC characteristics. As discussed in Section 1, the various conduction mechanisms under investigation are difficult

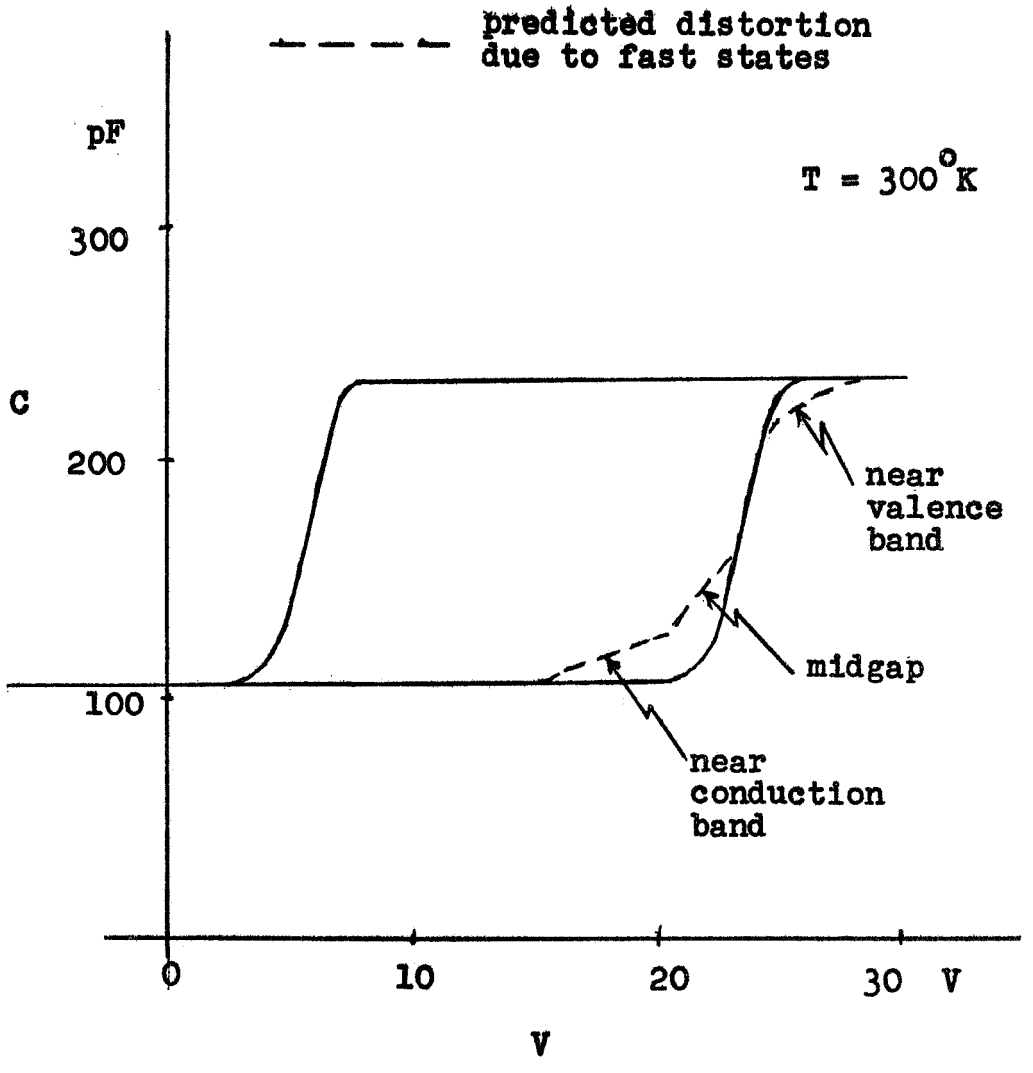


Figure 12. C-V Characteristics of Sample BN2000-4 Showing Lack of Fast States

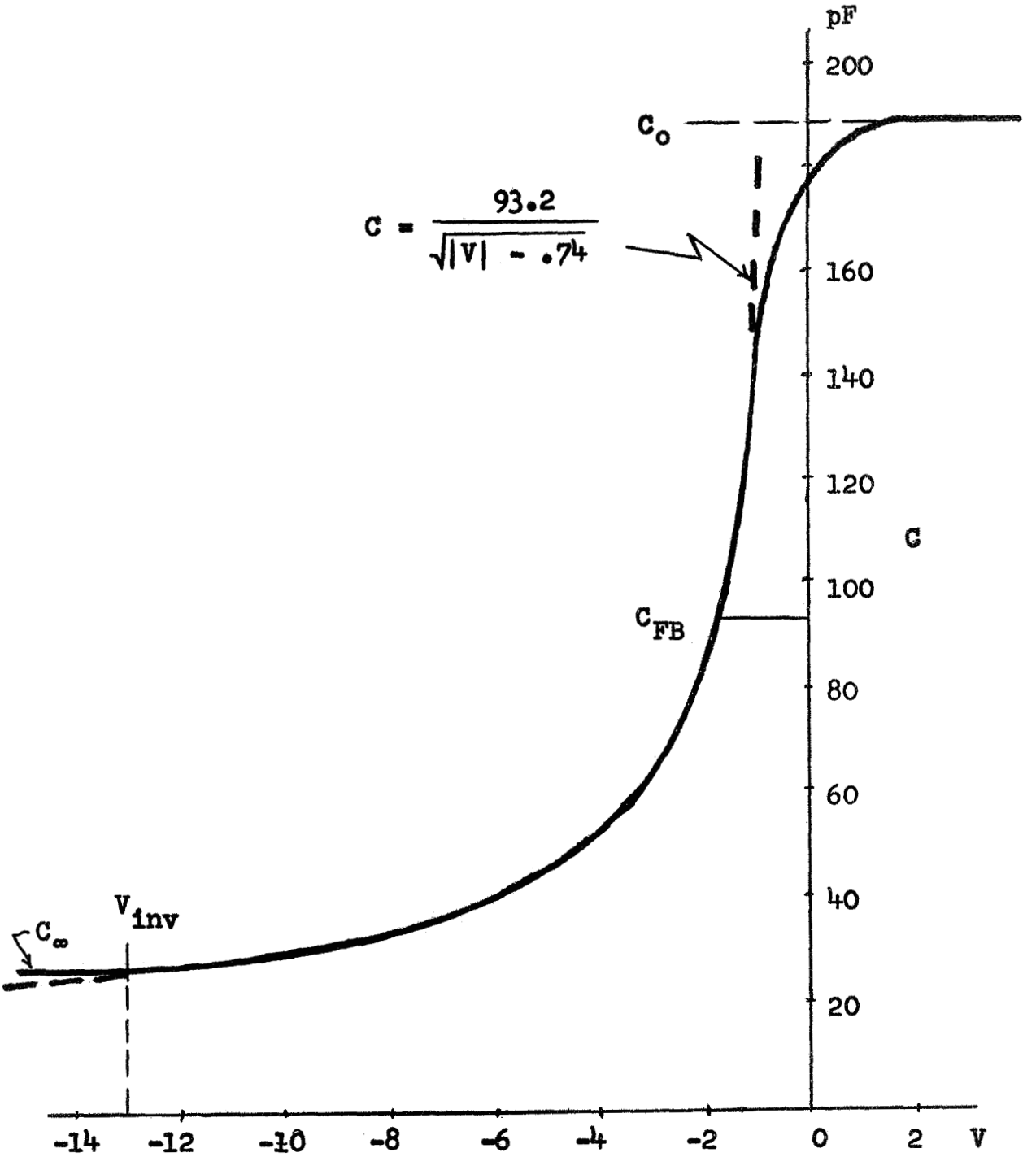


Figure 13. C-V Characteristics of Sample BN2000-6 at 77°K

to distinguish. Consequently, the experimental data must be taken with a high degree of accuracy. The logarithmic amplifier which could be considered as the most vital component in the original system, exhibited considerable instability with respect to time. Most of our data was taken over time intervals on the order of ten hours. In addition to the instability of the logarithmic amplifier considerable difficulty was experienced with the x-y plotter available. Here again the instability was mainly due to the long time periods over which the data was taken, since the plotter was not designed for this use. In order to overcome these difficulties the system shown in Figure 14 was utilized. This system has a disadvantage in that it requires continuous observation, thereby limiting the amount of data which could be taken. However, in obtaining data through this system the voltage readings were taken with a digital voltmeter, which resulted in data that was considerably more accurate than that which could be obtained from the x-y plotter in the automated system.

In the experiments which were conducted at low temperatures, the devices were submersed in a dewar of liquid nitrogen (77°K). The low temperature experiments were conducted in this manner due to the inefficiency of the Statham test chamber with respect to liquid nitrogen consumption at low temperatures and the mechanical failure of the test chamber at these temperatures for time intervals in excess of one-half hour. The mechanical failure was a result of the liquid nitrogen control valve freezing in the open position.

Thus, the data was taken with considerable accuracy but by a time-consuming process which limited the scope of work. While all of the equipment used was known to operate satisfactorily over normal, short-

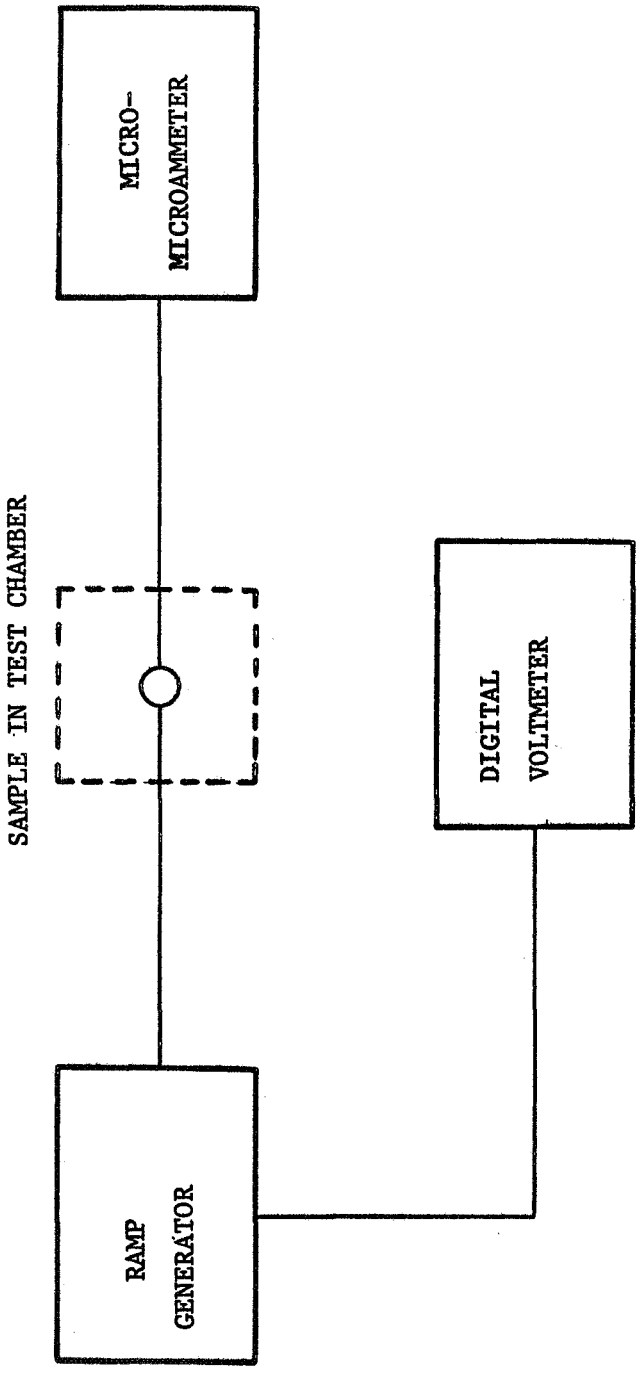


Figure 14. Diagram of circuit for measuring DC characteristics.

term test periods, this had been the first attempt at long-duration use.

3.2 C-V Characteristics

Figure 15 shows the circuit used to measure the capacitance-voltage characteristics. The capacitance of the sample is measured with a Tektronix Model 130 LC Meter which has been modified to provide an output signal proportional to the capacitance measured at the input. At one point within the meter the signal consists of a train of pulses whose separation is proportional to the sample capacitance. A single shot is used to increase the height and width of each pulse, and the pulse train is then "demodulated" to yield a dc voltage proportional to the sample capacitance. This dc voltage is plotted on the y-axis of a Moseley Model 135 x-y plotter, which is calibrated against the reading on the dial of the LC meter. By comparing readings for several standard capacitors measured at the sample holder with those for the same capacitors read directly at the LC meter, stray capacitance of the test jig and bias network was found to be a constant 60 pF. Bias voltage for the sample is provided by a voltage divider and two battery packs. The voltage divider consists of a 10-turn potentiometer driven by a dc motor (1 rpm). A switch is provided for starting, stopping, and reversing the direction of the motor. The bias voltage is plotted on the x-axis of the plotter. A voltmeter is used to monitor the bias voltage during the test, since the maximum and minimum voltages can be read with greater accuracy than that attainable by direct reading of the graph on the plotter. The voltage drop across the limiting resistor R_{lim} is negligible. The primary purpose of this

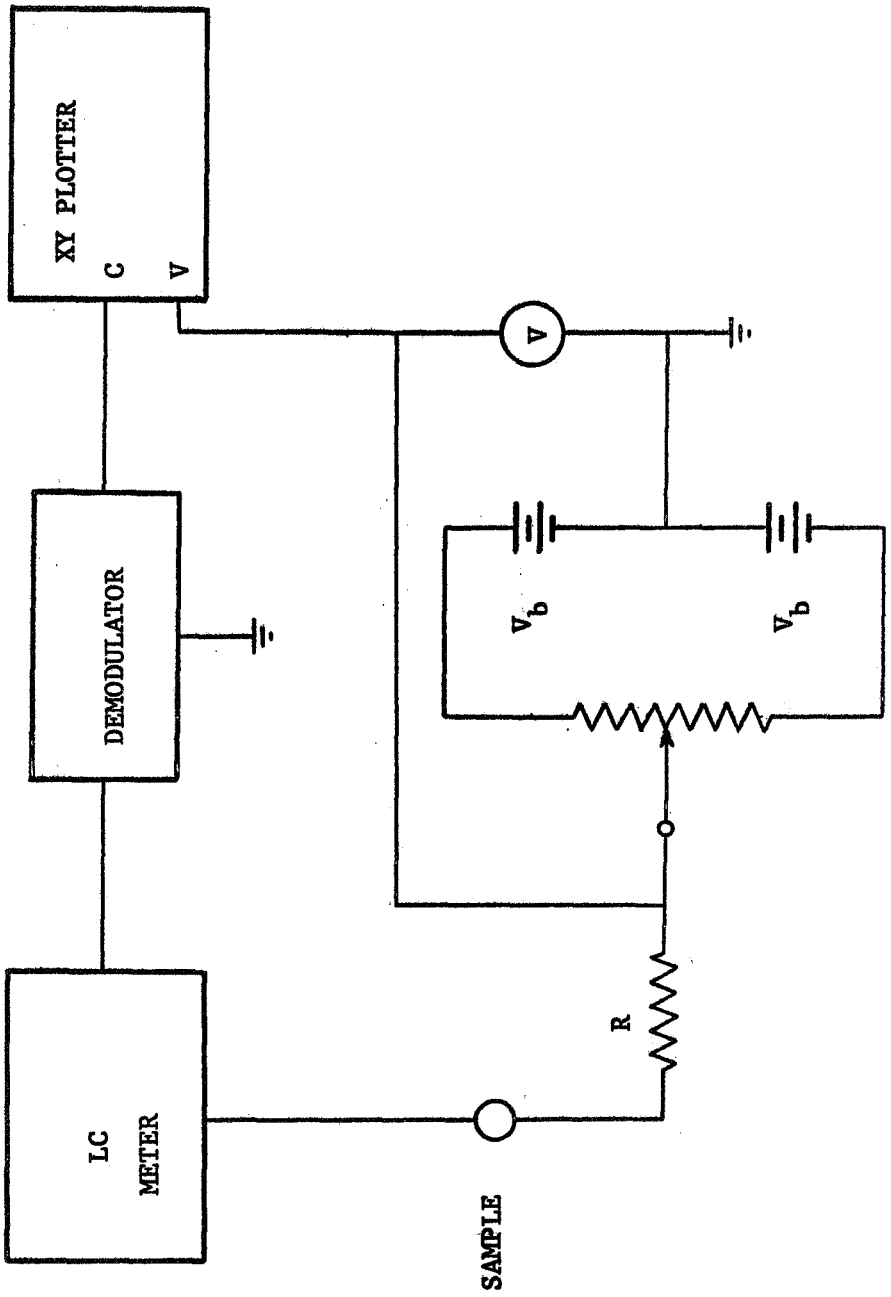


Figure 15. Diagram of circuit for measuring CV characteristics.

resistor is to protect the batteries in case of voltage breakdown of the samples.

The system worked quite well except for the inherent limitation of 300 pF as maximum readable capacitance, which is set by the LC meter, and the fact that only a single measuring frequency (approximately 100 kHz) is used. Having a means of dialing in the maximum and minimum voltage excursions would be convenient for future testing.

SUMMARY AND CONCLUSIONS

The MNOS capacitor acts like an MNS capacitor with an extra interface where a sheet of charge can be stored in slow states; the flatband voltage can be shifted any desired amount over a wide range of voltage by adjusting the density of stored charge. The conduction mechanism in the nitride appears to be primarily the Frenkel-Poole effect with an ohmic contribution at low fields. At high fields, the shape of the curves for field emission and Frenkel-Poole are frustratingly similar, so that field emission is not completely ruled out (though unlikely). Field emission may, however, be tied in with the onset of breakdown. The nitride conduction mechanisms so completely overshadowed those of the thin oxide layer that nothing concrete can be said about the latter.

The C-V hysteresis loop exhibited none of the predicted distortions due to fast surface or interface states, indicating that these will not be a problem in memory applications.

The need for changes in device dimensions and method of preparation in order to optimize shift in flatband voltage upon pulsing is definitely indicated.

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