N70-37091

NASA CR 66976

FEASIBILITY INVESTIGATION OF INSULATED-GATE FIELD-EFFECT TRANSISTORS FABRICATED BY TECHNIQUES COMPATIBLE WITH THICK-FILM TECHNOLOGY

By R. D. Baxter

May 29, 1970

Distribution of this report is provided in the interest of information exchange and should not be construed as endorsement by NASA of the material presented. Responsibility for the contents resides with the organization that prepared it.

CASE FILE COPY

Prepared under Contract No. NAS 1-9220 by
BATTELLE MEMORIAL INSTITUTE
Columbus Laboratories
Columbus, Ohio 43201

Langley Research Center

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

NASA CR-66976

FEASIBILITY INVESTIGATION OF INSULATED-GATE FIELD-EFFECT TRANSISTORS FABRICATED BY TECHNIQUES COMPATIBLE WITH THICK-FILM TECHNOLOGY

By R. D. Baxter

May 29, 1970

Prepared under Contract No. NAS 1-9220 by
BATTELLE MEMORIAL INSTITUTE
Columbus Laboratories
Columbus, Ohio 43201

Langley Research Center

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

TABLE OF CONTENTS

LIST OF TABLES

LIST OF TABLES
(Continued)

LIST OF FIGURES

FEASIBILITY INVESTIGATION OF INSULATED-GATE FIELD-EFFECT TRANSISTORS FABRICATED BY TECHNIQUES COMPATIBLE WITH THICK-FILM TECHNOLOGY

By R. D. Baxter

Battelle Memorial Institute
Columbus Laboratories
Columbus, Ohio 43201

SUMMARY

Techniques were investigated for depositing semiconducting layers at temperatures below those commonly used in the firing of thick-film pastes, which would thereby reduce the effects of contamination of the semiconductor by diffusion of migrant impurities from adjacent thick-film layers or components. The semiconductors employed in this study, PbS and CdS, were selected on the basis of a previous study(1)* performed at Battelle for the National Aeronautics and Space Administration.

PbS layers were precipitated at room temperature from aqueous solutions of lead acetate and thiourea using a modified Kicinski technique. The layers were p-type as deposited, with hole mobilities in the range 5 to 8 cm^2/volt-sec. The properties of as-deposited films and the results of experiments in which films were vacuum annealed and subsequently exposed to air at 25 C are consistent with the notion that the PbS layers are sensitized via oxygen contamination during growth, and that attaining adequate stability and control of film properties would be serious obstacles to the application of these films to TFT's.

CdS layers were pyrolitically deposited by chemical spraying, fogging, and whirler coating using the cadmium chloride-thiourea reagent scheme and by decomposition of organo-cadmium compounds using whirler-coated cadmium acetate-thioacetamide solutions. The crystallinity and sheet resistance of CdS films on Al_2O_3 were found to depend primarily on substrate temperature. Preferred (0002) orientation and resistivity values in the desired 10^3 to 10^4 ohm-cm range were obtained with the cadmium chloride-thiourea reagents at a substrate temperature of 410 C. Comparable values

*References are listed at end of report.

of sheet resistance and preferred crystallinity were not obtained below about 600 C with the cadmium acetate-thioacetamide systems. In addition, the latter mentioned films exhibited enhanced $10\bar{1}0$ orientation. No detectable Hall voltages were obtained on the CdS films. The reason for the apparently low mobilities is unknown.

Dielectric properties of thick-film $BaTiO_3$ layers were obtained as functions of frequency and applied bias by measurements on Au-$BaTiO_3$-Au capacitors.

Attempts to fabricate Au-SiO_2-Au capacitors by the low-temperature SiO_2-deposition technique were unsuccessful because of the occurrence of cracks, voids, and pinholes in the SiO_2 layers.

MIS (metal-insulator-semiconductor) and IGFET (insulated-gate field-effect transistor) structures employing thick-film gold electrode, $BaTiO_3$ dielectric, and chemically deposited PbS and CdS layers were also fabricated and evaluated. No field-effect modulation was observed. Evidence for physical and chemical incompatibilities between the $BaTiO_3$ and semiconducting layers was obtained.

It is concluded on the basis of this work that wet chemically deposited PbS and screen-printed $BaTiO_3$ are not promising candidate materials for thick-film IGFET applications. Continued investigation of low-temperature processes for deposition of CdS and SiO_2, however, is recommended.

INTRODUCTION

This is the Final Technical Report on the subject program and covers the research accomplishments from July 31, 1969, to May 31, 1970. The objective of the program was to investigate experimentally the use of low-temperature semiconductor-deposition techniques in fabricating thick-film active devices.

Previous attempts to produce an all thick-film, insulated-gate, field-effect transistor were generally unsuccessful because of contamination and degradation of the semiconductor and/or adjacent thick-film layers (electrodes, dielectric) by migrant impurities and the corrosive action of fluxes during firing.[2,3] The deposition of semiconducting layers by low-temperature techniques after thick-film firings have been completed avoids

the necessity of heating the entire metal-insulator-semiconductor laminate to high temperatures, and thereby decreases the likelihood of contamination.

Principal emphasis during the present program was on the application of the low-temperature deposition technique for the growth of PbS and CdS layers of sufficient quality to permit evaluation of their usefulness in inverted coplanar IGFET structures, and on investigation of the interactions between the semiconductor and adjacent electrode and dielectric layers.

EXPERIMENTAL DETAILS

Materials, Processes, and Fabrication Techniques

Substrate

Substrates used in this investigation were Alsimag 772, 99.5 percent Al_2O_3, obtained from American Lava Corporation. Substrate dimensions were 1 by 1 by 0.025 inch. The surface roughness according to the manufacturer's specifications, and subsequently verified at Battelle, was $\leq$8 microinches. It was this latter factor which prompted the use of Alsimag 772 substrates since it was felt that the smoother substrate surface available with this product than with the more conventional thick-film Al_2O_3 substrates afforded the opportunity to achieve smoother, more planar device structures. The substrates were vapor degreased and oven dried at 125 C prior to use.

Electrodes

Du Pont 8115 conductive gold paste was employed as thick-film source, drain, and gate electrodes in TFT structures and as $BaTiO_3$ thick-film capacitor electrodes. The electrodes were printed through a 200-mesh screen, dried for 20 minutes at 125 C, and fired at temperatures between 750 and 1000 C. Du Pont 8083 Pd-Au paste was also employed, primarily as a gate electrode under a $BaTiO_3$ gate insulator.

In some experiments, aluminum source and drain electrodes were evaporated into semiconducting CdS layers in order to compare the relative behavior of gold and aluminum electrodes.

Dielectrics

Both thick- and thin-film dielectric layers were prepared in this investigation. The thick-film dielectrics were Du Pont products EX 8289 and DP 8229 $BaTiO_3$ ferroelectric pastes. The layers were screen printed through a 325-mesh screen onto bare 1 by 1-inch Al_2O_3 substrates and onto substrates containing thick-film electrode patterns. After printing, the dielectric patterns were dried at 125 C for 20 minutes and fired at 900 to 1000 C. Fired thickness of layers printed from "as-received" pastes varied from 1 to 1.5 mils. By thinning the paste with n-butyl acetate, fired thicknesses of about 0.5 mil were achieved.

Thin-film SiO_2 layers were deposited initially from a suspension of SiO_2 in methanol (Emulsitone Silicafilm) and later by the oxidation of SiH_4. In the former method, the substrate was completely covered with the SiO_2 suspension and then spun at 1850, 3000, or 10,000 rpm for 30 seconds. The coated substrate was then cured at 200 C for 20 minutes in air. Further densification of the SiO_2 film was accomplished by heating in air at temperatures up to 1000 C. Although the technique has proven to be an effective means for depositing continuous, uniform coatings of SiO_2 onto silicon and other semiconductors, it did not prove satisfactory for the deposition of SiO_2 films onto screen-printed gold electrodes. This will be discussed more fully in a later section.

SiO_2 was also deposited by the controlled oxidation of silane, SiH_4, using the method described by Goldsmith and Kern[4]. Source materials were commercially obtained argon, containing 3 percent SiH_4, high-purity dry nitrogen, and oxygen. A hot plate served as the substrate heater. The apparatus employed was similar in appearance to that described in Reference (4). Flow rates for the SiH_4/A, N_2, and O_2 were 100, 1800, and 50 ml/min, respectively. The 100 ml/min flow rate for SiH_4/A corresponds to a SiH_4 flow rate of 3 ml/min, yielding an O_2/SiH_4 ratio of about 16. Depositions were made simultaneously onto thick-film gold on Al_2O_3, and onto polished silicon substrates. The latter were then used to estimate SiO_2 thickness on the assumption that deposition rates were the same on the silicon and gold. With this method also, problems were encountered in obtaining continuous coatings free of pinholes.

Semiconducting Layers

PbS. PbS layers were deposited by wet chemical methods onto bare Al_2O_3 substrates and onto substrates containing thick-film-gold electrode

and $BaTiO_3$ dielectric patterns. The chemical reagent scheme employed was that described by Kicinski[5], and is based on the precipitation of PbS from an aqueous solution of lead acetate and thiourea upon addition of sodium hydroxide. In the standard Kicinski method, the substrates are immersed in a mixture consisting of 60 cc of a 2 percent (by weight) aqueous solution of $SC[NH_2]_2$ and 30 cc of a 40 percent aqueous solution of $Pb[C_2H_2O_2]_2$, following which 2 cc of a 66-2/3 percent aqueous solution of NaOH is added dropwise. After 1 minute, an additional 8 cc of the NaOH solution is added. The substrates are removed from the deposition container after 10 minutes, washed in deionized water, and dried by heating to 100 C for 10 minutes in air.

During this investigation, variations of the Kicinski method were explored in an attempt to optimize such film properties as physical appearance, thickness, adherence, and electrical properties. Factors investigated for their influence on the resulting films included:

(1) Geometry of the container in which the depositions were accomplished

(2) Geometrical orientation of the substrates (e. g., horizontal, vertical, suspended, resting on bottom, etc.)

(3) The stage of the reaction at which the substrates are introduced

(4) Agitation or stirring of the solution during addition of NaOH

(5) Variation of the Pb/S ratio in solution

(6) Impurity additions during growth.

The effects of postdeposition heat treatment on the electrical properties of PbS layers were investigated both in air and under a vacuum of 10^{-5} mm Hg at temperatures up to 400 C. The vacuum anneals were carried out in a bell-jar-type vacuum evaporator equipped with a resistance-heated substrate holder. Substrate temperatures were monitored with a Chromel-Alumel thermocouple which was imbedded in the heater pattern. Heat treatments in air were accomplished with a thermostatically controlled hot plate or in a resistance-heated oven with a static air environment.

CdS. Two chemical reagent systems and a number of experimental methods for depositing CdS films were investigated. The first system, developed by Chamberlin and Skarman[6], is the chemical spray process. In this process, a 0.001 to 0.05 M solution of cadmium chloride and thiourea dissolved in an appropriate solvent is sprayed onto a heated substrate. Film formation occurs via pyrolitic decomposition of the complex $Cd[(NH_2)_2CS]_2Cl_2$ and subsequent precipitation of stoichiometric CdS, all sulfur excesses apparently being driven off as SO_2 and H_2S at the elevated substrate temperature.

According to Reference (6), the physical properties of spray-deposited films depend on such parameters as degree of atomization of the spray, concentration of the spray solution, substrate temperature, and nature of the substrate.

In general, the best results are obtained with a finely atomized spray, a dilute solution, and a high substrate temperature.

In the present investigation, spray depositions were carried out with two different spray nozzles – one of these, a DeVilbiss No. 40 nebulizer afforded the use of a very finely atomized fog (~1-μ droplets). Typical spray rates were about 250 ml/hour. Both water and methanol were used as solvents for the $CdCl_2$ and $CS(NH_2)_2$. Dry nitrogen was used to pressure the sprayers.

A heated turntable originally intended for use in the deposition of SiO_2 from silane was employed in the CdS depositions at temperatures below 300 C. At higher temperatures, however, the turntable was inoperative and the substrates were placed directly on a hot plate for spray depositions. Spray solutions were obtained either by directly dissolving $CdCl_2$ and $CS(NH_2)_2$ in the appropriate solvent to achieve solutions of the desired low molarity, or by dissolving the solid complex which precipitates from more concentrated (1 M) solutions of these reagents.

Solutions of $CdCl_2$ and $CS(NH_2)_2$ in methanol were also applied to Al_2O_3 substrates by fogging and by whirler coating. In both of these latter cases, the solution was applied to a cold (room temperature) substrate.

Fogging was accomplished with the nebulizer, and whirler coating was accomplished by completely covering the substrate with the reagent solution and spinning the excess off at 1850 rpm for 20 seconds. Between successive coats, the substrates were sintered on hot plates at temperatures up to 410 C. Although fogging could be accomplished either with aqueous or

methanol solutions, whirler coating was restricted to methanol solutions because of the increased wetting afforded by this solvent.

The second scheme investigated for the deposition of CdS layers was based on decomposition from organo-cadmium solution. The particular reagents employed were 1.5 M solutions of cadmium acetate, $Cd(OAc)_2 \cdot 2H_2O$, and thioacetamide (TA) dissolved in glacial acetic acid, HOAc.

The $Cd(OAc)_2 \cdot 2H_2O$ and TA solutions were then combined to give S/Cd ratios of 1:1 and 3:1. The resulting $Cd(OAc)_2 \cdot 2H_2O$-TA-HOAc solutions were applied by the whirler coating technique. For the initial application, four or five drops of solution was required to achieve complete coverage of the substrates. Thereafter, the surface was sufficiently wettable that application of one or two drops produced uniform coverage. A spin cycle of 1850 rpm for 10 seconds was typical.

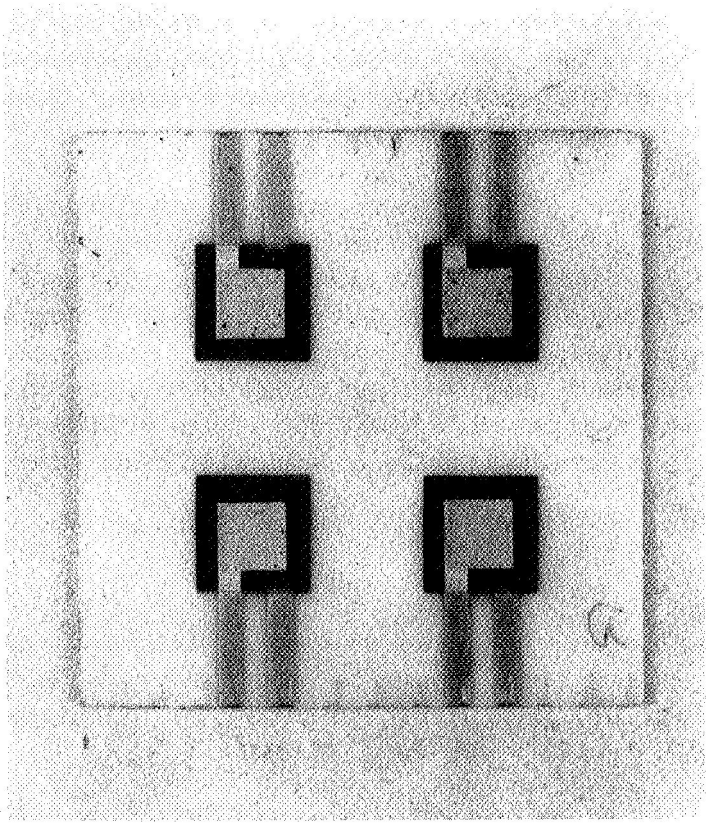
Between successive coats, the samples were sintered in air on hot plates, film side up. Sintering temperatures ranging from 100 to 410 C were employed. Postdeposition heat treatments were performed in a tubular, resistance-heated furnace at temperatures up to 620 C in a static air environment. The high-temperature firings were carried out initially with the film surfaces exposed, and resulted in the formation of a high-conductivity skin which appeared to be CdO. This problem was overcome by firing two samples simultaneously in a face-to-face configuration.

Device Structures

Multiple-layer active and passive device structures fabricated during this investigation include simple parallel-plate capacitors, MIS (metal-insulator-semiconductor) capacitors, and IGFET's (insulated-gate field-effect transistors).

Parallel-plate capacitors employed thick-film gold electrodes and either thick ($BaTiO_3$)- or thin (SiO_2)-film dielectrics.

Figure 1 shows an array of four thick-film capacitors on a 1 by 1-inch Al_2O_3 substrate. The lateral dimensions of the dielectric layers and electrodes shown in Figure 1 are 0.200 by 0.200 inch and 0.120 by 0.120 inch, respectively. The sequence of operations for fabricating such an array was as follows:



3X

FIGURE 1. THICK-FILM Au-$BaTiO_3$-Au CAPACITOR ARRAY

Step 1. Print bottom electrode (Du Pont 8115 gold), dry, fire at 750 C

Step 2. Print dielectric, dry

Step 3. Print top electrode, dry

Step 4. Cofire dielectric layer and top electrode at 850 to 1000 C.

In the case of thin-film dielectric layers Steps 2 to 4 become, respectively:

Step 2'. Form SiO_2 layer by whirler coating with Emulsitone Silicafilm or by oxidation of SiH_4

Step 3'. Densify SiO_2 by heat treatment in air

Step 4'. Print, dry, and fire top electrode.

MIS capacitors were fabricated in an analogous manner, and the same bottom electrode and dielectric patterns were employed. PbS or CdS was then deposited on top of the fired (densified in the case of SiO_2) dielectric. The actual procedure was to deposit the semiconductor over the entire substrate. KPR photoresist was then applied in the form of 0.200-inch-diameter dots registered directly above the dielectric patterns. After etching in dilute HCl to remove the semiconducting layer from the remainder of the substrate, the KPR was removed with trichloroethylene. The structure was completed by evaporating the top electrode which formed ohmic contact with the semiconductor.

Gold and either indium or aluminum were used as top electrode for PbS and CdS, respectively.

IGFET structures were fabricated in both the inverted coplanar and inverted staggered configuration. The ideal configuration from the standpoint of thick-film compatibility is inverted coplanar. Structures of this configuration were fabricated in arrays of four per substrate using methods similar to those described previously in connection with parallel-plate and MIS capacitor structures. In the inverted structures, the gate-electrode array is printed and fired first. Then the gate-insulator dielectric and source-drain electrodes are applied. Finally, the semiconducting layer is applied, masked with KPR, and etched to form the desired pattern. When

$BaTiO_3$ was used as the gate insulator, the $BaTiO_3$ and source-drain electrodes were cofired as in the fabrication of parallel-plate capacitors. Gate electrode and complete inverted coplanar structures are shown in Figures 2 and 3, respectively. Dimensions of the gate-electrode patterns were nominally 0.010 by 0.280 inch for the electrodes themselves and 0.040 x 0.160 for the contact pads shown at the substrate edges. The dielectric pattern, source electrode, and drain electrode have the same geometry as the dielectric and electrode patterns employed in the thick-film capacitors of Figure 1. The thick-film source-drain electrodes were applied by first printing and drying the source (drain) electrodes, then rotating the work (substrate) holder 180 degrees and printing the drain (source) electrodes with the same screen.

Inverted staggered structures were fabricated by printing and firing gate electrodes and dielectric layers in that sequence, depositing the semiconductor film on top of the gate insulator, and finally, evaporating the aluminum source and drain electrodes. These latter structures are not, of course, thick-film compatible, but were prepared solely as a reference structure with which to compare the electrode behavior of true thick-film (inverted-coplanar) structures.

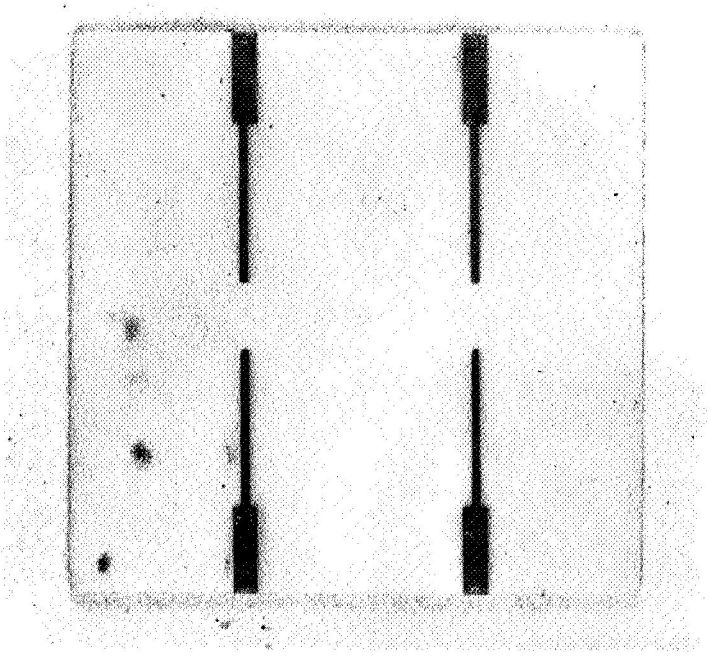
Characterization and Analysis

Semiconducting Layers

The primary method used to characterize semiconducting films of PbS or CdS was the measurement of sheet resistance (R_s), resistivity (ρ), and Hall coefficient (R_H).

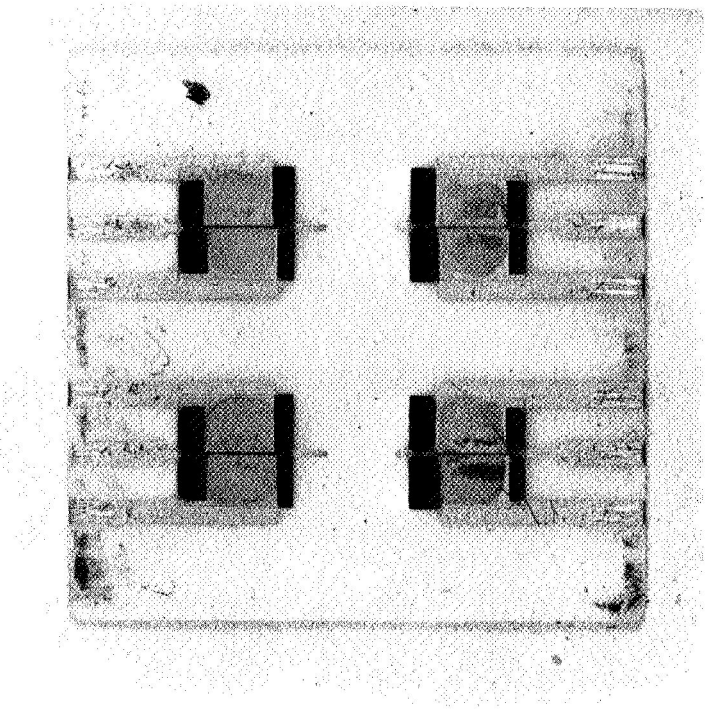
Sheet resistance was measured either by standard four-probe techniques with a Texas Instruments Model 635B crystal ρ meter or by two-terminal resistance measurements on an array of semiconducting film elements of fixed geometry, using a Keithly Model 610 B electrometer as an ohmmeter. Figure 4 shows such an array of 10 CdS semiconducting elements. Electrical contact to each end of the individual elements is provided by thick-film gold electrodes.

The array was prepared by printing and firing the electrode pattern, depositing CdS (or PbS) onto the entire substrate, and then forming the desired pattern of semiconducting elements by masking and etching. Measurements were made of the resistance and I-V characteristics of the individual elements and of series combinations of elements. From these



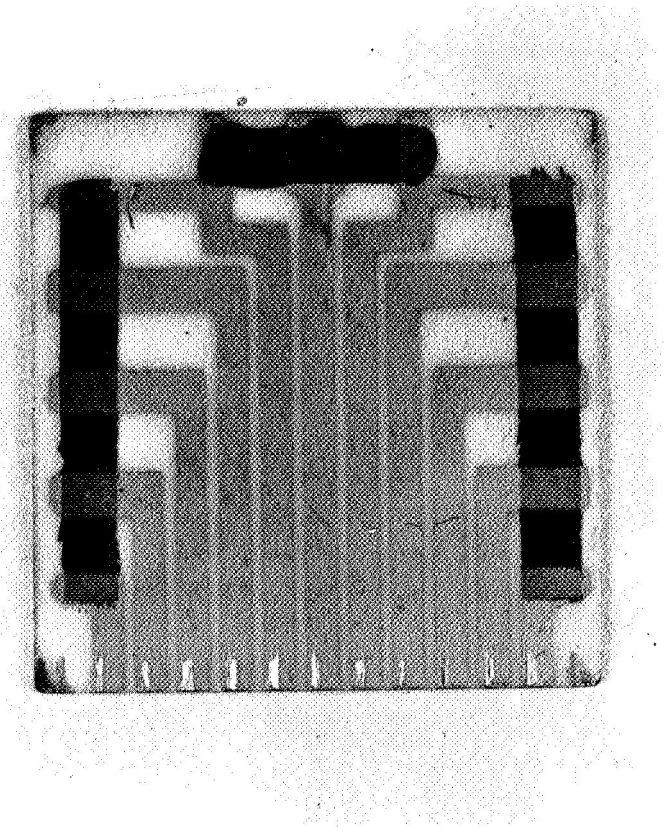
3X

FIGURE 2. THICK-FILM GOLD-GATE ELECTRODE ARRAY



3X

FIGURE 3. INVERTED CO-PLANAR IGFET ARRAY



3X

FIGURE 4. TEN-ELEMENT ARRAY OF CdS RESISTORS

data, both the spatial uniformity of the films and contact effects could be determined.

The Van der Pauw[7] method was used to obtain Hall coefficient and resistivity data. Square samples, obtained by sawing 1 by 1-inch substrates into nine equal 0.32 by 0.32-inch elements, were employed. Each element was provided with four ohmic contacts by evaporating indium dots or by applying an In-Ga mixture with a soldering pencil. In the case of low-resistance ($\leq 10^4$ ohms) films, voltage measurements were made with a Leeds and Northrup Type K-3 potentiometer, and sample current was provided by an Electronics Measurements Model C-612 constant-current supply. For higher resistance films, batteries were used as a current source, and voltages were measured with a Keithly Model 610 B electrometer. A magnetic flux density of 8770 gauss was employed in the Hall-coefficient measurements. Carrier concentration, n, and mobility, μ, were obtained from the simplified expressions $n = 1/R_H e$ and $\mu = \mu_H = R_H/\rho$; i.e., the Hall-coefficient factor was assumed equal to unity.

Homogeneity of each element was estimated from the ratio $R_{12,34}/R_{23,41} = (V_{34}/I_{12})/(V_{41}/I_{23})$, where the subscripts indicate the pairs of contacts being used as current (I) and potential (V) electrode. The enumeration of the contacts is arbitrary so long as they are numbered consecutively from 1 to 4 around the periphery of the specimens. For a completely homogeneous specimen with the contacts symmetrically located on the specimens edge, the ratio should be unity. In the present work, a value for this ratio in excess of two was taken as an indication of gross inhomogeneity. Spatial uniformity of the films was also determined by comparing the data obtained on each of the nine elements cut from a single substrate.

Semiconducting films were also characterized by a number of metallurgical and analytical methods including optical and electron microscopy, X-ray diffraction, and X-ray fluorescence in order to correlate the effects of film thickness, crystallinity, and composition with the observed electrical properties.

Dielectric Layers

The dielectric properties of $BaTiO_3$ thick-film layers were obtained from measurements of capacitance and dissipation factor as a function of frequency at zero applied bias, using the thick-film capacitor structure

described previously. The measurements were facilitated by a General Radio Type 716-C capacitance bridge, in conjunction with a GR 1210 C oscillator, and a GR 1232A null detector. Measurements of capacitance and conductance as a function of applied d-c bias at fixed frequencies were obtained through the use of a Booton Model 74C 100 K H_3 capacitance bridge. Bias voltage was supplied by a Fluke Model 301 C d-c power supply.

In the case of the fixed-frequency Booton bridge, the capacitance and conductance of the Au-$BaTiO_3$-Au capacitor were measured directly. However, this could not be done with the General Radio bridge since the highest value of capacitance which can be measured with this bridge at frequencies above 1 kHz is 1000 pf, a value below that of the thick-film capacitors. As a result, all measurements with the General Radio bridge were made with the unknown (thick film) capacitor in series with a precision condenser. The values of capacitance (C_x) and dissipation factor (D_x) for the unknown were then calculated from the expressions:

$$C_x = \frac{C'C}{C'-C}, \quad D_x = \frac{DC'-D'C}{C'-C},$$

where the primed symbols denote the values measured for the standard and the unprimed values denote the values measured for the series combination.

All MIS capacitance measurements were made at 100 kHz with the Boonton bridge.

RESULTS AND DISCUSSION

Semiconducting Layers

The device characteristics of an IGFET are strongly dependent on the carrier transport properties of the semiconducting layer. The device transconductance (g_m), for example, is directly proportional to the charge-carrier mobility (μ). The threshold or turn-on voltage is directly proportional to the carrier density (n). Thus, in general, one desires a semiconducting layer with a high mobility and low carrier concentration. In addition, the semiconductor must be physically, electrically, chemically, and metallurgically compatible with the dielectric layer, the source-drain electrodes, and the environment. Finally, the semiconductor must be capable of deposition (1) at a sufficiently low temperature that contamination of the semiconductor

does not occur to any significant degree and (2) by a process that does not alter the properties of other thick-film elements.

Accordingly, a substantial portion of the subject investigation was devoted to the deposition and characterization of the semiconducting films.

PbS

Chemically deposited PbS layers have been used for a number of years in the fabrication of infrared detectors. Consequently, information in the open literature dealing with the effects of deposition conditions, impurity additions, postdeposition anneal, etc., is concerned primarily with optimizing photoresponse rather than transport properties.[8-16] As a result, a rather systematic evaluation of deposition conditions and post-deposition treatments was required in this investigation.

Initial experiments employing the standard Kicinski technique proved the feasibility of depositing continuous, adherent films of PbS onto Al_2O_3 from aqueous solutions of lead acetate and thiourea. The films were deposited onto bare Al_2O_3 and onto Al_2O_3 substrates containing a thick-film gold electrode pattern. The substrates were suspended in a horizontal position in the deposition cell. Adherence to both the Al_2O_3 and gold was good, and the Au-PbS contact was ohmic. Typical values of sheet resistance for these films were on the order of 10^6 ohms/square, irrespective of whether the films were dried in air at room temperature or at 100 C. The films were all p-type as determined by thermal probing. No Hall voltage was detected in any of these early films, indicating that the carrier mobility was low (≤ 3 cm^3/volt-sec). Thus, insofar as the electrical properties were concerned, the films were quite similar to the oxygen-sensitized PbS films discussed in References (10, 13, 14).

Subsequent investigation of the deposition method indicated that film appearance, uniformity, and electrical properties were at least to some degree influenced by the following:

(1) Orientation of the substrate

(2) The state of the reaction at which substrates are introduced

(3) Agitation or stirring of the solution during addition of NaOH.

Uniform coverage of the substrate was accomplished most readily when the substrates were suspended in the deposition cell. Generally, complete

coverage occurred for substrates oriented in either a horizontal or vertical position. The film thicknesses, for a given deposition time, were not the same for these two orientations however. The horizontally oriented films were consistently thinner and consequently exhibited higher values of sheet resistance and a rather different appearance. The difference in thickness was readily observed by optical microscopy. In the case of films grown on horizontal substrates, the structure of the substrate could be seen quite clearly through the film, and no individual crystallites of PbS could be observed. In the case of vertically oriented films, the PbS film were sufficiently thick that the structure of this underlying substrate could not be seen. No differences were visible in the X-ray diffractograph of the two types of films however. In both cases, the only crystalline phase observed was randomly oriented PbS.

It was also observed, in agreement with other workers[5], that if the substrates were inserted into the growth cell after precipitation of PbS had commenced, adherent films could not be obtained.

As will be discussed in more detail later, a number of intermediate chemical reactions occur during PbS deposition, and some of these reaction products may have unfavorable effects on film properties. Therefore, in all subsequent depositions, the substrates were oriented vertically. This configuration yielded the largest apparent growth rate, and, thereby, the length of time the substrates remained in the deposition cell was decreased.

Methods investigated in an attempt to improve the electrical properties of deposited films included variation of the Pb/S ratio in solution to adjust stoichiometry and the addition of $AgNO_3$ to further speed up deposition[9]. Neither of these methods produced any significant improvements. Improved film properties were obtained, however, when the deposition solution was stirred right up to the point where PbS precipitation commenced. Representative data for films prepared in this manner are shown in Table I. The highest value of Hall mobility achieved was 34 cm^2/volt-sec, but the typical values achieved with the deposition techniques employed were 5 to 8 cm^2/volt-sec.

It should be observed that the films were still p-type, indicating that even these "higher" mobility films were in effect sensitized and not unlike O_2-annealed PbS film detectors. It seems reasonable to conclude then that the Kicinski technique as employed here with Al_2O_3 substrates produces a chemical sensitization which makes postdeposition oxidation unnecessary.

The results of vacuum-annealing experiments were also consistent with the notion that as-deposited films were oxygen sensitized. Table II gives the electrical properties of a number of chemically deposited PbS

TABLE I. ELECTRICAL PROPERTIES OF CHEMICALLY DEPOSITED PbS

Substrate Position	Sample	$\frac{\rho}{t}$, 10^4 ohms/square	$\frac{R_H}{t}$, 10^5 cm^2/coulomb	μ_H, cm^2/volt sec
	1(a)	--	--	--
	2	4.32	+3.04	7.0
	3(a)	--	--	--
	4	6.39	+4.88	7.6
	5	2.43	+1.28	5.3
	5-a(b)	3.24	+1.79	5.5
	6	5.73	+3.50	6.1
	7	6.98	+4.44	6.4
	8	3.72	+2.58	6.9
	9	4.37	+2.75	6.2

1	2	3
4	5	6
7	8	9

(a) No deposit; masked by substrate holder.
(b) Back side of sample.

TABLE II. EFFECT OF VACUUM ANNEALING ON THE ELECTRICAL PROPERTIES OF PbS FILMS

Sample	Before Anneal			Annealing Temp, C	Annealing Time, min	After Anneal		
	$\frac{R_H}{t}$ (a)	$\frac{\rho}{t}$ (b)	μ (c)			$\frac{R_H}{t}$ (a)	$\frac{\rho}{t}$ (b)	μ (c)
2	$+3.04 \times 10^5$	4.32×10^4	7.04	200	60	-1.09×10^4	7.80×10^2	14
4	$+4.88 \times 10^5$	6.39×10^4	7.6	200	15	N-type	N-type	N-type
5	$+1.28 \times 10^5$	2.43×10^4	5.3	200	30	-2.16×10^4	2.70×10^3	8
8	$+2.58 \times 10^5$	3.72×10^4	6.9	200	120	-2.87×10^3	9.16×10^2	3.1
9	$+2.75 \times 10^5$	4.37×10^4	6.3	400	120	N-type	N-type	N-type

(a) Cm^2/coulomb.
(b) Ohms/square.
(c) Cm^2/volt-sec.

films, both before and immediately after vacuum annealing. All of the samples were converted from p- to n-type by the annealing treatment. Normally, PbS as grown from the melt is n-type, the maximum melting point being on the lead-rich side of the stoichiometric composition. P-type conduction can be obtained by annealing melt-grown samples in the presence of excess sulfur. Thus, one might postulate incorrectly that chemically grown films are sulfur rich, and that vacuum annealing removes excess sulfur and thereby produces n-type material. That this is not the case is evidenced by the observation that upon exposure to air, the vacuum-annealed films reverted back to p-type at rates which varied from sample to sample. In the case of Samples 4 and 9, Table II, the electrical properties changed so rapidly as a function of time that meaningful Hall data could not be obtained. Both of these samples reverted back to p-type within a matter of a few days. Samples 2 and 8, on the other hand, were still n-type after 28 days, at which time the electrical properties were:

Sample 2: $\frac{\rho}{t} = 5.39 \times 10^3$ ohms/square

$\frac{R_H}{t} = -1.61 \times 10^4$ cm^2/coulomb

$\mu = 2.99$ cm^2/volt-sec

Sample 8: $\frac{\rho}{t} = 1.34 \times 10^4$ ohms/square

$\frac{R_H}{t} = -1.43 \times 10^4$ cm^2/coulomb

$\mu = 1.07$ cm^2/volt-sec

These effects were further studied on arrays of 10 PbS resistor elements having the geometry shown in Figure 4. The resistance of each element was measured prior to annealing and then monitored as a function of time at room temperature, in air, after a 60-minute vacuum anneal at 200 C. The results of such measurements are demonstrated by Figure 5, which represents the time dependence of the ratio R(t)/R(0), i.e., the ratio of resistance at time t to the resistance measured immediately after annealing (t = 0) for a single element. All samples exhibited a peak in R(t)/R(0) at $t = \tau$. The maximum value of the ratio $R(\tau)/R(0)$ and the value of τ varied among the different elements. For all elements however, thermal probing indicated n-type conduction for $t = \tau$ and p-type conduction for $t > \tau$.

The behavior of the annealed samples upon exposure to air is analogous to that observed by Hillenbrand[17] upon exposure of polycrystalline films of n-type PbS to oxygen. One might assume that the same mechanisms are operative. That is, oxygen uptake is assumed to occur via sorption and ionization of oxygen by capture of carrier electrons from the n-type film, chemisorption of oxygen on the PbS surface, and incorporation of oxygen into the lattice by replacement of a sulfur atom with a partial evolution of

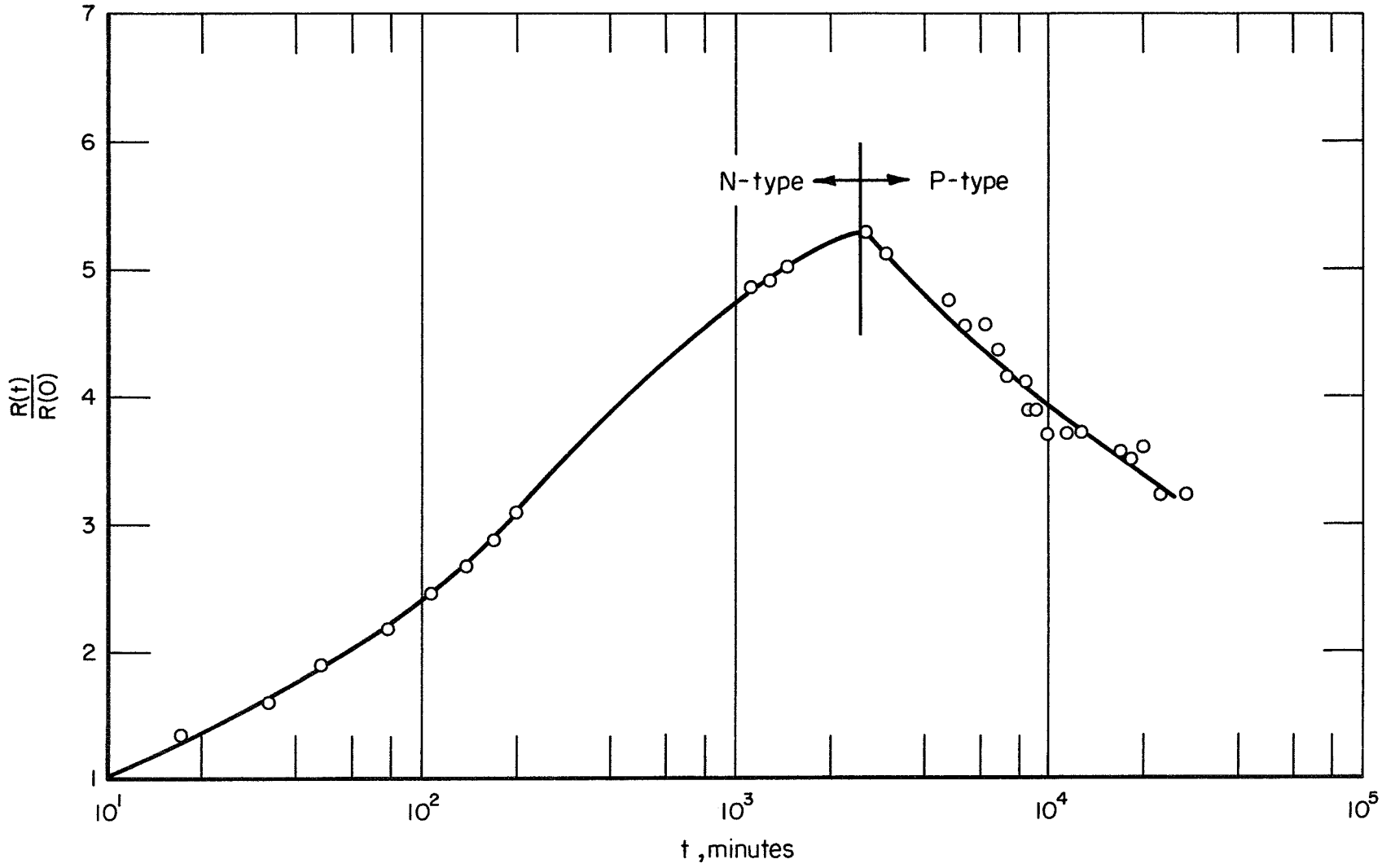


FIGURE 5. RESISTANCE OF VACUUM-ANNEALED PbS FILM AS A FUNCTION OF TIME AFTER EXPOSURE TO AIR AT 25 C

SO_2. It should also be noted that the behavior illustrated in Figure 5 is also similar to that which occurs during the "oxidation" or sensitizing of PbS IR detectors. During the sensitizing process, the films are heated in air or oxygen for a time slightly longer than that required to achieve a peak in film resistance (i.e., $t \gtrsim \tau$). It is at this point that optimum detector properties are achieved. Continued oxidation ($t >> \tau$) results in uniform p-type material and a subsequent decrease in detector performance.

Thus, the results to date lead to the following hypothesis: the PbS films as deposited by the Kicinski technique are "oversensitized". That is, sufficient oxygen is incorporated during the growth process to render the films uniformly p-type. As mentioned previously, the chemical reactions occurring during PbS deposition are rather varied and complex. It is assumed that upon mixing lead acetate and thiourea, a lead acetate thiourea complex is formed according to the reaction $x\ Pb[SC(NH_2)_2] = Pb_x\ [SC(NH_2)_2]_y\ [(C_2H_3O_2)_2]_x$. Addition of the first few drops of NaOH results in the precipitation of $Pb(OH)_2$. Further addition of NaOH results in decomposition of the complex and, ultimately, precipitation of PbS. In addition, however, other reactions occur which result in the formation of lead cyanamide $PbCN_2$ and lead carbonate $PbCO_3$. Oxygen and oxygen compounds such as PbO and $PbCO_3$ are reported to introduce acceptor levels in PbS. Therefore, the appearance of $Pb(OH)_2$ and $PbCO_3$ as reaction products indicates that if these compounds were to be incorporated into the films during deposition, p-type conduction might be expected. Daveydov and Mordvintsev[18] have in fact analyzed PbS layers deposited by the Kicinski method and found them to contain 0.3 mole percent PbO and 0.3 to 0.7 mole percent basic $PbCO_3$. Thus, Daveydov's work indicates that sufficient concentration of oxygen compounds are incorporated into PbS layers during growth to render the layer p-type. The oxygen can be removed to a large extent by vacuum annealing at 200 C; this produces n-type layers, but subsequent exposure to oxygen at room temperature leads to reoxidation and conversion back to p-type films A puzzling point is why the films prepared in this investigation are sensitized "as grown", while other workers find it necessary to perform a post-deposition sensitization. The answer may well be in the nature of the substrate.

The present investigation employed Al_2O_3 as opposed to the glass substrates used by detector manufacturers. Thus, it could be that adsorbed oxygen is already available on the Al_2O_3 surface or that the increased surface area of the rougher Al_2O_3 surface accelerates the oxidation process. In any event, the instability of the electrical properties of PbS films in oxygen represents a serious obstacle to the exploitation of this material in FET's. In particular, it implies that only those films which are sufficiently

oxidized so as to be stable can be employed. However, the carrier concentrations in such films will probably approach 10^{18} cm^{-3}, making appreciable field-effect modulation at reasonable gate voltages unlikely and resulting in large values of turn-on voltage.

CdS

Evaporated thin films of CdS have been successfully employed in the fabrication of IGFET's on glass substrate for a number of years. More recently, screen-printed thick films have been used to fabricate FET's on Al_2O_3 substrates by combined thick- and thin-film processes. However, the production of an all thick-film or thick-film-compatible structure revealed two problem areas[3]:

(a) Damage to other thick-film layers by the corrosive chlorine vapors released during firing of the CdS layers

(b) Degradation of the CdS during firing by migrant impurities from other thick-film layers (e.g., Au electrodes).

In the present work, attempts to overcome these problems centered around the investigation of CdS deposited by noncorrosive chemical techniques which could be carried out either at lower temperature or for shorter times at elevated temperatures.

The first method investigated was the chemical-spray technique employed by Chamberlin and Skarman[6] for the production of CdS photocells, and by Heime[19, 20] for the production of CdS FET's. In both of the above-referenced works, glass substrates were employed. Chamberlin's films, primarily high-resistivity films, were deposited in the temperature range 210 to 310 C. Heime employed a deposition temperature of 350 C, and obtained films with measured Hall mobilities of about 3 cm^2/volt-sec.

In the present work, initial preparations were carried out with a 0.02 M aqueous solution of cadmium chloride and thiourea at substrate temperatures in the range 200 to 300 C. The resultant films exhibited nonuniformity in thickness and in optical clarity, because of variations in droplet size and a nonuniform spray pattern. Attempts to overcome this problem by using a very finely atomized mist (1-μ droplets) generated by a DeVilbiss No. 40 nebulizer proved unsuccessful because thermal convection currents at the heated substrate prevented intimate contact between the mist and the substrate surface.

Improved uniformity was obtained by the use of a heated turntable which carried the substrates through the spray pattern and by using a solution of cadmium chloride and thiourea in methanol, rather than an aqueous solution.

All of the films prepared at temperatures below about 300 C were of the semi-insulating variety, with values of sheet resistance greater than 10^{12} ohms/square.

According to Reference (6), film crystallinity increases with increasing substrate temperature for a given substrate material, and, for a given temperature, film crystallinity is greater for films deposited on amorphous substrates. Recalling that Heime[19, 20] produced marginally acceptable layers on glass at 350 C, it seemed likely that even higher temperatures would be required to produce equally acceptable films on Al_2O_3.

Since the heated turntable could not be operated at temperatures above about 300 C, the effects of increasing temperature were investigated on substrates which were coated with the spray solution by fogging or whirler coating and subsequently fired at the desired temperature. Table III presents the results of X-ray diffractometry for samples fired at 260, 320, and 410 C. The table lists the intensities of the $(10\bar{1}0)$ and (0002) peaks relative to the $(10\bar{1}1)$ peak, the first column being the values expected for randomly oriented crystallites. These data indicate that the degree of preferred orientation along the 0002 direction did increase with increasing substrate temperature.

Also shown in Table III are the effects of deposition technique at a given 410 C substrate temperature. Clearly, the most highly oriented crystalline films are the ones prepared from methanol solutions by spraying and fogging. However, the film showing the least amount of preferred orientation, the whirler coated film, yielded the highest degree of electrical uniformity, as evidenced by resistance measurements on ten-element arrays as described previously. These results are presented in Table IV, which lists the ratio R_i/R_T, i.e., the ratio of the resistance of an individual element, R_i, to the sum of the 10 individual resistances, R_T. For a completely uniform film, the ratio should be 0.10 for each element. Although the criterion is not satisfied for any of the films measured, it is most closely approached by the whirler-coated film. The average values of dark resistance of Films A, B, and C were 1.09×10^{10}, 3.11×10^{8}, and 2.63×10^{11} ohms/square, respectively. Thus, in this case, the film resistance is seen to decrease with increasing crystallinity. Thickness determinations by Talysurf measurements were possible only on Film B.

TABLE III. RELATIVE INTENSITIES OF DIFFRACTION PEAKS FOR CdS FILMS PREPARED FROM CADMIUM CHLORIDE AND THIOUREA

Film	Method of Application	Sintering Temp, C	$\frac{I_{(h,k,-h+k,l)}}{I_{(1,0,\bar{1},1)}} \times 100$			Max Signal Height, percent full scale
			$10\bar{1}0$	0002	$10\bar{1}1$	
Standard random orientation	--	--	75	59	100	--
4-A[a]	Fogging	260	108	160	100	21
5-A[a]	"	320	210	430	100	39
6-A[a]	"	410	204	520	100	75
7-A[b]	Spray	410	220	206	100	33
11-A[a]	Spray	410	130	385	100	Off scale
12-A[a]	Whirler coat	410	270	270	100	13

(a) Methanol solution.
(b) Aqueous solution.

TABLE IV. SPATIAL DISTRIBUTION OF NORMALIZED SHEET RESISTANCE FOR A TEN-ELEMENT ARRAY OF CdS FILM RESISTORS

R_i/R_T[a]	Film A, Continuous Spray	Film B, Fogged	Film C, Whirler Coated
i = 1	0.103	0.109	0.067
2	0.147	0.085	0.140
3	0.229	0.021	0.117
4	0.289	0.010	0.167
5	0.137	0.071	0.078
6	0.0503	0.112	0.104
7	0.0250	0.266	0.042
8	0.0137	0.202	0.097
9	0.0041	0.106	0.094
10	0.0022	0.015	0.094

(a) R_i is the resistance of the ith single element; R_T is sum of the resistances of all ten elements.

The values of thickness determined for various elements on this film indicate a variation in resistivity of 4.1×10^3 to 9.6×10^4 ohm-cm, which represents a considerable amount of spatial nonhomogeneity in the electrical properties.

The goal to produce CdS films with a high degree of crystallinity, improved electrical properties, and improved spatial uniformity prompted the search for an alternative method of deposition: namely, precipitation from solutions of cadmium acetate and thioacetamide in glacial acetic acid.

Previous work at Battelle had established the feasibility of such a technique and indicated that 1.5 M solutions yielded optimum results. More-concentrated solutions decomposed rapidly upon storage at room temperature, and more-dilute solutions required an excessive number of coats to achieve the desired (0.5 to 1 μ) film thicknesses.

The effects of firing temperature on whirler-coated films deposited from cadmium acetate-TA solutions were generally similar to those discussed previously. That is, film crystallinity increased and sheet resistance decreased with increasing temperature. No peaks in the diffractographs corresponding to CdS were observed at all below 410 C. At this temperature, broad, poorly defined peaks first appear, but only for films prepared from solutions with a CdS ratio of 1:1. At 600 C, however, crystalline films with sheet resistances of 10^7 to 10^8 ohms/square were obtained. The sheet-resistance values were thus similar to those obtained with spray solutions at 410 C. However, the direction of preferred orientation was different. In contrast to the (0002) orientation exhibited by sprayed films, the whirler-coated TA films exhibited preferred orientation in the $(10\bar{1}0)$ direction as indicated by the data in Table V. The reason for this difference in orientation between films deposited from $CdCl_2$:thiourea and $Cd(OAc)_2 \cdot 2H_2O$:TA is not understood. It was not a chance occurrence, however. Essentially identical results were obtained on three separate TA-deposited films sintered at 600 C.

The spatial uniformity of these whirler-coated films was good. No Hall voltages were detected, however. Attempts to increase film mobility to a measurable level by baking the film in air were unsuccessful. In fact, when films were sintered at temperatures above about 500 C with the film surface exposed to air, a relatively highly conducting skin formed. Formation of this skin, later identified as CdO, was prevented by firing two films together in a face-to-face condition. Success in producing whirler-coated films of CdS with moderate resistivity from cadmium acetate and thioacetamide was achieved by chlorine additions, however. Chlorine doping was accomplished by adding $CdCl_2$ dissolved in methanol to the cadmium

TABLE V. RELATIVE INTENSITIES OF DIFFRACTION PEAKS FOR CdS FILMS PREPARED FROM CADMIUM ACETATE-THIOACETAMIDE

Film	Method of Application	Sintering Temp, C	$\frac{I_{(h,k,-h+k,l)}}{I_{(1,0,\bar{1},1)}} \times 100$			Max Signal Height, percent full scale
			$10\bar{1}0$	0002	$10\bar{1}1$	
Standard random orientation	--	--	75	59	100	--
8-A(a)	Whirler coat	410	100	75	100	4
10-A(b, c)	"	410	33	0	100	12
13-A(b)	"	410	50	75	100	8
16-A(b)	"	$\frac{320(d)}{600}$	99	33	100	82
17-A(b, c)	"	$\frac{320(d)}{600}$	77	24	100	51

(a) S:Cd = 3:1.
(b) S:Cd = 1:1.
(c) $CdCl_2$ in methanol added to solution.
(d) Sintered at 410 C between coats; final sintering at 600 C.

acetate-thioacetamide-glacial acetic acid solution. After whirler coating onto Al_2O_3 substrates, samples were sintered face-to-face at 600 C for 5 minutes in air. The resulting films exhibited a sheet resistance of about 2×10^6 ohms/square, which corresponds to a film resistivity of 100 to 200 ohm-cm. This value is comparable to that reported for CdS films chemically sprayed onto glass[19] and ceramic[21] substrates. The chlorine concentration, as determined spectrographically, was quite high (2 atomic percent); this suggests that much of the chlorine is electrically inactive, perhaps existing as $CdCl_2$. The amount of chlorine reported in Reference (21) in chemically sprayed films of comparable resistivity was about 0.2 atomic percent, a value still orders of magnitude higher than the carrier concentration of 1.5×10^{17} cm^{-3} observed by the authors of that work.

Dielectric Layers

The materials' criteria established for dielectric layers in a previous work[1] may be summarized as follows:

(1) Ratio of dielectric constant (K) to thickness (t) > 10^5 cm^{-1}

(2) Breakdown voltage (E) > 10^5 volts/cm

(3) Resistivity (ρ) > 10^6 ohm-cm

(4) A density of traps associated with the semiconductor-dielectric interface low enough to permit modulation of source-drain conductance by the transverse electric field imposed by a reasonable gate potential

(5) Good adhesion of adjacent layers

(6) Uniform thickness

(7) Freedom from pinholes and voids

(8) Low reactivity with the ambient environment at operating temperatures

(9) Chemical and metallurgical compatibility of adjacent layers during processing

(10) Low chemical and metallurgical reactivity at interface at operating temperatures.

Of these ten criteria, six could be investigated by the fabrication of the simple parallel-plate capacitors described in an earlier section of this report.

$BaTiO_3$

At the time of initiation of the present work, little information was available regarding the characteristics and dielectric properties of $BaTiO_3$ paste EX 8289 (Du Pont) when used in conjunction with Du Pont 8115 gold electrodes. According to the manufacturer's literature, typical 25 C characteristics of thick-film capacitors employing ~1.7-mil-thick layers of EX 8289 dielectric in conjunction with Du Pont 8289 palladium-silver electrodes were: dielectric constant (K) of 1200 at 1 kHz, dissipation factor (D.F.) <3.5 percent at 1 kHz, and R (insulation) $>10^9$ ohms at 100 volts.

The same literature also suggested that 8115 gold electrodes should be acceptable, but that lower values of capacitance would result. The results of the present work confirm this statement. Table VI presents the results of measurements on Au-$BaTiO_3$-Au structure fired at 900, 975, and 1000 C, respectively, using the same firing cycle as that employed in the manufacturer's tests. The data in Table VI were obtained on a total of 26 capacitors, nine each on substrates fired at 950 and 1000 C and eight on substrates fired at 975 C.

TABLE VI. DIELECTRIC PROPERTIES OF $BaTiO_3$ THICK FILMS

Firing Temperature, C	10^2 Hz		10^3 Hz		10^4 Hz		10^5 Hz	
	K(a)	D.F.(b)	K	D.F.	K	D.F.	K	D.F.
950	796	0.00847	787	0.00898	769	0.0126	752	0.00927
975	870	0.00979	859	0.00961	835	0.0124	820	0.00935
1000	846	0.00820	835	0.00844	814	0.0113	801	0.00873

(a) K is the dielectric constant.
(b) D.F. is the dissipation factor.

Some general comments can be made regarding the data. First, the data are simple averages. In the case of capacitance measurements, this seems justified, the variation in measured capacitance at a given firing temperature being on the order of 10 percent. In the case of dissipation factors, the spread is much larger. For example, for the substrate fired at 950 C, the total spread in D. F. at 10^2 Hz was 0. 00460 to 0. 0161 for nine capacitors. Moreover, seven of the nine capacitors had D. F. values of less than about 0. 009. The two remaining values of 0. 0116 and 0. 0161 then disproportionately affect the averages appearing in the table. Nevertheless, the trends evidenced by the data in Table II are real. K decreases somewhat with increasing frequency and D. F. passes through a maximum between 10^3 and 10^5 Hz.

Even though the value of K is well below the value of 1100 predicted for the firing temperature of 1000 C, the ratio $K/t > 10^5$ even for thicknesses up to 80 μ, or about 3 mils. Thus, Criterion (1) is seen to be satisfied. The measured values of insulation resistance at 100 volts were typically around 10^8 ohms, about an order of magnitude below that specified for Pd-Ag electrodes. This value, however, is still considered adequate with respect to Criterion (3). Breakdown voltages were in the range 300 to 350 volts, which corresponds to a maximum breakdown field strength of about 9×10^4 volts/cm. Thus the suitability with respect to Criterion (2) is marginal. Uniformity in the thickness of the dielectric layers was also marginal. All of the dielectric patterns exhibited a shoulder or ridge around the periphery of the pattern. Typically the ridge was 0. 2 to 0. 4 mils thicker than the central portion of the pattern. In most cases, however, the ridge was sufficiently narrow that the central, electrode-bearing region of the dielectric layer was uniformly thick to within $\leq$0. 1 mil. The preceding applied to the average thickness as determined by smoothing out the Talysurf results. Random variations in layer thickness, which are more a measure of surface roughness, constitute at most another $\pm$0. 1 mil.

In general, pinholes and voids did not represent a problem in metal/insulator/metal (MIM) capacitors when the dielectric layers were thicker than about 1. 2 to 1. 5 mils. When the thickness approached 1 mil or less, however, the occurrence of shorted units increased.

Criterion (8) was not investigated in this program, but there is evidence from other sources that oxygen is chemisorbed on $BaTiO_3$, leading to the formation of a surface dipole layer. (22, 23)

The remaining criteria are all concerned either with the effects at the semiconductor-dielectric interface or the physical, chemical, and metallurgical compatibility of the semiconductor and dielectric layers. The

suitability of screen-printed $BaTiO_3$ with respect to these criteria was investigated on MIS capacitor structures employing wet chemically deposited PbS, and chemically sprayed and whirler-coated CdS as semiconductors. The results obtained on MIS structures were, for the most part, discouraging with regard to both the $BaTiO_3$-semiconductor interface and mutual compatibility. No capacitance-voltage characteristics indicative of conventional MIS behavior were observed for either PbS or CdS on $BaTiO_3$. In all cases, the data for MIS capacitors resembled those of MIM structures, the capacitance (C) and conductance (G) decreasing monotonically with increasing bias of either polarity. Consequently, no quantitative information regarding surface states could be obtained.

The compatibility problem arose in connection with the deposition of CdS by the spray technique. The use of aqueous spray solutions to deposit CdS onto substrates containing Au-$BaTiO_3$ metal-insulator patterns invariably resulted in either the complete destruction (flaking off or eroding) or serious degradation (became spongy) of the $BaTiO_3$ layer. These problems were not encountered with the methanol spray, however. The problem may be of a thermal nature. Because of the higher heat of vaporization of water, the cooling effect of the spray would be greater and the thermal shock correspondingly larger with aqueous solutions.

SiO_2

No satisfactory MIM capacitors employing Du Pont 8115 gold and SiO_2 were fabricated during this program. Whirler-coated SiO_2 films cracked and flaked off the fired gold electrodes during densification at all temperatures greater than about 200 C. It is felt that a primary reason for this is the relatively rough surface characteristics of the gold electrodes. Talysurf profiles of gold electrodes revealed narrow spikes extending 0.2 mil above and below the average (smoothed out) thickness profile. Moreover, as many as six of these spikes occurred over a 10-mil section. The tendency during whirler coating is to fill in the low spots first and subsequently build up in thickness until the entire surface is covered. It seems likely that in the process of achieving complete coverage, quite thick SiO_2 regions are formed, and the difference in coefficient of expansion between the gold and SiO_2 causes cracking and peeling at elevated temperature. Attempts to verify this hypothesis by whirler coating SiO_2 layers onto smoother electrodes evaporated onto polished silicon-wafer or Al_2O_3 substrates yielded results which were not conclusive. In the case of gold on silicon, the SiO_2 layers cracked during densification, but this may have been caused by a Au-Si interaction (alloying). In the case of gold on Al_2O_3, the evaporated gold films peeled off the substrate during densification of the SiO_2.

When SiO_2 was deposited by oxidation of silane, no cracking or peeling was observed. However, the SiO_2 layers contained either pinholes or voids, since all the resulting MIM capacitors were shorted, even for SiO_2 thicknesses of greater than 6000 A. These results may also be associated with surface roughness. Similar negative results have been reported for MIM structures employing vapor-deposited Al_2O_3 as the insulator[24], where it was found that even polished tantalum and gold-plated copper surfaces were too rough.

The failure to successfully produce an acceptable Au-SiO_2-Au capacitor precluded the possibility of fabricating either MIS or IGFET devices in the inverted configuration.

IGFET Structures

In spite of the fact that measurements on MIS capacitors indicated that field-effect modulation of source-drain conductance was unlikely, a limited number of complete IGFET structures were fabricated in order to obtain a further check on the compatibility of the materials and deposition techniques. The structures employed Du Pont 8115 gold electrode and EX 8229 $BaTiO_3$ dielectric compositions. As anticipated, no useful field-effect modulation was observed. However, some observations relevant to the question of compatibility of materials and techniques were obtained as follows:

(1) The ease with which complete coverage of the various layers by the semiconductor was obtained decreased in the order Al_2O_3 - $BaTiO_3$ - Au, the same order in which surface roughness increased.

(2) Immediately after completion of an inverted IGFET structure, gate isolation was poor. In many cases, when CdS was used as the semiconductor, gate isolation could be improved by a prolonged bake at 100 C. In such cases, the poor isolation was probably caused by absorption of water during the etch and rinse steps used to form the semiconductor pattern. When PbS was used as the semiconductor, however, gate leakage remained high even after baking. Eight PbS IGFET structures were fabricated, and in all eight devices the gate insulation resistance was on the same order as the source-drain resistance. Apparently, the $BaTiO_3$ layers were sufficiently porous that PbS deposits formed conducting channels through the dielectrics.

TABLE VII. EMISSION SPECTROGRAPHIC ANALYSIS OF THICK-FILM PASTES

Element	Weight Percent of Element Present[a]		
	Au 8115	$BaTiO_3$ DP 8229	$BaTiO_3$ EX 8289
Au	Major	N(<. 1)	N(<. 1)
Ba	N(<. 01)	HIGH	HIGH
Ti	N(<. 01)	HIGH	HIGH
Fe	. 01)	. 01	1. -3.
B	. 3	. 05	. 05
Si	. 3	. 2	. 2
Mg	N(<. 005)	. 01	. 01
Pb	2. -5.	. 5	. 3
Bi	N(<. 01)	1. -3.	2. -5.
Al	. 01	. 2	. 2
Cu	. 01	. 01	. 01
Ag	. 01	N(<. 005)	N(<. 005)
Zr	N(<. 01)	N(<. 01)	. 5
Ca	N(<. 01)	. 07	. 07

(a) N means element not detected; the detection limit for the element is given in parentheses.

(3) The source-drain resistance of whirler-coated and CdS layers sintered at 600 C for 5 minutes was several orders of magnitude higher than the resistance of a CdS layer of comparable geometry on Al_2O_3. This observation indicates either that the nature of the $BaTiO_3$-CdS interface is such that the source-drain channel is completely pinched off even at applied gate voltages as high as 60 volts, or that severe degradation of the semiconducting properties of CdS occurred via contamination from the $BaTiO_3$ during sintering. Identical results were obtained with a different composition $BaTiO_3$ paste, Du Pont DP 8229, and with evaporated aluminum rather than fired gold electrodes. Thus, if contamination is a problem, the origin of the contaminant is in the dielectric compositions rather than the electrode. Spectrographic analyses of both EX 8289 and DP 8229 dielectric composition and of 8115 conductive gold appear in Table VII. It may be observed that with the exception, of course, of barium and titanium, all major CdS dopants common to both dielectric compositions are also common to the gold paste. Thus, there is nothing in these analyses that unambiguously identifies the possible contaminant.

There are other possible explanations for the observed high-resistance CdS films on $BaTiO_3$. One explanation is that owing to the surface character of printed and fired $BaTiO_3$, the CdS film in the vicinity of the $BaTiO_3$ interface is highly disordered, containing a large number of trapping centers and interface states.

Another possibility is the effect of the space-charge layer known to exist on ferroelectric $BaTiO_3$[25] and the likelihood of chemisorbed oxygen on both the $BaTiO_2$[22, 23] and CdS layers[21]. These are merely possibilities. The exact cause of the observed effects and the true nature of the $BaTiO_3$-CdS interface are presently unknown.

CONCLUSIONS AND RECOMMENDATIONS

The experimental results obtained during this investigation lead to the following conclusions and recommendations regarding the feasibility and approach for producing IGFET's by processing techniques compatible with thick-film technology.

(1) Wet chemically deposited PbS is not a promising candidate material for the semiconducting layer. The production of unsensitized PbS layers would require investigation of alternative reagent schemes in order to preclude chemical sensitization via oxygen contamination during deposition. Even if this were accomplished, the reactivity of PbS surfaces with ambient oxygen would in time probably result in sensitization leading to reduced carrier mobilities, barrier-limited conductivity, and inadequate control of carrier concentration and conductivity type. Thus, production of devices with reproducible and predictable properties is unlikely with wet chemically deposited PbS.

(2) CdS films prepared by spraying or fogging $CdCl_2$-$CS(NH_2)_2$ solutions and by whirler coating $Cd(OAc)_2$-$2H_2O$-TA solutions require further investigation. The electrical properties of CdS on Al_2O_3 obtained in the present work are discouraging in that no Hall measurement could be obtained. On the other hand, Heime[20] obtained effective mobilities as high as 100 cm^2/volt-sec in TFT's fabricated with chemically sprayed CdS and SiO_2 dielectrics even though no Hall mobility could be measured in the films prior to deposition of the SiO_2. A more comprehensive investigation of chemically deposited CdS is required in order to optimize deposition conditions and impurity additions before the feasibility of using this particular semiconductor can be unambiguouly established.

(3) Thick-film $BaTiO_3$ does not appear to be an acceptable dielectric for use as a gate insulator in the FET structure with chemically deposited PdS or CdS. Although the dielectric constant, bulk resistivity, and breakdown field are considered to be adequate, serious problems exist in the areas of adhesion, compatibility with adjacent layers, porosity, surface roughness, and reactivity with the environment. In addition, the nature of the $BaTiO_3$ surface and of the $BaTiO_3$-semiconductor interface is unknown. The fact that field-effect modulation has been achieved with ceramic $BaTiO_3$[2] (staggered structure on dielectric substrates) and with single crystals[25] implies that a fundamental difference exists between these forms of $BaTiO_3$ and the thick-film variety achieved by screen printing. It thus appears that the entire thick-film technology could benefit from a fundamental investigation of the physical, chemical, and electronic properties of thick-film $BaTiO_3$ layers.

(4) Low-temperature deposition of SiO_2 by oxidation of SiH_4 also requires further investigation. A key issue is whether the inability to fabricate satisfactory MIM structures with SiO_2 results from the inherent surface roughness of thick-film gold electrodes. If this is the case, the implication is that the present thick-film state of the art is not adequate. In fact, surface roughness may well be a limiting factor even if complete coverage of the electrode by SiO_2 can be achieved. Thin SiO_2 layers ($\leq$ 4000 A) would be required to achieve the desired value of $\frac{K}{t}$, and would replicate the electrode surface. Thus, random variations of surface roughness an order of magnitude greater than the insulator thickness would provide ample opportunity for exceedingly nonuniform fields. In addition, the effective channel length could be appreciably larger than the source-drain spacing. Finally, the occurrence of spikes in the thickness profile could have serious effects on the properties of the semiconducting layer since the degree of lattice disorder and hence defect density could be influenced by the roughness of the insulator-semiconductor interface.

As a consequence of Conclusions (1) through (4) above, it is recommended that work in the area of thick-film-compatible IGFET's emphasize those combinations of materials which have already proven themselves in other FET technologies, that is, the $CdS:SiO_2$ system. Thus far, many of the efforts in the area of thick-film active devices have involved a shotgun approach involving cursory investigation of a wide variety of dielectrics and a relatively smaller variety of semiconductors. The time may have come to settle on that system affording the best chance for success and exploit it. As of now, the $CdS:SiO_2$ system is the logical candidate.

It is also recommended, however, that the capabilities and shortcomings of thick-film technology be critically reviewed with respect to such qualities as surface roughness, paste composition, chemical reactivity of fluxes, etc., in an effort to determine whether there are inherent limitations which preclude the successful production of FET's with conventional thick-film electrodes.

REFERENCES

(1) Duncan, F. W., Chang, Y. F., and Gorton, H. C., "A Survey of Semiconductor Materials and Processes for Thick-Film Field-Effect Transistor Fabrication", Final Report, NAS 1-8077 (October, 1968).

(2) Sihvonen, Y. T., Parker, S. G., and Boyd, D. R., "Printable Insulated-Gate Field-Effect Transistors", J. Electrochem. Soc., 114, 96 (1967).

(3) Laznovsky, W., "Thick Film Active Devices", Final Report, NAS 1-7340 (June, 1968).

(4) Goldsmith, N., and Kern, W., "The Deposition of Vitreous Silicon Dioxide Films from Silane", RCA Review, 28, 153 (1967).

(5) Kicinski, F., "Preparation of Photoconductive Cells by Chemical Deposition of PbS", Chemistry and Industry, 17, 54 (1948).

(6) Chamberlin, R. R., and Skarman, J. S., "Chemical Spray Deposition Process for Inorganic Films", J. Electrochem. Soc., 113, 86 (1966).

(7) Van der Pauw, L. J., "A Method of Measuring the Resistivity and Hall Coefficient on Lamellae of Arbitrary Shape", Philips Tech. Rev., 20, 220 (1959).

(8) Feldner, E., Görlich, P., Krohs, A., and Wagner, G., "Some Aspects of the Influence of Temperature on the Photoconductive Properties of PbS Layers", Infrared Physics, 8, 161 (1968).

(9) Simić, V. M., and Marinković, $\overline{Z}$. R., "Influence of Impurities on Photosensitivity of Chemically Deposited Lead Sulphide Layers", Infrared Physics, 8, 189 (1968).

(10) Bykova, T. T., "Photoconductivity and Surface Photo-EMF of Epitaxial Films of Lead Sulfide", Soviet Physics-Solid State, 8, 759 (1966).

(11) Giroux, G., "Consistent Model for Lead Sulfide Photodetectors, I. Experimental Results", Can. J. Phys., 41, 1840 (1963); "II. New Model", ibid., p 1856.

(12) Zemel, J. N., and Varela, J. O., "Surface Properties of PbS Photoconductors", J. Phys. Chem. Solids, 14, 142 (1960).

(13) Snowden, D. P., and Portis, A. M., "Electrical Structure of PbS Films", Phys. Rev., 120, 1983 (1960).

(14) Lummis, F. L., and Petritz, R. L., "Noise, Time-Constant, and Hall Studies on Lead Sulfide Photoconductive Films", Phys. Rev., 105, 502 (1957).

(15) Petritz, R. L., "Theory of Photoconductivity in Semiconductor Films", Phys. Rev., 104, 1508 (1956).

(16) Moss, T. S., "Lead Salt Photoconductors", Proc. IRE, 43, 1869 (1955).

(17) Hillenbrand, L. J., "The Adsorption and Incorporation of Oxygen by Lead Sulfide at Room Temperature", J. Physical Chemistry, 73, 2902 (1969).

(18) Daveydov, M. S., and Mordvintsev, Yu. F., "Determination of Microimpurities in Photosensitive Layers of Lead Sulfide with the Aid of an Optical-Acoustic Gas Analyzer", J. Appl. Chem. USSR, 41, 2491 (1968).

(19) Heime, K., "Chemically Sprayed CdS Thin Film Transistors", S. S. Electronics, 10, 732 (1967).

(20) Heime, K., "Die Verwendbarkeit Aufgedampfter und Aufgespriihter CdS-und CdSe-Schichten Für Dünnschichttransistoren", Z. Angew. Phys., 24, 160 (1968).

(21) Micheletti, F. B., and Mark, P., "Effects of Chemisorbed Oxygen on the Electrical Properties of Chemically Sprayed CdS Thin Films", Applied Physics Letters, 10, 136 (1967).

(22) Thomas, R. T., Tredgold, R. H., and Williams, R. H., "The Influence of Gaseous Adsorption on the Metal-$BaTiO_3$ Contact", J. Phys. C. (Proc. Phys. Soc.) 1, 1370 (1968).

(23) Holt, J., "Surface Space Charge Layers on Semiconducting Barium Titanate", S. S. Electronics, 9, 813 (1966).

(24) Richman, D., Duffy, M. T., Carnes, J. E., Fanzucchi, P. J., "Improved Dielectric Films for Semiconductor Application", Quarterly Technical Report No. 1, Contract N00019-70-C-0129 (Feb., 1970).

(25) Buchman, P., "The Surface Properties of Barium Titanate", Solid-State Electronics, 11, 767 (1968).

NEW TECHNOLOGY APPENDIX

After a diligent review of the work performed under this contract, it is concluded that no innovation, discovery, improvement, or invention was made.

RDB/jvd

DISTRIBUTION LIST

No. Copies	
	NASA Langley Research Center Hampton, Virginia 23365
1	Attention: Research Program Records Unit, Mail Stop 122
1	Raymond L. Zavasky, Mail Stop 117
25	Robert L. Stermer, Mail Stop 470
	NASA Ames Research Center Moffett Field, California 94035
1	Attention: Library, Mail Stop 202-3
2	Thomas B. Fryer, Mail Stop 213-4
	NASA Flight Research Center P.O. Box 273 Edwards, California 93523
1	Attention: Library
2	Donald W. Veatch, Org. D
	Jet Propulsion Laboratory 4800 Oak Grove Drive Pasadena, California 91103
1	Attention: Library, Mail 111-113
	NASA Manned Spacecraft Center 2101 Webster Seabrook Road Houston, Texas 77058
1	Attention: Library, Code BM6
1	Saverio Gaudiano, Code EE2
	NASA Marshall Space Flight Center Huntsville, Alabama 35812
1	Attention: Library
1	Dorrence L. Anderson, S&E-ASTR-RM
1	Dr. Alvis M. Holladay, S&E-ASTR-RS
	NASA Wallops Station Wallops Island, Virginia 23337
1	Attention: Library
	NASA Lewis Research Center 21000 Brookpark Road Cleveland, Ohio 44135
1	Attention: Library, Mail Stop 60-3
2	John C. Sturman, Mail Stop 77-1

No. Copies	
	NASA Goddard Space Flight Center Greenbelt, Maryland 20771
1	Attention: Library
1	David H. Schaefer, Code 711
	NASA John F. Kennedy Space Center Kennedy Space Center, Florida 32899
1	Attention: Library, Code IS-CAS-42B
	National Aeronautics and Space Administration Washington, D. C. 20546
1	Attention: Library, Code USS-10
3	Theofolus P. Tsacoumis, Code REE
3	James R. Miles, Code REE
	General Electric Corporation Missile and Space Division P.O. Box 8555 Philadelphia, Pennsylvania 19101
1	Attention: A. Kanter, Room U4607 SPC
	Picatinny Arsenal Dover, New Jersey 07801
1	Attention: Dr. Gilbert L. Hand
	McDonnell Douglas Corporation Missile and Space Systems Division 3000 Ocean Park Boulevard Santa Monica, California 90406
1	Attention: A. Kondounarir, Unit 11
	The Bendix Corporation Bendix Semiconductor Division Holmdel, New Jersey 07733
1	Attention: G. E. Yurouski
	Commanding General U. S. Army Electronics Command Fort Monmouth, New Jersey 07703
1	Attention: AMSEL-RD-MT
	Department of Defense Advisory Group on Electron Decices 201 Varick Street, 9th Floor New York, New York 10014
5	Attention: D. Klieger
	NASA Scientific and Technical Information Facility
12+ repro.	P.O. Box 33 College Park, Maryland 20740