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A STUDY OF DYNAMIC LOAD SIMULATORS FOR ELECTRICAL SYSTEMS TEST FACILITY

FINAL REPORT

Program Period:

29 December 1969 to 30 June 1970

Prepared for

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
MANNED SPACECRAFT CENTER
HOUSTON, TEXAS, 77058

Contract Number NAS-9-10429

AVSD-0364-70-RR

17 August 1970

Prepared by

AVCO GOVERNMENT PRODUCTS GROUP
Systems Division
201 Lowell Street
Wilmington, Massachusetts, 01887

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Dynamic Load Simulator Study

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1. INTRODUCTION

This document is the final report of the Dynamic Load Simulator Study. This was a six-month study (29 December 1969 through 30 June 1970) conducted by Avco Corporation's Systems Division for the National Aeronautics and Space Administration under Contract NAS-9-10429. The basic objective of the study was the identification and investigation of various methods of characterizing and simulating the dynamic and steady-state electrical load responses of manned spacecraft equipment.

1.1 BACKGROUND

Both design and development of electrical power distribution and conditioning systems are highly dependent on the characteristics of the power sources and the various loads. The inter-relationships between these elements are particularly significant in the case of the complex systems of manned spacecraft. The need to maintain tight schedules in the Mercury, Gemini, and Apollo manned spacecraft programs made mandatory the use of load simulators in evaluating system performance. At best, however, such devices simulated only steady-state load conditions. Subsequent vehicle testing and flight experience has disclosed operational problems caused by transient (or dynamic) load characteristics being reflected into the system.

The dynamic load simulator study was undertaken to identify and investigage: (1) methods of interrogating electrical hardware to establish significant characteristics, and (2) methods of simulating both the dynamic and steady-state response of that hardware.

In the proposed concept the individual loads to be simulated will first be interrogated electrically (electronically) to identify quantitatively the parameters necessary to establish the load response to the power input. This data will then be processed to yield the information required to program the simulator to respond to the power input in a like manner. In practice, the interrogation/simulation process is characterized by the following sequence of events. Figure 1-1 shows the sequence in flow diagram form.

1. The load to be simulated is identified.

2. The load category and stimulation data are determined.

3. An interrogation method designed to yield the device response for all modes of operation is selected.

4. The load is interrogated.

5. The interrogation data is processed to identify the impedance-time history of the load for each mode of operation.

6. A simulator capable of being programmed to provide this variable impedance is selected.

7. A simulator program is generated.

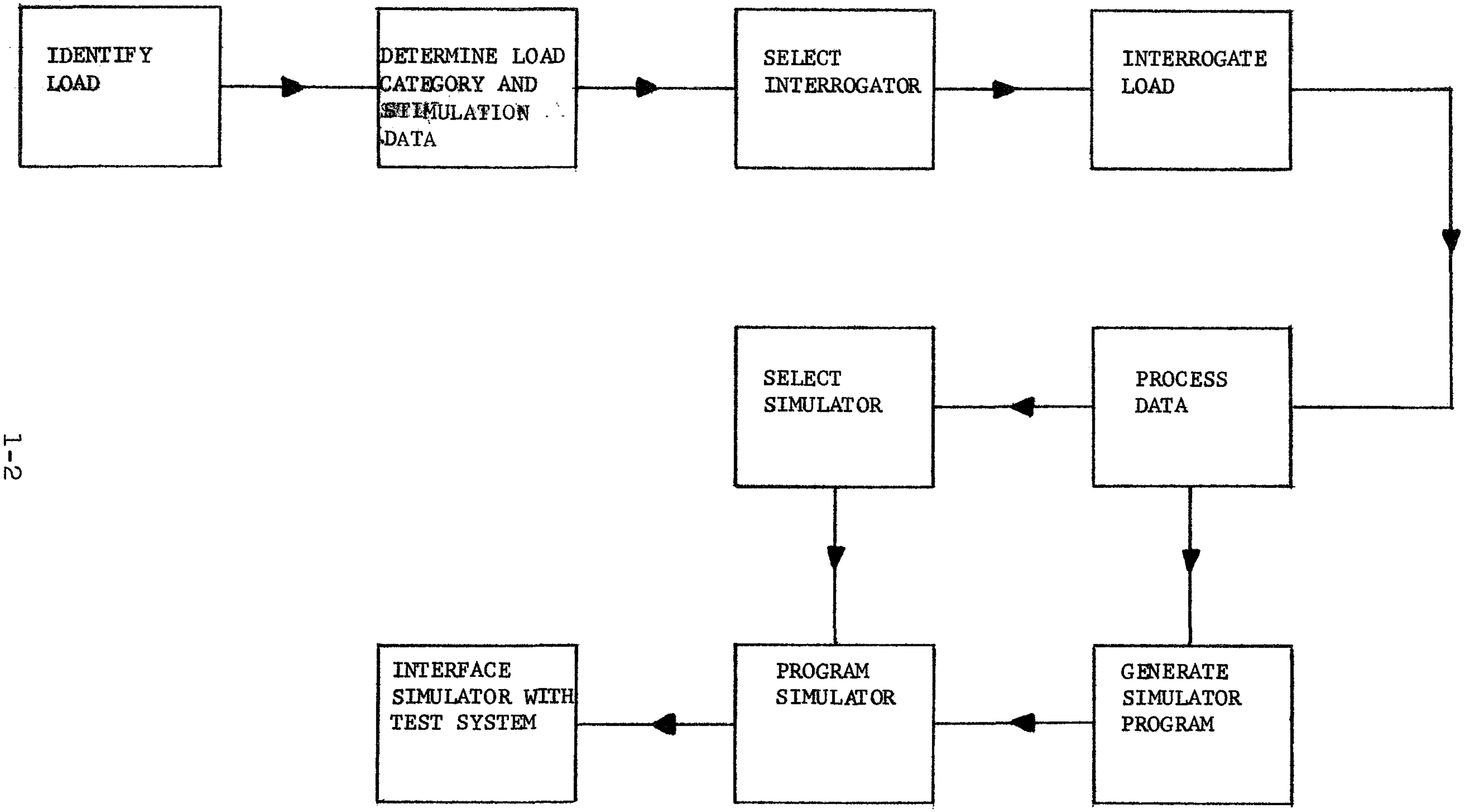


Figure 1-1   INTERROGATION/SIMULATION PROCESS FLOW DIAGRAM

8. The simulator program is entered into the simulator.

9. The simulator is connected to the power control and distribution system under test.

The interrogation and simulation techniques identified during this study can be implemented in appropriate hardware for use in testing the power conditioning and distribution systems of future manned spacecraft.

The use of such techniques and equipment is not limited, however, to this application. The availability of a load simulator capable of reproducing a specific dynamic response when stimulated by a power source would be of significant value during the development phase of any electrical hardware program. Such simulators would:

1. Permit load parameter changes to be introduced and evaluated.

2. Provide more convenient and readily available data points for system monitoring purposes.

3. Permit the assembly of a test configuration without tying up expensive and often unavailable equipment.

1.2 OBJECTIVES

The dynamic load simulator study was concentrated on the following general and specific objectives.

GENERAL

To identify and investigate various methods for characterizing and simulating the dynamic and steady-state electrical loads of manned spacecraft equipment.

SPECIFIC

- To investigate typical spacecraft equipment to identify and characterize the parameters significant to their electrical loading of power sources.

- To establish a set of requirements for an interrogator and an electrical load simulator.

- To identify techniques and concepts that may be useful in satisfying the interrogator and simulator requirements.

- To investigate these techniques and conduct a trade-off study to define and describe the more promising approaches.

- To recommend a preliminary design based on the results of the trade-off study, and present a program plan for implementing the design.

1.3 DEFINITIONS

The terms interrogation and simulation are used extensively throughout this report. A definition of these terms follows.

1.3.1 Interrogation

Interrogation is the quantitative determination of those parameters of a device that describe its dynamic and steady-state electrical response on the power lines to a specified application of voltage. In its broad sense the term includes the acquisition of this data and its processing to yield information in a formal suitable for programming a simulator to duplicate the load response.

1.3.2 Simulation

Simulation is the duplication on the power lines of the dynamic and steady-state response of an electrical load.

1.4 REPORT ORGANIZATION

The final report is organized as follows.

1. INTRODUCTION

   Provides background information, states the study objectives, defines key terms, indicates the way the report is organized, and lists pertinent contractual publications.

2. CONCLUSIONS AND RECOMMENDATIONS

   Presents conclusions drawn from the study and recommendations for future action.

3. STUDY APPROACH

   Summarizes the step-by-step approach adopted in carrying out the dynamic load simulator study.

4. AREAS OF INVESTIGATION

   Describes each of the major areas investigated.

5. INTERROGATION AND SIMULATION SYSTEM CONCEPT

   Discusses an over-all system concept, covering both the interrogation and simulation processes, and describes equipment requirements, implementation aspects, and trade-offs.

6. FEASIBILITY ASSESSMENT

   Indicates the feasibility of the system concept, in particular the feasibility of the two key elements of the system--network models and variable resistance devices.

7. RECOMMENDATIONS

   Recommends the next step to be taken in the system's evolution.

8. BIBLIOGRAPHY

Lists significant publications pertinent to the study.

1.5 PUBLICATIONS

Avco Systems Division documents published under this study contract are listed below. All are monthly progress reports. For summaries of these documents, see Appendix A.

1. A Study of Dynamic Load Simulators for Electrical Systems Test Facility, First Monthly Progress Report, for the Period 19 December 1969 to 31 January 1970; Avco Systems Division, AVSD-0065-70-CR, 5 February 1970.
2. A Study of Dynamic Load Simulators for Electrical Systems Test Facility, Second Monthly Progress Report, for the Period 1 February 1970 to 28 February 1970; Avco Systems Division, AVSD-0108-70-CR, 6 March 1970.
3. A Study of Dynamic Load Simulators for Electrical Systems Test Facility, Third Monthly Progress Report, for the Period 1 March 1970 to 31 March 1970; Avco Systems Division, AVSD-0157-70-CR, 6 April 1970.
4. A Study of Dynamic Load Simulators for Electrical Systems Test Facility, Fourth Monthly Progress Report, for the Period 1 April 1970 to 30 April 1970; Avco Systems Division, AVSD-0216-70-CR, 6 May 1970.
5. A Study of Dynamic Load Simulators for Electrical Systems Test Facility, Fifth Monthly Progress Report, for the Period 1 May 1970 to 31 May 1970; Avco Systems Division, AVSD-0259-70-CR, 12 June 1970.

2. CONCLUSIONS AND RECOMMENDATIONS

2.1 CONCLUSIONS

- The concept of electrically (electronically) interrogating and simulating the steady-state and dynamic response of manned spacecraft electrical loads is feasible.
- A process capable of performing the required interrogation and simulating functions has been described.
- The hardware required for implementing this interrogation/simulation process has been identified.
- The effectiveness of the more critical interrogation and simulation elements of the system has been demonstrated successfully in laboratory experiments.

2.2 RECOMMENDATIONS

It is recommended that a six-step program designed to demonstrate the practicality and efficiency of the system proposed in this report be initiated as a minimum-cost next step in the evolution of a dynamic load simulator system. The program is described in Paragraph 7 of the report.

3. STUDY APPROACH

3.1 GENERAL APPROACH

The dynamic load simulator study was conducted according to the approach summarized below and shown in logical flow diagram form in Figure 3-1. This approach is basically one of thoroughly analyzing requirements and subsequent synthesis of a system capable of satisfying those requirements.

<u>Step 1</u> - Identify electrical loads by class.
<u>Step 2</u> - Establish load parameters and load parameter ranges for each class of loads.
<u>Step 3</u> - Establish interrogation and simulation requirements.
<u>Step 4</u> - Identify potential interrogation and simulation techniques.
<u>Step 5</u> - Investigate the potential interrogation and simulation techniques and make appropriate trade-offs.
<u>Step 6</u> - Establish interface requirements.
<u>Step 7</u> - Select suitable interrogation and simulation design approaches.
<u>Step 8</u> - Define a feasible system concept.

3.2 IDENTIFICATION OF ELECTRICAL LOADS

Basic to establishing interrogator and simulator requirements is knowledge of the spacecraft electrical loads to be simulated. That is, the types of loads and their significant electrical parameters must be identified and a quantitative assessment made so that the extremes over which the interrogation and simulation process must operate can be established.

The electrical loads to be simulated are those system elements that ultimately use the energy. Figure 3-2 is a simplified block diagram of a power conditioning and distribution system. This study was concerned with the interrogation and simulation of the electrical loads at the interface with the distribution network, as shown in Figure 3-2.

A list of electrical loads peculiar to manned spacecraft was established early in the program. These loads are listed in Table 3-1. At that time, too, significant parameters to be used in characterizing the load response were also identified. These are listed in Table 3-2.

The load classifications identified in Table 3-1 were then divided into sub-classes to group together those load elements whose load characteristics were similar. Table 3-3 summarizes these loads along with estimates of significant parameters. The loads and parameters listed on that table represent: (1) the principal means for defining the scope of the dynamic load simulator study, and (2) the basis for defining a set of requirements for the interrogator and for the load simulator. These estimates are the result of engineering judgements based on examination and study of NASA-supplied data and identify the range through which the input parameters of the electrical loads of future manned spacecraft may be expected to vary. Table 3-3 covers two major sets of characteristics, as follows:

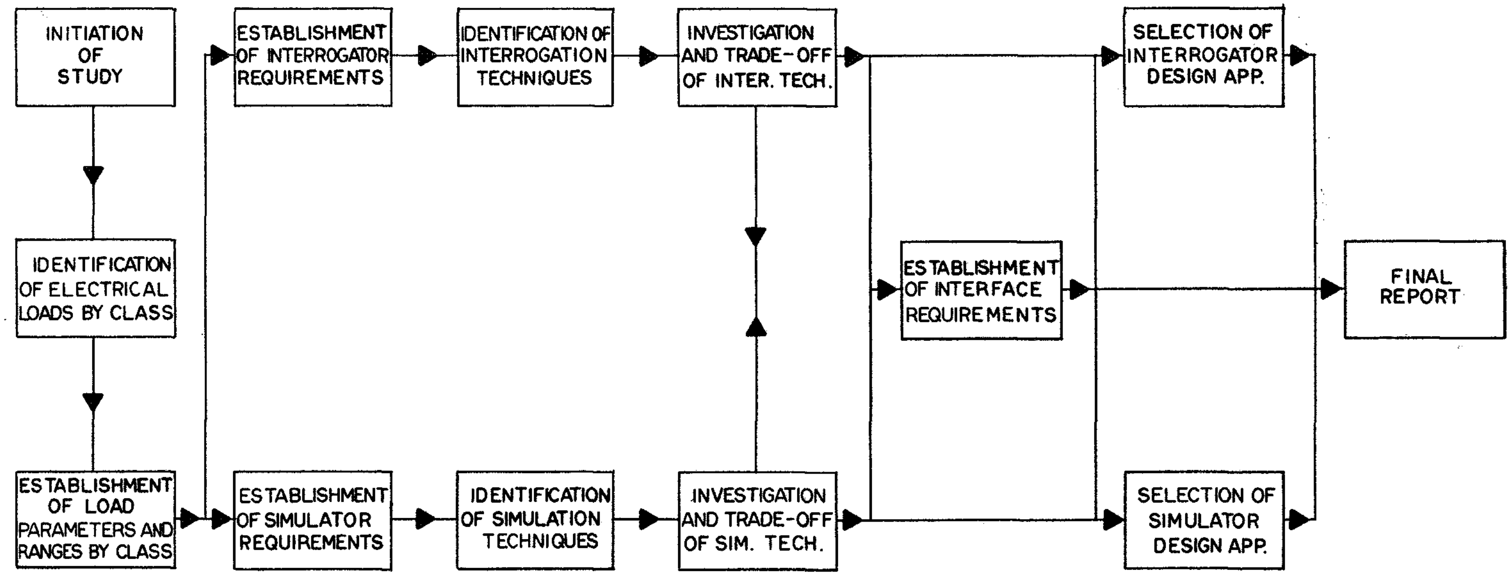


FIGURE 3-1 TECHNICAL APPROACH TO DYNAMIC ELECTRICAL LOAD STUDY--LOGICAL FLOW DIAGRAM

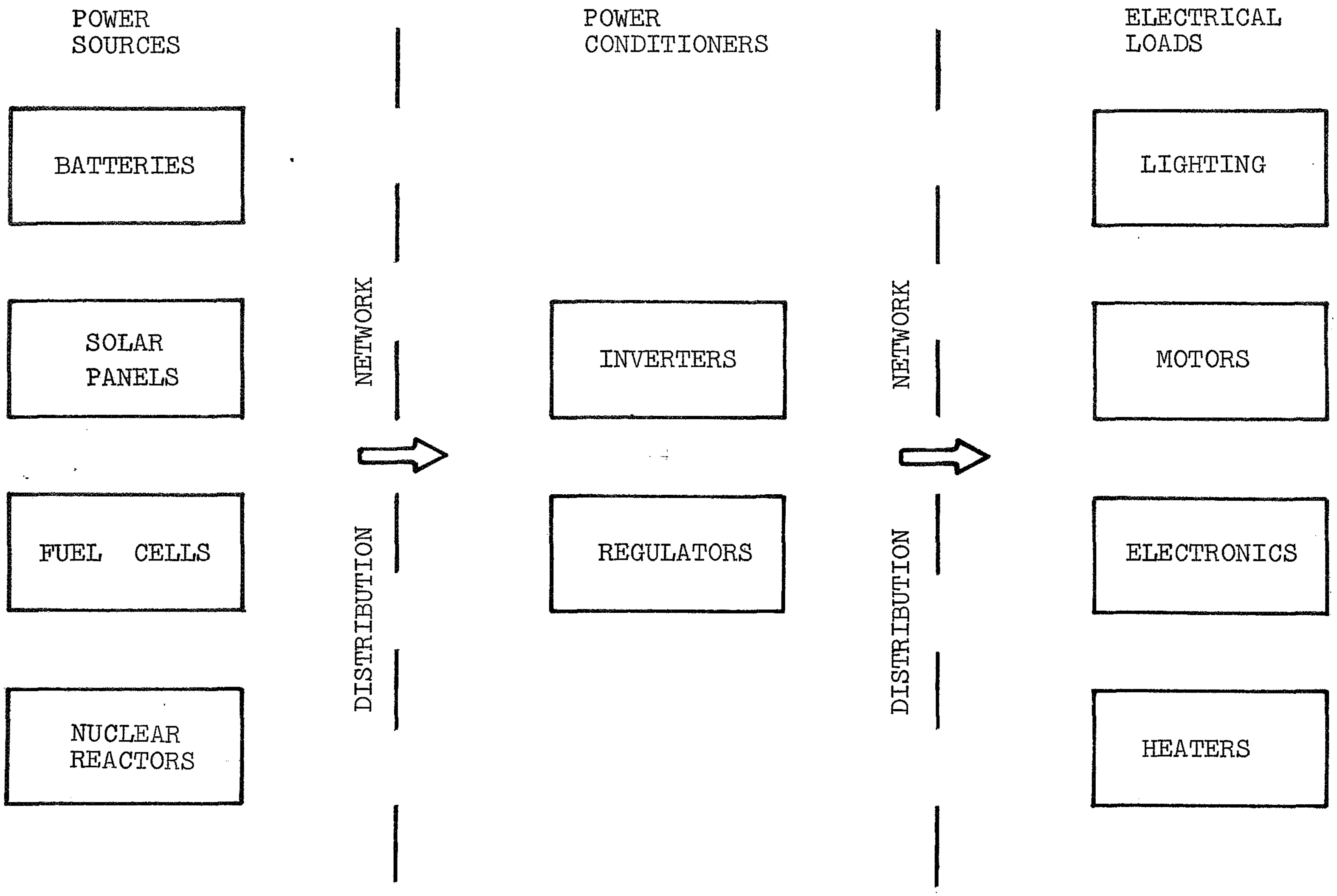


FIGURE 3-2
SIMPLIFIED DIAGRAM OF POWER CONDITIONING AND DISTRIBUTION SYSTEM

TABLE 3-1 SPACECRAFT ELECTRICAL LOAD CLASSIFICATION

1. Motors
2. Electronics
3. Heaters
4. Lighting
5. Solenoids and Relays
6. Pyrotechnics
7. Computers
8. Transducers and Servos
9. Electrolysis

TABLE 3-2 SIGNIFICANT LOAD PARAMETERS

1. Input Voltage
2. Input Current
3. Input Power
4. Input (Source) Frequency
5. Load Power Factor
6. Load Transient Amplitude
7. Load Transient Duration
8. Load Transient Frequency

TABLE 3-3 LOAD CLASSIFICATION AND INPUT PARAMETER RANGE ESTIMATES

LOAD CLASSIFICATION AND INPUT PARAMETER RANGE ESTIMATES															
	STEADY STATE CHARACTERISTICS					DYNAMIC CHARACTERISTICS									
CATEGORY	VOLTS	POWER	CURRENT	PWR	SOURCE	TURN-ON TRANSIENTS			TURN-OFF TRANSIENTS			OPERATING REMARKS			
	V	W	A	FACTOR	FREQUENCY	AMPL.	DUR	FREQ	AMPL	DUR	FREQ	RPM	TORQUE		
I MOTORS 1. D-C MOTORS A SPECIAL	6-35	3-100	.05-1.5	DC	DC	15A	1 SEC	1PLSE	1.5A	1SEC	1PLSE	7200	2 FT-lbs		APPLIED CURRENT CONSTANT AT RATED LOADS
B ≤1 HP	10-200	80-3500	1.5-15	DC	DC	120A	5SEC	1PLSE	15A	3SEC	1PLSE	7200	60FT-lbs		APPLIED CURRENT INCREASES WITH HORSEPOWER
C 1≤HP≤2	75-200	750-6000	10-50	DC	DC	500A	5 SEC	1PLSE	50A	5 SEC	1PLSE	3600	300FT-lbs		
2 A-C MOTORS A. SPECIAL	6-220	2-100	.05-2.0	.5	400Hz-1,3Φ	20A	1SEC	400Hz	2A	1SEC	400Hz	24,000	2 FT-lbs		APPLIED CURRENT CONSTANT AT RATED LOADS
B ≤1 HP	26 220	80-2000	1.5-10	.5	400HZ-1,3Φ	100A	5SEC	400Hz	10A	3 SEC	400Hz	8.000	60FT-lbs		APPLIED CURRENT INCREASE AT PEAK LOADS
C 1≤HP≤2	115-220	800-3500	4-20	.5	400Hz-3Φ	200A	5SEC	400Hz	20A	5 SEC	400Hz	3600	300 FT-lbs		
												PULSE	PULSE WIDTH	PULSE FREQ	
II ELECTRONICS 1. CONTROLLERS A SOLID STATE	20-35	10-70	0.5-2.0	DC	DC	3A	35MS	1PLSE	50V	100µS	1MHz	15A	50MS	10PPS	.02V-1KHz RIPPLE ON RETURN
B MAG CORE	20-35	20-140	1.0-4.0	DC	DC	40V	10µS	1PLSE	200V	10µS	1MHz	15A	50MS	10PPS	
C ELECTRO-MECH	20-40	20-300	1.0-8	DC	DC	20A	5MS	1PLSE	50V	5MS	10 KHz	15A	50MS	10PPS	ARCING WHEN SWITCHING
												KEYED POWER	FREQU.	DURATION	
2 COMMUNICATIONS A. TRANSMITTER a) SOLID STATE DC	20-40	2-10	.005-.5	DC	DC	60V	1MS	40KHz	60V	1MS	10MHz	50 W	CW	AS REQ	
b) SOLID STATE AC	24-115	1-5		.5	400Hz 3Φ	130V	1MS	40KHz	130V	1MS	10MHz	20W	CW	AS REQ	
c) VAC. TUBE	20-130	10-50		DC	DC	150V	1MS	40KHz	150V	1MS	10MHz	150W	CW	AS REQ	
B RECEIVER	12-35	1-5		DC	DC	50V	1MS	40KHz	50V	1MS	10MHz	10W	CW	AS REQ	
C. MODULATOR a) DC	6-35	1-3		DC	DC	50V	1MS	40KHz	50V	1MS	100MHz	5W	DIGITAL	1MIN.	
b) AC	24-115	0.5-5		.5	400Hz-1,3Φ	130V	1MS	40KHz	130V	1MS	100MHz	10 W	DIGITAL	1MIN.	
D AMPLIFIER a) DC	20-35	1-10		DC	DC	40A	1 SEC	2Hz	50V	1MS	10MHz	200W	CW	CW	
b) AC	115-220	15-25		.5	400Hz-1,3Φ	5A	5MS	100KHz	250V	1MS	10MHz	200W	CW	CW	
3 INSTRUMENTATION A TRANSDUCER	5-35	.01-3.0	.01-.10	DC	DC	50V	5MS	DC	50V	1MS	1MHz	VOLTAGE VARIES LINEARLY WITH AMBIENT CONDITIONS			
B GYROSCOPE	24-130	2-100	.05-1.5	.5	400-3Φ	4A	1MIN	1PLSE	200V	2MS	500Hz	CURRENT VARIES WITH TORQUE			
C ELECTRO-OPTICS	100-200	5-100		.5	800-2Φ	2A	1MIN	1PLSE	200V	2MS	1KHz				

TABLE 3-3 (Concl'd.) LOAD CLASSIFICATION AND INPUT PARAMETER RANGE ESTIMATES

LOAD CLASSIFICATION AND INPUT PARAMETER RANGE ESTIMATES

CATEGORY	STEADY STATE CHARACTERISTICS					DYNAMIC CHARACTERISTICS						
	VOLTS	POWER	CURRENT	PWR	SOURCE	TURN-ON TRANSIENTS			TURN-OFF TRANSIENTS			OPERATING REMARKS
	V	W	A	FACTOR	FREQUENCY	AMPL	DUR	FREQ	AMPL	DUR	FREQ	
III HEATERS												
A THERMOSTAT	6-40	20-250	.5-6.0	DC	DC	50V	3MS	10KHz	400V	3MS	300Hz	
B PROPORTIONAL	20-40	20-400	.5-10.	DC	DC	50V	1MS	1KHz	–	–		
IV LIGHTING												
A. ELECTROLUMIN.	100-120	.03-2		.5	400-1Φ							.2W BASED ON 60 in^2 OF LIGHTING SURFACE
B INCANDESCENT												
a) DC	1.2-55	0.1-100	.01-4	DC	DC	1 10A	100MS	30KHz	200V	1MS	1KHz	
b) AC	24-200	20-100	.1-2.0	.5	400-1/3Φ	.10A	100MS	30KHz	400V	1MS	1KHz	
C FLASHERS	20-200			DC	DC	250A	20MS	55PPS				250A PULSES FOR 20MS AT 55PPS
D. FLUORESCENT	100-200	2-40	.05-.5	.5	400-1Φ	2A	100MS	30KHZ	–	–	–	
V SOLENOID & RELAY												
A DC	6-120	.5-5	.01-20	DC	DC	140V	5MS	200Hz	1200V	5MS	1KHz	
B AC	6-230	.5-15	.01-5	.5	400-1Φ	250V	5MS	200Hz	2300V	5MS	1KHz	
VI PYROTECHNICS	ONE-SHOT DEVICES											
A INITIATORS						7A	10MS	100HZ	20-0A	250MS	DC	1 AMP-1 WATT NO-FIRE FOR 5 MIN. MIN
B PRESS. CARTRIDGE						7A	10MS	100Hz	20-.1A	6 SEC	DC	" " " " " " " " " "
VII COMPUTER												
A SOLID STATE												
DC	6-35	.005-35	.005-1.0	DC	DC	50V	1MS	1MHz	50V	1MS	1MHz	.02 VOLT RIPPLE ON RETURN
AC	6-120	.005-.35	.005-5.	.5	400-1/3Φ	140V	1MS	1MHz	140V	1MS	1MHz	
B MAGNETIC CORE												
DC	5-35	.5-70	.1-2.0	DC	DC	60V	1MS	1KHz	200V	5MS	10KHz	
AC	6-120	6-300	1-5.0	.5	400-1/3Φ	150V	1MS	1KHz	600V	5MS	10KHz	
VIII ELECTROLYSIS	28-200	(25-30)KW		DC	DC							
IX SUPPORT EQUIP												
A BATTERY CHARGER												SLOWLY DECAYING CURRENT OVER LONG TIME PERIOD
DC INPUT	20-40	1-100W										
AC INPUT	100-200	1-100W		.5	400-3Φ							
B FUEL CELL SENS.												RAMP V OUTPUT PROPORTIONATE TO AMBIENT CONDITIONS
AC INPUT	20-120	.1-50		.5	400-1/3Φ							

1. Steady State Characteristics. - Those characteristics that describe the response of the load as reflected on the input power lines during non-transient periods of load operation.

2. Dynamic Characteristics. - Those characteristics that describe the response of the load during the turn-on, turn-off, and other non-steady-state intervals, including periodic and non-periodic phenomena.

In each case conservative estimates of the parameter ranges were used. Those estimates given in terms of a range identify both the lowest and highest values expected for that category of load. The estimates given as a single value are based on an expected worst-case value for the category concerned.

The criterion used in developing the subcategories of electrical loads was that a subcategory would be created within a major load category when either or both of the following load characteristics existed:

1. A dynamic range in input current or voltage in excess of 10:1.
2. A fundamental difference in input current characteristics e.g., digital versus analog.

3.3 INTERROGATOR AND SIMULATOR REQUIREMENTS

A set of requirements for an interrogator and a simulator was established to serve as a basis for developing and governing the investigative and trade-off phases of the study. These requirements are quantitative to the extent possible and are based primarily upon the load data presented in Table 3-3.

The requirements for a dynamic electric load interrogator and for a dynamic load simulator are discussed in further detail in Paragraphs 3.3.1 and 3.3.2, respectively.

3.3.1 Dynamic Electrical Load Interrogator Requirements

The interrogator, for the purposes of this study, is the measurement element of a system whose ultimate purpose is the simulation of certain electrical characteristics of a device. It is anticipated that hardware capable of meeting the performance criteria of this requirement will be used along with appropriate simulation hardware in testing the power conditioning and distribution systems of future manned spacecraft.

The interrogation process will be used to determine the input parameters of a device in sufficient detail that a simulator can be designed to duplicate the dynamic and steady state response of the device.

I. PERFORMANCE

A. General

The basic purpose of interrogation is the quantitative determination of those parameters of a device which describe its dynamic and steady-state electrical response on the power lines to a specified application of power. The interrogation process must take into account all modes of operation of the device and must cover the entire range of expected input voltages.

B. Load Characteristics

The device to be interrogated will typically have a dynamic driving point impedance. The input current waveform to such a device will be composed of four parts, as shown in Figure 3-3.

The operating voltage of the devices to be interrogated will range between 6 and 200 VDC and 6 and 220 VAC. The AC voltage will be 400 Hz, 1 or 3 phase; or 800 Hz, 2 phase. Device power consumption will be typically less than 1 KW.

C. Stimulation

The interrogation process must include the input voltage and other stimulation necessary to exercise the device in all modes of operation.

D. Instrumentation

The interrogation process must include all of the instrumentation necessary for sensing, measuring, storing, and processing the input data. Measurement parameter requirements are:

> Accuracy - The accuracy of the interrogation process must be such as to permit meaningful simulation of the device.
>
> Frequency Response - The frequency response of the interrogation process must be sufficient to permit quantitative identification of device behavior under transient conditions 10 microseconds or longer in duration.
>
> Dynamic Range - The dynamic range of the interrogation process must be suitable for quantitatively determining the input parameters listed on Table 3-3.
>
> Channel Capacity - The channel capacity of the interrogation instrumentation must be consistent with the number of input terminals. Ten channels will be a minimum design goal.
>
> Input Impedance - Instrumentation, including sensors, must be such that the characteristics of the device under test will not be altered. As a design goal, device characteristics should not be altered by more than 1%.

E. Data

All data must be obtained by electrically (electronically) interrogating the device under test. This raw data must be capable of being processed to yield final data in a format compatible with the simulator program input.

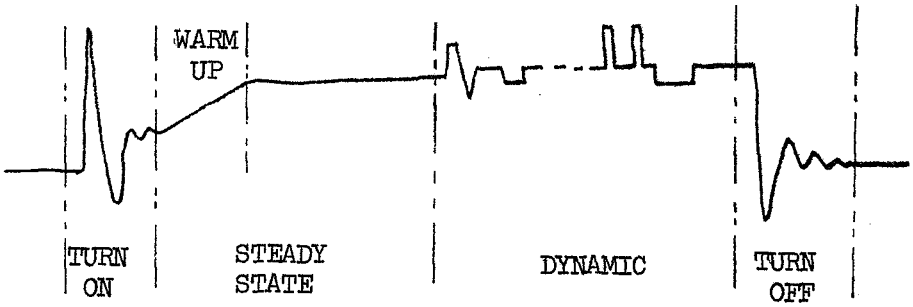


FIGURE 3-3 GRAPHICAL REPRESENTATION OF DYNAMIC ELECTRICAL LOAD CURRENT

F. Environmental

The interrogation hardware will be expected to meet all of its performance requirements when subjected to the temperature, humidity, and handling environments of a typical test laboratory.

G. Operating Time

The interrogation process must be capable of being automated, at least to the extent that a device may be interrogated frequently to determine the effects of altering selected device characteristics. The intent is to accomplish the interrogation in "real" time to permit the identification of device characteristics without significantly delaying test activities.

II. DESIGN AND CONSTRUCTION

A. Packaging

An interrogation scheme employing hardware that can be packaged in a single unit or central location will be a design goal.

B. Safety

The interrogation process may require operation at dangerous voltages and power levels. Accordingly, precaution must be taken in the design of the interrogation process to develop safe procedures and hardware configurations. Positive provisions for protecting test personnel and the devices under test must be incorporated.

3.3.2 Dynamic Electrical Load Simulator Requirements

The simulator, for the purposes of this study, is that element of a system whose ultimate purpose is the faithful representation of the dynamic electrical response of a hardware item. It is anticipated that hardware capable of meeting the performance criterions of this requirement will be used along with appropriate interrogation hardware in testing the power conditioning and distribution systems of future manned spacecraft.

The simulator will be used during ground tests of manned spacecraft to duplicate the dynamic and steady-state electrical response of individual load elements.

I. PERFORMANCE

A. Input Power

Input voltage to the simulator will range between 6 and 200 VDC and/or 6 and 220 VAC. The AC voltage will be 400 Hz single or 3-phase (3Θ), or 800 Hz-2Θ. The AC power factor will be 0.5 minimum. Entries in the volts, power factor, and source frequency columns under steady-state characteristics in Table 3-3 indicate the power requirements for each item. The remaining columns under steady-state characteristics list the anticipated power and current ranges each item must dissipate and draw (without degradation) for periods up to 1 hour. Dissipation of the heat generated by the simulator will be accomplished by proper heat sinking or other cooling equipment. However, utilization of such equipment must not impose any additional electrical requirements on the input power source beyond that of the device it is simulating.

B. Simulation Characteristics

The simulator will be a programmable device that will accurately reproduce on the input power circuit(s) the electrical characteristics of a spacecraft load element. It should be noted that the simulators are not to be simply scaled models of the hardware they represent. They will dissipate the same power levels as their hardware counterparts. Operation is defined as including transients experienced during turn-on and turn-off, conditions present during steady-state operation, and dynamic operating conditions. The load element to be simulated will be operated and interrogated. The operating parameters will then be stored in the simulator for application. A typical load waveform is shown in Figure 3-3.

Turn-on Transients - A typical listing of worst-case turn-on transients expected in the various categories is shown in Table 3-3 which lists the surge amplitude in volts or amperes, the duration of the transient effect, and the frequency of the transient pulse.

Steady-State Operation - This also includes the operating parameter warm-up. During warm-up the device to be simulated will draw more or less current for some finite period of time and then revert to its steady-state operating current. Typical warm-up parameters are listed in the turn-on transient column. Arbitrarily, if the transient duration is one second or longer, it may be considered warm-up. Typical operating steady-state characteristics of input voltage, power, current, power factor, and frequency source are listed in Table 3-3.

Dynamic Operation - A typical listing of the dynamic operating characteristics of the black boxes studied is given in Table 3-3 under Operating Remarks. As these remarks indicate, in some cases the input current will change linearly or exponentially over a given time period; in other cases the input circuit will reflect discrete current pulses.

Turn-Off Transients - Typical worst-case conditions inherent in the categories analyzed are listed in Table 3-3. These reflect their amplitudes in current or voltage, transient duration, and pulse frequency.

C. Control

The simulator must be capable of being programmed to operate over a wide voltage or current range with a time response of 10 microseconds or greater.

D. General Electrical Design Requirements

The simulator must include provisions to prevent damage to associated equipment under test in the event of a malfunction in the simulator or to the input power source. The simulator design must insure that it will not present an electrical hazard to any handling personnel. The simulator must be capable of being operated repeatedly without degradation.

E. Environments

The simulator must be operable within its design limits at normal ambient room temperatures. It must survive normal laboratory handling shock and be capable of being operated in any orientation.

II. DESIGN AND CONSTRUCTION

The simulator should occupy as small a volume as good design practice permits. The impedance elements of the simulator must be capable of being located in the same space occupied by the real load to permit the use of actual spacecraft cabling harnesses.

3.4 INTERROGATION AND SIMULATION TECHNIQUES

Once the interrogation and simulation requirements were defined, the next step in the study was to identify appropriate techniques for implementing these requirements.

A comprehensive literature search provided the information base essential to sound selection of interrogation and simulation techniques. This search is discussed in Paragraph 3.4.1. The interrogation and simulation techniques considered in the study are described in considerable detail in Paragraphs 3.4.2 and 3.4.3, respectively.

3.4.1 Literature Search

An extensive literature search was conducted to identify interrogation and simulation methods and techniques. This effort complemented that expended in compiling a comprehensive bibliography (Paragraph 8).

One phase of this search was concentrated on identifying the state-of-the-art in the areas of network analysis and network synthesis. This search, which yielded a promising file of publications, was conducted on the basis of the four extensive indexes listed in Table 3-4. This same table also indicates the key words used in this phase of the literature search. In addition to the network analysis and synthesis state-of-the-art investigation, Avco conducted an independent search in the area of computer technology--specifically in the following major areas of concentration:

1. Load Interrogation - The primary emphasis in this area was on determining what digital computer techniques are available for circuit synthesis and analysis.
2. Load Simulation - The search in this area was directed toward computer technology in process control, automated testing, and other real-time computer applications.

Information obtained during the library searches described above was supplemented by data obtained in response to letters of request sent to various vendors. The vendors questioned were those active in the areas of power dissipation elements, network analyses and measurement services, and variable impedance elements.

All of these efforts, plus those expended in compiling a bibliography, yielded the basic data necessary for meaningfully evaluating the interrogation and simulation requirements and techniques, defining appropriate trade-offs, and synthesizing a system concept.

3.4.2 Interrogation Techniques

Interrogation techniques fall into two basic areas - frequency domain and time domain. Table 3-5 summarizes various candidate interrogation techniques in these areas and presents pertinent descriptive information and trade-off data.

TABLE 3-4

LITERATURE SEARCH BIBLIOGRAPHY (NETWORK ANALYSIS AND SYNTHESIS)

Publication	Year	Key Words
Applied Science and Technology Index	1968-1969	Computers-Simulation Programs Electric Circuits Electric Circuits, Equivalent Electric Distribution Electric Transient Phenomena Impedance System Simulation Voltage Voltage Regulation
Engineering Index	1968-1969	Computers-Simulation Electric Circuits Electric Network Analyzers Electric Transmission
International Aerospace Abstracts	1968-1969	Breadboard Models Circuits Control Control Equipment Control Simulation Control Stability Electric Equipment Electric Networks Electric Power Electric Power Transmission Electrical Impedance Electronic Equipment Tests Equivalent Circuit Flight Simulators Linear Systems Network Analysis Network Synthesis Simulation Simulators Spacecraft Power Supplies
Scientific and Technical Aerosapce Reports (STAR)	1968-1969	SAME AS INTERNATIONAL AEROSPACE ABSTRACTS

TABLE 3-5 SUMMARY OF DYNAMIC ELECTRICAL LOAD INTERROGATION TECHNIQUES

METHOD	INTERROGATION SOURCE	RAW DATA	DATA PROCESSING	FINAL DATA	TRADE-OFF DATA
1. Impedance Bridge (Frequency Domain)	Sinusoid	$Z(\omega)$, Phase Angle	1. Plot $Z(\omega)$ and phase angle 2. Estimate model configuration 3. Optimize model response by iterative process of parameter value estimates and trial	Network model and parameter values	1. Raw data obtained at discrete frequencies. 2. Interrogation source not practically realized.
2. Impulse Response[a] (Frequency Domain)	Impulse	V, i = f(t)	1. Calculate $Z(\omega)$ 2. Plot $Z(\omega)$ 3. Estimate model configuration 4. Optimize (as for impedance bridge, above)	Network model and parameter values	1. Not suitable for non-linear devices. 2. Interrogation source not practically realized.
3. Rectangular Approximation (Frequency Domain)	Step	V, i = f(t)	1. Calculate $Y(\omega)$ 2. Plot $Y(\omega)$ 3. Estimate model configuration 4. Optimize (as for impedance bridge, above)	Network model and parameter values	1. Not suitable for non-linear devices.
4. Time Domain	Actual[b]	V, i = f(t)	1. Estimate model configuration 2. Optimize (as for impedance bridge, above)	Network model and parameter values	1. Applicable to linear and non-linear devices. 2. No unnecessary transformations or calculations

[a] The impulse response may also be obtained by cross-correlating a noise signal with the system output.

[b] Actual source means a source whose characteristics approximate those of the normal operating source.

In each interrogation scheme (except for the bridge method which measures the impedance directly) the basic data is obtained by stimulating the load and measuring the input voltage and current. The techniques differ basically in the method of stimulation selected and the data processing required. In each of the frequency domain techniques, the raw data is obtained in the time domain and then transposed into the frequency domain for further processing. This transformation--whether accomplished by Fourier techniques, rectangular (or trapezoidal approximation), or some other scheme--requires considerable computation and the approximations involved contribute inaccuracies. Also, these methods are restricted to linear devices.

The time domain technique, on the other hand, does not require domain transformation since the data is both acquired and used in the time domain. Furthermore, this technique is not limited to linear systems.

> Frequency Domain Techniques - In the frequency domain techniques the data is processed to yield impedance versus frequency, Z(W) information. A network model consisting of resistance (R), capacitance (C), and inductance (L) components is estimated and component values are assigned arbitrarily. This model is then optimized in a computer by an iterative process of judicious component value estimation followed by a comparison of the model's response with the calculated response of the original load as determined from the interrogation data. The final values resulting from this process are then printed out and a real network is constructed (or programmed) to conform to this configuration.
>
> Time Domain - In the time domain technique the device input current waveform, determined during interrogation, is duplicated by a network model much as in the case of the frequency domain techniques described previously. An estimate is made of a model configuration of R, L and C components and component values are assigned arbitrarily. The model response is then optimized by computer. The final values of R, L, and C are printed out. These represent the optimum value of each model component for the desired response. Much depends on the initial model configuration estimate since the computation involves only changes in component value. In any event, the final result is the best achievable for the particular model chosen. A significant parameter in this (or any) optimization process is the criterion used in judging "goodness-of-fit" of model response to the response of the real device. Optimization and criterion selection are covered in more detail in Paragraph 5 of this report.

3.4.3 Simulation Techniques

Two fundamental techniques for simulating the dynamic response characteristics of a device have been identified. They are: (1) network models comprised of R, L, and C components whose values can be adjusted to yield an impedance variation with time and, (2) variable resistance devices whose resistance is varied as a function of time to duplicate the voltage/current (V/I) ratio of the interrogated device.

Both techniques may be combined in a hybrid configuration. This permits, for example, the model to provide the steady-state response characteristics and the variable resistance to provide the dynamic response.

Table 3-6 summarizes load simulation techniques.

TABLE 3-6 LOAD SIMULATOR TECHNIQUES

METHOD	DESCRIPTION
NETWORK MODEL	R, L, C NETWORK WHOSE ELECTRICAL RESPONSE DUPLICATES THAT OF INTERROGATED LOAD.
VARIABLE RESISTANCE	CONTINUOUSLY VARIABLE RESISTANCE WHOSE VALUE IS EQUAL TO V/I OF INTERROGATED LOAD AT EACH POINT IN TIME.
HYBRID	COMBINATION OF NETWORK MODEL AND VARIABLE RESISTANCE TECHNIQUES.

3.4.3.1 Network Models

Network models can be constructed of passive components (R,L,C) and suitably adjusted such that model response to stimulation corresponds to that observed for the real device.

The model configuration and component values are determined during the interrogation process.

It should be noted that the network models of a simulator would not be scaled but would in fact dissipate power of the same levels as the real devices.

3.4.3.2 Variable Resistance

This method takes the analog voltage and current data obtained during interrogation and calculates

$$R(t) = \frac{V(t)}{i(t)}$$

at selected points in time. This calculation can be accomplished in either analog form (by using a divider circuit) or digital form (after converting the data using an analog-to-digital converter and then returning the processed data to analog form with a digital-to-analog (D/A) converter). In either case the R(t) is an analog representation of the voltage-current ratio over the entire duration of device operation.

If a magnetic tape is used to record the R(t), the tape need only be conditioned (amplified or attenuated) to permit it to serve as the programming input to a simulator. A more practical method would process the R(t) and store it in digital format. This would facilitate synchronization of the R(t) with timer or source frequency.

The entire process is easily mechanized and operates in real time.

There are, however, difficulties in using this process for alternating current (AC) circuits in which there is a significant phase difference in the voltage and current waveforms. However, the technique is promising in the DC case and is applicable to non-linear as well as linear networks.

4. AREAS OF INVESTIGATION

Investigative effort during the study was concentrated on those elements of the interrogation and simulation techniques for which there was little available data. The objective of the investigation in any particular area was to evaluate the concept only to the extent that its feasibility and practicality could be determined. No attempt was made to optimize a technique.

Certain elements of the interrogation process, e.g., data acquisition, were well-known, and standard laboratory techniques were more than adequate for accomplishing this phase of the process. Other elements, such as continuously variable impedance elements, modelling techniques, and computer optimization routines, were not as well known. Thus, the more intensive investigative efforts during the study were concentrated on these elements.

4.1 VARIABLE IMPEDANCE ELEMENTS

Table 4-1 summarizes variable impedance concepts identified during the study and presents estimates of device limitations. Several of the more promising of these concepts were examined in some detail and these examinations are described in the following discussions.

4.1.1 Variable Resistance Elements

All simulation schemes require resistive elements for power dissipation. In addition, some means must be provided for changing component values to accommodate changes in the resistance requirements. Simple schemes, such as switching high-power-rated resistors could provide this variability, but only at the expense of requiring large equipments to house the many different values of resistance, and complex switching schemes to utilize them most efficiently. A more efficient and versatile means of obtaining a variable resistance is based on using analog circuits whose input resistance is caused to vary as a function of a control voltage.

Several techniques for doing this were investigated in some detail.

TABLE 4-1 PRELIMINARY RANGE DATA OF VARIABLE IMPEDANCE DEVICES

Device	AC Voltage Capability	DC Voltage Capability	Power Dissipation Capability	Frequency Response Capability	Element Capability
	V, rms	volts	watts		
Impedance Multiplier	Peak Multiplier Supply Voltage = M (Input Voltage), where M is the multiplication factor		50	50 KHz	$10<R<10$ M 0.1 $H<L<10$ H 0.005 $uF<C<500$ uF
Rotator:					
A. Solid State	125	200	25 at 200 volts, 100 at 50 volts	50 KHz	$10<R<10$ M 0.1 $H<L<10$ H 0.005 $uF<C<500$ uF
B. Vacuum Tube	440	650	"	"	"
Transistor Resistance	125	175	100 at 50 volts, 25 at 175 volts	200 KHz	$0.1<R<100$ K
Saturable Core Reactor	440	650	Limited by physical size	a	1 $uH<L<100$ H
Switched Component	440	650	500	1 MHz	$0.1<R<100$ K, L & C limited by physical size

a To be determined.

4.1.1.1 Rotators

The rotator is a two-port device that has the property that when a resistor is connected to one port, the resulting characteristics of the other port are the voltage versus current characteristics of the resistor rotated by a prescribed angle.

I. Operational Amplifier Type

Figure 4-1 is a schematic diagram of an R-rotator circuit. If resistance R1 is large compared to the resistance synthesized by the circuit, then current i_4 (Figure 4-1) can be considered negligible, and

$$i_1 \approx i_x = \frac{e_1 - e_3}{R_x} \tag{Eq. 4.1}$$

where

i_1 - input current, in amperes

i_x - current from port 1 to port 2, in amperes

e_1 - input voltage, in volts

e_3 - amplifier output voltage, in volts

Rx is the resistance connected across port 2, in ohms. With reference to Figure 4-1, the amplifier output voltage, e_3 can be expressed as

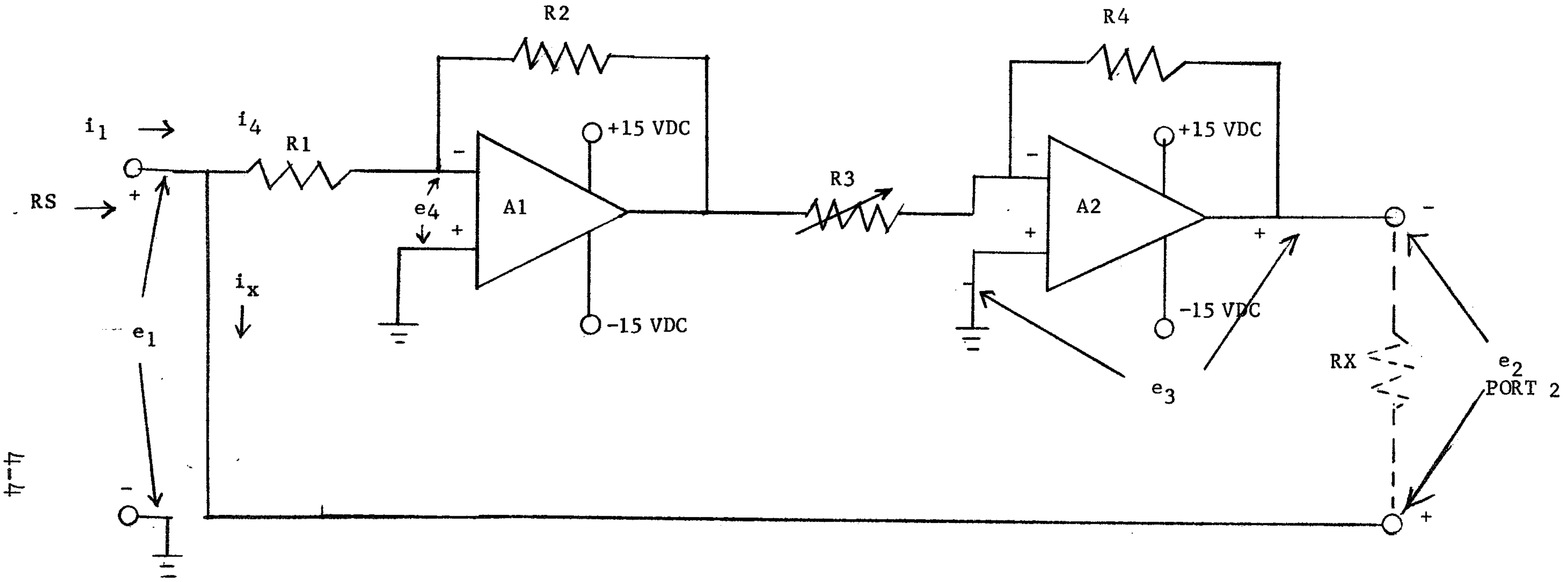
$$e_3 = A_v e_1 \tag{Eq. 4.2}$$

where A_v is the circuit voltage gain. If Equation 4.2 is substituted into Equation 4.1, then

$$i_1 \approx i_x = \frac{e_1 - A_v e_1}{R_x} \tag{Eq. 4.3}$$

The input resistance, R_s, can be expressed as

$$R_s = \frac{e_1}{i_1} \approx \frac{e_1}{i_x} \tag{Eq. 4.4}$$



R1 = R2 = R4 = 100 K ohm ½ watt 5% carbon resistor

R3 = 100 K ohm 5 watt carbon potentiometer

A1 = A2 = operational amplifier Philbrick Researches Inc. Model P2

FIGURE 4-1 OPERATIONAL AMPLIFIER TYPE ROTATOR

If Equation 4.3 is substituted into Equation 4.4, then

$$R_x \approx \frac{e_1 R_x}{e_1 - e_1 A_v} \approx R_x\left(\frac{1}{1 - A_v}\right) \qquad \text{(Eq. 4.5)}$$

Equation 4.5 indicates that the circuit input resistance, R_s, is a function of the terminating resistance, R_x, and the voltage gain of the circuit. Thus, if the voltage gain of the circuit can be varied by a control signal, a resistance whose magnitude can be varied may be synthesized. Several methods of varying amplifier gain by controlled signals are feasible.

If the operational amplifiers shown in Figure 4-1 are considered to be ideal, then the circuit voltage gain

$$A_v = \frac{R2\ R4}{R1\ R3} \qquad \text{(Eq. 4.6)}$$

However, since R1 = R2,

$$A_v = \frac{R4}{R3} \qquad \text{(Eq. 4.7)}$$

Substituting Equation 4.7 into Equation 4.5 gives:

$$R_s \approx \left(\frac{1}{1 - \frac{R4}{R3}}\right) \qquad \text{(Eq. 4.8)}$$

Equation 4.8 indicates that the magnitude of the resistance synthesized can be varied by changing the magnitude of resistance R3 or R4. Equation 4.5 indicates that negative resistance can be synthesized by a circuit gain of one or greater. If the circuit gain is less than one, the resistance synthesized will be positive.

Chua[1] indicates that for angles of rotation less than 50°, the percentage of maximum rotator error is less than the percentage error caused by circuitry parameter variations. Thus, good design practice would indicate that if high angles of rotation are required, they can best be achieved by the use of rotators connected in cascade.

---

[1] Chua, Leon O.; The Rotator - a New Network Component; Proceedings, IEEE, Vol. 55, No. 7, Sept. 1967.

While theory indicates that rotators have an infinite bandwidth, in practice the operation of the rotator deteriorates as frequency increases. The bandwidth of a rotator is determined by the circuitry and devices used to implement the rotator. In general, operational amplifier circuits have frequency limitations of approximately 50 KHz. Thus high frequency rotators would utilize circuits specifically designed for the rotator. If small values of resistance are to be synthesized, these circuits would be required to supply high stand-by currents and power dissipation will be high. However, it appears that several rotator circuits may be connected in parallel to reduce the currents required from the rotator circuitry.

II. Controlled-Source Type

Figure 4-2 shows the schematic diagram of a controlled-source type rotator. This circuit uses a controled source whose output voltage is equal to the voltage on the control terminal. If resistances A and B are large compared to the resistance synthesized by the circuit, Equations 4.1 through 4.5, above, also apply to the circuit. Because the voltage gain of the controlled source is unity, the voltage across resistor R_B will equal e_3. The voltage e_4 across resistor R_B is a function of the input voltage e_1 and is given by

$$e_4 = \frac{RB}{RA+RB} e_1 = e_3 \qquad \text{(Eq. 4.9)}$$

Equation 4.9 indicates that the voltage gain, A_v, of this circuit is given by

$$A_v = \frac{RB}{RA+RB} \qquad \text{(Eq. 4.10)}$$

If Equation 4.10 is substituted into Equation 4.5, the result is

$$R_s \approx R_x \left(\frac{1}{1 - \frac{RB}{RA+RB}} \right) \qquad \text{(Eq. 4.11)}$$

Equation 4.11 indicates the circuit input resistance is a function of resistances RA and RB. Current i_x will flow through the controlled source in the reverse direction. Most controlled sources are fabricated from unilateral devices which do not permit reverse currents to flow. A resistor and a diode were added to the circuit, as shown in Figure 4-3, to provide a path for current i_x around the controlled source.

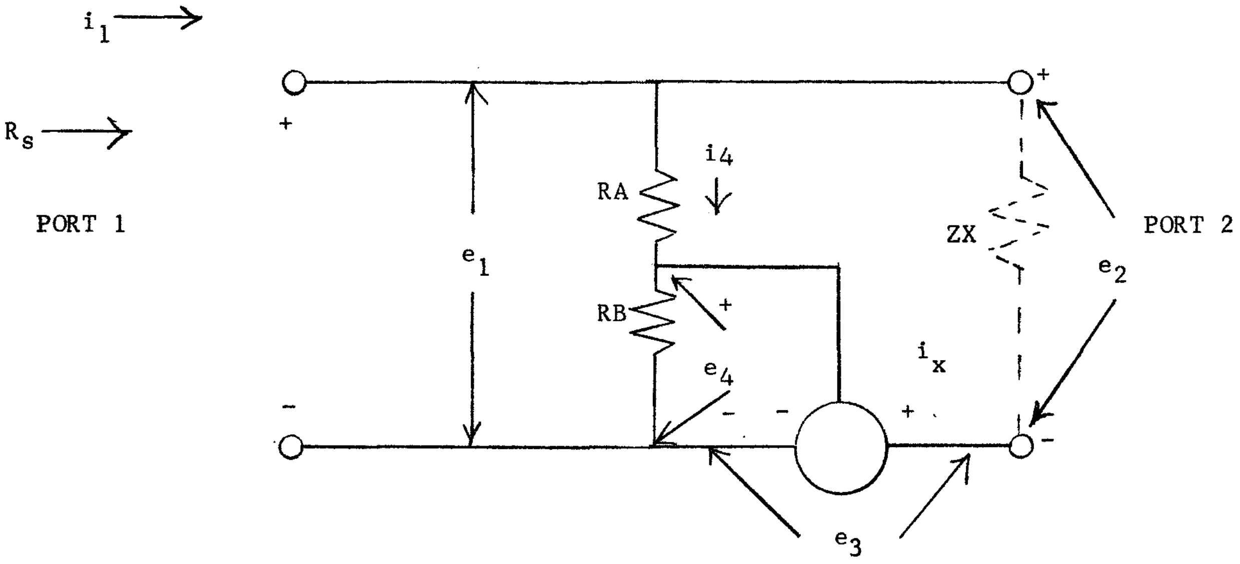
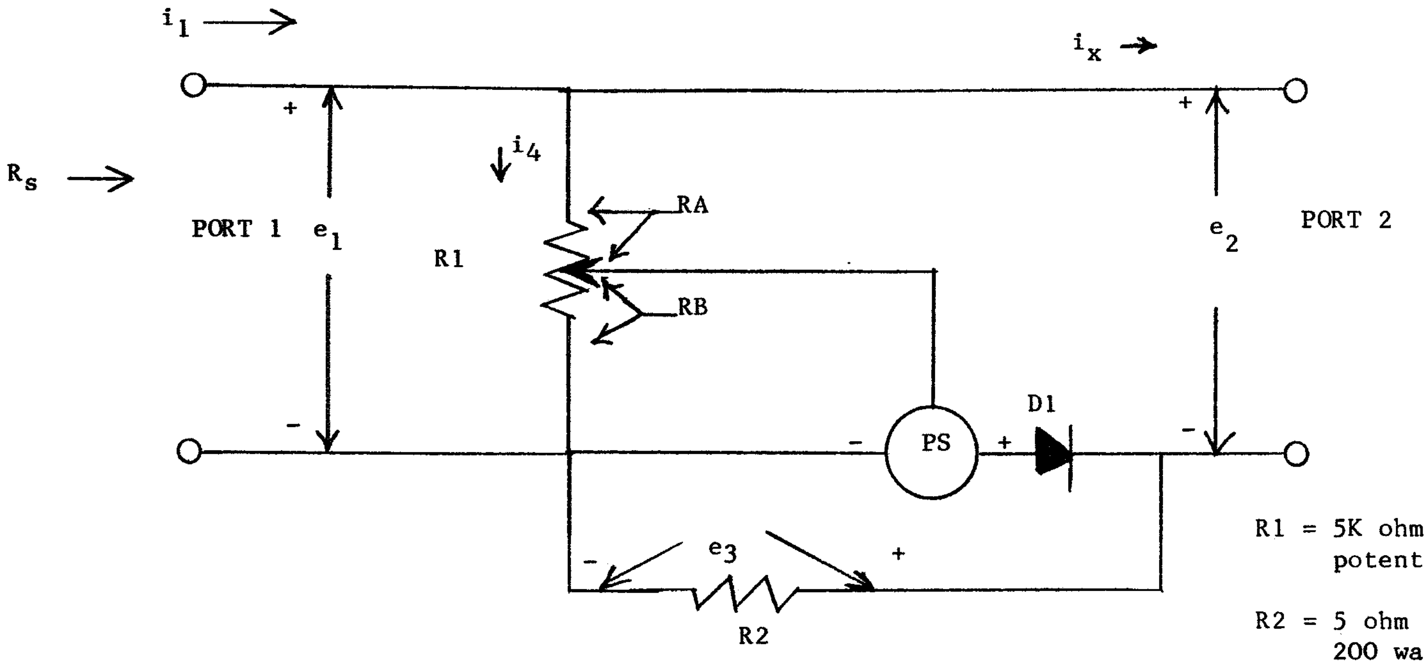


FIGURE 4-2 ROTATOR CIRCUIT USING A CONTROLLED SOURCE



R1 = 5K ohm carbon 5 watt potentiometer

R2 = 5 ohm wirewound resistor 200 watt

D1 = diode RCA type IN 1204A

PS = power supply Hewlett Packard model 6274A TAG 11721 connected in remote voltage program mode

FIGURE 4-3 PRACTICAL ROTATOR CIRCUIT

4.1.1.2 Multiplier Controlled Current Sinks

Another method of realizing a continuously variable resistance is by the use of an analog circuit using a multiplier, an operational amplifier, and a transistor power stage. This concept--called a multiplier-controlled current sink (MCCS)--is described in the following discussion.

I. DC Type Current Sink

Figure 4-4 is a schematic of a current interrogator. It consists of a simple resistance in series with the unknown load shown as $R_1(t)$. As R_1 varies with time, V_1 will also vary and will represent the real-time current through the load. Having achieved a function for $I_1(t)$, this is stored by any one of a number of means for later use as the control voltage for the MCCS.

Figure 4-5 is a schematic of a DC MCCS circuit. The circuit utilizes an analog multiplier, an operational amplifier and a power gain stage for the operational multiplier. The command signal, $V_1(t)$, is applied to the B input of the multiplier and a fraction of $E_2(t)$ is applied to the A input. The attenuation factor for the input is specified as $1/E_1$ where E_1 is the voltage used for interrogation in Figure 4-4. If $E_2(t)$ is equal to E_1, then the A input is equal to 1 volt and the output of the multiplier is equal to the multiplier scale factor times the B input. If $E_2(t)$ changes to $(1/2)E_1$, then the A input will equal 1/2 volt and the multiplier output will equal 1/2 its original value. The mulitplier output is therefore a control function that is modified by the voltage $E_2(t)$. This modified control function is applied to the non-inverting input of the operational amplifier whose gain is equal to the inverse of the multiplier gain. The amplifier loop is closed from the emitter of Q_2 to the inverting input and the result is that $V_1(t)$ appears across the load resistor R_3 and the current $I_2(t)$ is equal to $V_1(t)/R_3$.

The following analysis will show that the device input resistance equals the "unknown" resistance. Consider the interrogator circuit of Figure 4-4 and the simulator circuit of Figure 4-5.

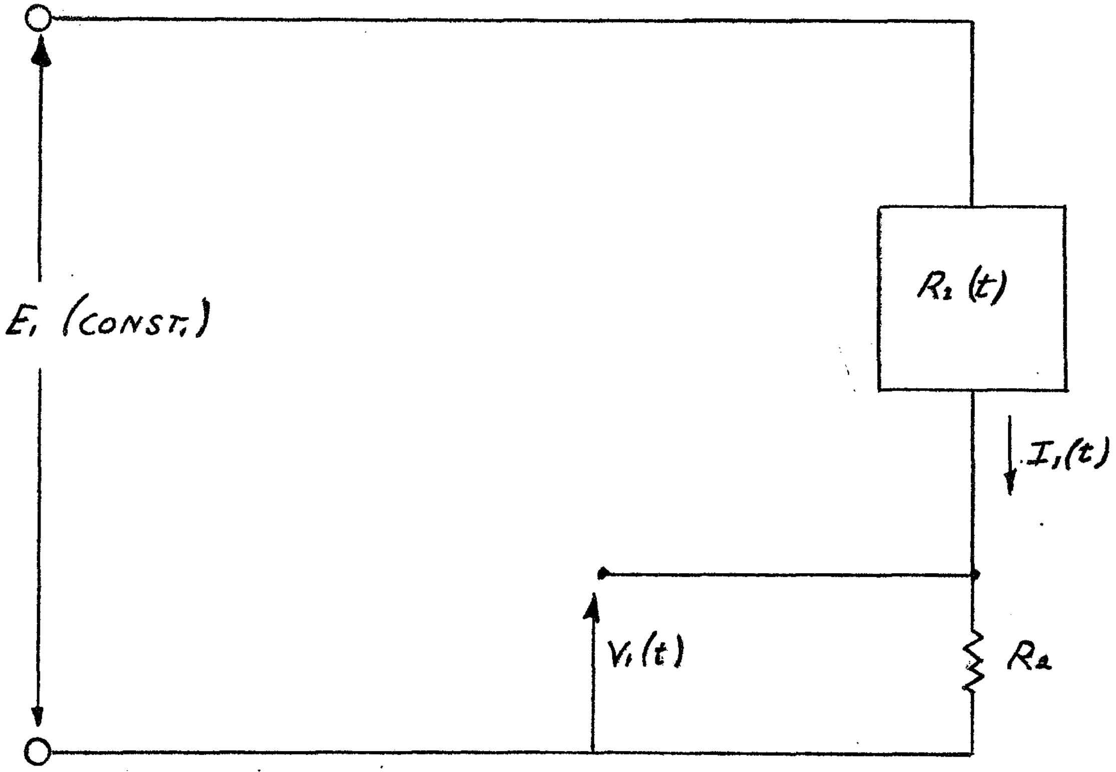
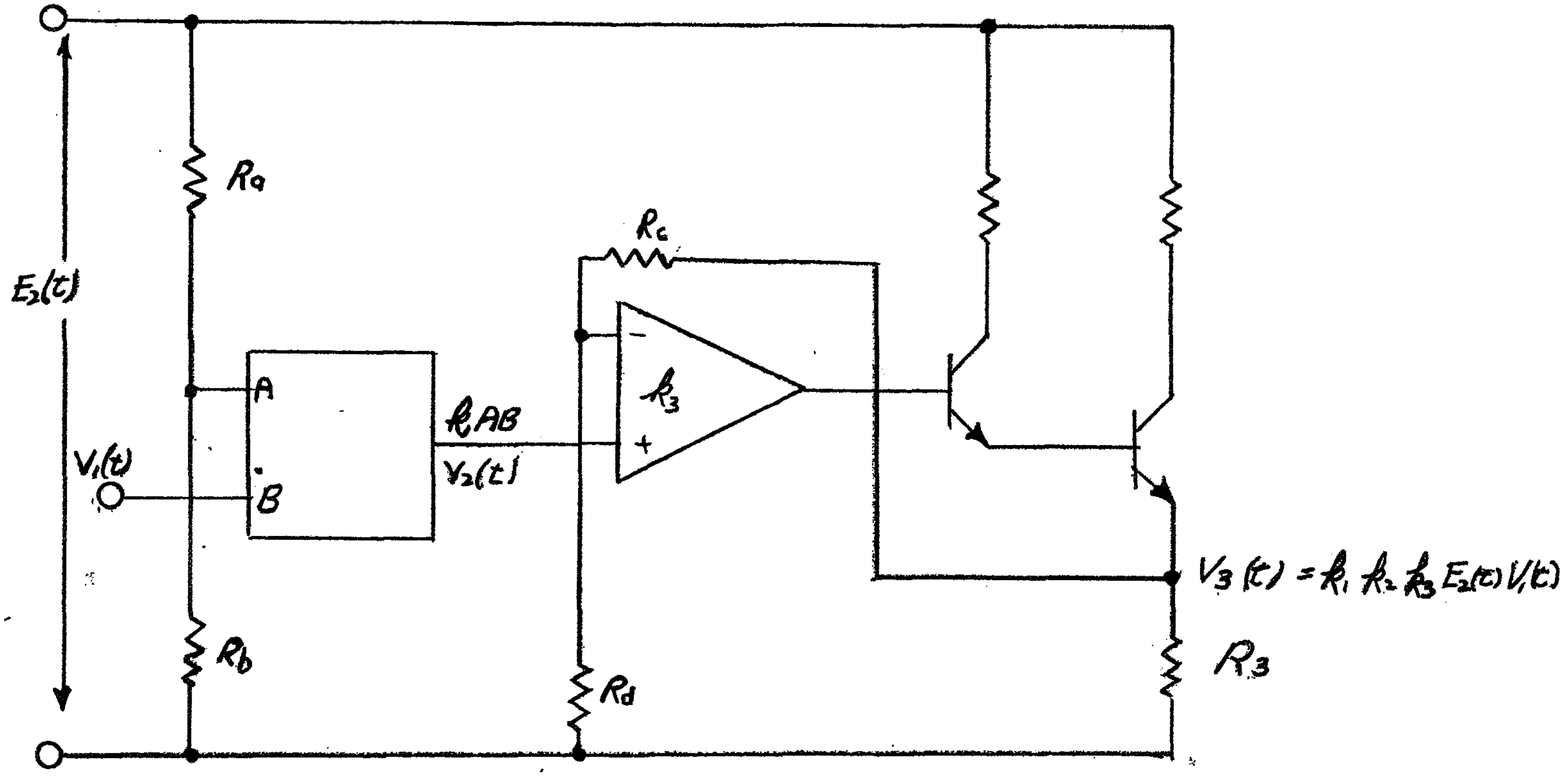


FIGURE 4-4 DC INTERROGATOR



$$k_2 = \frac{R_b}{R_a + R_b} \qquad k_1 = \frac{R_d}{R_c + R_d} = \frac{1}{k_3}$$

FIGURE 4-5 DC VOLTAGE-CONTROLLED RESISTANCE SIMULATOR

In Figure 4-4,

$$I_1(t) = E_1/R_1(t) = V_1(t) \qquad \text{if} \quad R_s = 1 \qquad \text{(Eq. 4.12)}$$

and in Figure 4-5,

$$V_2(t) - k_1 k_2 AB \qquad \text{(Eq. 4.13)}$$

where

k_1 = multiplier constant

$k_2 = 1/E_1$

Then,

$$V_2(t) = k_1 k_2 V_1(t) E_2(t) \qquad \text{(Eq. 4.14)}$$

and

$$V_3(t) = k_3 V_2(t) \qquad \text{(Eq. 4.15)}$$

where

k_3 = amplifier gain

and

$$I_2(t) = \frac{V_3(t)}{R_3} = k_3 V_2(t) = k_1 k_2 k_3 V_1(t) E_2(t) \qquad \text{(Eq. 4.16)}$$

If

$$R_3 = 1\Omega$$

then

$$\begin{aligned} R_2(t) &= E_2(t)/I_2(t) \\ &= \frac{E_2(t)}{k_1 k_2 k_3 V_1(t) E_2(t)} \end{aligned} \qquad \text{(Eq. 4.17)}$$

but

$$k_3 = 1/k_1$$

$$k_2 = 1/E_1$$

and

$$R_2(t) = \frac{E_2(t)\,E_1}{V_1(t)\,E_2(t)} = \frac{E_1}{V_1(t)} \qquad \text{(Eq. 4.18)}$$

Substituting Equation 4.12 into Equation 4.18, gives

$$R_2(t) = R_1(t)$$

II. AC-Type Current Sink

An AC MCCS is very similar to that of the DC MCCS. The requirements are identical in that a power consuming device must be interrogated, the resulting control function must be stored, and the simulator must reproduce the original results. The concept is similar in that a current is sampled and the current through the simulator is controlled. In this case, the output of the interrogator is the rms current through the load under interrogation. The condition that the rms voltage applied to the load under interrogation be constant and known applies similarly to this case.

Figure 4-6 is a schematic of an AC load interrogator. A small value resistor is placed in series with the load under test and the voltage developed across the resistor is proportional to the current flowing through it. The voltage developed is converted to an rms value and stored for later use as the command input to the simulator.

Figure 4-7 is a schematic of an A.C. MCCS which is essentially the same as the one shown in Figure 4-5, the difference being the bilateral power stage. The command applied to the B input to the multiplier is proportional to the rms current desired and is essentially a positive D.C. signal. The signal applied to the A input is a scaled portion of $E_2(t)$ but in this case, $E_2(t)$ is equal to $E_2 \text{Sin } wt$ and contains both positive and negative values. The output of the multiplier will, therefore, be negative when $E_2(t)$ is negative and as in the case of the DC simulator, the output of the multiplier multiplied by the amplifier gain will appear as $V_3(t)$ across R_3.

Again, it can be shown that the device resistance equals the "unknown" resistance.

Consider the circuit diagram in Figure 4-6. $V_1(t)$ is a positive command function that may change with time and has a scale factor of 1V/RMS amp required. E_1 is constant.

$$I_1(t) = E_1(t)/R_1(t) = \frac{E_1 \sin \omega t}{R_1(t)} \qquad \text{(Eq. 4.19)}$$

$$V_1(t) = I_1(t) R_1 = I_1(t) \quad \text{if} \quad R_s = 1 \qquad \text{(Eq. 4.20)}$$

$$= \frac{E_1(rms)}{R_1(t)}$$

Now, consider the circuit in Figure 4-7:

$$V_2(t) = k_1 k_2 V_1(t) E_2(t)$$

$$= k_1 k_2 V_1(t) E_2 \sin \omega t$$

where

k_1 = multiplier gain

$k_2 = 1/E_1(rms)$ where E_1 is from Figure 4-7.

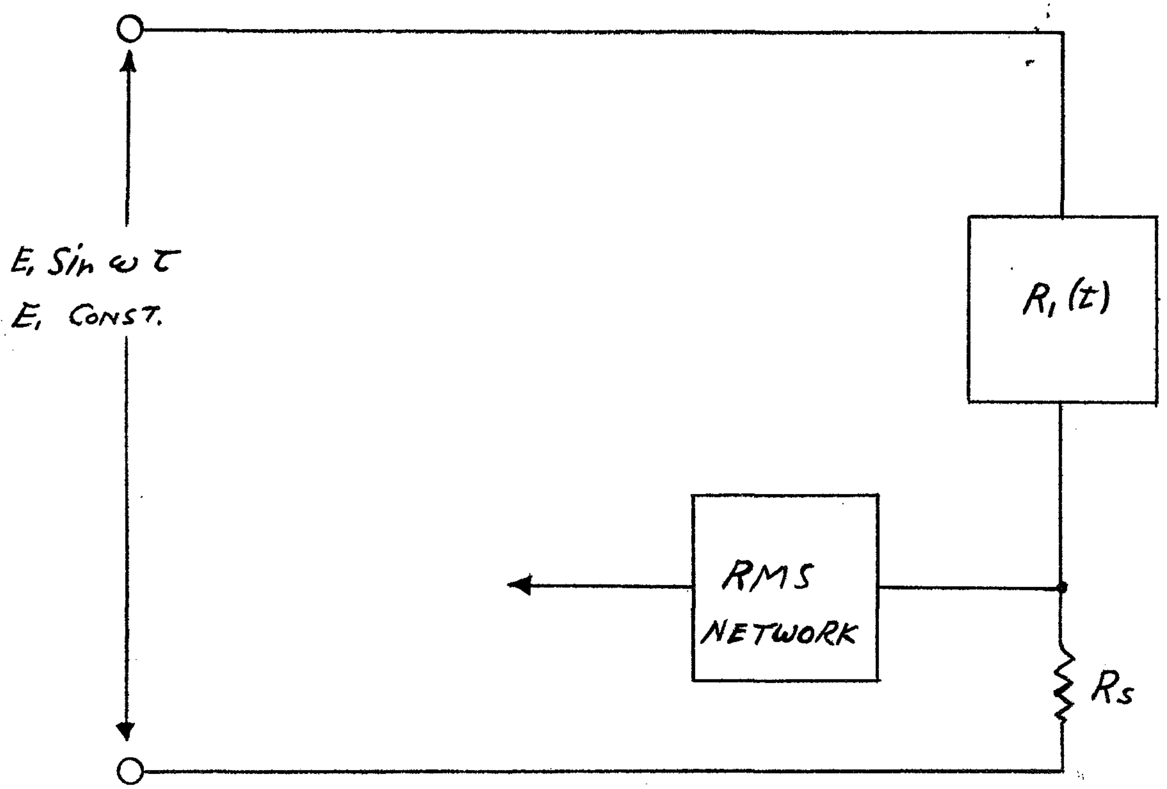
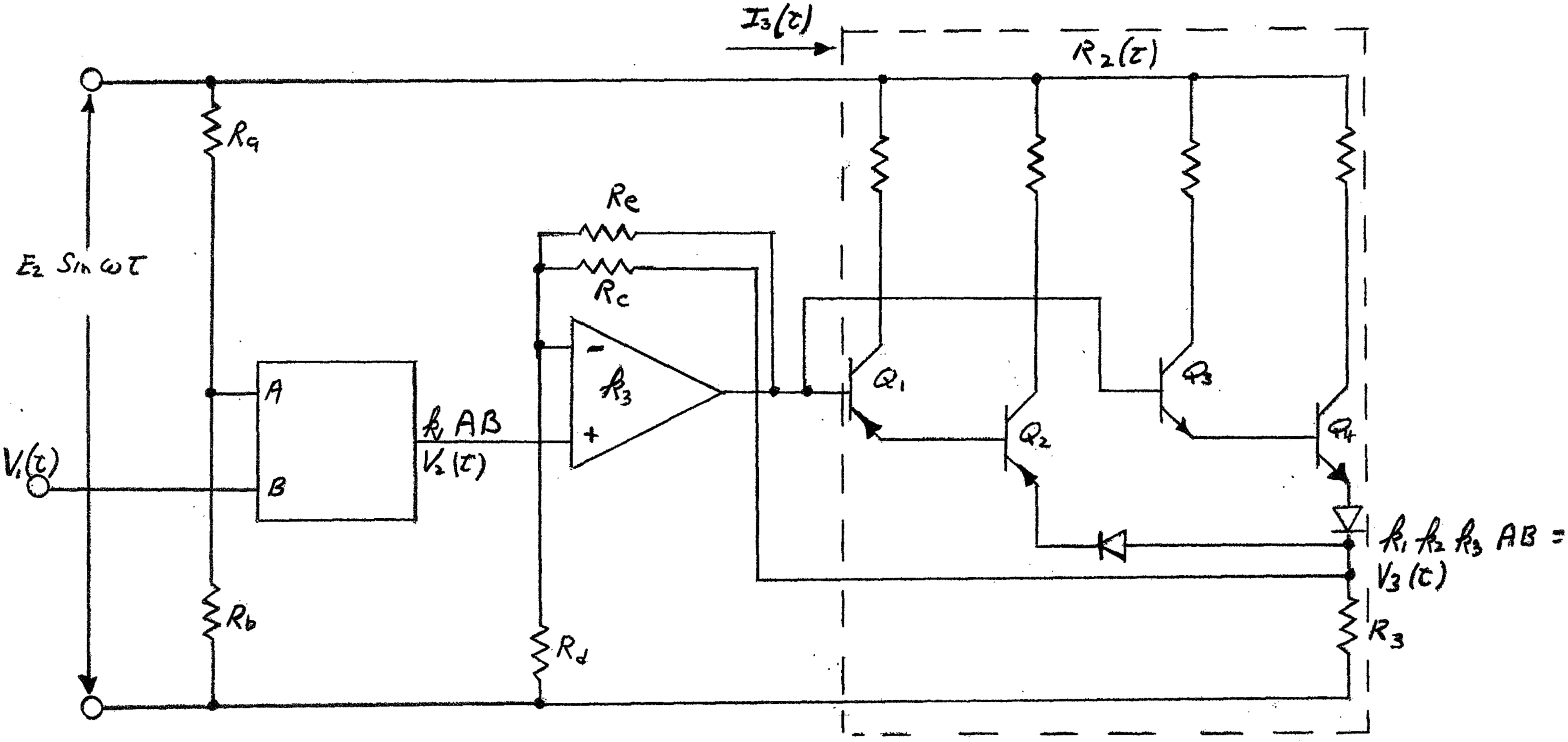


FIGURE 4-6 AC INTERROGATOR



$$k_2 = \frac{R_b}{R_a + R_b} \qquad k_3 \cong \frac{R_c + R_d}{R_d} = \frac{1}{k_1} \qquad R_e \geqslant 10 R_c$$

NOTE: $Q_1 + Q_2$ CONDUCT WHEN $E_2 \sin \omega \tau$ IS NEGATIVE
$Q_3 + Q_4$ CONDUCT WHEN $E_2 \sin \omega \tau$ IS POSITIVE

FIGURE 4-7 AC VOLTAGE-CONTROLLED RESISTANCE SIMULATOR

$$V_2(t) = \frac{k_1 V_1(t) E_2 \sin \omega t}{E_1 (rms)} \qquad \text{(Eq. 4.21)}$$

and

$$V_3(t) = k_3 V_2(t) \qquad \text{when} \qquad k_3 = 1/k_1$$

$$V_3(t) = \frac{V_1(t) E_2 \sin \omega t}{E_1 (rms)} \qquad \text{(Eq. 4.22)}$$

then

$$I_2(t) = V_3(t)/R_3 = V_3(t) \qquad \text{if} \qquad R_3 = 1$$

$$I_2(t) = \frac{V_1(t) E_2 \sin \omega t}{E_1 (rms)} \qquad \text{(Eq. 4.23)}$$

and

$$\begin{aligned} R_2(t) &= E_2(t)/I_2(t) \\ &= \frac{E_2 \sin \omega t \; E_1(rms)}{V_1(t) E_2 \sin \omega t} \\ &= \frac{E_1(rms)}{V_1(t)} \end{aligned} \qquad \text{(Eq. 4.24)}$$

Substituting Equation 4.20 into Equation 4.24 gives

$$R_2(t) = R_1(t)$$

It should be noted that changes in $V_1(t)$ will be limited by the time constant of the rms network in Figure 4-7, and the system will not be capable of reproducing step changes.

III. Limitations

A. DC-Type Current Sink

The frequency response of the DC system will be determined by the storage system or possibly by the multiplier. Typical multiplier performance will provide a response of 500 KHz with 2% attenuation.

The power handling capability for a single stage operating at 28 VDC has been analyzed. Figure 4-8 shows the key parameters together with the result that 390 watts can be handled. Additional output stages including the drive transistors, their collector and emitter resistors and pre-amplifier may be added in parallel. Figure 4-9 is a proposed parallel application.

B. AC-Type Current Sink

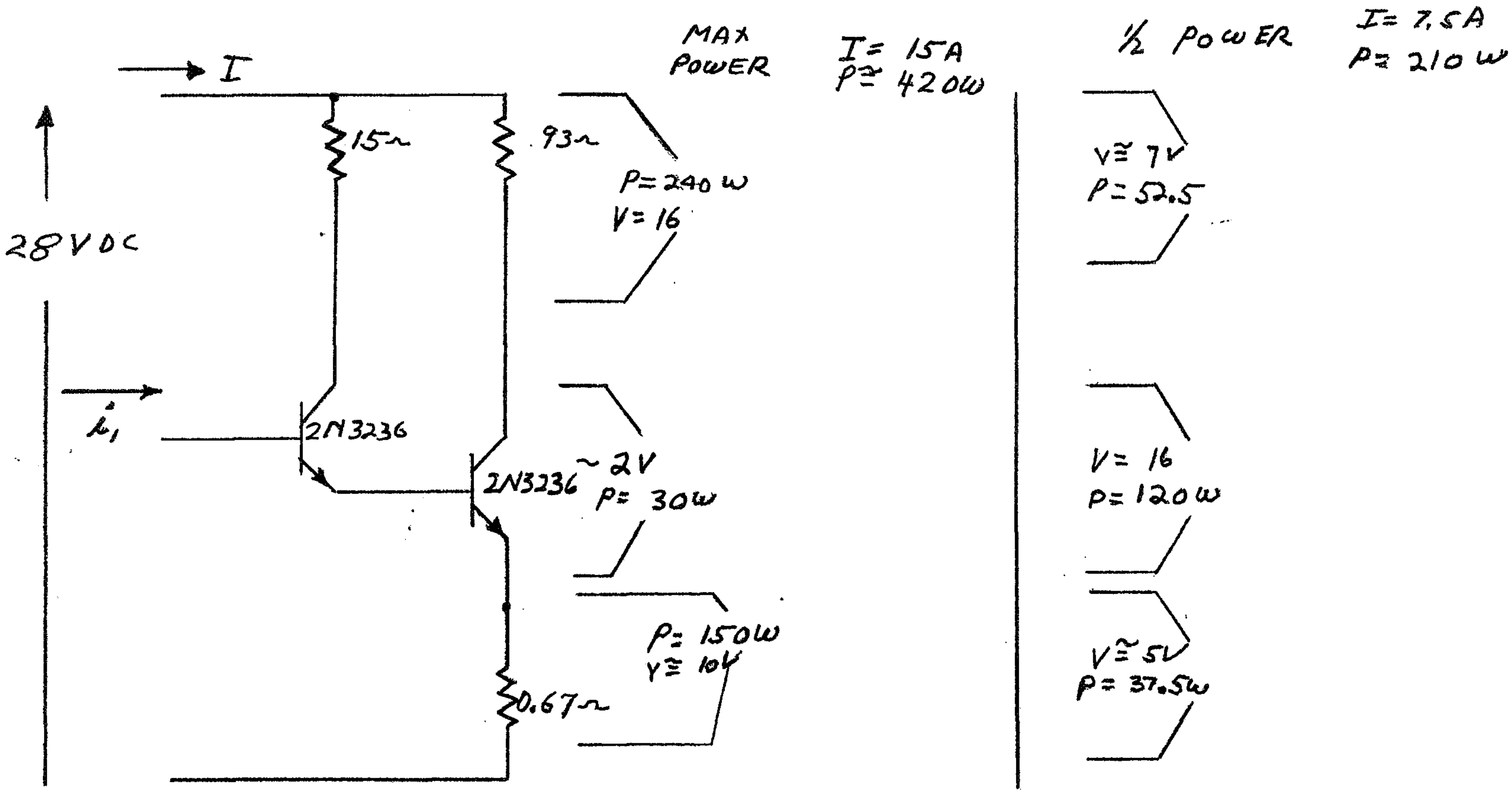
The frequency response of the A-C system is limited strictly by the rms network shown in Figure 4-6. The problem trade-off between the requirement to rectify and filter the voltage appearing across R_3 and to detect changes in the rms value. A reasonable compromise is to set the corner frequency of the filter at W/10. In the case of a 400 Hz application, this would limit the transient response to 40 Hz and this is clearly the limit for the system.

The power handling capability for the A-C case is somewhat complicated by the lack of PNP power transistors available with an adequate BV_{ceo} rating. The transistor must handle the peak A-C voltage in the forward direction. The diodes protect each stage in the reverse direction. Figure 4-10 is a schematic and analysis of the bilateral A-C power stage. The result of this analysis indicates a power limit of 220 watts. Additional stages may be added in a manner similar to that shown in Figure 4-9 if more power is required.

The A-C interrogator/simulator described herein is theoretically incapable of producing a phase shift. This phenomenon requires that at certain times during the A-C cycle the current be opposite to the voltage and this result can be achieved only if energy storage devices are used or if a power source is available within the simulator. Neither of these conditions exist.

4.1.1.3 Laboratory Experiments

Both rotators and current sinks were constructed during the study and demonstrated under dynamic conditions. In one experiment a dynamic load (several resistors and switches) was interrogated.



2N3236

I_c = 15A max.
P_c ≐ 150W "
β ≐ 17 min

β^2 = 290 min

$$i_1 = \frac{15}{290} = .052 \text{ max}$$

FIGURE 4-8 DC POWER STAGE SCHEMATIC DIAGRAM AND ANALYSIS

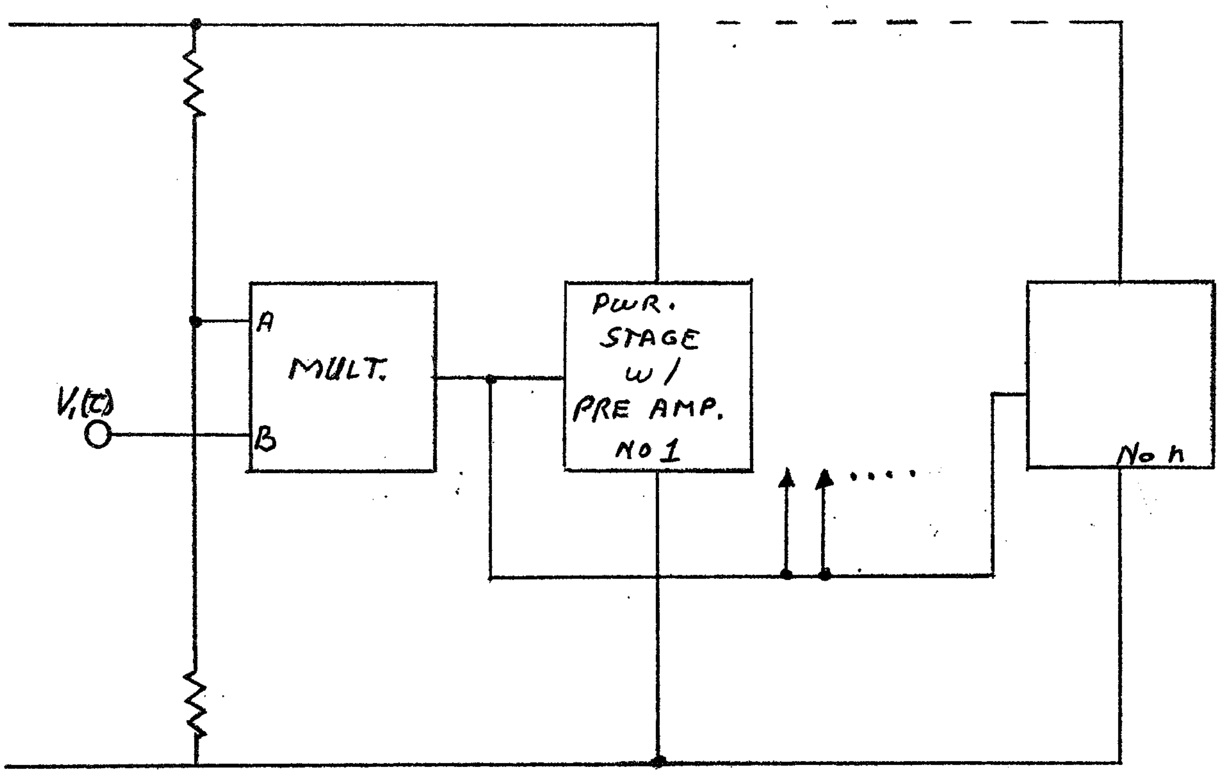
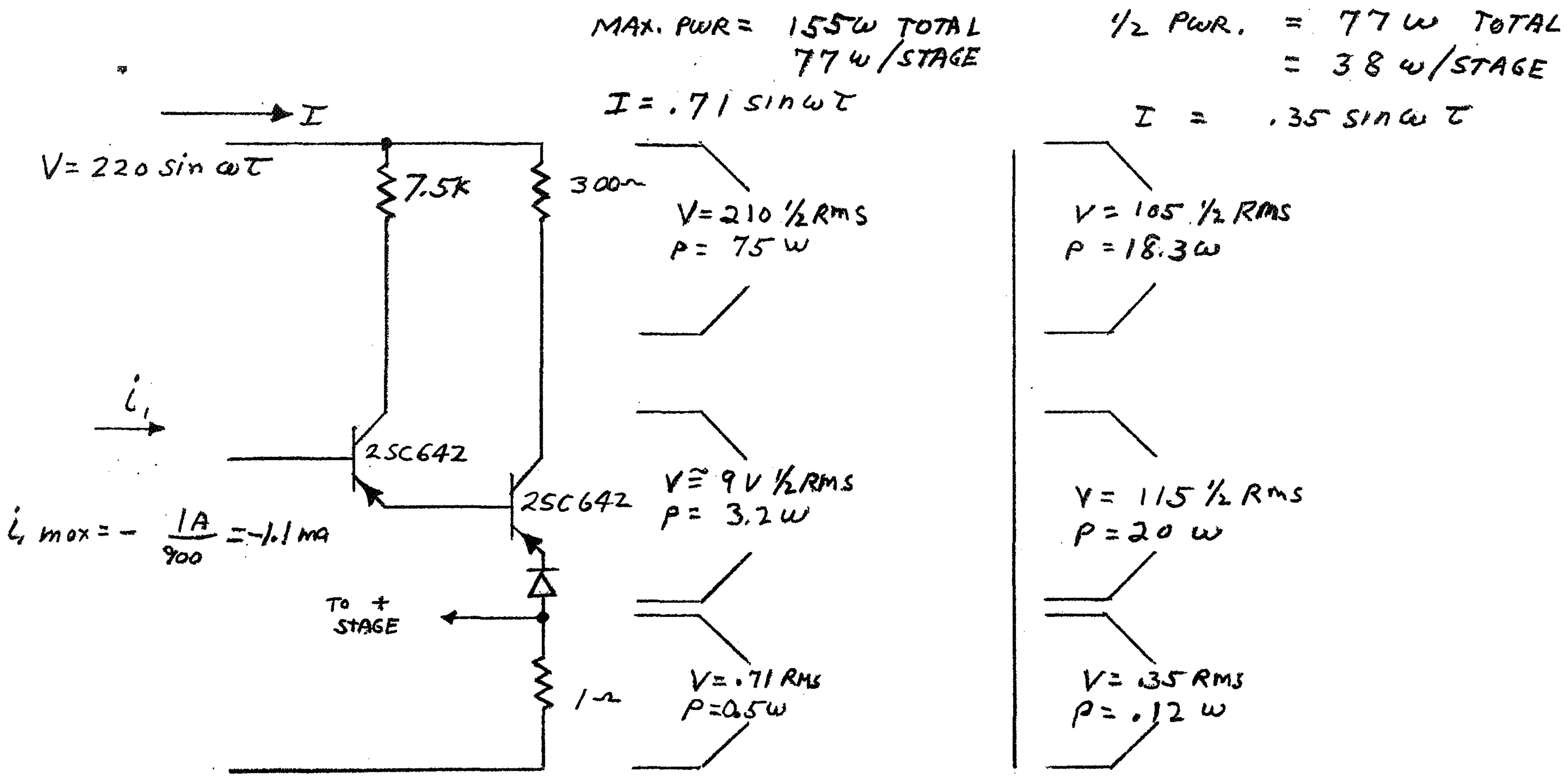


FIGURE 4-9 DC POWER STAGES IN PARALLEL



2SC642

I_c = 1A max.

P_c = 50 w max.

BV_{CEO} = 700 V

β = 30 min

β^2 = 900 min

NOTE:

Only negative stage shown because PNP power transistors are not available with I_c greater than 1 ampere, and V BV_{ceo} greater than 350 volts. This stage limits the capability of the AC simulator

FIGURE 4-10 AC POWER STAGE SCHEMATIC DIAGRAM AND ANALYSIS (NEGATIVE STAGE ONLY)

The resultant voltage and current data was processed to yield R(t). This R(t) was then converted from analog to digital form and stored in a small computer. Subsequently, the R(t) data was recovered from storage, processed into analog form, and applied to the control input of a resistance rotator. The resulting current response of the rotator duplicated (except for frequency) the response of the original load. The demonstration was carried out using available hardware. Accordingly, V(t)/i(t) was computed in real time by using an analog divider, and the rotator was one that used a relatively slow-response controlled source.

However, the results of the experiment clearly showed that the variable resistance technique is a feasible means of obtaining a dynamic load response.

A detailed report of this experiment is provided in Appendix F of the fifth monthly report.

In another experiment a current sink was assembled and its dynamic capabilities demonstrated by controlling the sink resistance with a square wave voltage. In this experiment a response of 50 KHz was achieved at a power level of over 100 watts.

Engineering reports of other laboratory investigations carried out during the study were included in the monthly reports.

4.1.2 Variable Reactance Elements

Reactance elements will be necessary for any simulation technique involving a network model (impedance). In order to permit changes in the model response, some means of varying the model component values must be included. As mentioned in the previous discussion, lumped components may be interconnected and switched in discrete steps. Of course this has the disadvantage that large volume and complex switching is required to achieve even a moderate dynamic range. Analog circuits were considered as means for realizing variable reactance elements and one such scheme is described briefly in the following discussion.

Figure 4-11 is a schematic diagram of an impedance multiplier circuit. If the operational amplifier is considered to be ideal, then the circuit voltage gain

$$AV = AV_1 \, AV_2$$

$$AV_1 = 1$$

$$AV = AV_2 = \frac{1-a}{a} = \frac{1}{a} - 1 \qquad \text{(Eq. 4.25)}$$

where

AV = magnitude of the circuit voltage gain

AV_1 = magnitude of the voltage gain of the first amplifier

AV_2 = magnitude of the voltage gain of the second amplifier

a = resistance ratio, in ohms, indicated in Figure 4-11.

The input current is given by

$$i_1 = c \, \frac{d(e_1 - e_2)}{dt} \qquad \text{(Eq. 4.26)}$$

where

c = the capacitance to be multiplied

e_1 = voltage between terminals 1 and 2

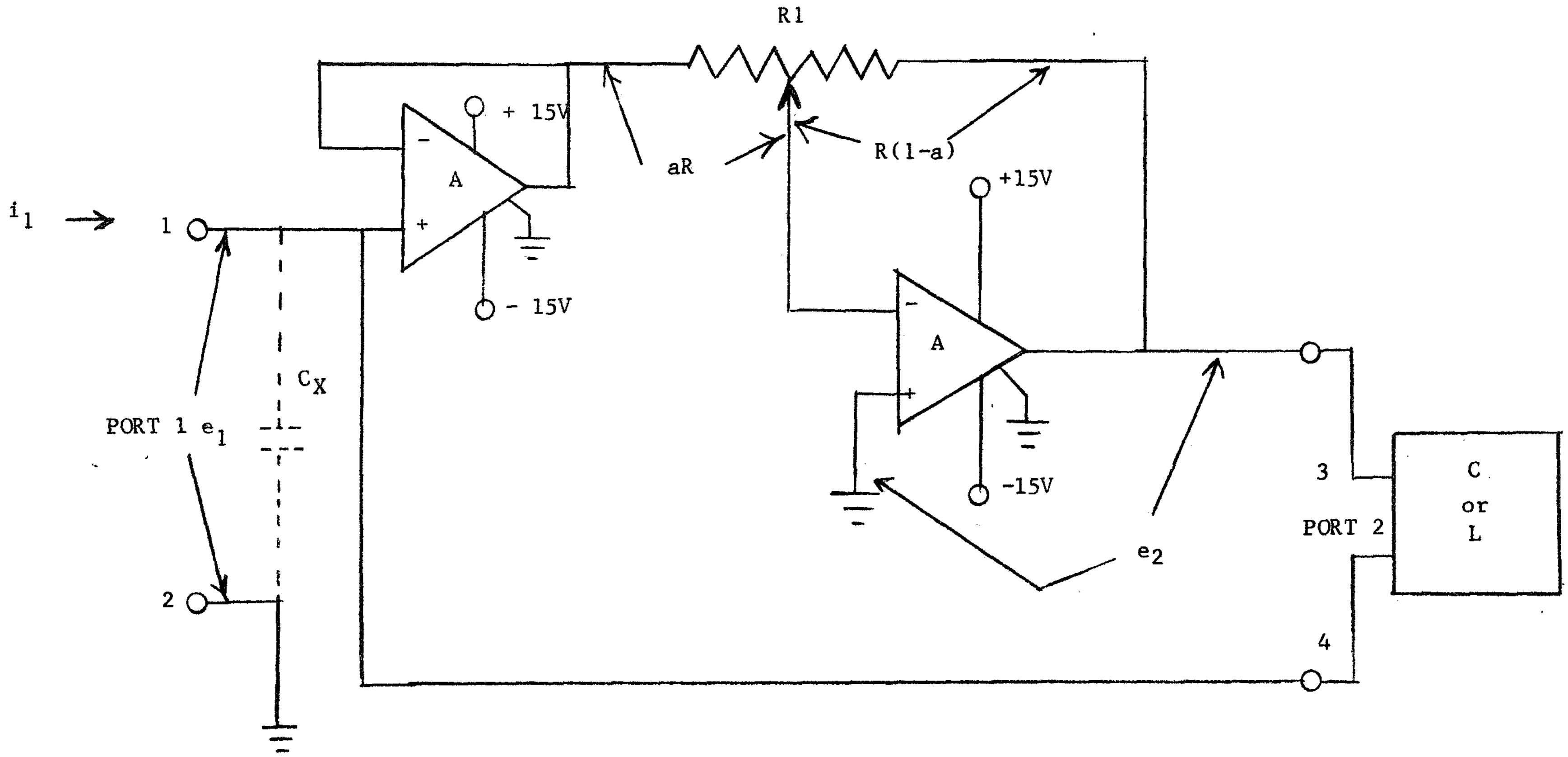
e_2 = voltage between terminals 3 and 2

The capacitance synthesized, is

$$c_x = \frac{i_1}{de_1/dt} \qquad \text{(Eq. 4.27)}$$

The output voltage, e_2, is given by

$$e_2 = -AV\,e_1 = -e_1\left(\frac{1}{a} - 1\right) \qquad \text{(Eq. 4.28)}$$



A = OPERATIONAL AMPLIFIER PHILBRICK MODEL P2

R = 500 K OHM 5 WATT POTENTIOMETER

FIGURE 4-11 IMPEDANCE MULTIPLIER CIRCUIT, SCHEMATIC DIAGRAM

Substituting Equation 4.26 into Equation 4.27 gives

$$c_x = \frac{c\,\dfrac{d\,(e_1 - e_2)}{dt}}{de_1/dt} \tag{Eq. 4.29}$$

Sustituting Equation 4.28 into Equation 4.29 gives

$$c_x = \frac{c}{a} \tag{Eq. 4.30}$$

Equation 4.30 indicates that the capacitance synthesized is equal to 1/a times the capacitance connected across port 2 of the circuit. Equation 4.26 indicates that current i_1 is a function of the difference between the input voltage e_1 and the output voltage e_2. Equation 4.27 shows that this current determines the amount of capacitance multiplication. Since the maximum output voltage is limited by the amplifier circuits, the largest capacitance multiplication that can be achieved in practice will be limited by the maximum input voltage to be applied to the circuit.

4.2 NETWORK MODELING

Practical electrical load simulators will include network models suitably adjusted to respond to voltage stimuli in a manner in which duplicates the real devices. Development of such models is a necessary step in the realization of electrical load simulators.

A first requirement is to specify what components can be used in the modeling. A second requirement is to define some criterion (or even a variety of criterions) that must be used to judge the degree of agreement between real devices and models. A third requirement is to indicate what types of driving signals are to be used.

4.2.1 Components

It is, of course, desirable to realize the simulator(s) as simply as possible. A lumped parameter model, with passive elements R, L, C, whose value can be changed in steps (by switching at appropriate moments) appears to be a desirable goal. The number of elements should be kept as low as possible. If some simple active components (such as buffer amplifiers) are allowed, the modeling process becomes easier. Hence, it may be desirable to allow amplifiers in the modeling. Continuously variable elements are rather complex and should be avoided whenever possible.

Experience has shown that the task of modeling is much easier when the designer knows something about the structure of his device and incorporates this *a priori* knowledge in his model. As an example, one can model an RC network also (exactly) by an RLC network (in the Darlington scheme), but at the cost of more elements and close coupling of inductances. Therefore, it seems reasonable to divide the devices in (at least) two major series. A first series consists of devices like motors, and solenoids, whose internal structure is known in some detail. Moreover, for some of these devices, such as the motors, a great deal of literature is available on modeling. The *a priori* knowledge of internal structure can generally be incorporated in the topology and choice of element-kind (R, L or C) of the model. The best fitting values of the parameters are determined by an automated search on the computer. Note also that the general models based on knowledge of internal structure may be too complicated for the present task (as may well be the case for the AC-motors) but they serve as a starting point for simplified models.

A second series consists of catch-all categories such as "electronics" which may contain a very large number of types of devices. Some specific devices, belonging to "electronics" can, of course, be modeled individually and thus belong to the first series, but the others are too numerous or of unknown structure to allow for individual modeling. A realistic approach for this series is to start with a few basic structures, containing a limited number of parameters, chosen for their flexibility in producing a good variety of responses. (see Section 4.4 for one scheme).

A search on the computer will then find the parameter values yielding the best fit, within the basic structures considered. Obviously, it may be difficult or even impossible to assign a direct physical interpretation of the components in the model in terms of the real device of the second series.

Generally speaking, one expects a better fit for the first series than for the second series. But, at least, one can find the best achievable match within the structures considered for the second series; it is up to the user to decide whether this best match is good enough. This point will be discussed more in connection with the choice of criterion, next.

4.2.2 Criterion of Fit

The choice of the criterion or criterions is very important, since it determines what type of approximation is used to judge the quality of the modeling. Some examples are given below. Figure 4-12 is used for reference.

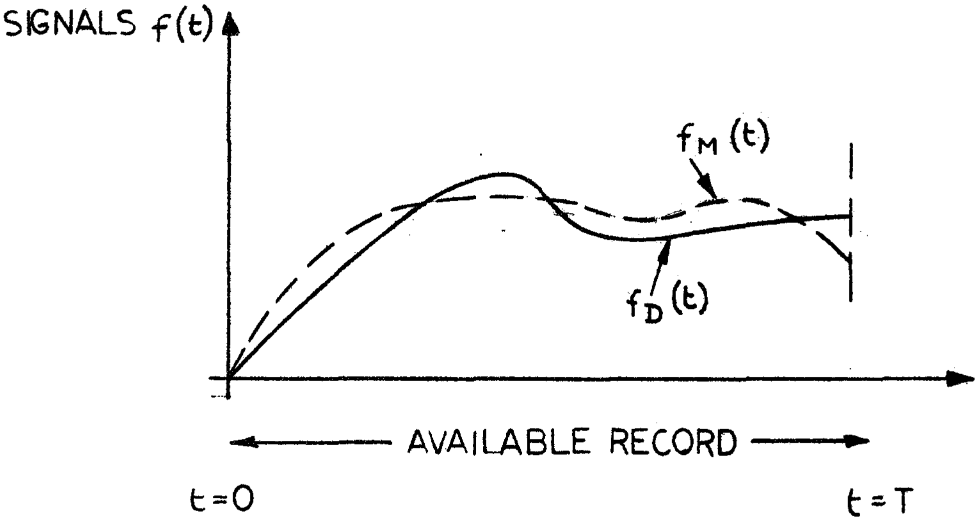


FIGURE 4-12 TRUE DEVICE RESPONSE AND MODEL RESPONSE

If the true device response is $f_D(t)$, and the model response is $f_M(t)$, then the instantaneous error can be defined as

$$e = f_M - f_D$$

where $0 \leq t \leq T$

Now, one can define the best model as that which minimizes (over the possible and allowed models)

1. $C_1 = \max |e(t)| \qquad 0 \leq t \leq T$ (peak error)
2. $C_2 = \left(\frac{1}{T} \int_0^T e^2 dt \right)^{1/2}$ (rms error)
3. $C_3 = \frac{1}{T} \int_0^T |e| \, dt$ (mean absolute error)

The Type C_1 may pose problems if narrow tolerances are demanded. It would appear that here an averaging type of criterion such as C_2, C_3 is more appropriate or, at least, easier to deal with than a point type criterion such as C_1. In fact, f(t) = power of the device, may be a good choice here (or else, f(t) is either current or voltage).

Since the measured signals on the real devices are time-functions and since the natural criterion of fit are also in the time domain, it is preferable to stay in the time-domain altogether and to avoid a detour in the frequency domain. Therefore, the computer program must be able to obtain dynamic responses in time, i.e., to compute $f_M(t)$ in terms of a given structure and given values of parameters (say, p_1, p_2,...p_n; where p_1 may be the numerical value given to a resistor, a capacitor or an inductor). Another important feature of the computer program is the automated search to locate the best values of $p_1 \ldots p_n$. It is known that search programs run into serious problems of time, convergence, efficiency, etc., for large numbers of parameters (i.e., large n); therefore, the number of allowable parameters must be kept low, say 10. Note that, because of limited accuracy of data on real devices, a relatively low order model may be theoretically best anyway.

A hybrid computer would probably be the best tool for the modeling, with time responses calculated by the analog elements and search logic handled by the digital part.

If one takes a sufficiently flexible set of basic structures (such as the ones chosen in Section 4.4.1, and if no limit is imposed on the number of parameters, then mathematical results show, at least theoretically, that criterions like C_2 and C_3 can be made arbitrarily close to zero, i.e., one can approximate to any desired degree according to C_2 and C_3 (except for unavoidable round-off and reading error). However, a very high degree of accuracy may require an impractically large number of parameters. If, on the other hand, an upper bound is imposed on the number of parameters, no general quantitative prediction can be made about the achievable accuracy.

4.2.3 Signals

The signals of interest are voltages and currents, in pairs, to give powers. One can consider two situations - either a device is basically a one-port, shown in Figure 4-13, and then it is described by its driving point characteristic.

$$F\,(v(t), i(t)) = 0$$

Or else it is a multi-port, say a two-port device (also shown on Figure 4-13).

Two-port modeling requires considerably more work and a more complicated synthesis (modeling) since it involves 4 (driving point or transfer) characteristics (3 if reciprocity exists), but reduces the total number of models when cascades of diodes are considered.

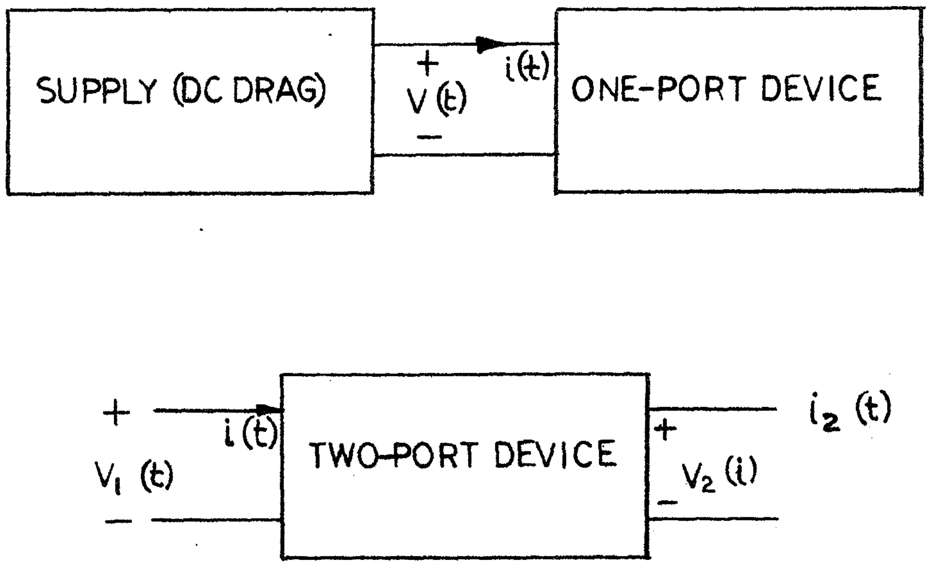


FIGURE 4-13 ONE- AND TWO-PORT DEVICES

4.3 COMPUTER OPTIMIZATION

4.3.1 Program Description

Network models can be made to provide responses quite similar to those of the real devices by suitable adjustment of the model component values. In order to permit the use of complex models (up to 20 model components) and to provide a consistent means of adjusting and evaluating the model parameters, a computer operation is indicated.

Avco Systems Division has developed and utilized optimization techniques for the selection of reentry vehicle designs and for the selection of decoy configurations whose trajectories matched the reentry vehicles trajectories within specified tolerances.

These applications have required the development of computer programs which optimize non-linear functions subject to non-linear constraints. Typically the degree of non-linearity and the actual behavior of the functions are relatively unknown.

These programs were adapted for use in the model optimization investigation of this study to permit gross assessment of feasibility.

4.3.1.1 Overall Program Organization

The major elements of the program are outlined in Figure 4-14. The input requirements are shown in the upper section, and the program itself is divided into analysis and synthesis modules.

The inputs to this program consist of an identification of the type of simulation network and starting values (initial guess) for the network parameters. The data describing the actual measured response of the equipment to be simulated is input. This is in the form of tables of the time histories of current and voltage. The criteria to be used to judge the adequacy of the simulation are identified by input qualities. Also any constraints on the calculated criterion values or on the allowable ranges of the design parameters are input.

The analysis module (1) calculates the transient behavior of the simulator network, and (2) calculates comparisons of the calculated response with the input data describing the response of the system to be simulated. This module is discussed in Section 4.4.1.2.

The synthesis module contains the logic and calculations required to search for values of the network parameters which will provide an acceptable or optimimum simulation of the original system. In an iterative process, the synthesis module organizes the relationships between the values of the network parameters being tried and the magnitudes of the criterions (mismatch) which result. From these relationships, new design values which will improve the simulation are selected and fed back to the analysis module. This process converges to the values of the network parameters which minimize the selected criterions. If the problem is overconstrained so that there is no acceptable simulation, the program will identify this result. The synthesis module is also discussed in Appendix B.

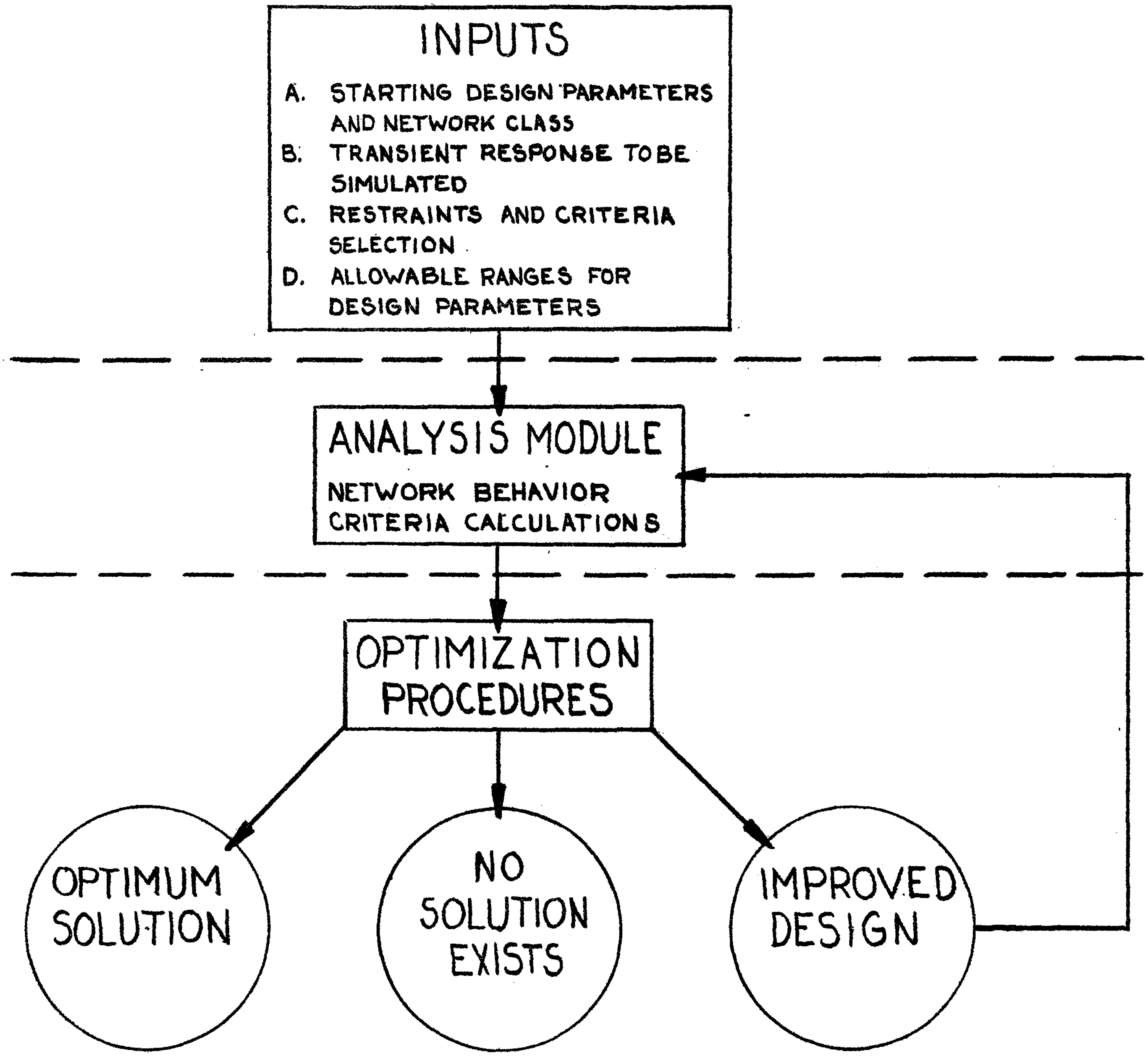


FIGURE 4-14 PROGRAM FOR DESIGNING OPTIMUM DYNAMIC LOAD SIMULATORS

Printouts are provided which summarize the various trials along the way to the optimum and detailed printouts are provided for the final network behavior. Machine plotting options are also provided in the program.

4.3.1.2 Analysis Module

An analysis module has been programmed to (1) calculate the transient behavior of electric networks, and (2) compare this calculated behiavior with the desired transient behavior which has been input. Options exist in the analysis module for calculating the behavior of various types of networks. A number of criterions are calculated as measures of the degree of simulation that has been achieved between the calculated response and the input response.

The analysis module has three basic building blocks:

1. A pure resistance, R_P (or conductance, γ_P), with admittance basis impulse-response

$$Y_p(t) = \gamma_p \, \delta(t) \qquad \gamma_p = 1/R_p \qquad \text{(Eq. 4.31)}$$

2. A series of resistance, R, and inductance, L, with admittance basis impulse-response

$$Y_R(t) = \delta \exp(-\rho t) \qquad \text{(Eq. 4.32)}$$

where

$\rho = R/L$
$\delta = 1/L$

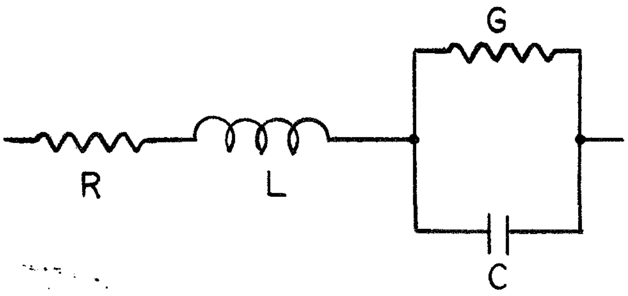
or

$R = \rho/\delta$
$L = 1/\delta$

This corresponds to a real root in the Laplace plane

$$Y(s) = \frac{1}{R + Ls} = \frac{\delta}{s + \rho}$$

3. The network below



$$Y(s) = \frac{\frac{1}{L}s + \frac{G}{LC}}{s^2 + \left(\frac{G}{C} + \frac{R}{L}\right)s + \left(\frac{1}{CL} + \frac{G}{C}\,\frac{R}{L}\right)}$$

with admittance basis impulse-response

$$y_c(t) = e^{-\sigma t}(\alpha \cos \omega t + \beta \sin \omega t) \quad \text{(Eq. 4.33)}$$

where

$$L = 1/\alpha \qquad R = \frac{\alpha\sigma - \beta\omega}{\alpha^2}$$

$$C = \frac{\alpha^3}{(\alpha^2+\beta^2)\omega^2} \qquad G = \frac{\alpha^2(\alpha\sigma+\beta\omega)}{(\alpha^2+\beta^2)\omega^2}$$

or, inversely,

$$\alpha = 1/L \qquad \sigma = \frac{1}{2}\left(\frac{G}{C}+\frac{R}{L}\right)$$

$$\omega^2 = \frac{1}{CL} - \frac{1}{4}\left(\frac{G}{C}-\frac{R}{L}\right)^2$$

$$\beta = \frac{\frac{1}{2L}\left(\frac{G}{C}-\frac{R}{L}\right)}{\sqrt{\frac{1}{CL}-\frac{1}{4}\left(\frac{G}{C}-\frac{R}{L}\right)^2}}$$

This corresponds with a pair of complex roots if

$$\left(\frac{G}{C}-\frac{R}{L}\right)^2 < \frac{4}{CL}$$

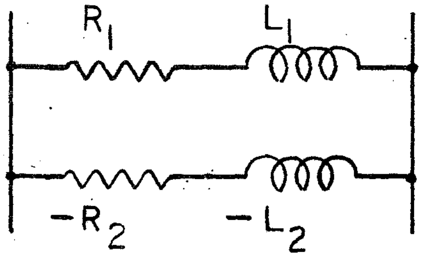
$$Y(s) = \frac{1}{2}\,\frac{\alpha+i\beta}{s+\sigma+i\omega} + \frac{1}{2}\,\frac{\alpha-i\beta}{s+\sigma-i\omega}$$

$$Y(s) = \frac{\alpha s + (\alpha\sigma+\beta\omega)}{s^2+2\sigma s+(\sigma^2+\omega^2)}$$

provided

$$\left(\frac{G}{C}-\frac{R}{L}\right)^2 < \frac{4}{CL}$$

Otherwise, one finds a pair of real roots, which can also be produced by the network shown below.



$$Y(t) = \frac{1}{L_1} \exp\left(-\frac{R_1}{L_1} t\right) - \frac{1}{L_2} \exp\left(-\frac{R_2}{L_2}\right) t$$

with

$$Y(s) = \frac{\left(\frac{1}{L_1} - \frac{1}{L_2}\right) s + \frac{R_2 - R_1}{L_1 L_2}}{s^2 + \left(\frac{R_1}{L_1} + \frac{R_2}{L_2}\right) s + \frac{R_1}{L_1} \frac{R_2}{L_2}}$$

The network can be realized as a passive circuit, when

$$R_1, L_1 > 0 , \quad R_2, L_2 < 0$$

or

$$R_2 , L_2 > 0$$

and, moreover,

$$\frac{L_1}{L_2} < 1 , \quad \frac{R_1}{R_2} < 1 , \quad \frac{R_1}{R_2} > \left(\frac{L_1}{L_2}\right)^2$$

Then, one finds that

$$L = \frac{L_1 L_2}{L_2 - L_1}$$

$$\frac{R}{L} = \frac{\left(\frac{R_1}{L_1}\right) L_2 - \left(\frac{R_2}{L_2}\right) L_1}{L_2 - L_1}$$

$$\frac{G}{C} = \frac{R_2 - R_1}{L_2 - L_1}$$

$$\frac{1}{LC} = \frac{\left(\frac{R_1}{L_1} - \frac{R_2}{L_2}\right)^2 L_1 L_2}{(L_2 - L_1)^2}$$

In each case, the program calculates the currents for given voltages by a discretized version of the superposition integral

$$i(t)=\int_0^t V(u)\, y(t-u)\, du$$

4.3.1.3 Criterions Available in the Program

Eight criterions are now available. Let $V(t)$ be voltage, $i(t)$ experimental current, and $i_a(t)$ approximate current for model. Then, one has for an observation interval

$$J_1 = \frac{1}{T}\int_0^T \left| i(t) - i_a(t) \right| dt$$

$$J_2 = \frac{1}{T}\int_0^T \left| \left(i(t) - i_a(t) \right) V(t) \right| dt$$

$$JC_1 = \max_{0 \le t \le T} \left| i(t) - i_a(t) \right|$$

$$JC_2 = \max_{0 \le t \le T} \left| \left(i(t) - i_a(t) \right) V(t) \right|$$

$$JS_1 = \frac{1}{T}\int_0^T \left(i(t) - i_a(t) \right)^2 dt$$

$$JS_2 = \frac{1}{T}\int_0^T \left(i(t) - i_a(t) \right)^2 \left(V(t) \right)^2 dt$$

$$JD_1 = \frac{1}{T}\int_0^T \left(\frac{di}{dt} - \frac{di_a}{dt} \right)^2 dt$$

$$JD_2 = \frac{1}{T}\int_0^T \left(\frac{dVi}{dt} - \frac{dVi_a}{dt} \right)^2 dt$$

Criterions with subscript w are similar to the corresponding ones with subscript 1. The former are based on power (current times voltage), the latter are using current only (for a given voltage input). The criteria J_1, JS_1, and JD_1 are all of the averaging type and deal with absolute error, error-squared, and first derivative error-squared, respectively. They are continuous and quite smooth with respect to the search parameters, meaning that a small change in some parameters will produce a small change in criterion value. Such criterions can be handled by the present search schemes (Rosenbrock or Davidon).

The criterion JC_1, on the other hand, is a local point criterion (maximum absolute error) and is not as smooth with respect to the search parameters. Therefore, more problems of convergence of search can be expected when JC_1 is used.

From results of network synthesis, it can be expected that the criterion surfaces may well have several local minima. This complicates the search and may require a variety of starting guesses to obtain the global minimum.

These criterions may be summed with relative weighing factors to produce combined figures of merit for network simulation. The various criterions may also be constrained, if desired, during the optimization process. These concepts are discussed more fully in Appendix B. These criterion calculation results may be selected to become the y_1 or y_i quantities discussed in that appendix.

4.3.2 Experimental Results

In order to demonstrate the adapted optimization program on real hardware problems, interrogations were made of a number of electrical and electronic devices available in the laboratory. A laboratory report on this load data is provided in Appendix C of the Fifth Monthly Report. The interrogation consisted of stimulating the device by application of the device's normal operating voltage and photographing an oscilloscope display of the resulting current into the device.

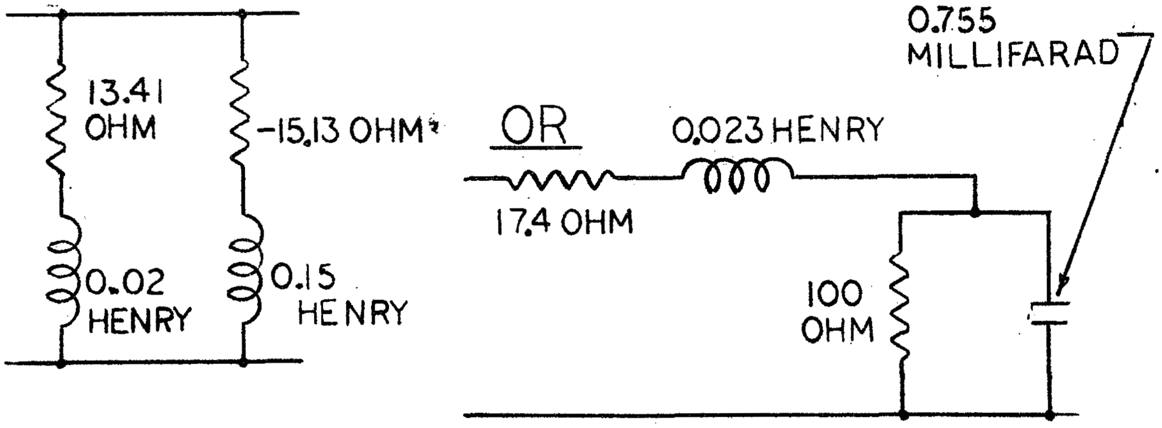
Several of these loads were then selected for use in demonstrating the computer programs. The current response along with the input voltage data was used by the computer as interrogation inputs.

The following discussion describes these experiments. In the computer graphs, circles denote experimental points while full lines indicate the approximation.

4.3.2.1 Example One: DC Motor

The step response is shown in Figure 4-15. Criterion J_1 was used here.

The corresponding network realization is shown below.



with admittance

$$Y(s) = \frac{43.3\,s + 573.3}{s^2 + 771.4\,s + 67631}$$

These results are very close to those obtained on the analog computer.

4.3.2.2 Example Two: DC Solenoid

The response in current to a step-input in voltage is shown in Figure 4-16. The time history can be divided into two parts. In Phase I the solenoid slug moves, providing a variable inductance. In Phase II, the slug having reached the end of its travel, the inductance is constant.

Therefore, it is not surprising that a really good fit cannot be obtained by means of a single linear (passive) constant parameter network covering both phases, if only a small number (e.g., six) of elements is allowed. (Note the sharp Vee between the phases, which is hard to simulate). One of the best obtainable results is shown in Figure 4-17. It uses the network shown below with six elements.

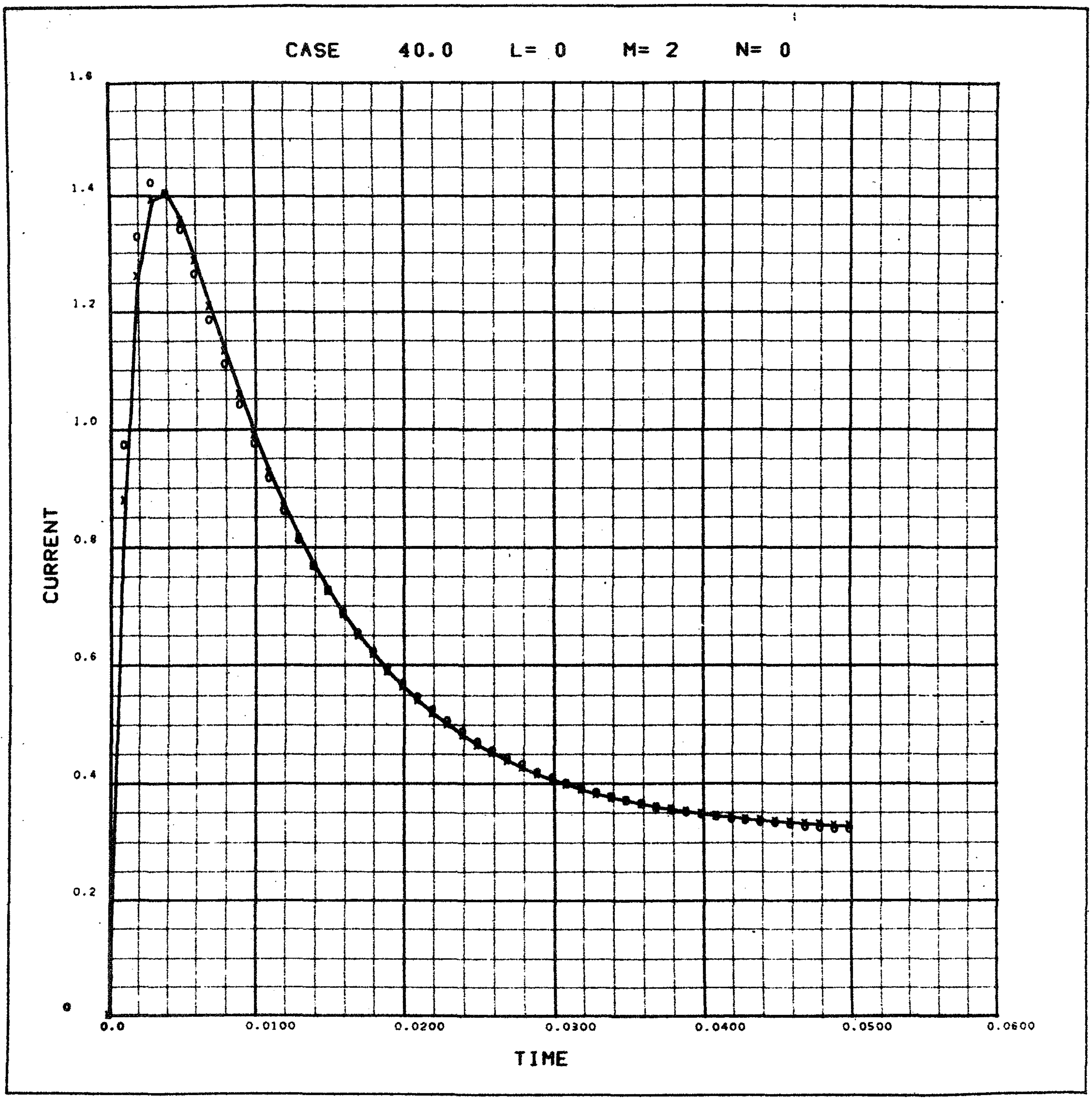


FIGURE 4-15 DC MOTOR, STEP RESPONSE

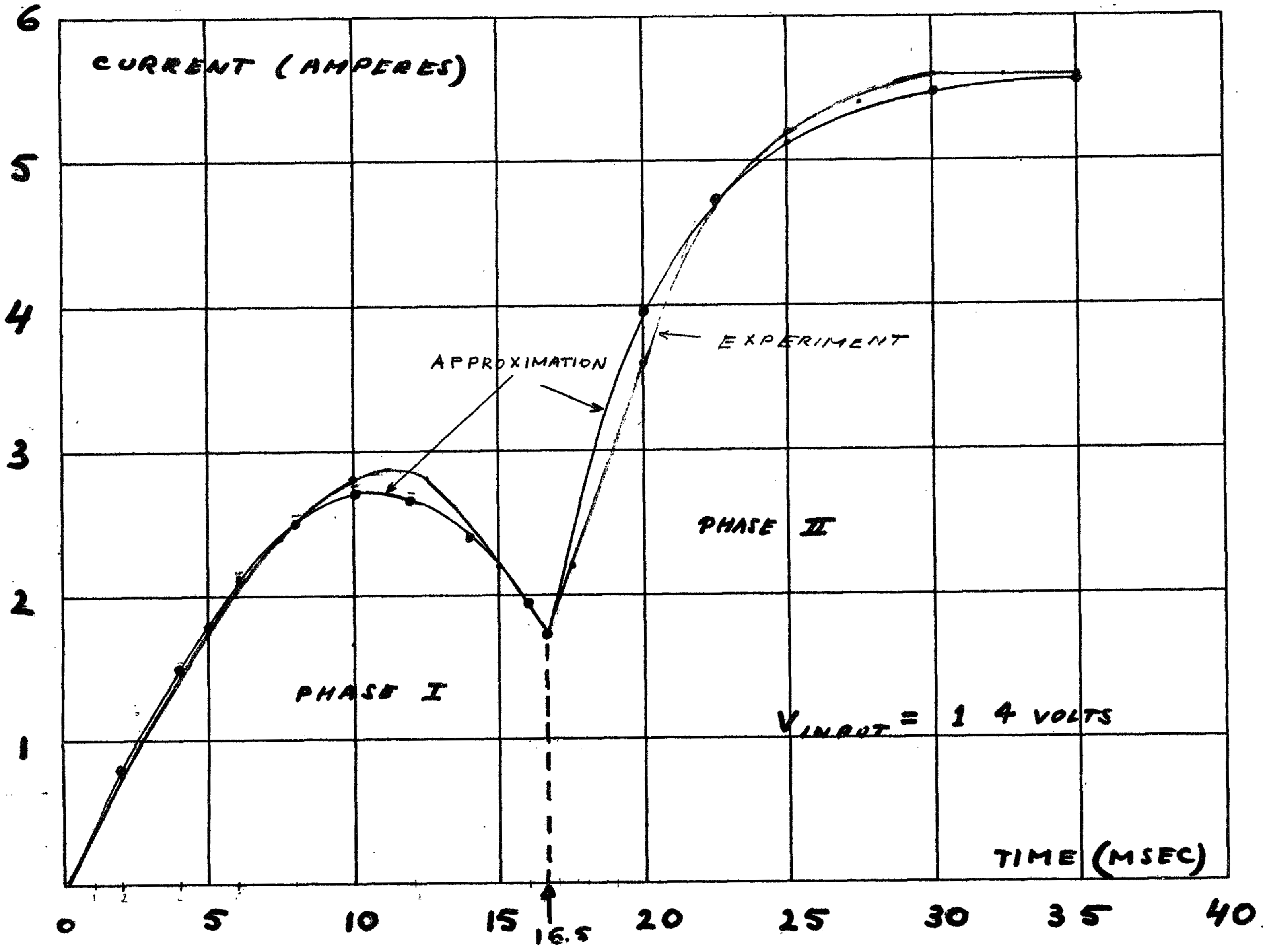


FIGURE 4-16 DC SOLENOID, STEP RESPONSE

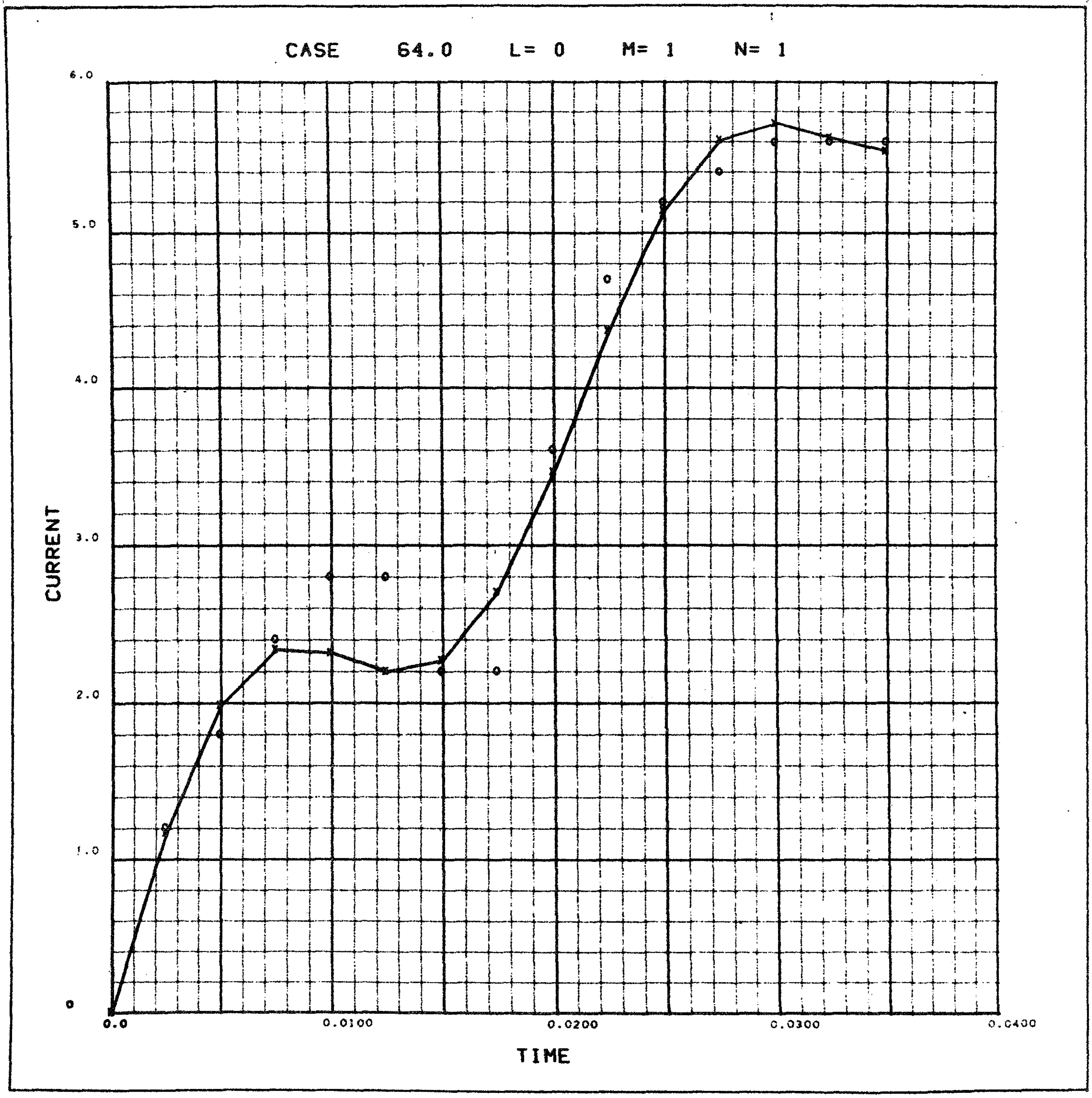
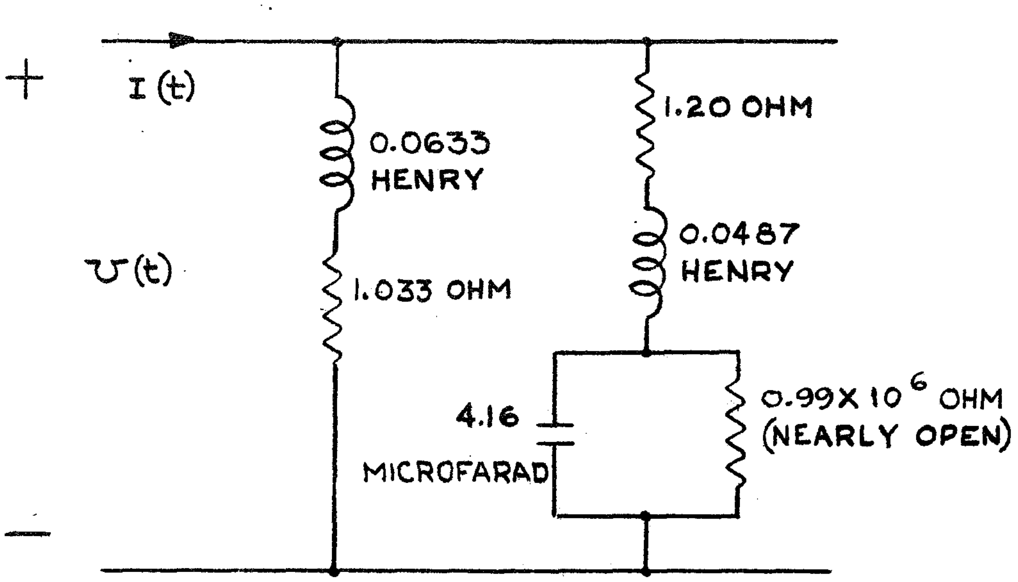


FIGURE 4-17 DC SOLENOID, RESPONSE SIMULATION



These values were obtained using the slope criterion, JD_1. Similar results were obtained by use of the criterion J_1. Better results can be obtained with a (still simple) model based on the physics of the events. One has two models, one for each phase, taken as linear passive systems for simplicity.

Phase I

One has

$$V = RI + L_w \frac{dI}{dt} + E_s \qquad \text{(Eq. 4.34)}$$

where

V = voltage of source

I = current from source

R, L = resistance and inductance of wiring

E_s = back-emf of solenoid

Further, if x denotes the motion of the slug (initially, $x(0) = \dot{x}(0) = 0$)

$$E_s = \frac{d}{dt}\left(L_s(x)\,I\right) = L_s(x)\frac{dI}{dt} + I\frac{dL_s(x)}{dt}$$

$$= L_s(x)\frac{dI}{dt} + I\frac{dL_s(x)}{dx}\,\frac{dx}{dt} \qquad \text{(Eq. 4.35)}$$

Slug motion (m = mass, f = friction coefficient)

$$m = \frac{d^2x}{dt^2} + f\frac{dx}{dt} = k(I) \qquad \text{(Eq. 4.36)}$$

Assuming a force-law, $k(I)$

$$\left[k(0) = 0\right],\ k(I) \approx k_I I$$

After linearization, one finds

$$V = RI + L_W\frac{dI}{dt} + \left(L_s(x)\right)_{aver}\frac{dI}{dt} + \left(I\frac{dL_s(x)}{dx}k_I\right)_{aver}\left(\frac{1}{f + m\,{}^{d}/_{dt}}\right)I$$

Using S as the Laplace operator, one now has

$$V = \left(R + L_1 S + \left(\frac{1}{CS + G}\right)\right)I$$

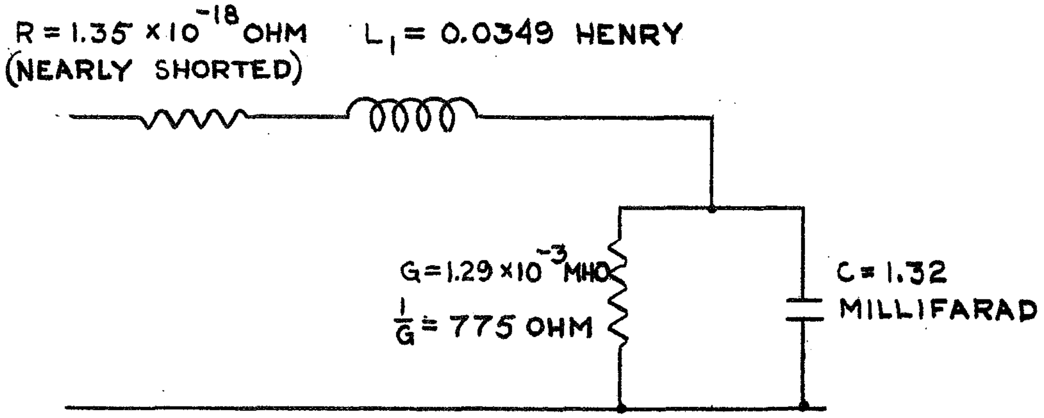
where

$$L_1 = L_w + \left(L_s(x)\right)_{aver}$$

$$C = \frac{m}{\left(I\frac{dL_s(x)}{dx}k_I\right)_{aver}}$$

$$G = \frac{f}{\left(I \frac{d L_s(x)}{dx} k_I \right)_{aver}}$$

The corresponding network, shown below, is well known.



A good approximation is shown in Figure 4-16. This corresponds with values of elements as indicated above. These values were obtained by criterion J_1. Very similar results were obtained with criterion JD_1.

Phase II

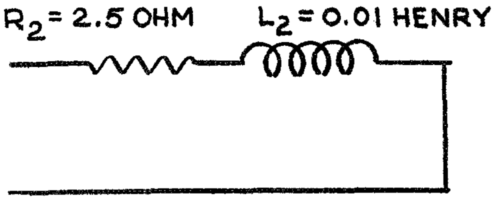
If one has $x \equiv$ constant $= x_{final}$

$$V = R_2 I + L_w \frac{dI}{dt} + L_s(x_{final}) \frac{dI}{dt}$$

$$= R_2 I + L_2 \frac{dI}{dt}$$

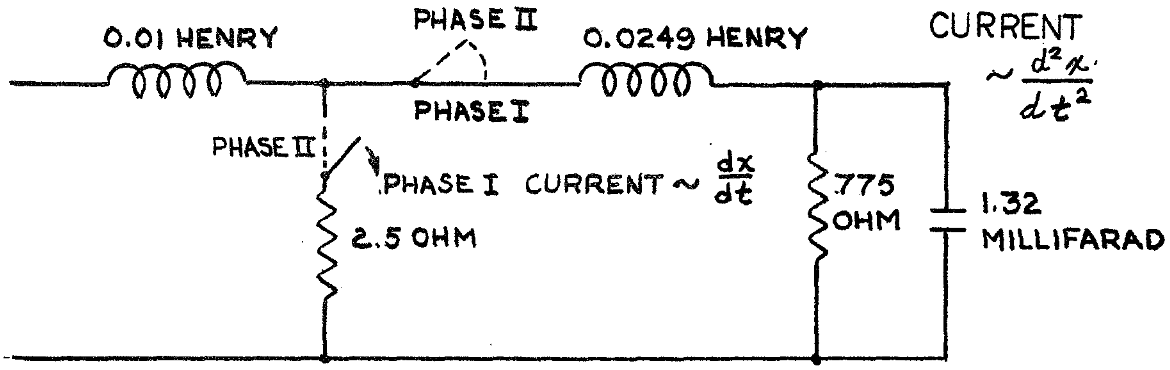
if $\quad L_2 = L_w + L_s(x_{final})$

The numerical values shown in the network below give the good fit shown in Figure 4-16.



(time constant = 4 msec)

The two phases can be combined into one model--the model shown below.



The closing of the switch depends on x, with closing time, t_s, given by

$$x = x_{final}$$

This law can be mechanized in the model.

4.3.2.3 Example Three: Amplifiers

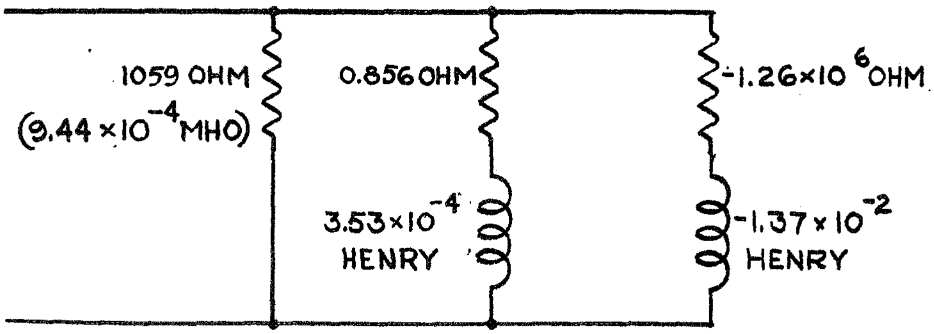
This is an AC situation, with input voltage

$$V(t) = 75 \sin (2\pi 60 t + \gamma)$$

with

$$\gamma = -11.5°$$

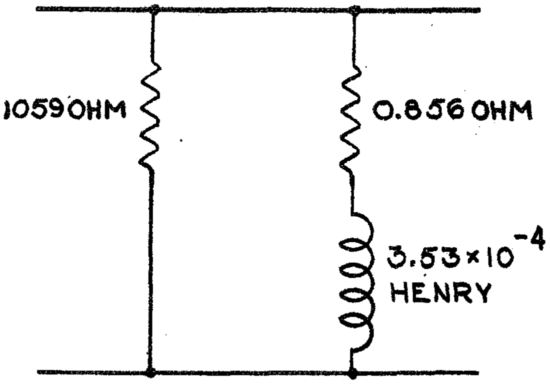
The following simple network, based on optimization by means of criterion J_1, was found by the computer.



This network is not passive, since

$$\frac{R_1}{R_2} < \left(\frac{L_1}{L_2}\right)^2$$

but is very similar in behavior to the passive network shown below. The latter was obtained by omitting the negative elements (with very high impedance).



The computer plot is shown in Figure 4-18.

4.3.2.3 Example Four: AC Solenoid

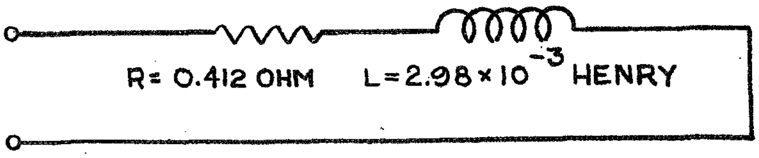
This is, again, an AC case. The input voltage is

$$V(t) = -75 \sin (2\pi 60t + \gamma)$$

with

$$\gamma = 31^\circ 20'$$

The following simple passive network



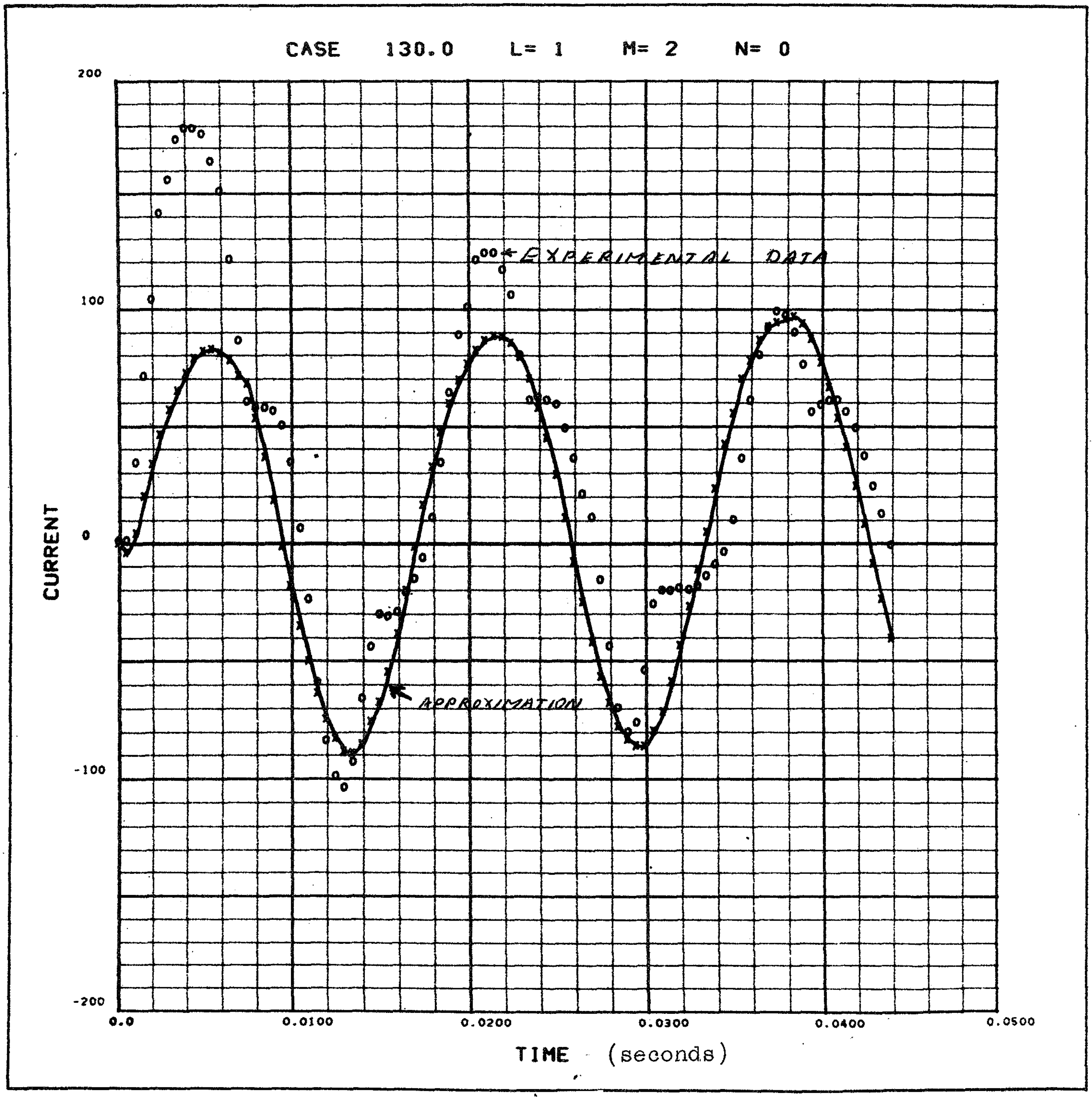
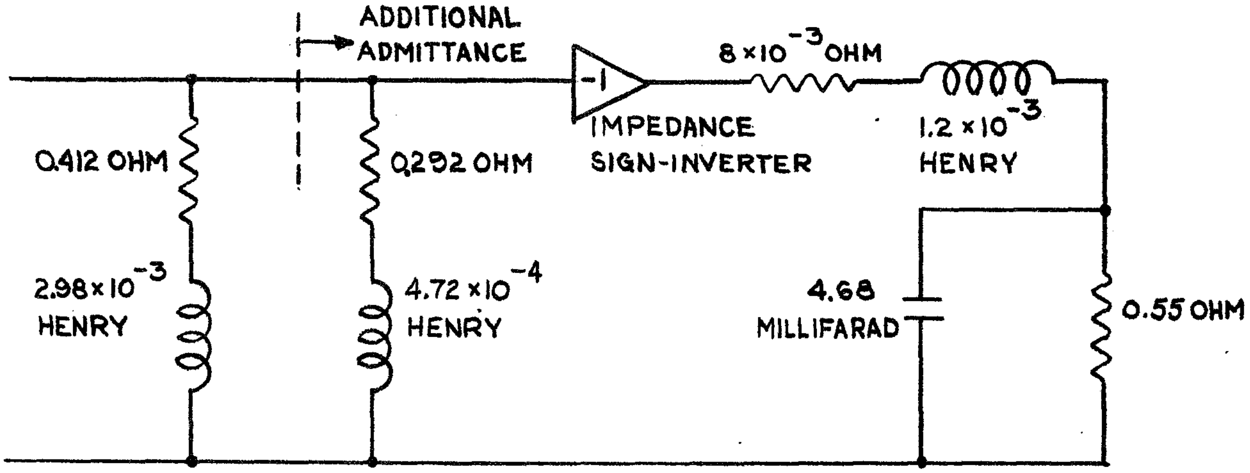


FIGURE 4-18 AC AMPLIFIER, COMPUTED AND EXPERIMENTAL DATA

gave the results shown in Figure 4-19. The steady-state phase shift and admittance magnitude are modelled very well, but the initial current peak is not well simulated. This initial high current is probably due to some non-linear effect (such as a resistance change caused by heating) and attempts to add passive networks to account for the current transient did not work out well (note that here one tries to simulate non-linearities, which are not necessarily sensitive to the phase of switch-on with respect to the voltage sine wave, by means of linear networks which are indeed sensitive to such phase relationships).

If linear active networks are allowed, such as the one shown below, (requiring amplifiers or other active elements), good simulation can be obtained as shown in Figure 4-20.



The steady-state response is the same as in Figure 4-19 (after 20 msec). The additional network has the admittance

$$1.77\left[\frac{377}{(s+200)^2+(377)^2}\right]\left[\frac{s^2+(377)^2}{0.52\,s+322}\right]$$

$$=\frac{2121}{s+619}-\frac{837\,s+329174}{(s+200)^2+(377)^2}$$

One has to check if this admittance is positive real to find out whether a passive realization (of course, as a different structure) is possible.

The result of a numerical check is that the admittance is not positive real and, hence, not realizable as a purely passive network.

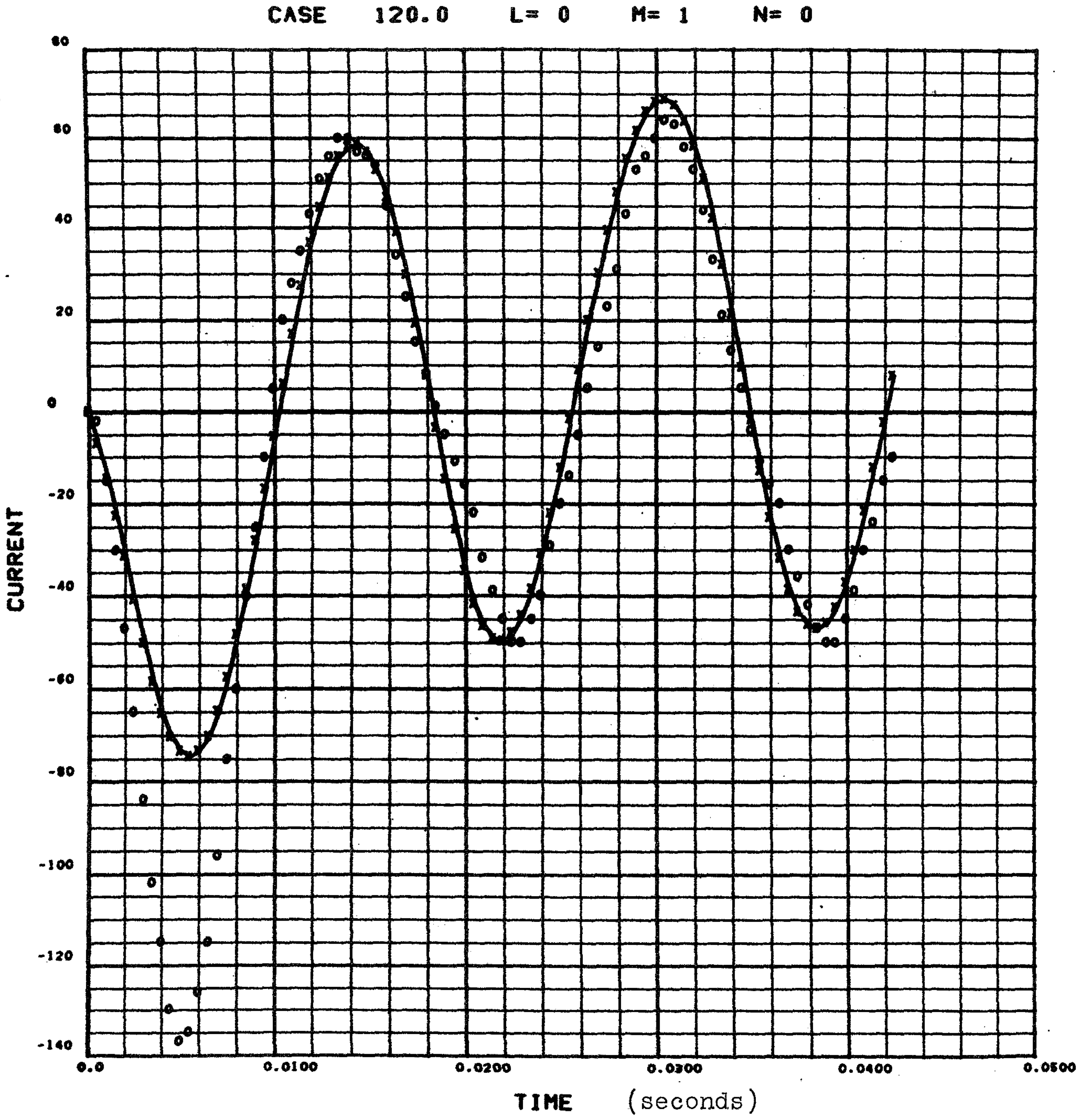


FIGURE 4-19 AC SOLENOID, RESPONSE SIMULATION, PASSIVE NETWORK

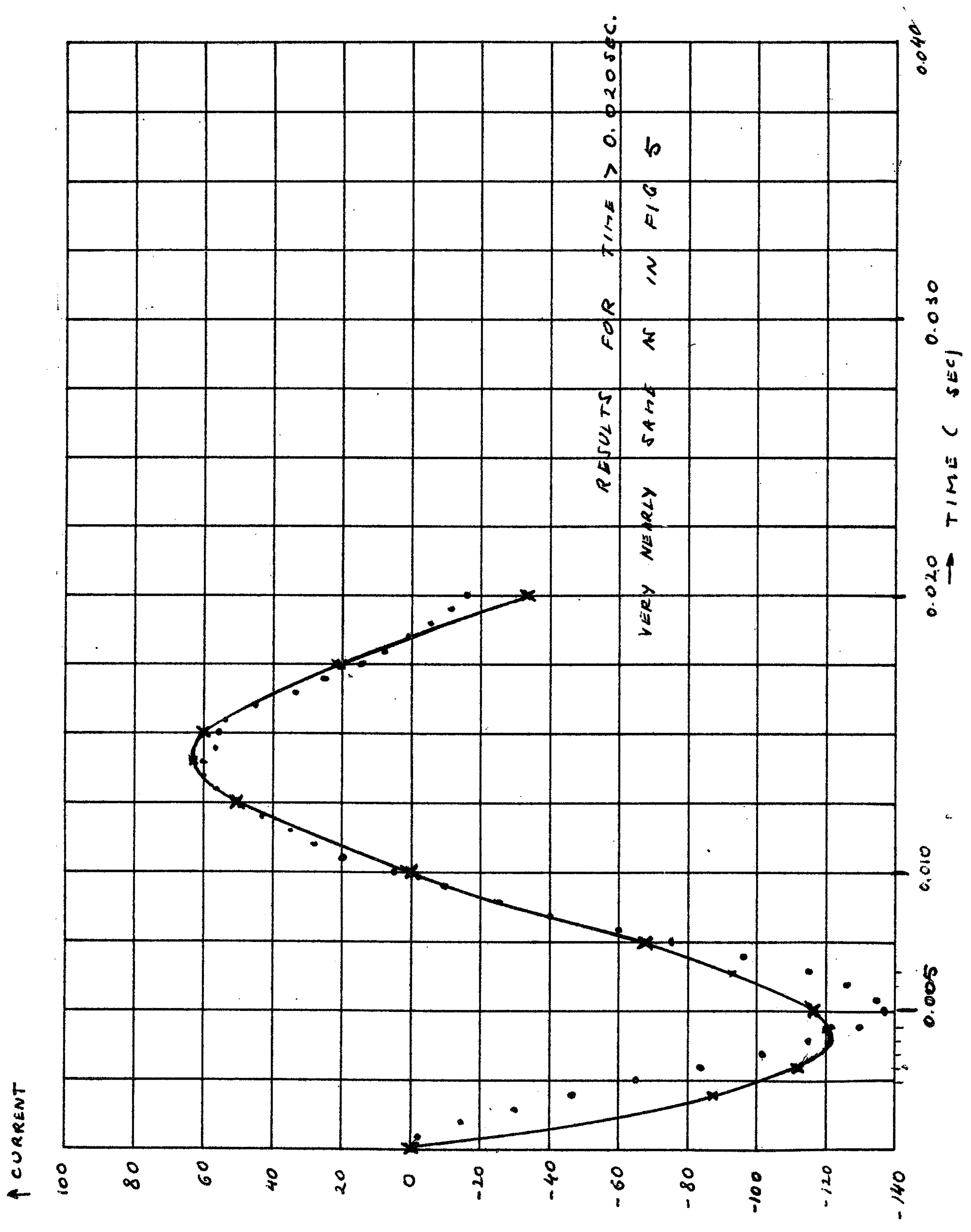


FIGURE 4-20 AC SOLENOID, RESPONSE SIMULATION, LINEAR ACTIVE NETWORK

5. INTERROGATION AND SIMULATION SYSTEM CONCEPT

Up to this point, the study has defined requirements and described techniques for implementing an interrogation and simulation process to be used in characterizing and simulating the dynamic and steady-state electrical loads of manned spacecraft equipment.

This section describes a total system approach which will draw upon those techniques to satisfy the overall requirements.

Table 5-1 is a summary of the baseline system requirements derived from the earlier summary of load parameter range estimates and from estimates of customer needs.

The interrogation/simulation process begins with identification of the driving point immitance of a specific electrical load and ends with the accurate simulation of that immitance by a device at voltage and current levels which are not scaled from the real levels. Further, the simulator has a flexibility which provides for varying simulator operation to accommodate a range of response characteristics.

The interrogation/simulation process can be characterized by the sequence of events listed below and shown schematically in flow diagram form in Figure 5-1.

1. The load to be simulated is identified.
2. The load category and stimulation data are determined.
3. An interrogation method designed to yield the device response for all modes of operation is selected.
4. The load is interrogated.
5. The interrogation data is processed to identify the impedance-time history of the load for each mode of operation.
6. A simulator capable of being programmed to provide this variable impedance is selected.
7. A simulator program is generated.
8. The simulator program is entered in the simulator.
9. The simulator is connected to the system under test.

5.1 INTERROGATION

5.1.1 General Description

The interrogator is shown schematically in general form in Figure 5-2. The methods by which each of the elements of Figure 5-2 will be implemented are discussed below:

TABLE 5-1

INTERROGATOR/SIMULATOR BASELINE SYSTEM REQUIREMENTS.

Voltage	0 to 200 VDC
	0 to 220 VAC (400 Hz, 1 or 3 phase)
Current	
Steady-state	0 to 20 Amps DC
	0 to 10 Amps AC
Dynamic	0 to 500 Amps DC
	0 to 200 Amps AC
Power	0 to 400 watts, typical
	(to 6 kilowatts for motors and 30 kilowatts for electrolysis)
Frequency Response	DC to 10 KHz for AC loads
	DC to 1 KHz for DC loads
Dynamic Operation	
Range	40 dB
Behavior	Periodic*
Duration of Dynamic Operation During Any Period	0.1 second, maximum
System Application	
Quantity of Simulators in Simultaneous Use	30, maximum
Duration of Total Operation Per Use	1 hour, maximum
Duration of Interrogation Interval	1 minute, maximum

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* Synchronous with excitation frequency for AC loads.

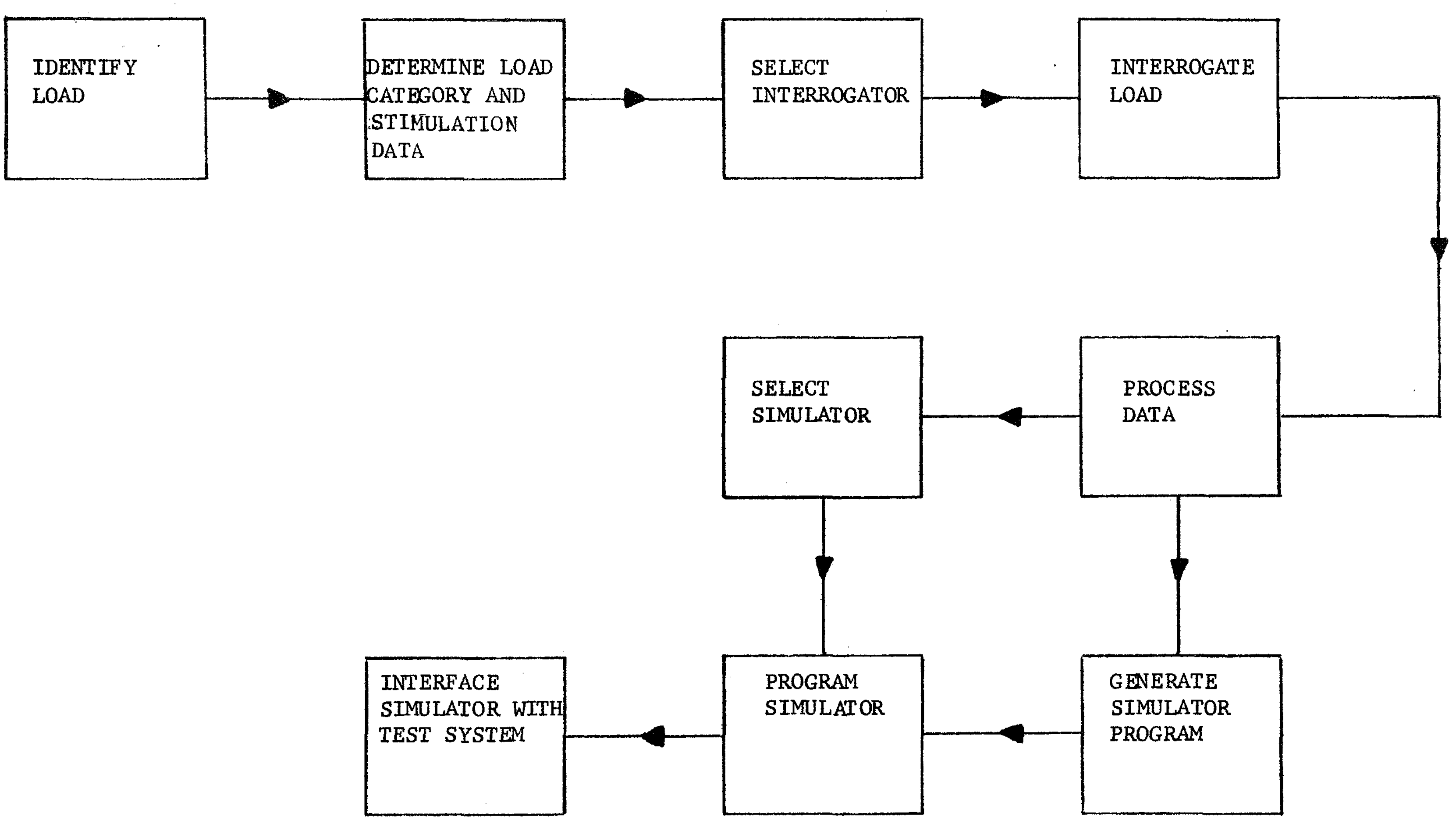


FIGURE 5-1 INTERROGATION/SIMULATION PROCESS FLOW DIAGRAM

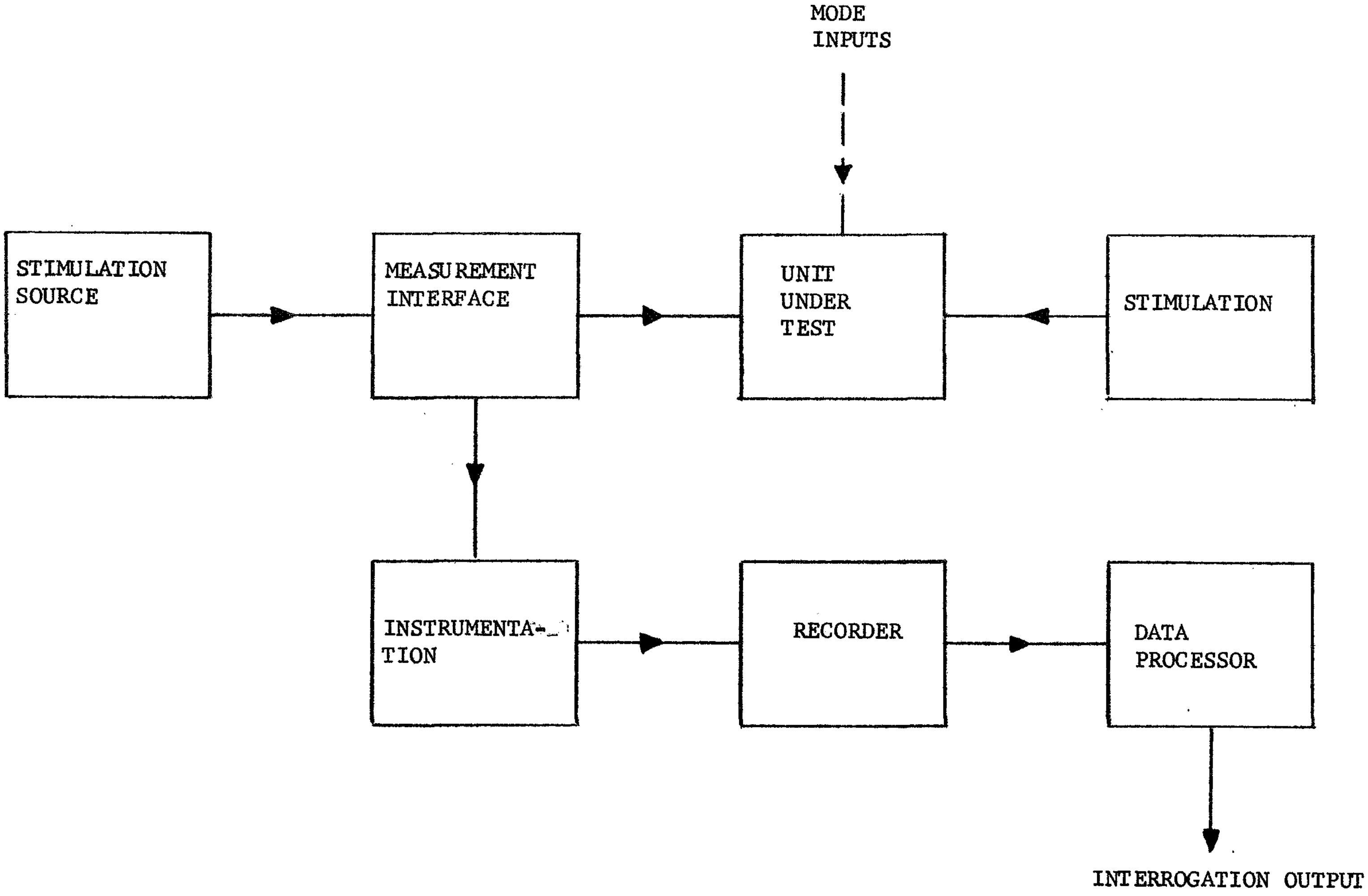


FIGURE 5-2 SIMPLIFIED BLOCK DIAGRAM OF LOAD INTERROGATOR

I. Stimulation Source - The stimulation source provides a voltage whose amplitude and frequency are within the specified nominal operating range of the unit under test (UUT). The source resistance will approximate that of the real source.

The source will be either DC or AC (single or three phase) and will be applied to the UUT as a step, using a fast-rise-time switching element.

II. Measurement Interface - The measurement interface can be an adapter cable in a "T" configuration. The three extensions of this cable interface with:

1. The interrogation source
2. The UUT
3. The instrumentation

The cable provides a breakout for each interface wire for voltage measurements. A conventional meter shunt installed in each power return lead permits current measurements.

III. Instrumentation - All voltage and current data is recorded in real time using an instrumentation quality tape recorder operating in the FM mode. Absolute values of voltage and current are determined by comparing the acquired data with calibration signals recorded on each recorder track prior to recording the interrogation data. A time signal (such as one of the Inter-Range Instrumentation Group, IRIG, codes) recorded on a separate track simultaneously with the interrogation data provides an accurate time base and facilitates tape editing and cueing.

IV. Stimulation - Other stimulations of the UUT which will produce a response on the power lines are also provided during the interrogation process. These might be temperature, load variations, signal inputs, etc. The specific stimulation to be included and the coincidence of these stimuli will be determined by the user on the basis of simulator application requirements and UUT specifications.

The user must make a similar decision specifying UUT operating modes of interest.

V. Data Processor - At this point in the process input voltage and current data associated with each mode of operation and stimulation of the UUT has been acquired and recorded in analog form. A data processing method designed to yield the simulator programming information is shown schematically in Figure 5-3. The analog data is first sampled at 1 millisecond intervals and stored on digital tape.

All processing is accomplished using digital techniques. However, if a different format is desired, the original analog tape (master) can be used to generate a new tape. The process is programmed into a computer (a small general-purpose computer is suitable) and all operations are automated. The data is processed to yield two items of information.

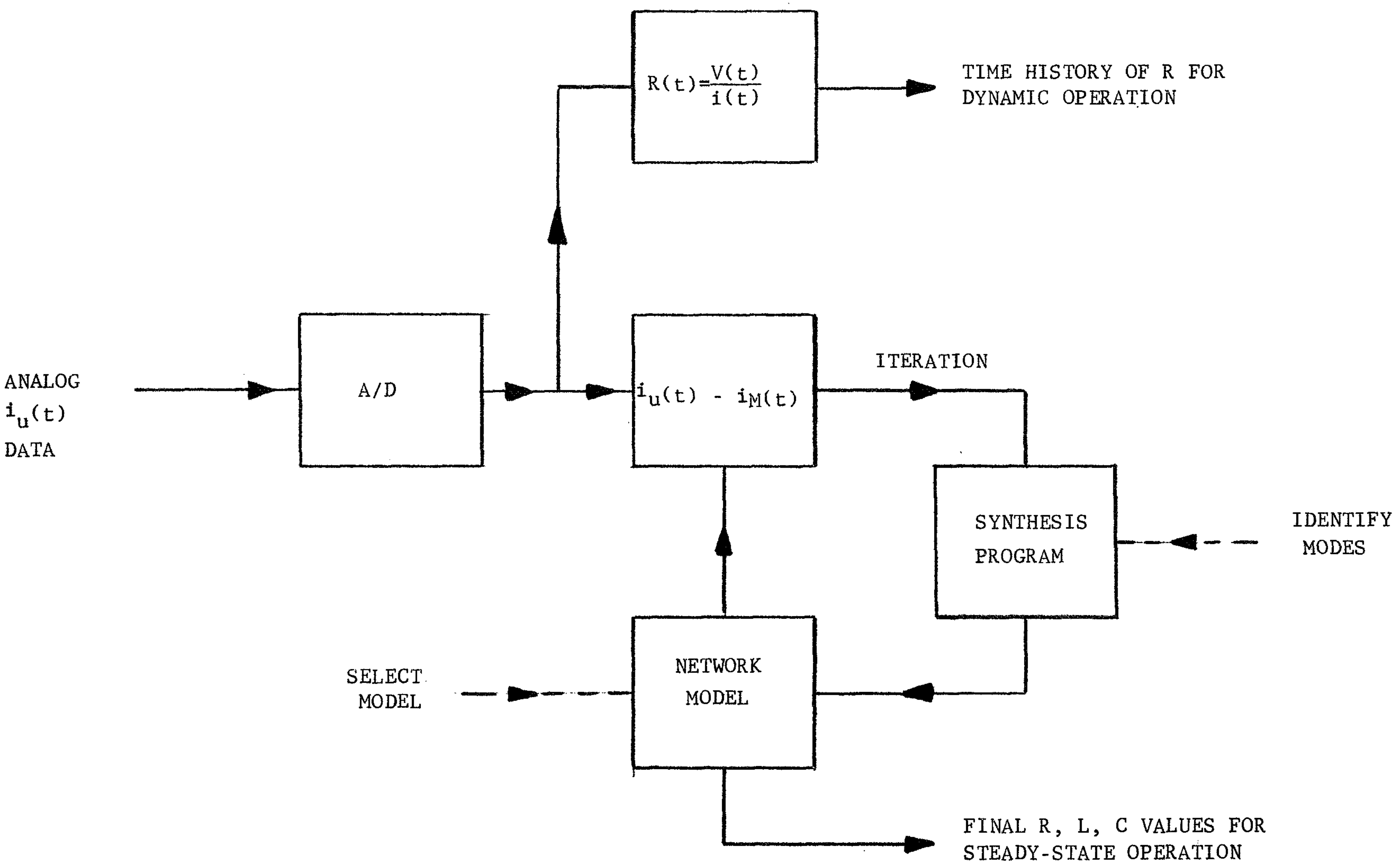


FIGURE 5-3 INTERROGATION PROCESS FOR OBTAINING STEADY-STATE AND DYNAMIC HISTORY

1. The specific R, L, C values in a given network configuration to provide the turn-on, turn-off, and steady-state (TO/TO/SS) response of the UUT.

2. The resistance/time history to provide the dynamic response of the UUT.

See Figure 5-4 for an illustration of the turn-on, turn-off, steady-state, and dynamic operation portions of the current response wave form.

A. Turn-on, Turn-off, and Steady-State Operation - The computer program will include an optimization process which will include a set of network models each of which represents a class of loads.

   These models will be composed of passive elements arranged in a network configuration whose response can be made to duplicate the load response by a judicious selection of the network element values as described earlier in Paragraph 4 of this report.

B. Dynamic Operation - For the dynamic portions of the response curve, the computer will calculate:

$$R(t) = V(t)/i(t)$$

   for each interval of sampled data. This will result in a time history of the voltage - current ratio over the entire duration of dynamic operation.

C. Stress Identification - For each of the operations just described (TO/TO/SS and dynamic) an additional computation would be made to determine the minimum required stress rating of each component. For resistors, this would be a power dissipation versus time curve; for capacitors, an applied voltage versus time curve; and for inductors, an applied current versus time curve.

5.1.2 Interrogation Computer Requirements and Trade-offs

5.1.2.1 Sampling and Phase Requirements for the AC Case

The sampling requirement is that enough, usually on the order of 3 to 10 samples per cycle of the highest data frequency, data samples are taken to define the maximum frequency of dynamic operation. Furthermore, for the AC case that the sample value can be referenced to a unique point on the waveform, for example the positive zero crossing. To insure that the voltage and current are sampled at the same time requires that the two channels be multiplexed and provided with individual sample and hold circuits.

The R(t) obtained by dividing the voltage and current time samples is specified at a point in time but is not related to a unique point on the voltage waveform which is required for accurate simulation. The following technique may

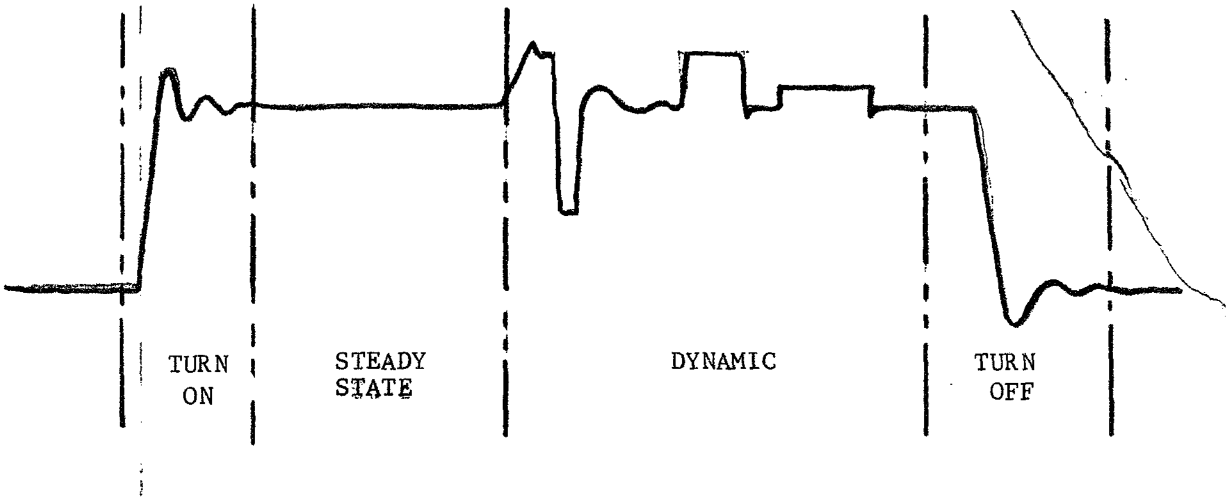


FIGURE 5-4 GRAPHICAL REPRESENTATION OF DYNAMIC ELECTRICAL LOAD CURRENT

be used to correct for the phase error. The voltage data samples are linearly interpolated to obtain the time of the zero crossing. Now R(t) data samples are linearly interpolated to obtain sample values at uniformly spaced Δt referenced to the zero crossing time. These are the R(t) values which would be used for the simulation.

The example shown in Figure 5-5 illustrates this technique. Sample values are shown at 15° intervals. The voltage zero crossing occurs mid-way between samples. Therefore, the voltage data is linearly interpolated to determine the time of the zero crossing, T_o. R(t) data is now interpolated to obtain R(t) values with uniform sample spacing referenced to T_o, shown as R_T values. The advantage of this approach is that it reduces the sample rate needed to obtain R(t) values referenced to a unique point on the voltage waveform.

Another approach to minimize the phase error is to sample at a faster rate such that the phase accuracy of R(t) is within acceptable limits. A phase error of 2° corresponds to a 3% of full scale error in the simulation and would probably be acceptable. The relationship of phase error and sample rate is

$$\text{phase error} = \pm\tfrac{1}{2}\,\frac{(\text{Source frequency} \times 360^\circ)}{\text{sample rate}}$$

For a source frequency of 400 Hz and sample rate of 10,000 sps the error is ±7.2°. This can be reduced using the interpolation technique described. Without interpolation, the sample rate required for a 2° phase error is 36,000 samples/sec.

5.1.2.2 Interrogation System Approaches

The interrogation system must perform 3 major functions -

Data Acquisition - Measure voltage and current time histories and record on magnetic tape

Analog-to-Digital Conversion - Convert measurements to digital values

Digital Computation - Perform digital computations required to obtain input values for simulator

For all approaches being considered the requirements are to provide digital representations of the voltage and current measurements for use in subsequent digital processing operations that will yield input data for the load simulators. The significant trade-off areas are individual equipments cost vs performance, and overall system configuration vs cost, flexibility of operation and turn around time, i.e. time required to obtain simulator inputs after the interrogation operation has been performed. For trade-off purposes, the interrogation system is considered to consist of 3 major subsystems: See Figure 5-6.

1. Data Acquisition System
2. A/D Conversion System
3. Digital Computer System

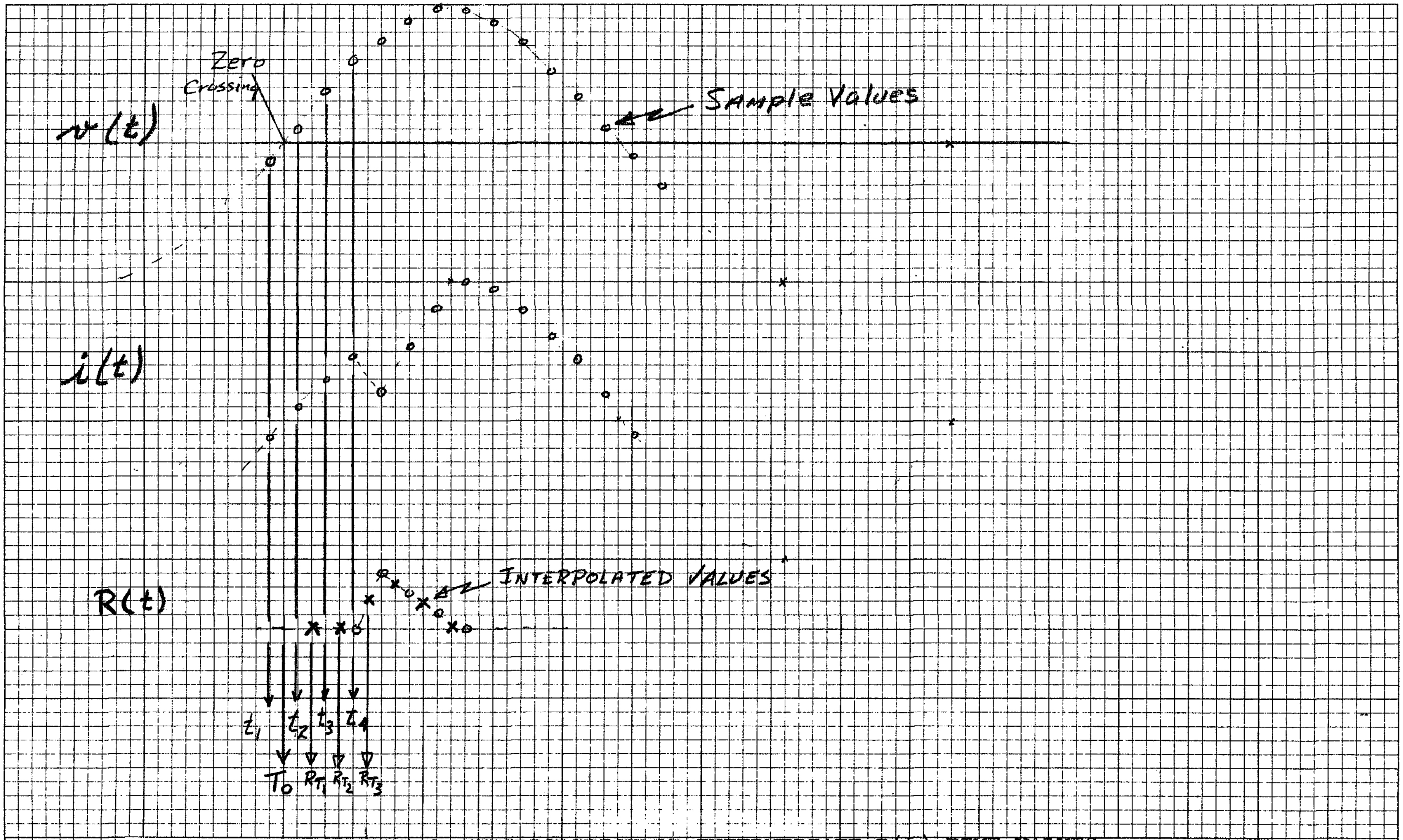


FIGURE 5-5 INTERPOLATION OF INTERMEDIATE R(t) TIME VALUES

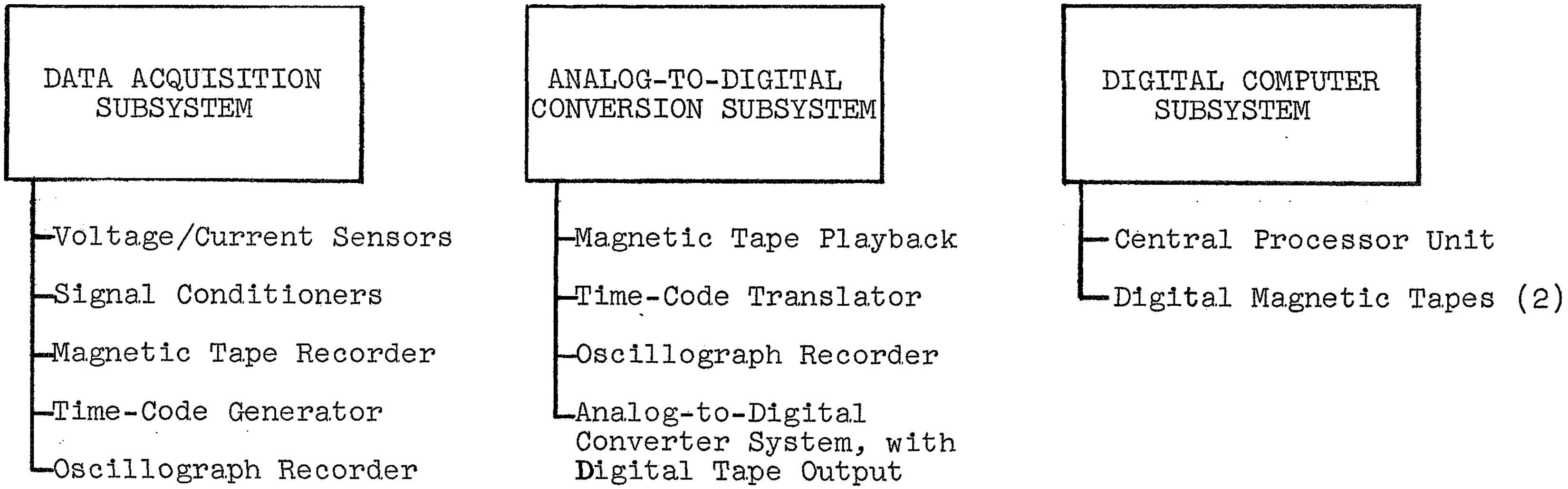


FIGURE 5-6 INTERROGATION SYSTEM, MAJOR SUBSYSTEMS

5.1.2.3 System Configurations

Five alternative system configurations, summarized in Table 5-2, were considered. These are discussed below.

A. Independent Stand-Alone System

This system configuration would include all hardware components and computer programs required for acquisition and processing. This approach provides maximum operational flexibility since the system is totally independent and capable of performing all necessary operations independently and under internally controlled scheduling. It also is the most costly approach, requiring a large initial equipment expense and large operating staff. Turn-around time would be on the order of 4 to 8 hours.

B. Modified Stand-Alone System

A variation of the first approach would include A/D conversion capability as part of the digital computer capability and share the acquisition magnetic tape recorder for tape playback. This approach would result in a moderate equipment cost saving at a small sacrifice in totally independent scheduling of operations; i.e. acquisition would preempt A/D conversion and A/D conversion would preempt computer processing. Turn-around time is not significantly affected.

C. Data Acquisition Only

This system configuration would include capability only for acquiring the data on analog magnetic tape. This tape would then be forwarded to a central agency with the necessary capability and operating skills for performing the analog-to-digital conversion and digital computations to provide outputs usable by the simulators. This is the minimum cost approach but has the greatest effect on operational flexibility and turn-around time. However, this approach is ideally suited for performing interrogation at remote locations since the size and complexity of remote interrogation, i.e. data acquisition, is minimized. Mobility is further enhanced by use of a portable instrumentation recorder.

D. Real-Time A/D Conversion

This approach would eliminate the analog magnetic tape recorder with a small cost saving. However, it complicates and increases the cost of acquisition at remote locations, and eliminates flexibility of data conditioning during the A/D coversion operation.

E. Stand-Alone Without Digital Computer

This approach would include A/D conversion capability in addition to magnetic tape record/reproduce. The A/D tape would then be sent to a central computer facility for processing. No clear-cut advantage in turn-around time, unless computer facility is located close to the simulator site.

TABLE 5-2

INTERROGATION SYSTEM TRADE-OFFS

System Configuration	Flexibility (%)	Turn-Around Time (Hrs.)	Relative Costs		Operating Staff (%)	Remote Site Operation
			Hardware (%)	Software (%)		
A - (Stand-Alone)	100	4-8	100	100	100	Good
B - (Modified Stand-Alone)	66	4-8	70	100	80	Good
C - (Data Acquisition Only)	33	24-72	15	50	20	Good
D - (Real Time A/D)	87	4-8	85	100	80	Poor
E - (Stand-Alone without Digital Computer)	66	24-72	60	50	40	Good

Definition of Headings: Flexibility - Relative degree of technical and scheduling control of interrogation operations. Assumes 50/50 split of technical and schedule control.

Turn-Around-Time - Represents time required to provide results of interrogation operation for simulator input. (Assumes 1 day out - 1 day process - 1 day back for worst case.)

Relative Costs and Operating Staff are normalized to configuration "A".

Remote Site Operation - Rated according to complexity and cost of Date Acquisition System required at remote site.

5.2 SIMULATION

5.2.1 General Description

The simulator is shown schematically in Figure 5-7. It is a device (one of a family) capable of being programmed to reproduce a specific impedance time curve. Different simulators would be required to accommodate the various classes of loads. The classes would correspond to those chosen for the network models of the interrogation process.

The simulator would provide a fixed impedance in a specific configuration corresponding to the interrogation model to provide the turn-on, turn-off, and steady-state portions of the current response. In parallel (and perhaps series-parallel) with the fixed impedance would be a resistance element, such as a rotator, whose value can be varied in an analog manner to accommodate the dynamic portions of the current response. See Figure 5-8 for a schematic representation of the fixed and variable elements.

For the TO/TO/SS operation, the simulator could be considered as consisting of a number of variable R, L, and C components and a complex switching matrix used to interconnect them in the specified configuration. Another concept might be to use a number of fixed R, L, and C components and vary the total R, L, or C of any element by switching.

Other variations of configuration could be conceived each of which effects component value changes by some mechanized analog or digital technique.

Each simulator, in addition to providing for the fixed impedance model, would provide for accommodating the variable resistance device. This device could be a separate element and connected to a specific simulator as required, or each simulator could contain the variable elements as part of its basic configuration. The former is a more versatile technique since it permits flexibility and can accommodate any power level without penalizing all simulators with unnecessary size and power requirements.

The resistance—time history of the UUT obtained in the interrogation process would be stored in digital form in the simulator memory. The transfer of digital values would be controlled by a clock or other programmed source to deliver the R(t) values at the required times.

The simulator would be interfaced with the system under test using a short adapter cable which accommodates the standard simulator connector on one end and the specific system connector on the other end. In use, the simulator would present the TO/TO/SS impedance to the interface. Upon operation of the simulator, by application of a voltage corresponding to that specified for the UUT, the variable resistance operation of the simulator would be initiated and would proceed until the voltage was removed. Removal of the input voltage would cause the variable R program to reset to its initial condition.

Implementing the simulation scheme just described would permit the packaging of all impedance and variable resistance elements in a small volume.

Cooling provisions, if necessary, would also be included in this package. All other elements of the simulator could be located remotely.

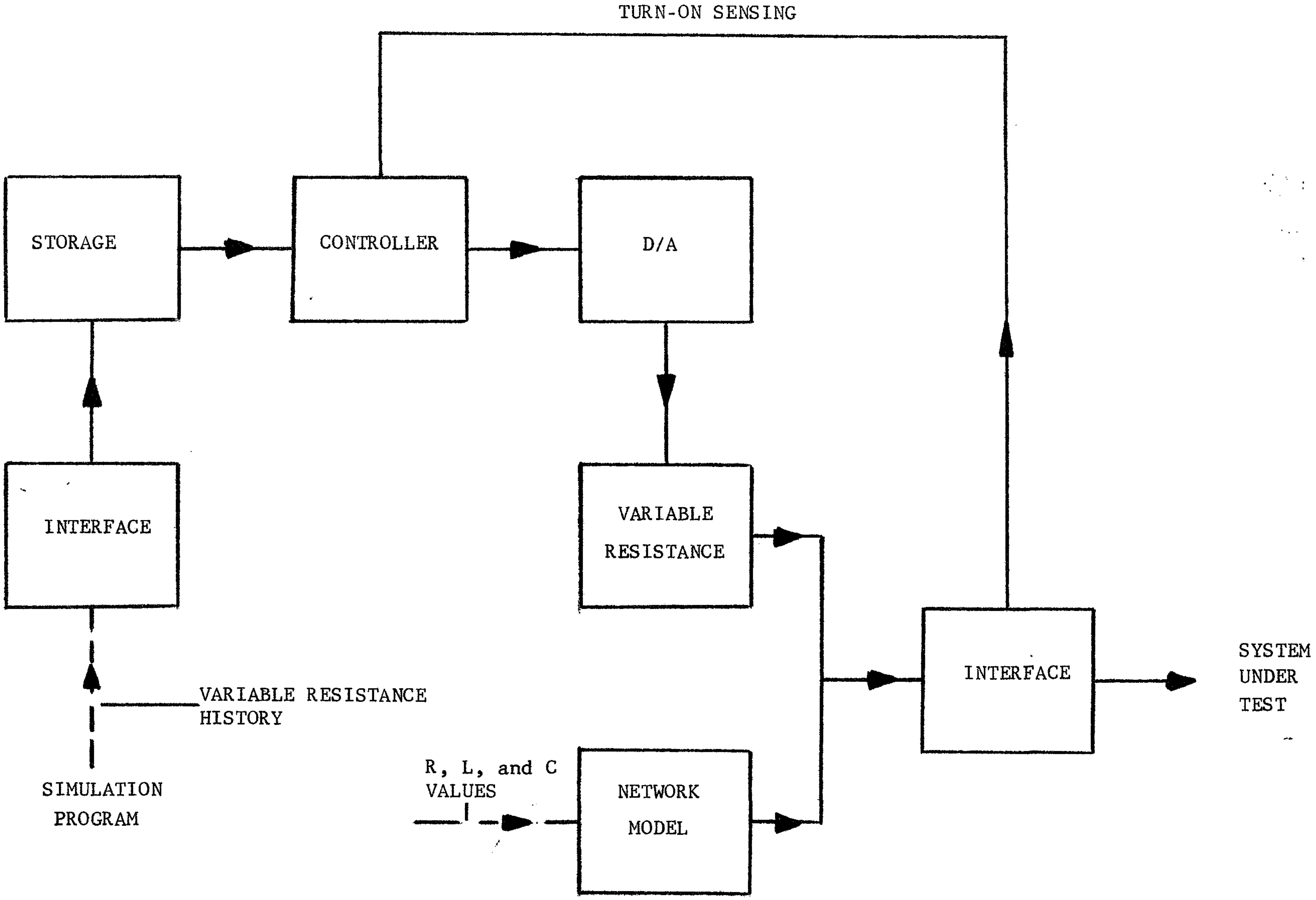


FIGURE 5-7 SIMULATOR CONCEPT FOR STEADY-STATE AND DYNAMIC OPERATION

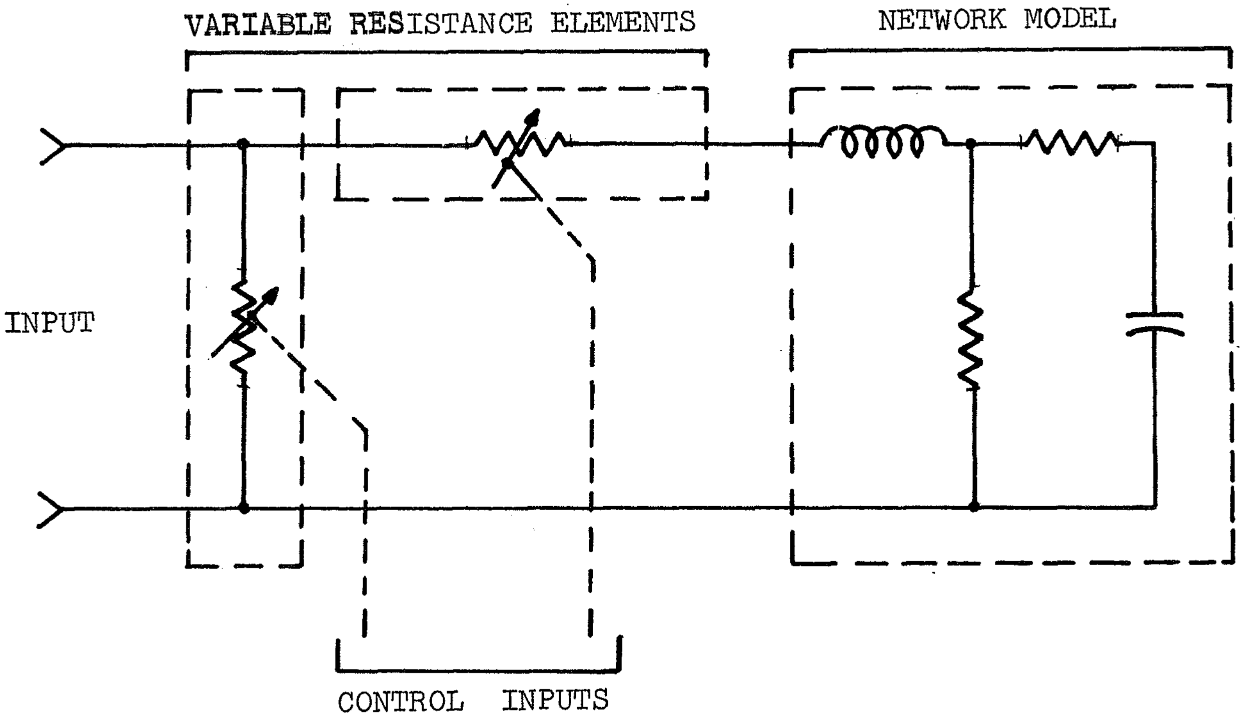


FIGURE 5-8

TYPICAL DYNAMIC LOAD SIMULATOR USING VARIABLE RESISTANCE ELEMENTS WITH NETWORK MODEL

In order to verify that simulator operation is acceptable, a validation process would be implemented. This would be accomplished by stimulating the simulator with the interrogation source and graphically recording the resultant current response. This response would then be compared with the response of the UUT determined during the interrogation. This comparison would be accomplished by visual observation of the two graphical displays.

5.2.2 Simulation Computer Requirements and Trade-offs

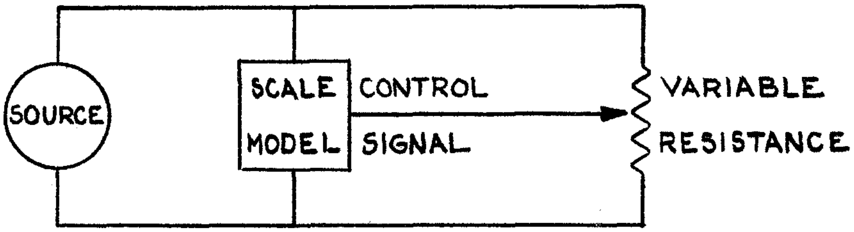
5.2.2.1 Simulator Approaches

The possible approaches to control the dynamic variations of load value are shown in Figure 5-9.

Level 1 indicates the objective which is to vary R(t) as a function of results obtained from the interrogation operation.

Level 2 indicates that the R(t) variation can be accomplished using either switched components or a continuously variable device.

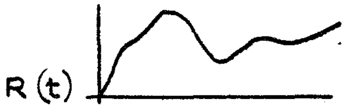
Level 3 indicates that the control signals can be obtained from stored data or from real time data. Real time may be a misnomer; what is meant is this type of operation.



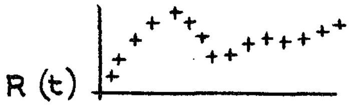
where the scale model duplicates the device's voltage-current performance characteristics at a scaled down power level and generates a control signal for a variable resistance.

Level 4 categorizes the form of data that is available for control.

Analog - continuous time history



Digital - sampled time history



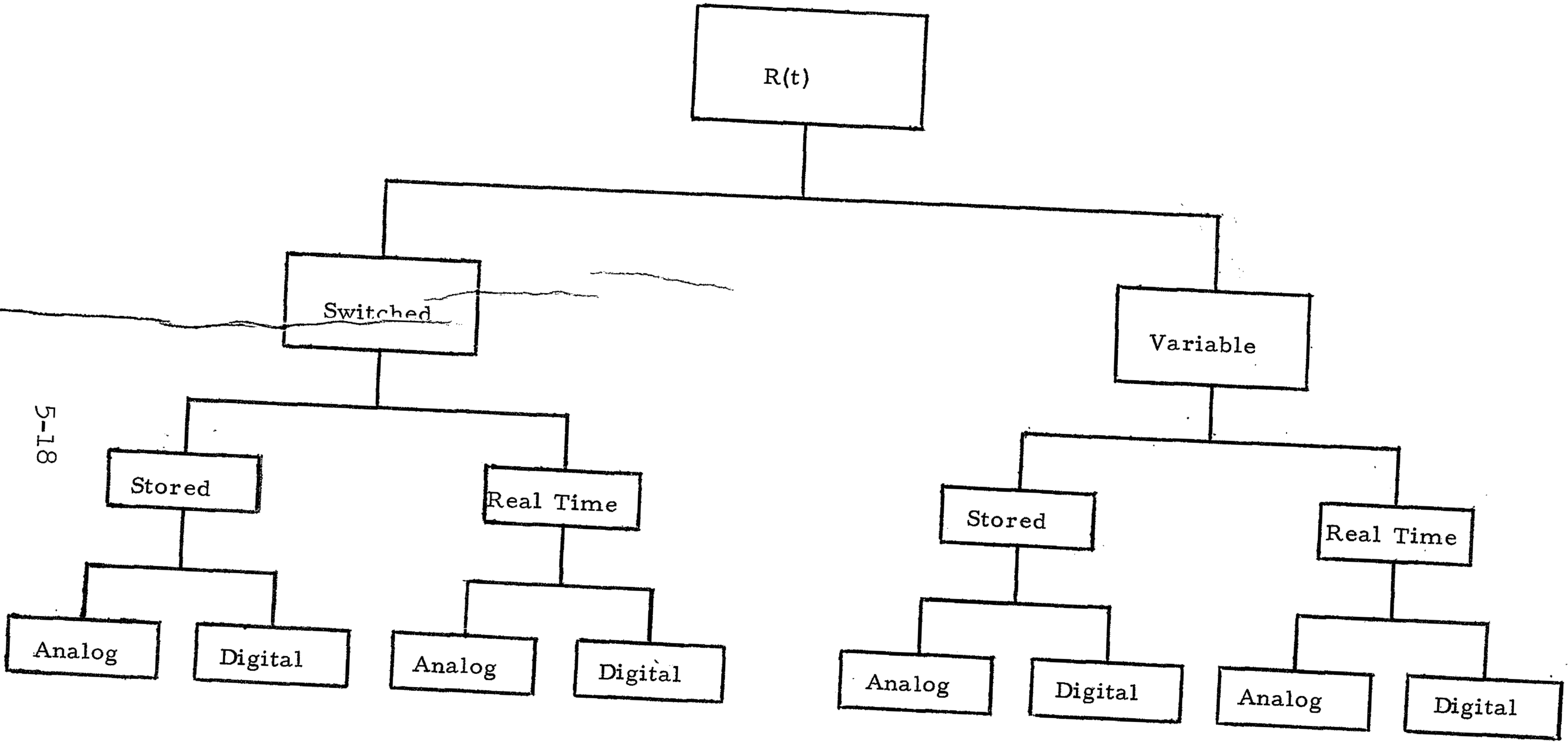


FIGURE 5-9 R(t) CONTROL APPROACHES

5.2.2.2 Switched Components Versus Variable Devices

From the storage and control standpoints, there is no significant difference between switching component values to provide a dynamic R(t) or providing a control signal for a variable device. A hybrid approach using both switched components for large changes in load value, and variable devices for handling small changes is possible but would increase the storage and control requirements for the simulator.

5.2.2.3 Stored Versus Real-Time Operation

The primary advantage of the real-time approach is its simplicity. The storage approach is more complicated and costly, but it has the advantage of flexibility in producing complex dynamic variations.

5.2.2.4 Analog Versus Digital Control Signals

Analog control signals are most directly suited for the real-time, variable mode of operation. For the stored mode of operation, the analog control signal approach cannot be used. The major difficulty being synchronization of the stored data with simulator turn on, and in the AC case the power frequency. Analog tape recorders have start-up times measured in terms of seconds which means that R(t) values would not be available until the recorder had reached its operating speed. For the switched mode of operation, analog control signals would have to be converted to digital form to control the switching.

Digital control signals are most directly suited for the stored, switched component mode of operation. There is no reason to consider digital control signals for the real-time operating mode. For the stored-variable mode of operation, digital control signals can easily be converted to analog form using an digital-to-analog converter (D/A). These units are available with operating speeds in the order of 5μseconds and conversion accuracies of 0.1%. A further advantage is that the switching discontinuities can be filtered using simple RC networks to provide a smoothly varying control signal.

5.2.2.5 Analysis of Digital Storage Parameters

The significant parameters which must be considered are storage capacity, data transfer rate, and synchronization of data readout. These parameters can be analyzed with reference to the following simulator requirements.

R(t) Dynamic Characteristics

AC Case	- R(t) occurs at the period of source voltage frequency and is defined by 25 samples per cycle of source frequency.
DC Case	- R(t) occurs periodically after turn-on and is defined by 100 samples in a 0.1 second interval.

Maximum number of simulators - 30

Dynamic Range of Control Signal - 1000:1

Accuracy of Control Signal - 1% of Full Scale

Simulator on-off - Controlled by sensing presence of external voltage.

The accuracy and dynamic range can be realized using a 10-bit data sample. This provides a control range of 0 to 1023 values.

For the AC case, the storage capacity is twenty-five 10-bit samples and the transfer rate is 10,000 samples per second for a 400 Hz power frequency. A very critical requirement is for the transfer of stored data to be synchronized to the source frequency in order to preserve the phase relationship between R(t) and the source voltage. This means that each simulator must generate a data transfer clock which is synchronized to the source frequency. This can be accomplished using a phase-locked loop approach with a voltage controlled oscillator (VCO) and a zero-crossing detector to establish a phase reference point.

For the DC case, the storage capacity is one hundred 10-bit samples and the transfer rate is 1,000 samples/second. The synchronization requirement is not critical. Data transfer can be controlled by a 1 KHz clock with readout commanded to repeat every ΔT interval, where ΔT could be obtained from time-of-day, i.e. every second repeat readout.

Two approaches are considered for providing digital storage and control of the simulator. One is to use a signal control computer to store the data for each simulator and control data transfer by sensing external interrupt signals. The other is to use separate storage and control logic for each simulator. For the AC case the single computer approach appears to be marginal as far as preserving the phase relationship of the data transfer. With direct memory access, computer transfer rates for a single output channel are on the order of 1μ second. Considering that memory readout would have to be time multiplexed for servicing up to 30 simulators implies that a minimum of 30 μseconds are required to provide one data sample to each simulator and it is more likely that 2 or 3 memory cycles would be required. Since 1° of phase at 400 Hz represents 7μ seconds, it is seen that phase errors in the order of 4° to 12° can be expected.

The separate storage/control approach, on the other hand, can easily provide data transfers in the order of 1-5μ seconds depending on memory cycle time selected. The advantages of this approach are that the simulation can be performed independently at various locations and the number of simulators can be expanded by simply adding N more units, whereas the single computer approach would have to be sized for the maximum number of simulators planned. The storage could be loaded manually, considering that the number of data samples are small, 25 or 100. This feature would lend itself to independent operation. However, to facilitate operation with multiple simulators, loading could be accomplished using a small computer with digital tape input. In this case the simulators would be treated as an external device. This also provides for another level of R(t) control since the stored values could be changed during a simulation run to simulate "slow" variations of R(t).

5.3 IMPLEMENTATION OF EQUIPMENT REQUIREMENTS

Major items of equipment have been identified and the necessary performance capabilities defined on the basis of preliminary interrogator/simulator requirements.

5.3.1 Interrogation System

The interrogation system consists of three basic subsystems, data acquisition, analog-to-digital conversion, and computer. These are discussed in Paragraphs 5.3.1 through 5.3.3, below, and shown in Figure 5-10.

5.3.1.1 Data Acquisition Subsystem

Output signals from voltage and current sensors will be conditioned to the range of 1 to 10 volts and recorded on an intermediate band instrumentation magnetic tape recorder using FM techniques. This will provide information bandwidths from 0 to 40 kHz at 120 inches/second and a channel signal—to—noise ratio of 50 db. Capability will be provided for recording 10 data channels - 3 phase voltages, 3 phase currents, neutral current, and 3-phase to neutral voltages. Additional channels will be provided for recording voice annotation, time code and servo reference frequency. A 1" - 14—track configuration is required. FM record and FM reproduce electronics will be provided for all tape speeds, 120 to 1-7/8 inches/sec, in order that time-base expansion techniques can be used in subsequent data processing operations. A 12-channel oscillograph recorder with 5kHz frequency response capability is required for quick-look data display and time editing. A time-code generator and time-code translator are required to facilitate locating areas of interest recorded on the tape.

5.3.1.2 Analog-to-Digital Conversion Subsystem

The A/D convertor will perform a 10-bit conversion on bi-polar signals in the range of 1-10 volts. This provides a 1000:1 resolution which is consistent with the simulator dynamic range requirement. A sampling rate of 20,000 samples per second will provide the capability required to sample two functions, voltage and current, at 10,000 samples/second. Capability for multiplexing 2 input channels with simultaneous sample and hold is required to preserve AC phase relationship. The A/D output will be recorded on a digital magnetic tape in standard computer—compatible format. It should be noted that the effective sampling rate can be increased by using time base expansion techniques during data playback, i.e. reducing the playback speed by a factor of 8 provides an effective sampling rate of 160,000. Operating features will be included for commanding start/stop of conversion at pre-selected times, sample rate control, digital output monitor, and calibration source.

5.3.1.3 Computer Subsystem

The computer will accept the digital magnetic tape produced by the A/D subsystem and perform the necessary digital operations to provide input data for the simulators. The computational requirements are as follows:

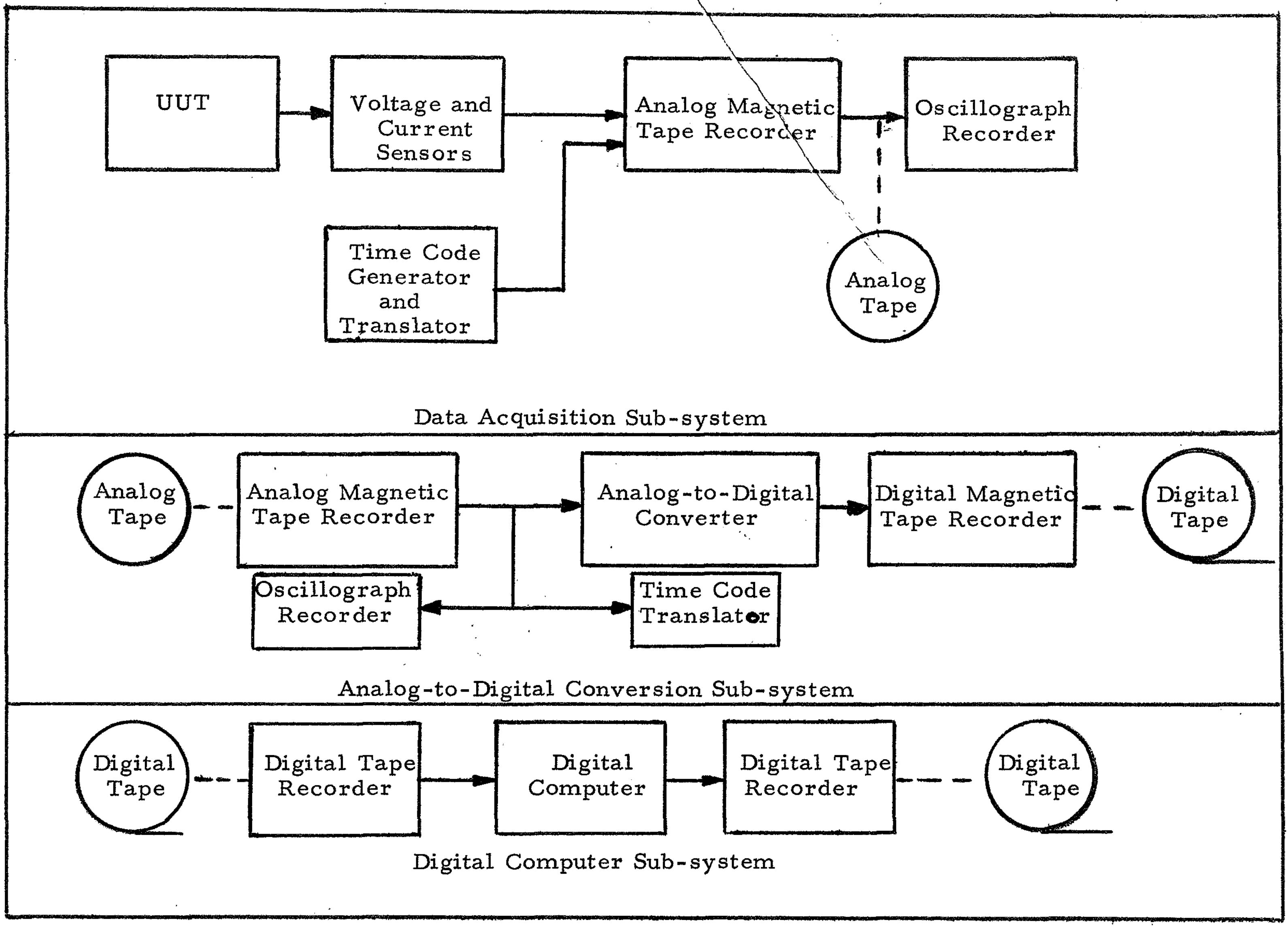


FIGURE 5-10 INTERROGATOR SYSTEM, BLOCK DIAGRAM

- Data Calibration
- Linear Interpolation
- Division
- Model Optimization
- Determine component stress ratings

The computer hardware configuration will include:

Central Processor Unit - 16-bit word, 32K memory size, 2 μ sec memory cycle time, with multiply/divide hardware.

Teletypewriter
2 Digital Magnetic Tapes
Line Printer } Desirable, but not required
Card Reader }

The computer software will include such standard items as:

Assembly Program
Fortran IV Compiler
Arithmetic Sub-routines
Floating Point

Computer programs will be required to perform the indicated operations.

The significant interrogator computer performance characteristics are summarized in Table 5-3.

A pictorial view of such a system is shown in Figure 5-11.

5.3.2 Simulator System

The simulator system will consist of a small control computer and individual storage and control logic for each simulator, see Figure 5-12.

The control computer will have the following capability:

Memory cycle time	2 microseconds
Memory word length	12 bits
Memory capacity	8000 words
External Interrupts	30

Other features required are digital magnetic tape input, teletype input/output, direct memory access channel, and a real-time clock. Assembly language and real-time executive monitor software are required.

The simulator storage will have the capability for storing one hundred 10-bit data samples, thus it provides adequate capacity for both the AC and DC cases. For the AC case, the data sample transfer will be synchronized to the external power source frequency, within 2° of phase and the transfer rate will

TABLE 5-3 INTERROGATION SYSTEM PERFORMANCE CHARACTERISTICS

DATA ACQUISITION SYSTEM	ANALOG-TO-DIGITAL CONVERSION SYSTEM	DIGITAL COMPUTER SYSTEM
10 CHANNELS 0-40 kHz FREQUENCY RESPONSE 50 db SNR	2 CHANNELS 10,000 SAMPLES/SEC/CHAN. SIMULTANEOUS SAMPLE & HOLD 10 BIT SAMPLE	16 BIT WORD 32k MEMORY PROGRAMS FOR - DATA CALIBRATION LINEAR INTERPOLATION DIVISION MODEL OPTIMIZATION COMPONENT STRESS RATING DETERMINATION
(AMPEX MODEL 1900)	(ASTRODATA MODEL AD-1)	(HONEYWELL MODEL 516)

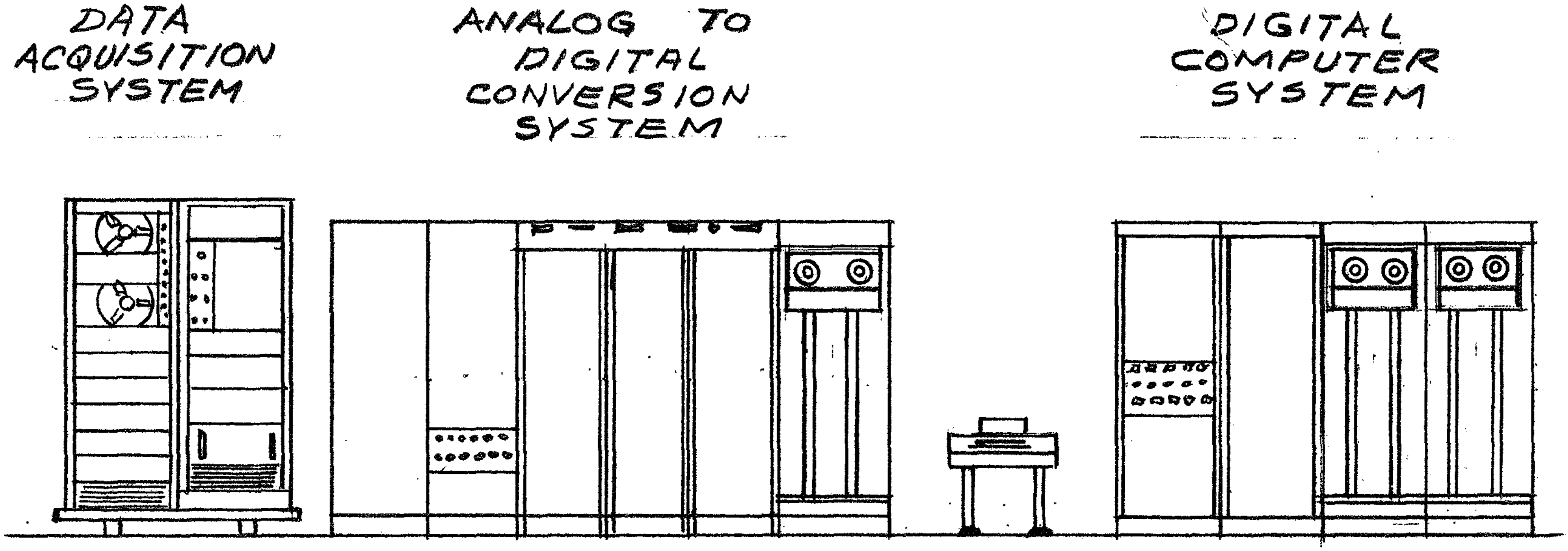


FIGURE 5-11 INTERROGATION SYSTEM, PICTORIAL DIAGRAM

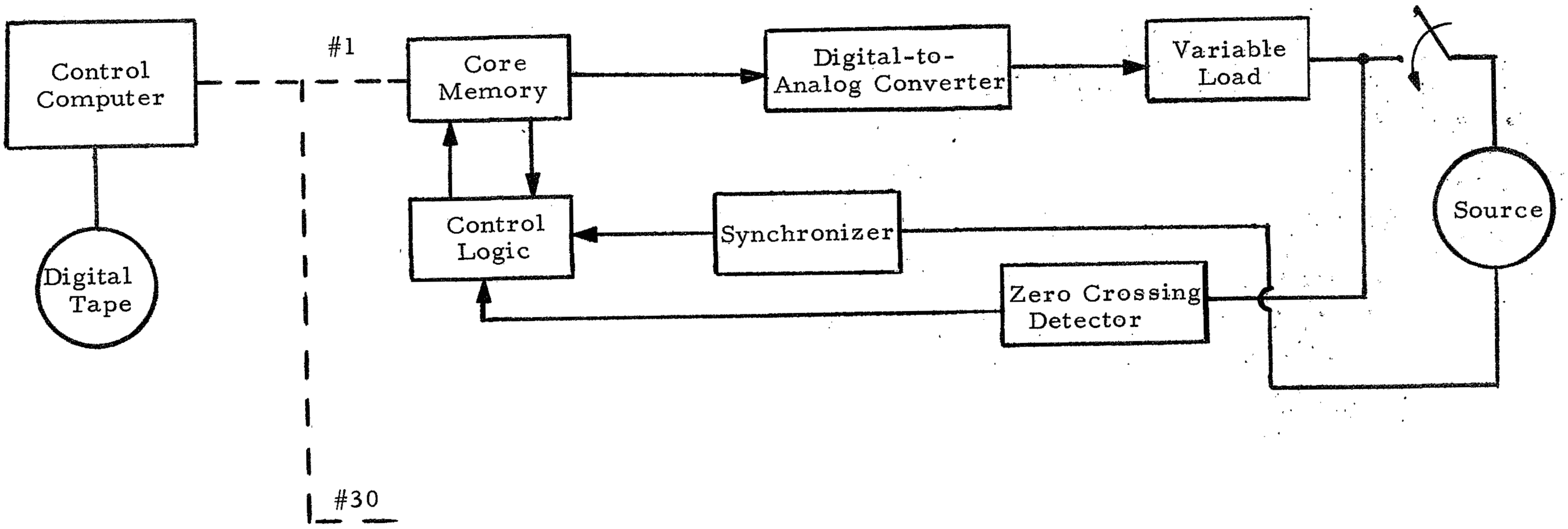


FIGURE 5-12 SIMULATOR SYSTEM, BLOCK DIAGRAM

be 10,000 samples/second. For the DC case, data sample transfer will occur at Δ T intervals, selectable from 0.1 to 10 seconds, and the transfer rate will be 1,000 samples/second. The storage will be interfaced to the control computer as an external output device which will allow for loading storage from digital magnetic tape. Provisions will also be included for loading storage manually to allow independent operation at a remote site.

Control logic will provide capability for initiating data transfer from an external switch closure, switch opening will reset storage to the initial value, and for controlling data transfer from an external clock signal.

The device used for synchronizing the external clock signal to the AC source frequency will maintain phase coherence within 2°. Phase–lock–loop response time in the order of 0.1 second will be required.

The output of the storage will interface with a digital-to-analog converter. The D/A will provide capability for a 10-bit conversion, 0.1% accuracy, and operating speeds in the order of 5-10 microseconds. Output filtering will be provided to minimize switching discontinuities. The output voltage range will be compatible with the requirements of the variable device, 0-10 volts.

The significant simulator computer performance characteristics are summarized in Table 5-4.

A pictorial view of a simulator, including the computer (storage and control units), is provided in Figure 5-13. A single console as shown can accommodate up to six simulators simultaneously.

5.4 INTERFACES

The interrogation/simulation process just described will have three major interfaces.

1. Interrogator/unit under test
2. Interrogator/simulator
3. Simulator/system under test.

These are shown in simplified block diagram form in Figure 5-14, and discussed briefly in the following paragraphs.

5.4.1 Interrogator/Unit Under Test Interface

This interface is the point in the system at which the interrogation measurements are obtained. Typically, each load to be interrogated will have a unique power connector. Provisions must be made for interfacing these connectors with the common connector on the interrogator.

Additionally, provisions must be made for sensing the voltage and current at the interface and routing such data to the appropriate measurement device.

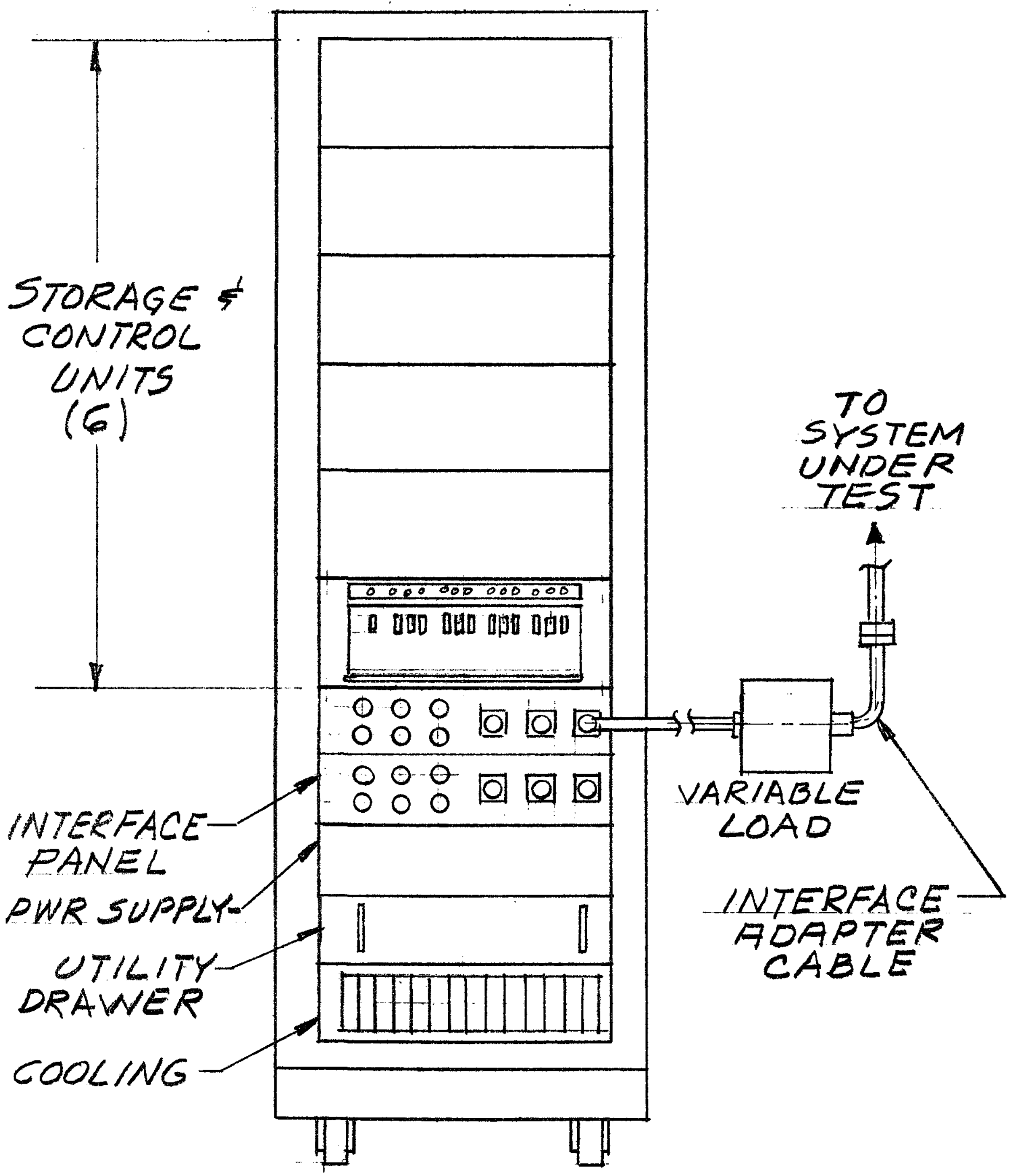
The voltage to the device may be DC or AC (both single and three-phase) and at high power levels.

TABLE 5-4 SIMULATION SYSTEM PERFORMANCE CHARACTERISTICS

- MEMORY CAPACITY - 4,000 WORDS
- WORD SIZE - 10 BITS
- TRANSFER RATE - 10,000 SAMPLES/SECOND
- DYNAMIC RANGE - 100:1
- SYNCHRONIZATION - 2° OF PHASE RELATIVE TO POWER SOURCE FREQUENCY

(Honeywell Model H112)

FIGURE 5-13 DYNAMIC LOAD SIMULATOR, PICTORIAL DIAGRAM



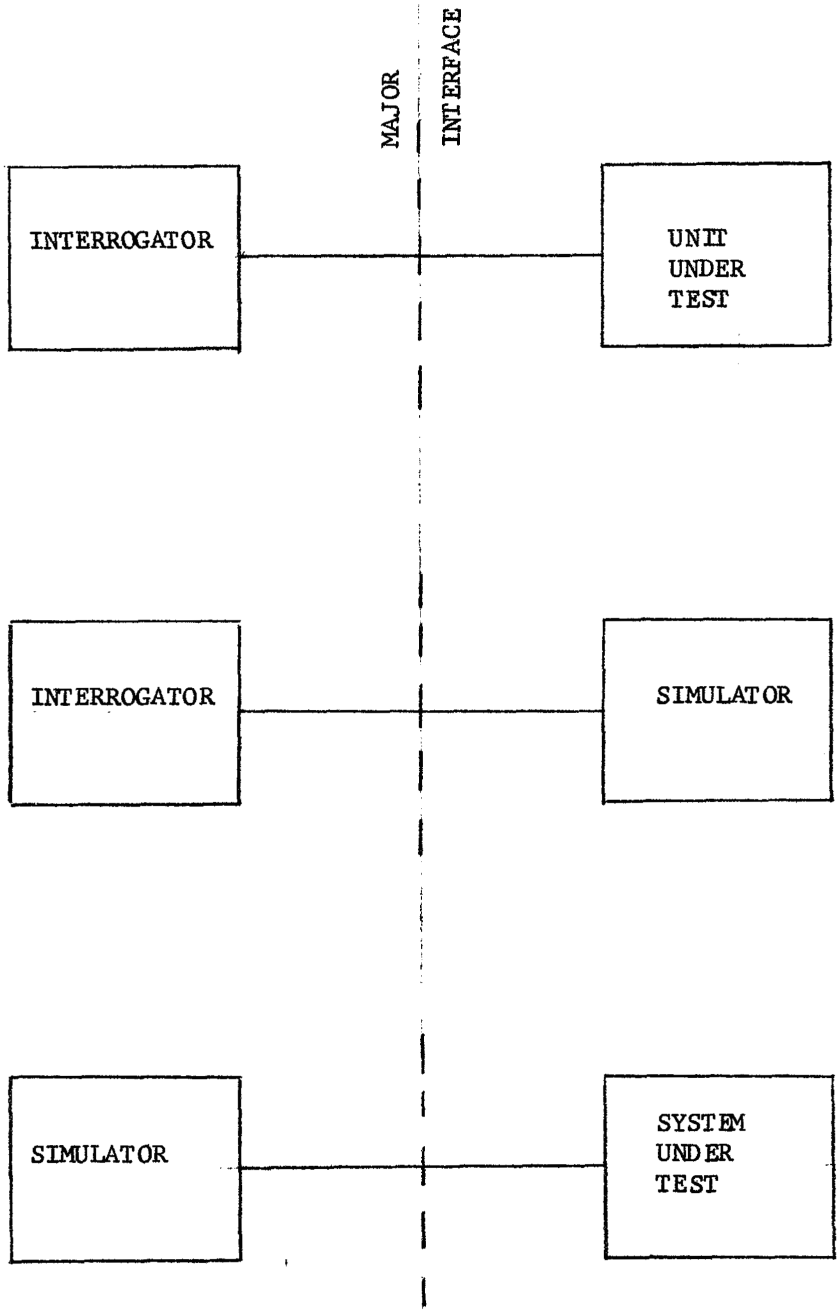


FIGURE 5-14 MAJOR SYSTEM INTERFACE IDENTIFICATION

5.4.2 Interrogator/Simulator Interface

The interface between the interrogation system and simulation system primarily involves the transfer of the impedance-time history parameters, as determined by the interrogation process, to the simulation system in a compatible format.

The primary requirement for the interrogator/simulator interface is, therefore, compatibility of information transfer. That is, the output of the interrogator system should be compatible with the simulator's input requirements. The interface is a function of the particular concept chosen. If, for example, the interrogation system output is in the form of digital data recorded on magnetic tape, then the simulation system must be capable of accepting digital data recorded on magnetic tape as an input.

The information transfer between the interrogation and simulation systems can take place either in real time or, by use of a suitable storage medium, in elapsed time.

5.4.3 Simulator/System Under Test Interface

It is anticipated that a family of simulators will be required to accommodate the various spacecraft electrical loads. Each of these simulators will be capable of representing (one-at-a-time) a number of loads, depending on the particular programming information entered in the simulator. Typically, each load will have a unique power connector. Provisions must be made for each simulator to accommodate a number of different interfaces.

In addition, it might be desirable to provide means for voltage and current data sensing at these interfaces to permit measurements to be made during system operation.

5.5 THREE-PHASE POWER CONSIDERATIONS

A review of the spacecraft load classification table (Table 3-3) shows that a number of the loads to be treated are operated by three-phase power. The discussions of the various interrogation and simulation methods thus far have not considered the specific nature of the input power. The interrogation techniques are, generally, applicable whether the normal operating power of the device is DC or single-phase AC.

Simulation of single-phase AC devices is somewhat more complicated than in the DC case, but the techniques described apply in either case.

It would seem that the three-phase AC case can be treated by using the same techniques that apply to the single-phase case. That is, a three-phase device would be interrogated by monitoring the voltage between all significant pairs of wires (e.g., between each pair or phases and between each phase and neutral) and the current in each current carrying wire. In the worst case, this would require a ten-channel measurement system. Alternatively, the interrogation might be accomplished in several passes, each one treating a different combination of phases.

In any event, the data, once obtained, would be processed as though the measurements had been made on a number of single-phase devices. Simulators would then be programmed to treat each case and interconnected in a three-phase configuration. Any interaction between the phases would be observed during interrogation and would automatically be programmed into the individual simulators.

6. ASSESSMENT OF FEASIBILITY

In the overall interrogation/simulation process described in paragraph 5, two key elements requiring consideration from the standpoint of feasibility are:

1. Development of network models whose response can be made to match accurately that of a specific load by appropriate adjustment of the values of elements in the model.
2. Development of variable resistance devices capable of operating at high voltage and current levels.

These elements are discussed in paragraph 6.1 and 6.2, respectively.

6.1 MODEL DEVELOPMENT

Examination of various models has resulted in development of: (1) several preliminary models of motors, and (2) a generalized model for representing a general load, such as that presented by an electronic device.

A significant consideration in model development is the selection of an optimization criterion for judging a given model's ability to reflect faithfully the response of an actual load. There are numerous criterions by which a comparison may be made between the model's response and the actual load's response (that is, the error) may be judged. These include the use of:

1. The sum of the absolute values of the error.
2. The sum of the squares of the errors.
3. The sum of the absolute errors between the derivative of the model's response and the derivative of the load's response.

In the computer optimization routine, iteration is performed to minimize the error defined by these various criterions. Selection of the criterion to be specified is based on engineering experience and judgment. To that extent, the selection is subjective.

The problem of assessing the feasibility of developing and implementing network models lies in the great variety of possible loads and consequent potentially great variety of responses. Arbitrary assignment of accuracy or cost requirements (or any combination of similar mutually dependent requirements) applicable to all possible loads presents a formidable problem, one that may, in fact, be virtually insoluble. It appears more practical to develop models for selected loads and to demonstrate the suitability of these models in the laboratory.

The investigations made in this study indicate that given an unrestricted number of model parameters or an unspecified model response accuracy, the concept of modeling is entirely feasible for use in a system identification/ simulation process. To be practical, of course, the number of model parameters must be limited (perhaps to less than 10) to permit optimization to be completed in a reasonable period of time. Also, some limit must be placed on the model accuracy.

The optimization computer programs used in the modeling investigations were adapted from existing software and, thus, were not as efficient as might be required. However, the models showed good correspondence with the actual devices.

6.2 VARIABLE RESISTANCE DEVICE DEVELOPMENT

The second key element from the aspect of determining process feasibility is the variable resistance element used for dynamic operation. Several techniques for implementing this element have already been examined and tested in the laboratory. One technique employs a resistance rotator. Laboratory tests were conducted on a rotator used to provide a dynamic response. The results of the experiment clearly demonstrated that a variable resistance device can simulate the response of a dynamic load, and, furthermore, that the variable resistance control signal can be derived from interrogation data, stored in digital format, and subsequently retrieved. Although this experiemnt was conducted at low voltage and current levels (approximately 40 volts and 1 ampere), the operating principles are equally applicable at higher voltage and current levels. Methods of handling these higher values have been described in the monthly progress reports.

6.3 COMPUTER HARDWARE AVAILABILITY

The interrogation system requirements are well within the capabilities of presently existing equipment. For example, the data acquisition system can be realized using an Ampex Model FR-1900 instrumentation recorder, CEC Model 5-133 oscillograph recorder and Astrodata Model 5200 time-code generator/ translator. The A/D conversion system presently exists as an Astrodata - Model AD-1 system. The digital computer hardware requirements are satisfied by any of a number of general-purpose computers and, with the exception of model optimization, all of the necessary computations as well as the data acquisition and A/D conversion are currently being routinely performed in Avco's data processing operation.

Simulator system requirements are also well within the capabilities of presently existing equipment. For example, the control computer requirements are satisfied using the Digital Equipment Corp. Model PDP-8/L. The storage and control requirements would be more than satisfied using a standard product such as the General Automation Model SPC-12 controller. However, it may be more cost effective to design a special unit using standard core memory and logic components. This would depend on how many units were required such that the design cost could be spread over several units. The phase synchronization could be achieved using phase lock loop techniques currently used in bit rate synchronizer and tape recorder servo speed control applications. The digital-to-analog converter requirements are met using an Analog Device Model DAC-T unit.

6.4 SUMMARY

The load interrogator and simulator concept is feasible. This conclusion is based on careful consideration of the following-listed results obtained during this study:

1. The computer and data processing software and hardware for implementing the process are available.

2. The variable impedance hardware's performance has been successfully demonstrated at low voltage and current levels; methods for handling higher levels have been proposed.

3. The development of network models to simulate the steady-state and turn-on/turn-off transient characteristics of loads is feasible when loads are considered on an individual basis.

7. RECOMMENDATIONS

The study has identified and investigated various methods of interrogating and simulating electrical equipment. Further, the study has described a hardware system capable of implementing the total process. Laboratory tests on the more critical elements of the process have demonstrated the proposed system's feasibility.

The next step in the evolution of dynamic load interrogators and simulators is implementing the proposed system to demonstrate its practicality and to assess in laboratory experiments its usefulness and completeness.

Table 7-1 summarizes hardware and software requirements for implementing the interrogation/simulation system and identifies the availability of the required items. As the table indicates, most of the hardware is readily available. Only those elements peculiar to load simulation would need development.

The following six-step program designed to demonstrate the practicality of the proposed approach is recommended as a minimum-cost next step in the system's evolution.

1. Interrogation of Real Equipment - Use existing data acquisition equipment to acquire voltage and current data on a number of (ten or fewer) items of actual spacecraft hardware stimulated in their various modes of operation.

2. Analog-to-Digital Conversion - Convert the analog data obtained in 1., above, into a digital format consistent with data processing needs. Existing processing hardware is available and adequate for this task.

3. Optimization Software Development - Develop software for computer optimization of network models. Existing optimization programs (e.g., the Avco program described in this report) can serve as a baseline. Evaluation and selection of suitable criterions for judging model accuracy would be a concurrent task.

4. Selection of One Representative Equipment - Select one of the equipments for which data had been acquired and processed. The equipment selected should be one that provides maximum exercise of the hardware and software, and provides a suitable test-bed for system evaluation.

5. Simulator Design and Development - Design and develop one load simulator to provide the hardware required to simulate the one equipment item selected in 4., above. The development and use of continuously variable impedance elements should receive particular emphasis. This simulator would be tested and delivered for evaluation and use by the customer.

6. Documentation - Provide a complete set of drawings, specifications, and manuals (operating and maintenance) to support the delivered hardware. The documentation should include the

TABLE 7-1 HARDWARE AND SOFTWARE AVAILABILITY

	CURRENTLY AVAILABLE	REQUIRE DESIGN AND DEVELOPMENT
I. INTERROGATION		
A. Data Acquisition Hardware		
1. Tape Recorder	X	
2. Oscillograph Recorder	X	
3. Signal Conditioning Equipment	X	
4. Time-Code Generator	X	
B. Data Processing Hardware		
1. Analog-to-Digital Converter	X	
2. Digital Computer System	X	
C. Data Processing Software		
1. Routine Computation	X	
2. Model Optimization		X
II. SIMULATION		
A. Storage and Control Hardware		
1. Computer	X	
2. Integration and Control Hardware		X
B. Variable Impedance Hardware		X

computer software for model optimization, along with all other software peculiar to the process.

The objective of this program would be to develop software and hardware compatible with software and hardware to be developed subsequently for a complete stand-alone system.

8. BIBLIOGRAPHY

As in any comprehensive study, compilation of a bibliography received high priority. The results of Avco's efforts in this area are summarized in Appendix C. All of the publications listed there have been reviewed and found significant in reference to the dynamic load simulator study.

APPENDIX A

This appendix summarizes the five monthly progress reports published by Avco Systems Division under the Dynamic Load Simulators for Electrical Systems Test Facility Study, NASA Contract No. NAS-9-10429.

1. First Monthly Progress Report, for the period 29 December 1969 to 31 January 1970. Avco Document No. AVSD-0065-70-CR, dated 5 February 1970

   SUMMARY

   Describes Avco's efforts in the following two areas of concentration:

   1. Identifying spacecraft electrical loads.
   2. Identifying candidate interrogation and simulation techniques.

2. Second Monthly Progress Report, for the period 1 February 1970 to 28 February 1970. Avco Document No. AVSD-0108-70-CR, dated 6 March 1970

   SUMMARY

   Covers efforts in the following-listed areas:

   1. Completion of spacecraft electrical load identification.
   2. Establishment of requirements for developing and evaluating interrogation and simulation techniques.
   3. Identification of the interrogation and simulation techniques to be investigated.
   4. Establishment of contact with selected vendors in the areas of power dissipative devices, variable impedance elements, network analyzers, and measurement devices.

3. Third Monthly Progress Report, for the period 1 March 1970 to 31 March 1970. Avco Document No. AVSD-0157-70-CR, dated 6 April 1970.

   SUMMARY

   Describes efforts in the areas of:

   1. Examination of the various interrogation and simulation techniques. Particular emphasis was placed on measurement and data processing considerations, and on non-linearity and three-phase power considerations.
   2. Preliminary investigation of system interfaces.

4. Fourth Monthly Progress Report, for the period 1 April 1970 to 30 April 1970. Avco Document No. AVSD-0216-70-CR, dated 6 May 1970.

SUMMARY

Describes efforts in the areas of:

1. Continuation of the examination of interrogation and simulation techniques.
2. Establishment of requirements for the three major system interfaces.
3. Development of a total system concept and preliminary findings regarding the feasibility of implementing the concept.

5. Fifth Monthly Progress Report, for the period 1 May 1970 to 31 May 1970. Avco Document No. AVSD-0259-70-CR, dated 12 June 1970.

SUMMARY

Describes efforts in the areas of:

1. Investigation of the feasibility of using noise- and cross-correlation techniques for determining the system driving point immitance.
2. Investigation of a computer program that uses a frequency-domain technique for optimizing network models.
3. Investigation of the feasibility of constructing general network models for use in synthesizing time-domain iterative networks.
4. Demonstration in laboratory tests of an interrogation and simulation process based on a variable resistance technique.
5. Conduct of a trade-off study in the areas of interrogation and simulation techniques and their hardware implementation.
6. Development of a preliminary design for implementing an interrogation and simulation process.
7. Appraising the feasibility of implementing this process in hardware.

APPENDIX B

OPTIMIZATION PROCEDURES

The following description of Avco's optimization procedures for computer handling of network modelling has been extracted (with minor editorial changes) from Avco Document No. AVSSD-B798-610-6782, dated 23 April 1970 (pages 27 through 44, and pages 48 and 49).

2.3.2 Penalty Function Transformation

The penalty function proposed for this program allows the constrained optimization problem to be solved as a sequence of unconstrained problems. This section contains descriptions of the penalty function equation, the technique for defining a dummy function if the current search point is outside the capability of the analysis modules, and the techniques for tightening a constraint after each unconstrained search.

2.3.2.1 Function Evaluation

The analysis portion of the program characterizes the specifics of each design by a set of numbers called y_i. The selection of the desired combination of these quantities to be used in the penalty function is made by the user by means of input codes. The actual penalty function equation is described in the section called sequential optimization.

An alternate way of describing the calculation of the value of the penalty function, F, is as follows. Let F be the sum of the NP individual constraint terms, f_i:

$$F = \sum_{i=1}^{NP} f_i$$

where each term is:

$$f_i = \begin{cases} 0.0 \text{ if the constrained quantity is within the limits} \\ k_i\,(|\text{amount out of the limits}|)^I \text{ if not within limits} \end{cases}$$

where k_i and I are inputs. If the penalty function, F, is zero, the design is within all the constraints. If the penalty function is not zero, then its magnitude represents the "amount" that this design is unacceptable. The penalty function thus reduces the entire set of performance histories and design constraint situations to a single number (F). Optimization techniques can then be applied to find the designs which result in smaller values of the penalty function until a design is found which has a penalty function value of zero. This would then complete one "solution-finding" operation. The detail of the process of utilizing a sequence of solution-finding operations to obtain an optimum solution will be discussed in the section called sequential optimization.

2.3.2.2 Screening Operations

It is possible for an optimizer to specify that a design be evaluated which is not physically meaningful or which is outside the capability of the analysis modules. A testing procedure has been set up which "screens" out such situations and defines a value for the penalty function, F, which is equal to the sum of the last calculated value from the penalty function equation, D, plus the amount the design failed the screening test:

$$F = D + \sum_{i=1}^{N_S} S_i \left\{ \langle LL_i - X_i \rangle^2 + \langle X_i - UL_i \rangle^2 \right\}$$

where S_i is input; and the design parameters, X_i, the lower limits, LL_i, and the upper limits, UL_i, are specified within the program. It is assumed in this formulation that the initial design is input so that it passes the screening test.

2.3.2.3 Sequential Optimization

A technique for formulating the solution-finding problem was discussed in the Function Evaluation section. This technique has been extended to allow performance and design constraints to be included in the search for an optimum design. The extended technique effectively transforms the constrained optimization problem onto a sequence of solution-finding problems which are solved using unconstrained optimization techniques. The technique is based on the Schmidt and Fox penalty function equation of Reference 15 which will be considered in the following form:

$$F = k_1 \langle y_1 - UB_1 \rangle^E + \sum_{i=2}^{M} k_i \left\{ \langle LB_i - y_i \rangle^E + \langle y_i - UB_i \rangle^E \right\}$$

where:

F	is the penalty function which is searched for a zero or a minimum by the optimizer
k_1	is the multiplier (scale factor) for the quantity being minimized
y_1	is the quantity being minimized
UB_1	is an upper bound on the quantity being minimized
E	is the exponent which is normally 2 but can be set to 1 for special problems
M	is the total number of terms in the penalty equation
k_i	is the multiplier (scale factor) for each constraint
LB_i	is the lower bound for each constraint
y_i	is the value of each item being constrained
UB_i	is the upper bound for each constraint

$$\langle A \rangle \text{ is } \begin{cases} A \text{ if } A \text{ is positive} \\ 0.0 \text{ if } A \text{ is zero or negative} \end{cases}$$

There are two cases to be considered. The first is where the quantity being minimized is a calculated value or a design variable and the second is where the quantity is an input quantity which is not an active design variable.

For the cases where the quantity being minimized, y_1, is a calculated value or a design variable, the procedure is to input the exponents, the upper and lower bounds, and the multipliers. The first upper bound, UB_1, is selected to be reasonable large (based on experience and judgment). The multipliers, k_i, are allowed for numerical purposes and do not theoretically enter into the process at all. The first solution-finding operation is initiated from an input initial design. The optimizer modifies the design until every constraint is satisfied. At this point every term of the penalty equation is zero and the value of the penalty function, F, is therefore zero. The parameters describing this acceptable design are carried over to describe the initial configuration for the next solution-finding step. The first upper bound, UB_1, is reduced for the second solution-finding operation. Each time that it is possible to find an acceptable design, the constraint is tightened by a factor, W_{RF}, and the process is repeated:

$$(UB_1)_{I+1} = W_{RF}(y_1)_I$$

After a series of solution-finding problems, the constraint will have become so tight that a solution is no longer possible. In this situation, the search procedure finds that F has a minimum and that it is not possible to find a design where F equals zero, thus it is not possible to find a design which satisfies all the imposed constraints. The next-to-the-last design then is declared the optimum (within the tolerance implied by the factor, W_{RF}).

This technique of approaching the optimum from the "acceptable" side has been found to be a practical technique for design work.

A parallel procedure is used when the quantity being minimized, y_1, is an input which has not been identified as a design variable. After each successful solution-finding operation, the value of the input itself is changed:

$$(y_1)_{I+1} = W_{RF}(y_1)_I$$

Again, the solution-finding process is repeated until it is no longer possible to find a solution. The next-to-last design is then declared the optimum (within the implied tolerance).

When the general multivariable optimizers are used, the exponents in the penalty equation must have a value of two so that the first derivatives of the function with respect to the design variables will be continuous. However, since the Fibonacci techniques do not have any continuity restrictions, the exponents can be set to a value of one and the constrained optimum can be searched for directly. For one- and two-variable problems where Fibonacci techniques are applicable, setting the exponents to one and providing suitable k_i multipliers eliminates the need for the series of solution-finding operations discussed above.

2.3.3 Gradient Of The Penalty Function

When required, the gradient of the penalty function is calculated using finite differences. The increments, ΔX_i, are inputs to the program. Each element of the gradient is calculated as:

$$G_i = \frac{F(X_i + \Delta X_i) - F(X_i)}{\Delta X_i} \qquad i = 1\text{, Number of design variables}$$

2.3.4 Search Logic

Four separate serach techniques will be mechanized for possible selection by the user. The first is the Davidon Variable Metric Method for Minimization which is a multivariable unconstrained technique. It utilizes the gradient and an approximation of the matrix of second partial derivatives to locate the minimum. The second technique is the Rosenbrock Rotating Coordinate Method which locates the unconstrained minimum of a multivariable function without the direct calculation of the gradient. The third technique is the one-variable Fibonacci method which locates the minimum of an unimodel function within a specified interval. The fourth technique is the two-variable Fibonacci method which locates the minimum within a specified region by obtaining the minimum of a series of one-variable solutions. In fulfillment of the ADTECH III and IV contracts (References 12 and 13), Avco reviewed the state of the art in optimizing nonlinear functions subject to nonlinear constraints. It was concluded that there is no technique which has simultaneously the characteristics of superior reliability and superior efficiency for all types of functions. The effectiveness of a given optimizer frequently depends on the depth of understanding that the user has of the mathematical characteristics of the function currently being optimized. This understanding is implemented through selections of starting designs, control constants, and stopping tolerances. The optimizers being proposed for this program have been formulated with the dual objectives of allowing initial studies to be performed with minimum required input and allowing continuing studies to be performed more efficiently with input best suited to the situations at hand.

Of the optimizers investigated in the ADTECH studies, four were selected for incorporation into the Optimum Decoy Design Program (Section 2.4). The Davidon Variable Metric Method is judged to be one of the most suitable optimizers from the class of gradient methods while the Rosenbrock Rotating Coordinate Method is one of the most suitable from the class which does not calculate the gradient directly. Each of these techniques had advantages and disadvantages and neither is superior for all problems. Rather than arbitrarily select one or the other, both have been mechanized and the user may select either based on his experience with his problem. The two Fibonacci techniques are provided as options for the special situations where one- or two-variable optimizations are required to be solved with high reliability.

The four proposed search techniques will be discussed in more detail in the following sections.

2.3.4.1 Davidon Method

The Variable Metric Method for Minimization is a multivariable technique which uses special gradient methods to locate unconstrained minimums or zeros of a function. A simplified flow chart of the Davidon Method is shown in Figure 14.

This method is a modified gradient technique having more sophistication than the first-order steepest-descent methods and far less computational requirements per step than the second-order gradient methods. The program requires an initial starting coordinate (initial design point), X^P, an estimate of the inverse of the matrix of second partial derivatives of the function with respect to the design variables, H, and a procedure for evaluating the function, F, and its gradient, G. The Davidon method selects a step size, λ, and a search direction based on the modified gradient, HG. The next design to be evaluated, X, is determined from the matrix equation:

$$X = X^P - \lambda HG$$

The step size is estimated by the program (based on the value of the function, the gradient, and the estimate of H) to overstep or bracket the minimum along the search direction. If the minimum has been bracketed, an interpolation is made for the approximate minimum. Based on the behavior of the function during the overstep and the interpolation, the metric H is modified and the process is repeated from the best point available. The identity matrix is typically used for the initial estimate of H unless other information is available.

It is the use of first-order calculations (gradient) to improve the estimate of the second-order parameter H which gives the Davidon technique its power and efficiency. If the penalty function becomes zero, an acceptable design has been obtained and the problem is complete. If the transformed-gradient becomes less than a tolerance, ϵ , a nonzero minimum has been located. This implies that it is not possible to reduce the function further.

If the estimated step size does not bracket the minimum, the Davidon program modifies the H matrix and selects a new search direction. An alternate approach which is more consistent with the basic theory is to change the estimated step size until the new point does bracket the minimum. Although this approach is theoretically sound, actual experience in running both approaches has indicated that the original approach is faster for most problems.

Another variation away from the basic theory is included in the program at the point where the minimum in the search direction has been bracketed. Calculations are made to estimate whether the function is behaving in such a way that a "perpendicular" step would be more advantageous than back-tracking to interpolate for the minimum in the search direction. This possibility is attractive because of the characteristics of certain functions. Safeguards are

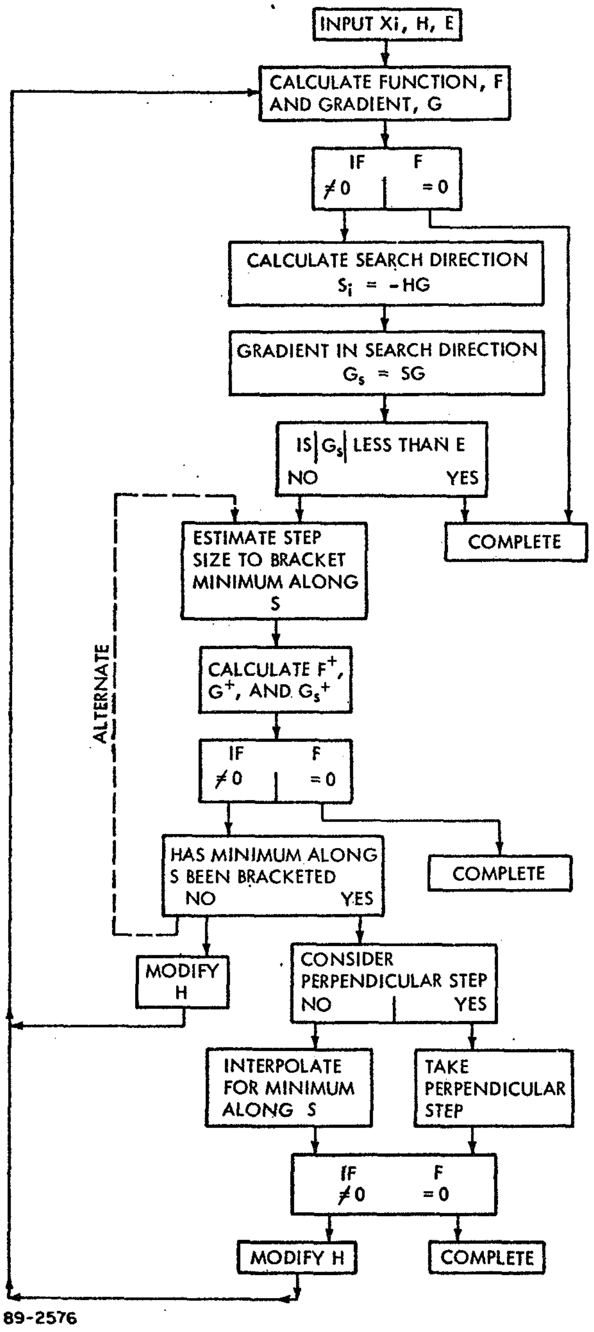


Figure 14 SIMPLIFIED DAVIDON FLOW CHART

included in the program so that the process is stable. For example, if the perpendicular step is worse than expected, the program returns to the normal logic and interpolates for the minimum in the search direction.

The program, as currently mechanized, differs from the description in the Ref. 16 with regard to the limits on the maximum size of the step length, λ. In the program the step length is:

$$\lambda = \text{smaller of} \begin{cases} 2.0 \\ -M\,(f/gs) \end{cases}$$

where M is an input which may be adjusted by the user

The random step operations described for subroutine STUFF (Ref. 16) have not been mechanized since they would tend to interfere with the sequential constrained optimization process.

The Davidon technique has been applied to several functions in order to investigate its capabilities and limitations in the solution-finding mode. There are a number of classical check problems in the optimization literature which have been intentionally designed to emphasize the weaknesses of various optimization techniques. For this study, these functions have been modified to include the features of the penalty function equation. The check cases have been graded in various levels of difficulty. One of the most difficult two-dimensional functions is one developed by Rosenbrock (see Reference 17), which has a narrow curved valley with steep sides. The problem is to start from various points and search for the region of acceptable solutions.

An example of the search path obtained using the Davidon method is shown in Figure 15. In Figure 15, the search is started on one of the constraints. For this check case, it was necessary for the optimizer to calculate the function and the gradient at 8 points. Since this is a two-dimensional problem and since finite difference techniques are being used to calculate the gradient, three evaluations of the function are required at each point for a total of 24 evaluations.

The number of function evaluations required for each check case are labeled "time units" in the figures.

Another example is shown in Figure 16. The Davidon technique in an optimization mode is applied to a quadratic function. For each of the points labeled in the figure, three evaluations of the function are performed in order to obtain the function and the gradient. The Davidon technique is particularly efficient for quadratic or nearly quadratic functions.

2.3.4.2 Rosenbrock Method

The Rosenbrock Rotating Coordinate Minimization Technique (Reference 17) is an algorithm for selecting trial values for the input parameters of a given system model in such a way that a function of the performance of the system is optimized.

FIGURE 15

EXAMPLE OF DAVIDON TECHNIQUE APPLIED TO A CONSTRAINED ROSENBROCK FUNCTION WITH STARTING POINT AT (0.5, 1.5)

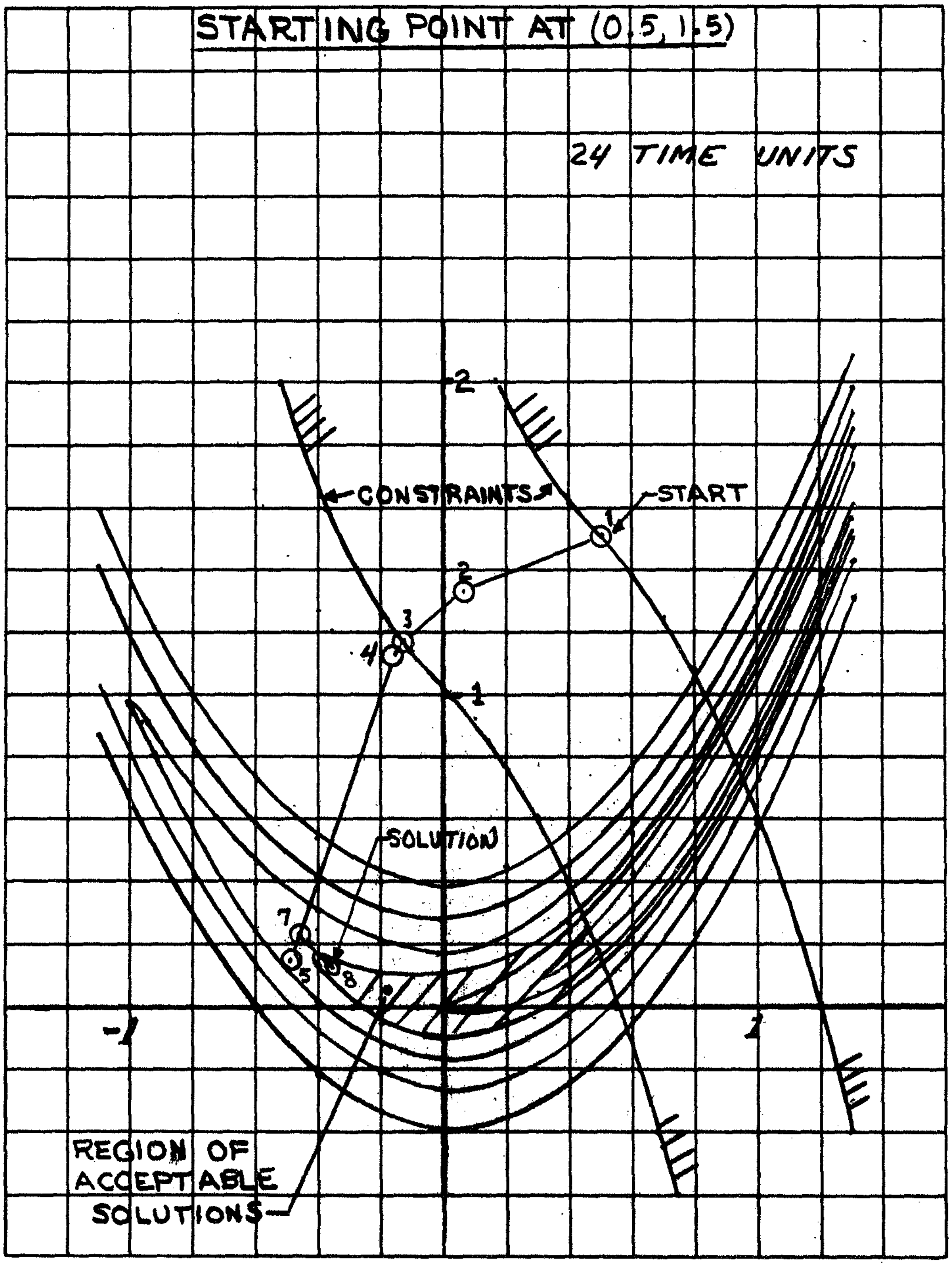
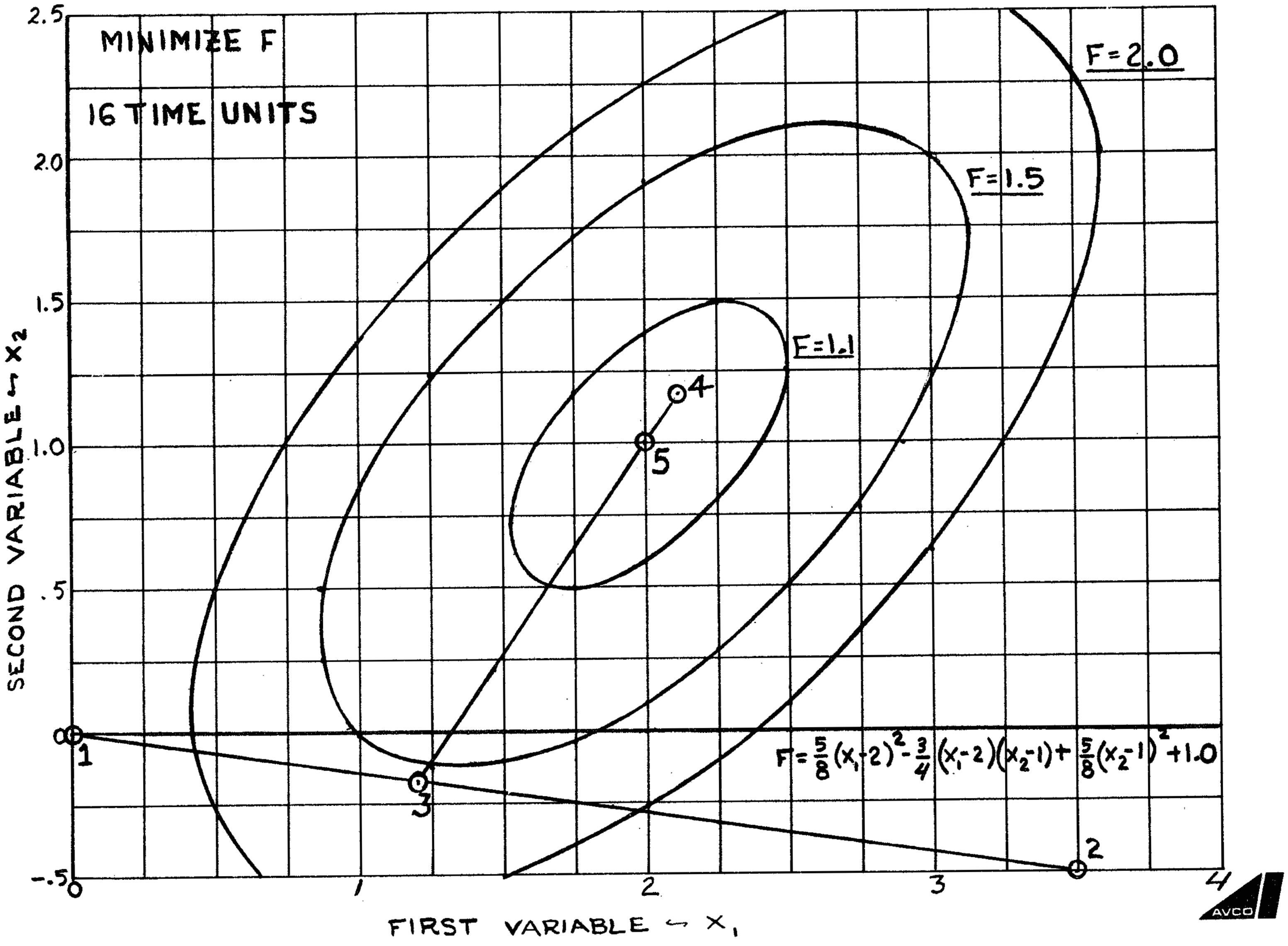


FIGURE 16

EXAMPLE USING DAVIDON'S TECHNIQUE



The technique is referred to as "rotating coordinates" because of the fashion in which the variables are perturbed. Rather than varying the input parameters of the system model one-at-a-time, this method rotates the coordinate system in parameter space so that one axis points in the "best" direction of search. The remaining axes for exploration, which are mutually orthogonal, are obtained with a Gram-Schmidt orthogonalization procedure. A search is taken along each of these directions one at a time using the logic which is described below, and then a new set of axes are developed. Flow charts for the technique are shown in Figures 17 and 18.

The search technique involved consists of taking trial steps along each of the coordinate axes. The trial is a "success" if the functional value is less than the value on the previous trial; otherwise it is a "failure." The step sizes are determined in the following manner. An initial step size (ΔX) is an input quantity. After a successful trial, the length of the previous step is multiplied by a constant a, ($a > 1$) and this is added to the previous value used to locate the next trial. After a "failure," the previous step size is multiplied by -B ($0 < B < 1$) and this is added to the previous value. If this stepping procedure produces a functional value within a specified tolerance level (TØL) of the previous functional value the step is called a "success." The trials in a given direction are complete when there has been a "success" followed by a "failure." The initial step in the new search (i.e., after the rotation of the coordinate axes) is dependent upon the total of the successful steps from the previous search. In particular, if d_n is the algebraic sum of all successful trials in the n^{th} direction, then the initial trial of the next search in the n^{th} direction will be $y\, d_n$, ($y > 0$), where y is a preset constant. Although all of the above constants, a, B, y, TØL, are preset, they may be input as different values to suit the need of a particular problem.

After a set of trials has been completed in one direction, the program searches along the next orthogonal direction until all N directions have been treated. A new set of directions is then calculated. All of the trials along the N directions and the subsequent calculation of a new set of directions is called a "stage."

The rotating coordinate axes are related to the parameter axes by the direction cosine matrix $[C_{\ell n}]$, with which steps in a given direction can be resolved into parameter changes. For the first stage, $[C_{\ell n}]$ is a unit matrix so that each step, e_n, corresponds to a change in only one of the system parameters X_{ℓ}. For each subsequent stage, a new direction cosine matrix is computed using the Gram-Schmidt procedure as follows;

Let $\bar{\xi}_1^{\,o}$, $\bar{\xi}_2^{\,o}$, ..., $\bar{\xi}_N^{\,o}$ be the set of orthogonal unit vectors defining the directions in the original stage. Suppose that d_1 is the algebraic sum of all successful steps in the direction $\bar{\xi}_1^{\,o}$, etc. Then define the set of vectors:

$$
\begin{aligned}
\bar{A}_1 &= d_1 \bar{\xi}_1^{\,o} + d_2 \bar{\xi}_2^{\,o} + \cdots + d_N \bar{\xi}_N^{\,o} \\
\bar{A}_2 &= \phantom{d_1 \bar{\xi}_1^{\,o} +{}} d_2 \bar{\xi}_2^{\,o} + \cdots + d_N \bar{\xi}_N^{\,o} \\
&\vdots \\
\bar{A}_N &= \phantom{d_1 \bar{\xi}_1^{\,o} + d_2 \bar{\xi}_2^{\,o} + \cdots +{}} d_N \bar{\xi}_N^{\,o}
\end{aligned}
$$

The orthogonal unit vectors $\bar{\xi}_1^{\,1}$, $\bar{\xi}_2^{\,1}$, ..., $\bar{\xi}_N^{\,1}$ for the next stage are now obtained using the following vector equations:

$$\bar{B}_1 = \bar{A}_1$$

$$\bar{\xi}_1^{\,1} = \bar{B}_1/|\bar{B}_1|$$

$$\bar{B}_2 = \bar{A}_2 - (\bar{A}_2 \cdot \bar{\xi}_1^{\,1})\bar{\xi}_1^{\,1}$$

$$\bar{\xi}_2^{\,1} = \bar{B}_2/|\bar{B}_2|$$

$$\vdots$$

$$\bar{B}_N = \bar{A}_N - \sum_{j=1}^{N-1} (\bar{A}_N \cdot \bar{\xi}_j^{\,1})\,\bar{\xi}_j^{\,1}$$

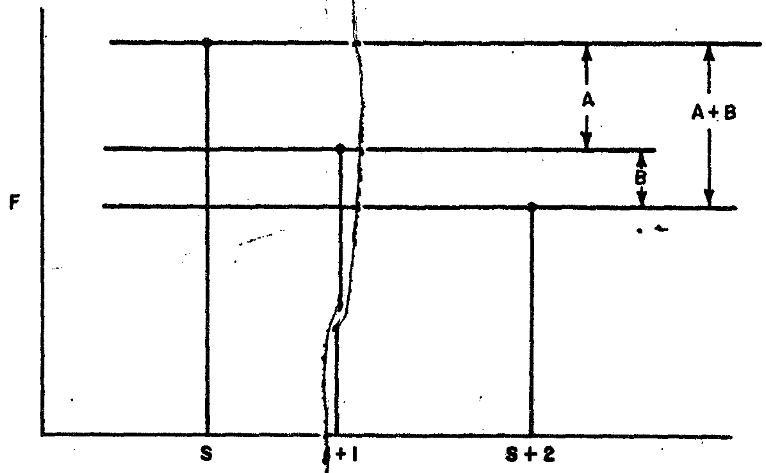
$$\bar{\xi}_N = \bar{B}_N/|\bar{B}_N|$$

The new direction cosine matrix is obtained by taking the transpose of the matrix comprised of the components of $\bar{\xi}_N^{\,1}$ along the parameter axes. With the new coordinate system defined, the search is repeated in each of the new directions in turn. The result of applying these equations several times is to ensure that $\bar{\xi}_1$ lies along the direction of fastest advance, $\bar{\xi}_2$ along the best direction which can be found normal to $\bar{\xi}_1$ and so on.

The stopping logic is based on the value of the function. For a value of the function that is undefined, an error message is printed out and the search is stopped. The same thing happens if the total number of function evaluations for a given set of constraints equals an input limit. If the value of the function is zero or if three succeeding functional values are within a defined interval of each other, a solution is considered to have been found. Considering the diagram below, the intervals for successive functional values which define a solution are

$$(F_s - F_{s+2}) < \text{DEL}\; F_s \quad \text{and} \quad \frac{F_{s+1} - F_{s+2}}{F_s - F_{s+1}} < \text{RATU}$$

where DEL and RATU are input limits.



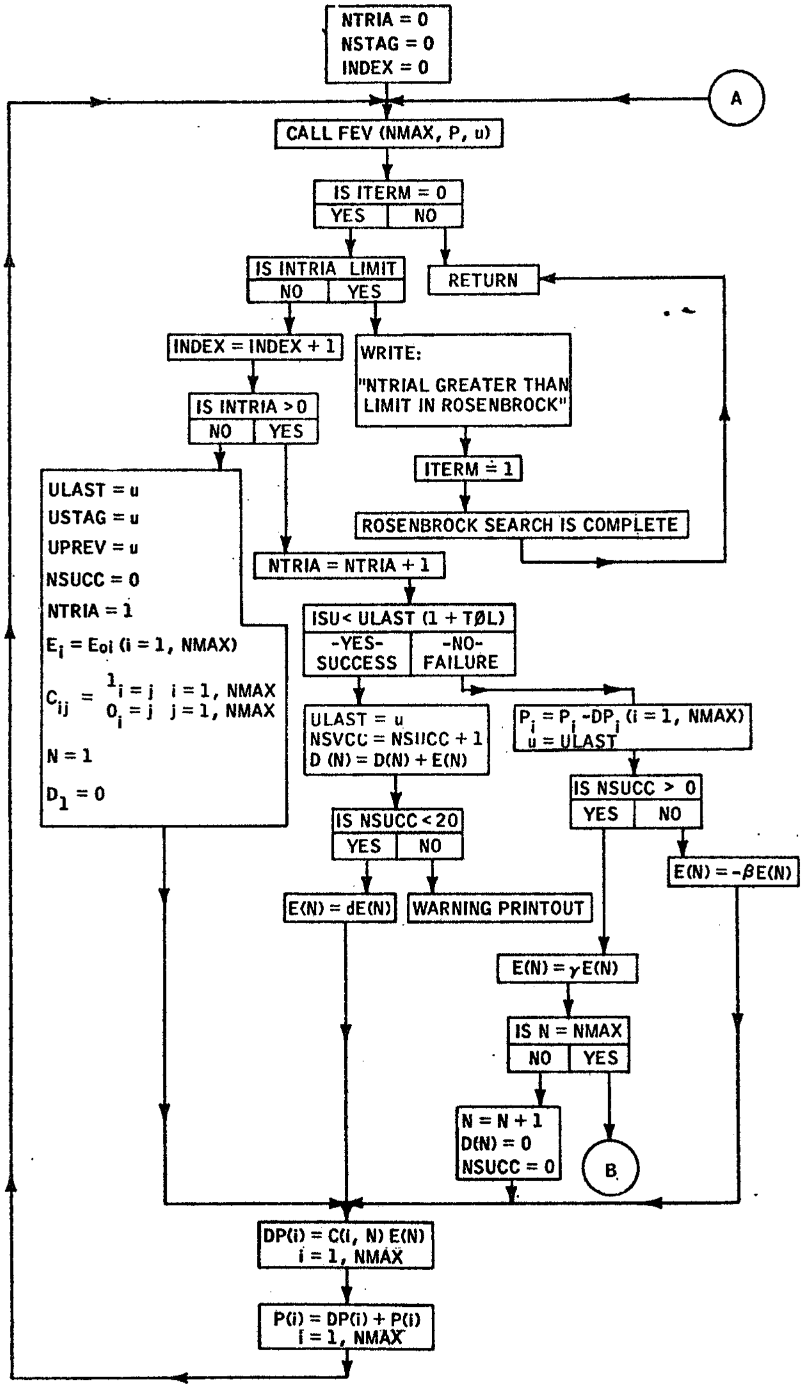


Figure 17 ROSENBROCK FLOW CHART, PART 1

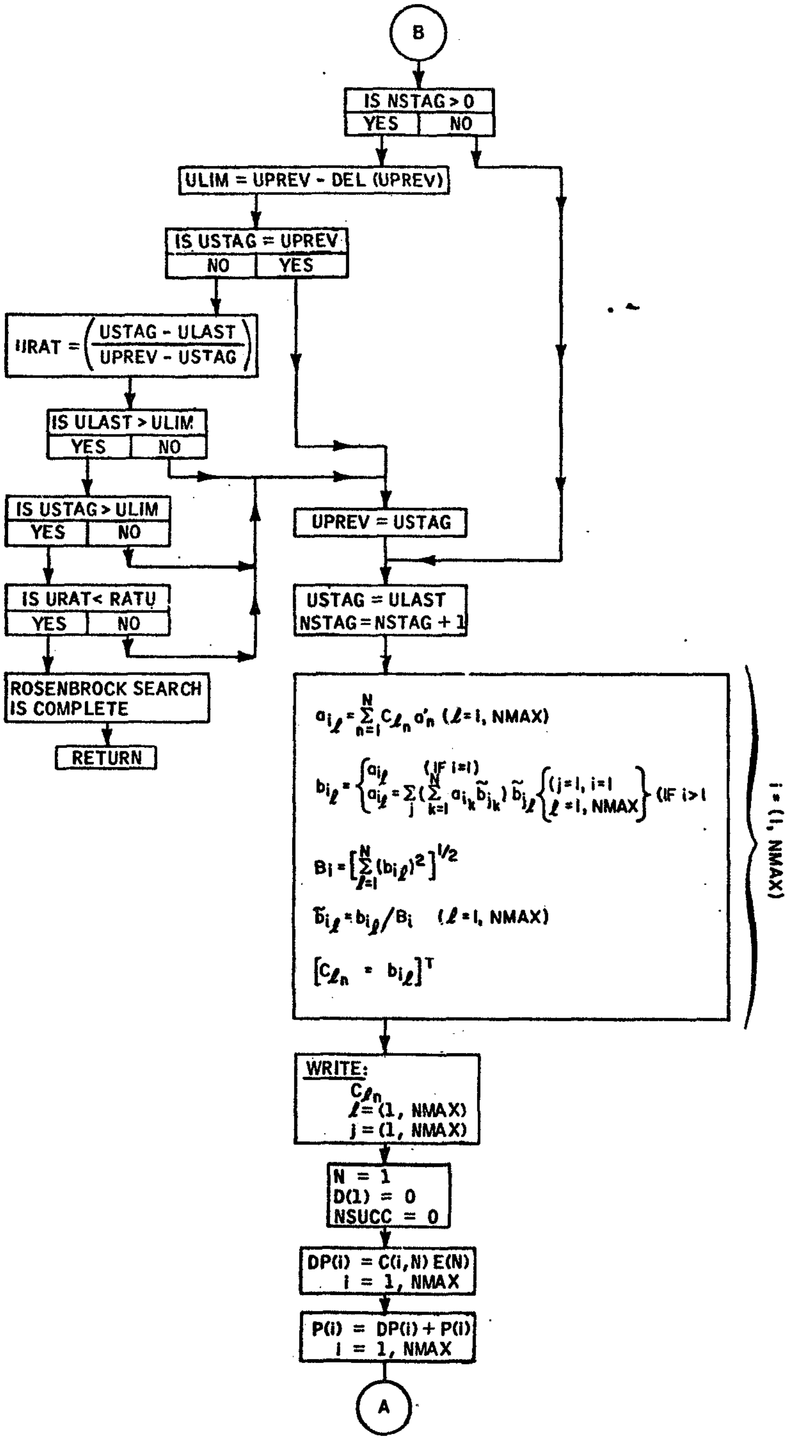


Figure 18. ROSENBROCK FLOW CHART, PART 2

The functional values, F_s, F_{s+1}, F_{s+2}, are those obtained when the trial steps have been completed for all the system orientations.

Figure 19 illustrates the operation of the Rosenbrock Method in an unconstrained optimization mode. A total of 35 trials organized in 4 stages (coordinate systems) are required to obtain the optimum and meet the stopping criteria. Eleven selected trials are shown in Figure 19 to illustrate the coordinate rotations and general pattern of the trials.

2.3.4.3 One-Variable Fibonacci Method

The Fibonacci search technique is a search scheme for finding the maximum or minimum of a one-variable function within defined limits. The function has to be at least piecewise continuous, single valued, and also have only one optimum (i.e., maximum or minimum) within the interval. These restrictions define a unimodal function (pp. 10-13 of Reference 18). , The initial interval, L_1 , is defined by an upper bound, B, and a lower bound, A , where

$$L_1 = B - A$$

Either the number of function evaluations, F, to be made during the search or an end-of-search accuracy limit, A_c, defined in terms of a number of independent variable units away from the actual maximum or minimum within the interval has to be given.

The technique is based on direct comparison of values of the function, which are used to exclude parts of the search interval. The placement and comparison of the points is continued until the interval is sufficiently small or until the function is zero. The points are located so as to maximize the interval to be excluded at each step.

The location of the first two points in the initial search interval is dependent upon the total number of function evaluations to be made during the search. If the accuracy is given, a trial Fibonacci number, F_{NT}, is defined

$$F_{NT} = \frac{L_1}{A_c}$$

The actual Fibonacci number is obtained through an iteration process where

$$F_1 = 1$$

$$F_2 = 2$$

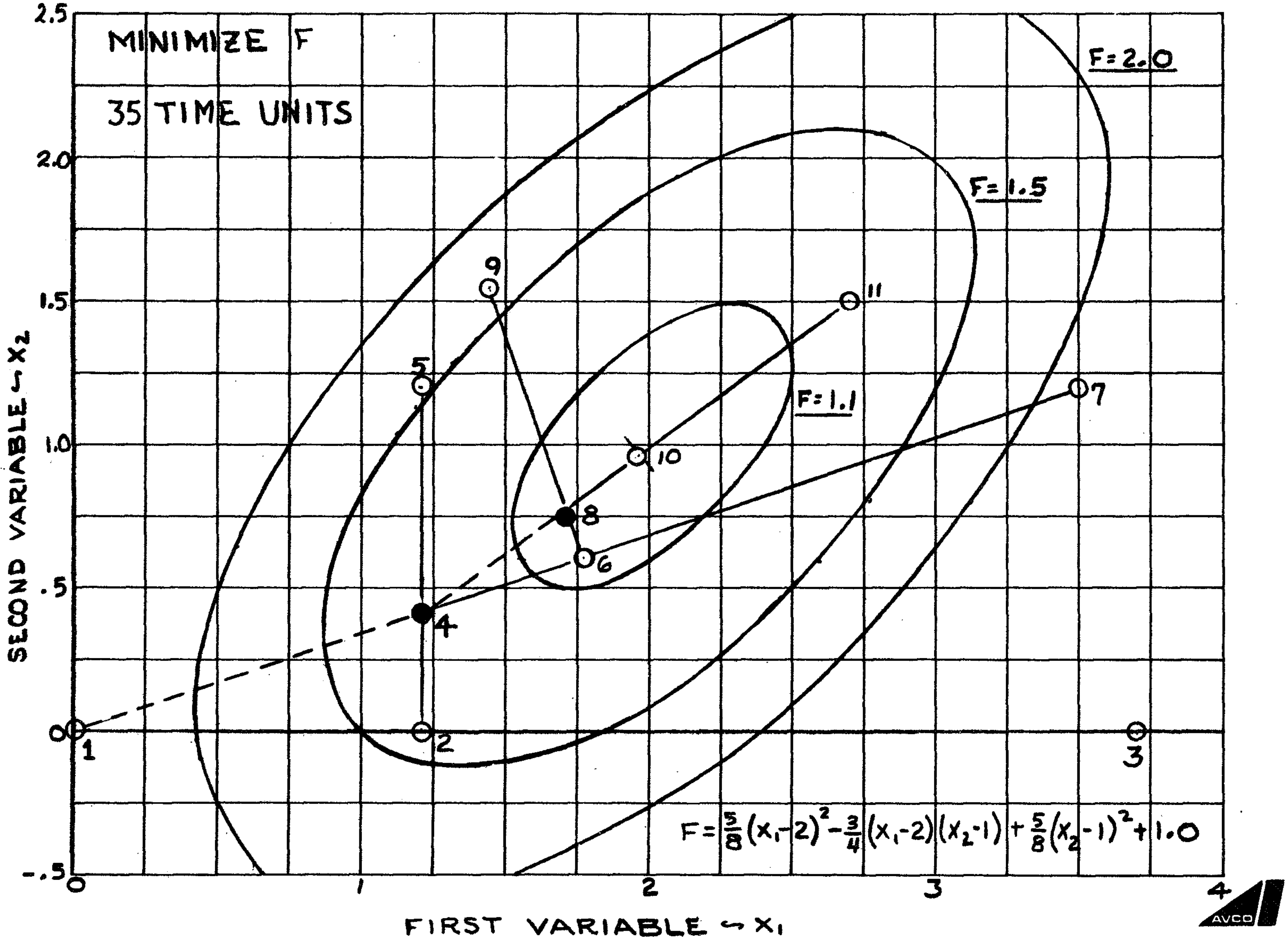
$$F_n = F_{n-1} + F_{n-2} \qquad n = 3, 4, 5, ---$$

The iteration process is continued until the first value of n at which $F_n \geq F_{nT}$ is found. The number of function evaluations to be used within a given accuracy limit is then:

$$N_F = n - 2$$

FIGURE 19

EXAMPLE USING ROSENBROCK'S TECHNIQUE



Likewise, if the number of function evaluations is given the associated Fibonacci number is found by applying the above process in reverse order.

The two evaluation points in the first interval are located as follows:

$$X_1 = A + \left(\frac{F_{n-1}}{F_n}\right) L_1$$

$$X_2 = A + \left(\frac{F_{n-2}}{F_n}\right) L_1$$

and the corresponding functional values, Y_1 and Y_2 are computed. Comparing the two functional values and choosing one of the associated evaluation points to be a new end point yields a new interval for computing the next evaluation point. For instance, in the search for a maximum the evaluation point associated with the smallest functional value becomes an end point for the new interval containing the other evaluation point and the remaining end point. Then a new evaluation point is placed in the new interval a distance of ΔX units from the end point retained from the previous interval.

$$\Delta X = \left(\frac{F_{n-j}}{F_n}\right) L_1 \qquad j = 3, 4, ---, N_K$$

where the subscript j is the number of the particular evaluation point being found for that interval. The new functional value for the interval is computed and compared with the functional value retained from the previous interval so that a new interval can be determined. This process is repeated until the appropriate number of function evaluations have been made. The maximum or minimum of the function is obtained by directly comparing the functional value of the final evaluation point, the evaluation point retained from the last interval, and the new end point for the last interval.

2.3.4.4 Two-Variable Fibonacci Method

The Fibonacci search technique for a two-variable function in a bounded region is the application of the one-variable Fibonacci search to each variable. Taking one of the variables to be the secondary independent variable and the other to be the primary independent variable, the method employed in this technique is the optimization of the primary independent variable during each step of the optimization of the secondary independent variable. That is for each evaluation point selected during the optimization of the secondary variable, the primary independent variable is optimized. Then, the secondary value and the optimum primary value are stored in a table. This process is repeated until the desired number of evaluations have been made on the secondary independent variable. The table is then searched for the optimum secondary value, producing also the associated optimum primary value.

The restriction of unimodality (see description of one variable Fibonacci) applies in a stricter sense for the two-variable Fibonacci technique. Not only does the two-variable function have to be unimodal, but the associated one-variable functions for the one-variable Fibonacci searches must also be unimodal. For a unimodal two-variable function, whether or not the two one-variable functions are unimodal sometimes depends on which independent variable is chosen to be the secondary variable. Thus, the choice of which variable is to be the secondary independent variable is important.

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APPENDIX C

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