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A VERSATILE, LOW COST PACKAGING TECHNIQUE FOR SPACECRAFT ELECTRONICS

HARRY CHERNIKOFF

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GSFC
GODDARD SPACE FLIGHT CENTER
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ABSTRACT

The Electronic Development Branch of Goddard Space Flight Center has developed a Spacecraft Computer known as the On-Board Processor (OBP). Two packages, the Input/Output Unit (I/O) and the Central Processing Unit (CPU) were fabricated using a point-to-point wiring technique known as Micropoint. This technique, developed by Micro Technology Incorporated in California, utilizes teflon insulated nickel wire and gold plated stainless steel pins pressed into glass epoxy boards to produce high density, low cost circuit boards.

Most of the circuits in the I/O and CPU are flatpacks; this allowed the design of a standard board. The boards consist of 1/16 inch glass-epoxy double sided printed circuit (PC) material having the power plane on one side and the ground plane on the other. Ground and power pins are soldered to the PC. Flat ribbon cable interconnects the circuit boards through a single centrally located grandmother board. The flatpacks are gap-welded and discrete components are soldered to the pins. The boards are then conformal coated with polyurethane and the units are potted with clear silicone rubber.

These units have successfully completed qualification level environmental tests.

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INTRODUCTION

The Electronic Development Branch at NASA's Goddard Space Flight Center has developed a general purpose stored program computer for use in scientific spacecraft. This computer, known as the On-Board Processor (OBP) is scheduled to be launched on board the Orbiting Astronomical Observatory C (OAO-C) in 1972. The OBP consists of an Input/Output Unit (I/O), a Central Processing Unit (CPU), four Electronic Memories Incorporated SEMS 5L memories, and a power converter. The I/O and CPU units (Figure 1) were fabricated by Micro Technology Incorporated of California.

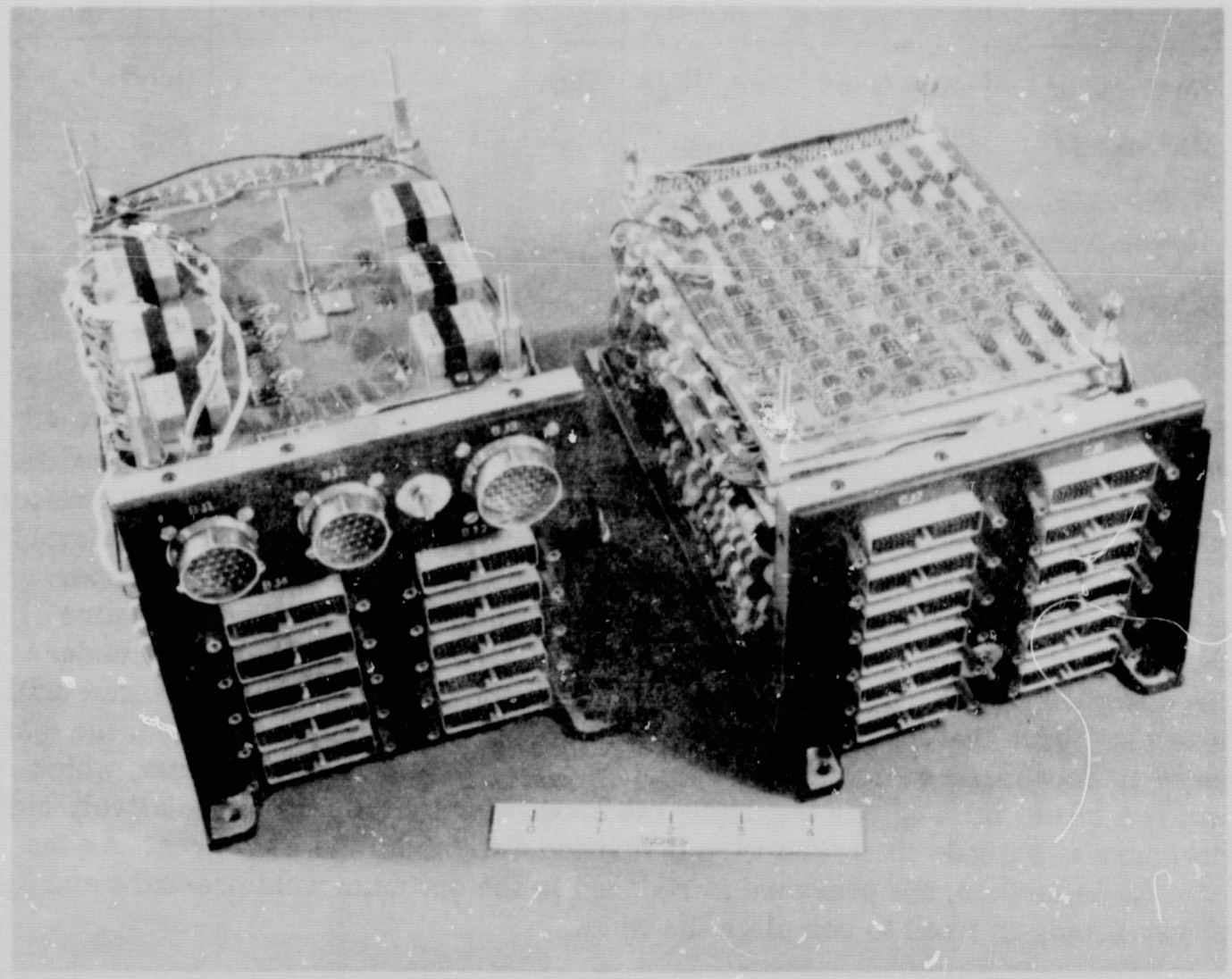

Figure 1. OBP I/O and CPU Units

The OBP development program was funded for one engineering model and one proto-flight unit. For this reason, ease of checkout and the ability to make repairs and changes without compromising reliability were prime considerations in the package design. A number of board designs were considered, including multi-layer printed circuit board, "microsticks" (flatpacks interconnected with etched nickel patterns), and multi-layer welded wire matrix. The technique chosen, known as Micropoint, appeared to meet all the requirements. Its main drawback was that it was a relatively new process. Table 1 outlines some of the trade-offs involved in the choice.

Table 1

Characteristics of Four Design Approaches Considered

	Size	Cost	Reliability	Ease of Repair	Ease of Test
Multi-layer	Very Good	Very High	High	Poor	Good
Microstick	Good	Medium	High	Poor	Fair
Welded Multi-layer Matrix	Poor	Medium	High	Fair	Good
Micropoint	Good	Low	Limited Data	Very Good	Very Good

Figures 2 and 3 show the basic materials used in the Micropoint process. Gold plated stainless steel pins are pressed into glass epoxy boards. Teflon insulated nickel wire is then welded point-to-point to the pins by means of a special welder (Figure 4). This welder consists of a fixed lower electrode and a hollow movable upper electrode controlled by a foot pedal. The wire is fed through the upper electrode as shown in Figure 5. With the aid of a stereo microscope (Figure 6) the board is positioned between the electrodes so that the desired pin is under the upper electrode. During the positioning, the upper electrode is lowered until it is just above the pin to allow exact positioning. To complete the weld, the foot pedal is depressed completely to actuate a motor driven cam. The cam, which has two lobes, first drives the upper electrode against the pin at a relatively high pressure to extrude the teflon wire insulation away from the weld area. As the cam turns further, the pressure is reduced to the optimum weld pressure and the power supply is fired to complete the weld.

The Micropoint technique has several unique advantages. All points common to a signal are connected by a single unbroken wire. The technique is relatively

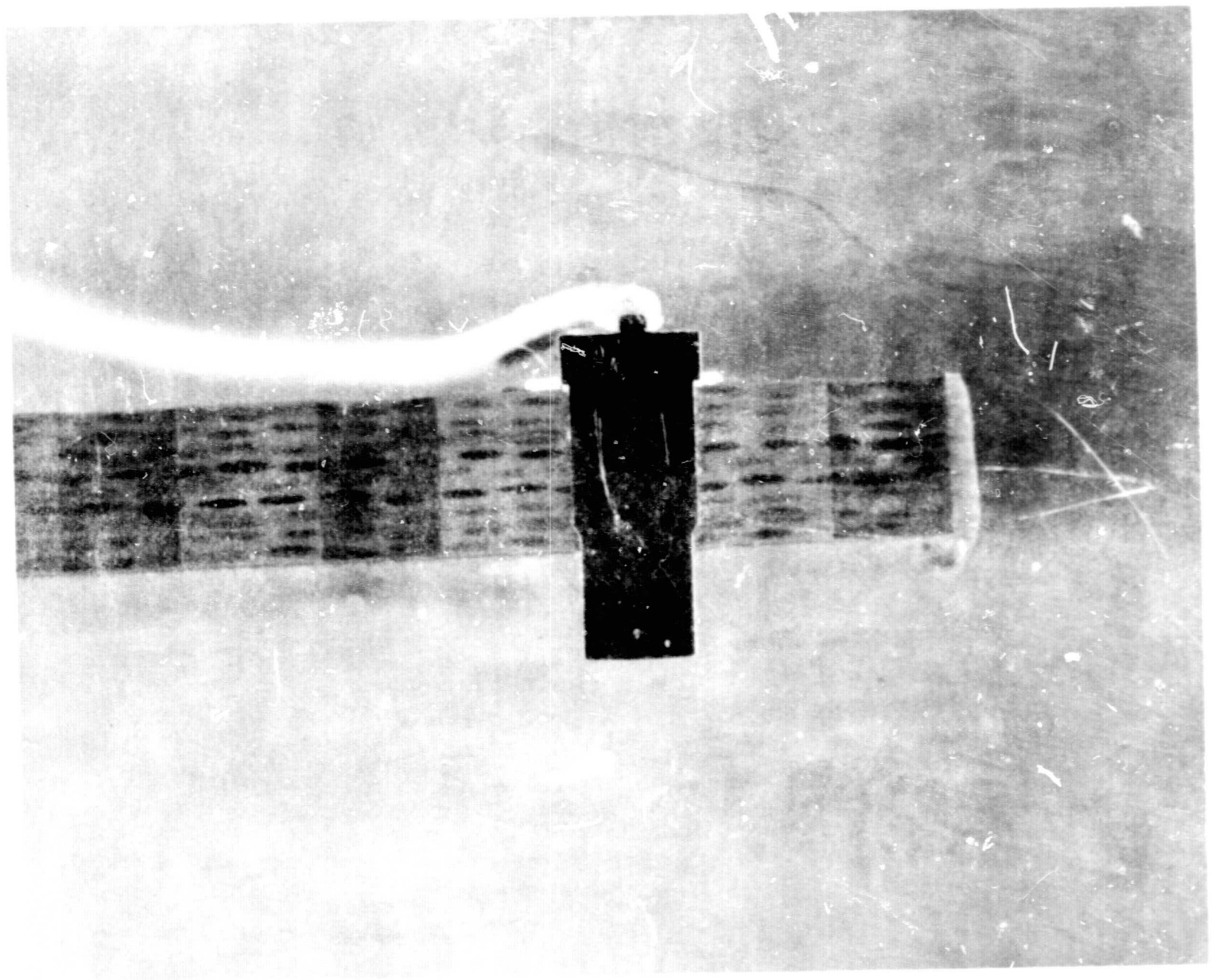

Figure 2. Basic Micropoint Materials: Board, Pin, and Wire

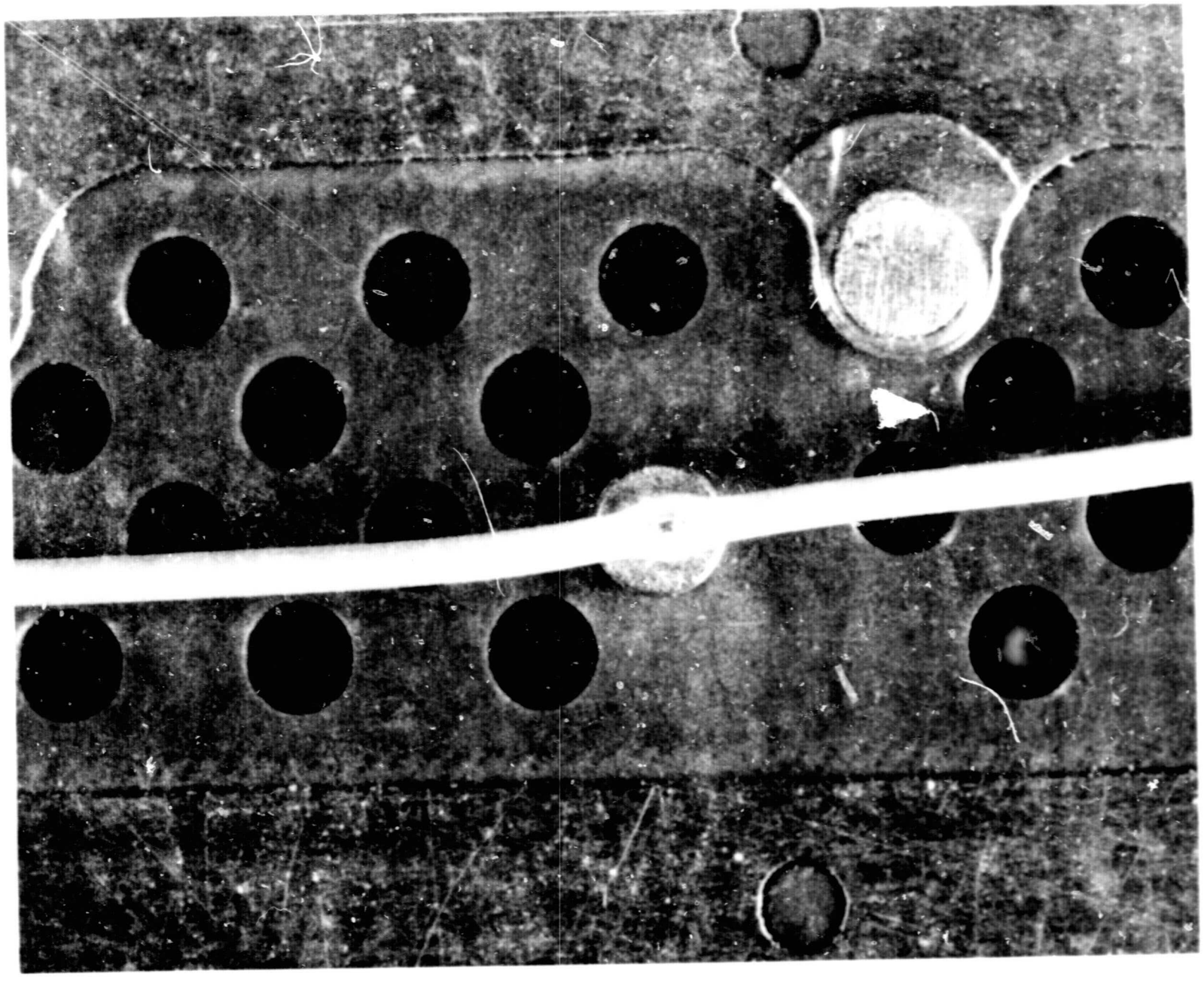

Figure 3. Typical Micropoint Connection

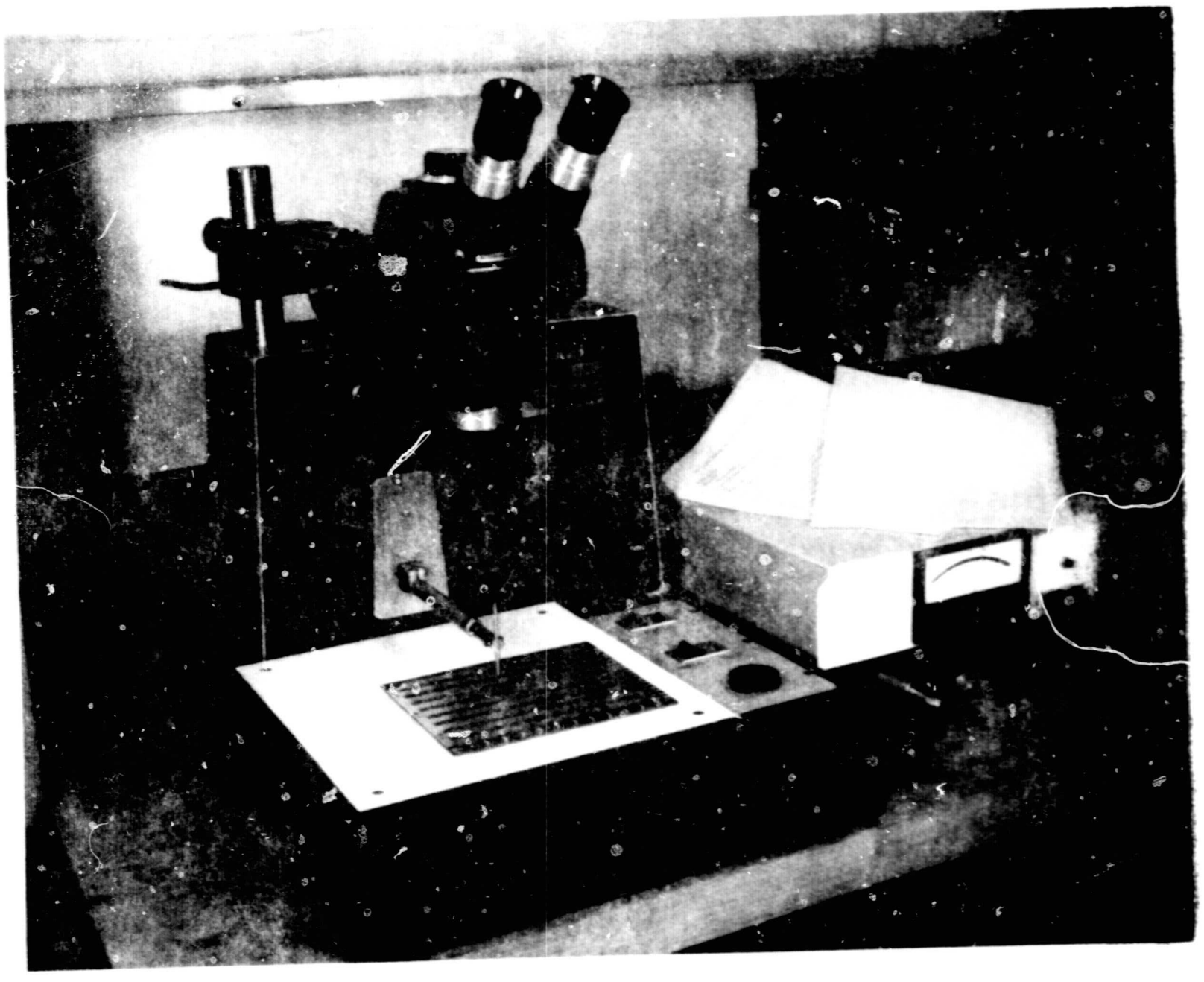

Figure 4. Micropoint Welder

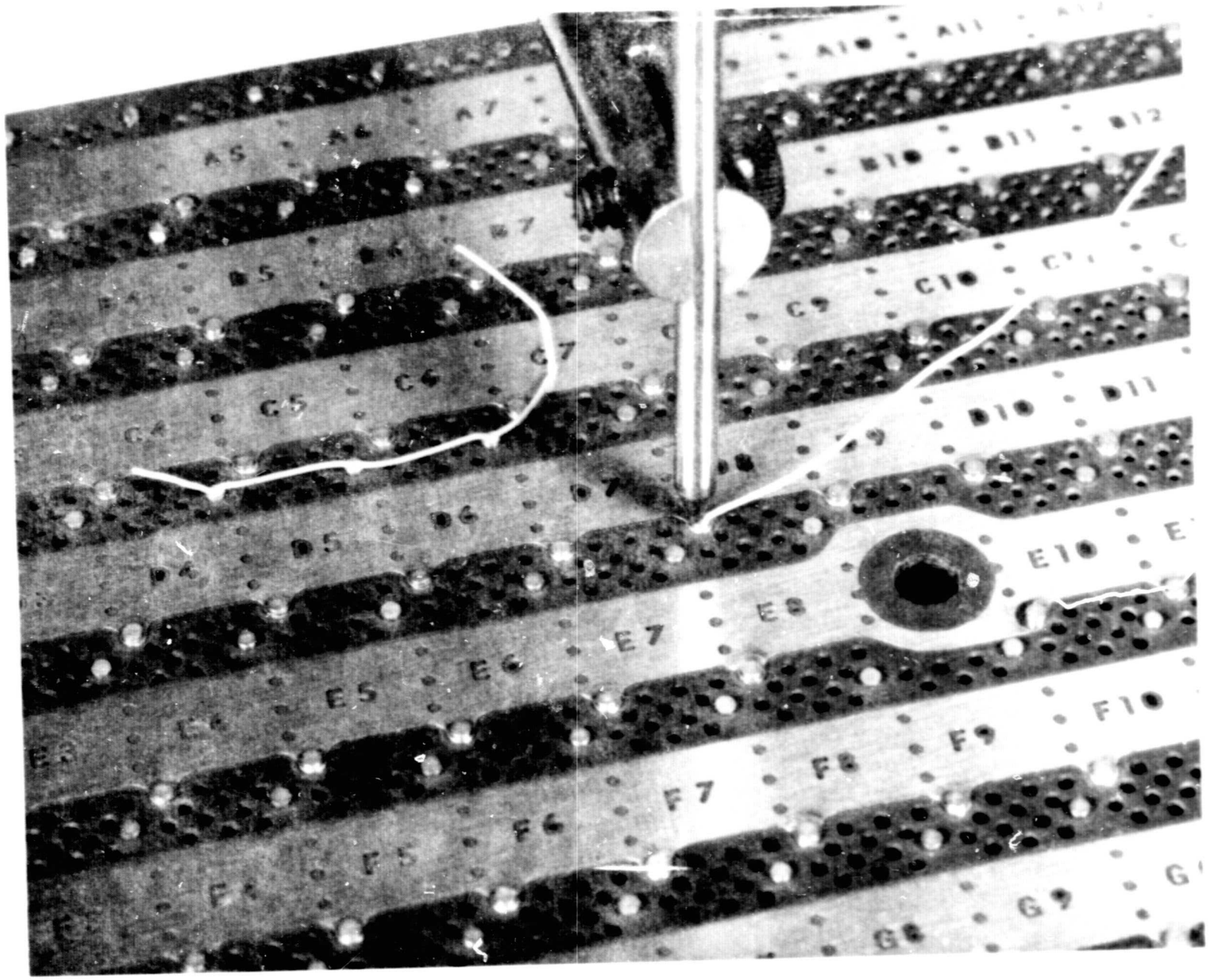

Figure 5. Micropoint Wire Feed Electrode

Figure 6. Micropoint Welding Operation

simple and involves common-place materials except for the unique welding machine. The design and tooling costs are low; the system allows standardization of card design. The operation can be automated to any extent desired, from component layout and generation of the wire list to actual positioning of the board by a Numerical Control (NC) system. Several companies have recently built NC wiring systems using this technique.

BOARD DESIGN

Since most of the circuits for both the CPU and the I/O were 14-lead flatpacks, a standard board was designed, measuring 5-1/2" × 6-1/2" and containing provision for 124 flatpacks. Figure 7 shows the wiring side, with an etched power plane. Figure 8 shows the component side with a ground plane. The board material is 1/16 inch fiberglass-epoxy printed circuit (PC) board with 2-oz. copper on both sides. The PC is appropriately extended to the ground and power pins and solder plated; then the remainder of the PC is gold plated. Originally, the power and ground pins were to be inserted and the board heated to fuse the pins to the PC; however, initial results were not satisfactory so the flight boards were hand soldered.

Figure 3 shows a closeup of a power pin after soldering. The pins are retained in the board by employing holes .001 to .002 inch undersize; this results in a retention force of about 10 pounds. The tip of the pin has a smaller diameter than the body to aid in loading. The lower edge of the board contained three rows of bifurcated pins for output leads to connectors. One narrow edge contained four rows of bifurcated pins for up to two layers of flat ribbon cable used to interconnect boards.

Figure 9 shows a completed board containing 120 flatpacks. The decoupling capacitors in the upper right corner were placed in unused locations on all boards thus requiring no modification of the standard board configuration.

Figure 10 shows a board containing a number of different flatpacks and discrete components using the standard pin arrangement; however, because of varying power and ground configurations on the flatpacks, the power and ground planes have been modified. In all cases except the board shown in Figure 11 and one other board containing mostly relays, discrete components were accommodated in the standard flatpack locations on the boards. Figures 11 and 12 show how discrete components were accommodated on a special board. Standard pins were used with the components soldered on the heads of the pins. All flatpacks were parallel-gap-welded with standard equipment.

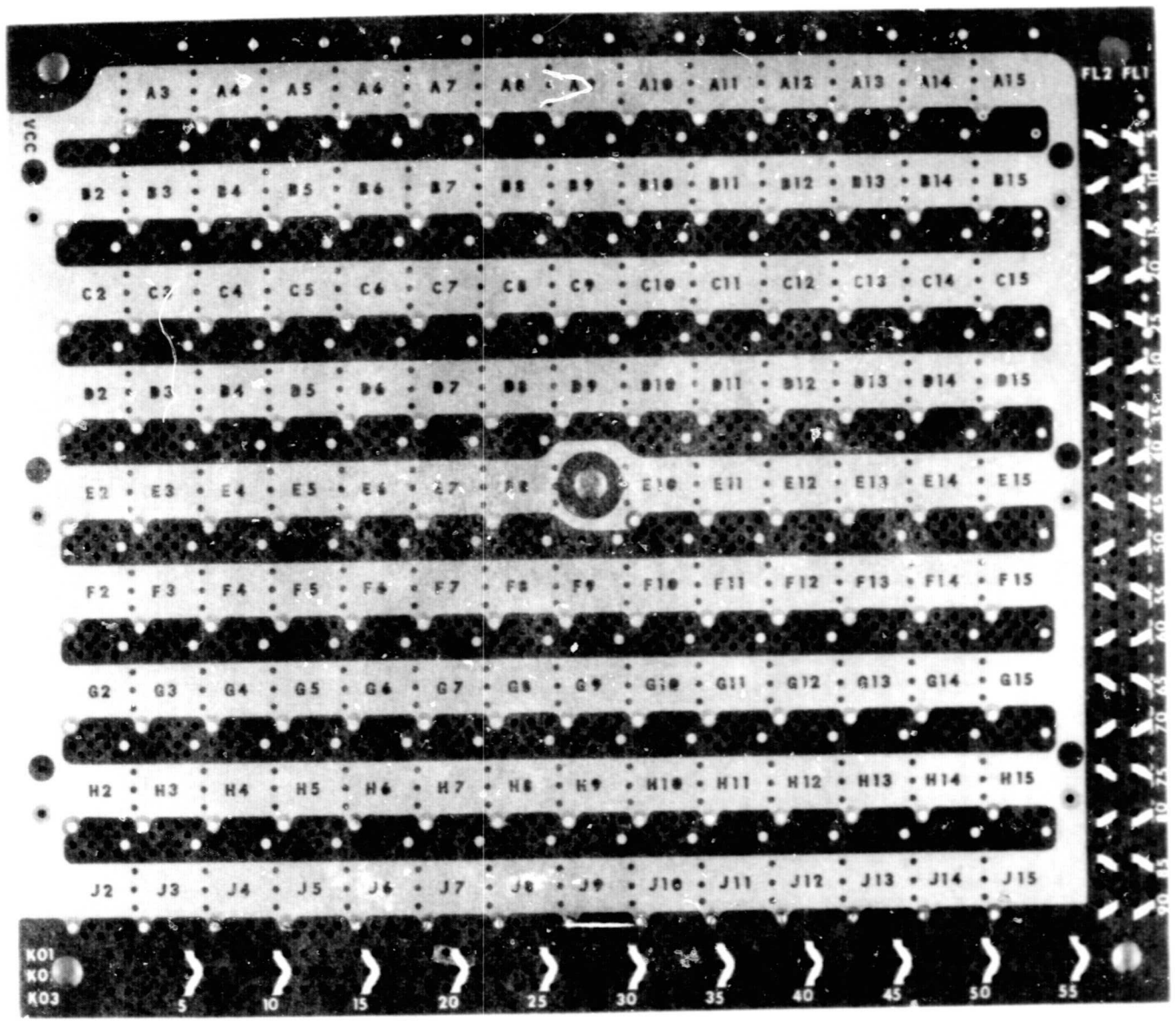

Figure 7. Wiring Side of a Typical Board With Etched Power Plane

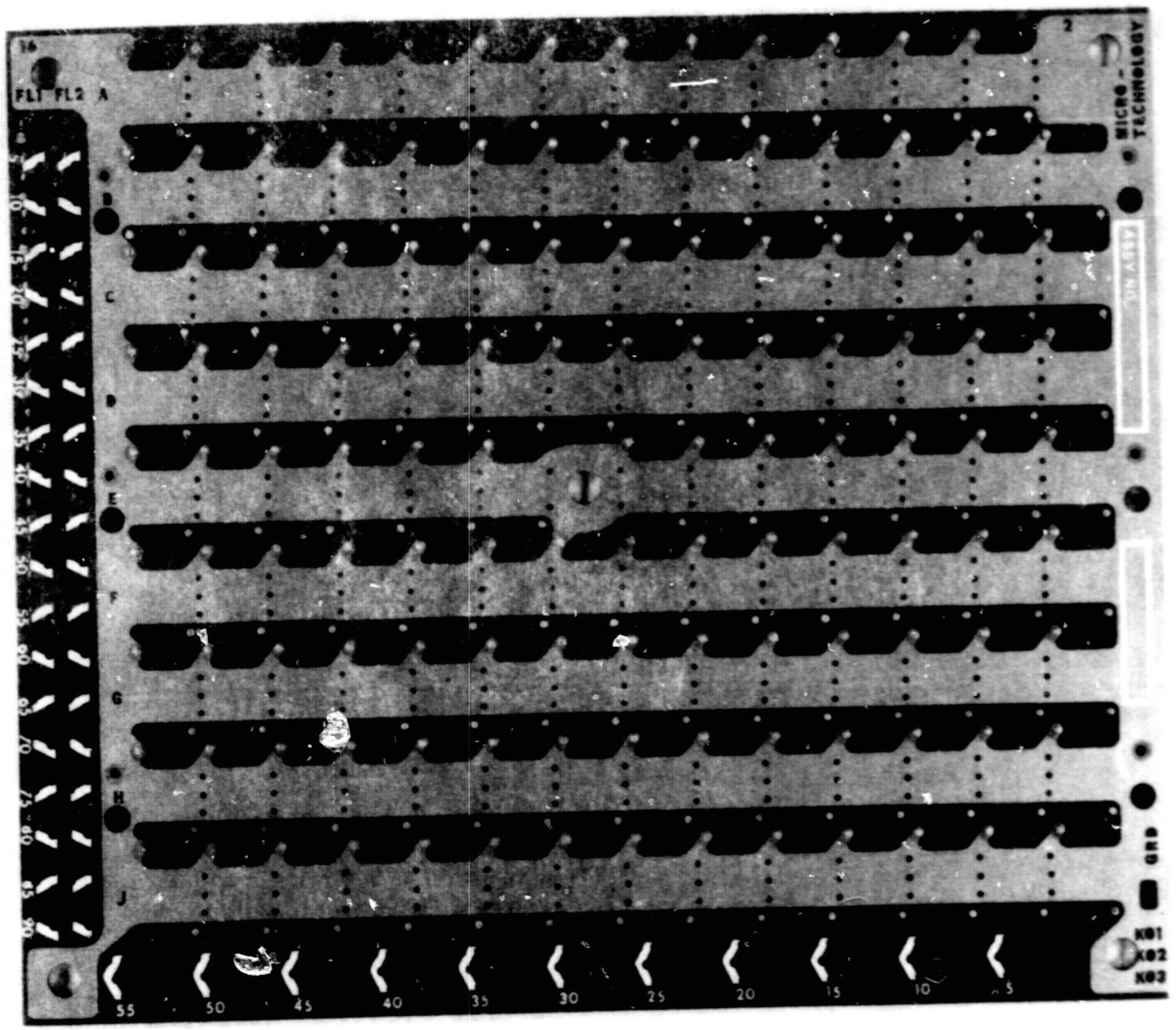

Figure 8. Component Side of a Typical Board With Etched Ground Plane

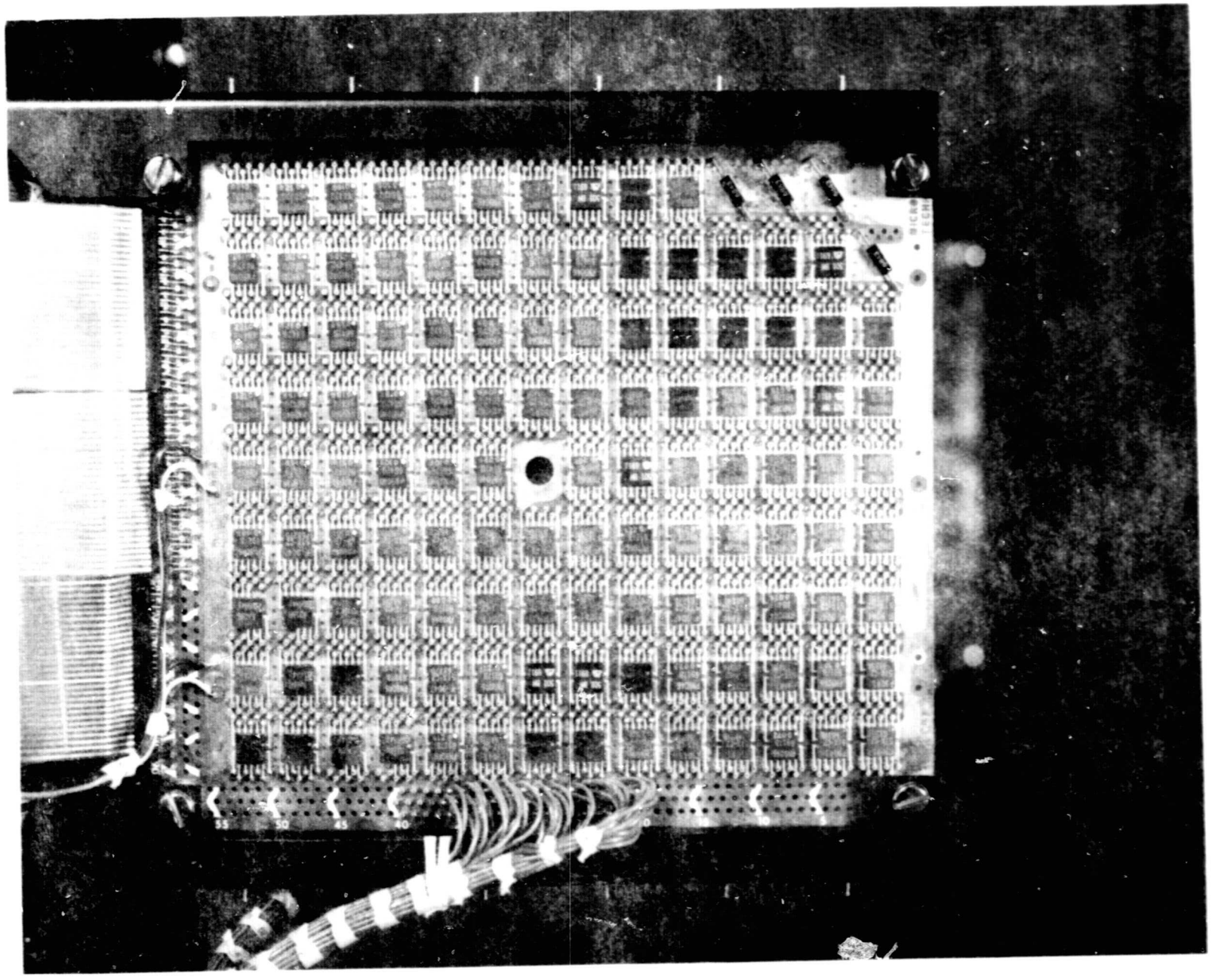

Figure 9. Completed Board Containing 120 Flatpacks

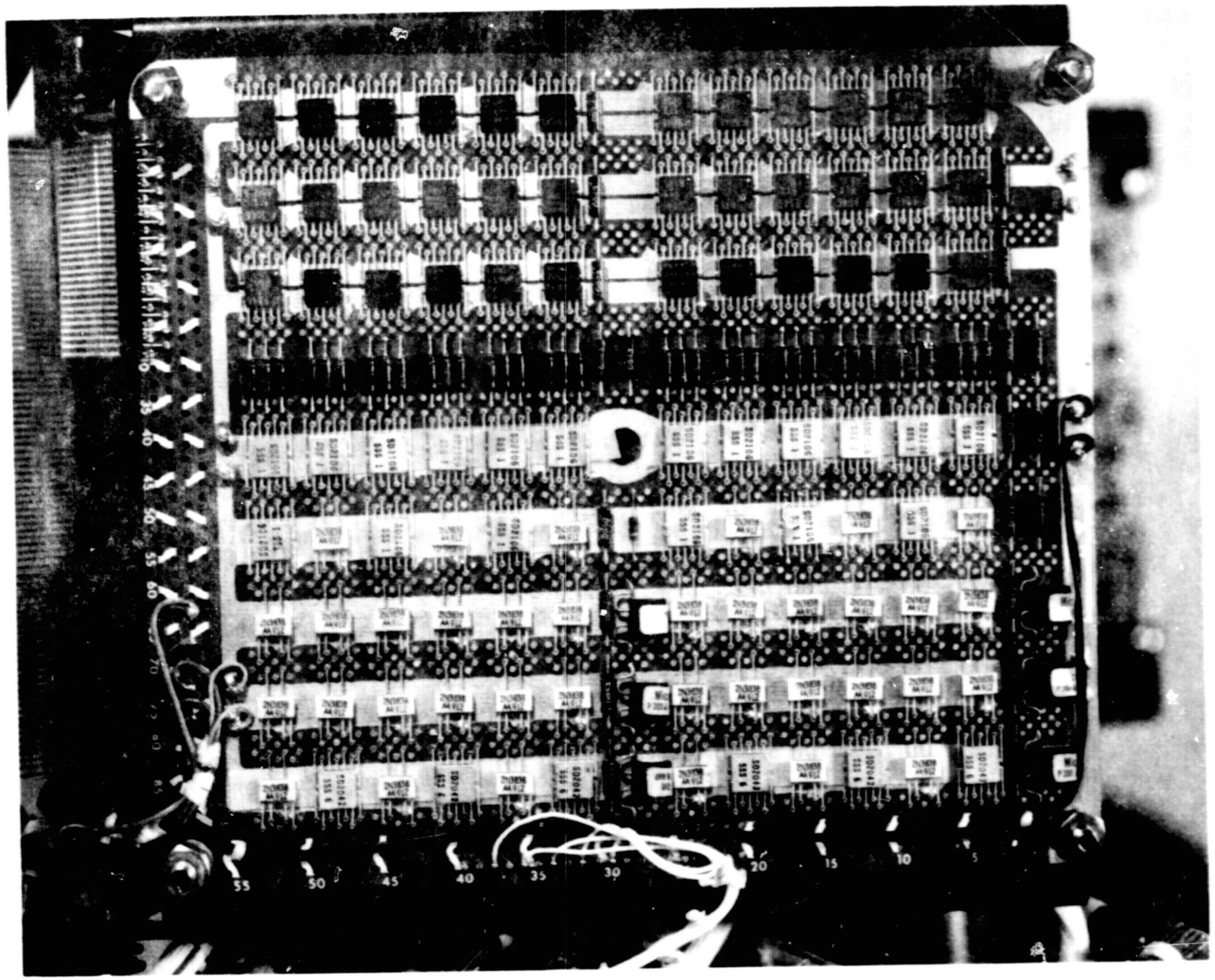

Figure 10. Board Containing Various Types of Components

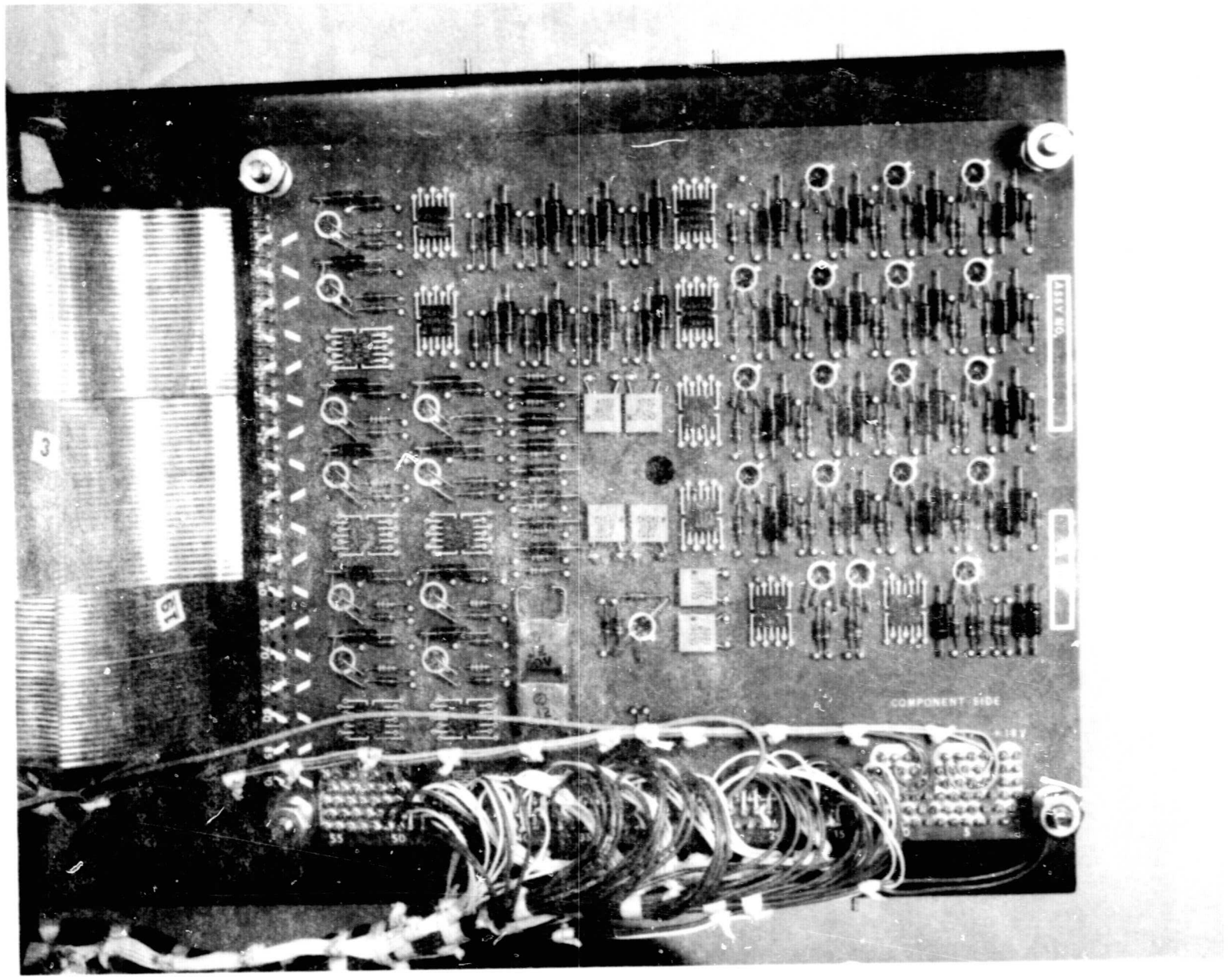

Figure 11. Component Side of Board With Discrete Components

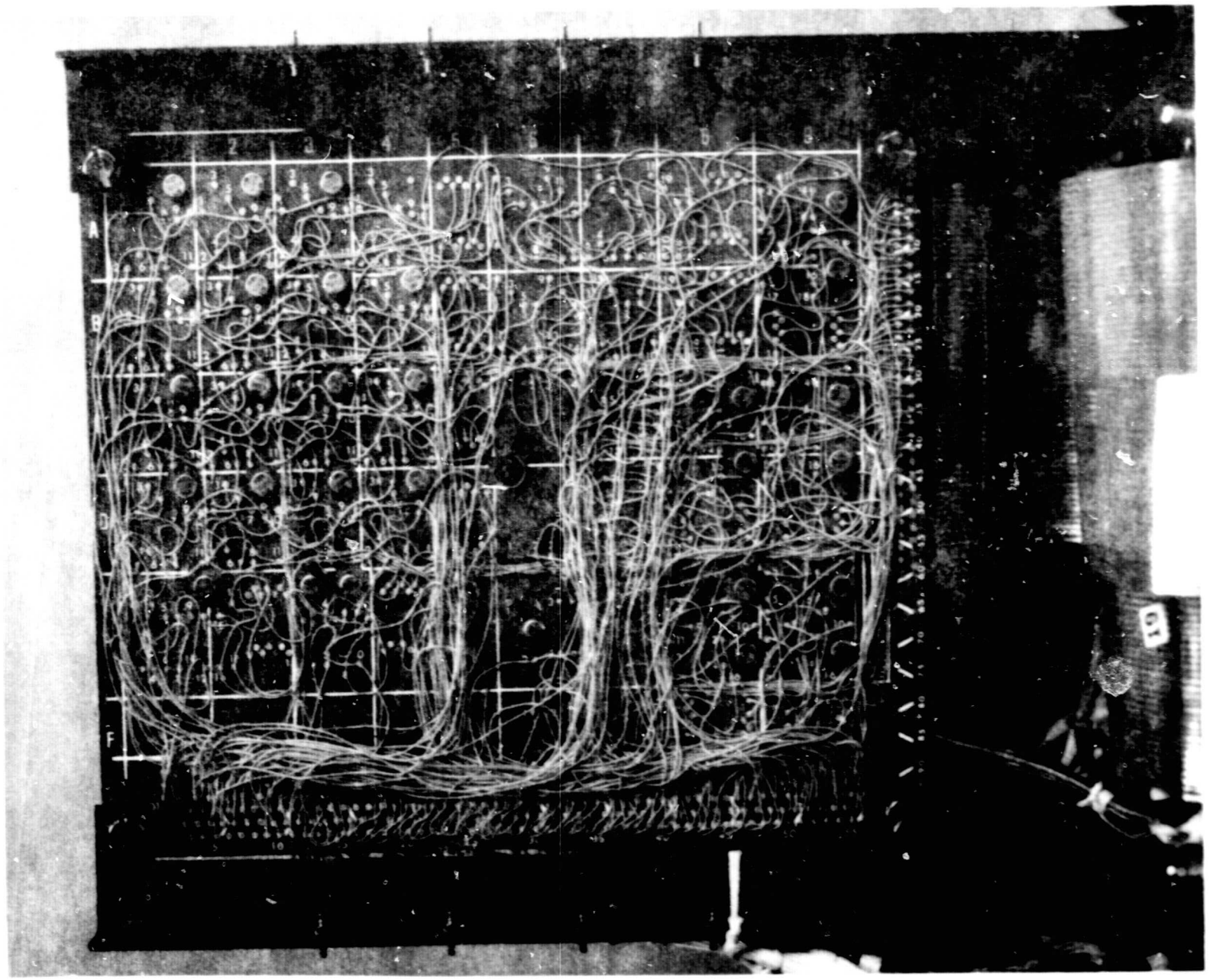

Figure 12. Wiring Side of Board With Discrete Components

GRANDMOTHER BOARD CONCEPT

Because of package size constraints and the large number of interconnects between boards, it was decided to utilize flat ribbon cable and a grandmother (granny) board concept for board interconnection. Figures 13 and 14 show the granny board. The flat ribbon cables which fan out in both directions from the granny are attached to both the granny and the logic boards by .020 inch gold plated nickel pins soldered to bifurcated pins on the boards. When folded, the granny board is in the center of the stack as shown in Figure 13. The flat cable is teflon insulated copper conductors on .050 inch centers. The .020 inch gold plated nickel pins are welded to the conductors, and the ends are potted with epoxy.

FINAL ASSEMBLY AND CHECKOUT

After the granny board was completed, the flat cables were soldered to it. Stacking was then begun, and the flat cable was soldered to each board after it was placed on the stack. Appropriate spacers were used between boards. After the stacking was complete, the connector cable, which was fabricated on a jig, was placed in position with the board stack on a mockup of the container. The individual cable wires were then cut to length and attached to the boards; half of the stack was unfolded at a time to enable the assembler to solder the cables in place. After cable attachment the units were placed in the container and delivered to Goddard.

Upon receipt at Goddard, the units were unfolded and placed in a fixture (Figure 17) which allowed access to all circuitry for checkout. To prevent accidental damage to both the wiring and flatpacks, plexiglass plates were attached to both sides of the boards. On the circuit side, the plexiglass plate contained a hole pattern matching the board pin pattern. This allowed access to all signal points through use of small probes held on the plate by double faced adhesive tape. Figure 18 shows the use of the test probe.

Repairs and changes were made with polyurethane insulated wire soldered to the pins after clipping the welded wire and removing any excess weld material.

After the individual units were checked out, they were stacked together in their fixtures and interconnected with their test console as shown in Figure 19.

Thermal testing was performed with the units in their containers. After the testing was complete the units were again mounted on their fixture and conformally spray-coated with polyurethane. Then they were stacked in their containers, ready for encapsulation.

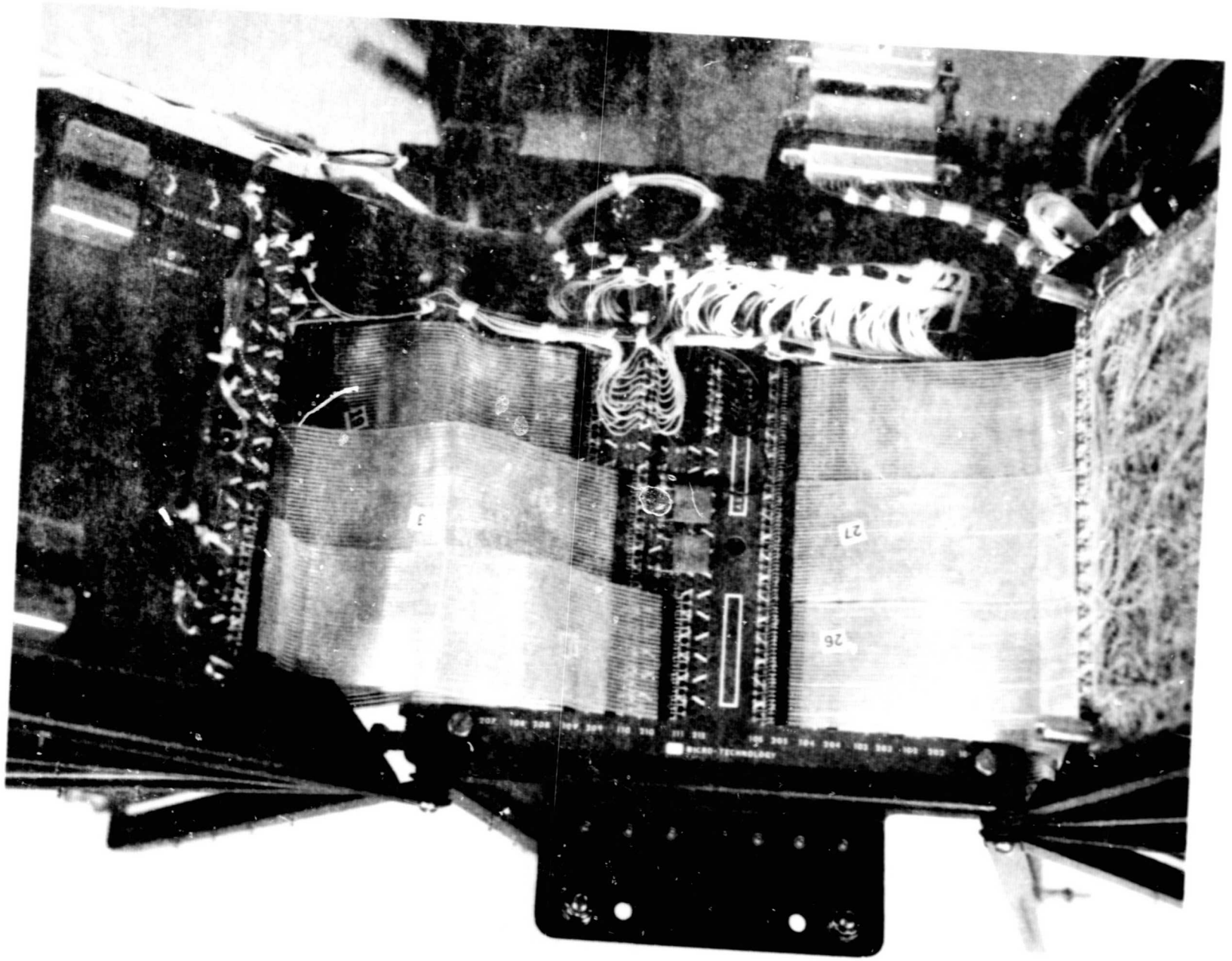

Figure 13. I/O Granny Board

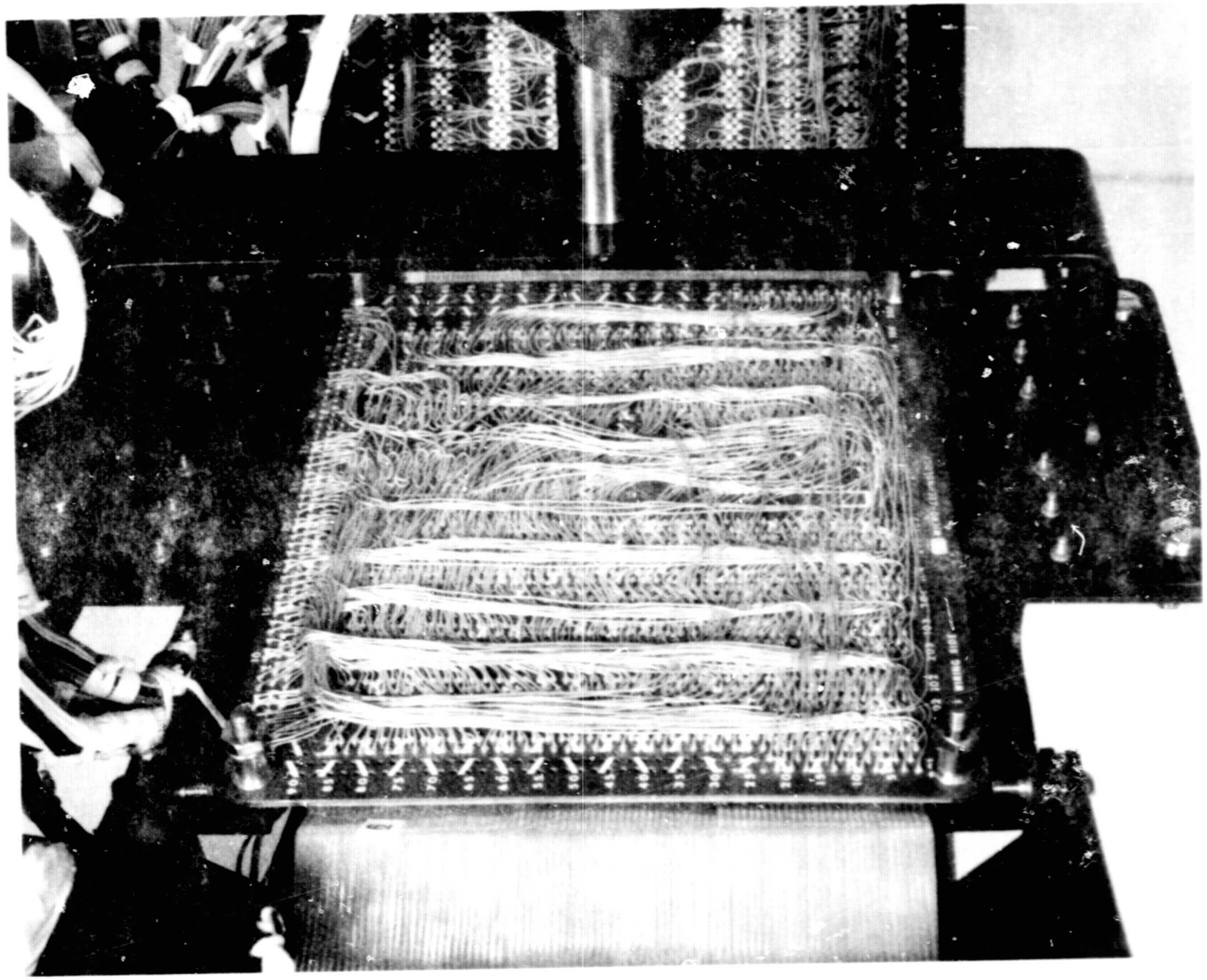

Figure 14. Wiring Side of I O Granny Board

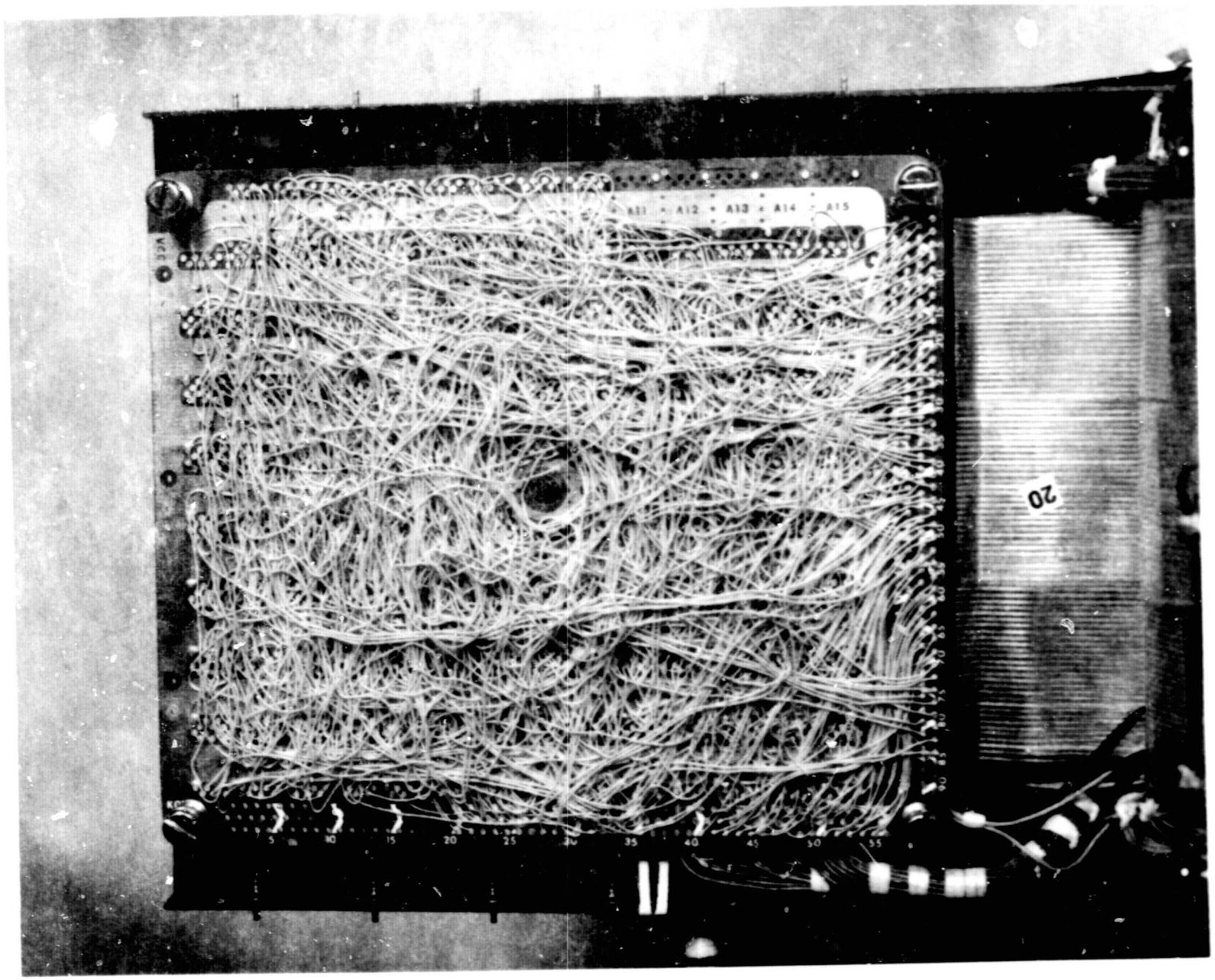

Figure 15. Wiring Side of Typical CPU Board

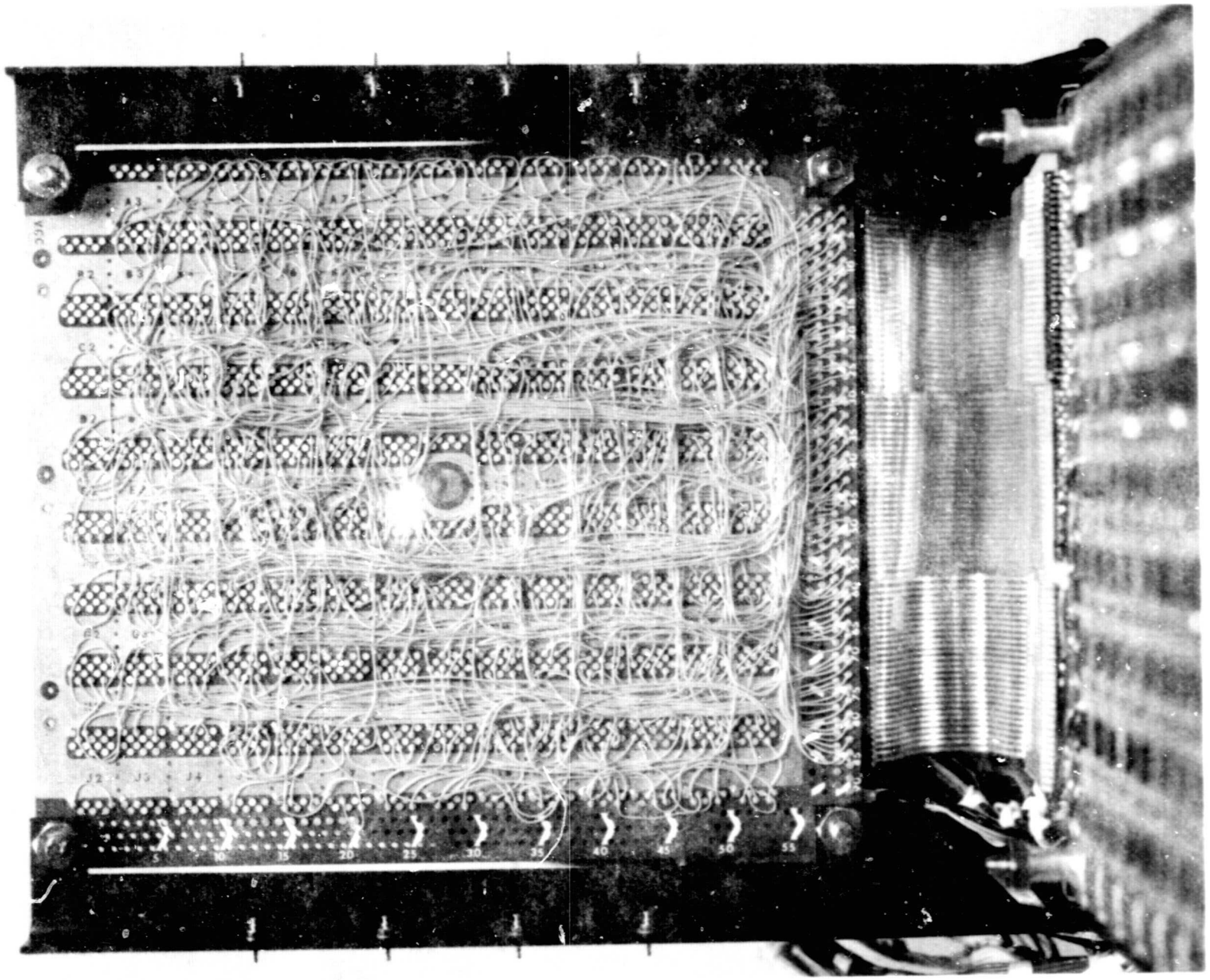

Figure 16. Wiring Side of Typical I/O Board

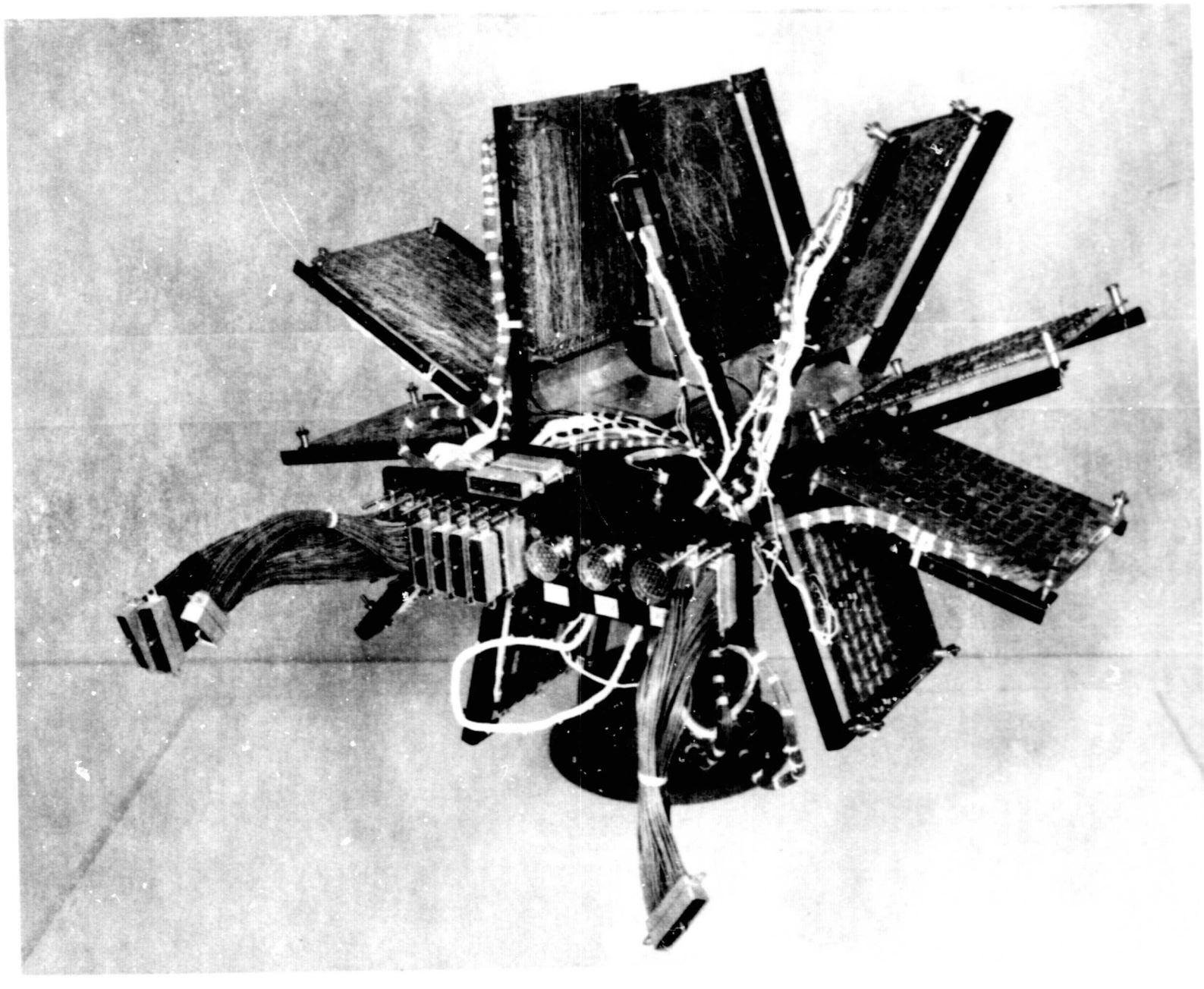

Figure 17. I/O Holding Fixture

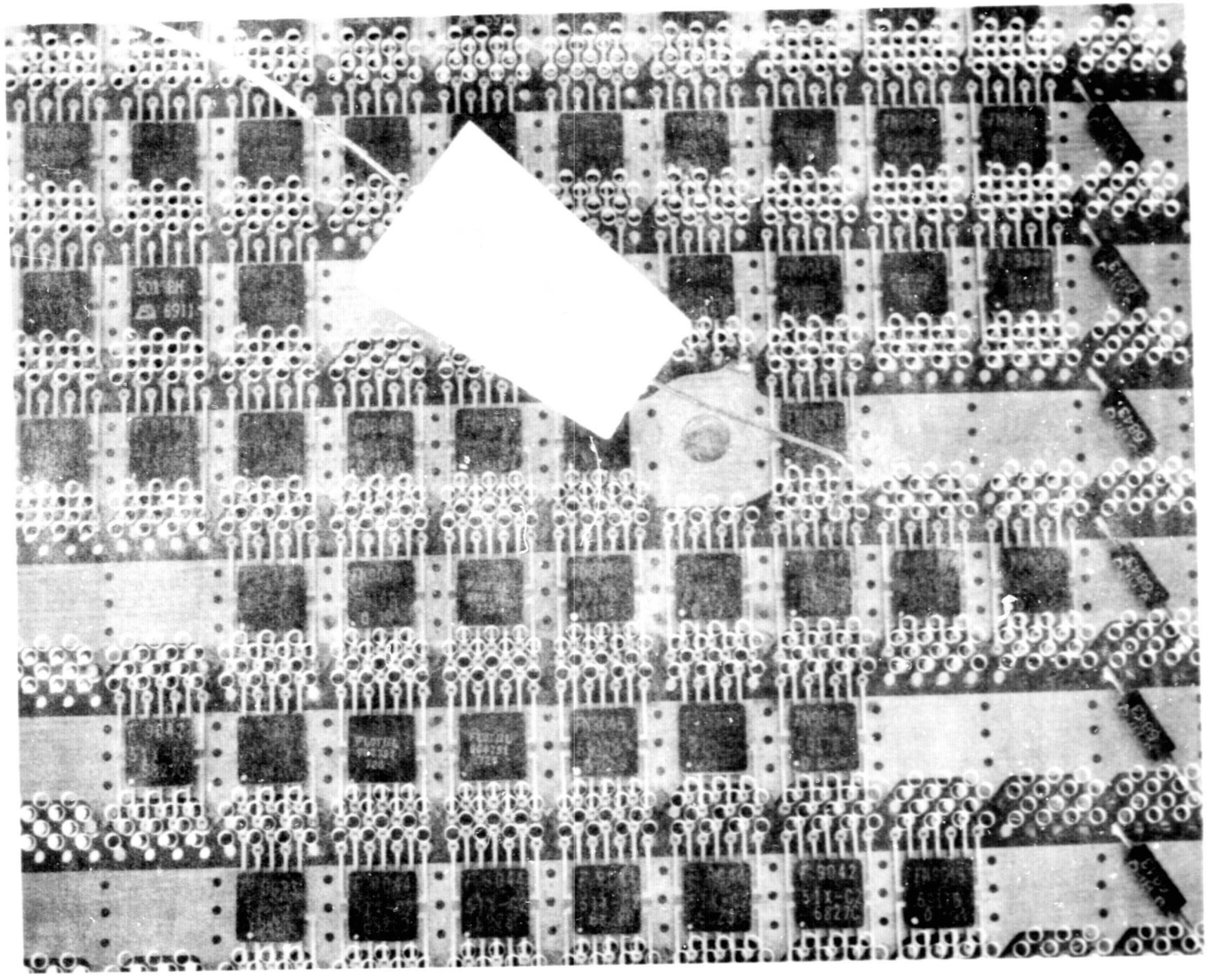

Figure 18. Test Probe

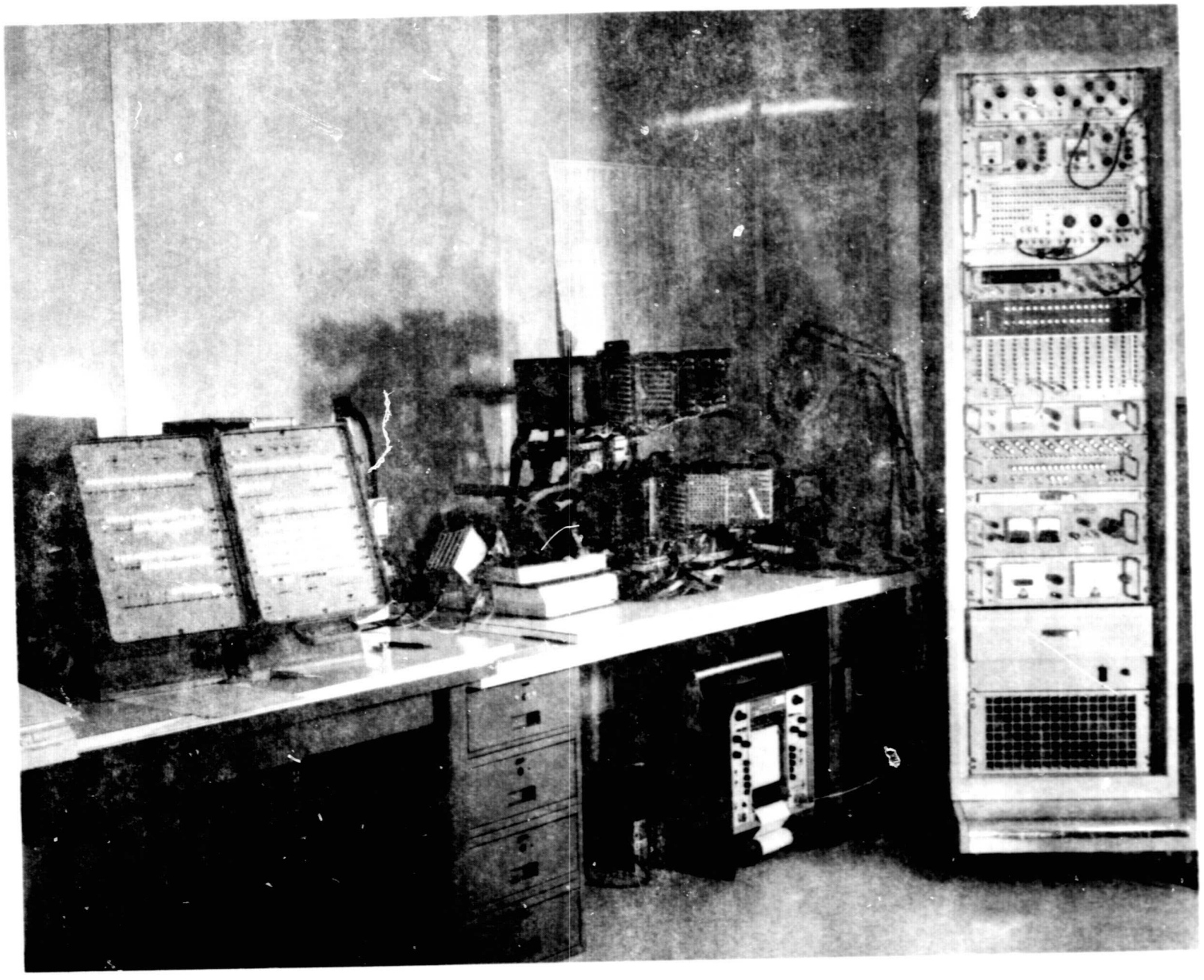

Figure 19. OBP Clean Room Test System

To help reduce the temperature gradient, a specially designed copper fin assembly was slipped between boards and bolted to the cover. This assembly is shown in Figure 20.

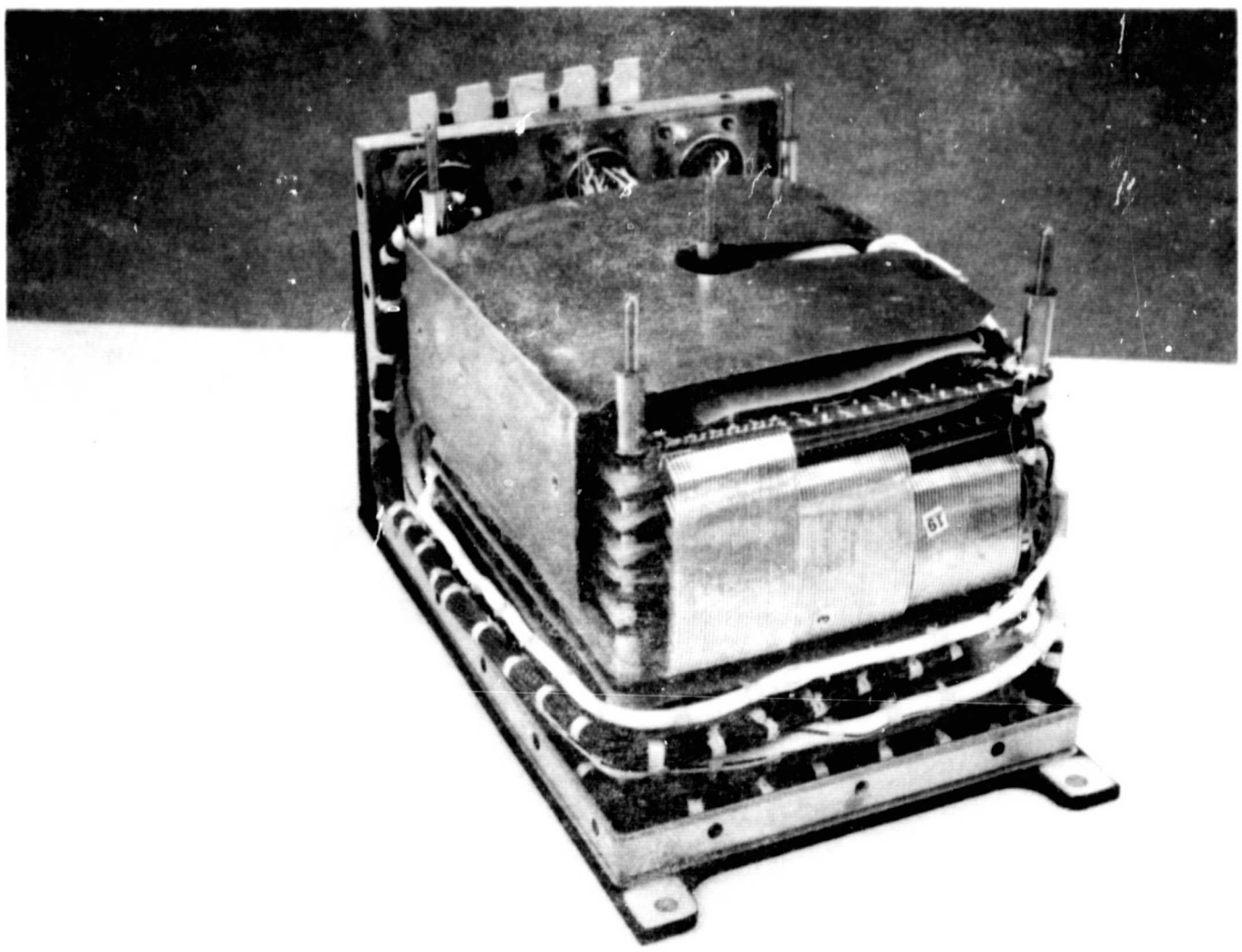

Figure 20. I/O With Copper Fin Assembly

ENCAPSULATION

A number of encapsulating materials were considered for these units. Among them were polyurethane foam, ploy urethane conformal coating, silicone rubber, and silicone rubber foam. Table 2 shows some of the trade-offs involved in the choice.

It was anticipated that at some point in the program there would be a requirement to rework the units for either changes or repair. Thus, ease of depotting and

Table 2

Characteristics of Encapsulating Materials Considered

Material	Mechanical	Depotting Ease	Weight	Thermal
Polyurethane Foam	Excellent	Poor	Excellent	Poor
Silicone Rubber Foam	Good	Fair	Fair	Fair
Polyurethane Coating	Fair	Good	Excellent	Fair
Clear Silicone Rubber	Excellent	Very Good	Poor	Fair

rework was considered important. For mechanical and thermal reasons, a solid potting material was desirable. The clear silicone rubber proved to have the best overall characteristics and was chosen. Also, to prevent accidental damage to the wiring during a depotting operation, a thin polyurethane conformal coating was sprayed on all boards prior to potting the units. This served to tie the Micropoint wiring together and to the boards and thus prevent accidental snagging of the wiring. Because the computed overall OBP weight exceeded the amount budgeted, the open areas in the I/O and CPU packages were filled with small hollow epoxy spheres prior to encapsulation.

ENVIRONMENTAL TEST RESULTS

Both units have been successfully vibration-tested to OAO-C flight levels. Preliminary thermal testing has been performed. Two shorts in the Micropoint wiring were discovered during this thermal testing. These will be discussed in detail later. The units are currently undergoing six cycles of thermal-vacuum test. The Table 3 outlines the test specification.

PROBLEM AREAS

Several potential problem areas were investigated prior to the start of board fabrication or wiring. One was pin retention over the required temperature range. A study indicated that a negative clearance of .001 to .002 inch between pin and hole would provide a pin retention force greater than 10 pounds after temperature cycling.

Table 3

Environmental Test Specifications for OAO-C

Temperature

-35 ±3°C to +65 ±3°C

Shock

Four shock pulses along each axis according to the following schedule: X (thrust axis), two 30g shocks (±) 6 ms and two 30g shocks (±) of 12 ms duration. Y axis (lateral), two 15g shocks (±) of 6 ms and two 15g shocks (±) of 12 ms duration. Z axis (lateral), same as Y. (May be completed during vibration testing if expedient.)

Vibration

Sinusoidal, 4 Octaves/Min. All Axes		Random, 2 Min./Axis All Axes	
Frequency	Level	Frequency	Level
5-20 Hz	1/2" DA	15 Hz	0.010 g^2/Hz
20-110 Hz	10.0 g Peak	15-70 Hz	Linear Increase
110-2000 Hz	5.0 g Peak	70-100 Hz	0.31 g^2/Hz
		100-400 Hz	Linear Decrease
		400-2000 Hz	0.02 g^2/Hz

Another area of concern was Micropoint weld consistency. It was decided that sample pull tests would be performed after each 300 to 400 welds. Should a sample fail the test, a non-destructive calibrated "push" test would be employed to test the questionable welds. In the fabrication of the flight boards, the need for this test did not arise.

The most serious problem that developed was shorts which occurred on several CPU boards. Examination revealed two different causes: One cause was the assembler attempting to reduce wire buildup by routing wires between pins and

pressing them down against the board; this caused shorts where the wire pressed against the sharp edges of the pins. Shorts also resulted when wiring was run over pins which were at the end of a wire run. The wire ends had been cut off with standard diagonal cutters that left sharp chisel points, and these points penetrated the insulation of wiring run over the pins and pressed against the points in attempts to reduce wire buildup. Figure 15 shows a typical CPU board. Because of the density, it was impossible to inspect all wiring after the wiring was completed.

After the CPU wiring had been started, the wire lists were examined to determine the optimum sorting to minimize wire buildup. It was determined that a change from the numerical sort, in which wiring ran generally vertically, to an alphabetic sort in which the wiring ran generally horizontally along the rows would probably somewhat reduce the buildup. The I/O wire lists were re-run with the alphabetic sort. Figure 16 shows a typical I/O board: Not only was the buildup reduced, but the wiring operation was much faster because the pin area could be kept clear of wiring. Inspection of all pins could be performed after all wiring was completed.

To date no shorts have been observed in the I/O unit. Because of the number of shorts observed in the CPU (approximately 8), the present unit will be considered a prototype and a new CPU flight unit is currently planned. The wire lists will be revised as described.

FUTURE DEVELOPMENTS

Several new flight packages are currently being developed using the Micropoint technique. Several changes have been made in the process specifications to improve the quality. One change requires the use of flush cutters to cut the Micropoint wire at the end of a signal run, reducing the likelihood of sharp points on the wires. Another change specifies that the Micropoint wire shall be routed away from pins containing the beginning and end of a wire run. Micro Technology Incorporated and other manufacturers are investigating the use of different types of insulation, including teflon with an additional surface coating, to improve the protection against cut-through.

On the basis of experience with the OBP and several smaller packages utilizing the Micropoint technique, this technique is believed to be basically a reliable, low cost technique. Further development is needed to improve the insulation properties and to make the process less assembler-dependent.