NASA TECHNICAL NOTE

NASA TN D-5960

NASA TN D-5960

A SPIN SYNCHRONOUS CLOCK FOR SPIN-STABILIZED VEHICLES

by E. John Pyle

Goddard Space Flight Center
Greenbelt, Md. 20771

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION • WASHINGTON, D. C. • SEPTEMBER 1970

National Aeronautics And Space Administration

Completed
7-30-71 Sec

ERRATA

NASA Technical Note D-5960

May 1970

A SPIN SYNCHRONOUS CLOCK FOR SPIN-STABILIZED VEHICLES

by E. John Pyle

To correct this document, replace pages 11 through 16 with the enclosed pages.

Issued October 1971

1. Report No. NASA TN D-5960	2. Government Accession No.	3. Recipient's Catalog No.
4. Title and Subtitle: A Spin Synchronous Clock For Spin-Stabilized Vehicles		5. Report Date: September 1970 6. Performing Organization Code
7. Author(s): E. John Pyle		8. Performing Organization Report No.
9. Performing Organization Name and Address: Goddard Space Flight Center, Greenbelt, Maryland 20771		10. Work Unit No. 11. Contract or Grant No.
12. Sponsoring Agency Name and Address: National Aeronautics and Space Administration, Washington, D.C. 20546		13. Type of Report and Period Covered: Technical Note 14. Sponsoring Agency Code
15. Supplementary Notes		

16. Abstract The Spin Synchronous Clock (SSC) is a digital system that generates a time-based clock signal synchronized to the spin rate of a spin-stabilized vehicle. The basic function of the device is to supply a series of pulses defining equal angular intervals within the spin period. This function is accomplished by the generation of a signal whose frequency is a multiple of the spin rate. The clock signal may be synchronized to any spin event detected aboard the vehicle, such as the magnetic field crossing or the sun line crossing.

The majority of scientific experiments on spin-stabilized spacecraft have directional detectors. Therefore, the spinning motion of the spacecraft causes these detectors to perform a circular scan of the celestial sphere. With an onboard clock synchronized to the spin rate and independent of telemetry format restrictions, the experimenter is free to sample data only from that region of space in which he is interested.

Also, the SSC may be used to increase the accuracy and to reduce the complexity of other vehicle functions, such as attitude control, miniprobe separation, and electronically despun antennas.

17. Key Words Suggested by Author: Spin-stabilized spacecraft Synchronous timing function Spin synchronous clock	18. Distribution Statement: Unclassified-Unlimited

19. Security Classif. (of this report)	20. Security Classif. (of this page)	21. No. of Pages	22. Price*
Unclassified	Unclassified	16	$3.00

*For sale by the Clearinghouse for Federal Scientific and Technical Information Springfield, Virginia 22151

CONTENTS

A SPIN SYNCHRONOUS CLOCK FOR SPIN-STABILIZED VEHICLES

by

E. John Pyle
Goddard Space Flight Center

INTRODUCTION

The technique used to generate a spin-synchronized signal whose frequency is a multiple of the spin rate is best presented by the use of a simple example.

Assume the existence of a spin-stabilized spacecraft with a spin period of 10 s that must be divided into 16 equal intervals. The spin period is measured by a counter C_1 that uses f_1, a 100-Hz frequency source. Hence, in a single spin, the counter C_1 will accumulate 1000 counts. The contents of C_1 are transferred to a storage register and are compared to the contents of a second counter C_0. The criterion for the comparison and the generation of a pulse is that the number in the counter C_0 be equal to the number in the storage register. Further, let the source frequency f_0 of counter C_0 be 16 times that at which the spin period was sampled ($f_0 = 1.6\text{kHz} = 16f_1$). Therefore, 0.625 s after it starts counting, counter C_0 will register the number 1000. At this time the comparator circuit will generate a pulse. If this pulse resets counter C_0, then 0.625 s later C_0 will have reached the count of 1000 again and will cause the generation of a second pulse from the comparator. Hence, if counter C_0 initially starts at the beginning of the definition of a spin period, the comparison circuitry will produce 16 pulses within the spin period of 10 s.

Therefore, the basic technique used by the Spin Synchronous Clock (SSC) to generate a specific number of pulses during the spacecraft rotation period is the production of a comparator pulse each time the counter C_0 attains a specific reference value. The reference value, representing the spin period of the spacecraft, is generated every spin period from a clock frequency f_1 used as the gating source for a counter C_1. When a higher clock frequency f_0 is used as the source for the second counter C_0, the reference value attained is a multiple of the ratio of the two frequency sources f_0/f_1. Therefore, when the frequency ratio is made equal to the number of pulses desired within a spin period, the comparator output is synchronized to the spin rate and contains the desired frequency.

If the lower frequency f_1 is generated from the higher frequency f_0 by the use of a binary counter, the frequency ratio f_0/f_1 is a binary number. The capacity of this frequency-dividing counter C_d determines the ratio f_0/f_1, which is the number of pulses desired within a spin period.

The spin period is defined by converting an onboard observation, such as the sun line crossing or the magnetic field crossing, into a command pulse for the SSC. The time interval between successive command pulses is measured by using the frequency f_1 as the counting source for a counter C_1. This interval counter C_1 then contains the number of counts of f_1 that occurred between two successive command pulses and, hence, represents the rotation period of the spacecraft. For the interval counter C_1 to record every spin of the spacecraft, the information must be transferred to a storage register and the counter C_1 reset upon each occurrence of the command pulse.

When the spin period information is transferred to a storage register, it is available for comparison with the state of counter C_0, which is in continuous operation and has a source frequency of f_0. When this continuous counter C_0 reaches the value contained in the storage register, the comparator generates a pulse that resets C_0. The pulses generated by the comparator become the basic time clock signal produced by the SSC.

SYSTEM DESCRIPTION

The basic function of the SSC is to generate 2^n pulses per spin period. These pulses divide the rotational period into $2^n - 1$ equal time intervals plus one remaining interval that may be slightly greater or smaller than the other intervals. To accomplish this function, the SSC receives two signals from the spacecraft systems. One is a high frequency signal f_0, the other is the command pulse. The SSC uses this command pulse to define the rotational period of the spacecraft.

For the purpose of a detailed description, the SSC can be considered to be composed of three subsystems: a control logic, a comparison logic, and an output counter.

The following definitions of terms apply to all the above subsystems:

2^n = number of pulses generated in a single spin period,

f_0 = high-frequency voltage square wave,

and

f_1 = a voltage square wave related to f_0 by the relation $f_0 = 2^n f_1$.

Control Logic

The function of this subsystem is to provide the basic control logic for the SSC. The subsystem consists of two counters and associated decoding gates that generate the timing functions necessary to control the operation of the interval counter C_1.

A block diagram is shown in Figure 1, and the signal definitions are presented in Tables 1 and 2.

The leading edge of the command pulse resets both counters to zero, which indicates the start of a spin period. The counter C_d performs the frequency division on the f_0 signal. C_d is n stages in length and has a capacity of $2^n - 1$. Hence, the output signal of its last stage supplies the frequency f_1 used in the measurement of the spin period length.

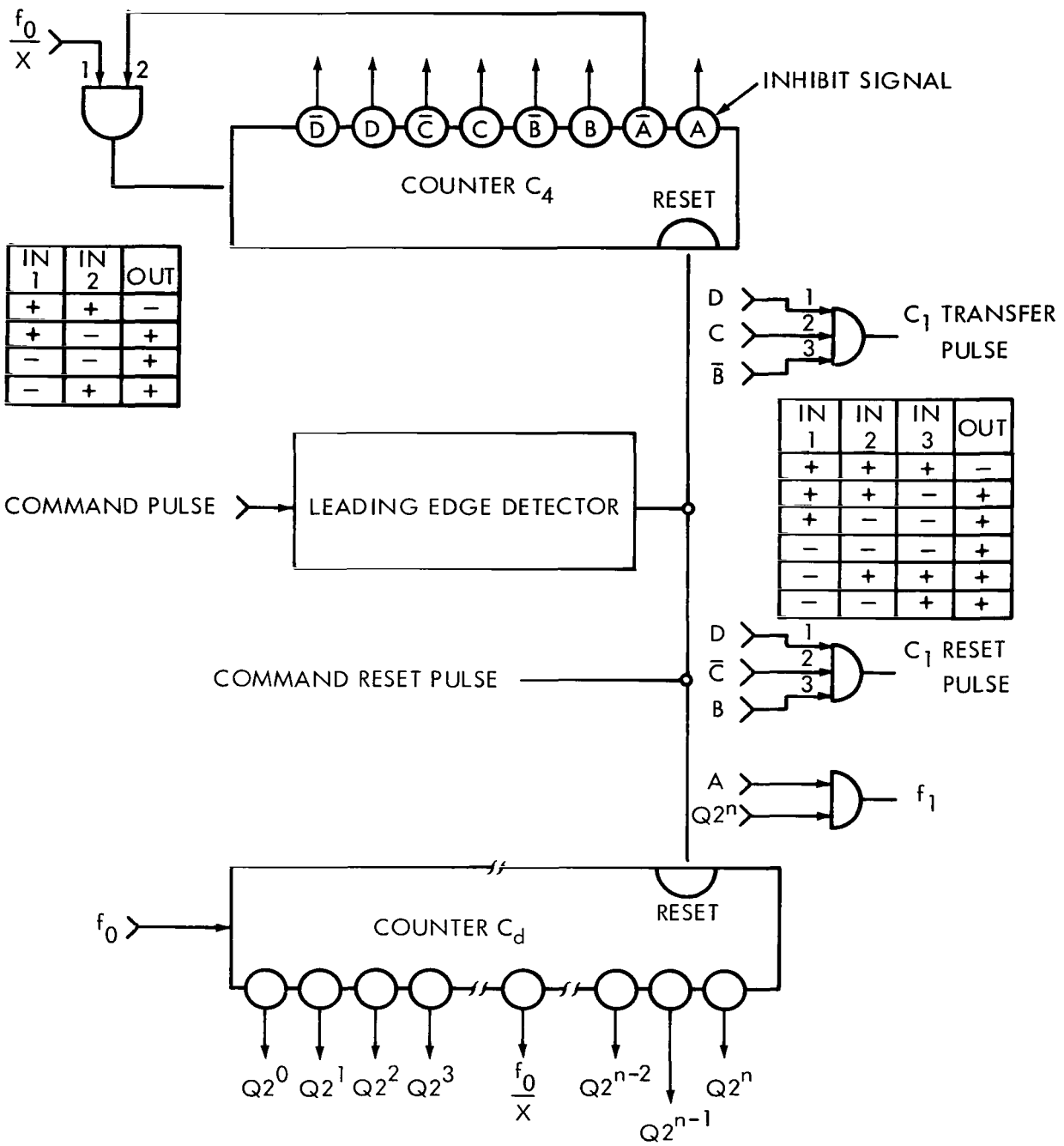

Figure 1–Control logic subsystem block diagram.

Table 1—Input signals to control logic subsystem.

Designation	Origin	Descriptive remarks
f_0 signal	External to SSC	Square wave voltage signal whose frequency is f_0.
Command pulse	External to SSC	Voltage pulse whose leading edge defines the start of a spin period.

Table 2—Output signals from control logic subsystem.

Designation	Destination	Descriptive remarks
C_1 transfer pulse	Interval counter C_1	A voltage pulse occurring slightly after the command pulse and used to transfer the contents of C_1 into a storage register.
C_1 inhibit signal	Interval counter C_1	A voltage level occurring with the command pulse.
C_1 reset pulse	Interval counter C_1	A voltage pulse occurring after the C_1 transfer pulse and used to reset C_1 to zero.
$Q2^0$ thru $Q2^n$	External to SSC except for two. One goes to C_4, the other to C_1.	The voltage output of each separate stage of the C_d counter.
Command reset pulse	Output counter	A voltage pulse occurring coincident with the leading edge of the command pulse.

The second counter C_4 and its associated decoding generates three signals for the control of the operation of the interval counter C_1. These are a C_1 inhibit signal (a voltage that prevents C_1 from changing its contents during transfer pulse occurrence), at C_1 transfer pulse (a pulse that transfers the contents of the C_1 counter into a storage register), and a C_1 reset pulse (a pulse that resets the C_1 counter to zero following the transfer pulse).

The block diagram (Figure 1) shows the logic for these three functions and the fact that the input to C_4 is a gated function of one of the intermediate stages of C_d. The gating insures that the three C_1 control signals occur only once each spin period. Using an intermediate stage of C_d as an input to C_4 merely provides reset and transfer pulses of convenient duration. The only restriction is that these control signals be completed before the first count of f_1 enters the interval counter C_1.

Comparison Logic

The comparison logic subsystem consists of two counters, C_0 and C_1, a parallel load storage register, and a comparator (Figure 2). The storage register accepts and retains the information from the interval counter C_1 once each spin period. The second counter C_0 operates continuously at a rate of f_0 and, along with the storage register, provides the inputs to the comparator. When the contents of the storage register and the counter C_0 are identical, the comparator generates a pulse. In a given spin period, the pulses generated by the comparator become the clock signal synchronized to the spin period. These pulses, along with the command reset pulse, are used to reset the counter C_0. Hence, they must be such that their action does not cause the loss of an f_0 count. This places a constraint on the pulse width of the comparator-generated pulses as well as on the command reset pulse.

The signal definitions are presented in Tables 3 and 4.

Output Counter

The pulses generated by the comparator compose the clock signal synchronized to the spin period. This signal is used as the input to the output counter C_t. Hence, decoding the output counter C_t makes information available about the instantaneous pointing direction of a point on the spacecraft.

A block diagram of the output counter subsystem is shown in Figure 3. During the rotation period, the counter C_t should reach a count of 2^n and then be reset to zero by the command reset pulse. If 2^n counts have been accumulated and a command reset pulse does not occur, the counter C_t continues until 2^{n+1} counts have been accumulated. If a command reset pulse still has not occurred by this time, the circuitry associated with the counter C_t generates a pseudocommand signal every time the contents of C_t are changed by 2^n pulses from the comparator. Hence, the output counter subsystem will wait one spin period following the loss of the command reset pulse before generating a pseudocommand signal every 2^n pulses from the comparator. The signal definitions are presented in Tables 5 and 6.

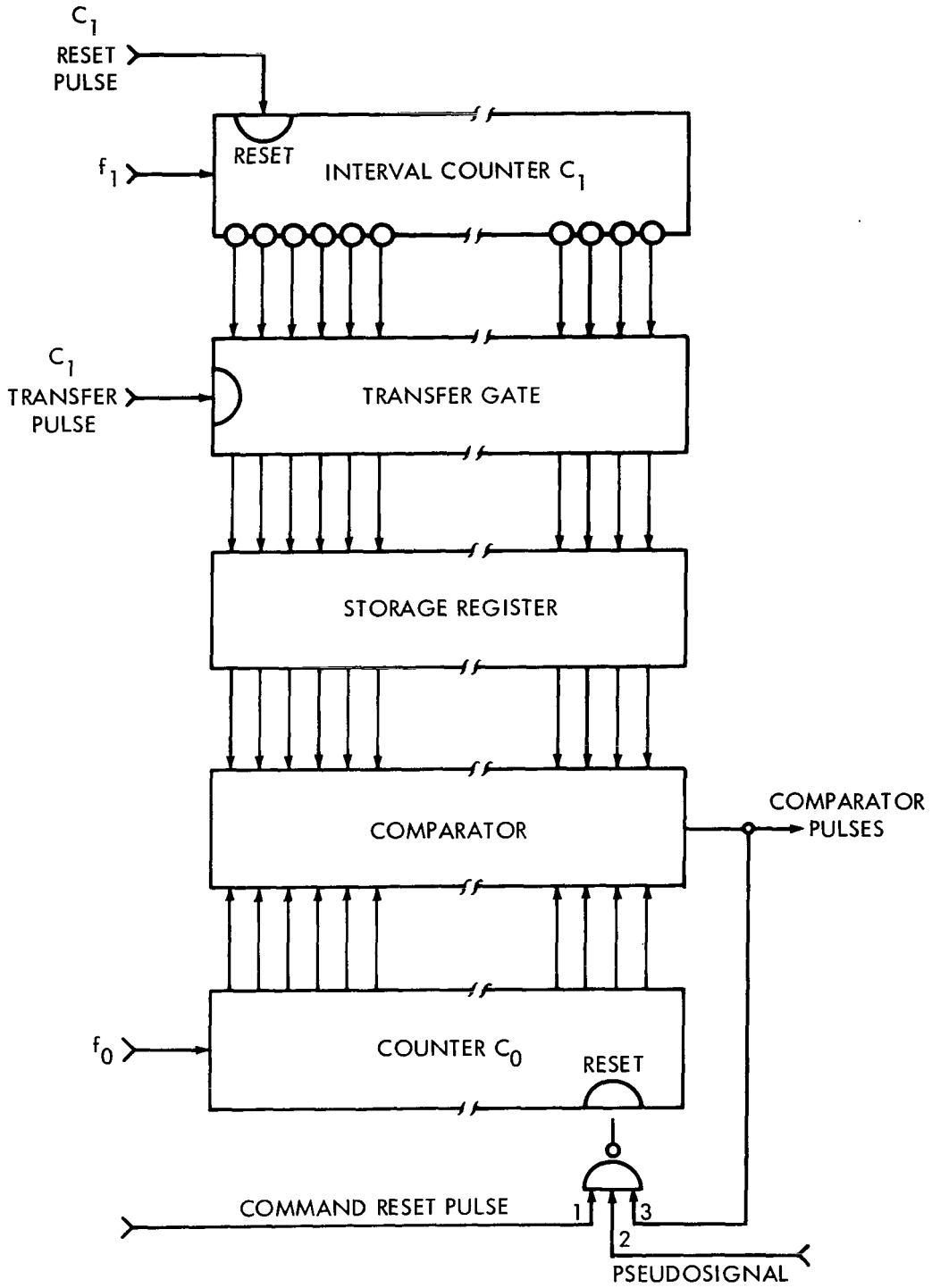

Figure 2–Comparison logic block diagram.

Table 3—Input signals to comparison logic subsystem.

Designation	Origin	Descriptive remarks
C_1 transfer pulse	Control logic	A voltage pulse occurring slightly after the command pulse and used to transfer the contents of C_1 into a storage register.
C_1 inhibit signal	Control logic	A voltage level occurring with the command pulse.
C_1 reset pulse	Control logic	A voltage pulse occurring after the C_1 transfer pulse and used to reset C_1 to zero.
f_0 signal	External to SSC	A square wave voltage signal whose frequency is f_0.
Command reset pulse	Control logic	A voltage pulse occurring at the same time as the leading edge of the command pulse.
f_1 signal	Control logic	A square wave voltage whose frequency is f_1. ($f_1 = f_0/2^n$).
Pseudosignal	Output counter	A voltage pulse generated at the last known spin rate to replace the lost command reset pulse.

Table 4—Output signals from comparison logic subsystem.

Designation	Destination	Descriptive remarks
Comparator pulses	Output counter and external to SSC	A voltage pulse train forming the basic spin-synchronized signal.

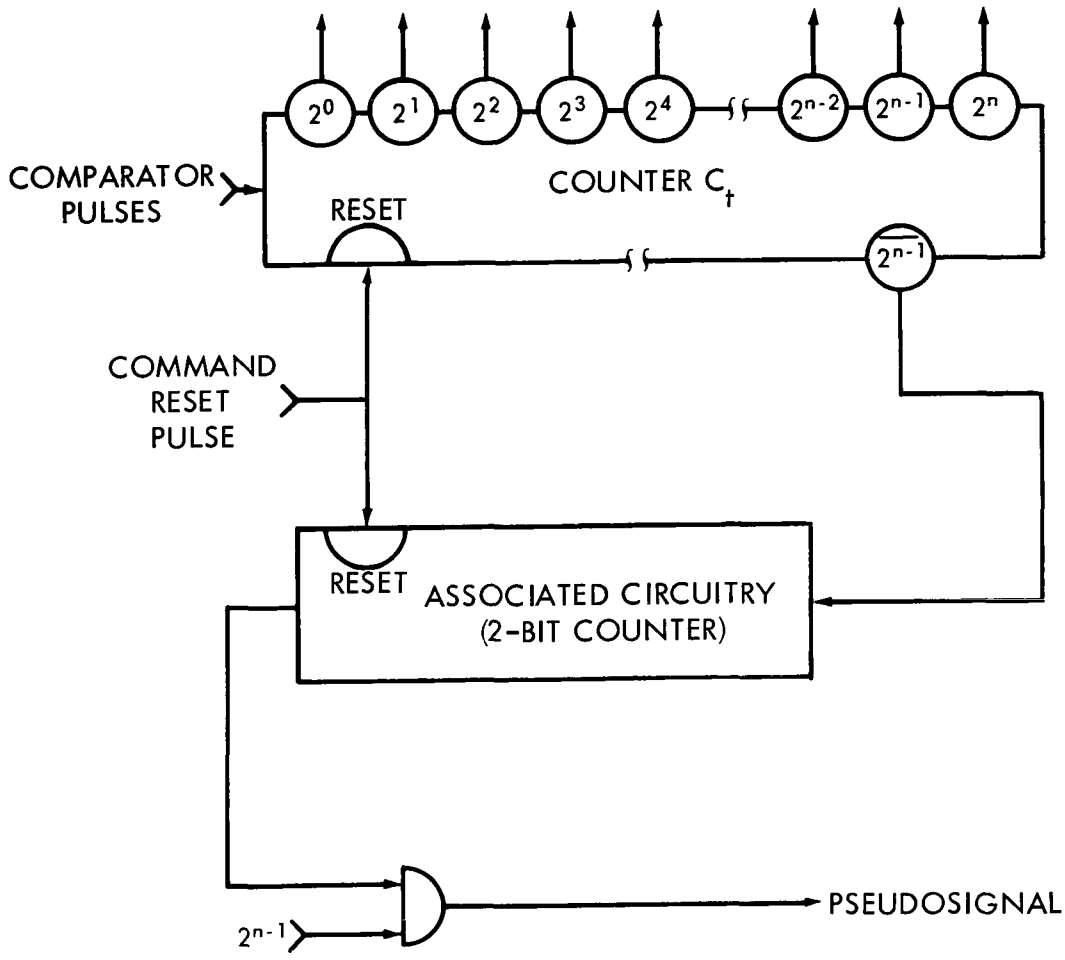

Figure 3–Output counter subsystem block diagram.

Table 5–Input signals to output counter subsystem.

Designation	Origin	Descriptive remarks
Comparator pulses	Comparison logic	A voltage pulse train forming the basic spin-synchronized signal.
Command reset pulse	Control logic	A voltage pulse occurring at the same time as the leading edge of command pulse.

Table 6—Output signals from output counter subsystem.

Designation	Destination	Descriptive remarks
$C_t 2^0$ through $C_t 2^n$	External to SSC	A voltage signal of each stage of counter C_t.
Pseudosignal	Comparison logic	A voltage pulse generated at the last known spin rate to replace the lost command reset pulse.

SYSTEM PERFORMANCE

The SSC divides the spin period into 2^n sectors by using the information in the storage register as the basic interval to be sectored. An investigation of the accuracy of this information will lead to an evaluation of the system performance.

Consider the representation of the spin period by the interval counter C_1. This representation of the spin period may be less than the true spin period by one count of f_1. This discrepancy follows directly from the division process performed in the generation of the f_1 signal. Since division can generate both a quotient and a remainder, the C_1 representation can differ from the true spin period by the amount of this remainder. This means that if the spin period is not an integer multiple of T_1, where $T_1 = f_1$, the contents of C_1 will be less than the spin period. This difference can be as small as one count or as great as $2^n - 1$ counts of f_0.

Another consideration not previously mentioned is the interaction between the C_1 inhibit signal and the f_1 signal when the spin period is measured. This effect may cause an extra count to be placed in the C_1 counter if the inhibit signal occurs at a time when the f_1 signal is 1. The f_1 signal is 1 when the contents of counter C_d are equal to or greater than one-half its capacity; i.e., when the last stage of C_d is 1.

The combined effect of these two considerations is to incorporate a round-off error into the interval counter C_1. If the remainder of the division process is less than one-half, the interval counter contains only the number of counts of f_1 that occurred during the spin period. If the remainder is equal to or greater than one-half, the interval counter contains a count equal to the number of counts of f_1 sampled during the spin period plus the extra count due to the action of the inhibit signal. Hence, the error in the interval counter has been translated, resulting in a total error of $\pm 1/2$ count of f_1. The total error in C_1 as a function of the remainder in C_d is shown in Figure 4. Thus, when the remainder is less than one-half, the output counter attains a count of 2^n before the next SSC command pulse. The maximum value of this time lapse is equal to $T_1/2$, where T_1 is measured in units of time.

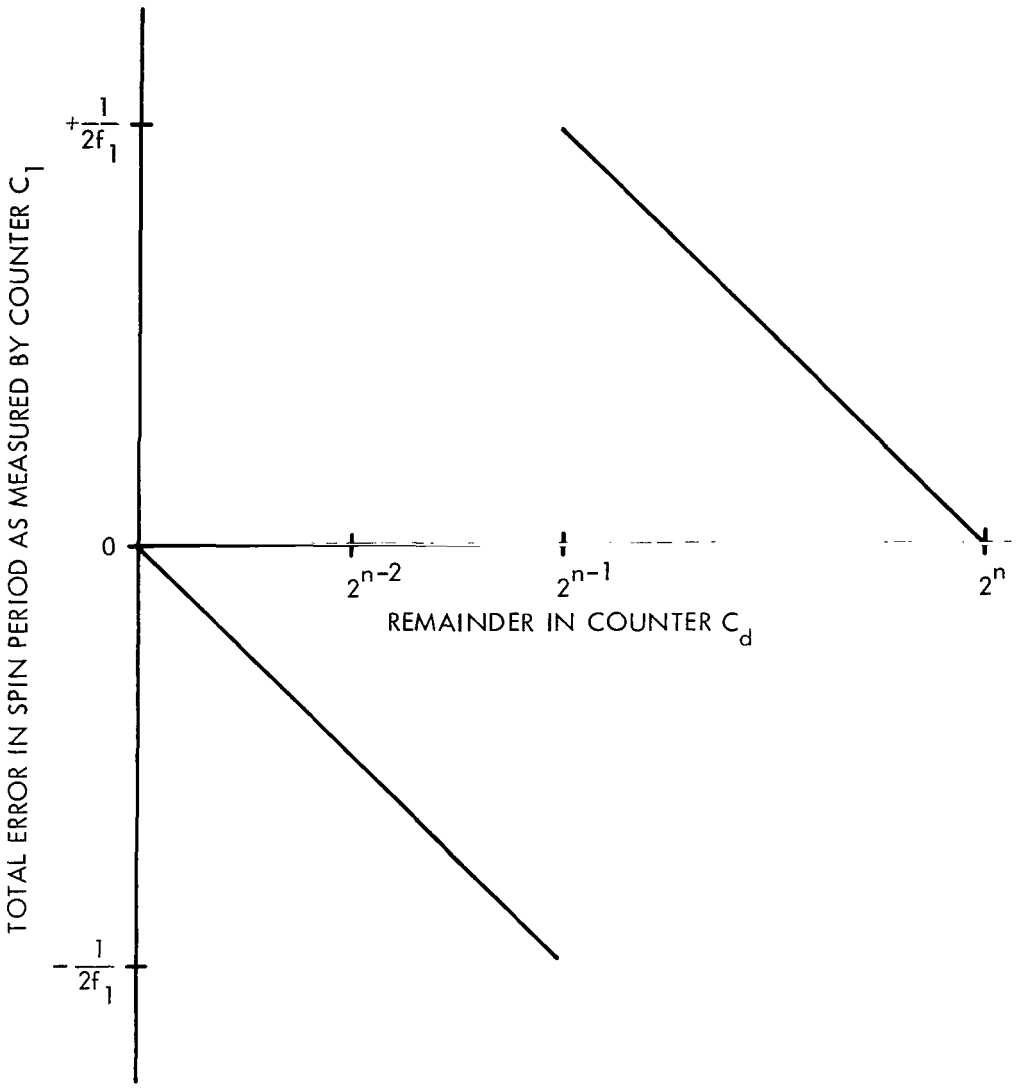

Figure 4—Total error in C_1 as a function of the remainder in C_d.

Another factor affecting system performance is the variation in two successive spin period intervals. This variation may result from a "jitter" effect of the onboard instrument generating the command pulse or directly from the motion of the spacecraft (precession). Since the operation of the SSC is based on the assumption that two successive spin periods are equal, this spin period fluctuation has a one-to-one effect on system performance. However, this effect simply reduces the accuracy of the location of the sector pulses in a given spin interval.

A companion factor to the above short-term fluctuation is the long-term loss of the command pulse. This effect is taken into account in the operation of the output counter C_t. The C_t counter operates in such a manner that if the command pulse does not occur after 2^n pulses, the counter will continue to count until either 2^{n+1} counts have been registered or the command pulse occurs. When 2^{n+1} counts have been accumulated, the associated circuitry generates a pseudocommand signal. This signal resets the continuous counter C_0 but does not update the interval counter C_1. Therefore, the system waits one rotation period following the loss of the command pulse before generating a pseudocommand signal at the last known spin period interval stored in the storage register. Hence, even if a long-term loss of the command pulse occurs, the system continues to operate on the basis of the last known spin period measurement.

SECTOR DETERMINATION: LOCATION AND WIDTH

If the location in a given spin period of a specific sector region is to be defined, consideration must first be given to a reference system. Let this reference system be based on the 360° of rotation in a spin period. Then, each pulse generated by the comparator and defining the end of a sector region will be separated from the previous one by $360/2^n$ degrees of rotation. Hence, in this reference system, the 2^nth sector pulse will occur coincidentally with the command pulse and the width of each and every sector will be $360°/2^n$.

The actual Spin Synchronous Clock (SSC) will generate sector pulses based on the spin period representation present in the storage register. Hence, these sector pulses will match the ideal reference system if, and only if, the remainder of the division process is equal to zero. In all other cases (remainder $\neq 0$), the sector pulse generated by the comparator circuit in the actual system will be shifted from the reference system location by ϵ, where

$$\epsilon = \left[\begin{array}{ll} -\dfrac{T_0 R k}{2^n}, & \text{for } R < 2^{n-1} \\ +\dfrac{(2^n - R) T_0 k}{2^n}, & \text{for } R \geq 2^{n-1} \end{array}\right] = \text{shift in sector pulse location,}$$

2^n = number of sector pulses in a spin,

T_0 = $1/f_0$ = period of the f_0 signal,

R = remainder ($1 \leq R \leq 2^n - 1$),

and

k = number of the sector ($1, 2, 3, \ldots 2^n - 1, 2^n$).

Now examine the case for $R < 2^{n-1}$. The storage register contains a time representation of the spin period that is less than the true spin period. Hence, the interval being divided into 2^n sectors is equal to the true spin period minus the time represented by the remainder. In reference to Figure 5,

N = number of counts in interval counter C_1,

$(2^n N + R)T_0$ = true spin period,

and

$2^n T_0 N$ = time representation of spin period by the storage register.

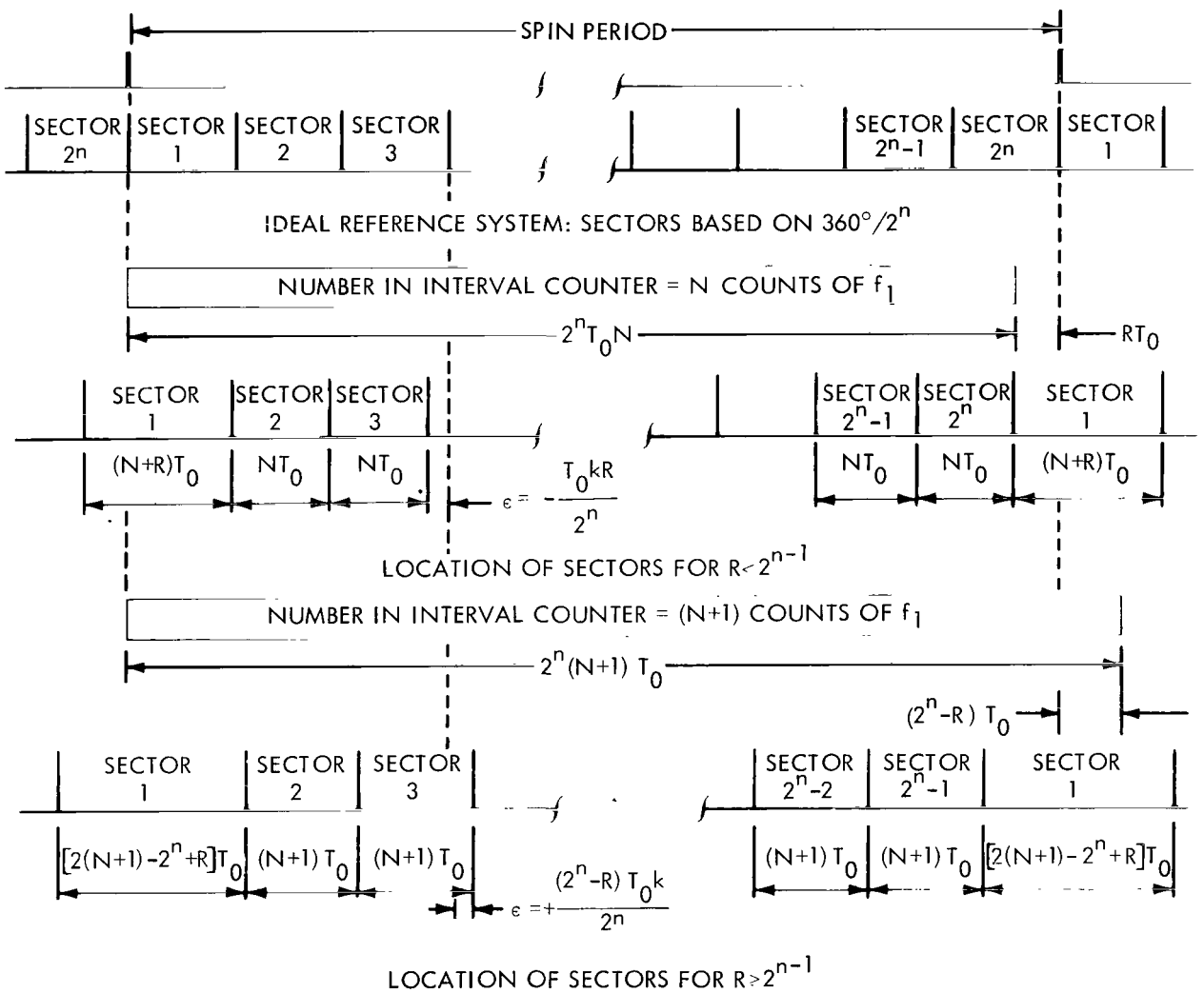

Figure 5–Sector location as a function of the remainder.

Therefore, each sector pulse is generated slightly before the location of its corresponding ideal reference sector pulse. This effect is cumulative and results in the generation of the 2^nth sector pulse T_0R seconds before the 2^nth ideal reference location. Since each sector pulse resets the continuous counter C_0, this counter will have obtained a value of R counts when the command pulse occurs. Hence, if the first sector is defined as the time interval between the command pulse and the next pulse generated by the comparator, this results in an effective "dead time" between the end of the 2^nth sector and the start of the first sector on the next spin. That is,

$$\left.\begin{aligned} \text{dead time width} &= RT_0 \\ \text{sector width} &= NT_0 \end{aligned}\right\} \quad \text{for } R < 2^{n-1}.$$

Therefore, the time between the 2^nth sector pulse and the first sector pulse in the next spin will include the dead time and have a value of $(N + R)T_0$.

When $R \geq 2^{n-1}$, the information in the storage register represents the true spin period plus the effect of the inhibit signal's adding a count to the interval counter C_1. Now, $(2^nN + R)T_0$ is the true spin period, and $2^n(N + 1)T_0$ is the time representation of the spin period by storage register. Hence, it is the quantity $2^n(N + 1)T_0$ that is divided by 2^n. The result is that each sector pulse is generated by the comparator slightly after its corresponding ideal reference location. Again, this effect is cumulative and the 2^nth sector pulse should occur at a time interval of $(2^n-R)T_0$ after its ideal reference location. This time is also after the command pulse, which resets both the continuous and output counters. Hence, the system will reset before the generation of the 2^n th sector. Therefore, the comparator will generate only 2^{n-1} pulses in a given spin period. That is,

$$\left.\begin{aligned} \text{dead time width} &= (2^n-R)T_0 \\ \text{sector width} &= (N + 1)T_0 \end{aligned}\right\} \quad \text{for } R \geq 2^{n-1}.$$

Here again, the dead time width is included in the interval between the 2^n-1 sector pulse and the first sector pulse in the next spin period. This interval will therefore have a value of $[2(N + 1) - (2^n-R)]T_0$.

Hence, the location of each sector pulse and the width of each sector can be determined from knowledge of the spin period and remainder values.

OPERATING RANGE: f_0, 2^n, RPM

The operating range of the SSC (Figure 6) is determined by the relationship between f_0, 2^n, and the spin rate of the spacecraft (RPM). As previously mentioned, the division can generate both a quotient and a remainder. The effect of the remainder is to shift the sector pulse from its reference location. The maximum shift occurs in the 2^nth sector and has a value of RT_0. Hence, if R is greater than the number of counts that represents

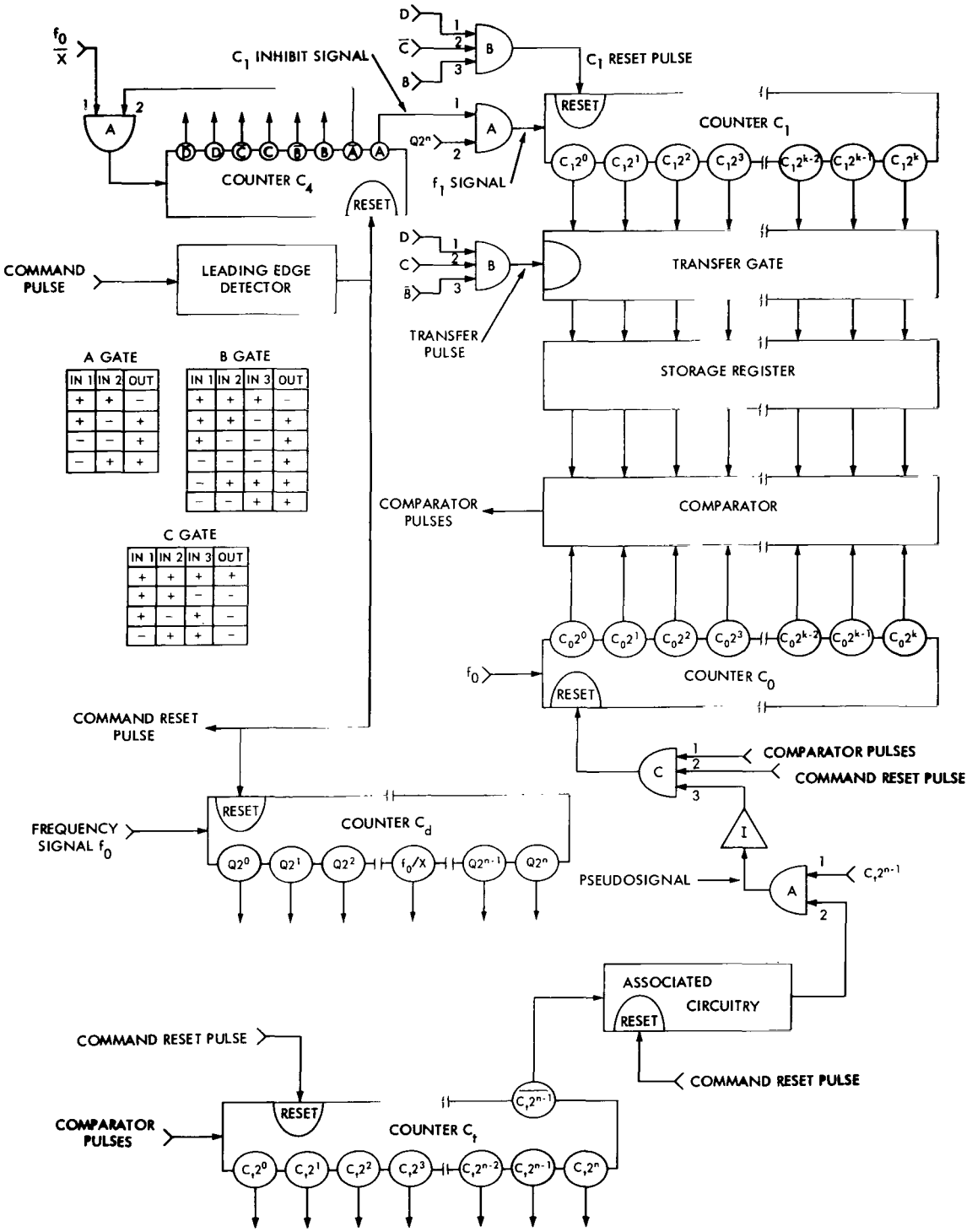

Figure 6–SSC block diagram.

the spin period in the interval counter C_1, the shift caused by R may be greater than a sector width. Therefore, one constraint on the relationship between f_0, 2^n, and RPM is that the number of pulses in the interval counter C_1 be equal to or greater than R. R_{max} equals 2^n-1, and N_{ic} is greater than or equal to 2^n, where N_{ic} is the number of pulses in interval counter C_1.

Since N_{ic} is a result of the frequency division by 2^n, the minimum number of pulses into the frequency divider counter C_d N_{id} must satisfy the following relations:

$$N_{id} \geq 2^n N_{io}, \text{ where } N_{io} \text{ is the number of pulses out of the counter } C_d,$$

$$N_{id} = \frac{\text{Spin Period}}{T_0} = \frac{60 f_0}{\text{RPM}},$$

$$N_{id} = N_{ic},$$

$$N_{id} \geq 2^n N_{ic} \geq 2^{2n},$$

$$\frac{60 f_0}{\text{RPM}} \geq 2^{2n}$$

and

$$f_0 \geq \frac{2^{2n} \text{ RPM}}{60}.$$

A further constraint on the operating range of the SSC is that N_{ic}, the number of pulses into the interval counter, must not exceed its capacity. That is, if

$$2^k = \text{capacity of the interval counter } C_1,$$

$$N_{ic} \leq 2^k,$$

and

$$N_{io} \leq 2^k$$

and since

$$N_{io} \leq \frac{N_{id}}{2^n}$$

and

$$N_{id} = \frac{60 f_0}{\text{RPM}},$$

then

$$\frac{60f_0}{2^n(\mathrm{RPM})} \leq 2^k$$

or

$$f_0 \leq \frac{2^{n+k}(\mathrm{RPM})}{60} .$$

Consideration of both constraints yields

$$\frac{2^{2n}(\mathrm{RPM})}{60} \leq f_0 \leq \frac{2^{n+k}(\mathrm{RPM})}{60} .$$

CONCLUSIONS

A time-based clock signal synchronized to the spin rate can be generated aboard a spin-stabilized spacecraft. This signal, which consists of a series of 2^n pulses, will divide the rotational period into 2^n-1 equal time intervals plus one remaining interval that may be slightly greater or smaller than the other intervals. The exact location and width of these intervals as a function of time can be determined by telemetering certain parameters from the spacecraft, i.e., the remainder. The system can be made to operate over a wide range of spin rates, and with the development in large-scale integrated circuits and metal-oxide-silicon field-effect transistors, the problems of weight, size, and power for such a system become insignificant. A block diagram of such a system is shown in Figure 6.

Goddard Space Flight Center
National Aeronautics and Space Administration
Greenbelt, Maryland, May 7, 1970
861-51-75-01-51

"The aeronautical and space activities of the United States shall be conducted so as to contribute . . . to the expansion of human knowledge of phenomena in the atmosphere and space. The Administration shall provide for the widest practicable and appropriate dissemination of information concerning its activities and the results thereof."

—NATIONAL AERONAUTICS AND SPACE ACT OF 1958

NASA SCIENTIFIC AND TECHNICAL PUBLICATIONS

TECHNICAL REPORTS: Scientific and technical information considered important, complete, and a lasting contribution to existing knowledge.

TECHNICAL NOTES: Information less broad in scope but nevertheless of importance as a contribution to existing knowledge.

TECHNICAL MEMORANDUMS: Information receiving limited distribution because of preliminary data, security classification, or other reasons.

CONTRACTOR REPORTS: Scientific and technical information generated under a NASA contract or grant and considered an important contribution to existing knowledge.

TECHNICAL TRANSLATIONS: Information published in a foreign language considered to merit NASA distribution in English.

SPECIAL PUBLICATIONS: Information derived from or of value to NASA activities. Publications include conference proceedings, monographs, data compilations, handbooks, sourcebooks, and special bibliographies.

TECHNOLOGY UTILIZATION PUBLICATIONS: Information on technology used by NASA that may be of particular interest in commercial and other non-aerospace applications. Publications include Tech Briefs, Technology Utilization Reports and Notes, and Technology Surveys.

Details on the availability of these publications may be obtained from:

SCIENTIFIC AND TECHNICAL INFORMATION DIVISION

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

Washington, D.C. 20546