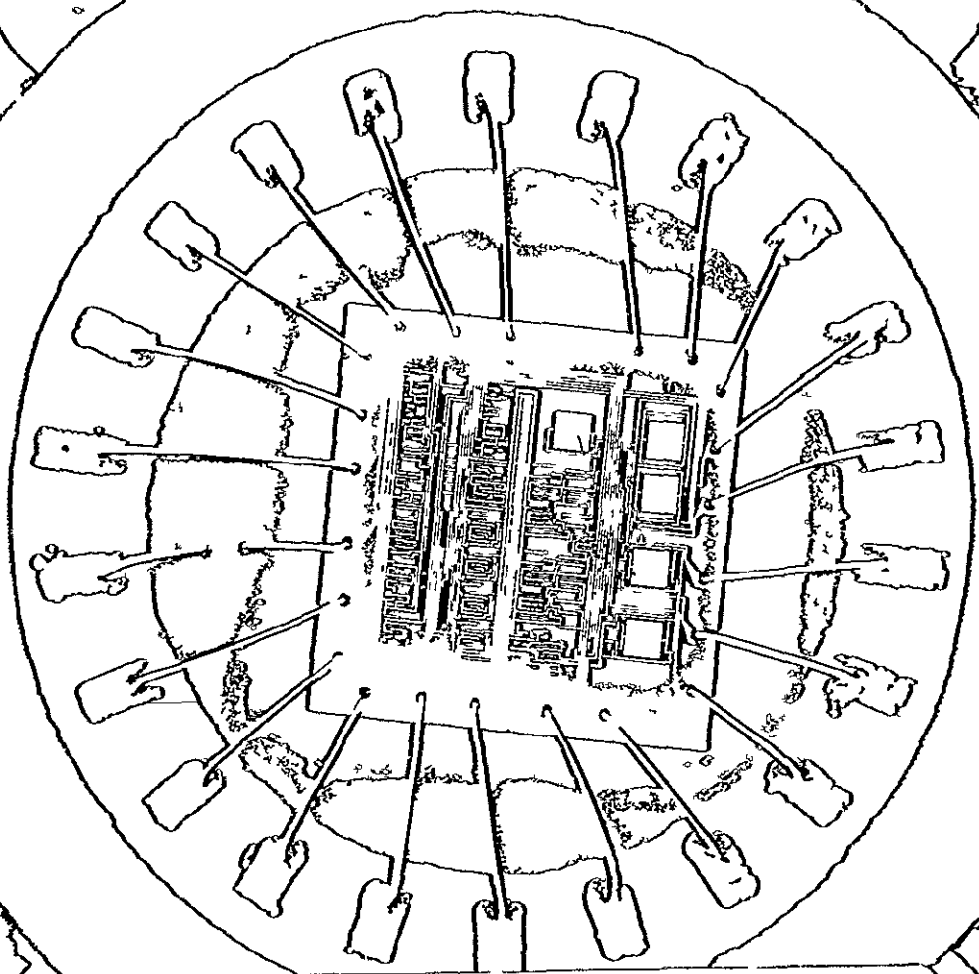
An All Monolithic MOS A/D Converter



TRW
SYSTEMS GROUP

ONE SPACE PARK, REDONDO BEACH CALIFORNIA 90278

FINAL REPORT

LOW POWER CLOCKS, MULTIPLEXERS, REGISTERS AND A/D CONVERTER

TRW Report No. 12529-6001-R0-00

Prepared for

National Aeronautics and Space Administration
George C Marshall Space Flight Center
Marshall Space Flight Center, Alabama

Under Contract No NAS8-23072

June 30, 1970

Prepared by James Eastman

Prepared by Archie MacMillan

Microelectronic Arrays Department

TRW SYSTEMS

ABSTRACT

A review of the work done to date to develop an all monolithic, MOS, 10 bit, Analog-to-Digital Converter on NASA Contract NAS8-23072 is presented First the converter design goals are given, and then a functional description of the conversion method is discussed This is followed by a detailed analysis of the circuit design

The converter design is then broken into its subfunctions and test results from each of the subfunctions are compared to the desired results The validity of the method of conversion employed is proven by test results from a converter showing 7 bit accuracy at 5 k conversions/sec over a given input voltage range

The problems in the existing A/D design are identified and changes to correct these problems are presented It is believed that when these corrections are implemented, all of the design goals can be achieved

A system which has a multiplexer at the input to the A/D converter, a serial-to-parallel converter at the output, and a two phase clock generator to drive all of them is described The compatibility of each of the devices is demonstrated Detailed test procedures and test data for each of the devices (multiplexers, serial to parallel converters and clock drivers) delivered under the contract requirements are given

CONTENTS

CONTENTS (Continued)

APPENDICES

ILLUSTRATIONS

TABLES

SECTION I

DESIGN OF A/D CONVERTER

1 0 GENERAL DESIGN GOALS

The overriding design consideration was the desire to achieve a monolithic design This approach has been successful except that the compensation of the operational amplifier requires external components

The converter is designed to be a 10 bit converter including sign It was designed to operate at a conversion speed greater than 45 kHz with an overall accuracy of 0 1%

Three power supplies are required, all of them have a common ground There are two noncritical supplies required at voltages of +12 and -27 volts One precision supply -5 12 volts is required as a reference voltage Since the precision of the conversion depends directly upon the precision of the reference supply, the tolerance allowed for the reference supply is less than 0 1%

The design is based on having a two-phase clock which is nonoverlapping and at standard MOS levels from 0 volts to -15 volts

The output of the converter is a 10 bit serial word As the logic diagram indicates, this output is buffered so that it comes out at standard MOS levels from 0 to -20 volts The buffer has a drive capability of 50 pF The capability of driving 50 pF should give sufficient margin to get from one package to another on a circuit board

The second output is a sync signal for the multiplexer The signal has a 2.2 μsec minimum pulse width at standard MOS levels It has the same drive capability as the data output It will drive 50 pF It is timed at the 10th bit of the conversion so that when a conversion is finished, while the A/D converter is recycling, the multiplexer is cycled to the next channel The sync output signal is intended specifically to set the counter advance of an PL 4S16C 16-channel Random/Sequential Access Multiplexer The sync output is shown on the right-hand side of the logic diagram The converter is intended to convert the input voltages between plus and minus five volts It is intended for the full military temperature range

2 0 FUNCTIONAL DESCRIPTION

This section gives a brief functional description of the operation of the A/D Converter The designation of the various elements refers to the logic diagram, Figure 1

2 1 Digital Logic

The flip-flop chain which consists of four flip-flops (A, B, C, and D) is clocked by a signal t'_{odd} This is one of the two phases of the incoming clock signal There is a buffer on the input The reason for the buffer is that we are required to have the substrate for the whole chip held to the most positive potential which, in this case, is +12 V We have an interface between standard MOS levels which are at ground and the chip where the substrate is at +12 Volts There is a buffer to make that conversion and a similar consideration requires a buffer on the other clock input The four flip-flops are used as a counter to count each incoming clock pulse There is a decoding network that decodes the 10th bit time, and that is then used in conjunction with the reset flip-flop (E) to reset the flip-flop chain and start the count over Also, there is a decoding gate that decodes the proper time to reset the whole converter

Flip-flop (Z) is used to hold a signal for a whole bit time to give the 2.2 μsec signal from the sync output for the multiplexer The reason for this is that the multiplexer specification requires a 1 μsec minimum pulsewidth to cycle so this guarantees a signal that is at least 1 μsec long The gates (M and N) are used to inhibit the clocks in the rest of the logic during the reset time They are enabled by signal $\overline{T}_o$ which only goes to zero during the reset interval

There is again a requirement for level shifting (gates O and P) The levels must be watched in two places One is in the capacitance switching transistors because there can be either polarity there, $\pm$5 volts, so the levels must be properly adjusted so that these transistors don't turn on unintentionally Furthermore, voltages must pass through two transfer gates to generate signals L_o and L_1 The voltage levels

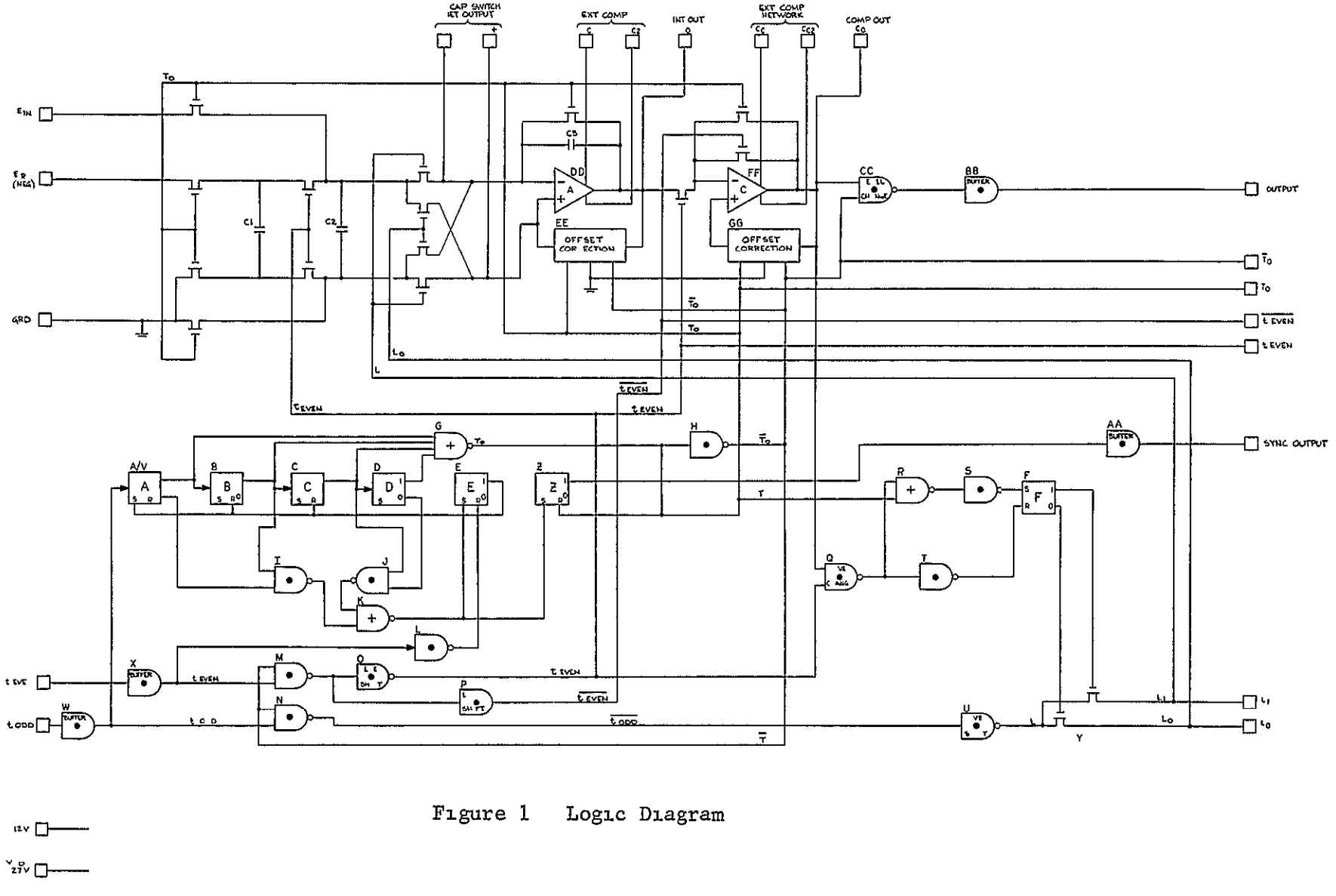


Figure 1 Logic Diagram

passing through must be sufficiently down so that these gates can be turned on

2 2 Decoding of Comparator Output

The network, which consists of several gates, flip-flop (F), and transfer gates is a network which is used to detect the polarity of the voltage on the operational amplifier and then to adjust the switches so that either one side or the other side is turned to apply the proper polarity charge to the input of the operational amplifier A complete conversion cycle will be described later which shows how they should operate

2 3 Capacitance Switching Network

The section containing capacitors C1 and C2 represent the capacitance switching network and the associated switches They first of all allow a reference voltage to charge C1 and an unknown voltage to charge C2 and then allow the associated charge transfer to the operational amplifier

2 4 Amplifier/Comparator

The two circuits called A and C are the same circuit They are just used in a little different way, one as an operational amplifier, the other as a comparator, and each has an offset correction network associated with it This network is intended to keep the offset within the required accuracy The reason for gates CC and O is that the comparator has an output swing between +5 and -5 volts To have this compatible with the rest of the logic on the chip requires a conversion of the levels to get back to standard voltage levels

3 0 CONVERSION CYCLE

The conversion cycle starts with a reset period when signal T_o is a one T_o is fed into the offset correction network It is also fed to MOS switches which are connected across both the amplifier and the comparator, which turn both the amplifier and comparator into unity gain amplifiers The output of the amplifier is applied across the capacitor in the offset correction network and since this is a unity gain voltage

follower the output voltage represents the offset voltage That voltage is inverted by switches and later on fed back to the input which cancels the offset voltage During T_o both clocks are being inhibited at gates M and N That means the amplifier and comparator are disconnected Also during T_o, there is a one into R which means a zero into S, which means a one at the set input to flip-flop F Flip-flop F is set and the transfer gate is turned on so that the next time t_{odd} comes through it will go through L1 This is so that during the first bit time, when the unknown voltage appears across C2, the switches are closed to connect the unknown directly to the operational amplifier In this way the polarity of the unknown voltage is known after it goes through the comparator Also, during T_o a set of four switches is energized, two of them connect an unknown voltage through capacitor C2 to ground and the other two connect the reference voltage, the -5 12V supply, to capacitor C1 and also to ground Capacitor C3, which is used for charge storage, is discharged during T_o also To summarize-at the end of the reset period the reference voltage, -5 12 V, is present across C1, an unknown voltage appears across C2, an offset correction has been performed on the amplifier, an offset correction has been performed on the comparator, flip-flop F is set to allow signal L1 to go through, and L1 when it occurs, will energize the proper switches so that the unknown voltage is connected directly across the amplifier

Now consider the first bit time of the clock signal t'_{odd}. At the end of T_o the opposite signal $\overline{T}_o$ is supplied to gates M and N so that these gates are no longer inhibited t'_{odd} goes through buffer W and will be inverted by gate N It is then inverted again and level shifted by U The reason for the level shifting is the need to have a higher voltage on the gate of the transfer gate than the voltage of the signal going through the gate Flip-flop F is already set and signal t'_{odd} appears as signal L_1 and connects the unknown to the input of the amplifier

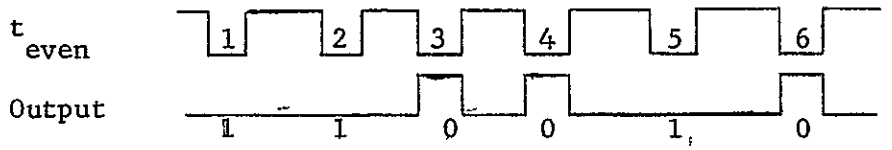
For an example, consider an unknown voltage of +3 volts Capacitors C2 and C3 are the same size (There is no requirement that they be identical although it makes the mathematics nicer if they are reasonably equal) So with +3 volts supplied to C2, when the gates are energized there will be +3 V supplied to the input of the operational amplifier, and that will charge up the output of the operational amplifier to -3 V So at the end of t'_{odd} (1) there will be a -3V signal on the amplifier output During this time the comparator is disconnected from the operational amplifier, and the comparator is held at ground The reason for this is to help speed in terms of the overall voltage swing of the comparator. It is held at ground and then swings to either ± 5 volts This cuts the voltage swing in half Otherwise it might be at -5 volts and then have to swing all the way over to +5 V

After t'_{odd} (1) goes off, Capacitor C2 is disconnected from the amplifier Then t'_{even} (1) occurs and is transferred through gates M and O Signal t_{even} (1) does a number of things First, t_{even} will connect the amplifier to the comparator Also $\overline{t_{even}}$ now disappears so the comparator is no longer a unity gain amplifier but rather an open-loop amplifier It will sense the -3 V present at the output of the amplifier and the comparator output will swing to +5 V During this time t_{even} is applied to the switches between C1 and C2 so C1 and C2 are connected in parallel When capacitors C1 and C2 are connected in parallel, the -5 12 V which is applied across C1 will divide, by the charge being divided equally between C1 and C2, and half the voltage will appear across C1 and half the voltage across C2 In other words, C2 will charge up to -2 56 V Also during t_{even} gate Q is enabled However, the comparator output went to +5 V So there is a zero at the other input of Q This keeps the output of Q at a 1 level, which keeps flip-flop F set Simultaneously the +5 V is inverted by gate CC and appears as a one at the output The output bit comes out as one indicating a positive unknown At the end of this time there is -2 56 V applied across C2 The switches now open and disconnect C1 from C2 A switch opens and

disconnects the comparator from the amplifier Also, a switch is closed and returns the comparator to a unity gain amplifier Then during t'_{odd} (2) a signal is again propagated through U which becomes L1 so that -2 56 V is now connected to the inverting input of the amplifier It will transfer +2 56 volts to the output Now there will be -440 mv left at the amplifier output The comparator will again swing to +5 V and again a one will appear as the output bit During the next parallel connection of C1 and C2, we start with 2 56 V and after connecting there will be 1 28 V across C1 and C2 During t_{odd} (3), +1 28 V is transferred to C3 It will appear at the output as a positive 1 28 V and that will overcome the - 44 V At the end of this time there will be +0 84 V at the output of the amplifier During the next t_{even} the plus voltage is sensed by the inverting comparator The comparator output will go to -5 V Now a zero output from the converter occurs A one now appears at the reset terminal of flipflop That is supposed to energize gate L_o for the next cycle

During t'_{odd} (4) signal L_o connects C_2 as an inverted capacitor to A The output of A goes to 0 84 - 0 64 = 0 2 volts During t'_{even} (4) L_o is removed and C_2 is disconnected from A C compares and its output goes to -5 V C2 is connected to C1 (C2 charges to -0 32 V) Flip-flop F is reset (the comparator output is -) for L_o A "0" appears at the output (Bit 3)

The output word and timing are such that the output only will have a zero level during t_{even} For the example discussed above the output would appear as



Therefore, the output should be sampled during t_{even} The question of a register to store the output word arose as a design consideration Since there are several intended applications for the converter, it was decided not to attempt to put a register on the chip Where a register

is required, there are numerous registers commercially available, either for serial in - serial out or for serial in - parallel out

To summarize the conversion cycle, it should be noted that the charge from the reference voltage is always added to capacitor C3 with a polarity that tries to drive the voltage across C3 to zero This results in a negative unknown voltage resulting in an output which is complemented Consider the following example

$E_{unknown} = -3$ V

1 During t_{odd} (1)
Output of A goes to +3 V

2 During t_{even} (1)
Comparator output goes to -5 volts
A "0" appears at output (negative input voltage)
Flip-flop F is reset for L_o
C_2 charges to -2 56 volts

3 During t_{odd} (2)
Output of A goes to 3 - 2 56 - 0 44 V

4 During t_{even} (2)
Comparator output goes to -5 volts
A "0" appears at output (MSB)
Flip-flop F stays reset for L_o
C_2 charges to -1 28 volts

5 During t_{odd} (3)
Output of A goes to 0 44 - 1 28 = -0 84 V

6 During t_{even} (3)
Comparator output goes to +5 volts
A "1" appears at output

The output word will therefore be

0 0 1 1 0 1 0 0 1 1 which is the complement of the actual word

The remaining consideration is the effect of offset voltages in the amplifier and comparator There will always be some offset voltage

present even though it may be small in comparison to the accuracy requirement of the converter To see what limitations this imposes consider an input of 2 56 volts The first bit of the output would be a 1, then during $t_{odd}(2)$ the output of the amplifier would go to $\pm E$ offset

E_{oc} represents the input offset after offset correction has been performed and is equal to $\frac{E_o}{1 + A}$ where E_o is the actual input offset and A is the open loop gain At the output of the comparator during t_{even} (2) this voltage will appear as $\frac{E_o A}{1 + A} \approx E_o$ Since a zero or small voltage at the output of the comparator is treated as +5 volts, the output will be a 1 During the next t_{odd} 1 28 volts will be transferred to C_3 and the output thereafter will be a string of zeros

The ± 5 volt swing of the amplifier is dictated by the voltage swing to be allowed for on C3 For design simplicity, the same design is used for the amplifier and comparator, thus the comparator also has a ± 5 volt output swing capability The gain is dictated by the requirement that the offset voltage after correction be much smaller than the accuracy requirement of the converter (5 mV). In order to allow uncorrected offsets of up to 0 5 volts, this requires a gain greater than 10^3

4 0 DETAILED DESIGN CONSIDERATIONS

4 1 Timing and Digital Logic

Now we consider the timing and the digital logic For reference refer to the logic and timing diagrams The time scale indicated is a microsecond per major division At the top of the timing diagram are the two-phase clock inputs, t'_{odd} and t'_{even} The next four waveforms indicated are the one outputs of flip-flops A, B, C and D The four flip flops comprise the counter The counter starts out with a count of 16 (1, 1, 1, 1) This is the first bit time of the conversion The counter proceeds to count down from 16 0, 1, 1, 1 is the next state that occurs shortly after two microseconds. Flip-flop A's 1 output goes to a 0 and the other three flip-flops stay at 1 Then it counts to 1, 0, 1, 1 which appears between 4 and 6 μs. The counter proceeds to count in that manner until the 10th bit time when t'_{odd} occurs at 18 μsec At that time, the 1 output of flip-flop A is a 0, flip-flop B and C are both 1's, and flip-flop D is a 0, and that is decoded to recognize the 10th bit time

and to start the reset cycle For decoding, gates I and J are used The inputs to I and J are all 1's so that their outputs are both 0 With both inputs to gate K zero, it has a 1 out. This 1 is applied to the set terminal of flip-flop E This flip-flop is also driven by what could be called $\overline{t'_{even}}$ During the 10th bit time of t'_{odd}, although a 1 is being applied to the set line, there is also a 1 in the reset line The flip-flop does not change state at that time but has to wait until the end of the bit time. At the end of t'_{odd}, t'_{even} goes to a 1 which means that there is now a 0 applied to the reset terminal Flip-flop E is now free to toggle. Therefore, flip-flop E gets set at the 10th bit time of t'_{even} At that time, a 1 is generated by flip-flop E and that is used to set flip-flop A and reset flip-flops B and C This forces flip-flops A, B and C to assume the states shown at the 10th bit time of t'_{even} Flip-flop A is a 1, flip-flops B, C and D are 0 At the start of the 11th bit time t'_{odd} toggles flip-flop A so that it goes to 0 After the 11th bit time of t'_{odd} the counter is in the 0, 0, 0, 0 state At the first bit time after the reset interval, all four of the flip-flops toggle and go to 1's The basic timing is indicated on the timing diagram and to toggle all four of the flip-flops takes about 200 ns How long it takes to toggle all four flip-flops is not crucial They must do it within a whole bit time which is 2 μsec They need not toggle any faster

The decoding of the reset interval is done by decoding the arrival of the 0, 0, 0, 0 state That is done with NOR gate G It is a four input NOR-gate and when all four inputs are at 0, then there is a 1 out, which is the T_o signal It is inverted and used also as a $\overline{T_o}$. There is a requirement that that signal snap off promptly at the end of the reset interval It will because as soon as any one of the inputs to G goes to a 1, the output goes to a 0 T_o performs the offset correction and the resetting of the whole converter and supplies the unknown voltage and reference voltage to the capacitors R forces the flip-flops to assume a 0, 1, 1, 0 count at t'_{even} of the 10th bit time. What would be the 12th bit time is the first bit time of the next conversion cycle The flip-flops then go to all 1's and as soon as any one of them changes, the gate generating T_o is released and this ends the reset signal

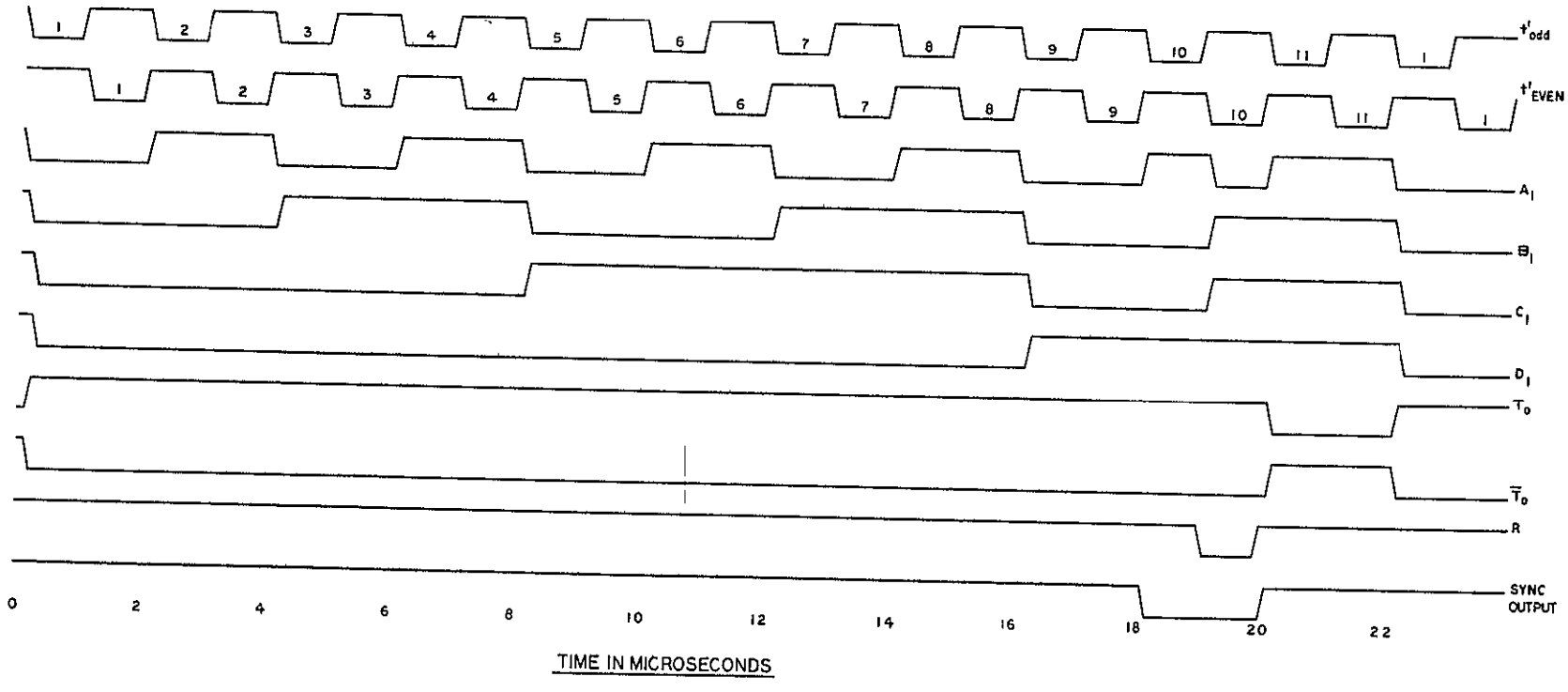


Figure 2 Timing Diagram

When the converter is first turned on, no matter what state it is in, it will start counting If it starts somewhere between 16 and 6, it will count down and reset will occur If it starts somewhere between 5 and 0, again it will count down to 0 and then start with the proper count So it cannot be locked up in a false state No matter what state the flip-flops are in when power is applied, they count until the normal conversion cycle begins

The other signal indicated on the timing diagram is the signal that goes out to the multiplexer This is generated by taking the signal which sets flip-flop E and using it to set flip-flop Z. This gives a 1 out which is not inverted, but is buffered. The signal would start at t'_{odd} of the 10th bit time It starts at the beginning of the last bit of the conversion and T_o is used to reset it.

The digital logic is based on a standard inverter design, Figure 3

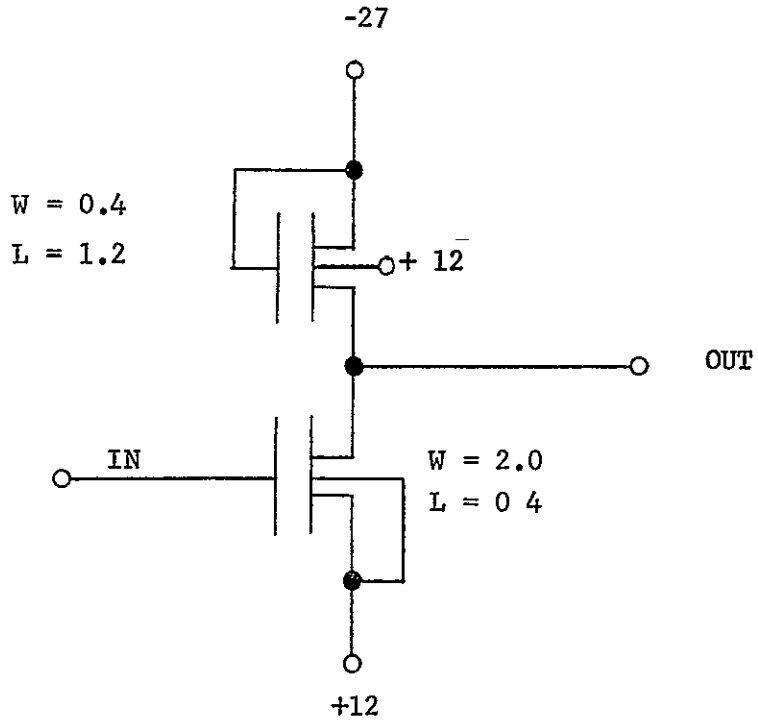


Figure 3. Standard Inverter Design

These are the dimensions of the devices as drawn on the composite The converter is built with a shallow diffusion process, and we have allowed for underdiffusion from both sides of 0.1 mil total The effective lengths of the inverter are less than the drawn sizes by this amount With this ratio of inverter sizes, the input levels would be +11.4 V for the 0 level and -21.6 V for the 1 level This inverter design thus allows a noise margin of better than 1.5 V The design limits for threshold voltage are 2.5 V $\pm$0 5 V The minimum threshold voltage would be 2 V and with 12 V on the source it would take a 0 level at +10 V to turn on. -21.6 V gives sufficient drive capability for the 1 level and results in a 32 V swing. The speed is a function of the capacitance being driven. With this inverter ratio there is more than sufficient speed The worst case path for propagation delay appears to be for signals t_{even} and t_{odd} which have to propogate through three levels of logic. However, the inverters are driving very low, on-the-chip, capacitances and the speed is more than sufficient The worst case, as far as an inverter is concerned, would be going from a 0 to a 1 This is because it has to charge the capacitance through a load device which is normally small and drawing a small current To charge the capacitance would take longer than it would to discharge it through the inverter device which is relatively much larger

The 1 level voltage has the sensitivity of the threshold voltage Effectively the voltage drop across the load device is the actual threshold voltage of the device plus the contribution to the effective threshold due to the substrate voltage If the threshold voltage changes $\pm$0.5 V, effectively the 1 level changes by $\pm$ 0 5 V There is such a big drive on the inverter that, if the threshold changes half a volt, it cannot be seen at the output of the inverter For a 1 V change in the overall threshold, from 2 V to 3 V, the 0 level changes .10 V so that the inverter design is insensitive to threshold voltage. The inverter is the basic component that makes up all the NOR gates The NOR gates use inverter devices in parallel They are all the same size so the same inverter ratios are used For the single input Nand gates that are used in gates such as L, O, S, T and for the unclocked flip-flops E, Z and F, the same inverter ratios are used. The set and reset of

flip-flops E, Z and F use a pair of devices and again the same inverter ratio is used For a two input Nand gate essentially the same concept was used The same load device, width 4 mil and length 1 2 mil, was used Because of stacking of voltage across two inverter devices, the inverter devices are designed with twice the width So their width is 4 mils and length 4 mil This represents the structure of all the two input Nand gates.

The "clocked" flip-flops start out like the unclocked ones They have a pair of cross-coupled gates Again the same inverter ratio is used for the load 4 length and width 1 2 mils, for the inverter devices width 2 mils and length 4 mil

Refer to the schematic for operation of the "clocked" flip-flop Assume that a clock input is present at the input of flip-flop A The clock signal is t'_{odd} and the inverted clock signal is $\overline{t'_{odd}}$ and is applied to devices 3 and 13 Now let us assume a particular state with one output (device 3) a 0 and the other (device 13) a 1 Device 8 is on and device 9 is off The inverted clock signal $\overline{t'_{odd}}$ is present so that device 3 will be turned on. Its output is a 0 level so that the gate of 4 will see a 0 level. If we go to the other side, a parallel effect is occurring $\overline{t'_{odd}}$ is present, device 13 is on, and the 1 level will pass through device 13 and appear at the gate of device 12 and will turn it on With t'_{odd} not present, device 5 is off as is device 11 When t'_{odd} appears, the picture is reversed. t'_{odd} turns on devices 5 and 11 while devices 3 and 13 are turned off There is a 0 stored on the gate of device 4 which keeps this device off Even if device 3 is turned on there is no current path However, a 1 is stored on device 12 which turns it on, and with device 11 on will provide a path to $\pm$12 volts This will turn off device 8 and turn on device 9 Therefore the flip-flop will change state To summarize the flip-flop operation, assume the right hand side of flip-flop A is at a 1 level, device 13 is turned on which traps charge on the gate of device 12 After device 13 goes off, device 11 is turned on and device 12 is on due to the trapped charge This provides a path to +12 volts which will make the right hand side of the flip-flop go to a 0 level

In the process of designing the flip-flop it was found that the voltage change applied to the gate of device 3 was being fed through to

the gate of device 4 There is a capacitance voltage divider there The 0 levels were to the point where device 4 was just barely turned on Rather than permit a design which had an obvious problem, another cross-coupled set of devices was added Devices 77 and 78 in flip-flop A were cross coupled in the manner shown If we again consider the case then the output of flip-flop A on the right hand side is at a 1 level, when device 13 is turned on, device 77 will also be turned on, forcing the zero level on the gate of device 4 to +12 volts

In terms of device sizes, the same concepts were followed The flip-flop is formed of inverters and Nand gates The ratios are the same as for the previous inverters and Nand gates The cross-coupling devices (77 and 78) are small since all we have to do is transmit this charge from node to node.

Since the flip-flops require a clock and an inverted clock, the first flip-flop has an inverter preceding it This is a standard inverter and is included in the symbol on the logic diagram The flip-flops change state on the negative transition. There is a change in state when the clock goes negative Since an inverter is needed with the first flip-flop, that could have been carried through all the flip-flops However, flip-flop A has both the 1 output and the 0 output available so those are used to drive B, etc. Since both signals are available this eliminates the need for an inverter in flip-flops B, C, and D

The buffers for the clock inputs to the chip require as an output a level that goes from +11 to a substantial negative voltage The input is standard MOS levels, -1 V to -20 V, so it is a level shifter It provides a voltage swing between +11 and -14 4 The stage connected to -27 V is simply a source follower and the voltage swings at the output tend to follow the voltage swings at the input This is simply a voltage level translating scheme There is no inversion, and the stage was designed so that -1 volt on the input gate gives +11 V on the output The input swings 22 volts in the negative direction and the output will swing 25 volts actuating the circuits that follow Gain is achieved for the following reason With -1 V at the input, device 4 is unsaturated It has a small resistance because there is only 1 V dropped across it As the output voltage climbs up, it goes into saturation, and

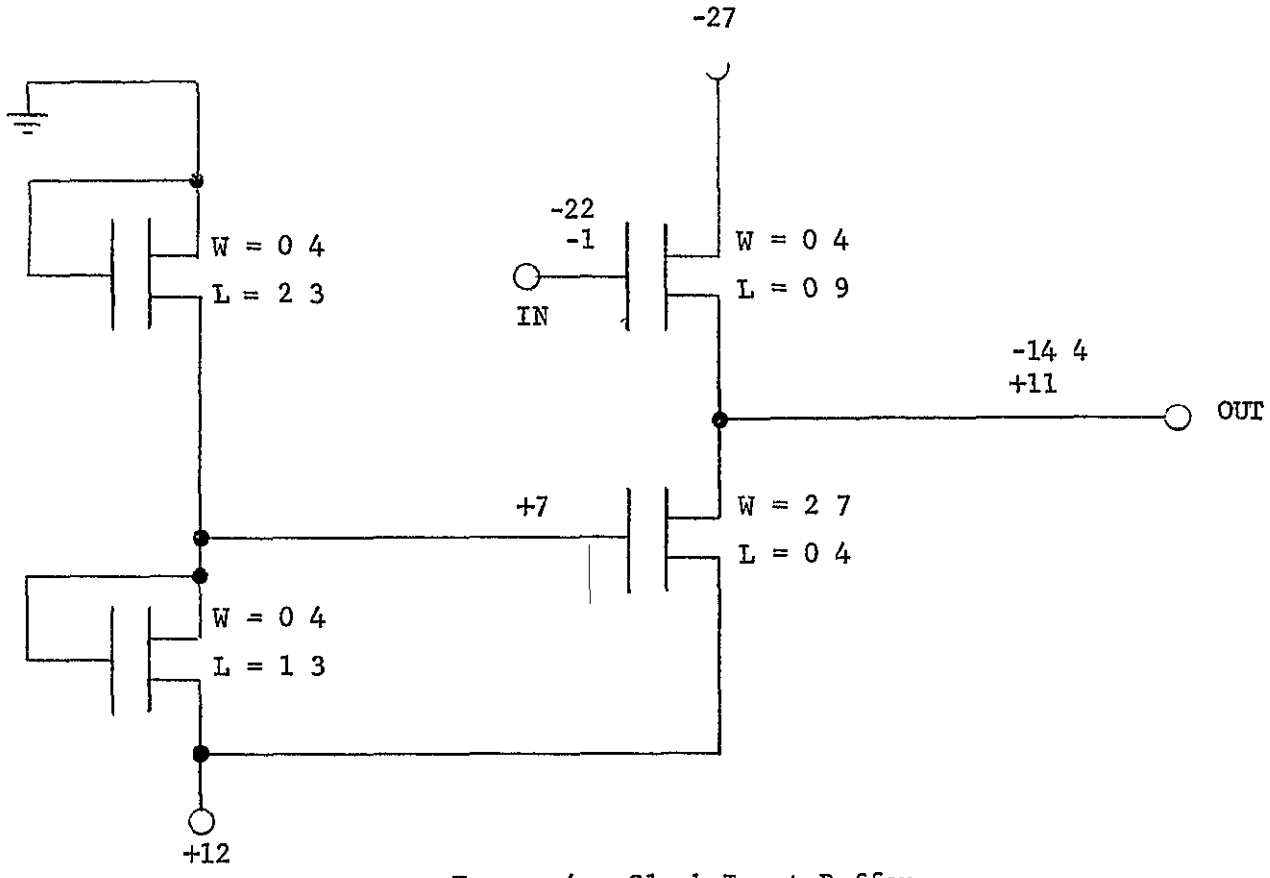


Figure 4. Clock Input Buffer

the resistance increases It operates along a line of constant gate voltage It starts with 1 V across it with a low resistance and the drain to source voltage is forced to increase as more current is supplied by device 3. This increases the resistance and some gain is achieved. Devices 1 and 2 are a voltage divider They divide 12 V into +7 to provide a constant gave voltage to device 4

The input portion of the level changing circuit is shown in Figure 5 It feeds a stage identical to a clock input buffer The device sizes and voltage swings are shown When the input goes from -5 to 0 to +5, the output of the clock input buffer circuit goes from -4.4 to +10 2 to +11 2 The entire circuit was deliberately designed so that it does not discriminate between +5 and 0 volts. The reason for this is that when the comparator is connected in the unity gain configuration, a 0 level is desired so that some spurious signal is not introduced into gates T or R The swing achieved between 0 and -5 is a substantial swing. It is about a 15 V swing and will drive MOS. The circuit could be translated to ground if all the +12 points were ground and we had a -39 V supply. Then 0 volts becomes negative 12 volts If it were desired to drive this chip from DTL or T^2L instead of MOS the design just discussed could be used for that purpose The circuit is designed to go from a 5 V swing (-5 to 0) to MOS levels (-16 4 to -1.8 V) if the circuit is referred to ground

4 2 Amplifier and Capacitance Switching Network

First, consider the capacitance switching network (Figure 6) This figure shows the p-n back biased junctions that are associated with each of these capacitors These capacitors have a metal plate over about 1000Å of silicon-dioxide The capacitance switching network is laid out so that it is symmetric Where we have one MOS device, there is another in parallel The reason this was done is to avoid errors due to capacitance feedthrough. If a signal is present to turn device 147 on, then device 146 is turned on so that C1 sees equal and opposite feed-through from the two devices If device 146 was not present then there would be a voltage divider formed Most of the voltage would appear across the feedthrough capacitance but there would be a voltage that would appear as well across capacitor C1. This could result in charge being trapped on C1 when device 147 is turned off with a resulting error

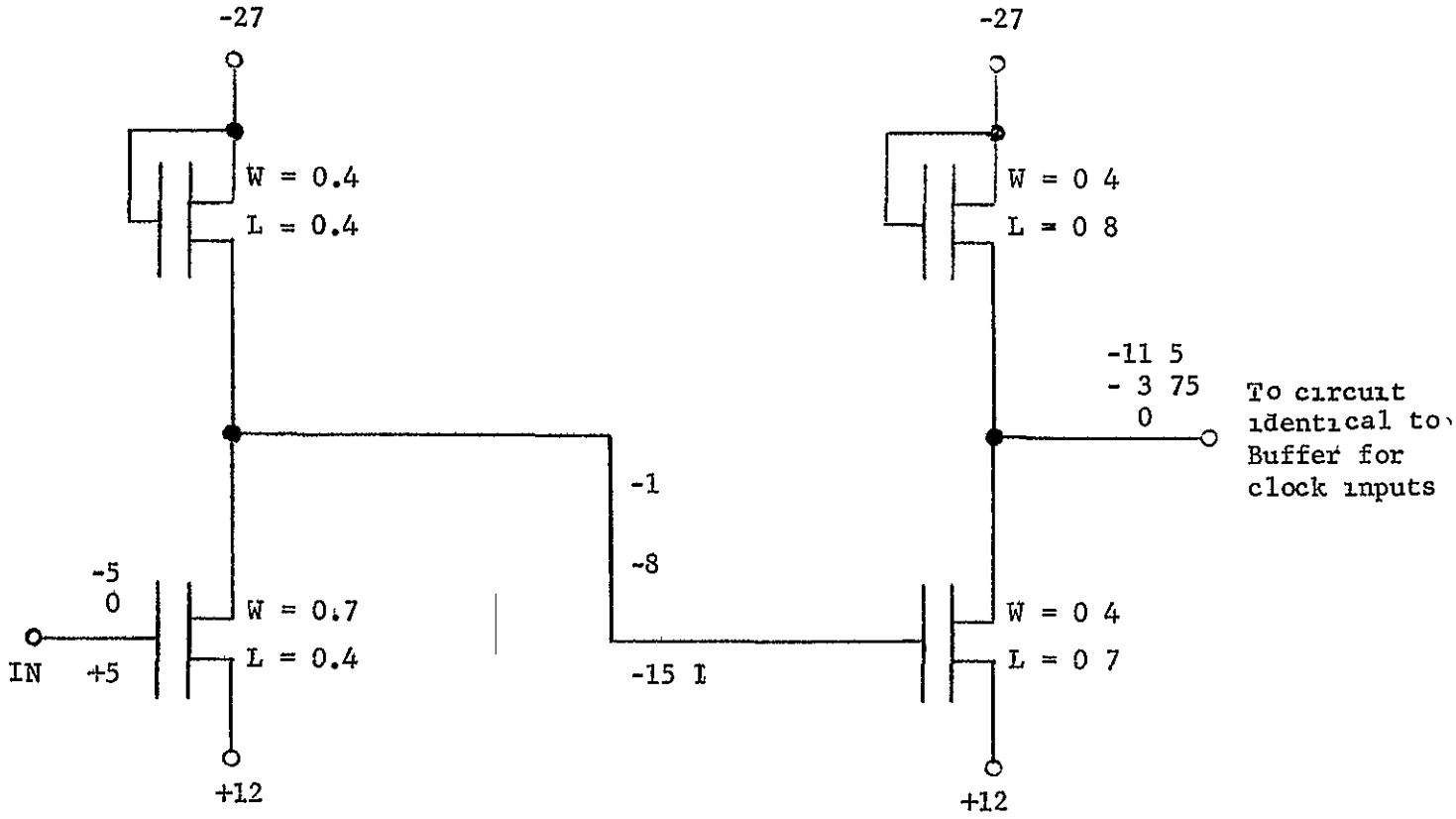


Figure 5. Input Portion of the Level Changing Circuit

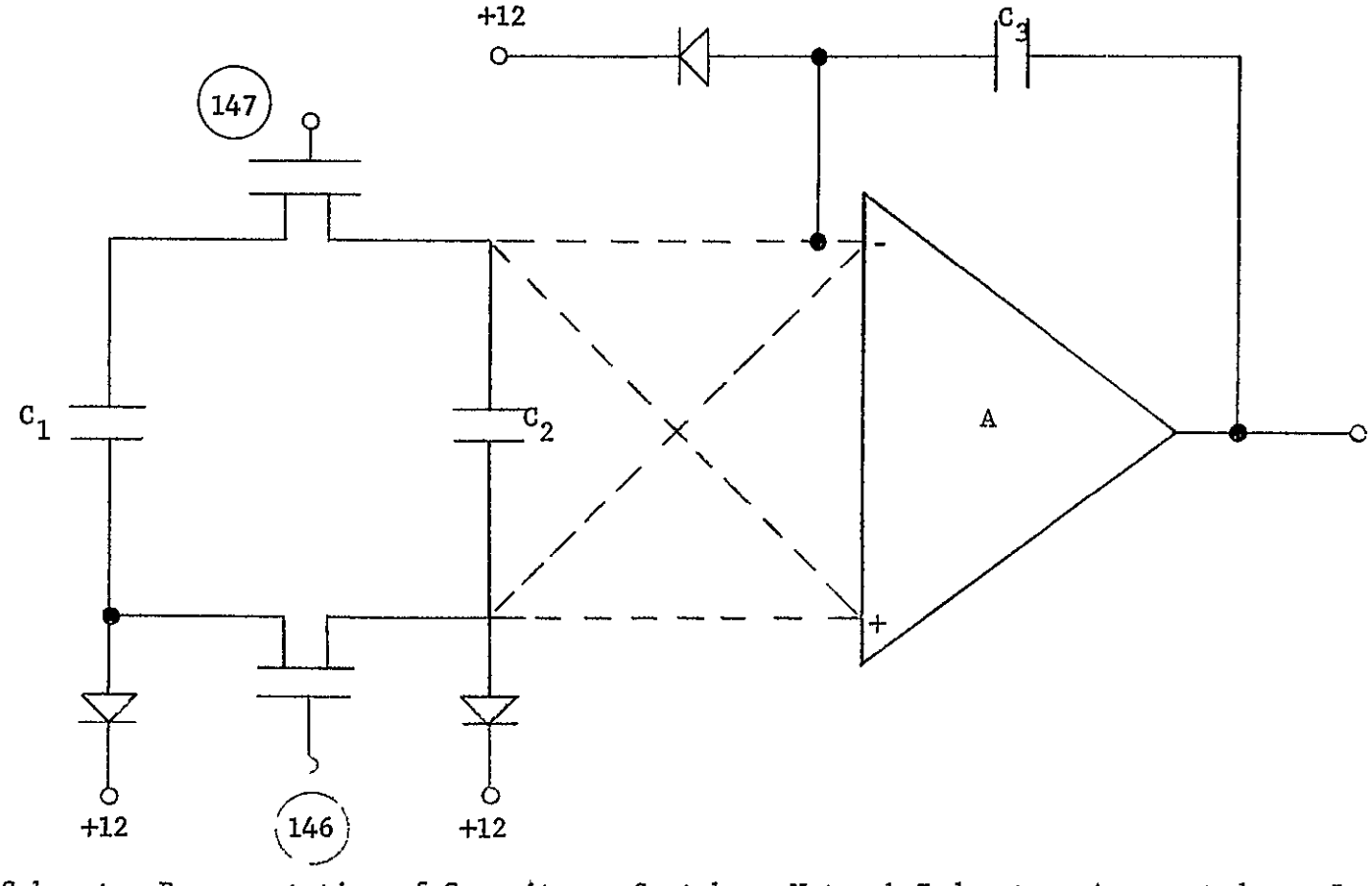


Figure 6 Schematic Representation of Capacitance Switching Network Indicating Associated p-n Junctions

being introduced. When we have two devices which are symmetric and the same size, we expect the feedthrough capacitance to be the same Whatever charge is transferred in one path will also be transferred in an equal amount in the opposite direction in the other path and the net voltage change across capacitors C1 or C2 will be zero. Therefore, the capacitance switching network is laid out as symmetrically as is possible The symmetry carries through all the way from the input to the operational amplifier There are two switches which allow the reference voltage to charge capacitor C1 These are two switches which connect the two capacitors in parallel and there are two switches which allow the input voltage to be placed across capacitor C2. There are two switches that connect C2 to the operational amplifier and two which invert if we want to invert the polarity A number of schemes for connecting these capacitors were examined But, the critical feature, which was examined in detail, is that there is a voltage variable capacitor across each of the diodes. This is the capacitance associated with a back biased p-n junction Initially when the reference voltage is charging capacitor C1 and the unknown voltage is charging the capacitance C2, both of the lower nodes on C1 and C2 are connected to ground. Each of these lower capacitor nodes is at ground potential which means that the capacitor associated with the back biased p-n junction is charged up to 12 V Now if we examine what happens as we carry through some of the operations of the A/D converter we find the input of the amplifier, when operating, is at virtual ground The amplifier will have a gain greater than 1000 and even with volts out, the bias potential at the input can only be a few mV So, for all practical purposes, the input is at ground When capacitor C2 is connected to the input of the operational amplifier by the set of switches then the ground potential at the lower node of C2 will be connected to a virtual ground There will not be any charge transfer through the capacitance associated with the back biased p-n junction. The other situation that occurs is when capacitors C1 and C2 are being connected in parallel In this case again both nodes are at ground potential and connecting them together does not change that If the cross coupling switching occurred between the capacitances then one of the capacitor-junction nodes would have to be at a potential other than ground As soon as the potentials are changed from ground, a charge will be displaced

which will affect the voltage across C1 or C2 That is the reason the cross coupling network was placed between Capacitor C2 and the operational amplifier

The p-n junction associated with the capacitances dictated the size of C2 and consequently the sizes for C1 and C2 There will be a leakage current through the diode and the worst case leakage current is estimated as 1nA The governing equation is

$$I = C \frac{dv}{dt} \quad \text{or} \quad \Delta V = \frac{1}{C} I \Delta t$$

The output voltage is required to stay within a millivolt for 20 μsec Inserting numerical values gives a capacitance of 20 pF This capacitance was chosen on the basis of the leakage current through the substrate diode and the requirement that the output voltage should not change by more than a millivolt in the entire 20 μsec conversion period The device sizes used in the capacitance switching networks are 3 mil by 0 4 mil Once the capacitances are chosen, sizes for these devices are established from a calculation of the effective on resistance of the switch, taking into account the voltage levels applied to the switch The operating levels applied to the switch are chosen to allow an input of either ± 5 volts, since the operating range of the converter is to be plus or minus 5 volts If +5 V is applied at the input and the device has a 2 5 V threshold, then if +2 5 V were applied to the gate, the switch could be on To avoid that problem, the voltage levels used are +4 volts and -20 volts

The mask layout of the capacitance switching network is symmetric to enhance the balance to compensate for capacitance feedthrough from the gate overlap capacitances When the masks are cut, the gates have specified dimensions However, in the process of diffusing in the source and drain regions there is an underdiffusion which results in a gate overlap capacitance The capacitances between gate-source and gate-drain may become unbalanced due to mask alignment errors However, by using a symmetrical layout, not only schematically, but physically, any unbalance in one transistor is reflected in its balancing transistor For example, suppose that the masks were misaligned so that one transistor had a larger gate-drain than gate-source capacitance. This would mean that the balancing transistor would have the same capacitive unbalance and hence the capacitive feedthrough voltages would still cancel

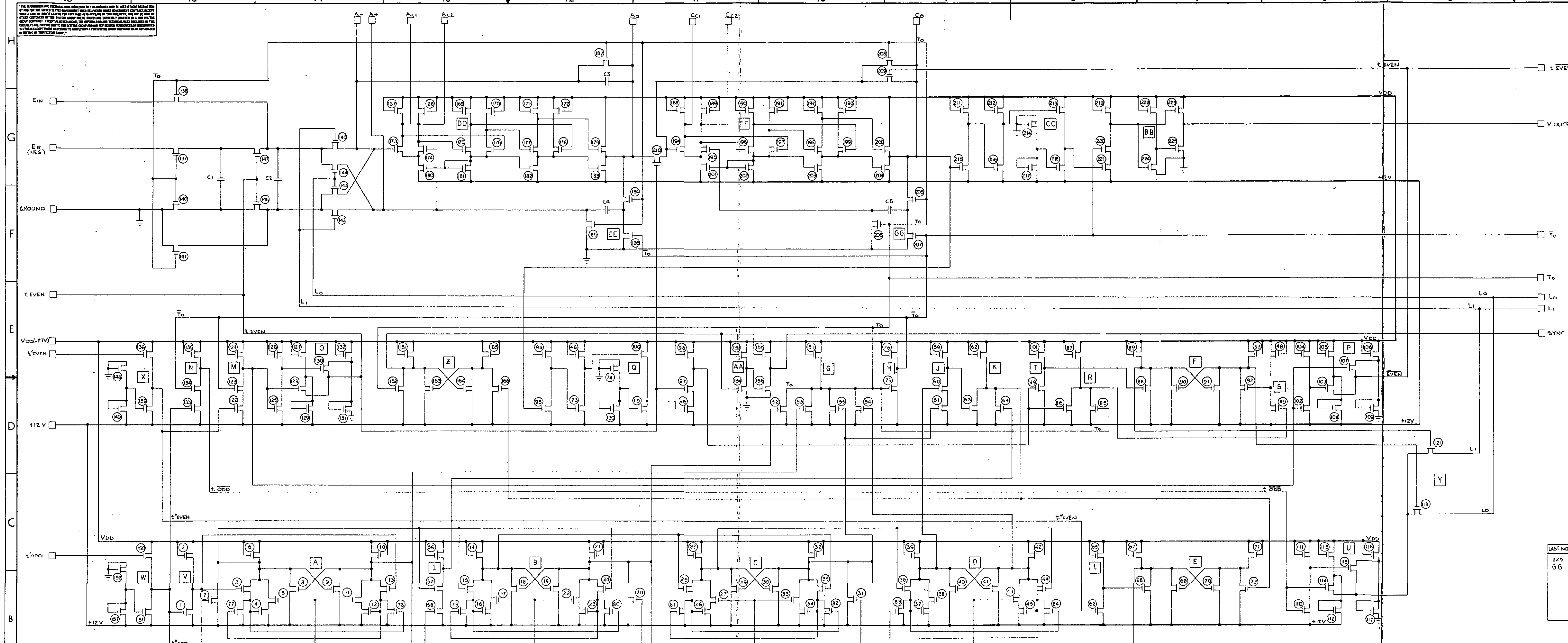
In addition, the voltage swings to t_{even}, L_1 and L_o have been reduced as described previously This has the effect of reducing the feedthrough voltage if any mismatch exists

Capacitors C1 and C2 must be matched in order to obtain the required accuracy The matching requirement has been investigated analytically and it was shown that the capacitors must be matched to within the overall accuracy of the conversion To obtain a conversion accuracy of 0 1%, capacitors C1 and C2 must be matched to within 0 1%

There is no requirement that C3 be matched with C1 and C2 C3 can, theoretically, be any value. The reason it can be any value is that, if you think in terms of charge instead of voltage, you start with a charge representing your unknown voltage on C2. You deliver that charge to C3 and then start dividing down the charge on C1 by halves That charge is delivered to the input of the operational amplifier and is transferred, inverted, and placed on C3. In principle the capacitor C3 would have any value Q = CV so for a given charge if the capacitor is bigger, the voltage is smaller When capacitor C2 is charged and connected to the operational amplifier input, the output will drive an equal and opposite amount of charge into it to force the input back to virtual ground

There are practical limitations on the value of C3 If C3 were small with respect to C2, large voltage swings would be required at the amplifier output If C3 were 2 pF instead of 20 pF and C1 and C2 were still 20 pF, this would require 50 volt swings instead of 5 volt swings On the other hand, if C3 were 200 pF, then there would be about half a volt swing at the amplifier output The swings would be of the order of any offset in the comparator It does not appear that it is desirable to compress the voltage swings The desirable situation seems to be when there is a one to one correspondence in voltage swings

The configuration for the amplifier for the unit is shown on the A/D converter schematic (Figure 7), Devices 167 through 183 This has a dc gain of about 1600 or 68 db It is composed of three differential stages and a source follower level shifting stage on the output. The supply voltages are +12 to -27 V and the output swings about ground It is apparent that differential stages are required to tolerate variations in power supply voltages and to tolerate different threshold voltages The design philosophy for this converter is a design which is



DEVICE SIZES IN MILS											
DEVICE NO.	WIDTH	LENGTH	DEVICE NO.	WIDTH	LENGTH	DEVICE NO.	WIDTH	LENGTH	DEVICE NO.	WIDTH	LENGTH
1	4.0	0.4	61	4.0	0.4	121	2.0	0.4	181	2.3	0.4
2	0.4	1.2	62	0.4	1.2	122	4.0	0.4	182	4.6	1.5
3	0.8	0.4	63	2.0	0.4	123	4.0	0.4	183	4.5	0.4
4	4.0	0.4	64	2.0	0.4	124	0.4	1.2	184	1.0	0.4
5	4.0	0.4	65	0.4	1.2	125	2.0	0.4	185	1.0	0.4
6	0.4	1.2	66	4.0	0.4	126	0.4	1.2	186	1.0	0.4
7	2.0	0.4	67	0.4	1.2	127	0.9	2.1	187	1.0	0.4
8	2.0	0.4	68	2.0	0.4	128	2.0	0.4	188	0.4	6.0
9	2.0	0.4	69	2.0	0.4	129	3.3	0.4	189	0.4	6.0
10	0.4	1.2	70	2.0	0.4	130	2.0	0.4	190	0.4	6.0
11	4.0	0.4	71	0.4	1.2	131	0.4	1.0	191	0.4	6.0
12	4.0	0.4	72	2.0	0.4	132	1.7	0.4	192	0.4	6.0
13	0.8	0.4	73	0.4	0.7	133	4.0	0.4	193	0.4	6.0
14	0.4	1.2	74	0.4	2.3	134	4.0	0.4	194	6.0	0.4
15	0.8	0.4	75	2.0	0.4	135	0.4	1.2	195	6.0	0.4
16	4.0	0.4	76	0.4	1.2	136	0.4	0.9	196	6.0	0.4
17	4.0	0.4	77	0.4	0.4	137	1.0	0.4	197	6.0	0.4
18	2.0	0.4	78	0.4	0.4	138	1.0	0.4	198	6.0	0.4
19	2.0	0.4	79	0.4	0.4	139	2.7	0.4	199	6.0	0.4
20	2.0	0.4	80	0.4	0.4	140	1.0	0.4	200	12.0	0.4
21	0.4	1.2	81	0.4	0.4	141	1.0	0.4	201	2.1	0.4
22	4.0	0.4	82	0.4	0.4	142	3.0	0.4	202	2.3	0.4
23	4.0	0.4	83	0.4	0.4	143	3.0	0.4	203	4.6	1.5
24	0.8	0.4	84	0.4	0.4	144	3.0	0.4	204	4.5	0.4
25	0.8	0.4	85	2.0	0.4	145	3.0	0.4	205	1.0	0.4
26	4.0	0.4	86	2.0	0.4	146	3.0	0.4	206	1.0	0.4
27	4.0	0.4	87	0.4	1.2	147	3.0	0.4	207	1.0	0.4
28	0.4	1.2	88	2.0	0.4	148	0.4	2.3	208	1.0	0.4
29	2.0	0.4	89	0.4	1.2	149	0.4	1.3	209	1.0	0.4
30	2.0	0.4	90	2.0	0.4	150	0.4	0.9	210	1.0	0.4
31	2.0	0.4	91	2.0	0.4	151	2.7	0.4	211	0.8	0.7
32	0.4	1.2	92	2.0	0.4	152	0.4	2.3	212	0.4	0.8
33	4.0	0.4	93	0.4	1.2	153	0.4	1.2	213	0.4	0.9
34	4.0	0.4	94	0.8	0.7	154	2.0	0.4	214	0.4	2.3
35	0.8	0.4	95	0.9	0.4	155	2.0	0.4	215	0.9	0.4
36	0.8	0.4	96	6.0	0.4	156	2.0	0.4	216	0.4	0.7
37	4.0	0.4	97	4.0	0.4	157	0.4	1.3	217	0.4	1.3
38	4.0	0.4	98	0.4	6.0	158	—	—	218	2.7	0.4
39	0.4	1.2	99	4.0	0.4	159	—	—	219	0.4	6.0
40	2.0	0.4	100	0.4	0.9	160	—	—	220	4.0	0.4
41	2.0	0.4	101	0.4	1.2	161	0.4	1.2	221	6.0	0.4
42	0.4	1.2	102	2.0	0.4	162	2.0	0.4	222	0.4	1.2
43	4.0	0.4	103	2.0	0.4	163	2.0	0.4	223	2.0	0.4
44	0.8	0.4	104	0.4	1.2	164	2.0	0.4	224	2.0	0.4
45	4.0	0.4	105	0.9	2.1	165	0.4	1.2	225	2.0	0.4
46	0.4	0.8	106	1.7	0.4	166	2.0	0.4			
47	—	—	107	2.0	0.4	167	0.4	6.0			
48	0.4	1.2	108	3.3	0.4	168	0.4	6.0			
49	2.0	0.4	109	0.4	1.0	169	0.4	6.0			
50	—	—	110	2.0	0.4	170	0.4	6.0			
51	0.4	1.2	111	0.4	1.2	171	0.4	6.0			
52	2.0	0.4	112	3.3	0.4	172	0.4	6.0			
53	2.0	0.4	113	0.9	2.1	173	6.0	0.4			
54	2.0	0.4	114	2.0	0.4	174	6.0	0.4			
55	2.0	0.4	115	2.0	0.4	175	6.0	0.4			
56	0.4	1.2	116	1.7	0.4	176	6.0	0.4	C1	10.0	10.0
57	4.0	0.4	117	0.4	1.0	177	6.0	0.4	C2	10.0	10.0
58	4.0	0.4	118	2.0	0.4	178	6.0	0.4	C3	10.0	10.0
59	0.4	1.2	119	2.7	0.4	179	12.0	0.4	C4	10.0	10.0
60	4.0	0.4	120	0.4	1.3	180	2.1	0.4	C5	10.0	10.0

LAST NO. USED	NO'S NOT USED
225 GG	47, 50, 158, 159, 160

5. ☐, ○ INDICATES IDENTIFICATION MARKING AND IS FOR REF ONLY
4. FOR ASSY DWG SEE X260049
3. FOR DIE NO SEE X260050
2. FOR LOGIC DIAGRAM SEE X256460
1. IDENTIFICATION MARKING PER PR 12-1
TYPE ____ CLASS ____ PART NUMBER ____

NOTES: UNLESS OTHERWISE SPECIFIED

TRW
ONE SPACE PARK · REDONDO BEACH, CALIFORNIA

SCHEMATIC DIAGRAM – MOS A/D CONVERTER A/D-01

SIZE J | CODE IDENT NO. 11982 | X258625

FRAME 11982 X258625 REV B

FOLDOUT FRAME 1

FOLDOUT FRAME 2

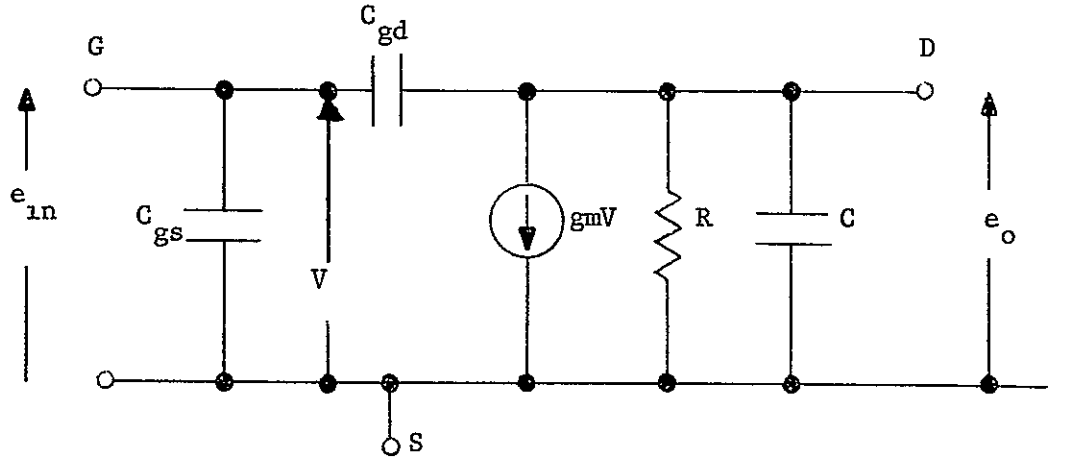
FOLDOUT FRAME 3

not critical in the sense of not requiring a threshold voltage accurate to 5 significant figures. Sufficient margin exists both in the digital part and in the analog part so that if wafer fabrication results in a threshold voltage of 2.8 V or 2.3 V, the converter will work in both cases. An amplifier with a single differential stage was designed first. A fixed voltage was assumed for a current source, transistor 180. The amplifier had load transistors, 167 and 168, and amplifying transistors, 173 and 174. The length is 6 mils and the width is 0.4 mils for the load transistors and the values are inverted for the amplifying transistors. These were chosen to give a large gain per stage, of the order of 15 to 16, which results from the ratios chosen. These are transistor sizes that can be fabricated and that will work effectively. The properties of the single stage were examined and they gave excellent power supply rejection although more gain was needed. The succeeding stages are differential to take advantage of the fact that an additional gain factor of 2 results from going differential rather than single ended. There are three differential stages with their associated load transistors and also current sources for the three stages which incorporate common mode feedback which is fed back from the drain of transistor 181 to the gate of transistor 180.

One of the most difficult problems in the dc design occurred in the output stage. The voltage levels keep climbing in succeeding stages. When the output is reached, there is 18 V at the drain of transistor 177 which is the dc operating level of that stage. The output of the amplifier must swing ± 5 V about ground. It is easy to get the negative swing at the output because device 179 is hooked directly to the -27 V supply. If it is turned on hard, that is, if the voltage on the gate of device 179 goes to -18 V, the output will swing negative. However, +5 is reasonably close to +12 V and it is hard to design the output stage to get that swing. After several tries a design was achieved where there is a nominal 5 V swing but an actual 6 V swing. This gives a design with a volt margin. This amplifier is used for the comparator as well.

There is a stability problem associated with closed loop operation of the amplifier. A simple model for an individual stage is considered, which has an input appearing across the gate to source capacitance, an overlap feedback capacitance C_{gd} and a current source. R represents the

load resistance The output capacitance could be either an overlap capacitance across the load device or due to the few mils of p-region connecting the amplifying and load devices together There is capacitance to the substrate and capacitance to ground at that node The parallel combination of those would represent capacitance C



If this simple circuit is examined and the transfer function is determined, you find a zero in the right hand plane and a pole in the left hand plane which are basically the RC product

$$\frac{e_o}{e_{in}} = K \frac{S - gm/c_{gd}}{S + \frac{1}{R(C_{gd}+C)}}$$

If the numbers are examined, the RC product results in a pole at about 1 MHz and the zero at about 1.5 GHz When the dc design was complete, two parallel efforts were undertaken An MOS circuit analysis computer program was used to simulate every part of the converter with one exception The one thing that the program cannot do is simulate a circuit where a capacitance is applied between two modes. It was not able to simulate the capacitance switching network where there are capacitances between modes. AC analysis was used to determine the magnitude and phase characteristics between the inverting input and the output When the results were plotted and examined in the vicinity of the unity gain crossover frequency, there is a phase contribution of 60^{o} per stage

This indicates three poles at the corner frequency which is about a megacycle At this frequency the problem is analogous to the classical RC coupled amplifier problem As you sweep over the frequency range each stage contributes phase shift and the amplifier becomes unstable with 180^{o} total phase shift There are three stages and when the frequency range is swept as soon as there is 60^{o} phase shift per stage, the amplifier becomes unstable If the phase change per stage is examined, it is about 60^{o} at the unity gain crossover frequency With no compensation the gain at the unity crossover frequency is about 40 db The classical way of stabilizing integrated circuit operational amplifiers is to go back to extremely low frequencies, on the order of 100 cycles, and put in a single pole, and use that roll off. If one goes to a low frequency and puts in a single pole then the magnitude characteristic is rolled off until the unity gain crossover frequency is reached after which it goes down 80 db per decade There is additional phase inserted but the new unity gain crossover frequency is low enough that the additional phase can be tolerated This is the first stabilization approach examined There are a number of ways to achieve a low frequency pole One of them would be to take one of the poles that is associated with the parallel RC and use a capacitor from the load device source to ground or by coupling a capacitor between the two output nodes of the first stage The value of the capacitance needed to give a pole close to the origin is of the order of 2000 pF That is obviously unrealizable on a chip Another approach is to take advantage of the Miller capacitance. For example, 20 pF is placed between the inputs and outputs of the second stage, and the stage has a gain of 15, then looking into the input node fifteen times the capacitance will appear. Effectively this puts 300 pF across each one of the input stage load devices. When this is done, at the unity gain crossover frequency there is 14 db of excess gain as opposed to 42 before. This single step gets rid of approximately 28 db of excess gain. However, it is still unstable. There are also other approaches that can be taken The nodes at the input and at the output are available An option is available on any of these stages to use some positive feedback for phase lead correction

The results of the dc analysis indicate a high degree of dc stability in terms of threshold voltages and power supply variations that resulted from the differential input On a nominal dc basis with 0 V at the inputs, the output is at - 048 V That is with 2 5 V threshold throughout and -27 V and +12 V supplies Now if the threshold voltage is changed to 3 V, this changes the output to - 032 V The output has changed by only 15 mV. A change of half a volt in the 12 V supply made the output go to 003 V For half a volt change in the positive supply, there is a change of 45 mV on the output or referred back to the input with a gain of a thousand, there is 04 mV referred to the input for a .5 V change in the 12 V supply As noted earlier, the output has a capability for at least a ± 6 V swing with a design requirement for a 5 V swing. For a 1 V change in the 27 V supply, there is a change at the output of 335 mV and, with a gain of 1000, that gives 0.3 mV referred to the input The dc design of the amplifier has resulted in an amplifier which is not sensitive to changes in the +12 V supply, or the -27 V supply and will tolerate threshold voltages easily within the range of 2 to 3 volts It has common mode feedback which is effective and is exemplified by the relatively small changes in output due to the changes in the supply

The operational amplifier and the comparator are identical stages The offset correction network consists of devices 184-186 and capacitor C4 The circuit uses the signals that are described on the logic diagram as T_o and $\overline{T_o}$ T_o arrives during the time that we want to reset the converter and adjust for offset correction At time T_o the amplifier is connected as a unity gain amplifier The non-inverting input to the amplifier is grounded by device 185 which is tied to T_o The circuit has the amplifier connected for unity gain with the non-inverting input grounded, and the output connected to capacitance C4 which is grounded The offset voltage can be represented as error voltage applied to the non-inverting input, and the voltage that results at the output across capacitance C4 will be the offset voltage times the closed loop gain Capacitor C4 will charge to this voltage. Now for a gain of 1000 capacitor C4 will effectively charge up to the offset error The actual voltage would be $A/(1 + A)$ times the offset voltage Therefore, capacitor C4 charges up to the error voltage during time T_o. At the end

of T_o the amplifier is disconnected as a unity gain amplifier The non-inverting input is disconnected from ground and connected to the side of C4 which was previously grounded, and the side of C4 which was connected to the amplifier output is now grounded. The capacitance is now connected to the non-inverting input, but it is connected so that it has a voltage which is equal and opposite to the offset voltage The voltage on C4 is bucking out the offset voltage and the offset has been corrected The timing problems associated with charging C4 are the same as the timing problems that were present in charging capacitors C1 and C2 to the reference voltage in the capacitance switching network. In fact, the timing problems are a little less severe because there is effectively 2 μsec to charge capacitance C4 There is only a microsecond to transfer charge between capacitors in the capacitance switching network The values used for the capacitances and the switches in the offset connection network are the same as were used in the capacitance switching network The offset correction networks for the amplifier and the comparator are identical

SECTION 2

TEST RESULTS AND DATA

1 0 INTRODUCTION

Since there are problems with certain sections of the present A/D design, it is necessary to analyze the subfunctions which are needed to make an A/D conversion and to determine the degree to which their design goals were achieved The A/D converter can be broken into the five subfunctions shown in Figure 8 There is also one other subfunction which is not shown and that is level shifting for interfacing the various subfunctions

2 0 SUBFUNCTIONS

2 1 11 Bit Time Counter

The eleven bit time counter must provide two signals, Sync Out and T_o Sync Out must go to a one at t'_{odd} of bit time 10 and return to zero at t'_{odd} of bit time 11 at which time T_o begins T_o must return to zero at the beginning of bit time 1 Photograph #1 shows that the circuit does work as designed The clocks were run at a low frequency so that the bit times would be clearly defined in the photograph Photograph #2, on the other hand, was taken with the clocks running at the required 440 kc This shows that the counter will function at the desired frequencies When viewing this photograph, consider that the signals are driving capacitative loads which are much greater than would be driven without the scope probes attached

The "1" and "0" levels of each signal were checked by manually stepping the counter and then measuring the signal with a D V M Data from the first lot revealed a problem with 0 level of T_o Table 1 shows that the zero level of T_o was 4-5 V below design level Since four inverters drive a single load device to produce T_o, it was hard to believe that there was an error in the design of the T_o circuit Further investigation proved that the fault lay with the +12 bus line The 4-5 V was being dropped across the P-tunnel in that line The P-tunnel problem will be discussed further in a later section As a temporary fix, a wire was bonded from the package (which is at +12 V) to the low voltage side of the P-tunnel The result can be seen in Photograph #3 The "0" level is just below +12 V Although varying the power supplies alters

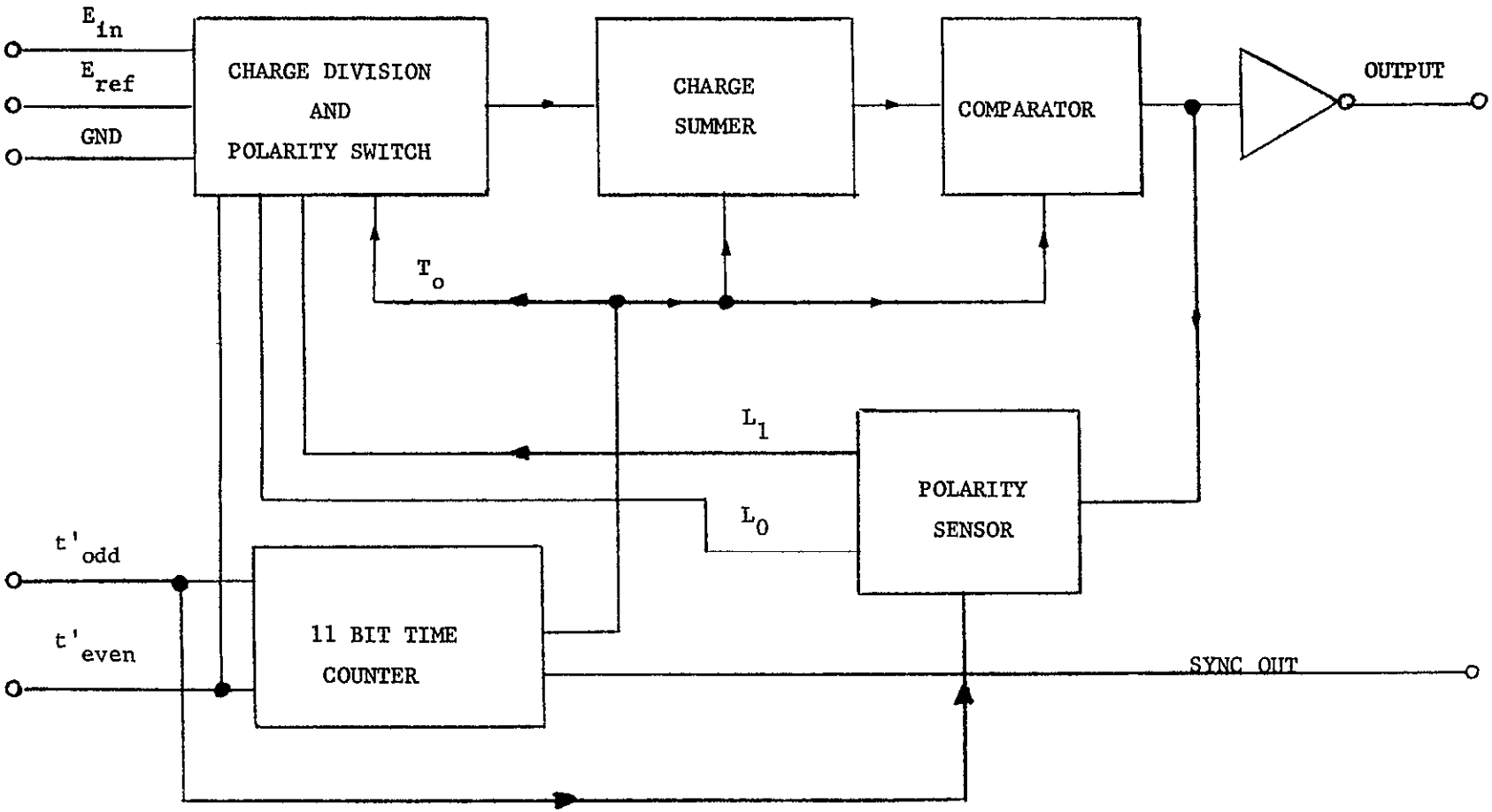


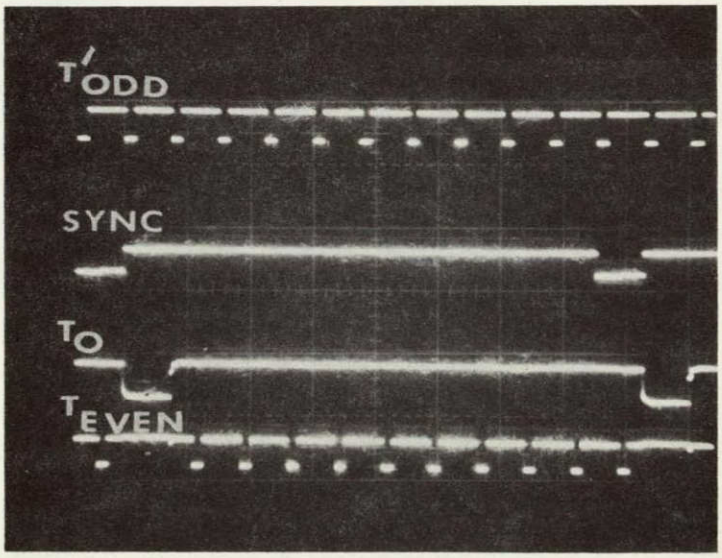
Figure 8 MOS A/D Converter Block Diagram

TABLE 1

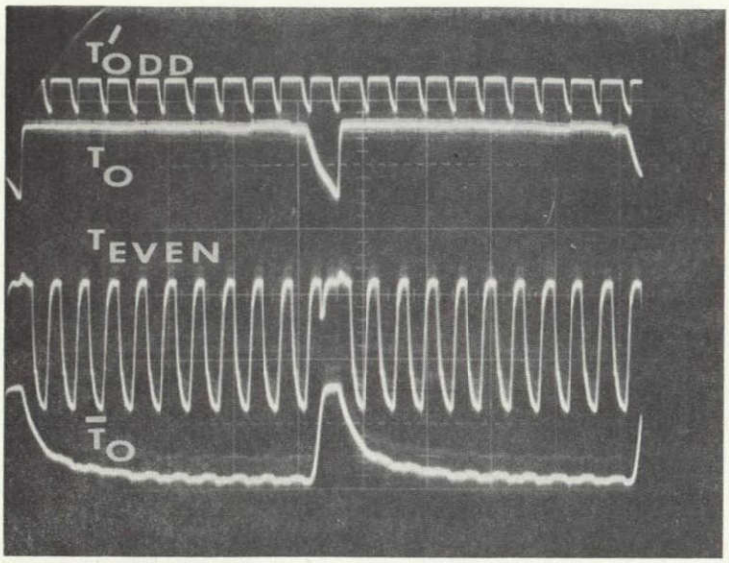
DC LOGIC LEVELS (VOLTS)*

Lot	Wafer	Unit	T_o		$\overline{T}_o$		T_{even}		Synch Out	
			1	0	1	0	1	0	1	0
70	83	16	-21.2	+5.74	-21.2	4.88	-19.03	.60	-20.3	-.13
70	83	26	-21.2	+5.93	-21.2	+6.68	-19.7	+.91	-20.4	-.12
70	83	28	-20.9	+4.87	-21.0	+4.87	-19.7	+.67	-20.0	-.14

* Power supplies at +12 and -27 V



Photograph #1
Clock Frequency - 62 cps



GND

GND

GND

50 V/Div

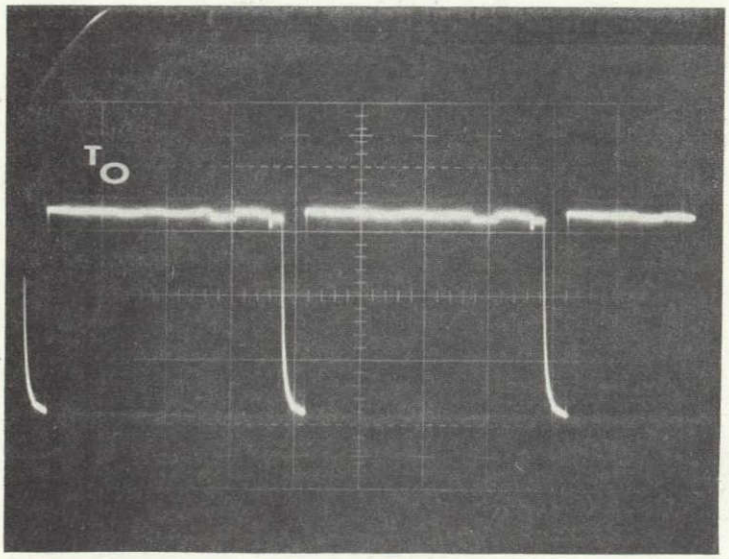
20 V/Div

5 V/Div

20 V/Div

Photograph #2

Clock Frequency = 440 kc



GND

20 V/Div

Photograph #3

Clock Frequency = 55 kc

the one and zero levels, it seems to have little effect on the counter's ability to function. The circuit will function at +17 V and -23 V or at +9 and -30 as well as the standard +12 and -27 V. (Threshold voltage variation seems to have little effect also.) Photograph #1 shows the output of a unit which came from a lot (70) that had typical thresholds of 1.5 V to 2.0 V whereas Photograph #2 shows the output of a unit which comes from a lot (124) that had typical thresholds of 3.0 to 3.7 V. It can be said, then, that the 11 bit time counter design is a good one and will function properly under all worst case conditions.

2.2 Charge Division and Polarity Switch

The charge division network consists of capacitors C_1 and C_2 and devices 137, 138, 140, 141, 146, and 147. The polarity switch consists of devices 142 through 145. The matching requirements for capacitors C_1 and C_2 (.1%) are given on 1-22. No adequate measurement techniques have been found to determine whether this degree of matching has been met. Instruments capable of measuring .01 pf are incapable of nulling the effects of the series resistances of the input devices, the capacitances of the leads, and the noise due to various sources (such as p-n junction noise). Ultimately, the decision as to whether the capacitors are matched to within 0.1% will have to be determined by the accuracy of the converter.

One of the major concerns when the A/D converter was designed was whether five capacitors, each occupying 100 $mils^2$, could be made on a single chip without having a large yield loss due to pinholes in the oxide between the capacitor plates. All five capacitors were tested on chips from several wafers. The worst pass rate from any wafer was 70%. The criteria for rejection were that the chip had to have no capacitors which were shorted and all capacitors had to be a nominal 20 pf.

The best method to determine whether the switching devices associated with this subfunction are working properly is to observe the output of the amplifier. During the first bit time, the input voltage should appear at the output of the amplifier. During the next bit times, the reference voltage should cause the amplifier to step in either the positive or the negative direction (depending on whether there has been an L_o or an L_1 signal). An L_o signal should cause the amplifier output to go negative and an L_1 signal should cause it to go positive. Also, if the reference

voltage is being divided properly, each step after bit 2 should be one-half the size of the previous step.

The L_o, L_1 inputs to the polarity switch shown in Photograph #4 were generated by external circuitry. The amplifier output shows that the charge division and polarity switches do function as described above. Because there are inaccuracies due to leakage currents at the input of the charge summing amplifier, effects on the accuracy of the converter due to the charge division and polarity switch section have not been evaluated. However, the test results show that this section of the A/D converter does function as designed and will not be a source for appreciable yield loss.

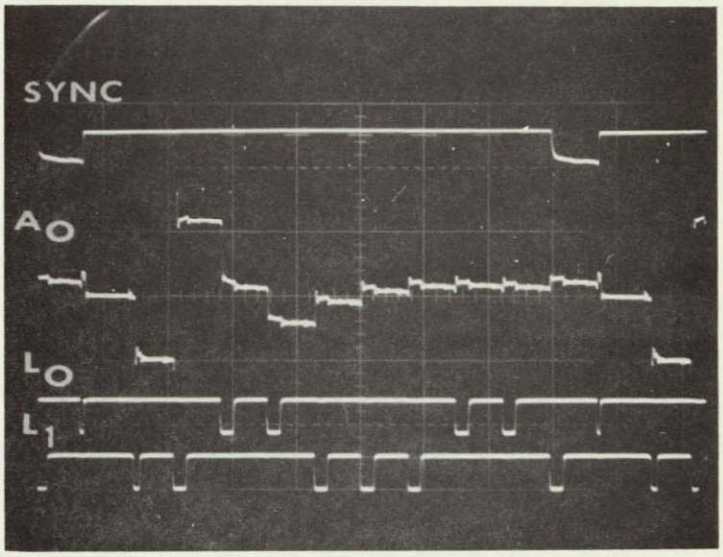
2.3 Charge Summer and Comparator

Although the Charge Summer and Comparator perform different system functions, they use identical amplifiers to perform each function. Therefore, test results from either amplifier can be used to evaluate both. The amplifier parameters most critical to the system are gain and phase as a function of frequency, input offset, input offset drift, and dynamic range.

The maximum low frequency gain required in the system is 60 db. Tests show that there is little difficulty achieving this gain. Table 2 shows the gain at 100 cps of units from two different wafer lots. The devices from lot 70 probably have gains higher than that shown in Table . The measurements shown here were taken before the +12V bus line p-tunnel problem was discovered. Therefore, the amplifiers had to work from power supplies that were about 4 volts lower than design levels. The open loop frequency response of the amplifiers has been measured. The results of these tests will be given in a later section.

TABLE 2

Wafer Lot	Unit No.	Gain at 100 cps db	Typical Threshold for Wafer Lot
70	19	60	1.5 → 2.0
70	28	60	1.5 2.0
124	2405	62	3.0 3.7
124	2406	65	3.0 3.7



GND

20 V/Div

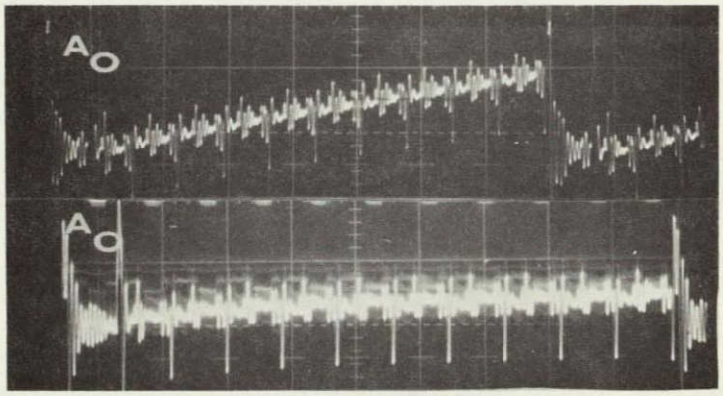
2 V/Div

50 V/Div

50 V/Div

Photograph 4

Clock Frequency = 50 kc



GND

GND

200 mV/div

200 mV/Div

Photograph 5

Clock Frequency = 42.5 kc

Typically, input offset voltages have been very low. Table 3 shows the offset voltages from several devices from wafer lot 124. All of them have substantially less offset voltage than the 500 mV maximum allowed.

TABLE 3

AMPLIFIER INPUT OFFSET

Unit No.	Input Offset (mV)
2405	+17
2406	+3
2503	+33
2702	+9

Offset drift, however, is a major problem. Photograph #5 is a composite of two photographs. The top trace is the output of the amplifier with the A/D converter running with both the reference and the input voltages grounded. Under these conditions, the amplifier output should go to ground potential and remain there. Photograph #5 shows that this is not the case. There is constant leakage current which, over the period of a conversion, causes the output to drift about 250 mV. (In this photograph the clock frequency was 42.5 kc so that the conversion period is 235 μS.) It was assumed that the offset drift was being caused by p-n junction leakage currents depositing charge on the input capacitors (mainly C_4). To prove that this was the case, the device was sprayed with freon in order to lower junction temperature, and thereby reduce junction leakage currents. The results of this experiment can be seen in the bottom trace of Photograph #5. The offset drift has been cut in half. (The sweep rate of the oscilloscope has been changed in the bottom half of Photograph #5, not the clock frequency.) The main source for leakage is the p-tub that forms one side of the diffused capacitors. The equivalent circuit of the charge summer including the diodes which are the p-tubs diffused into the n substrate material is shown in Figure 9. The effects of these leakage currents could be eliminated by placing the p-tub on the opposite side of the capacitor so that the equivalent circuit for the charge summer would look like Figure 10.

In this configuration, the leakage currents would be shunted to ground rather than through the capacitors.

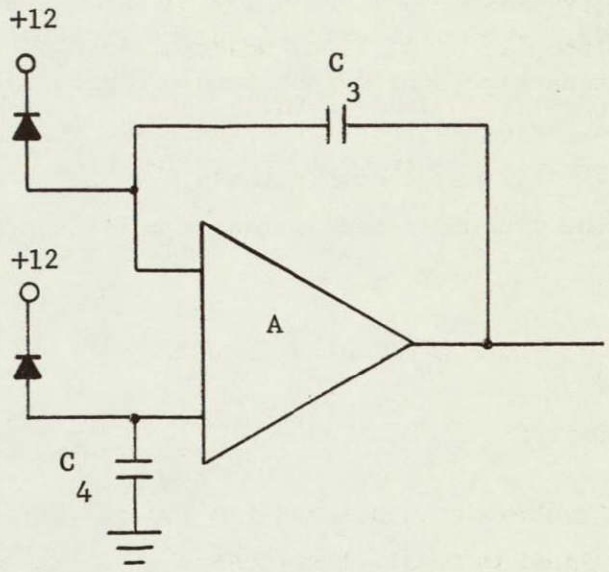


Figure 9. Equivalent Circuit for Charge Summer As Designed

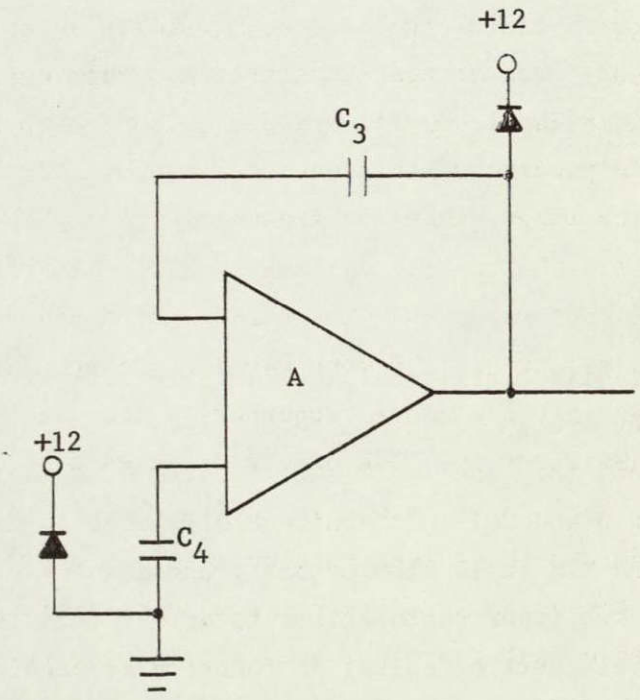


Figure 10. Equivalent Circuit for Suggested Change in Charge Summer Design

Because the output stage of the amplifier is a source follower, the dynamic range depends, to a large extent, on the threshold voltage of the transistors. Unfortunately, none of the lots produced after the p-tunnel problem was resolved, have had transistor threshold voltages in the nominal range (2-3V). All have been in the 3.0 to 3.7 V range. Some typical values for the dynamic range of these amplifiers are shown in Table 4.

TABLE 4

AMPLIFIER DYNAMIC RANGE

Wafer Lot	Unit No.	Positive Dynamic Range	Negative Dynamic Range
124	2405	+5.8V	-12.5V
124	2406	+5.5V	-12.0V
124	2503	6.0V	-11.5
124	2702	6.2	-12.0

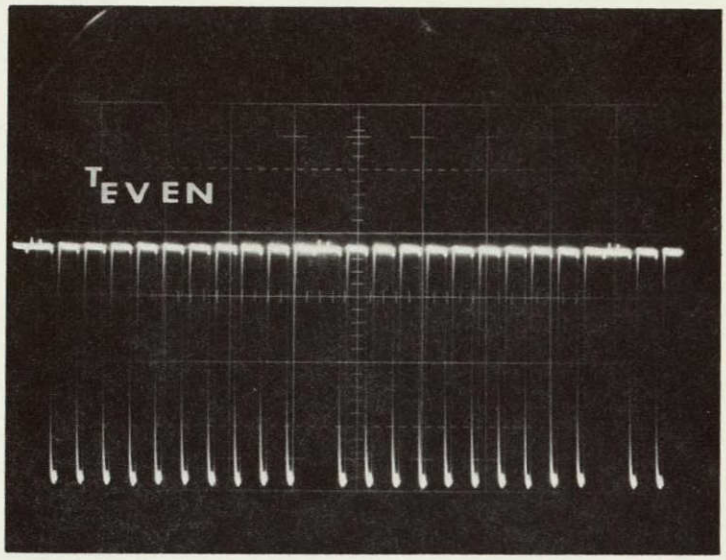
Even with the higher threshold, the amplifiers have the required $\pm$5V dynamic range.

2.4 Polarity Sensor

A logic error has been found in the polarity sensor subfunction which consists of gates Q, R, S, T and flip-flop F. Therefore, no meaningful test results on this section of the converter can be given here. An explanation of that error and the required correction will be given in the next section.

2.5 Level Shifting

There are four different logic level shifting circuits within the A/D converter. They are the input buffers (Gates W and X), the output buffers (Gates AA and BB), the level shift (Gates O, P, and U), and the level change (Gates Q and CC). It would be difficult to measure the output from gates W and X. It is also probably unnecessary since the net effect is that the two other subfunctions it drives (the 11 bit time counter and the level shift circuits) do function as required. (Photograph #6. If gate W is working properly the output from gate O should swing between +4V and -14.5V. Photograph 6 shows that this is indeed the case. Note that the inhibit gate, M, also has to be working properly since every 11th bit of t_{even} is being inhibited.

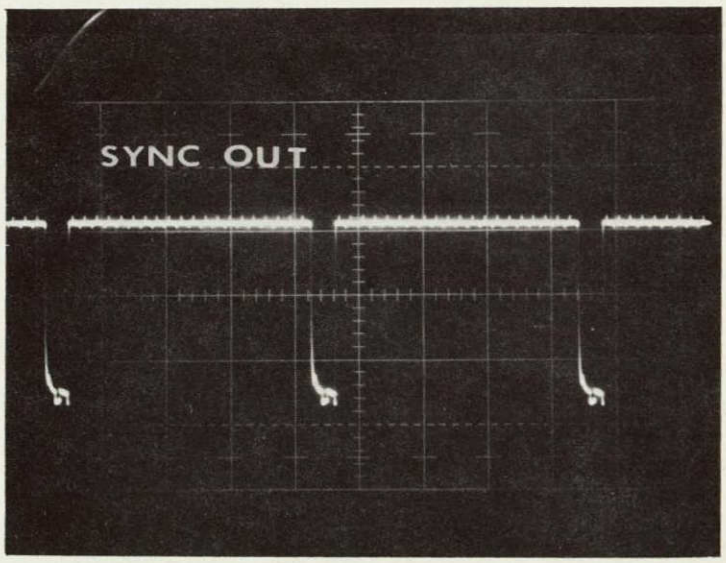


GND

5 V/Div

Photograph 6

Clock Frequency = 55 kc



GNI

Photograph 7

Clock Frequency = 55 kc

Photograph #7 shows the synch out signal of device #3517. It shows that the output buffers do work as designed. The negative level attained is about one volt less than was expected. This can be attributed to the fact that this unit had threshold voltages of about 3.7 V.

Preliminary investigations into the level change circuit have shown that there appears to be a problem with its ability to discriminate between 0 V and -5 V. Further investigation into the level change circuit should be undertaken before the A/D converter is redesigned.

3.0 OVERALL PERFORMANCE OF THE A/D CONVERTER

In order to prove the feasibility of this method of A/D conversion, to verify the functional performance of the A/D, and to obtain test data, circuitry external to the converter was used to overcome the logic error in the polarity sensor circuit and the leakage to the input of the amplifier. The logic error was corrected by using the comparator, T_o, and $\overline{T}_o$ outputs from the A/D converter as inputs to the circuit shown in Figure 11.

The L_o,L_1 outputs from the external circuitry shown were then fed back into the A/D Converter. The external circuitry had sufficient drive to overpower any signals coming from the internal polarity sensor circuit. Errors in the accuracy of the conversion due to amplifier input offset drift were minimized by supplying a constant current of -18 nA to the non-inverting input of the charge summing amplifier.

After these two corrections were made, the A/D converter was run at 5 k conversions/sec and randomly selected voltages were applied at the input.

The desired converter output word and the external L_1 signal are exactly the same. Therefore, the L_1 signal can be used as the output word. Because the external polarity sensor circuit of Figure 11 and the level change circuit CC in the A/D converter could not be made to interpret the output of the comparator in the same manner, the externally generated L_1 signal had to be used as the output word. The results of this test are shown in Table 5 and the data is plotted in Figure 12. A typical conversion is shown in Photograph #8. Between -2 V and +5 V the converter is accurate to within 280 mV. Between +1 V and +4.5 V the converter is accurate to within 70 mV.

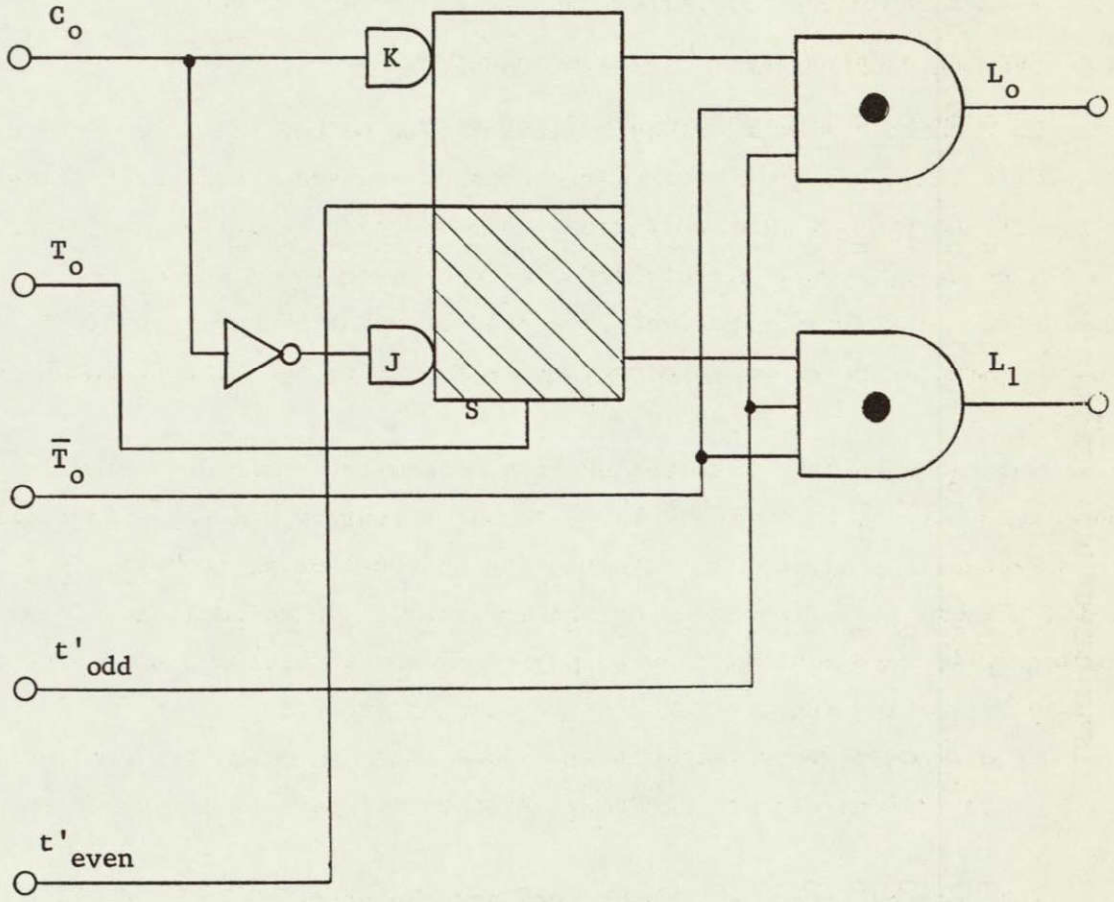


Figure 11. External Polarity Sensor Circuit

TABLE 5

INPUT-OUTPUT DATA FOR UNIT 3517

Input	Bit 1 (Sign)	2 (2.56)	3 (1.28)	4 (.64)	5 (.32)	6 (.16)	7 (.08)	8 (.04)	9 (.02)	10 (.01)	=	Output Decimal Equivalent
0.0V	1	0	= 0	0	0	1	1	1	0	0	=	+ .28
+0.35	1	0	0	0	1	1	0	0	0	1	=	+ .49
+1.00	1	0	0	1	1	0	0	0	1	1	=	+ .99
+1.28	1	0	0	1	1	1	1	1	1	1	=	+1.27
+2.00	1	0	1	1	0	0	0	1	0	0	=	+1.46
+2.56	1	0	1	1	1	1	1	1	1	1	=	+2.55
+3.98	1	1	1	0	0	0	1	1	0	0	=	+3.96
+4.47	1	1	1	0	1	1	1	0	0	0	=	+4.40
+5.00	1	1	1	1	1	1	1	1	1	1	=	+5.12
- .50	0	1	1	1	0	0	1	0	0	1	=	- .54
-1.50	0	1	0	1	1	0	0	1	1	0	=	-1.53
-2.00	0	1	0	0	1	1	1	1	1	1	=	-1.92
-3.00	0	0	1	1	1	1	0	0	1	0	=	-2.69
-4.00	0	0	1	0	1	1	0	0	1	0	+	-3.33
-5.00	0	0	1	0	0	1	1	0	0	0	+	-3.59

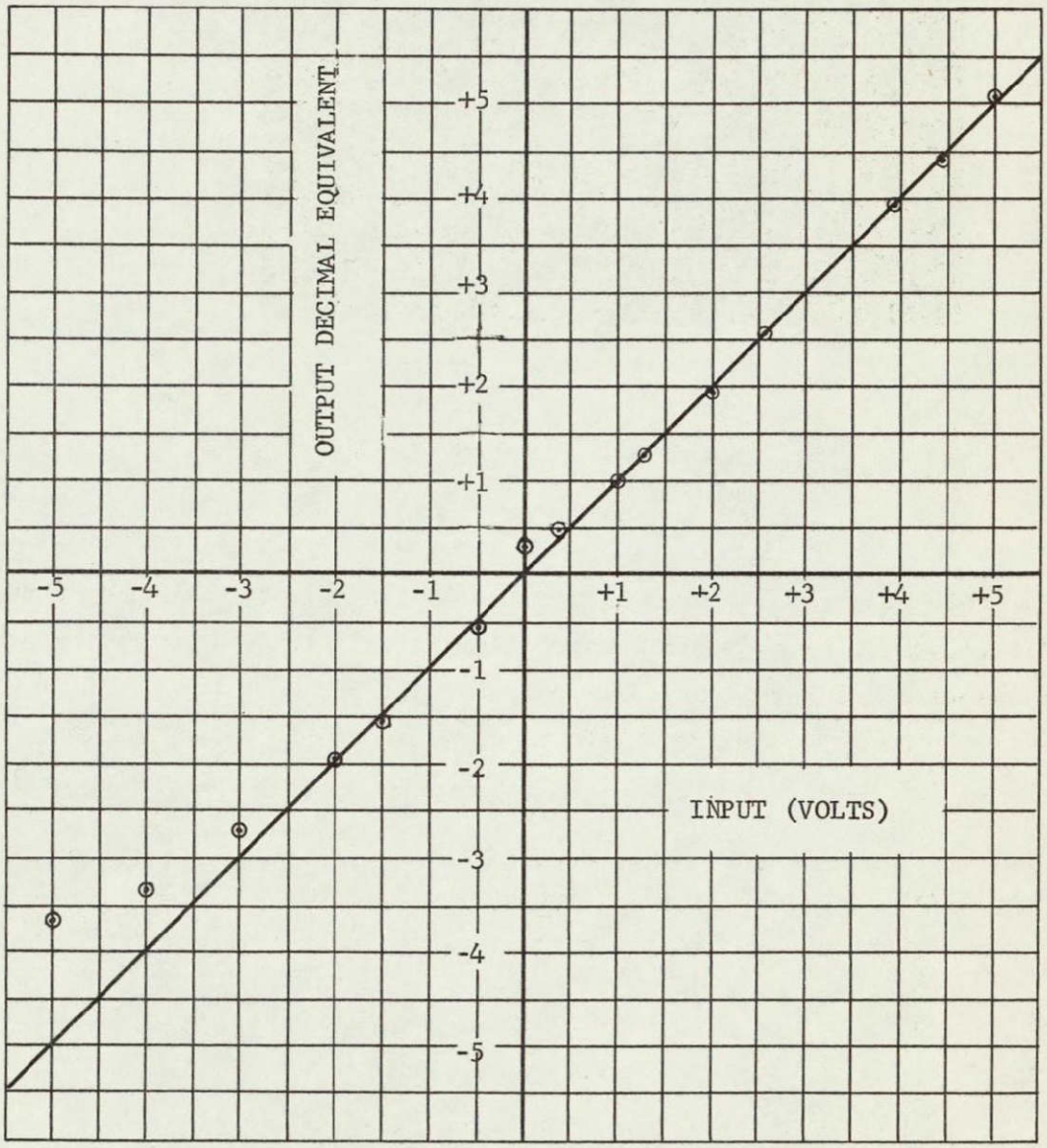
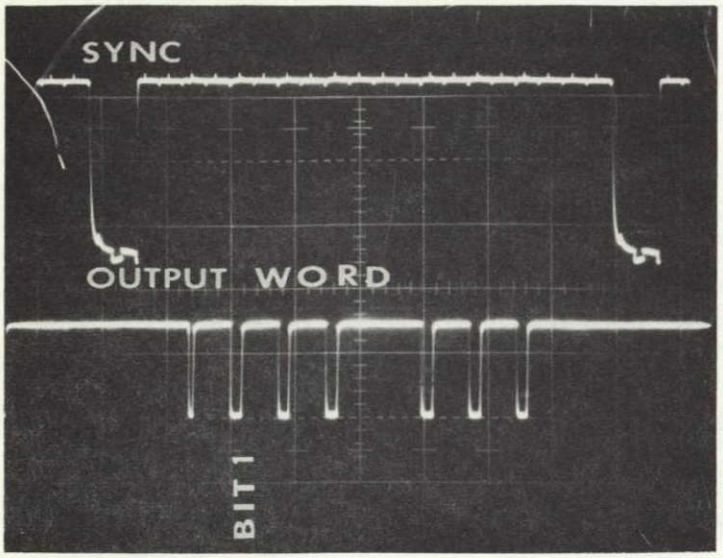


Figure 12. Plot of Data Shown in Table 5

GND



5 V/Div

20 V/Div

Photograph 8
Clock Frequency = 55 kc

One other aspect to consider in the over-all performance of the A/D converter is the total power dissipation. Table 6 shows the power dissipation of three devices from wafer lot 70.

TABLE 6

TOTAL POWER DISSIPATION

Unit No.	Current From +12 V Supply (mA)	Current From -27 V Supply (mA)	Total Power Dissipation (mW)
26	14.2	13.5	535
16	17.0	18.0	727
3	9.0	10.0	440

Obviously, this is much higher than was originally intended. It is also a source for conversion inaccuracy since p-n junction leakages are a function of temperature. A redesign of the A/D converter should include all means possible to lower the power dissipation.

We believe that the test results presented here prove that this method is a valid approach to an all monolithic A/D converter and that, with minor design changes, the goals set out in the introduce to this report can be attained.

SECTION 3

IDENTIFICATION OF PROBLEM AREAS AND PROPOSED SOLUTIONS

1.0 PROBLEM AREAS

The problem areas associated with the initial design and layout of the A/D Converter are summarized in Table 7.

The most serious problem is a logic error. This logic error prevents the converter from operating properly. The problem is centered in the circuit used to set flip-flop F so that signals L_1, or L_o are obtained depending upon the comparator output. Refer to the logic diagram, page 3.

The desired functional relations are:

1. If during t'_{even}, the comparator output is a zero, flip-flop F is set.
2. If during t'_{even}, the comparator output is a one, flip-flop F is reset.
3. During T_o flip-flop F is to be set.
4. During $\overline{t_{even}}$ flip-flop F is to remain in the state in which it was put during t'_{even}.

The present circuit fails the 4th functional relation. During $\overline{t_{even}}$, t_{even} is a "o" giving a "1" out of Q. This results in a "o" out of T, a "o" out of R, and a "1" out of S so that flip-flop F is set during t_{even} and does not remain in the reset mode if it was reset during t_{even}.

The proposed correction is shown below.

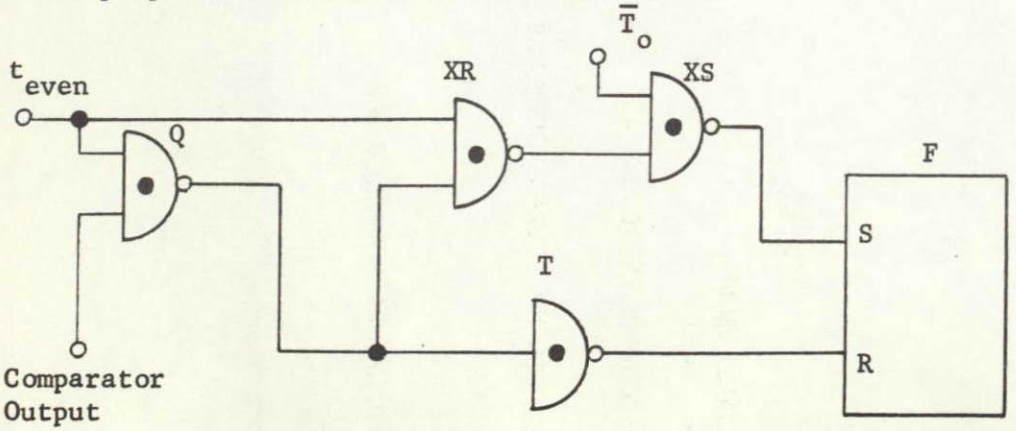


TABLE 7

A/D CONVERTER

AD/01

PROBLEM SUMMARY

PROBLEM	EFFECT	SOLUTION
LOGIC ERROR (L_1 & L_0)	AMPLIFIER ALWAYS DRIVEN IN SAME DIRECTION	REDESIGN GATES R & S
P-TUNNEL IN GROUND AND +12 BUSS	EXCESSIVE VOLTAGE DROPS IN P-TUNNEL	RELAYOUT TO ELIMINATE P-TUNNEL
EXCESSIVE VOLTAGE SUPPLIES	EXCESSIVE POWER CONSUMPTION, ELEVATED CHIP TEMPERATURE, EXCESSIVE LEAKAGE CURRENT, FIELD INVERSION	REDESIGN TO OPERATE WITH LOWER SUPPLY LEVELS
AMPLIFIER COMPENSATION	OVERCOMPENSATION RESULTS IN A LOSS OF CONVERSION SPEED	OPTIMIZE COMPENSATION

Gates XR and XS replace the present R and S gates.

For relation 1, there is a "1" out of Q, a "o" out of T, a "o" out of XR and a "1" out of XS and flip-flop F is set.

For relation 2, there is a "o" out of Q, a "1" out of T, a "1" out of XR, and a "o" out of XS and flip-flop F is reset.

For relation 3, $\overline{T_o}$ is a "o", t_{even} is a "o" and there is a "1" out of Q, a "o" out of T, a "1" out of XR, a "1" out of XS and flip-flop F is set.

For relation 4, t_{even} is a "o" resulting in a "1" out of both Q and XR, since $\overline{T_o}$ is a "1" there will be a "o" out of both XS and T and the flip-flop remains in its present state.

The problem associated with the p-tunnel in the ground and +12 volt buss can be seen by refering to the composite mask layout, page 58. From the bonding pad the +12 buss enters a p-tunnel before it is distributed to the rest of the chip. This p-tunnel has a higher resistance than was originally anticipated. Also, the circuit draws more current. These two factors lead to a voltage drop across the p-tunnel of approximately 5 volts. The problem associated with the ground buss is similar in nature. The resistance assciated with p-tunnel in the ground buss provides a common point for voltages to be developed. Both of these problems can easily be corrected by a minor redesign of the mask layout which would eliminate the p-tunnels. As a temporary measure, a laser was used to cut the emulsion on working masks, to provide pads that were bonded to +12 or ground respectively. This eliminated those problems and resulted in the proper voltages being applied to the circuits in the converter.

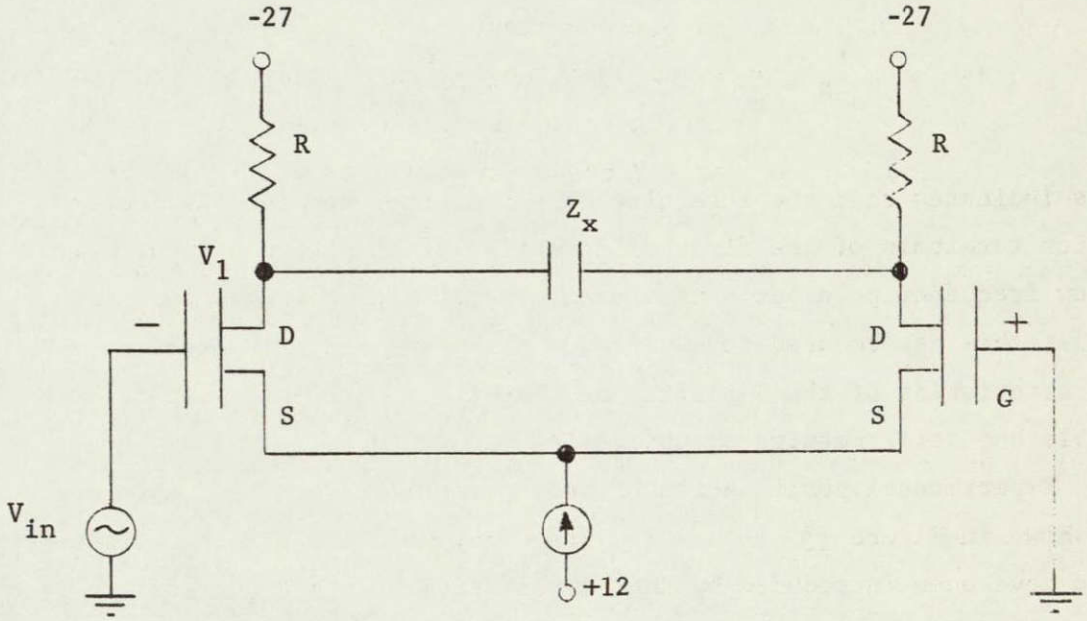
The original design called for -27 V and +12 V supplies. These voltages result in a 39 volt potential between metal interconnect lines on the top surface of the chip and the substrate. This voltage can result in field inversion. Field inversion results in the formation of spurious p-regions which can act to connect together portions of the circuit in an unwanted way. This results in a circuit malfunction. The major effect of field inversion is a loss of yield. The voltage necessary for field inversion to occur is typically 35 to 50 volts.

An additional reason for consideration of the use of lower supply voltages is the power dissipation. The present power dissipation on

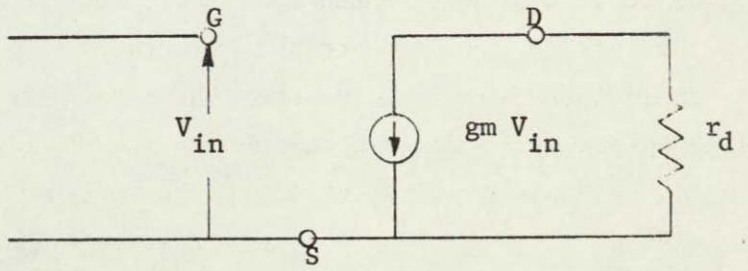
the chip is excessive and results in the chip operating at elevated temperature. This results in excessive leakage currents which affect the accuracy of the converter. A reduction of the power supply levels to a 30 volt overall level (+12, -18 or ±15 V) would avoid the field inversion problem; would result in a 40% reduction in power dissipation; and would greatly reduce the leakage currents.

2. COMPENSATION OF THE MOS OPERATIONAL AMPLIFIER

The first stage of the amplifier has been modeled as follows:



The MOS input transistors have an equivalent circuit:



The current source is replaced by a resistance R_c and R represents the dynamic resistance of the MOS load transistors.

The transfer function V_1/V_{in} can be shown to be:

$$\frac{V_1}{V_{in}} = - \frac{gm/2}{\left[g + \left(\frac{\alpha+2}{\alpha}\right) G \right]} \frac{S + \frac{g + \left(\frac{1+\alpha}{\alpha}\right) G}{C}}{S + \frac{g+G}{2C}}$$

where

$$g = \frac{1}{r_d} \qquad G = \frac{1}{R} \qquad \alpha = \frac{G_c}{g + gm} \qquad G_c = \frac{1}{R_c}$$

This indicates that the insertion of a capacitor between the compensation terminals of the first differential stage not only results in a low frequency pole but a zero occurring at higher frequency. As a result this can be used to advantage in shaping the high frequency characteristics of the amplifier so that it is unity-gain closed-loop stable but still retains a substantial bandwidth.

Experimental verification of this performance has been obtained. As shown in Figure 13, both a low frequency pole and a higher frequency zero have been introduced by the compensation. With the transfer characteristic shown, the amplifier would have a bandwidth in a unity-gain closed-loop configuration of well in excess of 1 MHz. The requirement for bandwidth is critical so that the necessary speed to operate at conversion rates of 40 kHz can be obtained.

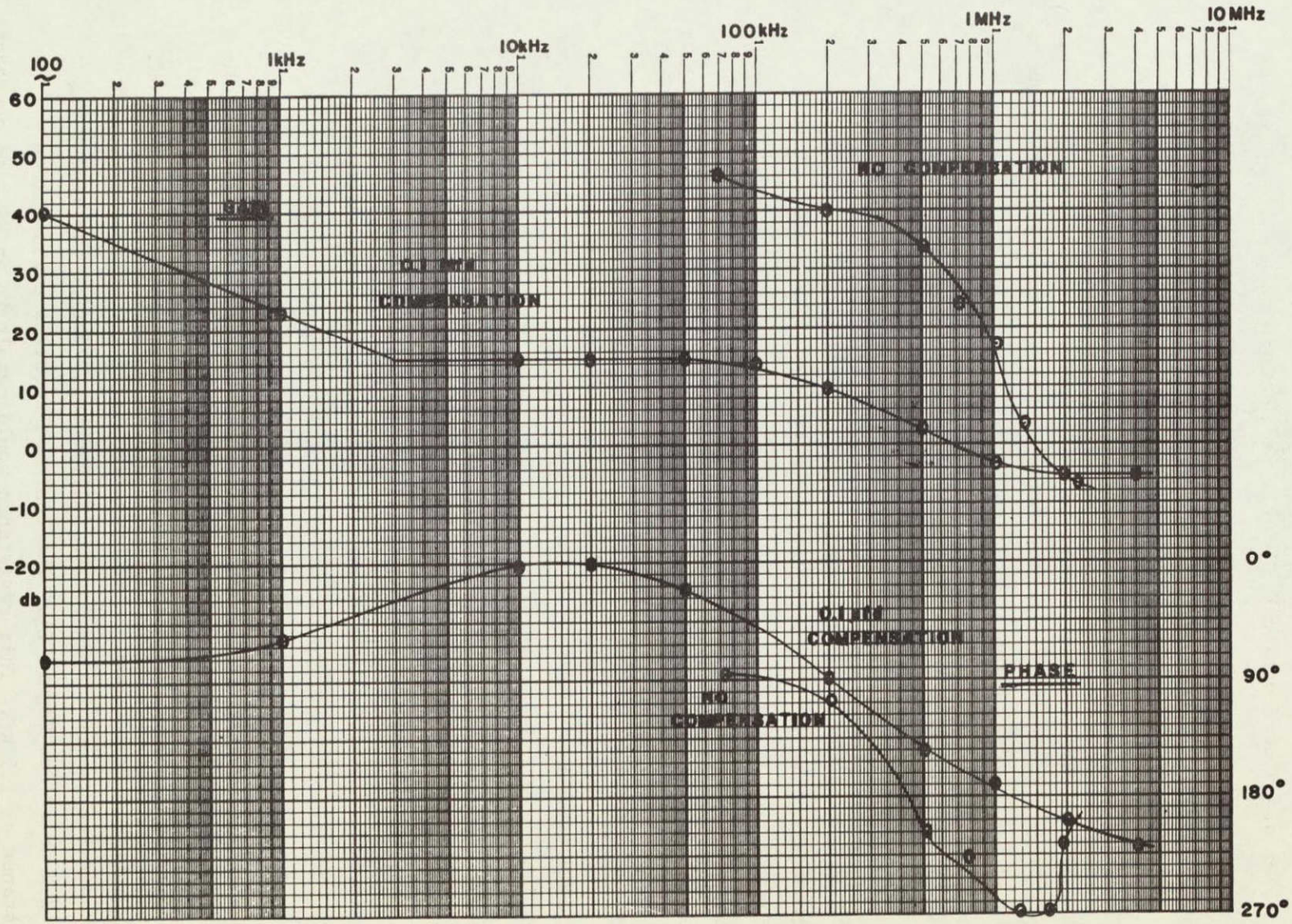


Figure 13. Amplifier Frequency Response

SECTION 4

SYSTEM DESCRIPTION

1.0 GENERAL

This contract calls for the purchase, testi ng and delivery of a two-phase clock generator, serial-to-parallel converter, and 16-channel multiplexer, all of which would be compatible with the analog-to-digital converter to be developed. A discussion of the entire system then should begin with a review of the input-output characteristics of the A/D converter.

The converter requires a non-overlapping two phase clock capable of running at 440 kc with a pulse width of about 1 μsec. The minimum one level is -10 V and the maximum 0 level is -2.0 V. The A/D converter will put out a 10 bit word and a synchronization signal, each of which has a minimum 1 level of -15 V and a maximum 0 of 0.0 V when driving a capacitive load. The system timing diagram (Figure 14) shows that the synch out signal lasts from the beginning of t'_{odd} of bit time 10 to the beginning of t'_{odd} of bit time 11. At 440 kc this corresponds to a pulse width of about 2.2 μsec.

2.0 MULTIPLEXER

The A/D synch signal was originally specified and designed to interface with the multiplexer (Philco-Ford PL4S16C). When used in the sequential mode, as is shown in Figure 14, the multiplexer requires a minimum pulse width of 2 μsec at a maximum clock frequency of 100 kc. The minimum 1 level in is -9 V and the maximum 0 level is -3 V. The clock rate into the multiplexer from the A/D converter is the same as the conversion rate; 40 kc. The A/D synch signal is more than adequate in both respects. Other multiplexer parameters which are important to consider within the system are: channel on resistance of the switches and switch input impedance to ground in the On as well as the Off condition. The channel on resistance has to be sufficiently low so that C_2 of the A/D converter (about 20 pF) can be fully charged during the time T_o is a 1, 2.2 μsec (See Figure 2). The contract requires a channel on resistance of 1.5 kΩ. This resistance would result in an RC time constant

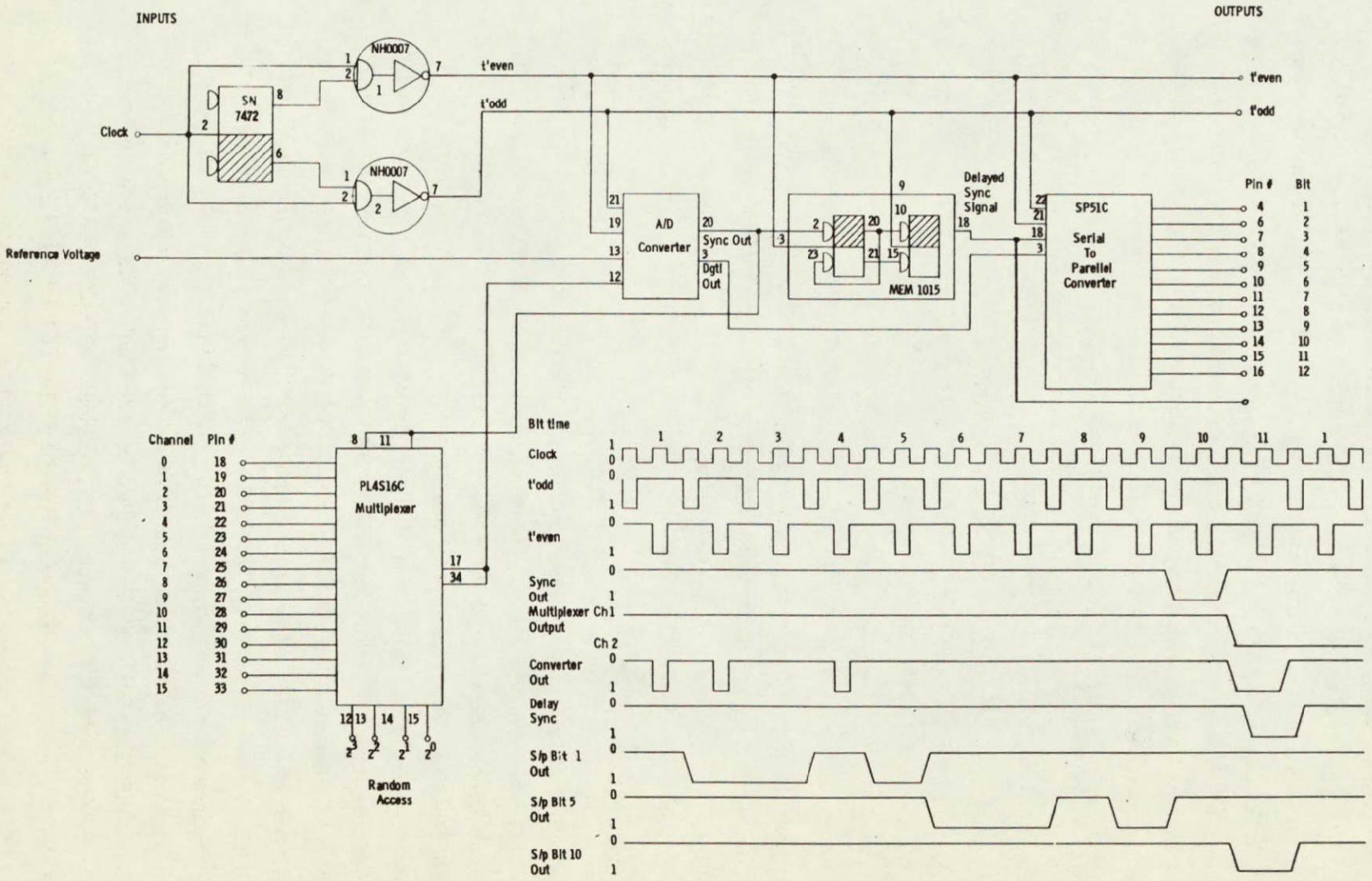


Figure 14. System Schematic and Timing Diagram

of 30 μsec which means the capacitor has more than 700 time constants to charge. (Test results show that the on resistance is easily below the 1.5 kΩ requirement.) The switch input impedance to ground was found to be far greater than 10 mΩ in the Off as well as On condition. Although the units were tested in the sequential mode only, they may be used in the random access mode. The inputs for the random access mode are shown on Figure 14 .

3.0 SERIAL TO PARALLEL CONVERTER AND DELAY CIRCUIT

The serial to parallel converter in this system is the A.M.I. SP51C. It is 12 bits long, resettable, and allows for permanent data storage. It uses the same clocks as the A/D converter but needs a 1 level of -24 V minimum and a 0 level of -2 maximum. Although it is not stated on the specification sheet, there is also a requirement that the $\emptyset_2$ clock be at least 1 μsec wide. The system diagram (Figure 14) shows the $\emptyset_1$ clock input is connected to t'_{even}. This is because the A/D data is clocked out on t'_{even} of each bit time. The data input requirements are:

1. That it be good through the end of the $\emptyset_1$ clock (t'_{even})
2. That the 1 level be -9.0 V min, and
3. That the 0 level be -3.5 V max.

There is sufficient delay through the A/D converter to comply with condition (1), and it has already been shown that conditions (2) and (3) are met. Since the data is clocked out during t'_{even}, the 10th bit of information will be clocked out during t'_{even} of the 10th bit time and will not become available from the serial to parallel converter until t'_{odd} of bit time 11. The data will be available until t'_{odd} of bit time one of the next conversion. The most significant bit will be at pin 14, and the least significant bit at pin 4. A synchronization signal is needed to indicate when the information is available.

A suggested method for obtaining this signal is shown in the system diagram. All that is required is one General Instruments MEM 1015 Dual MOS Flip-Flop. The output of the device is shown in the timing diagram as "Delay Sync". This signal may also be used to reset all the S/P converter outputs to zero at the end of each conversion cycle. The system schematic shows the devices connected so that

resetting will occur.

4.0 TWO PHASE CLOCK GENERATOR

The A/D converter, serial to parallel converter, and the MEM1015 are all driven from the same two phase clock generator. The generator converts a single phase clock pulse working at TTL levels into two phases working at MOS levels. It consists of three devices, one SN7472 flip-flop and two NH0007 MOS clock drivers. The clock drivers have two inputs which are anded, and then level shifted. When a TTL one is present at each input, an MOS one occurs at the output. When connected as shown in Figure 14, the SN7472 toggles and alternately applies a 1 to each clock driver input, resulting in the outputs t'_{even} and t'_{odd} shown in the system timing diagram (Figure 14). This method is used because of its great versatility. The generator can be run at any speed from dc to about 2 Mhz and with any pulse width which does not cause over lapping. The pulse width and pulse spacing of the two phases is determined solely by the input clock.

The system requirements of the two phase clock generator are determined by the A/D converter and the serial to parallel converter. For the A/D converter to run at its maximum rate, 40 K-conversion/sec, the two phase clock would have to run at 440 kc. As was stated earlier, the $\emptyset_2$ clock of the serial to parallel converter must be at least 1 μsec wide. Therefore, the clock input to the two phase generator must be 880 kc/sec and the pulse width must be 1 μsec. Test results imply that these requirements may be difficult to meet. Specifically, the off time of the clock driver appears to be too high. It should be noted, however, that the device, when tested, was driving a much higher load than would normally be seen in the system. Also, there are several speed-up techniques which could have been used to eliminate the problem. These techniques may be found in National Semiconductor's applications notes An-18. The speed-up techniques were not employed because, at present, the clock rise and fall times are adequate to drive the A/D converter. The two phase clock 0 level requirement is the same for all the devices in the system, -2 V max. The maximum 1 level is also the same, -30 V. The minimum clock level is determined by the serial to parallel converter. It requires a minimum 1 level of -24 V. Test

results show that the limits are easily attainable.

5.0 SUMMARY OF SYSTEM REQUIREMENTS AND TESTING

Pin connections for each of the devices within the system are given in Appendix 1. Data sheets for the devices other than the A/D converter and the SN7472 are in Appendix 2. A review of Appendix 1 shows that six power supplies and one clock are required to run the entire system. The necessary power supplies are: -27.0 $\pm$1.0 V, -23.0 $\pm$1.0 V, +5.0 $\pm$1.0 V, +12.0 $\pm$1.0 V, -12.5 $\pm$0.5 V, and -5.12 V $\pm$0.1%. The clock must be capable of producing a +5 V pulse 1 μsec wide at 880 kc/sec.

All the devices supplied under this contract have been subjected to the environmental conditioning required by the contract. They have been burned in at 125°C for 100 hours under what was considered to be the worst case for each type device. For instance, a negative dc voltage was applied to the $\emptyset_1$ and $\emptyset_2$ clock inputs of the serial to parallel converter while the multiplexers were connected in the sequential mode and made to step through each channel. Electrical tests were performed with system compatibility being the prime consideration. Detailed test procedures are given in Appendix 3. Test results and data are given in Appendix 4.

SECTION 5

PHYSICAL LAYOUT TO PROCESS PARAMETERS

Figure 15 is a print of the A/D converter composite artwork. The lettering on the artwork corresponds to that shown on the logic diagram and circuit schematic. The actual chip size is 115 mils x 115 mils. There is a total of 225 MOS transistors and 5 MOS capacitors on the chip. Twenty-three bonding pads are available for test and evaluation whereas only thirteen are required for normal operation.

The MOS technology used in the fabrication of the converter is shallow diffusion (0.05 mil), low threshold (2.0-3.0 V), p-channel enhancement mode.

Photograph #9 shows an A/D converter mounted and bonded in its 3/8" diameter 22 lead flat-pack.

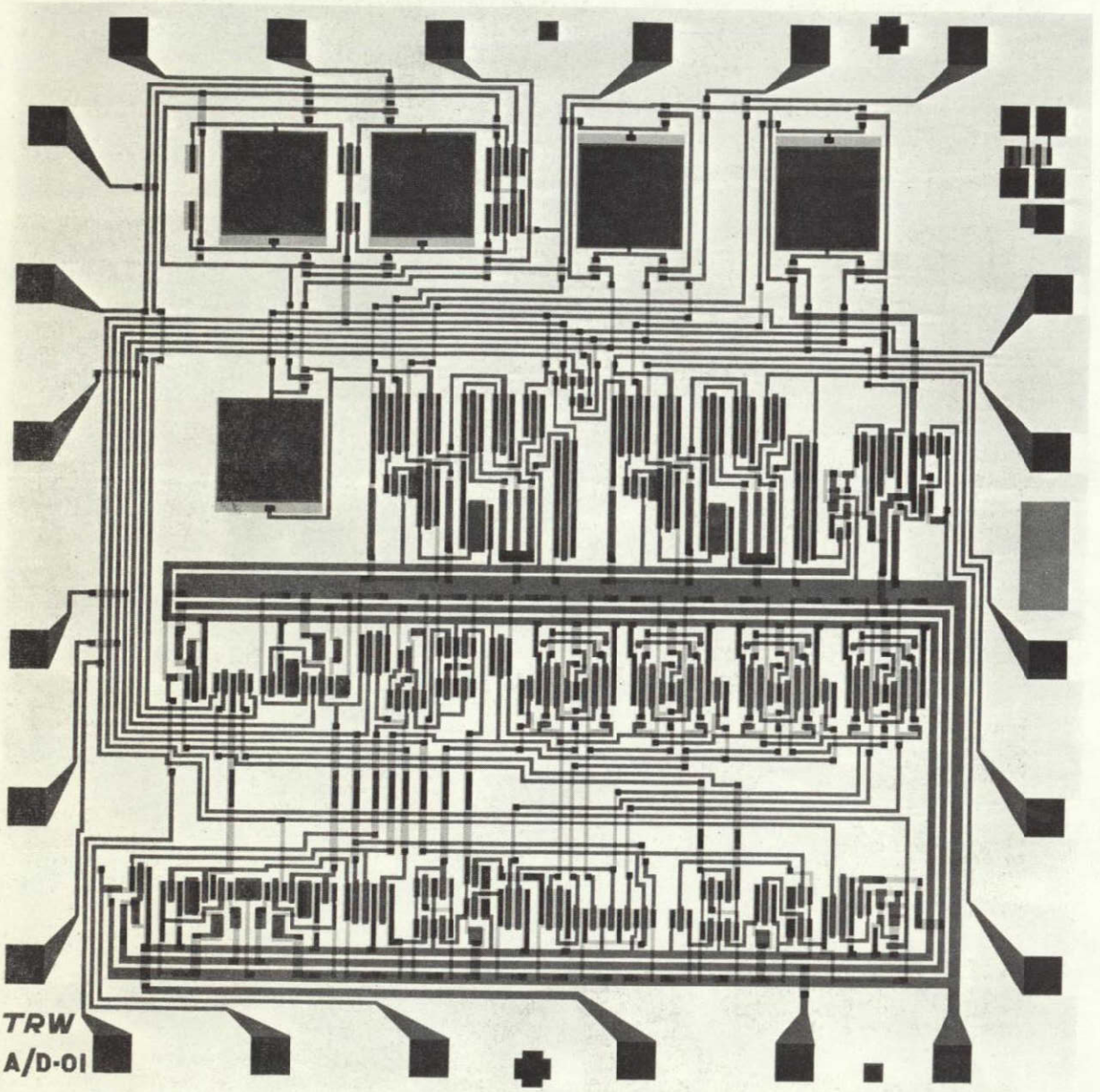
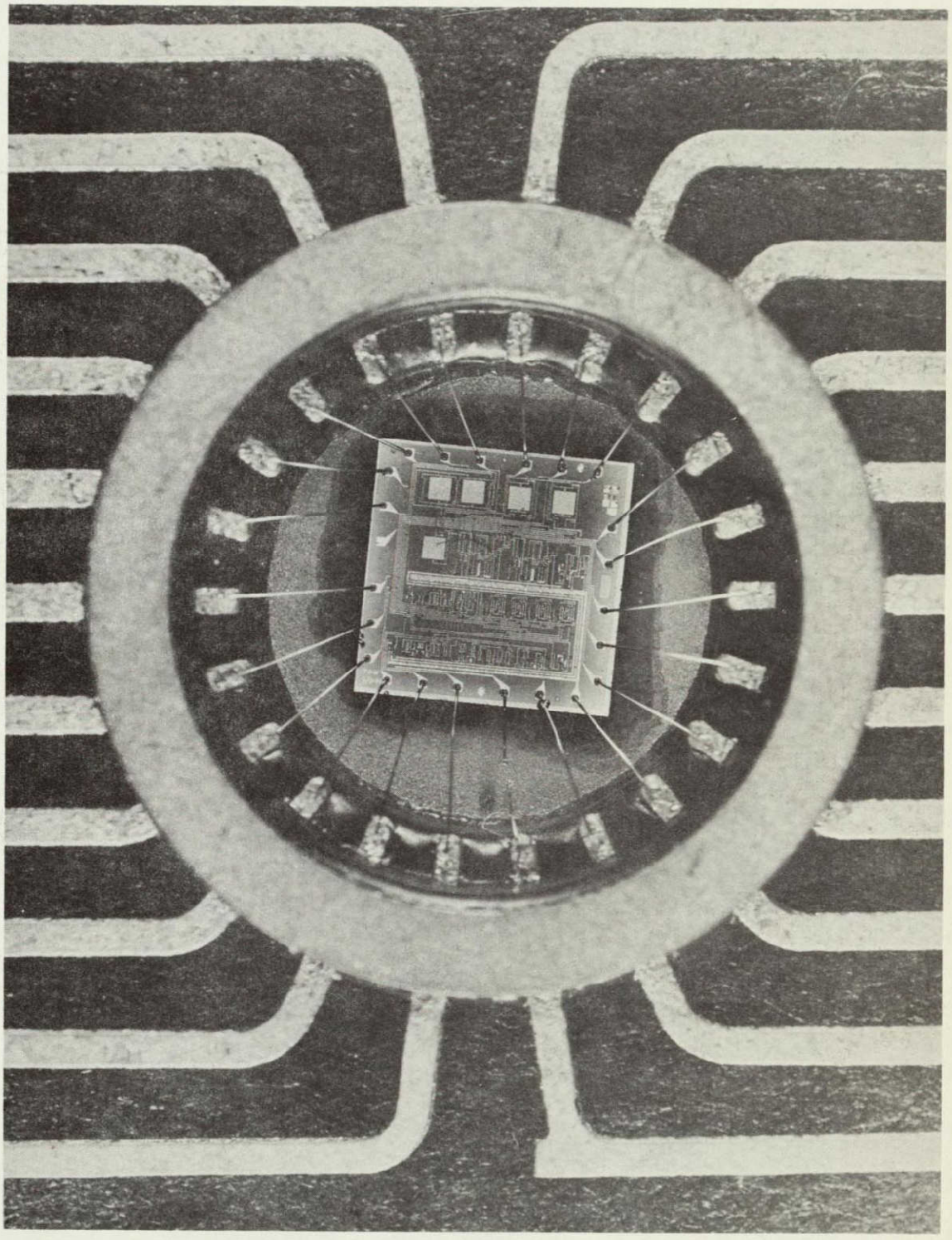


Figure 15. Composite Artwork



APPENDIX 1

PIN CONNECTIONS FOR TOTAL SYSTEM

TABLE 1

A/D Converter

Pin	Connection	Pin	Connection
1	Gnd	12	From multiplexer
2	-27 0 V	13	-5 120 V
3	Output	14	L_o
4	C_o	15	L_1
5	C_{C2}	16	$\overline{T}_o$
6	C_{C1}	17	T_o
7	A_{C2}	18	t_{even}
8	A_{C1}	19	t'_{even}
9	A_o	20	Synch out
10	A+	21	t'_{odd}
11	A-	22	+12 0 V

TABLE 2

PL4S16C 16-Channel MOS Multiplexer (Sequential Operation)

Pin	Connection	Pin	Connection
1	+5.0 V	18	Channel 0
2	-23 0 V	19	Channel 1
3	No connection	20	Channel 2
4	No connection	21	Channel 3
5	-23 0 V	22	Channel 4
6	No connection	23	Channel 5
7	+5 0 V	24	Channel 6
8	From A/D Synch Out	25	Channel 7
9	No connection	26	Channel 8
10	-23 0 V	27	Channel 9
11	From A/D Synch Out	28	Channel 10
12	No connection	29	Channel 11
13	No connection	30	Channel 12
14	No connection	31	Channel 13
15	No connection	32	Channel 14
16	+5.0 V	33	Channel 15
17	To A/D converter	34	To A/D converter

TABLE 3

SP51C MOS Serial/Parallel Converter

Pin	Connection	Pin	Connection
1	Gnd	12	Bit 8 out
2	-27 0 V	13	Bit 9 out
3	From A/D output	14	Bit 10 out
4	Bit 1 out	15	Bit 11 out
5	Gnd	16	Bit 12 out
6	Bit 2 out	17	-27 0 V
7	Bit 3 out	18	From MEM1015
8	Bit 4 out	19	Gnd
9	Bit 5 out	20	-27 0 V
10	Bit 6 out	21	From t'_{even}
11	Bit 7 out	22	From t'_{odd}

TABLE 4

For MEM1015

Pin	Connection	Pin	Connection
1	Gnd	13	No connection
2	From A/D Synch out	14	Gnd
3	From t'_{even}	15	To pin 21
4	Gnd	16	Gnd
5	Gnd	17	No connection
6	-27 0 V	18	To serial/parallel converter
7	Gnd	19	To -12 5 V
8	Gnd	20	To pins 10, 23
9	From t'_{odd}	21	To pin 15
10	To pins 20, 23	22	Gnd
11	Gnd	23	To pins 10, 20
12	No connection	24	Gnd

TABLE 5

NH0007 MOS Clock Driver

Pin	Connection	Pin	Connection
1	From clock	6	-27 0 V
2	From Sn7472	7	Output
3	No connection	8	No connection
4	Gnd	9	+5 0 V
5	No connection	10	Gnd

TABLE 6

Pin Connections for SN7472 Flip-flop*

Pin	Connection	Pin	Connection
1	No connection	8	To clock driver 2
2	No connection	9	No connection
3	No connection	10	No connection
4	No connection	11	No connection
5	No connection	12	From clock
6	To clock driver 1	13	No connection
7	Gnd	14	+5 0 V

*Comes in a standard dual in-line package

APPENDIX 2

DATA SHEETS

12–BIT SERIAL/PARALLEL CONVERTER SP51C

FUNCTIONAL DESCRIPTION — The 12 Bit Serial to Parallel Converter is one of a family of compatible 1 MHz MOS integrated circuits This circuit is capable of converting serial input data to parallel output data Permanent data storage is achieved when the clocks are in the proper states of ϕ_1 = ground and ϕ_2 = –27V Set and Reset inputs are provided to set or reset all stages in parallel synchronously one bit time after the Set or Reset command occurs Power consumption is essentially independent of frequency and typically is 270 mW for V_{GG} = –27V Zener diode gate protection is featured on all inputs The schematic of a typical stage is shown in Fig 1 The package dimensions are shown in Fig 2 and the connection diagram is shown in Fig 3

APPLICATIONS — The SP01C can be used to perform a variety of functions It is capable of converting serial data to 12 bit parallel data It may be operated as a 12 channel commutator, a 1 to 12 bit serial shift register or as a D/A converter ladder driver Fig 4 shows typical waveforms for circuit operation as a shift register or a serial to parallel/ converter

MAXIMUM RATINGS (Note 1)

MAXIMUM TEMPERATURES	
Storage Temperature	–65 to +150°C
Operating Channel (Junction) Temperature	–55 to +150°C
Operating Ambient Temperature	–25 to +75°C
MAXIMUM PACKAGE POWER DISSIPATION (Note 2)	
Total Dissipation at 25°C Ambient Temperature	635 mW
MAXIMUM VOLTAGES (Referenced to Ground Pin)	
Maximum Negative Voltage on any Pin	–30 Vdc
Maximum Positive Voltage on any Pin	+0 3 Vdc

ELECTRICAL CHARACTERISTICS — Characteristics apply at the test conditions T_A = 25°C Load = 10 MΩ + 20 pF to ground

Characteristics	Min	Typ	Max	Units	Conditions
Supply Voltage (V_{GG})	–24	–27	–30	V	
DC Power Consumption	—	270	—	mW	V_{GG} = –27V V_ϕ = –27V f = 1 0 MHz
Clock 1 Level (V	–24	–27	–30	V	
Clock 0 Level	0	—	– 2 0	V	
Shift Rate	dc	—	1 0	MHz	V_{GG} = –27V V_ϕ = –27V
ϕ_1 Clock Pulse Width	450	—	—	ns	
ϕ_2 Clock Pulse Width	450	—	—	ns	
Clock Pulse Spacing	0	—	50	μs	
Input Pulse Width	300	—	—	ns	Note 3
Input 1 Level	– 9 0	—	—	V	
Input 0 Level	—	—	– 3 5	V	
Output 1 Level	– 9 5	—	—	V	V_{GG}=-30V,Common$_2$=-30V
Output 0 Level	—	—	– 2 0	V	V_ϕ=-27V,f=1 0MHz ϕ_W=450ns
Output Switch Current (I_{SW})	—	—	–10	mA	
Output Switch Resistance	—	1800	—	Ω	Common=-10V,I_{SW}=-1 0μA
Output Switch Resistance	—	700	—	Ω	Common=0V,I_{SW}=-1 0μA
Output Switch Offset	—	0	—	mV	
Input Capacity	—	2 5	—	pF	V_{in} = 0V
Clock Capacity	—	10	—	pF	V_ϕ = 0V

Note 1 This product can be supplied to meet full military specifications
Note 2 Derating factor is 5 1 mW/°C above +25°C ambient
Note 3 Two non overlapping clock pulses, ϕ_1 and ϕ_2 are required Input data is required to be valid through the end of the ϕ_1 clock

AMERICAN MICRO-SYSTEMS, INC

3800 HOMESTEAD ROAD SANTA CLARA CALIFORNIA 95051 ● (408) 246-0330

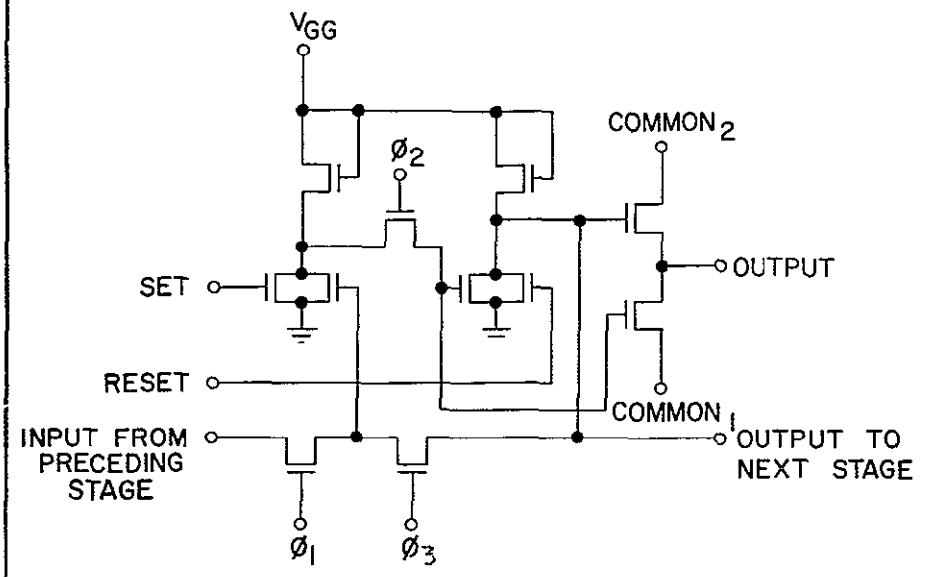


Fig 1 Schematic of a Typical Stage

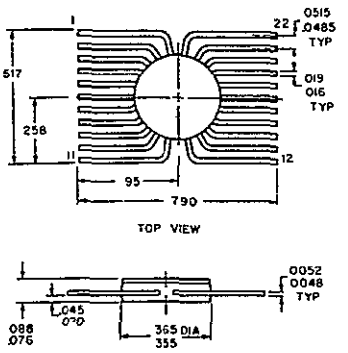
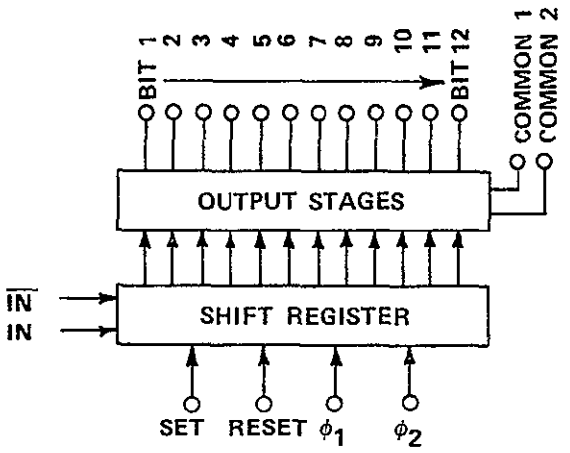


Fig 2 Package Dimensions



Pin	Function	Pin	Function
1	GND	12	BIT 8
2	IN	13	BIT 9
3	IN	14	BIT 10
4	BIT 1	15	BIT 11
5	COMMON 1	16	BIT 12
6	BIT 2	17	COMMON 2
7	BIT 3	18	RESET
8	BIT 4	19	SET
9	BIT 5	20	V_{GG}
10	BIT 6	21	ϕ_1
11	BIT 7	22	ϕ_2

NOTES

1 Pin 3 must be grounded when not in use
Pin 2 must be at V_{GG} when not in use
2 For shift register applications ground Pin 5 and apply −27 V to Pin 17
3 For commutator usage apply inputs to Pins 4 6 16 Take output from Pins 5 or 17
4 For D/A converter applications put ground on Pin 5 and −10 V on Pin 17 Connect Pins 4 6 16 to D/A ladder
5 Output switches will be in position shown with continuous zeros on true input or after reset is energized
6 All unused inputs should be grounded

Fig 3 Connection Diagram

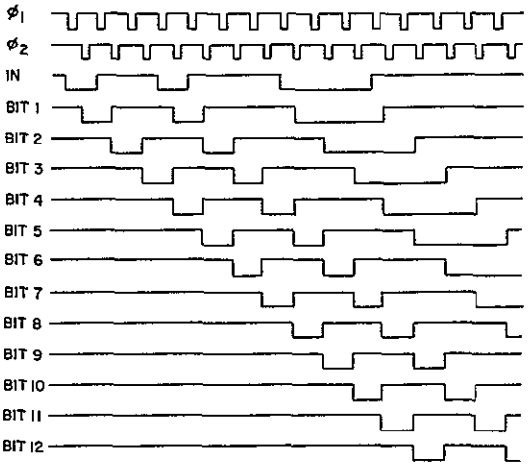


Fig 4 Typical Waveforms For Operation as a Shift Register or Converter

GENERAL INSTRUMENT

GENERAL INSTRUMENT MTOS INTEGRATED CIRCUIT

ADVANCE
JULY 1, 1967

DUAL J/K FLIP-FLOP

MEM 1015

DESCRIPTION

The MEM 1015 dual J K flip flop is constructed on a single monolithic chip utilizing MTOS P channel enhancement mode transistors A chip contains two identical flip flops Each has a separate clock input, two J inputs (OR'ed together) and two K inputs (OR'ed together), a direct set and a direct reset A truth table is provided which describes the output switch ing conditions for all input combinations

TRUTH TABLE

Q_n	J_1 J_2	K_1 K_2	S	R	Q_{n+1}	Notes
0 1	0 0 0 0	0 0 0 0	0 0	0 0	0 1	No change of state of outputs
Ø	{0 1 1 0 1 1}	0 0	0	0	1	J input must be "1" when clock is "1 " Outputs change state on trailing edge of clock input (positive going edge)
Ø	0 0	{0 1 1 0 1 1}	0	0	0	K input must be "1" when clock is "1 " Outputs change state on trainling edge of clock input (positive going edge)
Q_n	{0 1 1 0 1 1}	{0 1 1 0 1 1}	0	0	$\overline{Q}_n$	Toggle mode Inputs must be "1" when clock is "1 " Outputs change state on trail ing edge of clock input (positive going)
Ø	Ø	Ø	0	1	0	Direct reset Outputs change state on lead ing edge of reset input (negative going edge)
Ø	Ø	Ø	1	0	1	Direct set Outputs change state on leading edge of set input (negative going edge)
Ø	Ø	Ø	1	1	X	Non allowable condition

Ø = don't care
X = undefined state

MAXIMUM RATINGS

Drain Voltage (V_{dd})	−30V to +0 3V
Gate Voltage (V_{GG})	−30V to +0 3V
Logic Input Voltage	−30V to +0 3V
Storage Temperature	−55°C to +150°C
Operating Temperature	−55°C to +85°C

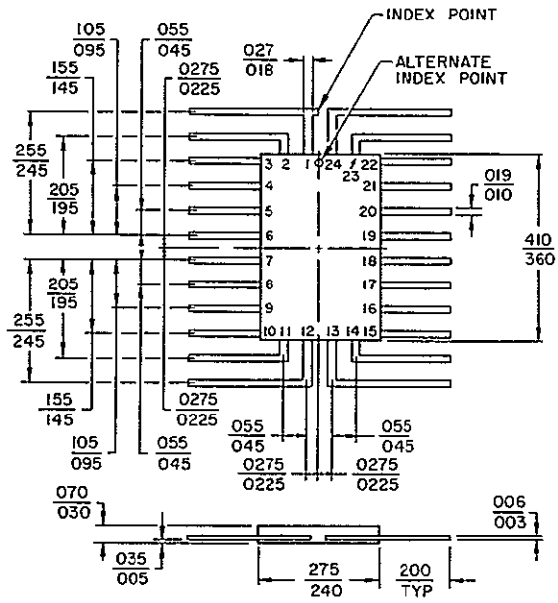
ELECTRICAL CHARACTERISTICS

STANDARD CONDITIONS (unless otherwise specified)

V_{GG} = −27 Volts ± 1 Volt R_L = 1 0MΩ, C_L = 25 pF T_A = −55°C to +85°C,
V_{DD} = −13 Volts ± 1 Volt

Characteristics	Min	Typ	Max	Units	Conditions
Clock Input					
Repetition rate	d c	—	1 0	MHz	
Rise & fall time (10% to 90%)	—	—	50 0	μS	
Logic "0" level	—	—	2 0	Volts	
Logic 1 level	−10	—	—	Volts	
Leakage current	—	—	5 0	μA	V_{CLOCK} = −20 volts
Control Inputs					
Logic 0 level	—	—	2 0	Volts	
Logic 1 level	−10	—	—	Volts	
Leakage current	—	—	5 0	μA	V_n = −20 volts
Capacity	—	2 0	3 0	pF	
Outputs					
Propagation delay (Tpd) (50% clock to 50% output)	—	300	350	nS	(See Fig 1)
Rise time (10% to 90%)	—	120	150	nS	−9 0 volts to −2 2 volts
Fall time (10% to 90%)	—	160	200	nS	−2 2 volts to −9 0 volts
Voltage drive capability	−10	—	—	Volts	R_L = 25K ohms to ground
Capacitance drive capability	—	—	25	pF	
Impedance to ground	—	1000	2500	Ohms	I_{out} = 1 0 mA
Supply Current					
I_{GG}	—	3 2	4 75	mA	
I_{DD}	—	2 0	2 8	mA	

24 LEAD FLAT PACK



Note All dimensions in inches

TERMINALS

P/N	FUNCTION	P/N	FUNCTION
1	Ground	13	No connection
2	J_{1A}	14	J_{2B}
3	$Clock_A$	15	K_{1B}
4	$Reset_A$	16	K_{2B}
5	Set_A	17	$\overline{Q}_B$
6	V_{GG}	18	Q_B
7	Set_B	19	V_{DD}
8	$Reset_B$	20	Q_A
9	$Clock_B$	21	$\overline{Q}_A$
10	J_{1B}	22	K_{2A}
11	Ground	23	K_{1A}
12	No connection	24	J_{2A}

TYPICAL WAVEFORMS

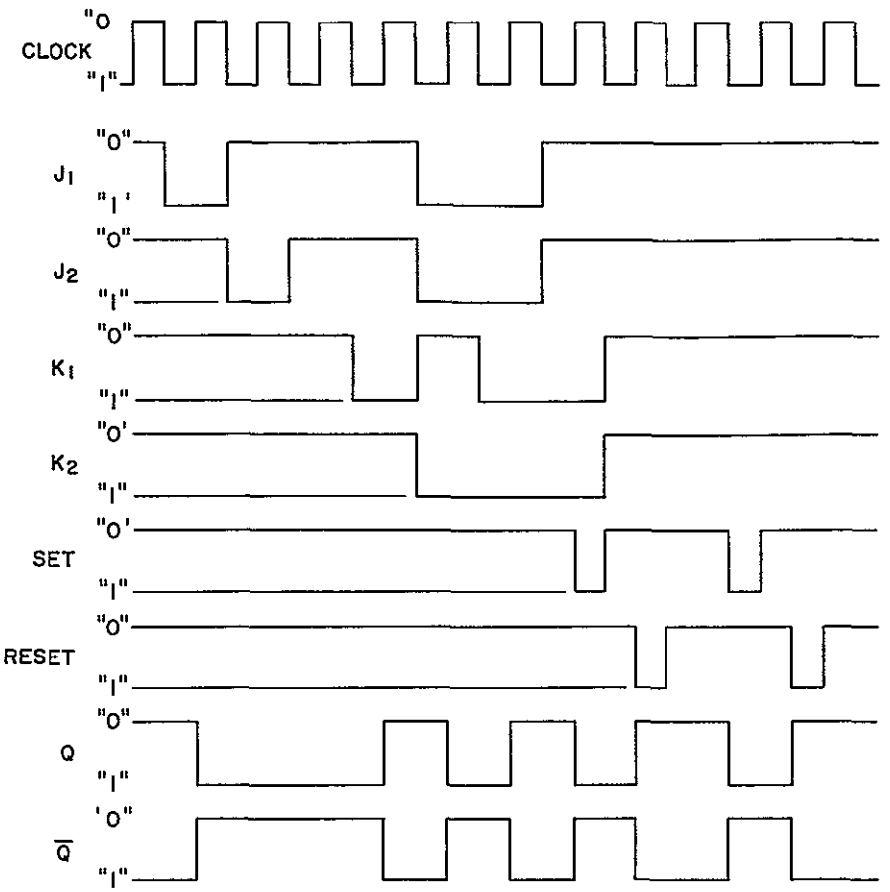
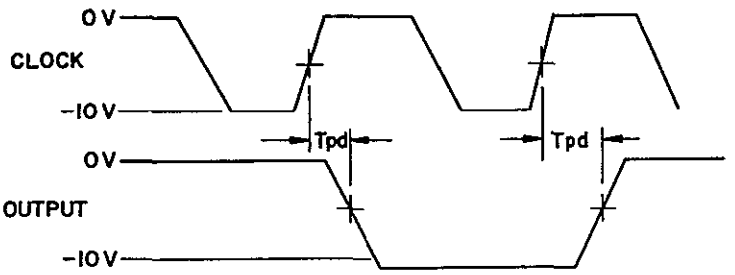


FIGURE 1



GENERAL INSTRUMENT CORPORATION
MICROELECTRONICS DIVISION

EASTERN AREA SALES HEADQUARTERS, 65 Gouverneur St., Newark N J 07104, (201) HU 5 0072
CENTRAL AREA SALES HEADQUARTERS, 6054 West Touhy Ave Chicago, Ill 60648 (312) 774 7800
WESTERN AREA SALES HEADQUARTERS, 18455 Burbank Blvd Tarzana, Calif 91356, (213) 873-6500

600 West John Street
Hicksville, L I N Y. 11802
(516) OV 1 8000

Printed in U S A

16-CHANNEL MOS MULTIPLEXER pL4S16C

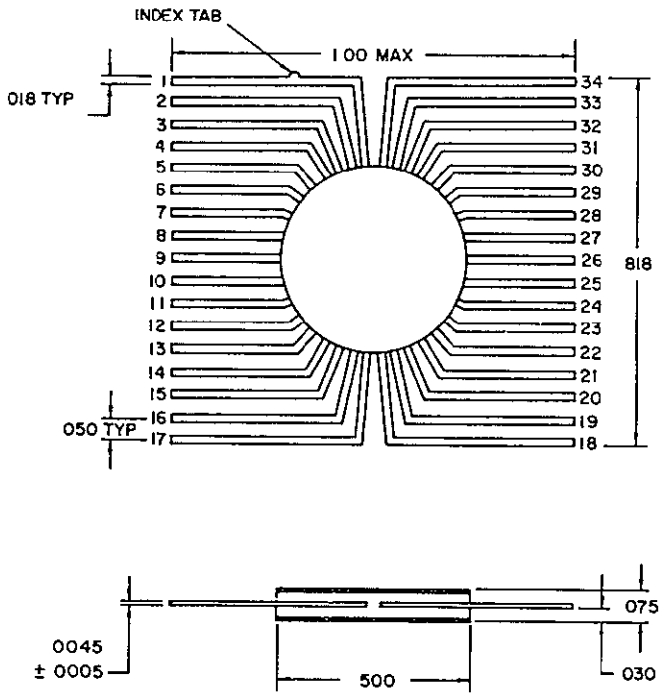
TENTATIVE SPECIFICATIONS

OCTOBER 1969

GENERAL DESCRIPTION

The Philco Ford pL4S16C 16 Channel Multiplexer is a monolithic MOS LSI device which may be used in many applications requiring sequential or random access multiplexing The applications include telemetry satellite communications sample data systems etc The chip contains 16 channel switches a 4-bit address register/counter random access gating decode matrix and a control flip flop The control flip flop is used for additional address storage when large multiplexing systems (any multiple of sixteen) are formed by suitable interconnection of pL4S16 devices The device may also be used as an 8 Channel Differential Multiplexer For detailed device operation see Application Note No 406

PACKAGING



34-Lead Flat Package

Pin No	Function	Pin No	Function
1	Ground	18	CH 0
2	V_{DD}	19	CH 1
3	Output Shunt Control	20	CH 2
4	Sync Out	21	CH 3
5	Control F/F Set	22	CH 4
6	Control F/F $\overline{\text{Reset}}$ Out	23	CH 5
7	Control F/F Reset	24	CH 6
8	Control F/F Clock	25	CH 7
9	Matrix Control Out	26	CH 8
10	8/16 Control	27	CH 9
11	Clock	28	CH 10
12	2^3 Address In	29	CH 11
13	2^2 Address In	30	CH 12
14	2^1 Address In	31	CH 13
15	2^0 Address In	32	CH 14
16	Parallel Load	33	CH 15
17	Multiplex Out (0-7)	34	Multiplex Out (8-15)

PHILCO Ford

MICROELECTRONICS DIVISION
Philco-Ford Corporation
Blue Bell, Pennsylvania 19422

MAXIMUM RATINGS

Storage Temperature Range Ambient	-65°C to +150°C
Operating Temperature Range	0°C to +70°C
V_{DD}	-33V to +0 3V (See Note 1)

ELECTRICAL CHARACTERISTICS

Standard Conditions (Unless Otherwise Specified)

T_A = +25°C V_{DD} = -28 ±1V **Logic Output Load** - 500 kΩ, 20 pF to Ground

CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
Signal Voltages V_{IN}	0	-10	Volts	See Note 2
Clock Frequency	0	100	kHz	Sequential Mode
Clock and Parallel Load Pulse Width	2		μs	See Note 3
Switch Settling Time		5	μs	From -10V point on clock to 90% point on output R_S = 1kΩ
All Logic/Control Inputs				
1	-9		Volts	
0		-3	Volts	
Input Capacitance (Each Channel)		5	pF	V_{IN} = -5V
Channel Switch R_{ON}		1000	Ω	V_{IN} = -1V
Shunt Switch R_{ON}		1000	Ω	$V_{pin\ 3}$ = -9V V_{OUT} = -1 0V
Switch Input Leakage		10	nA	V_{IN} = -5V T_A = +25°C
Output Leakage (16 Channels in Parallel)		20	nA	V_{IN} = -5V T_A = +25°C
Channel Switch OFF Impedance Z_{OFF}	3		MΩ	V_{IN} = -10V f = 50 kHz
Power Dissipation		150	mW	V_{DD} = -28V

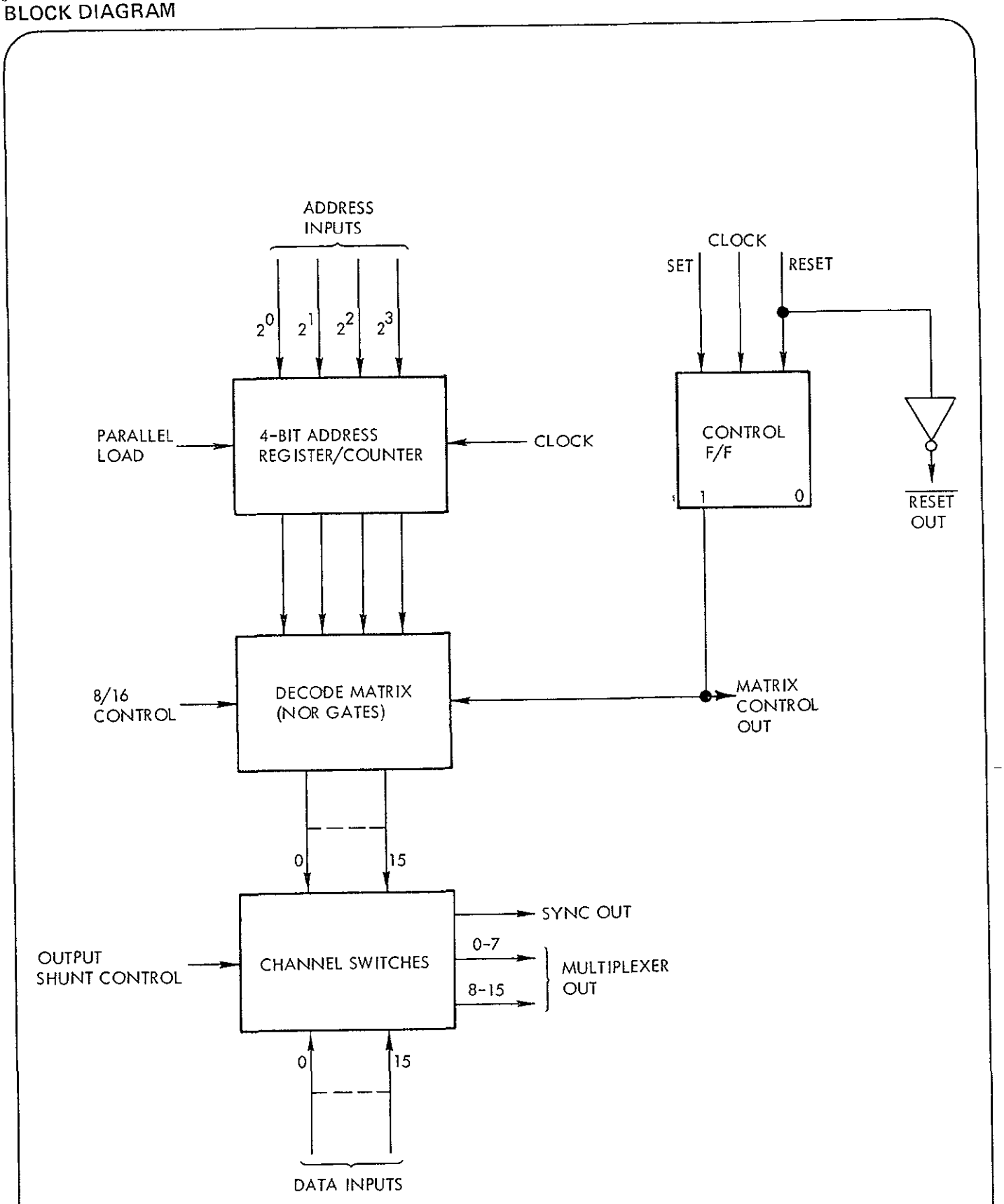
NOTES

1 A voltage more positive than 0 3 V with respect to GND (pin 1) should not be applied to any pin If positive input voltages are used pin 1 should be held at the most positive input voltage and V_{DD} should be reduced to maintain 28 V + 1 V across the circuit

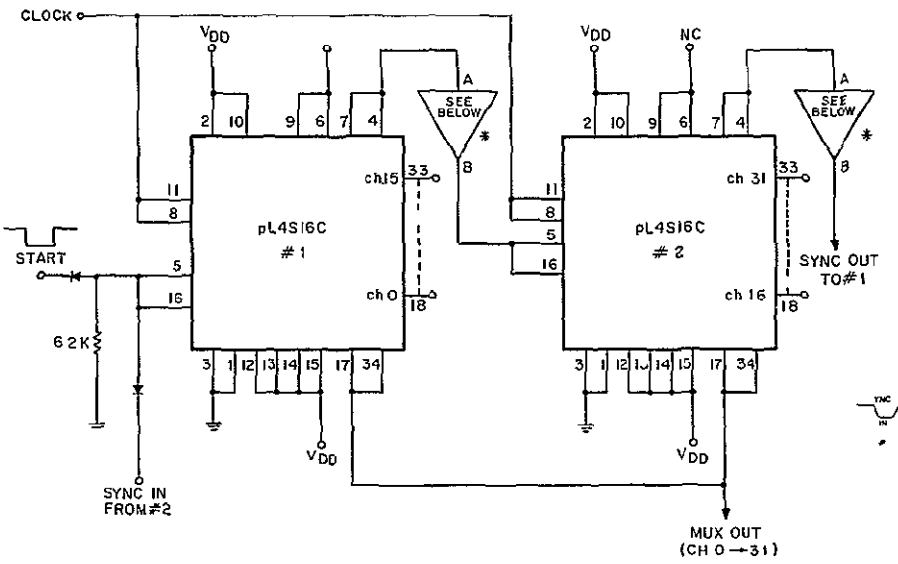
2 Pin 1 (GND) may be biased to other voltages to change the signal voltage range For example if pin 1 is biased to +5V the signal voltage range becomes +5V Pin 2 (V_{DD}) should then be held at 23V +1V to maintain 28V +1V across the circuit

3 The address inputs pins 12 through 15 should remain at a fixed logic level during the parallel load pulse

BLOCK DIAGRAM



TYPICAL INTERCONNECTIONS



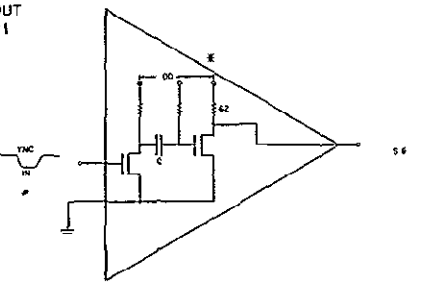
TYPICAL COMPONENTS

Q1 Q2 = MOS FET (2N3608 pL4S10) or Equiv

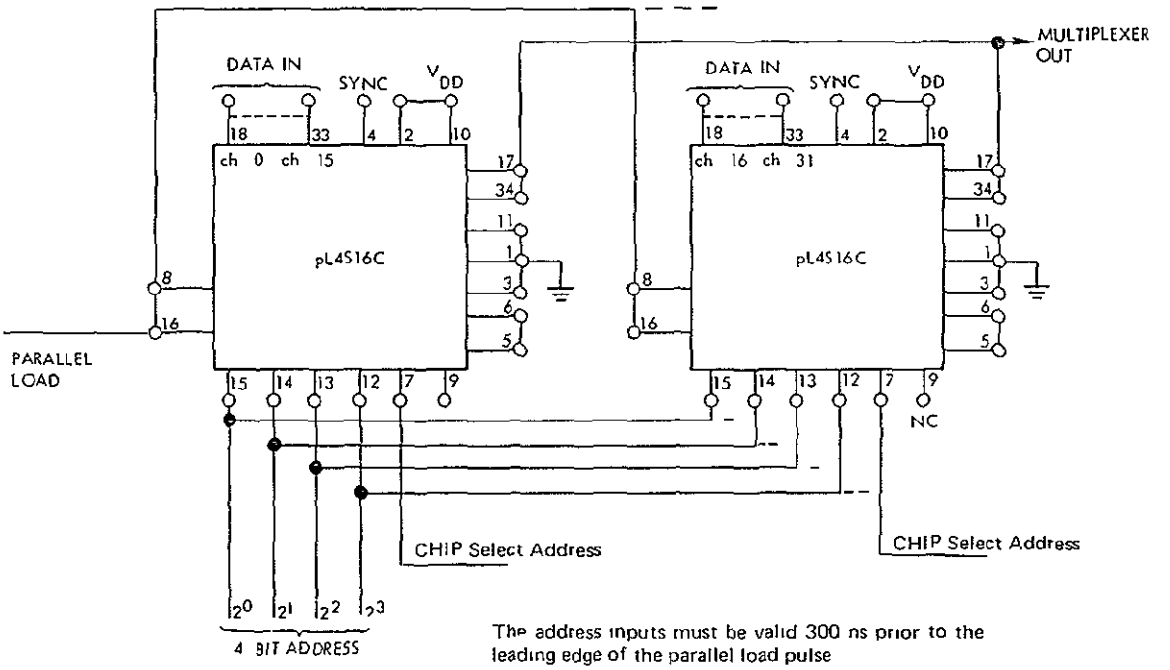
R = 1 MΩ

C = 1200 pF

For 1 MS (IKC) Clock



SEQUENTIAL SAMPLING OF 32 CHANNELS



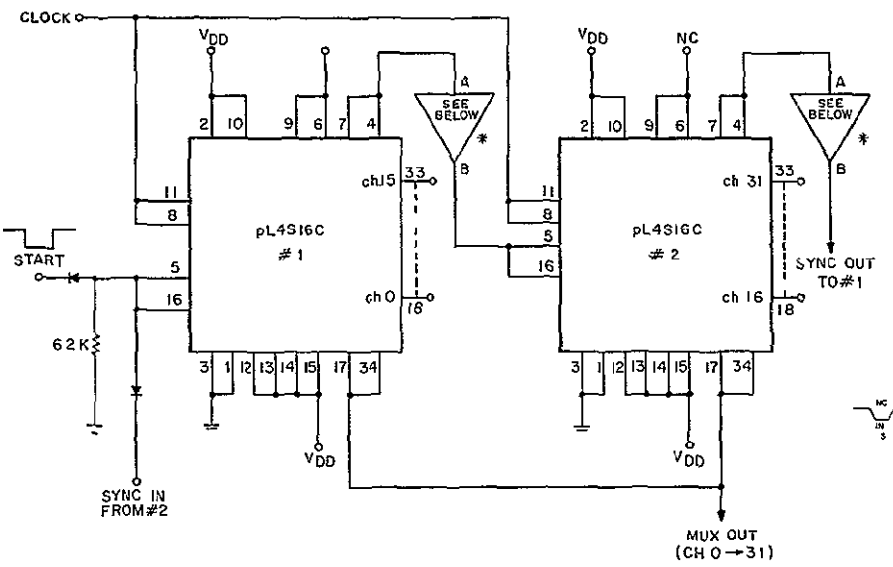
The address inputs must be valid 300 ns prior to the leading edge of the parallel load pulse

RANDOM ACCESS TO 32 OR MORE CHANNELS

For further information contact nearest sales office

Printed in USA

TYPICAL INTERCONNECTIONS



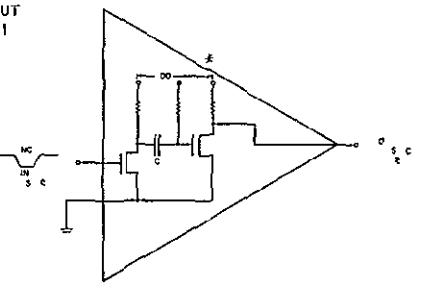
TYPICAL COMPONENTS

Q1 Q2 = MOS FET (2N3608 pL4S10) or Equiv

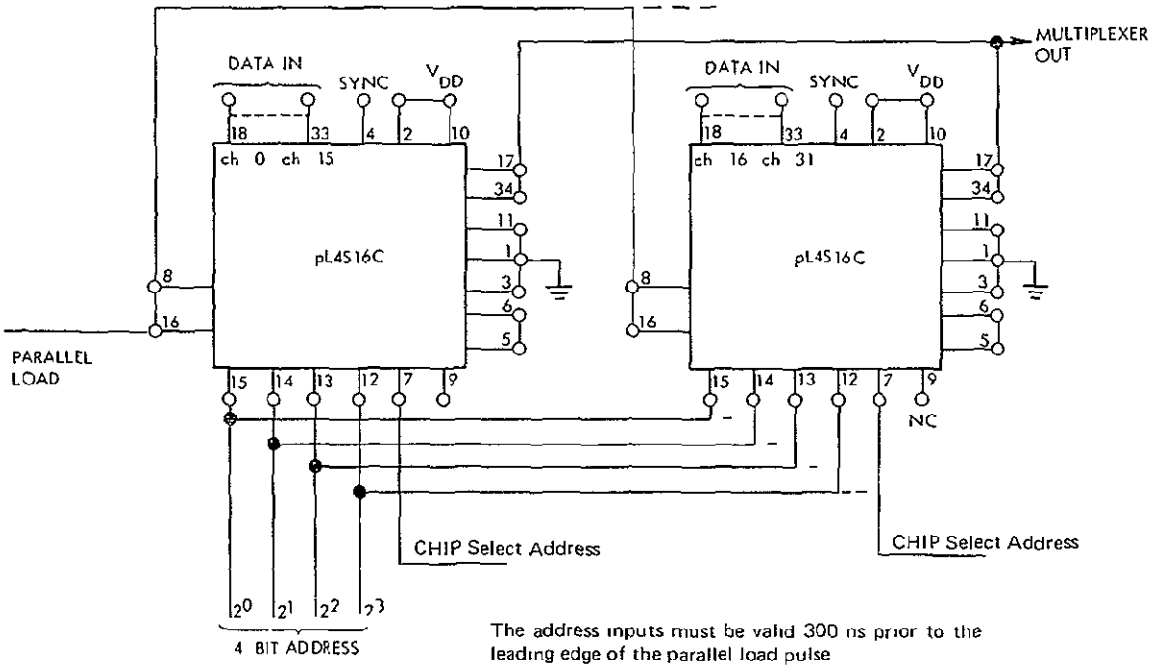
R = 1 MΩ

C = 1200 pF

For 1 MS (1KC) Clock



SEQUENTIAL SAMPLING OF 32 CHANNELS



RANDOM ACCESS TO 32 OR MORE CHANNELS

Printed in USA

NH0007/NH0007C MOS clock driver

NH0007/NH0007C MOS clock driver

general description

The NH0007 is a voltage translator and power booster designed for interfacing between conventional TTL or DTL voltage levels and those levels associated with inputs or clocks of MOS FET type devices The design allows the user a wide latitude in selection of supply voltages and is especially useful in normally off applications since power dissipation is typically only 5 milliwatts in the off state

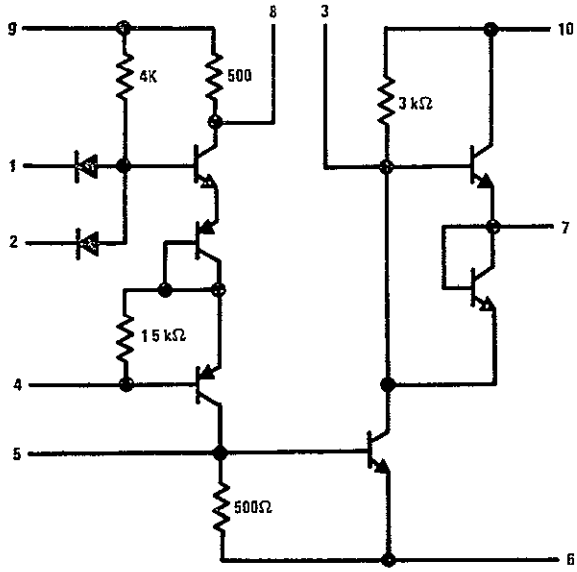
Additional features include

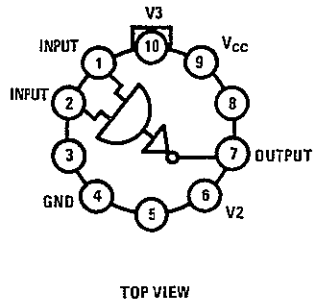
- 30 volts (max) output swing
- Standard 5V power supply
- Peak currents in excess of ±300 mA available
- Compatible with all MOS devices
- Temperature range

  NH0007 −55°C to +125°C

  NH0007C 0°C to +70°C
- High speed 5 MHz with nominal load
- External trimming possible for increased performance

schematic and connection diagram

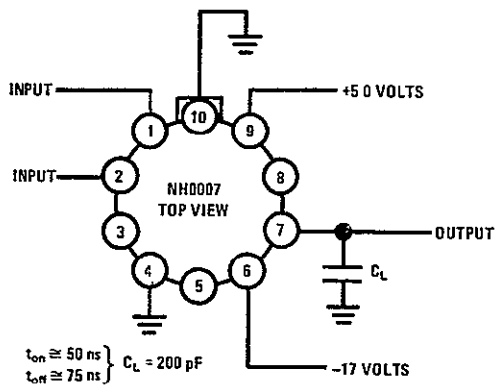




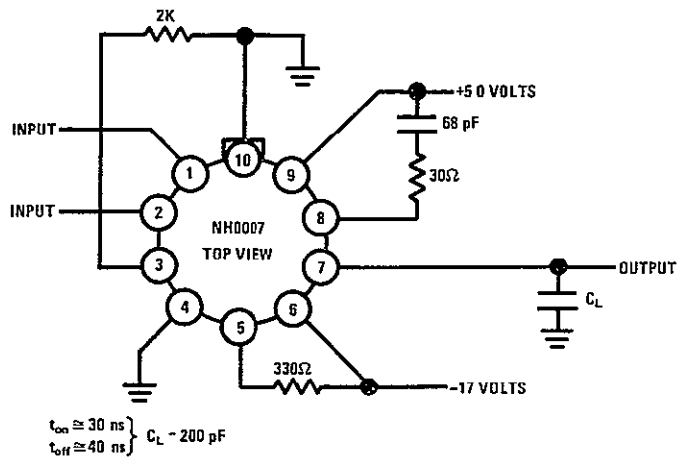
TOP VIEW

typical applications

Switching Time Test Configuration



High Speed Operation



PRINTED IN U S A

absolute maximum ratings

V_{CC} Supply Voltage		8 volts
V_2 Supply Voltage		−40 volts
V_3 Supply Voltage		+28 volts
(V_3 − V_2) Voltage Differential		30 volts
Input Voltage		5 5 volts
Peak Output Current		±500 mA
Storage Temperature Range		−65°C to +150°C
Operating Temperature Range	NH0007	−55°C to +125°C
	NH0007C	0°C to +70°C
Lead Temperature (Soldering 60 sec)		300°C 1/16 from case

electrical characteristics (Note 1)

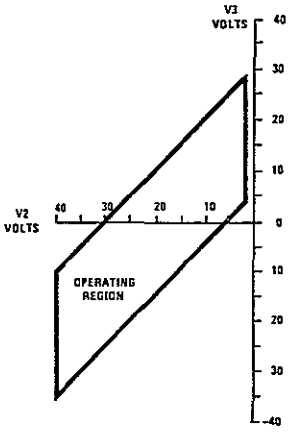
PARAMETER	CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
Logical 1 Input Voltage	V_{CC} = 4 5V	2 2			V
Logical 0 Input Voltage	V_{CC} = 4 5V			0 8	V
Logical 1 Input Current	V_{CC} = 5 5V V_{IN} = 5 5V			100	μA
Logical 0 Input Current	V_{CC} = 5 5V V_{IN} = 0 4V		1 0	1 5	mA
Logical 1 Output Voltage	V_{CC} = 5 5V I_{OUT} = 30 mA V_{IN} = 0 8V	V_3 − 4 0			V
	V_{CC} = 5 5V I_{OUT} = 1 mA V_{IN} = 0 8V	V_3 − 2 0			V
Logical 0 Output Voltage	V_{CC} = 4 5V I_{OUT} = 30 mA V_{IN} = 2 2V			V_2 + 2 0	V
Transition Time to Logical 0 Output	C_L = 200 pF (Note 3)		50		ns
Transition Time to Logical 1 Output	C_L = 200 pF (Note 3)		75		ns

Note 1 Min/max limits apply across the guaranteed range of −55 C to +125 C for the NH0007 and from 0°C to +70 C for the NH0007C for all allowable values of V_2 and V_3

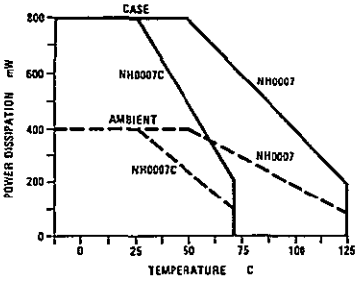
Note 2 All typical values measured at T_A = 25°C with V_{CC} = 5 0 volt V_2 = −25 volts V_3 = 0 volts

Note 3 Transition time measured from time V_o = 50% value until V_o has reached 80% of final value

Allowable Values for V2 and V3



Power Dissipation Vs Ambient and Case Temperature



National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, California 95051
(408) 732-5000 / TWX (910) 339-9240

APPENDIX 3

TEST PROCEDURES

TRW
SYSTEMS GROUP

MICROELECTRONICS CENTER

MANUFACTURING PROCESS

TITLE

ELECTRICAL TESTS FOR NATIONAL SEMICONDUCTOR

NH0007 MOS CLOCK DRIVER

DATE 6-18-70 DOCUMENT NO MF1-562A

SUPERSEDING Original Issue

4-23-70

Originator	Prepared:	Approved
J. E. Eaton	K I Novinsky	
	Documentation	Product Development
Approved:	**Approved**	
	J Egan	
Product Applications	Department Manager	

NOTE This document for MEC use only.

DOCUMENT NO MF1-562A

REVISION RECORD

REVISION	DATE	AUTHORIZATION	EFFECTIVE PAGES
	4-23-70	See Title Page	Original Issues Pages 1 through 3
Rev. A.	6-18-70		Page 2, 4.4, 4.4.2· added "after 10 sec." Page 3, Pulse Generator Output 2μsec max

ACCEPTANCE TEST PLAN

ELECTRICAL TESTS FOR NATIONAL SEMICONDUCTOR NH0007 MOS CLOCK DRIVER

1 SCOPE

This document specifies the electrical tests to be performed on the National Semiconductor NH0007 MOS Clock Driver.

2. EQUIPMENT REQUIRED

2.1 Test Equipment

a Lambda LH-124 (or equivalent) power supplies (2 required)

b HP 3440 Digital Voltmeter (or equivalent)

c Oscilloscope, Tektronix 541 or 545 with type N plug-in.

d Probes - 7 pF 10:1 (4 required)

e Pulse Generator, Rutherford B7B (or equivalent)

3. PREPARATION FOR OPERATION

3 1 Turn on oscilloscope

3.2 Turn on DVM

3.3 Turn on V_{DD} supply and adjust for read -25 VDC

3.4 Turn on V_{CC} supply and adjust to +5 VDC $\pm$ 1 VDC.

3.5 Turn on pulse generator and adjust to output similar to that shown in Figure 1

4. OPERATIONAL PROCEDURES

4 1 Turn on Time measurement

4.1.1 Connect device as shown in Figure 1

4.1 2 Adjust output of the device so that the one level is at 25 VDC $\pm$ 5 VDC

4.1.3 With the oscilloscope, measure the output Turn on time to read less than 95 nsec Record these readings The measurement points shall be from 10% of the pulse generator to 90% of the clock output

4.1 4 Reverse leads connected to pins 1 and 2, and repeat step 4.1.3.

4 2 Turn off time measurement

4 2 1 Leave setup as in 4 1

4.2 2 With the oscilloscope, measure the output turnoff time to be less than 180 ns The measurement points shall be from 90% of the pulse generator output to 10% of the clock output (Record these readings)

4 2 3 Reverse the leads connected to pins 1 and 2 and repeat step 4 2 2

4 3 "1" Output Level

4 3.1 Connect device as shown in Figure 1 except that the pulse generator should be replaced with $+V_{CC}$

4 3.2 With the DVM measure the output to read -24.0 $\pm$ 5 VDC Record this reading

4 4 "0" Output Level

4 4 1 Connect Pin 2 to ground

4 4 2 With the DVM measure the output to read -0 3 + 3, - 1 VDC (after 10 second)

4 5 High Temperature Testing

4 5 1 Place unit in environmental chamber

4 5 2 Elevate temperature to 100°C and allow to stabilize for 5 minutes

4 5 3 Repeat steps 4 1 through 4 4

4 6 Low Temperature Testing

4 6 1 Reduce chamber temperature to -20°C and allow to stabilize for five minutes

4 6 2 Repeat steps 4 1 through 4 4 with the following exceptions

a. 4.1.3 . turn on time to read less than 130 nsec

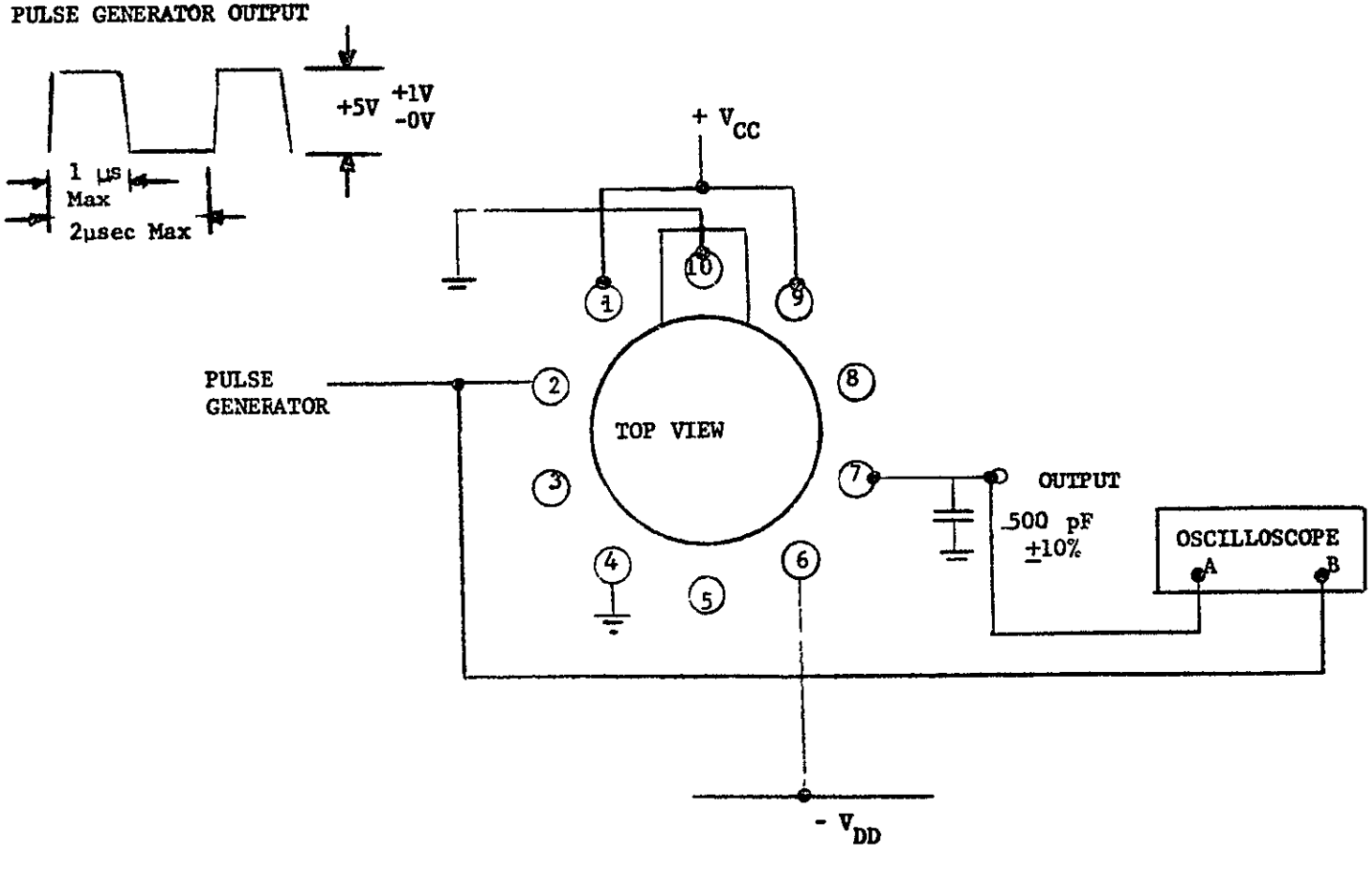

PULSE GENERATOR OUTPUT
+5V
+1V
-0V
1 µs
Max
2µsec Max
+ V_{CC}
PULSE
GENERATOR
TOP VIEW
OUTPUT
500 pF
±10%
OSCILLOSCOPE
A
B
- V_{DD}

Figure 1

TRW
SYSTEMS GROUP

MICROELECTRONICS CENTER

MANUFACTURING PROCESS

TITLE

FINAL ACCEPTANCE TEST PLAN
FOR
A M I 12-BIT SERIAL-TO-PARALLEL
CONVERTER, PN SP51C

DATE 6-18-70 DOCUMENT NO MF1-560A

SUPERSEDING Original Issue
4-1-70

Originator

Prepared:

Documentation

Approved

Product Development

Approved:

Product Applications

Approved

Department Manager

NOTE: This document for MEC use only.

DOCUMENT NO· MF1-560A

REVISION RECORD

REVISION	DATE	AUTHORIZATION	EFFECTIVE PAGES
	4-1-70	See Title Page	Original Issue Pages 1 through 5
Rev. A	6-16-70		Page 1, Para. 2, 2.1c, correct to read Type M Plug-in. Page 2, Add 4.1.5A Page 2, 4.2, 4.2.1, correct and add to end of sentence. Page 3, Make additions to drawing. Page4, Figure 2 , Correction in Figures. Page 1, Para. 4, 4.1.3, Addition at end of sentence.

FINAL ACCEPTANCE TEST PLAN
FOR
A M I. 12-BIT SERIAL-TO-PARALLEL CONVERTER, PN SP51C

1 Scope

This document specifies the final functional tests to be performed on the A M I SP51C serial-to-parallel converters

2. Equipment Required

2.1 Test Equipment

a. Lambda LH-124 (or equivalent) power supplies (4 required)
b. H-P 3440 Digital Voltmeter (or equivalent)
c. Oscilloscope, Tektronix 541 or 545 with Type M Plug-in (or equivalent)
d. Probes - 7 pF 10 1
e Pulse Generator, Rutherford B7B, or equivalent
f. Two phase Converter, any circuit capable of producing an output similar to that shown on Figure 2

3. Preparation for Operation

3 1 Turn on oscilloscope.
3 2 Connect power supplies as shown in Figure 1
3.3 Turn on D V M

4. Operational Procedure

4 1 Function Test

4 1 1 Connect device as shown in Figure 1
4.1 2 Turn on power supply #3 and adjust to read -24 0 VDC
4.1.3. Turn on power supply #4 and adjust to read -9 0 VDC $^{-1.0V}_{+0\ 0V}$
4 1 4 Turn on power supply #1 and adjust to +5 VDC.
4 1.5 Turn on power supply #2 and pulse generator Adjust them both so as to achieve an output from the two-phase generator as shown in Figure 2.

4 1 5A Connect pin 16 to pin 18

4 1 6 With the oscilloscope, check to see that the output on each pin is the same as that shown on Figure 3

4 1.7 Adjust power supply #3 to read -30 VDC and repeat step 4 1 6.

4.2 Output 1 Level

4.2 1 Disconnect Pin 16 from Pin 18 (leave all power supplies set as in 4.1.2). Gnd pin 18.

4 2 2 With the DVM, measure the outputs of Pins 4, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16 The meter should read -9 5 VDC min.

4.3 Output 0 Level

4 3 1 Decrease power supply #4 to -3 5 VDC

4 3 2 Repeat step #4 2 2 except that the meter shall read 0.0 VDC maximum

4 4 High Temperature Test

4 4.1 Place unit in temperature chamber

4 4.2 Elevate temperature to $100^{\circ} \pm 5^{\circ}C$ and allow to stabilize for 5 minutes

4 4 3 Repeat steps 4 1, 4 2, and 4.3.

4 5 Low Temperature Test

4 5.1 Lower chamber temperature to $-20^{\circ}C$ and allow to stabilize for 5 minutes

4.5 2 Repeat steps 4.1, 4 2 and 4 3.

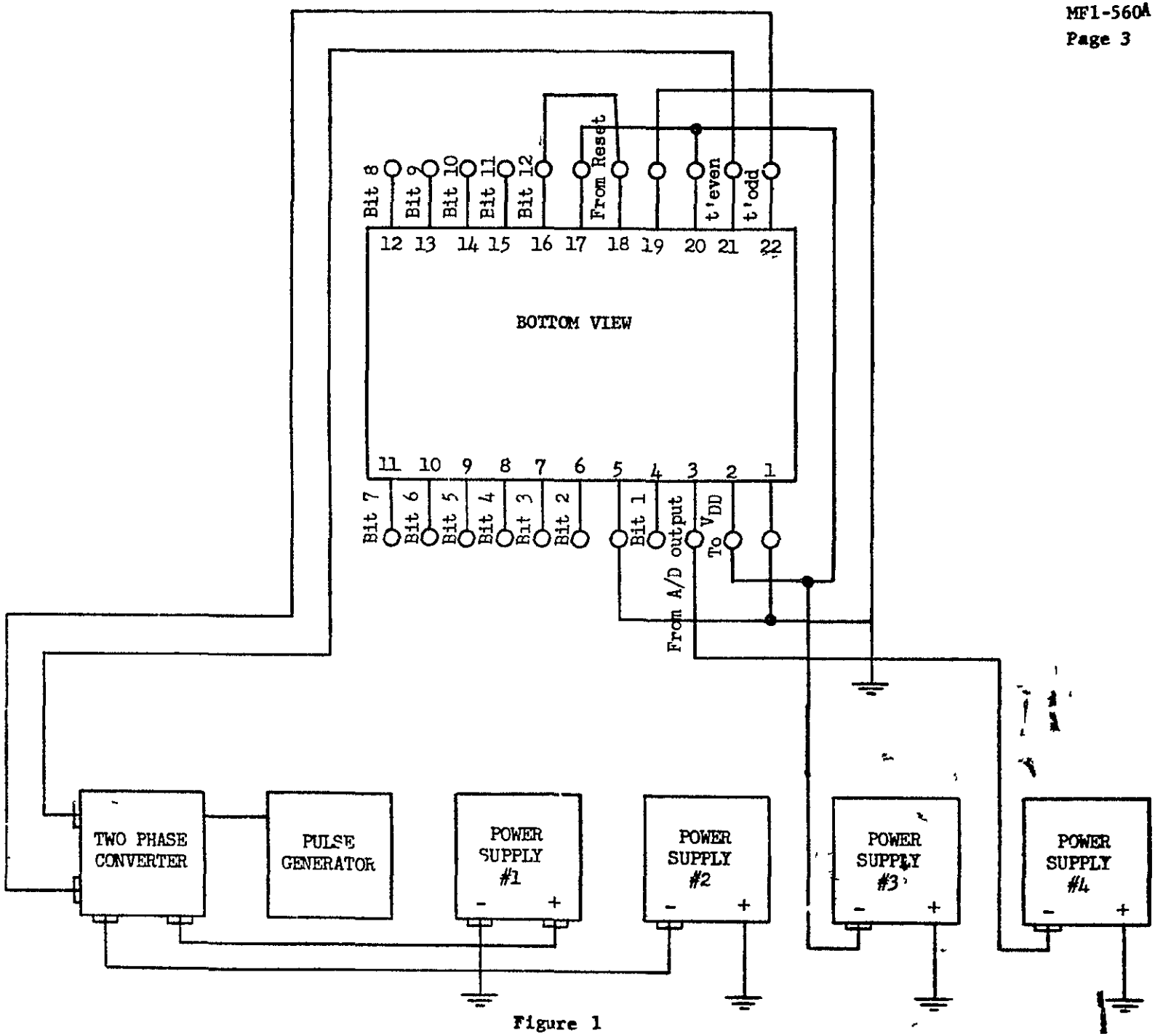

Bit 8
Bit 9
Bit 10
Bit 11
Bit 12
From Reset
t'even
t'odd
12 13 14 15 16 17 18 19 20 21 22
BOTTOM VIEW
11 10 9 8 7 6 5 4 3 2 1
Bit 7
Bit 6
Bit 5
Bit 4
Bit 3
Bit 2
Bit 1
From A/D output
To V_{DD}
TWO PHASE CONVERTER
PULSE GENERATOR
POWER SUPPLY #1
POWER SUPPLY #2
POWER SUPPLY #3
POWER SUPPLY #4
- +

Figure 1

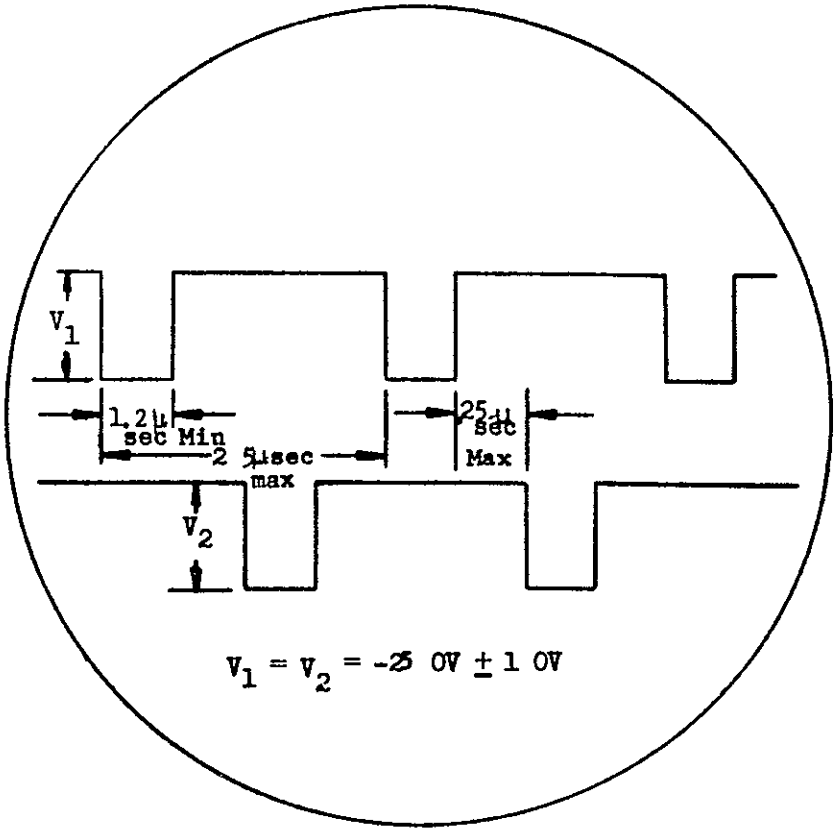
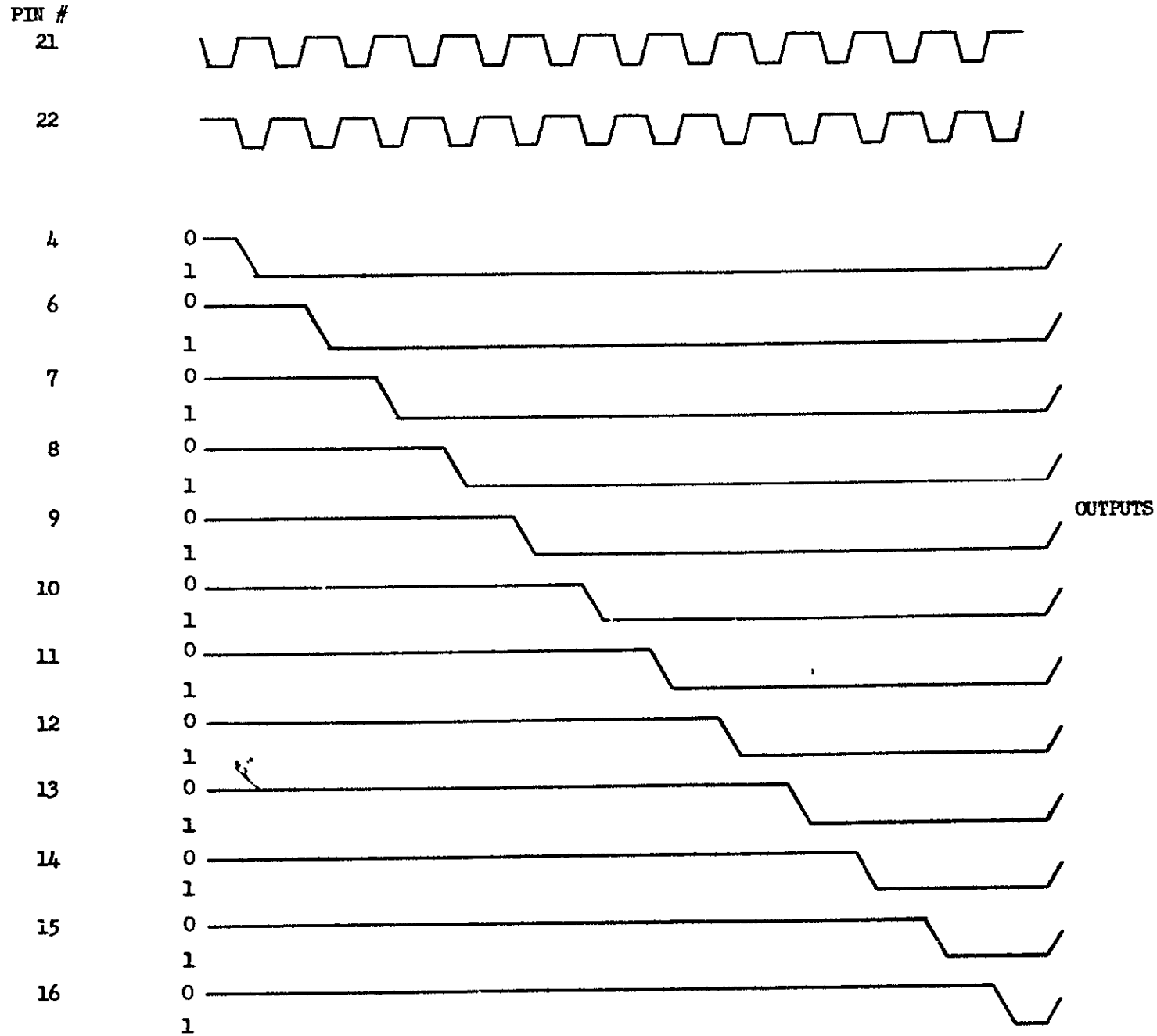


FIGURE 2

FIGURE 3



TRW

MICROELECTRONICS CENTER

MANUFACTURING PROCESS

TITLE

FINAL ACCEPTANCE TEST PLAN
FOR
PHILCO-FORD 16 CHANNEL MOS MULTIPLEXER
PN pL4S16C

DATE. 6-18-70 DOCUMENT NO MF1-557A

SUPERSEDING Original

Issue 2-23-70

Originator

Prepared

K S Morashige
Documentation

Approved

Product Development

Approved

Product Applications

Approved

Department Manager

NOTE This document for MEC use only.

REVISION RECORD

REVISION	DATE	AUTHORIZATION	EFFECTIVE PAGES
	2-23-70	See Title Page	Original Issue, pages 1 through 7
Rev. A	6-18-70		Page 1, Para 2, 2 1 g, eliminate Page 2, 4 2.1, 4 3 3, 4 4 3, add last sentence Page 2, 4.4.3 last sentenced corrected. Page 2, 4.5.5 correct figure Page 2, 4.6 eliminate entirely. Page 3, changed values in Not 2 Page 7, eliminated

MF1-557A

FINAL ACCEPTANCE TEST PLAN
FOR
PHILCO-FORD 16 CHANNEL MOS MULTIPLEXER
PN pL4S16C

1 SCOPE

This document describes the Final Functional Test for the Philco-Ford 16 channel MOS Multiplexer, Philco-Ford PN pL4S16C

2 EQUIPMENT REQUIREMENT

2 1 Test Equipment

a. Lambda LH-124 (or equivalent) power supplies (3 required)

b H-P 3440 Digital Voltmeter with H-P 3440A multi-function plug-in unit

c Oscilloscope, Tektronix 541 or 545 with type N plug-in

d Probes - 7 pF 10 1 (4 required)

e Pulse Generator, Rutherford B7B, or equivalent

f. Signal Generator, Hp - 200CD, or equivalent

3. PREPARATION FOR OPERATION

3 1 Turn on oscilloscope

3 2 Turn on power supplies and adjust them to read as shown in Figure 1

3.3 Turn off power supplies

3.4 Turn on pulse generator and adjust to values shown on Figure 1

4. OPERATIONAL PROCEDURE

4 1 Function Test

4 1 1 Connect device as shown in Figure 1

4.1.2 Turn on power supplies. The presentation on the oscilloscope shall be similar to that shown in Figure 2

4 2 Off State Input Resistance

4.2 1 Connect device as shown in Figure 3 Resistance shall be greater than 10 MΩ Record this reading.

4 3 On State Dynamic Impednace

4.3 1 Connect device as shown in Figure 4

4.3.2 Alternately apply GND -23V to pin 11 until resistance on meter drops significantly.

4 3 3 Read DVM Must be less than 1500 Ω Record this reading

4 4 On State Input Impedance

4 4.1 Leave circuit in the state achieved in 4 3.

4.4 2 Connect the device as shown in Figure 3

4 4 3 Read DVM Must be greater than 1 MΩ Record this reading.

4.5 High and Low Temperature Functional Test

4.5 1 Place device in the environmental chamber and connect as shown in Figure 1

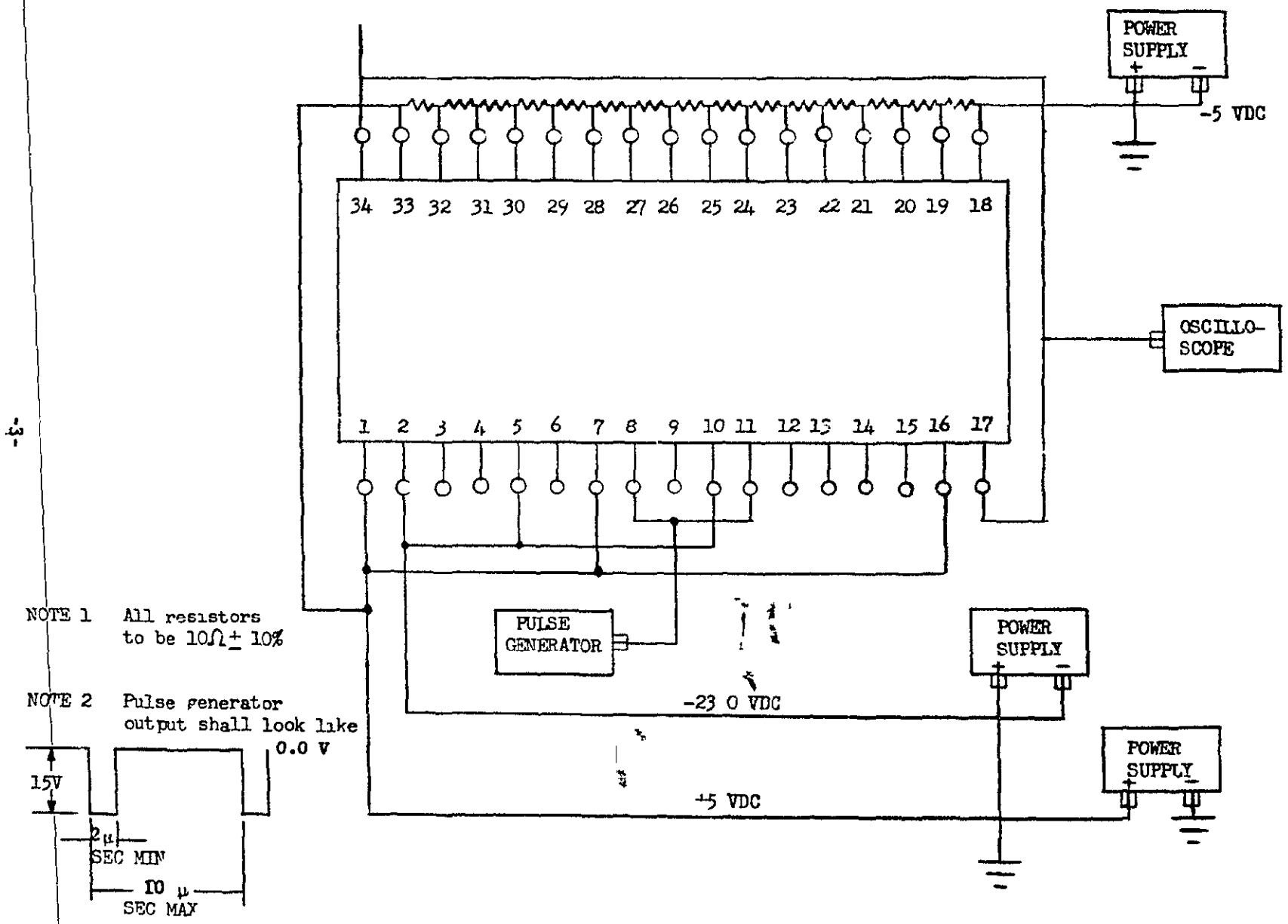
4 5 2 Elevate oven temperature to 100°C ±5°C Allow five (5) minutes for oven to stabilize

4 5 3 Repeat test 4 1

4 5.4 Reduce oven temperature to -20°C ±5°C. Allow five (5) minutes for oven to stabilize

4 5 5 Repeat test 4 1

FIGURE 1



NOTE 1 All resistors to be 10Ω ± 10%

NOTE 2 Pulse generator output shall look like

MR1-557A

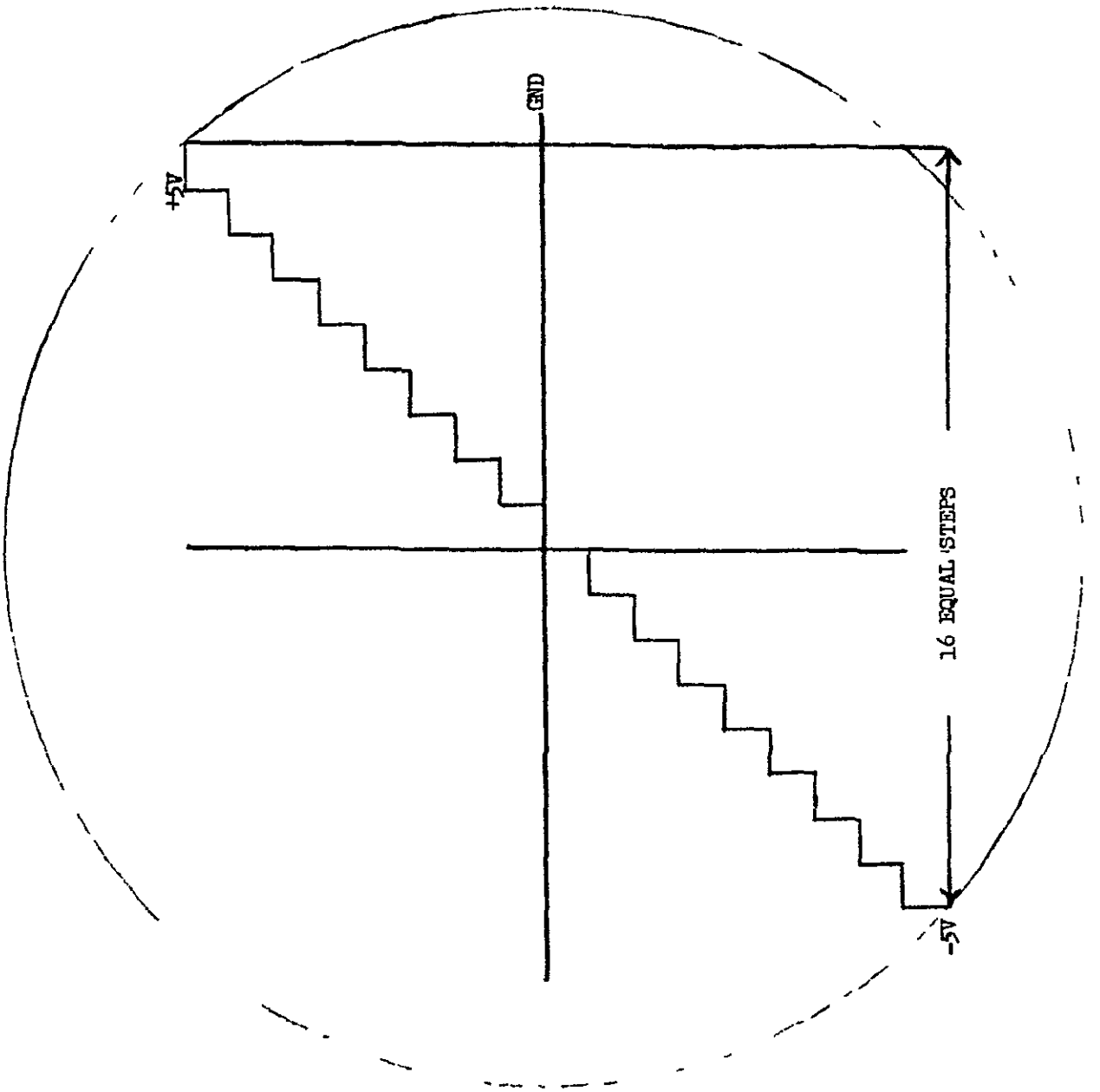


FIGURE 2

FIGURE 3

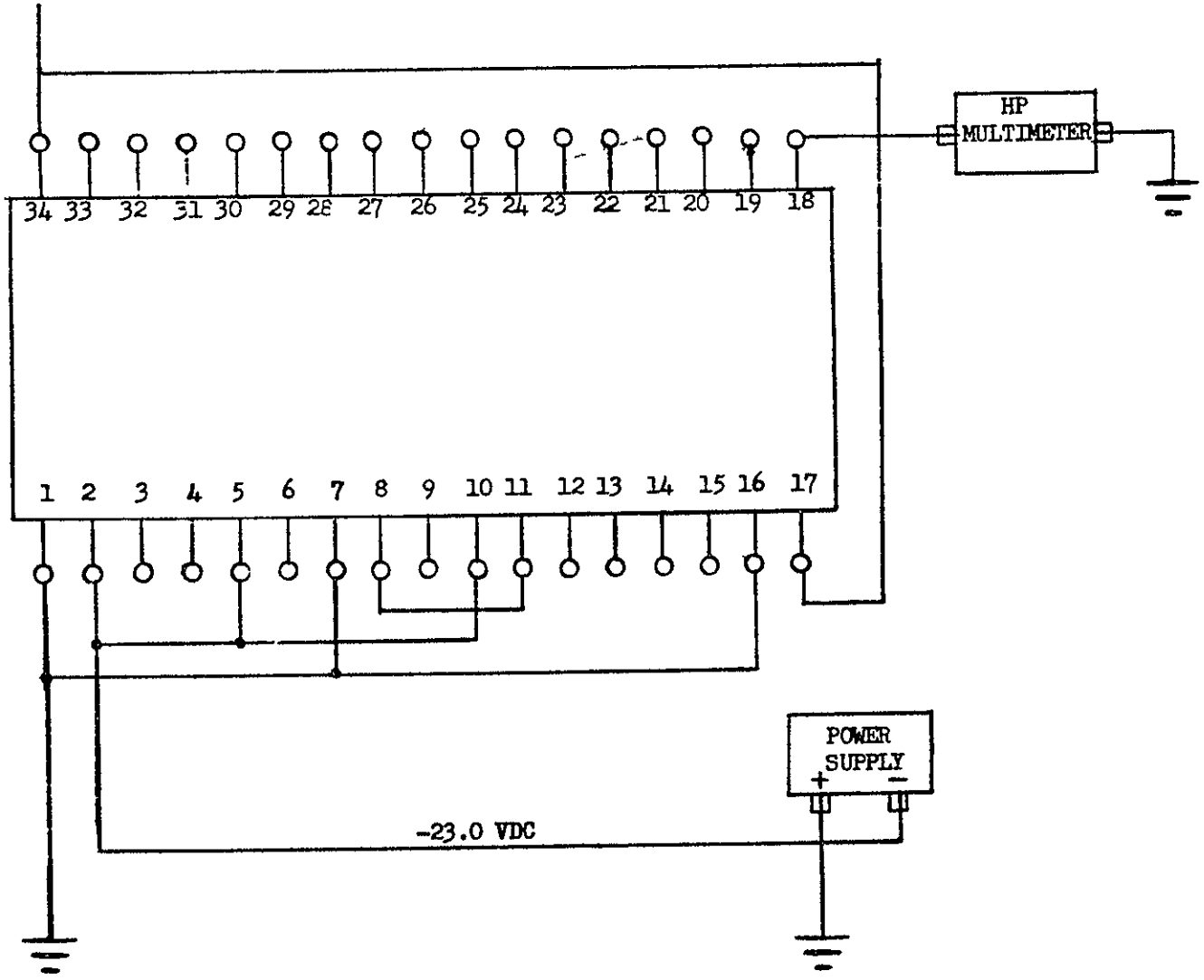
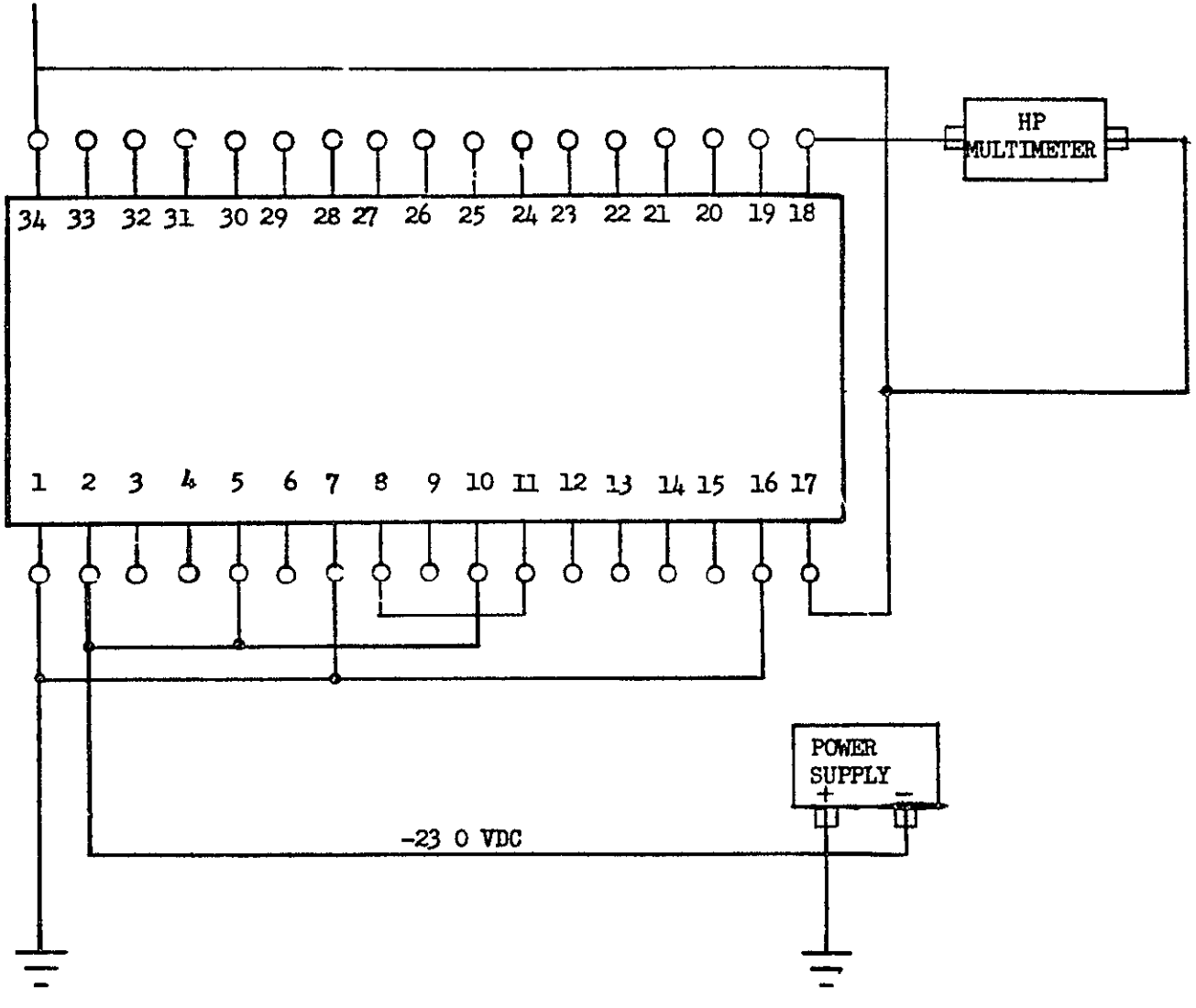

HP
MULTIMETER
34 33 32 31 30 29 28 27 26 25 24 23 22 21 20 19 18
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17
POWER
SUPPLY
+
−
-23.0 VDC

FIGURE 4


HP
MULTIMETER
34 33 32 31 30 29 28 27 26 25 24 23 22 21 20 19 18
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17
POWER
SUPPLY
+
-
-23 0 VDC

APPENDIX 4

BURN-IN DATA

PN PL4S16C MULTIPLEXER AFTER 100 HOUR BURN-IN

	At Room Temperature				100°C Temp	-20°C Temp
S/N	Parameters					
	4 1 2	4 2.1	4 3.3	4 4.3	4 5 3	4 5 5
1	Pass	>10MΩ	841Ω	>10MΩ	Pass	Pass
2	Pass		745Ω		Pass	Pass
3	Pass		2 1K		Pass	Fail
4	Fail					
5	Pass		405Ω		Pass	Pass
6	Pass		972Ω		Pass	Pass
7	Pass		808Ω		Pass	Pass
8	Fail					
9	Pass		609Ω		Fail	Pass
10	Pass		403Ω		Pass	Pass
11	Pass		700Ω		Pass	Pass
12	Pass		1 1K		Pass	Pass
13	Pass	>10MΩ	587Ω	>10MΩ	Pass	Pass

PL4S16C 16-CHANNEL MULTIPLEXER

BEFORE 100 HOUR BURN-IN

S/N	Parameter 4.1.2
1	Pass
2	Pass
3	Pass
4	Pass
5	Pass
6	Pass
7	Pass
8	Pass
9	Pass
10	Pass
11	Pass
12	Pass
13	Pass
14	Fail
15	Fail
16	Fail
17	Fail

NH0007 MOS CLOCK DRIVER, HIGH TEMPERATURE TESTING - 100°C

Serial Number	Parameters 4.1 3	4 1.4	4 2.2	4.2.3	4 3 2	4 4 2
	← Nanoseconds →				← Volts →	
2	75 0	75 0	150	150	-24 4	0.0
3	74 0	75 0	150	140	-24 4	0 0
4	65 0	65.0	150	150	-24 4	0 0
5	85 0	75.0	150	150	-24 5	0.0
6	65 0	65 0	150	150	-24 6	0.0
7	75.0	75	140	150	-24 5	0 0
8	60	60	150	150	-24 5	0.0
9	60	60	150	150	-24 4	0 0
10	60	60	150	150	-24.4	0 0
11	70	70	150	150	-24.5	0 0
12	60	60	125	130	-24 5	0 0
13	60	60	150	150	-24.4	0 0
15	60	60	150	150	-24.4	0 0
17	60	60	150	160	-24 6	0 0
18	60	60	150	150	-24 6	0 0
19	50	50	150	150	-24 4	0 0
20	60	60	150	150	-24.5	0 0
21	50	50	160	160	-24.6	0 0

NH0007 MOS CLOCK DRIVER, LOW TEMPERATURE TESTING - 20°C

Serial Number	Parameters 4 1.3	4.1.4	4 2 2	4 2.3	4 3.2	4 4 2
	← Nanoseconds →				← Volts →	
2	80	80	150	150	-24.0	0 0
3	100	100	150	150	-24.3	0 0
4	80	80	150	150	-24 2	0 0
5	No output----------					
6	80	80	100	100	-24.3	0 0
7	80	80	150	150	-24.0	0 0
8	80	80	170	170	-24.0	0 0
9	80	80	150	150	-24.1	0 0
10	80	80	150	150	-24 3	0 0
11	100	100	150	130	-24 2	0 0
12	100	100	120	125	-24 0	0 0
13	80	80	140	140	-24.0	0 0
15	100	100	100	100	-24 2	0 0
17	80	100	100	100	-24 3	0 0
18	100	80	115	110	-24 4	0.0
19	100	80	110	100	-24 4	0 0
20	80	80	100	100	-24.1	0 0
21	50	60	130	130	-24 3	0 0

NH0007 MOS CLOCK DRIVER, AFTER 100 HOUR BURN-IN

Serial Number	Parameters					
	4 1 3	4 1 4	4 2 2	4 2 3	4 3 2	4 4 2
	Nanoseconds				Volts	
2	60.0	55 0	95 0	95 0	-24 2	+ 030
3	65 0	58 0	93 0	95 0	-24.4	000
4	65 0	58 0	95 0	95 0	-24 3	+ 166
5	65 0	66.0	100.0	100 0	-24 2	000
6	65 0	62 0	80 0	92 0	-24 4	+ 055
7	68 0	65 0	98 0	96 0	-24.2	+ 185
8	54 0	52 0	102 0	100 0	-24 2	+ 188
9	55 0	56 0	96 0	94 0	-24 2	+ 062
10	60.0	56 0	98 0	96 0	-24 3	+ 040
11	58.0	65.0	102 0	100 0	-24 3	+ 199
12	60 0	58 0	92 0	90 0	-24 2	+.144
13	56 0	56 0	100 0	100 0	-24 1	+ 156
14	No Output ----------					
15	56 0	58.0	90 0	92 0	-24 2	+.125
16	No Output----------					
17	58 0	56 0	96 0	94 0	-24 4	+ 155
18	66 0	64 0	86 0	88 0	-24 4	+ 188
19	64 0	66 0	86 0	84 0	-24 3	+ 028
20	64 0	62.0	84 0	86 0	-24 2	+ 101
21	54 0	54 0	92 0	90 0	-24 4	+ 175
22	No Output----------					

NH0007 MOS CLOCK DRIVER, PRE BURN-IN TESTING

Serial Number	Parameter 4 3 (Volts)	Parameter 4 4 (Volts)
1	-23 6	-000
2	-24 2	+ 190
3	-24 4	003
4	-24 4	+ 190
5	-24.2	000
6	-24 2	+ 185
7	-24 2	+.205
8	-24 1	+ 207
9	-24 3	+ 219
10	-24 3	+ 206
11	-24 3	+ 218
12	-24 2	+.152
13	-24.1	+ 179
14	-24 4	+.200
15	-24 2	+ 159
16	-24 9	000
17	-24.4	+ 185
18	-24 4	000
19	-24 3	000
20	-24 1	000
21	-24 4	+ 220
22	-24 3	+ 202
23	- 5 7	000
24	00 0	+.296
25	00 0	_ 274
26	- 3 5	000

SP51C SERIAL TO PARALLEL CONVERTER

AFTER 100 HOURS BURN-IN

AT 100°C

Parameter 4 2 2

Pin #	S/N 1	S/N 2	S/N 5	S/N 6	S/N 8	S/N 10
4	13 13	10 90	13 31	13 12	11 51	13 30
6	13 04	10 86	13 33	13 25	11 52	13 16
7	12 93	11 01	13 32	13 22	11 54	13 33
8	13 01	10 95	13 31	13 19	11 63	13 13
9	12 84	10 89	13 18	12 77	11 60	13 37
10	13 41	11 30	13 68	13 36	11 50	14 01
11	13 33	11 29	13 63	13 37	11 67	13 99
12	13 37	11 28	13 67	13 40	11 81	14 10
13	13 37	11 44	13 62	13 55	11 86	14 07
14	13 19	11 42	13 58	13 33	11 76	13 96
15	13 09	11 30	13 36	13 31	11 72	14 04
16	13 08	11 09	13 27	13 33	11 72	13 72

Pin #	S/N 11	S/N 12	S/N 13	S/N 14	S/N 15
4	12 41	12 98	12 72	11 72	12 01
6	12 46	11 98	12 73	11 69	12 00
7	12 49	12 08	12 78	11 63	11 88
8	12 56	12 17	12 90	11 85	12 03
9	12 42	12 08	12 16	11 81	11 91
10	12 59	12 99	12 72	12 07	11 84
11	12 36	12 94	12 57	11 75	11 81
12	12 37	12 97	12 61	11 82	11 99
13	12 23	13 17	12 57	11 85	11 97
14	12 22	13 23	12 64	11 84	12 08
15	12 11	12 91	12 72	11 71	12 09
16	11 95	12 80	12 64	11 75	12 05

All measurements in Volts

SP51C SERIAL TO PARALLEL CONVERTER AFTER 100 HOURS BURN-IN

AT 100°C TEMPERATURE

Parameter 4 3.2

Pin #	S/N 1	S/N 2	S/N 5	S/N 6	S/N 8	S/N 10
4	0 0	0 0	0 0	0 0	0 0	0 0
6	0.0	0 0	0 0	0 0	0 0	0 0
7	0 0	0 0	0 0	0 0	0 0	0 0
8	0 0	0 0	0 0	0 0	0 0	0 0
9	0 0	0 0	0 0	0 0	0 0	0 0
10	0 0	0 0	0 0	0 0	0 0	0 0
11	0 0	0 0	0 0	0 0	0 0	0 0
12	0 0	0 0	0 0	0 0	0 0	0 0
13	0 0	0 0	0 0	0 0	0 0	0 0
14	0 0	0 0	0 0	0 0	0 0	0 0
15	0 0	0 0	0 0	0 0	0 0	0 0

Pin #	S/N 11	S/N 12	S/N 13	S/N 14	S/N 15
4	0 0	0 0	0 0	0 0	0 0
6	0 0	0 0	0 0	0 0	0 0
7	0 0	0.0	0 0	0 0	0 0
8	0.0	0 0	0 0	0 0	0 0
9	0 0	0 0	0 0	0 0	0 0
10	0 0	0.0	0 0	0 0	0 0
11	0 0	0 0	0 0	0 0	0.0
12	0 0	0 0	0 0	0 0	0 0
13	0 0	0 0	0 0	0 0	0 0
14	0 0	0 0	0 0	0 0	0 0
15	0 0	0 0	0 0	0 0	0 0
16	0 0	0 0	0 0	0 0	0 0

All measurements in Volts

SP51C SERIAL TO PARALLEL CONVERTER AFTER 100 HOURS BURN-IN

AT -20°C TEMPERATURE

Parameter 4 2 2

Pin #	S/N 1	S/N 2	S/N 5	S/N 6	S/N 8	S/N 10
4	13 86	12 09	14 20	14 02	12 50	14 18
6	13 59	11 87	14 08	11 90	12 25	13 87
7	13 52	11 98	13 97	11 85	12 27	13 91
8	13 58	12 02	14 01	11 91	12 30	13 74
9	14 14	12 37	14 43	14 25	13 10	14 63
10	14 08	12 42	14 31	14 01	12 27	14 42
11	13 97	12 27	14 19	13 97	12 36	14 29
12	13 98	12 42	14 34	13 99	12 35	14 52
13	13 89	12 53	14 26	13 96	12 51	14 54
14	13 80	12 41	14 22	14 04	12 54	14 51
15	13 61	12 28	14 00	13 88	12 43	14 38
16	12 95	11 05	11 15	13 15	11 57	13 52

Pin #	S/N 11	S/N 12	S/N 13	S/N 14	S/N 15
4	13 10	13 78	13 55	12 47	12 76
6	13 07	12 60	13 31	12 03	12 29
7	12 91	12 85	13 46	1198	12 21
8	13 05	12 83	13 56	12 08	12 34
9	14 00	13 75	11 78	13 32	13 42
10	13 06	13 63	13 29	12 44	12 26
11	12 82	13 63	13 16	12 18	12 21
12	12 73	13 76	13 19	12 19	12 38
13	12 67	13 92	13 14	12 30	12 31
14	12 62	13 86	13 23	12 14	12 35
15	12 55	13 48	13 23	12 14	12 41
16	11 87	12 65	12 39	11 58	11 87

All measurements in Volts

SP51C SERIAL TO PARALLEL CONVERTER AFTER 100 HOURS BURN-IN

AT -20°C TEMPERATURE

Parameter 4 3 2

Pin #	S/N 1	S/N 2	S/N 5	S/N 6	S/N 8	S/N 10
4	0 0	0 0	0 0	0 0	0 0	0 0
6	0 0	0 0	0 0	0 0	0 0	0 0
7	0 0	0.0	0 0	0 0	0 0	0 0
8	0 0	0 0	0 0	0 0	0 0	0 0
9	0.0	0 0	0 0	0 0	0 0	0 0
10	0.0	0 0	0 0	0 0	0 0	0 0
11	0.0	0 0	0 0	0 0	0 0	0 0
12	0.0	0 0	0 0	0 0	0 0	0 0
13	0.0	0.0	0 0	0 0	0 0	0 0
14	0.0	0.0	0.0	0 0	0 0	0 0
15	0.0	0.0	0.0	0 0	0 0	0 0
16	0 0	0.0	0.0	0 0	0 0	0 0

Pin #	S/N 11	S/N 12	S/N 13	S/N 14	S/N 15
4	0.0	0 0	0 0	0 0	0 0
6	0 0	0 0	0 0	0 0	0 0
7	0.0	0 0	0 0	0 0	0 0
8	0 0	0 0	0 0	0 0	0 0
9	0 0	0 0	0 0	0 0	0 0
10	0 0	0 0	0 0	0 0	0 0
11	0 0	0 0	0 0	0 0	0 0
12	0 0	0 0	0 0	0 0	0 0
13	0 0	0 0	0 0	0 0	0 0
14	0 0	0 0	0 0	0 0	0 0
15	0 0	0 0	0 0	0 0	0 0
16	0 0	0 0	0 0	0 0	0 0

All measurements in Volts

SP51C SERIAL TO PARALLEL CONVERTER AFTER 100 HOURS BURN-IN

S/N	At Room Temperature Parameters		At 100°C Temperature Parameters		At -20°C Temperature Parameters	
	4 1 6	4 1.7	4.1 6	4 1 7	4 1 6	4 1 7
1	OK	OK	OK	OK	OK	OK
2	OK	OK	OK	OK	OK	OK
3	OK	OK	Failed	Failed	Failed	Failed
4	OK	OK	Failed	Failed	Failed	Failed
5	OK	OK	OK	OK	OK	OK
6	OK	OK	OK	OK	OK	OK
7	OK	OK	Failed	Failed	Failed	Failed
8	OK	OK	OK	OK	OK	OK
9	OK	OK	Failed	Failed	Failed	Failed
10	OK	OK	OK	OK	OK	OK
11	OK	OK	OK	OK	OK	OK
12	OK	OK	OK	OK	OK	OK
13	OK	OK	OK	OK	OK	OK
14	OK	OK	OK	OK	OK	OK
15	OK	OK	OK	OK	OK	OK

SP51C SERIAL TO PARALLEL CONVERTER AFTER 100 HOURS BURN-IN
AT ROOM TEMPERATURE

Parameter 4 2 2

Pin #	S/N 1	S/N 2	S/N 3	S/N 4	S/N 5	S/N 6	S/N 7	S/N 8
4	13.95	12.03	11 89	11 28	14 31	14 15	11 93	12.59
6	13 72	11 92	11 71	11 21	14 24	14 07	11 64	12 43
7	13 65	12.00	11 80	11 19	14 13	14 03	11.62	12 46
8	13 69	12.03	11 80	11.22	14 17	14 07	11 64	12 48
9	13.92	12 09	12 05	11 88	14 21	14.03	11.55	12 86
10	14.18	12 40	11 52	11.42	14 45	14 18	11 13	12 44
11	14 09	12 27	11.61	11 25	14 35	14 14	11 06	12 53
12	14.12	12.41	11.70	11 39	14.49	14 16	11 24	12.53
13	14 03	12 53	11 66	11 66	14 42	14.14	11 33	12 68
14	13.94	12 41	11.56	11.72	14.37	14 21	11 49	12 72
15	13 78	12.28	11 51	11 59	14.15	14 06	11 48	12 61
16	12 94	10.99	10.49	10.55	13 15	13 21	10 37	11 64

Pin #	S/N 9	S/N 10	S/N 11	S/N 12	S/N 13	S/N 14	S/N 15
4	12.08	14.32	12.70	13.83	13.73	12 65	12 97
6	11.89	14 06	13 32	12 69	13 54	12 42	12 65
7	11 97	14 10	13 21	12 91	13 69	12 34	12 61
8	12 03	13 93	13 33	12 89	13 79	12 47	12 70
9	12 43	14 47	13 75	13 46	11 88	13 16	13 26
10	11 70	14 61	13 36	13 74	13 51	12 77	12 56
11	11 59	14 42	13 12	13 71	13 37	12 53	12 55
12	11 77	14 74	12 97	14 03	13 36	12 60	12 72
13	11.77	14 74	12 97	14 03	13 36	12 60	12 72
14	11 87	14 71	12 94	13 98	13 48	12 47	12 75
15	11 72	14.57	12 78	13 58	13 47	12.45	12.81
16	10 86	13.61	11.87	12 64	12 46	11.65	11.92

SP51C SERIAL TO PARALLEL CONVERTER AFTER 100 HOURS BURN-IN

AT ROOM TEMPERATURE

Parameter 4 3 2

Pin #	S/N 1	S/N 2	S/N 3	S/N 4	S/N 5	S/N 6	S/N 7	S/N 8
4	0 0	0 0	0 0	0.0	0 0	0 0	0 0	0 0
6	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0
7	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0
8	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0
9	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0
10	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0
11	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0
12	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0
13	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0
14	0 0	0 0	0 0	0 0	0 0	0 0	0 0	0 0
15	0.0	0 0	0 0	0 0	0 0	0 0	0 0	0 0
16	0.0	0 0	0 0	0 0	0 0	0 0	0 0	0 0

Pin #	S/N 9	S/N 10	S/N 11	S/N 12	S/N 13	S/N 14	S/N 15
4	0 0	0 0	0 0	0 0	0 0	0 0	0.0
6	0 0	0 0	0 0	0 0	0 0	0 0	0 0
7	0 0	0.0	0 0	0 0	0 0	0 0	0 0
8	0 0	0 0	0 0	0 0	0 0	0 0	0 0
9	0 0	0 0	0 0	0 0	0 0	0 0	0 0
10	0 0	0 0	0 0	0 0	0 0	0 0	0 0
11	0 0	0 0	0 0	0.0	0 0	0 0	0 0
12	0 0	0 0	0 0	0 0	0 0	0 0	0 0
13	0 0	0 0	0 0	0 0	0 0	0 0	0 0
14	0 0	0 0	0 0	0 0	0 0	0 0	0 0
15	0 0	0 0	0 0	0 0	0 0	0 0	0 0
16	0 0	0 0	0 0	0 0	0 0	0 0	0 0