STUDY OF SEMICONDUCTOR HETEROJUNCTIONS

OF ZnSe, GaAs and Ge

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ABSTRACT

The fabrication problems and device characteristics of ZnSe-GaAs and Ge-GaAs heterojunctions are being studied. The nZnSe-pGaAs structure, in particular, is being examined because of its potential in high-temperature solar cells.

Scanning-beam electron microscopy and transmission electron microscopy studies show that the perfection of the GaAs substrate and its preparation before growth of the ZnSe are very important in determining the transistor behavior observed. Substitution of a Zn diffusion slow-cool process after growth, for the quench process used earlier, has resulted in current gain from (100)GaAs transistors, which is an orientation that did not previously show gain. Various ZnSe-GaAs structures were pulsed to high current densities in a search for light-emission, but no light output was detected.

Success was achieved in the growth of single-crystal ZnS on (111)GaP by the HCl close-spaced transport process. This is a lattice-match heterojunction structure on which almost no previous work has been reported. Further studies of the pair are planned, including electrical and electro-optical characteristics, if the ZnS resistivity can be lowered. Attempts to grow ZnTe upon GaSb were frustrated by substrate-etching, probably caused by the Te in the system.

During the report period, recharging of the iodine system for the growth of pGe on GaAs at low temperatures, led to a considerable amount of reqorking of the system. This is now complete, and the system is now in a state for further growth runs.

1. INTRODUCTION

The properties of semiconductor heterojunctions have been under study for some years now. In this field, an event of major practical importance has been the development recently, by Bell Labs, RCA and in Russia, of heterojunction injection lasers with threshold current densities for 300°K laser action of less than a quarter of the current densities required of conventional GaAs lasers. The operating lifetime and reliability of GaAs lasers has been profoundly altered by this recent development. GaAlAs heterojunction layers are used to provide "confinement" action in the laser.

The work under the present contract is not involved directly with injection lasers, but we are concerned with discovering as much as possible about the electrical and electro-optical properties of heterojunction interfaces. Conceptually there are significant advantages to be hoped for in working towards the perfection of heterojunction properties. For instance the efficiency expected of a heterojunction nZnSe-pGaAs solar cell is larger than that of Si solar cells at 300°K, in the ratio of 13.3 to 11.9% for a typical calculation. Moreover, at higher temperatures, say 500°K, the potential advantage of the heterojunction becomes very pronounced because the energy gap of GaAs is greater than that of Si. For example a Si cell may drop to below 4% in efficiency at 500°K whereas the efficiency for GaAs-based structures remains high.

In a comparative study of the theoretical properties of nZnSe-pGaAs and nGaAs-pGaAs solar cells the heterojunction structure is higher in efficiency. This is because the front face of a GaAs cell must be made very thin, otherwise the sharp photon absorption edge and the high surface-recombination cause considerable carrier loss. We have suggested that a heteroface structure, such as nZnSe-nGaAs-pGaAs could reduce the surface recombination effect and improve GaAs solar cell performance. Built-in fields may also be added to all of these structures, within the limitations of the fabricational procedures that have been developed, to improve collection efficiency.

In addition to the solar cell potential the heterojunction structures are also of interest as sensors of optical signals, and possibly as solid-state infra-red image up-converters.

At present most heterojunction structures are limited in performance by recombination at the interface between the two semiconductors. The effect is best studied by the fabrication of heterojunction transistors since the gain of such structures provides information on how the current divides between the injected and recombination components. Discussion of heterojunction transistor behavior therefore is an extensive part of this quarterly report. Good progress has been made in understanding the electrical properties of ZnSe/GaAs structures in relation to the details of fabrication technology. However, there is much still to be learned here, and we have not yet obtained the specimens needed for optical studies.

A highlight of the work during the quarter has been discovery that our HCl transport system is capable of growing good ZnS layers on single-crystal GaP substrates. This is a lattice-match situation and therefore a potentially worthwhile heterojunction. However, we know of only one previous reference to such growths and this does not examine the electrical or electro-optical properties of the pair. We plan to begin such studies in the next few months to determine information about injection and collection properties of the pair. ZnS is of course well known for its electroluminescent properties, and GaP is also a light emitter with injection under suitable doping conditions.

2. EXAMINATION OF ZnSe/GaAs TRANSISTOR INTERFACES

We have continued to look for some difference at (111) and (100) interfaces of identically fabricated ZnSe-GaAs transistors that might explain the failure of (100) transistors to show gain while their identical (111) counterparts show current gains as high as 35. It is believed that dislocations generated at the ZnSe-GaAs interface are responsible for this behavior. Dislocations at the interface can arise from lattice mismatch (misfit dislocations), Zn diffusion (misfit dislocations), and differences in thermal coefficient of expansion between ZnSe and GaAs (slip). Slip on (111) planes can become a serious problem above 500°C where both growth and thermal quenching occur. The major effects of dislocations at the interface are an increase in defect (non-injecting) current and a loss in gain. Dislocations penetrating into the GaAs base region could seriously reduce lifetime and gain. If greater densities of dislocations appear at (100) interfaces, than at

(111) interfaces, a possible explanation of the orientation effect would exist.

Several identically-fabricated (from the same GaAs boule) (111) and (100) ZnSe-GaAs transistors were examined on the scanning beam electron microscope (SBEM) and the transmission electron microscope (TEM) at Westinghouse Research Laboratories. The SBEM was operated mostly in the charge-collection mode, but the secondary emission mode (optical) was frequently used to check the difference between it and the conduction mode. The secondary emission mode can not see small electrical perturbations such as dislocations and typically yields a picture resembling that of an optical microscope except that the depth of field is enormous. The charge-collection mode is capable of seeing only electrically active dislocations and can resolve them into individual lines provided they are more than 300 Å apart. Thus, the maximum resolving power of the SBEM is about $10^5 cm^{-2}$ dislocations. The TEM can easily resolve 10^7-$10^8 cm^{-2}$ dislocations (electrically active and inactive) and is a necessary tool for uncovering high densities of dislocations. For this examination the TEM was operated under two-beam bright field conditions.

Typical devices were mounted on headers and examined on the SBEM. Then the same devices were removed from the headers and prepared for the TEM. TEM specimen preparation consisted of removing the ZnSe and thinning from the collector back-side with a bromine-methanol jet etch. Only one set of devices was successfully thinned because etching of {111} faces is extremely difficult and frequently results in cracked or punched through specimens. For run TR-21 a (111)A and (100) ZnSe-GaAs interface pair was successfully thinned, with the (111)B interface cracking. However, TEM examination continued on the two successful interfaces.

Run TR-21 consisted of growing a 3 μm layer of ZnSe upon (111)B and (100) n type GaAs and a 1.5 μm layer of ZnSe upon (111)A n type GaAs all cut from the same boule of "zero" dislocation density GaAs. This material has shown no more than $10^2 cm^{-2}$ dislocations after dislocation etching. The growth rate upon (111)B and (100) GaAs surfaces is twice that upon (111)A GaAs surfaces and accounts for the difference in ZnSe grown layer thickness. All three orientations were then simultaneously subjected to the Zn diffusion-quench step of base formation (650°C, 5 min.). The characteristics of these transistors are given in Table I.

Table I Electrical Characteristics of ZnSe - GaAs Transistors

TR-21 processed identically. Zn diffusion at 650° C for 5 minutes.

Orientation	(111)A	(111)B	(100)
ZnSe thickness, μm	1.5	2.5	2.5
Base Width, μm	.75	.25	.25
Coll-Base Rev. breakdown voltage, volts	18	8	12
Emit-Base Rev. breakdown voltage, volts	15	10	10
ZnSe resistivity, ohm-cm	10^5	5×10^3	10^4
h_{fe}	2-5	None	None

The low gain of the (111)A transistor, can be explained by its large basewidth which is a result of higher Zn concentration and penetration allowed by its thinner emitter region. The (100) structure shows the type of behavior previously seen, namely no transistor gain.

The (111)B transistor ought to have a gain of at least 5. However, its abnormally low emitter-base and collector-base reverse breakdown voltages indicate the possibility of abnormally high dislocation densities in and around the base region. Note that the (100) transistor, which never works, also has lower reverse breakdown voltages than the (111) Ga transistor. This is the first time that a (111)As transistor has not had current gain, and this anomalous behavior suggests that SBEM and TEM should show dislocations present. Figs. 1, 2 and 3 show SBEM charge-collection micrographs of the transistors. Secondary emission micrographs were identical to optical microscope photographs and are not shown. The charge-collection modes uses either the emitter-base or base-collector open-circuit voltage to modulate the intensity of a CRT tube and is sensitive to electrical perturbations a diffusion length (1-2 μm) on either side of the junctions. Grids of dislocation traces running at 60° to each other are seen in the base of the (111)As transistor whereas the (111)Ga transistor shows no observable electrically active dislocations. Dislocations were not defined well enough to be resolved at higher magnification. This is the first time that well ordered dislocations were seen in (111) transistors (and the first time that one did not work). Some dark blotches were seen in parts of other (111) transistor bases under high magnification but were believed to be inclusions or precipitates. These same blotches were also seen with various densities on (100) transistors. The fact that the dislocations remain after ZnSe removal indicates that plastic deformation of the GaAs has occurred. The penetration of the dislocations from the interface into the collector or back into the ZnSe could not be definitely ascertained since the beam could not be made to pass through the collector into the base or through the base into the ZnSe. By appropriate grounding of terminals and lowered beam voltages, it was concluded that dislocations did not extend very far into the ZnSe. X-ray topographs of ZnSe layers indicate excessive strain. Consequently a great deal of strain may be in the thin layer of ZnSe with little relief by dislocations.

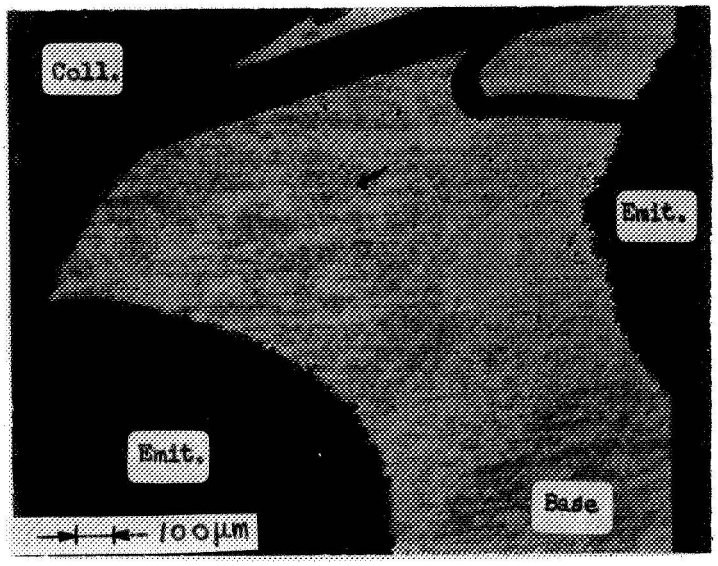


Fig. 1 CONDUCTION mode SBEM micrograph (25KV) of the base region of TR-21-111-As.
Emitter and collector grounded (the transistor has two emitter regions). Modulating voltage is from base to collector (emitter). Two grids of dislocation lines at 60° to each other are barely evident in the base region.

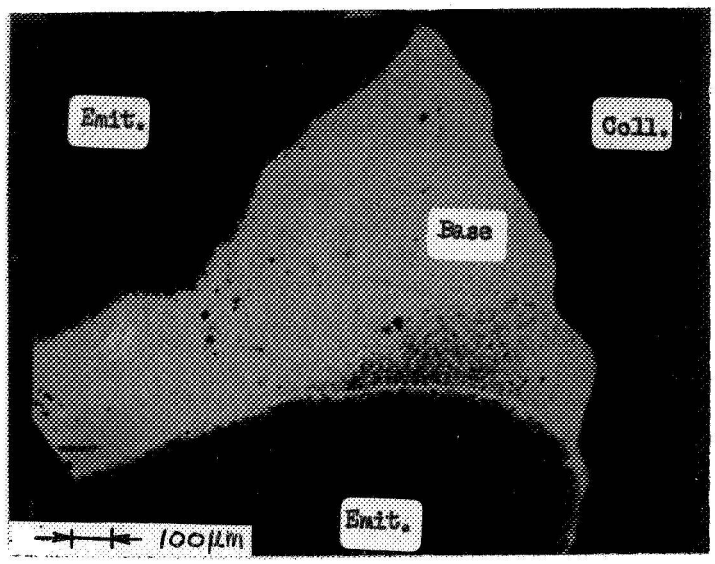


Fig. 2 Conduction mode SBEM micrograph (25KV) of the Base region of TR-21-111-Ga. Emitter and collector grounded. Modulating voltage is from base to collector (emitter). No dislocations are observed.

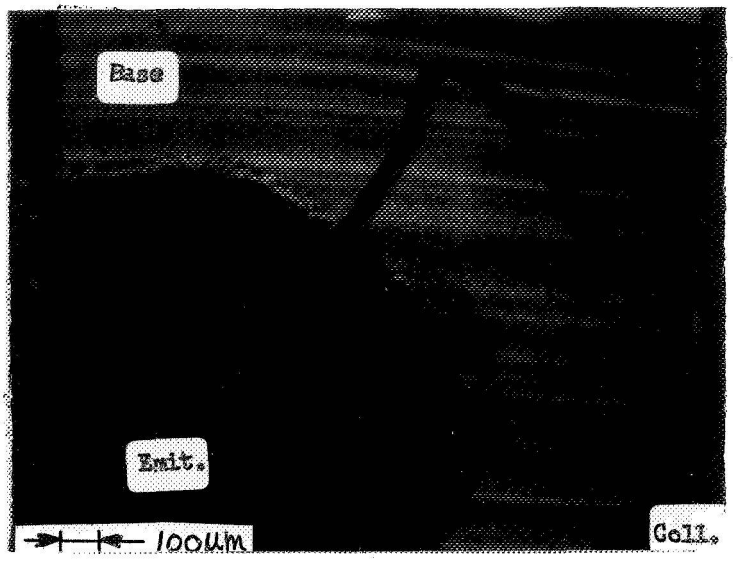


Fig. 3 Conduction mode SBEM micrograph (25KV) of the base region of Tr-21-100. Emitter and collector grounded. Modulation voltage is from base to collector (emitter). Electrically active growth striations are observed.

The (100) transistor (Fig. 3) shows nothing that resembles traces of dislocations. The bands that are seen in the base region (and do not penetrate into the ZnSe) are believed to be growth striations. They are not seen optically or by the SBEM secondary emission mode and are therefore considered to be electrically active. These striations are seen in all (100) transistors by both SBEM and etching techniques (to be discussed) but are never present in (111) transistors cut from the same boule or any other boule. They are present in all (100) substrates before growth,are not present in (111) substrates, cannot be removed chemically, and are probably a result of the GaAs manufacture. Many such growth situations have been reported in the literature, especially with Te doped boat-grown and melt-pulled GaAs. The crystals used in this study were all (111) Czochralski grown and doped with Sn. For this type of growth, striations arise as a result of cyclic temperature fluctuations during growth. If the pull direction is (111), then striations reside in (111) planes and intersect (100) planes as light and dark bands. These striations are known to increase the lasing current threshold of GaAs p-n junction lasers because they contain precipitates which increase light absorption.

Since the striations appear to be electrically active, it is possible that they are influencing (100) transistor behavior. These striations are probably also active on (111) planes but are unobservable by SBEM techniques since they lie uniformly in the plane of interest. The failure of the (111)As transistor may be due to growth on a particularly bad (111) striation plane. Bad in this sense might mean a high density of precipitates which might effect the lattice constant or thermal coefficient of expansion enough to warrant the formation of an abnormally high dislocation density after temperature cycling. If a good (111) striation plane is chosen for growth, then the transistor works normally. Although these arguments are tentative, they are the only explanation of the orientation effect in ZnSe-GaAs heterojunction transistors that we can offer at the present time.

Figs. 4 and 5 show TEM micrographs of TR-21 for (111)A and (100) orientations. Unfortunately the interesting transistor, TR-21-111As, cracked while thinning. It was hoped that the dislocations seen in this transistor by the SBEM (Fig. 1) could be resolved for orientation and density. Edge dislocations in <110> and <112> lines are seen in the (111)A transistor and are typical of both misfit and slip viewed in the

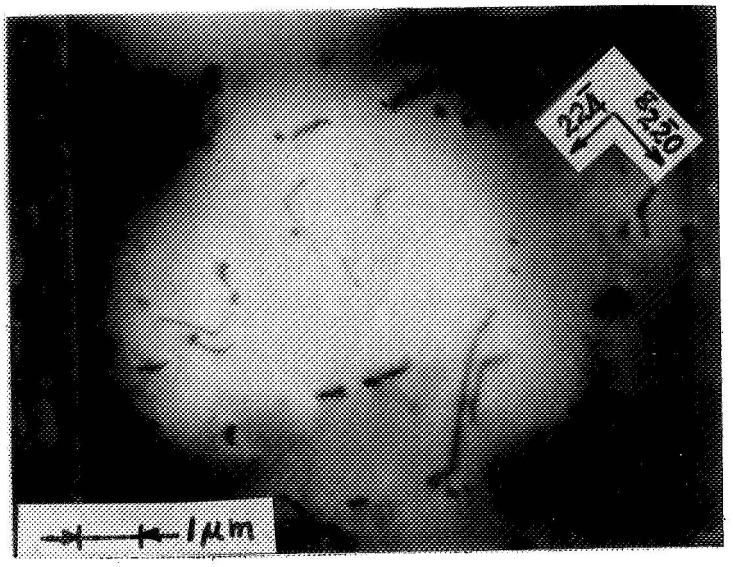


Fig. 4 TEM micrograph of TR-21-111 Ga. 80 KV Beam perpendicular to foil. Edge dislocations running in <110> and <112> directions are observed.

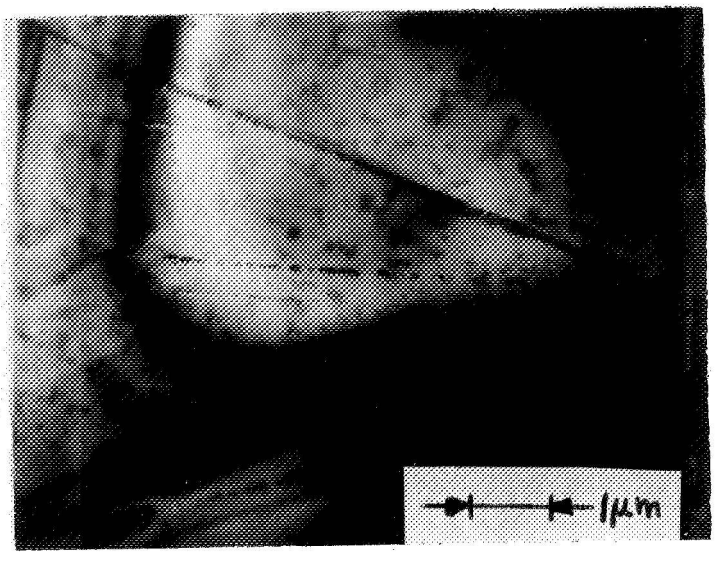


Fig. 5 TEM micrograph of TR-21-100. 80 KV Beam perpendicular to foil. Only scratches are observed.

(111) plane for FCC crystals. The Burgers vector direction was not determined. These were definite edge dislocations since (1) they could be made to go in and out of contrast, and (2) they did not go out of contrast entirely. Their density, although not uniform at this magnification, was averaged to be about $2 - 5 \times 10^4$ cm^{-2} which is lower than previous dislocation density studies on transistor bases using chemical etches. A simple calculation of misfit dislocation spacing in natural ZnSe-GaAs interfaces gives a value of about 0.3 μm indicating that misfit dislocations would be much more closely spaced than any dislocation seen in Fig. 4. However, any slight increase in the lattice constants difference could increase the dislocation spacing by at least an order of magnitude. At this point it is not clear whether the dislocation seen in Fig. 4 are misfit, slip, or even inclined dislocations that bend out of the foil plane. There is no guarantee that they are electrically active since none were seen by SBEM techniques.

Fig. 5 shows a TEM micrograph of the (100) oriented transistor TR-21-100. Here nothing that resembled dislocations was seen. Only straight lines were observed that showed no contrast variation as the sample was tipped. For this reason these lines were believed to be scratches. Also observed are small spots which might be precipitates but do not show any strain pattern. These spots are not observed in the (111)A transistor (Fig. 4). The presence of the scratches was a surprise and suggested some deficiency in our final sample preparation technique. Accordingly, a study of these techniques was undertaken. This was done by subjecting as-polished and final etched (100) and (111) n-type GaAs transistor substrates (cut from the same boule) to the GaAs AB dislocation etch (2 ml H_2O, 8 mg $AgNO_3$, 1g CrO_3, 1 ml HF 75°C). This etch readily reveals scratches and dislocations.

As-polished samples were hand lapped to 1 μm with Al_2O_3 grit and then polished with a 1:3 chlorox: H_2O solution on a pellon pad to remove 1-2 mils of material. Surfaces resulting from this treatment are optically flat and smooth with no scratches. As a final etch before growth (100) and (111)As samples are etched in an H_2SO_4:H_2O_2:H_2O (5:1:1) solution at 90°C until 10 μm of material is removed. (111)A samples are etched in a chlorox:water (1:3, 1:2) solution at 70°-90°C.

Figs. 6 and 7 show the results of dislocation etching (111)As and (100) surfaces after chlorox polishing but before peroxide etching. The (111) surface is badly scratched while the (100) surface shows pits which could be the traces of scratches farther below the surface. Etch pit counts are 10^4-10^5 cm^{-2} which is 2-3 orders of magnitude higher than before polishing. After these samples are repolished, treated with the sulfuric-peroxide final etch, and resubjected to the dislocation etch, the resulting surfaces are much improved. Figs. 8 and 9 give the results. The (111) surface is featureless while the 100 surface shows some spiral loops which may be helical dislocations. Note that the dislocation etch reveals the familiar growth striations seen on (100) surfaces. From these results we conclude that our polishing technique is capable of producing scratch-free surfaces. However, this does not exclude the possibility that the scratches seen in Fig. 5 were due to poor technique. In the future we will be extremely careful in our final sample preparation techniques.

Results from the SBEM and TEM studies have yielded the following observations.

(1) Growth striations may exist in the GaAs material we used for ZnSe-GaAs transistors. They are electrically active and appear to be on (111) planes. They probably contribute to the gain-orientation effect that we observe.

(2) (111) transistors with abnormally high electrically active dislocation densities show no gain indicating a direct relationship between dislocations and transistor performance.

(3) Dislocation densities as high as 5×10^4 cm^{-2} can be tolerated in the base region of normally operating (111) transistors. It is not certain whether these dislocations are electrically active.

(4) At present it is not certain whether slip or misfit is responsible for the observed dislocations.

(5) The ZnSe emitter layer is under considerable strain and does not show dislocations when viewed with the SBEM.

(6) Dislocations are not observed for (100) transistors by either SBEM or TEM techniques.

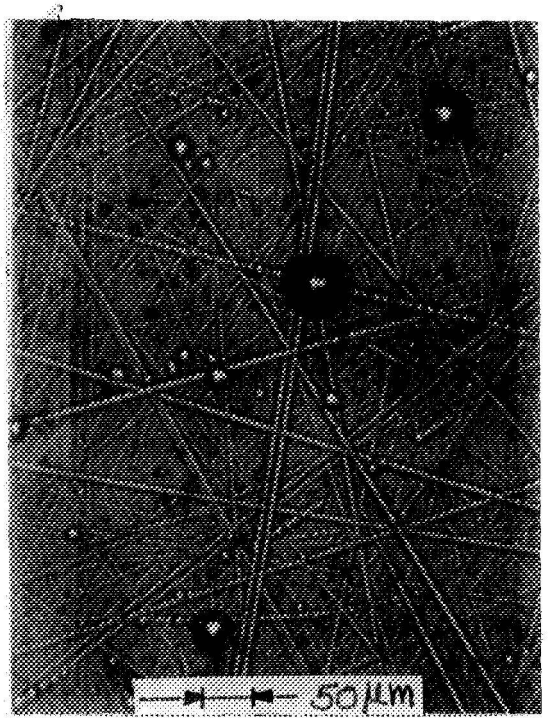


Fig. 6 Chlorox "As-polished" (111)B Bulk GaAs Surface after AB dislocation etch.

Fig. 7 Chlorox "As-polished" (100) Bulk GaAs Surface after AB dislocation etch.

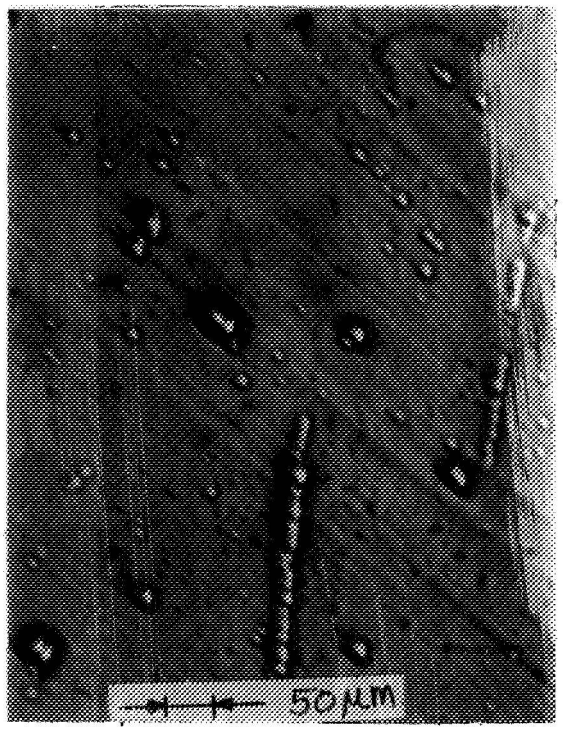


Fig. 8 Surface of Fig. 6 by repolishing in chlorox, etching in H_2SO_4-H_2O_2-H_2O etch and treating with AB dislocation etch.

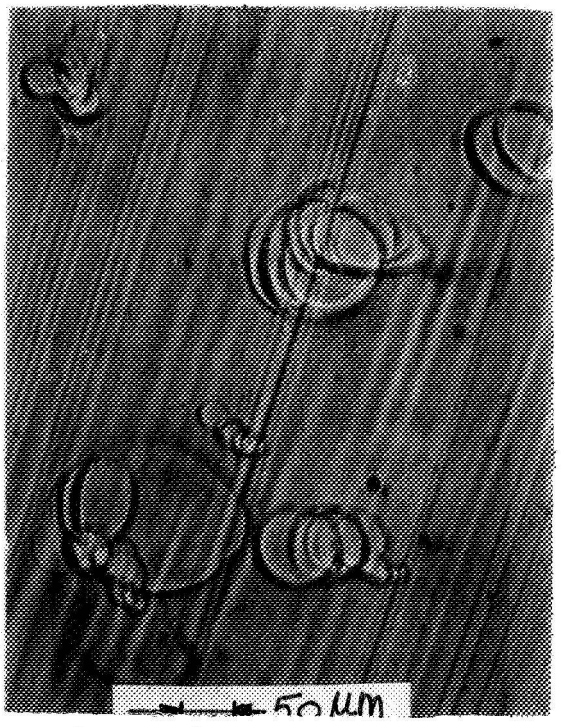


Fig. 9 Surface of Fig. 7 by repolishing in chlorox, etching in H_2SO_4-H_2O_2-H_2O etch, and treating with AB dislocation etch.

We plan to continue a limited number of experiments along the lines presented to gather more information on the orientation effect

3. ACHIEVEMENT OF GAIN IN (100) TRANSISTORS

As a result of the previous studies we considered changes in our fabrication technique that might reduce ZnSe-GaAs interface dislocations, since these dislocations appear to be the source of low gain in transistors. In particular we replaced the Zn diffusion-quenching step with a Zn vapor treatment during cool-down in the growth system. This treatment involves no rapid temperature variations and has previously been used to reduce grown ZnSe resistivity to 10^3 ohm-cm in ZnSe-Ge devices.

In this method a quartz boat charged with Zn is placed in the growth tube so that it is not attacked by HCl during ZnSe growth.As the ZnSe grown layer is cooling down after growth, the quartz boat, previously unheated, is slowly heated up to 700-800°C so that it reaches its maximum temperature when the ZnSe has cooled to 580-600°C. H_2 is passed over the hot zinc so that its vapor is swept over the ZnSe until the growth has cooled to 430°C. Then both the Zn and ZnSe are allowed to free cool to room temperature. At the higher temperatures Zn diffusion in GaAs is rapid enough to form a base region in the GaAs, whereas at lower temperatures the presence of Zn prevents self-compensation by Zn vacancies in ZnSe. A cooling rate of 3°C/min. (faster than used in ZnSe/Ge device fabrication) is necessary to achieve small base widths with large concentration gradients. The faster cooling rate has not been found to be injurious to device properties, does not crack 3 μm grown layers, and makes process control somewhat easier. The entire process is quite tedious. Cooling too slowly or starting to diffuse at too high a temperature can easily produce basewidths that are too large. Because the technique is almost an art, it was not tried at an earlier stage. The base diffusion times and temperatures obtained from previously quenched transistors were an invaluable aid in determining the time-temperature schedule for the new process. It is almost impossible to assess the effective diffusion times and temperatures in this process. Base region carrier concentration profiles will have to be taken to properly evaluate the devices made by this process. Then an "effective" diffusion time and temperature may be deduced.

Amazingly successful results were obtained using this new process. The first devices attempted, TR-23, were fabricated from scrap GaAs, (111)As oriented, and Te doped to 2×10^{16} cm^{-3}. The dislocation density of this material before fabrication was of the order of 5×10^{5} cm^{-2}. Although inferior from a standpoint of initial defects and Te doping, this material produced some transistors with common-emitter current gains as high as 150 (with correspondingly high ZnSe resistivity of 5×10^{5} Ω-cm). Most transistors from this run were typified by the TR-23 data presented in Table II and Fig. 10. Emitter current density was limited by high ZnSe resistivity so that maximum gain was typically 50-70. Note that at $J_E = 3$ Amp/cm^2 the gain begins to increase rapidly. Again the gain varies as a fractional power of the emitter current which we have found to be common in heterojunction transistors.

Initial success prompted a simultaneous growth on (111)As and (100) "zero" dislocation density samples cut from a single boule. The Zn diffusion-slow-cool process was used. Although the base width was larger than expected (.7 μm), both orientations showed normal transistor action with the (100) transistor having a slight edge in gain possibly due to its higher ZnSe resistivity. The results for these transistors, TR-24, are presented in Table II and Fig. 10-13. Fig. 11 shows the emitter-base characteristic typical of both orientations. Fig. 12 compares base-collector characteristics for both orientations. In all transistors from this run (100) orientations produced better reverse base-collector characteristics than did (111) orientation. The reason for this is not understood. Fig. 13 shows the common-emitter characteristics. The looping in the flat portion of the curves is due to high ZnSe resistivity hysteresis (traps, defects, etc.) and can be eliminated by d-c plotting. Fig. 10 shows a similar injection behavior for both orientations.

It now appears that orientation effects on injection can be eliminated by slow cooling, and that quenching is a harmful processing technique. Future transistors will be made by the slow cooling process. Thus some progress has been made toward explaining and reducing orientation effects on gain in ZnSe-GaAs transistors.

Table II Comparison of TR-23 and TR-24 Transistors

Transistor	Orientation	ZnSe Thickness, μm	ZnSe Resistivity, ohm-cm	Basewidth μm	h_{fe} (at I_E=1A/cm^2)	h_{fe} (at I_E=10A/cm^2)
TR-23	(111)As	2.5	5×10^4	0.2	32	-
TR-24	(111)As	2.5	2×10^3	0.7	.22	.75
TR-24	(100)	2.5	5×10^3	0.7	.80	1.8

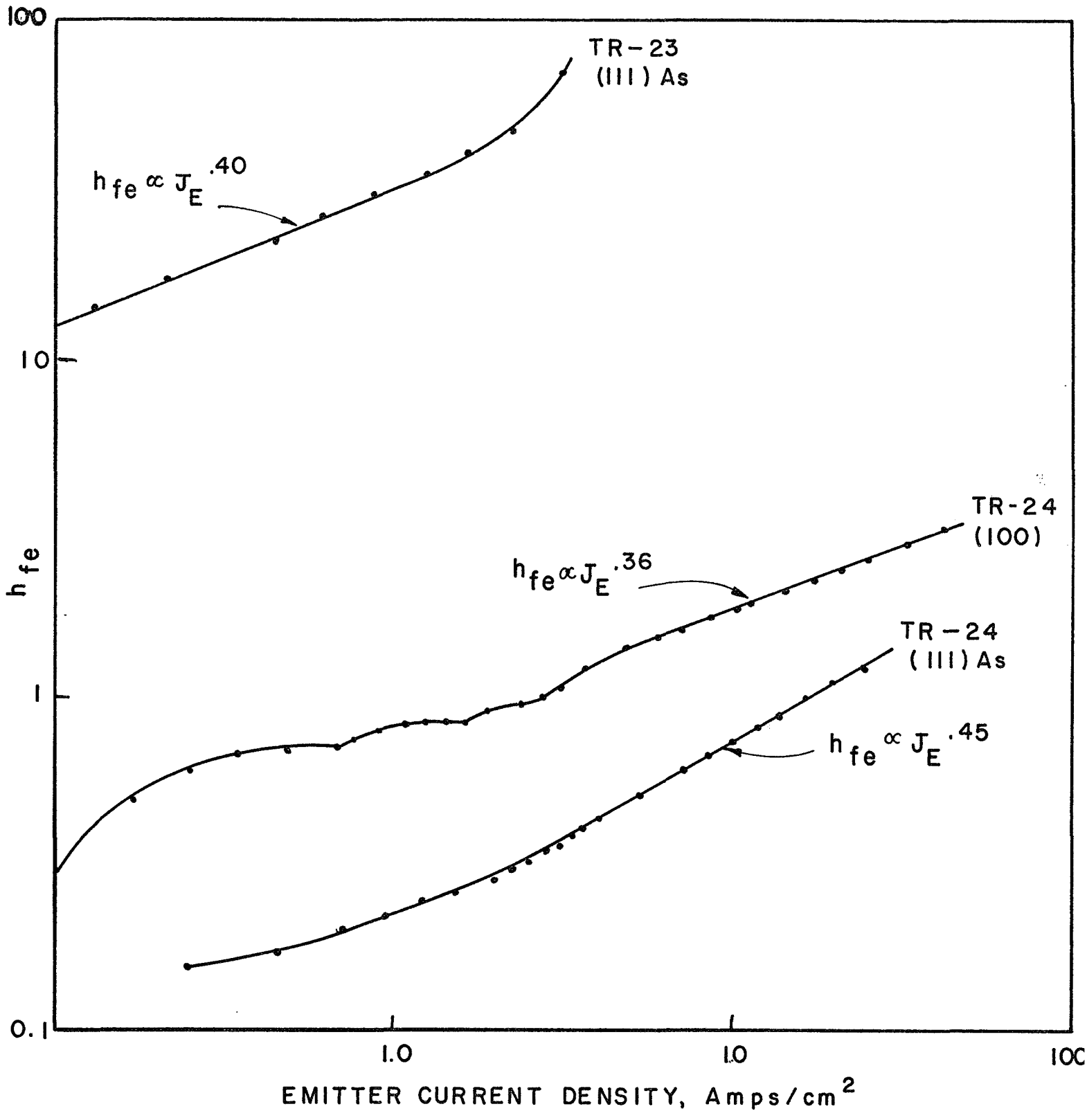


Fig. 10 Comparison of h_{fe} vs. J_E for TR-24 (100) and (111) As Orientations. High gain transistor TR-23 also included.

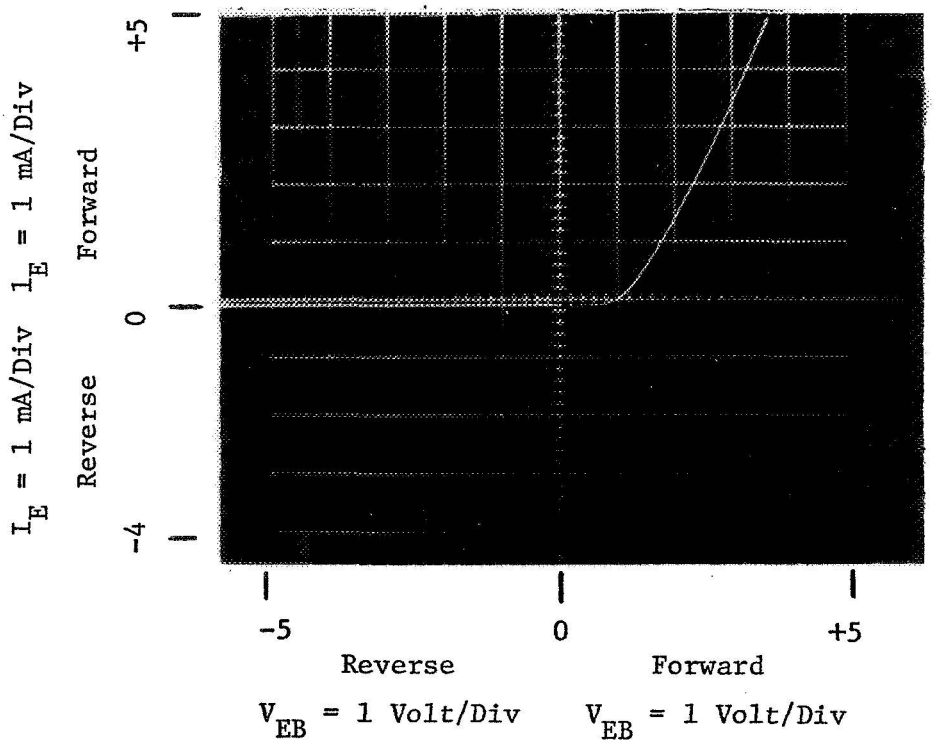
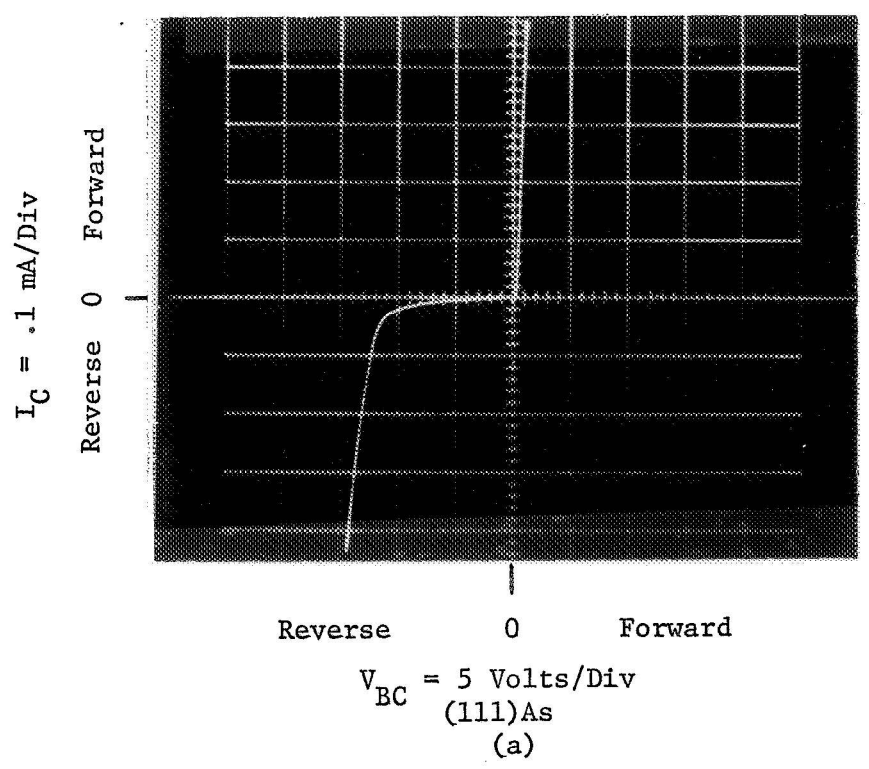


Fig. 11 Typical Emitter - Base characteristic obtained for TR-24 (111)As and (100) orientations. Reverse breakdown is soft at 30-35 volts.



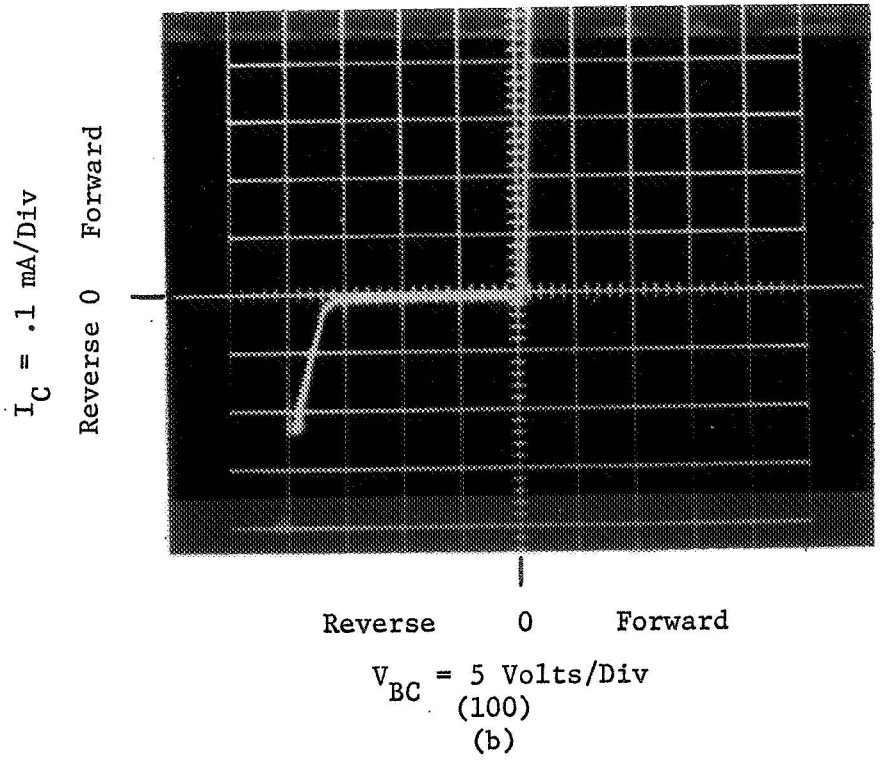
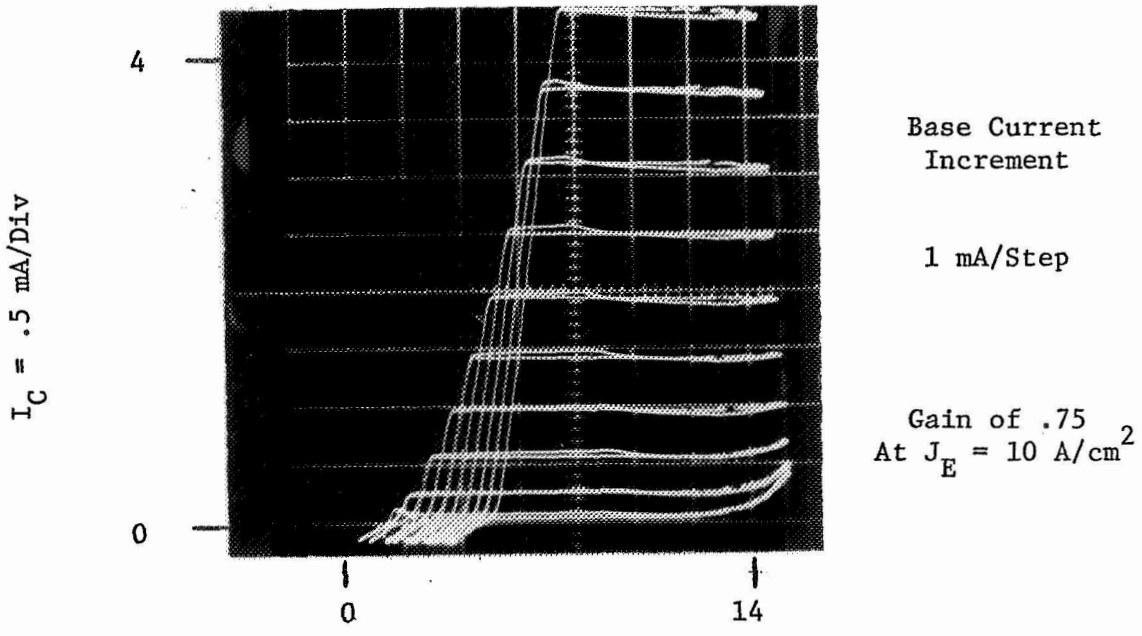
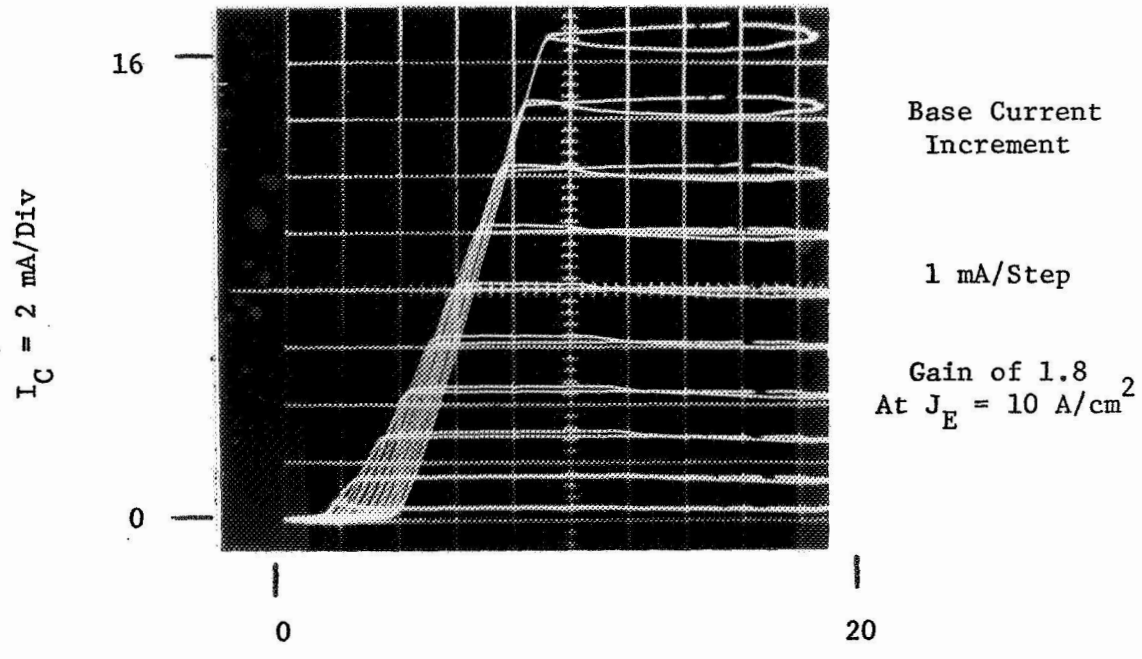


Fig. 12 Comparison of (111)As and (100) Base-Collector characteristics for TR-24.



(a) TR-24 (111)As



(b) TR-24 (100)

Fig. 13 Comparison of Common-Emitter characteristics of (111)As and (100) TR-24 Transistors.

4. ZnSe-GaAs TRANSISTORS USING EPITAXIAL GaAs

The use of commercially available epitaxial GaAs substrate material for ZnSe-GaAs transistors was examined, by a trial growth run, as a possible means of obtaining reduced interface dislocation formation and improved base lifetime. The highest gain GaAs homotransistors have almost always been reported on epitaxial material since it appears to have longer lifetimes, higher mobilities, and fewer defects than equivalently doped bulk material. The mobility of the material used in this study was twice that (manufacturer's claim) of the usual bulk material used. No information on lifetime could be obtained from the manufacturer (Monsanto). Table III shows the material characteristics supplied with the material. Substrate material was Czrochralski grown, Te doped. Although heavily Te doped GaAs is notorious for growth striations, doping non-uniformities, and precipitates, this epi-material was obtained since it was available. A wait of 4-6 months was anticipated if Sn or S doped n^+ substrate was ordered. The 1.4 μm n layer was the largest that the manufacturer could supply in (111)As orientation.

ZnSe was grown simultaneously upon (111)As and (100) epi GaAs. Growth morphology and growth rate was no different than that of bulk material. Transistors were made by the Zn diffusion-quench technique (650°C, 5 min.). This should give basewidth of 0.25-0.30 μm and a ZnSe resistivity of 10^3-10^4 ohm-cm. Gain for (111) transistors should be from 2-10. Table IV shows the resulting transistor characteristics.

The (100) transistor performed about a half to a third as well as a good (111) bulk transistor with the same basewidth and ZnSe resistivity. The (111)As Transistor of the epi-material however failed to work at all, possibly because of its large basewidth. The reason for the difference in (100) and (111) basewidths is not directly obvious. Although the n/n^+ dopings were the same, the n and n^+ growth runs (by the manufacturer) were different for each orientation. Thus, the number of defects in the two orientations could be considerably different. Preferential rapid diffusion of Zn in the (111)As sample may have occurred if defect densities were large. Note that the low collector-base reverse breakdown voltage could be the result of defects.

Table III Properties of Epitaxial n/n^+ GaAs used for ZnSe-GaAs Transistors

Orientation	(111) As	(100)
n doping, cm^{-3}	1.2×10^{16},Sn	1.4×10^{16},Sn
n^+ doping, cm^{-3}	2×10^{18},Te	2×10^{18},Te
n region thickness, μm	1.4	20.5
n region mobility, cm^2/volt.sec	4900	4750

Table IV Properties of Transistors made from Epitaxial GaAs Substrates

Orientation	(100)	(111)As
ZnSe Thickness, μm	2.5	2.5
ZnSe Resistivity, Ω-cm	5×10^3	10^5
Basewidth, μm	.3	.8
Gain at I_E=1.0A/cm^2	1.0	0
Base-Collector rev. Breakdown Voltage, Volts	15	2

Epitaxial (100) and (111)As material was examined for defects by cleaning in solvents and then immersing in the GaAs AB dislocation etch. (Prior to growth no polishing or etching was done on epitaxial material since n layers were thin and the surface was mirror smooth and scratch free.) Figs. 14 and 15 show the results. The (111)As sample is heavily dislocated (10^7-$10^8 cm^{-2}$ dislocations) while the (100) material appears to have $10^5 cm^{-2}$ dislocations. A scratch is also visible in the etched (111)As sample. The (100) sample also shows the now-familiar striation bands.

Although the dislocation etch removes about 10 μm of material before successfully revealing defects, it is apparent that the (111)As material is seriously faulted and should not be used for transistors. The (100) material has made the best (100) transistors so far seen using the Zn diffusion-quench technique.

5. SEARCH FOR LIGHT EMISSION FROM ZnSe-GaAs JUNCTIONS

In our last Quarterly Report we reported the absence of light emission from low resistance ZnSe-GaAs diodes pulsed to forward current densities as high as 5×10^4 A/cm^2. Failure of these devices to emit light was explained by proposing that the 900°C Zn diffusion step and the 650°C quench provided too many defect states in the GaAs band gap to allow radiative recombination transistors. This was supported by I-V data, since the forward current varies as $I_f \propto e^{AV_f}$ where A is temperature independent, implying a possible defect current transport mechanism with little electron injection into the GaAs.

It was proposed that ZnSe-GaAs diodes and transistors fabricated at lower temperatures (650°C) may prove to be better light emitters because (1) ZnSe-GaAs transistors show current gain indicating electron injection into GaAs and (2) less interfacial strain and misfit dislocations will be present so that non-radiative recombination centers are minimized. All injection and recombination is presumably in the GaAs since the large valence band discontinuity prevents hole injection into the ZnSe. Consequently, emitted radiation energy should be at or slightly less than the GaAs band gap (1.35 eV). The main problem with these devices is that the high ZnSe resistivity (10^3 ohm-cm) limits the maximum current density that can be applied.

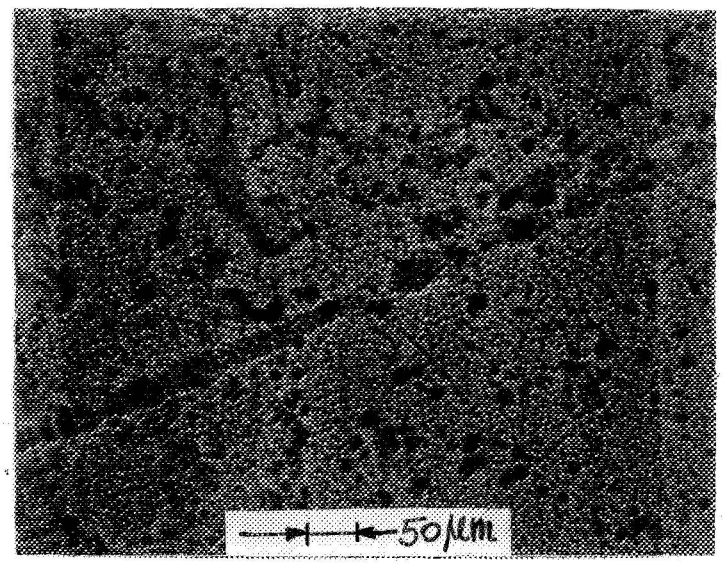


Fig. 14 (111)As Epi GaAs material after AB dislocation etch.

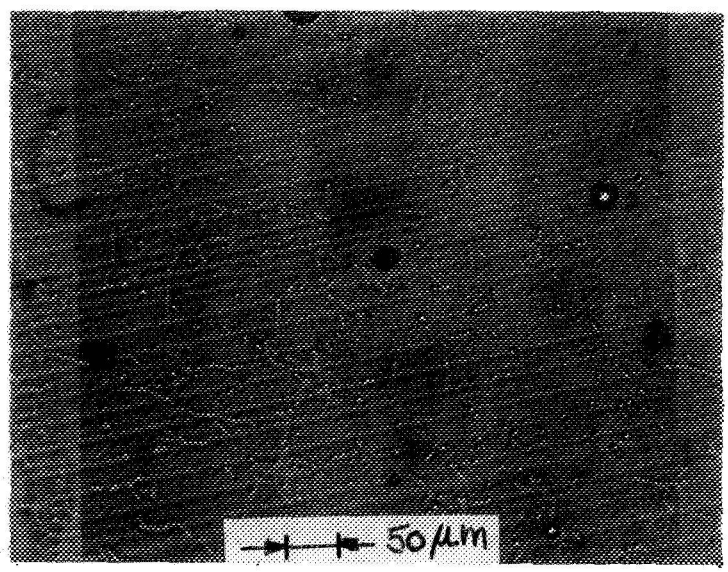


Fig. 15 (100)E_{pi} GaAs material after AB dislocation etch.

During this quarter we examined high-resistivity ZnSe-GaAs diodes and transistors for light emission. Devices were mounted flush with the front of a 7102 photomultiplier tube which has a S1 response (sensitive to 0.3 μm <wavelength<1.2μm). This tube was spot checked by inserting a GaP electroluminescent diode in front of it. The GaP diode was pulsed with and without a 10 mil thick GaAs filter between it and the PM tube. In both cases the PM tube was easily saturated indicating that it did respond to near GaP and GaAs band-gap radiation and was quite sensitive. When ZnSe-GaAs devices were placed in front of the PM tube and pulsed, light emission was nil. Maximum pulsed current densities ranged from 2×10^3 A/cm^2 to 5×10^4 A/cm^2 depending on the device.

Table V lists device properties and experimental parameters for the devices tested. ZnSe-GaAs diodes were fabricated by growing ZnSe upon (111)As bulk p-type GaAs (.03 ohm-cm, Zn), etching mesas (to reduce surface currents) and applying In contacts. ZnSe-GaAs transistors were also mesa etched and made by both the 650°C quench and Zn vapor-slow-cool methods. Note that both emitter-base and base-collector junctions were examined in transistors. This was done since recombination processes should be similar at both junctions because the basewidth is only 0.2-0.75 μm. The results from both junctions serve as a cross check on each other. However, no trace of light was observed from either junction. This indicates a non-radiative recombination mechanism in the base-collector region of the GaAs.

It is difficult to estimate the injection capabilities of the emitter and collector at the high current levels used. Transistor characteristics cannot be measured above I_B=20 mA due to large emitter resistance. However, since gain is seen, some injection is occurring. Gain and injection increase with I_E. Both emitter-base and collector-base forward I-V curves at low current are of the form $I_f \propto e^{AV_f}$ where I_f<1mA and A is nearly temperature independent which is suggestive of the absence of over-the-barrier injection. Yet some injection does occur at I_E<1mA (See TR-23 and TR-24 in Fig. 10 for an emitter area of 4×10^{-4} cm^2). Thus, I-V characteristics are not totally reliable for predicting injection ability.

Table V Summary of Properties of Devices Examined for Light Emission

Device	Method of ZnSe Doping	Junction Pulsed	Orientation	ρ ZnSe ohm-cm	h_{fe}	Basewidth μm	Effective cont.diameter mils	Max. Current Density A/cm^2	Max Current Amp
CS-61	Slow-Zn-cool	ZnSe-GaAs	(111)As	10^3	-	-	8	8×10^3	2
CS-61	Slow-Zn-cool	ZnSe-GaAs	(111)As	10^3	-	-	1/4-1/2	5×10^4	.05
TR-21	Quench	ZnSe-GaAs	(111)Ga	10^5	2	.75	1/4-1/2	2×10^4	.02
TR-23	Slow-Zn-cool	ZnSe-GaAs	(111)As	10^4	50	.25	1/2-1	5×10^3	.02
TR-23	Slow-Zn-cool	GaAs pn	(111)As	10^4	50	.25	4	1.5×10^4	2
TR-24	Slow-Zn-cool	ZnSe-GaAs	(100)	5×10^3	2	.70	8	2×10^3	.5
TR-24	Slow-Zn-cool	ZnSe-GaAs	(111)As	5×10^3	1	.70	8	2×10^3	.5
TR-24	Slow-Zn-cool	GaAs pn	100	5×10^3	2	.70	4	2.5×10^4	2
TR-24	Slow-Zn-cool	GaAs pn	(111)As	5×10^3	1	.70	4	2.5×10^4	2

Note: The ZnSe thicknesses were about 2.5 μm. The current pulse width was about 2 μsec

An attempt was made to measure the injection efficiency of the GaAs base-collector junction. Low injection efficiency may be part of the explanation for no light emission from this junction. The ZnSe-GaAs transistor was turned around so that the ZnSe was the collector, and the n-type GaAs was the emitter. In normal operation this transistor had a maximum gain of 2 at I_B=20 mA with basewidth 0.7 μm. With reverse operation a constant gain of 5×10^{-4} was found at base currents as high as 200 mA indicating that electron injection into the base region was low, even at high currents. Hole injection into the n type GaAs could not be checked, but since the base doping is larger than that of the collector (n GaAs), hole injection is favorable and this along with defects may be responsible for the low electron injection.

Since most reports indicate that electron injection on the p side of GaAs diodes is responsible for good injection electroluminescence, the low electron injection abilities of the base-collector junction may be responsible for the lack of light emission. Also dislocation induced states in the band gap may provide an abundance of non-radiative recombination paths.

Returning to Table V one notes that some devices had very small effective contact diameters which lead to high current densities ($2 - 5 \times 10^4$ A/cm^2) for currents of 20-50 mA. Even under these conditions no light was observed. If more current was applied, the ZnSe broke down and remained a dead short. Fig. 16 shows the ZnSe contact area of a shorted diode after the 10 mil In dot was removed. The circular ring represents the periphery of the contact area while the dark spots are shorted ZnSe. It is believed that, although the contact physically covered the area inside the ring, electrical contact was made only where the ZnSe shorted out. At high current densities the ZnSe broke down due to excessive electric field, even when 40 pps - 0.5 μs pulses were applied (indicating that this is not a heating effect). This problem was remedied by In alloying at 325°C-350°C for 20 sec. rather than the normal 300°C for 10 sec. Electrical contact area then corresponded to physical contact area, and no ZnSe shorting occurred. This new contacting procedure will be employed on all future devices.

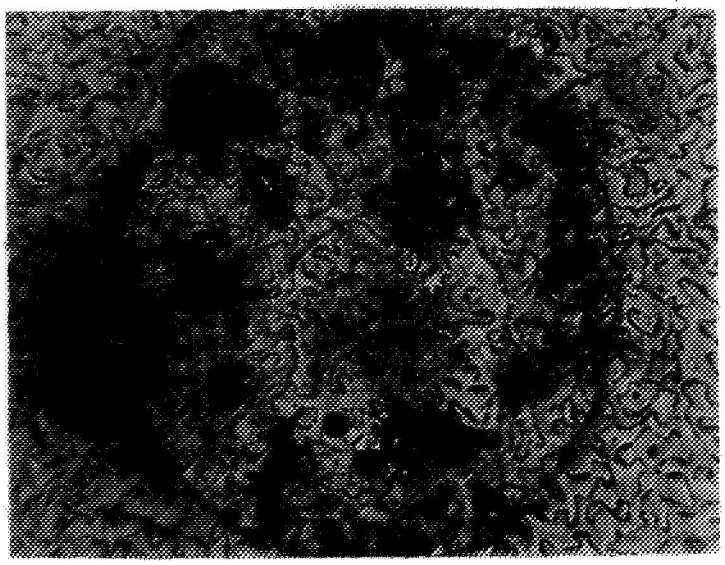


Fig. 16 ZnSe Contact Area After Pulsing to 50 mA (TR-21) 50X.

6. OTHER GROWTH STUDIES WITH THE HCl TRANSPORT SYSTEM

a) Growth of ZnS Upon GaP

The growth of ZnS upon (111)B oriented GaP was successfully accomplished using the HCl close-spaced system. This closely parallels our previous success with ZnSe grown upon GaP. Although ZnS crystallizes in the hexagonal structure, its lattice match to cubic GaP is quite good for (111), (0001) growth planes (.5% mismatch). Fig. 17 shows the ZnS growth morphology for the growth conditions listed below.

Seed (GaP) Temp.	650°C
Source (ZnS) Temp.	780°C
HCl Conc.	.04%
Growth Rate	3.0 μm/hr.
ZnS Thickness	3.5 μm
Source ZnS Doping	10^{18} Ga/cm^{-3}
Seed GaP Doping	2×10^{17} Zn/cm^{-3}
Grown ZnS Resistivity	10^{8} ohm-cm

The grown layer could be selectively removed with concentrated HCl revealing a smooth etch-free GaP surface similar to that before growth. This is shown in Fig. 18. Note that the HCl has revealed interfacial strain lines in the GaP, indicating that this heterojunction pair is under considerable strain and may not be able to undergo any rapid temperature variations without cracking. However no cracks were observed in the ZnS grown layer that we obtained.

The ZnS resistivity, as-grown, is very high since ZnS behaves as ZnSe does and achieves almost complete Zn vacancy compensation of donors at growth temperatures. An attempt was made to reduce as-grown ZnS resistivity by passing zinc vapor over the grown layer as it slowly cooled in the growth system. This is the same method described in the ZnSe-GaAs transistor section. It produced ZnS layers with resistivities between 10^{5} - 10^{6} ohm-cm, indicating either that (1) the Zn step is not efficient in removing Zn vacancies; (2) the Ga source ZnS dopant is not transporting; or (3) acceptor impurities in the ZnS source are readily transporting and compensating the donors. With regard to possibility (1) we know relatively little about the temperature required for removal of Zn vacancies from ZnS and it remains to be examined whether it might be

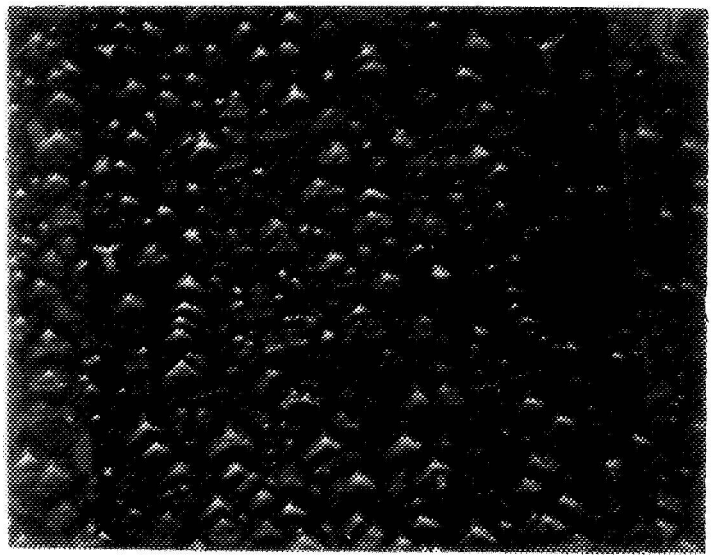


Fig. 17 ZnS As-Grown Surface (Cs-58, 250X)

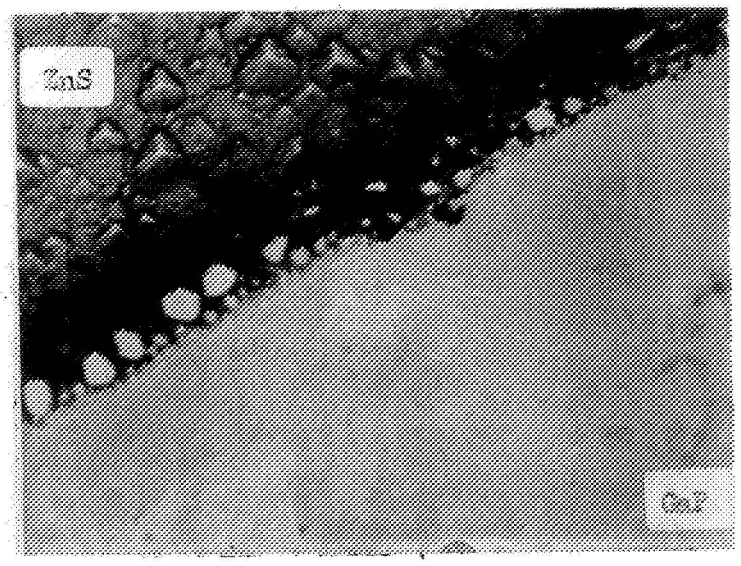


Fig. 18 ZnS-GaP interface with the ZnS partially removed (Cs-58, 250X)

higher than for zinc vacancy suppression in ZnSe. On the other possibilities, involving dopant transportation, several things may be tried. The ZnS source was not gettered in Zn to remove residual acceptor impurities. In the future this will be done, and the improvement in grown ZnS resistivity noted. Also it is a well known fact that Ga is a deep-donor in ZnS whereas Al is a shallow donor. Consequently future runs will also be done with gettered Al-doped ZnS sources. Al does not transport with ZnSe, but there is always a chance that ZnS may prove more successful.

We hope to make more ZnS/GaP growths during the next quarter and evaluate their electrical properties.

b) Growth of ZnTe upon GaSb

Two attempts were made to grow pZnTe upon nGaSb in the HCl close-spaced system. ZnTe and GaSb have an excellent lattice match (.13% mismatch) and the ZnTe retains its p type conductivity after heating (i.e. Zn vacancies contribute to conductivity rather than causing a severe autocompensation effect as in ZnSe and ZnS). However the two attempts at growth were failures. Although the GaSb was protected by SiO_2 on its five non-growth faces, severe etching occurred at seed temperatures of 550°C and 650°C. At the corresponding source temperatures of 670°C and 780°C 6 μm of ZnTe was etched away and mostly deposited on the blocks around the GaSb but not on it. GaSb etching was too severe to allow growth.

Successful growth of ZnTe upon GaSb in the HCl close-spaced system is doubtful. The very lowest HCl concentrations (.02-.04%) were used for the two runs to minimize the etching of the seed if HCl is responsible for it. The seed temperature was lowered to 550°C with serious etching still occurring. Lower seed temperatures will probably not reduce the etching problem enough since the amount of etching does not appear to be decreasing (etching of GaSb was as pronounced at 550°C as at 650°C). Furthermore, lower seed temperatures increase the probability of polycrystalline growth and necessitate lower source temperatures lowering the etch rate of ZnTe. Lower HCl concentrations are not feasible without gross modification of the growth system.

From other growth studies with ZnTe not involving HCl we have found etching of various substrates to occur. Therefore it appears possible that Te from the ZnTe could be the agent responsible for etching of the GaSb. We have discontinued these growth attempts.

7. LOW TEMPERATURE GROWTH OF Ge ON GaAs BY IODINE TRANSPORT

During this quarter work was completed on altering and recharging of the iodine source column. In the final growth runs of the last quarter it had become apparent that the iodine vapor was not coming to equilibrium saturation in the carrier gas stream before passing to the hydrogen iodide converter. This resulted in lower growth rates and accompanying higher dopant incorporation into the grown layers. Before the column was removed from the system, however, a series of manometer measurements were made to determine the pressure of the carrier gas mixture at the dopant flow meter tap-off on the low pressure side of the hydrogen and helium needle valves. These measurements have been used to calibrate the dopant carrier flow as a function of the main flows. Previously dopant flows had been set assuming independence from the main carrier flow rates; these measurements indicate an interdependence of these flows, particularly at lower dopant flow readings. Since most runs have been made at a single set of carrier flows and dopant flows above the range of strong interdependence, this effect had been neglected.

The iodine column was removed from the system, the remnants of the first iodine charge dissolved from it, and the pyrex filler beads removed. A thermocouple tube running the length of the column was broken at one end and was repaired. After winding of the column heater, the column was cleaned and reinstalled. A visual check of the source germanium showed it to be present in adequate amount. Following this a leak check showed the column to be tight. The new charge of 1 kilogram iodine was loaded with its filler beads and the filling tube sealed. The column was then evacuated for two hours to remove water vapor picked up by the iodine during loading. Heating of the hydrogen iodide converter to 80°C prevented appreciable iodine diffusion from the column while allowing water vapor to be pumped out. This is possible since the vapor pressure of water is 30 to 80 times that of iodine at the temperatures involved.

A purging run was then made to bring the column up to pressure and to bring the surface of the germanium to growth cleanliness. Two undoped runs were made with growth rates comparable to that of the previous fully charged column but with a resistivity substantially lower than the best previous undoped growths. It was also apparent visually that all the water vapor had not been purged from the column. With a further purging run, it became apparent that a gross leak had developed; a closer inspection showed that the bottom of the pyrex column had been cracked half way around. It is thought that an omitted annealing step when the thermocouple tube repair was made along with the impact of the pyrex beads and iodine falling the length of the column during loading caused a small crack which was further enlarged with the thermal cycling of the column during each successive run.

As a result of these experiences, a new column was fabricated entirely of quartz with a quartz hydrogen iodide converter attached and quartz-to-pyrex graded joints to the pyrex inlet and outlet valves. The new column was identical in design to the previous one with the converter placed at a greater distance from the column to reduce internal transport of iodine from the hotter to the cooler inner wall sides. After heaters were wound, the column was wrapped in an insulating jacket to aid in the same reduction. Following cleaning and leak checking of the new column, a fresh supply of beads and a new 1 kilogram charge of iodine was loaded in such a way as to prevent the first material from impacting the bottom of the column. After the filler tube of this column was sealed with a quartz plug, the column was evacuated as before (with the hydrogen iodide converter at 80°C) and left being pumped on overnight to remove the last traces of water vapor.

A purging run was followed by an undoped growth run which again gave a growth rate indicative of a carrier gas flow saturated with iodine vapor. The resistivity of this growth was 0.5 ohm cm (n-type) which approaches the best previous undoped growths. Material has been polished in preparation for following doped growths. In addition, a sampling oscilloscope is being incorporated into a set-up for pulse injection/recovery measurements on previously grown and fabricated diodes.